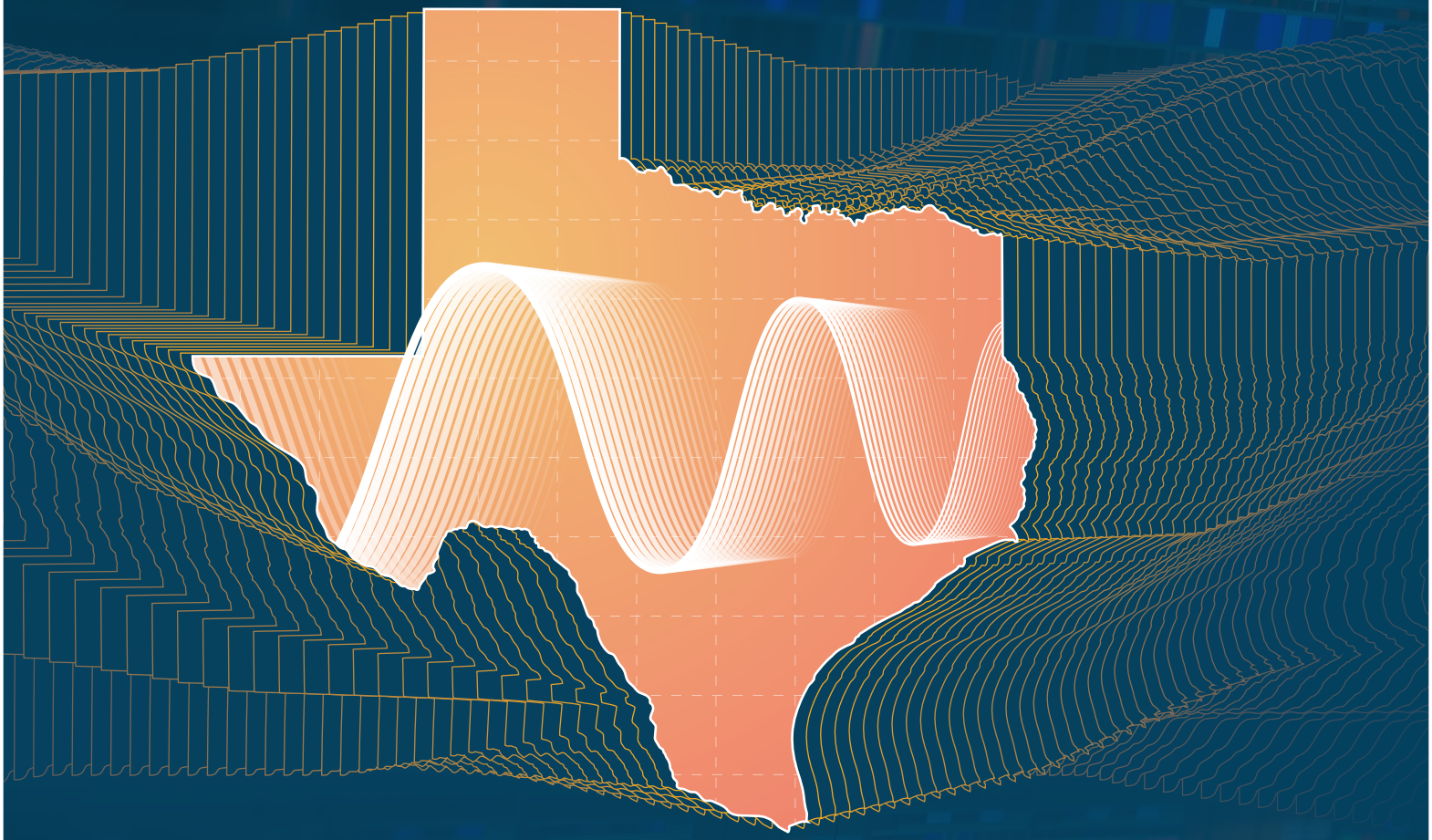
TEXAS ANALOG CENTER OF EXCELLENCE

ERIK JONSSON SCHOOL OF ENGINEERING AND COMPUTER SCIENCE



Annual Report 2018 – 2019

SRC®

TxACE TEXAS ANALOG CENTER OF EXCELLENCE

50 YEARS

THE UNIVERSITY OF TEXAS AT DALLAS

TxACE MISSION

The Texas Analog Center of Excellence seeks to create fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, health care, and public safety and security.

TxACE THRUSTS

- *Safety, Security and Health Care*
- *Energy Efficiency*
- *Fundamental Analog Circuits*

TxACE 2018-2019 ANNUAL REPORT

The Texas Analog Center of Excellence (TxACE), located at the University of Texas at Dallas is the largest analog research center based in an academic institution. Analog and mixed signal integrated circuits engineering is both a major opportunity and challenge. Analog circuitry is a critical component of the majority of products for the $450+ billion per year integrated circuits industry, as a part of sensing, actuation, communication, power management and others. Digital integrated circuits such as microprocessors, logic circuits and memories are now integrating analog functions such as input/output circuits, phase locked loops, temperature sensors and power management circuits. It is also common to find microcontrollers with multiple analog-to-digital and digital-to-analog converters. These circuitries impact almost all aspect of modern life: safety security, health care, transportation, energy, entertainment and others.

Creation of advanced analog and mixed signal circuits and systems depends on the availability of engineering talent for analog research and development. TxACE was established to help translate the opportunity into economic benefits by overcoming the challenge and meeting the need. TxACE was established through a collaboration of the state of Texas, Texas Instruments, the Semiconductor Research Corporation, the University of Texas System, and The University of Texas at Dallas.

The research tasks are organized into three research thrust areas: Safety, Security and Health Care, Energy Efficiency and Fundamental Analog. The scope of investigation extends from circuits operating at dc through terahertz, data converters that sample at a few samples/sec to 10's of Giga-samples/sec, AC-to-DC and DC-to-AC converters working at µW to Watts, energy harvesting circuits, sensors and many more. Significant improvements to existing mixed signal systems and new applications have been made and continued to be anticipated. Students who have been exposed to hands-on innovative research are forming the leading edge of analog talent flow into the industry. Close collaboration with and responsiveness to industry needs provide focus to the educational experience.

DIRECTOR'S MESSAGE

The Texas Analog Center of Excellence (TxACE) is leading analog research and education. Last year, the Center together with SRC, its member companies and other agencies has brain stormed to define the research directions for the 2nd decade. There are broad interests in advanced sensors, analog-digital mixed signal hybrid computing to improve energy efficiency of artificial intelligence, security of mixed signal hardware, and using these technologies to foresee the future to prevent failures or mitigate their impact. This consensus will help enhance existing research and broaden our research, and help accomplish our mission of creating fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, health care, and public safety and security.

Over the past year, TxACE researchers published 23 journal and 58 conference papers. We also filed 9 patent applications and 1 invention disclosure, and were granted 1 patent. Fourteen Ph.D. and nine M.S. students have completed their degree program. The Center funded 57 research tasks led by 60 principal investigators at 27 institutions, including three international universities. The Center supported 184 graduate and undergraduate students.

The Center is continuing to excel in research. There are always too many accomplishments to list all here. A selected list includes increasing the bandwidth of noise shaping SAR ADC by 2X using time interleaving, demonstration of a 3-GHz 8X clock multiplier that achieves the integrated jitter of 138 fs,rms and -249 dB FoM, generation of 180-GHz MSK signals with 10-Gbps data rate which is 5X higher than that for the state of art at 3X higher carrier frequency, demonstration of mm-wave CMOS power amplifier (28 GHz to 39 GHz) with active impedance tuning that achieves P_{sat}>19dBm and PAE_{peak}>20%, and can tolerate changes of load impedance, and demonstration of a tool that can localize a design bug to a specific circuit module.

The TxACE laboratory is continuing to help advance integrated circuit research by making its instruments and expertise available to researchers and our industrial partners all over the world.

I would like to thank the students, principal investigators and staff for their efforts, and UT Dallas, the University of Texas System, TI, and SRC, as well as many friends of TxACE all over the world for their generous support. I look forward to another year of working with the TxACE team to make our world better through our research, education and innovation.

Kenneth K. O, Director TxACE
Texas Instruments Distinguished
University Chair Professor
The University of Texas at Dallas

BACKGROUND & VISION

The $450+ billion per year integrated circuits industry is evolving into an analog/digital mixed signal industry. Analog circuits are providing or supporting critical functions such as sensing, actuation, communication, power management and others. These circuits impact almost all aspect of modern life including safety, security, health care, transportation, energy, and entertainment. To lead this change, in particular to lead analog and mixed signal technology education, research, commercialization, manufacturing, and job creation, the Texas Analog Center of Excellence was announced by Texas Governor Rick Perry in October 2008 as a collaboration of the Semiconductor Research Corporation, state of Texas through its Texas Emerging Technology Fund, Texas Instruments Inc., University of Texas system and University of Texas at Dallas. The Center seeks to accomplish the objectives by creating fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, healthcare, and public safety and security as well as by improving the research and educational infrastructure.

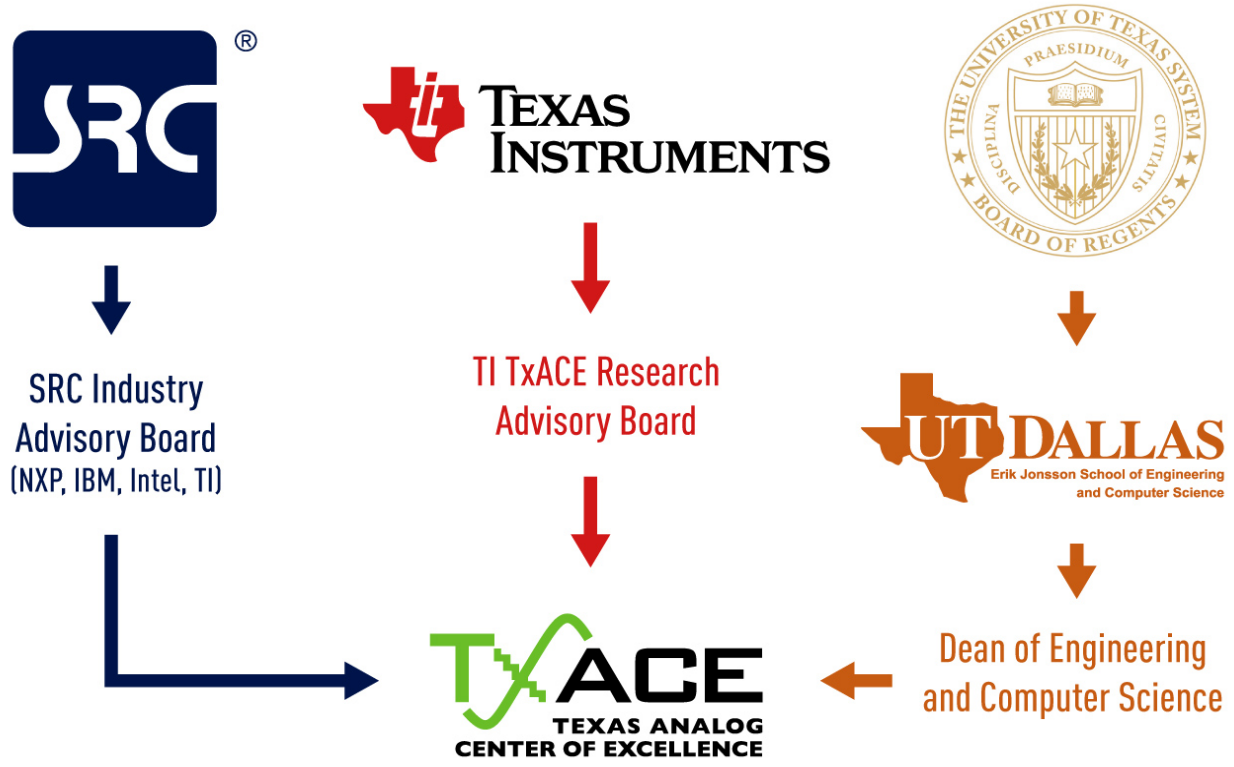


Figure 1. TxACE organization relative to the sponsoring collaboration (2018-2019).

CENTER ORGANIZATION

The Texas Analog Center of Excellence is guided by agreements established with the Center sponsors. Members of the industrial advisory boards identify the research needs and select research tasks in consultation with the Center leadership. Figure 1 diagrams the relationship of TxACE to the members of the sponsoring collaboration.

The internal organization of the Center is structured to flexibly perform the research mission while fully embracing the educational missions of the Universities.

Figure 2 shows the center management structure. The TxACE Director is Professor Kenneth O. The research is arranged into three thrusts that comply with the center mission: Safety, Security and Health Care, Energy Efficiency and Fundamental Analog Research. The third thrust consists of vital research that cuts across the first two research thrusts. The thrust leaders are Prof. Yiorgos Makris of the University of Texas at Dallas for safety, security and health care, and Prof. Ali Niknejad of the University of California, Berkeley for energy efficiency. The leader for fundamental analog is Prof. Pavan Hanumolu of University of Illinois, Urbana-Champaign. The thrust leaders along with Professor Dongsheng Ma of the The University of Texas at Dallas form the executive committee. The committee, along with the director, forms the leadership team that works to improve the research productivity by increasing collaboration, better leveraging the diverse capabilities of principle investigators of the Center, and lowering research barriers. The leadership team also identifies new research opportunities for consideration by the Industrial Advisory Boards.

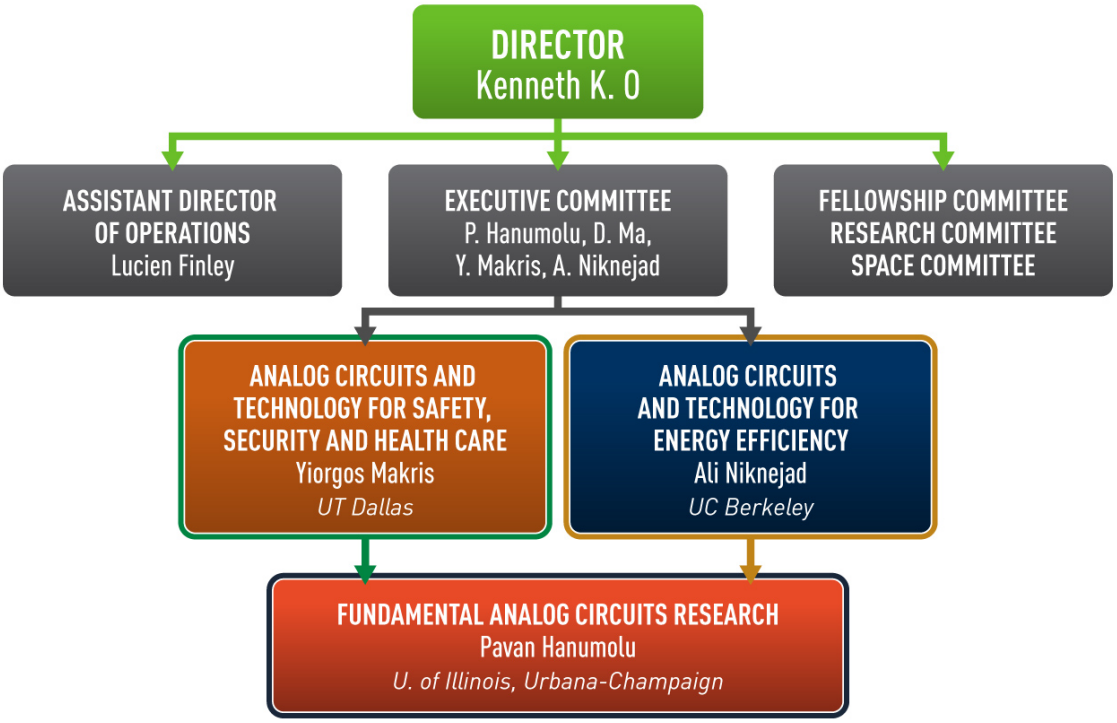


Figure 2. TxACE organization for management of research

SAFETY, SECURITY & HEALTH CARE

(Thrust leader: Yiorgos Makris, University of Texas at Dallas)

TxACE is developing analog technologies that enhance public safety and security, and health care. The thrust is working to reduce the cost of millimeter wave imaging and on-vehicle radar technology for automotive safety by researching signal processing techniques that reduce system complexity and transmitter architecture that can efficiently adapt to changing antenna characteristics. This thrust is also investigating vibration sensors, CO_2 sensors and sensing techniques to monitor health of motors and mixed signal circuits including power devices, as well as, sensor fusion techniques that can enable monitoring behaviors of a driver in an automobile. This thrust also includes research tasks on mixed signal hardware security utilizing machine learning techniques.

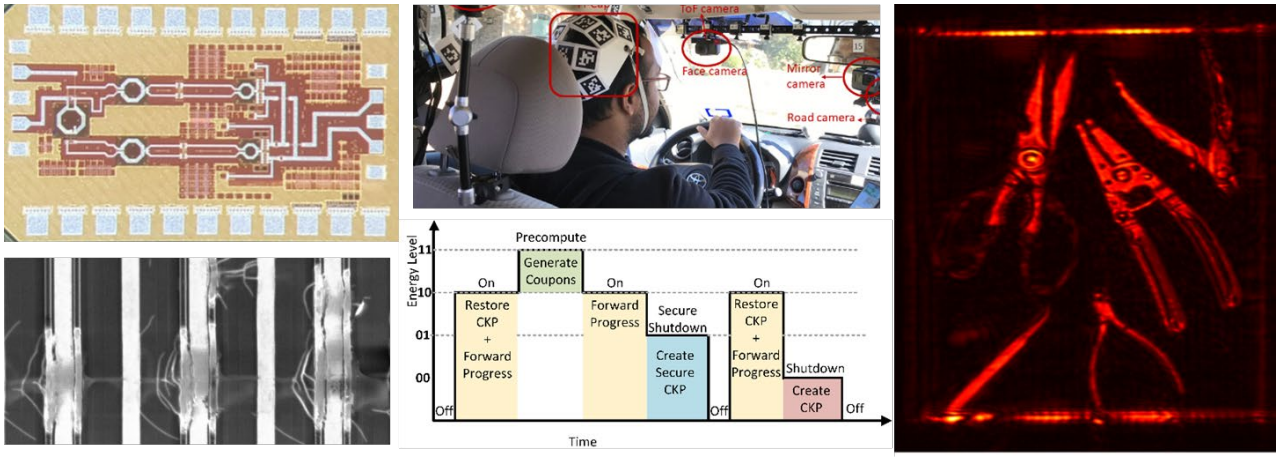


Figure 3. (Top left) Reconfigurable mm-Wave transmitter with active impedance synthesis using a multi-port node-conjugated combiner (K. Sengupta, Princeton), (Top center) A driver wearing a Fi-Cap, a helmet with fiducial markers designed for head pose estimation (C. Busso, UT Dallas), (Bottom left) SEM image of a failed E-mode GaN HEMT, showing electrical discharge and cracks on the gate/source side (M. Kim and S. Shichijo, UT Dallas), (Bottom center) Energy level indicator used to realize secure intermittent microprocessor architecture. A 2-bit indicator is used to adapt the computations of the load based on the availability of energy in the energy storage unit, such as a super capacitor (P. Schaumont, Virginia Tech), (Right) Image formed using a commercial 77-GHz CMOS radar module (M. Torlak, UT Dallas).

ENERGY EFFICIENCY

(Thrust leader: Ali Niknejad, UC Berkeley)

TxACE is committed to alleviate the global energy problem by improving the energy efficiency of electronic systems as well as by developing analog technologies that can make energy generation, distribution and utilization more efficient. The Center is also working to energize and power long-lasting in-situ microscale devices such as wireless microsensors, biomedical implants, and portable microelectronics. The research in this thrust includes power converters, co-optimization of converters and regulators with systems powered by them, I/O with power consumption that scales with the data rate, optimization of TSV placement for thermal management, efficient drivers for a power stage with reduced EMI, ultra low-power analog to digital converters, ultra-capacitors formed using carbon nano-tubes, a fast start-up crystal oscillator with reduced power consumption, built-in self-test for power management IC's, System-In-Package energy harvester and others.

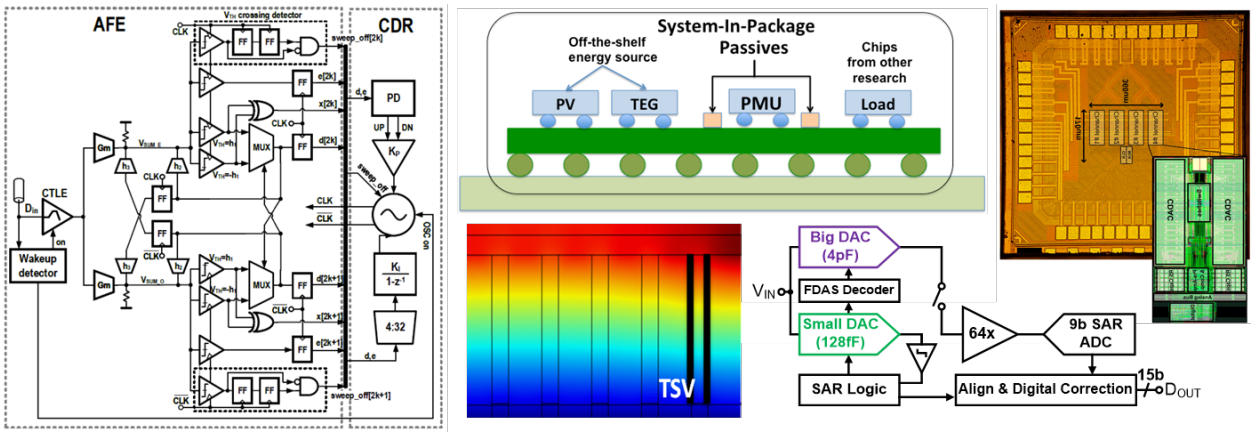


Figure 4. (Left) Baud rate receiver for energy efficient I/O (P. Hanumolu, UIUC), (Top center) System-in-package energy harvester (S. Mukhopadhyay, Georgia Tech.), (Bottom center) Simulated cross-sectional temperature distribution with TSV's (J. Lee, N. Bagherzadeh, UC-Irvine), (Right) The first interleaved noise-shaping SAR ADC. It also uses for the first time a four-stage ring amplifier (M. Flynn, U. of Michigan).

FUNDAMENTAL ANALOG CIRCUITS RESEARCH

(Thrust leader: Pavan Hanumolu, U. of Illinois Urbana-Champaign)

Research in this thrust focuses on cross-cutting areas in analog and mixed signal circuits which impact all of the TxACE application areas (Energy Efficiency, Public Safety and Security, Health Care). The list of research includes design of a wide variety of analog-to-digital converters, communication links, temperature sensors, I/O circuits, noise reduction techniques, new amplifier topologies suitable for use in nano-scale CMOS, development of CAD tools and testing of integrated circuits.

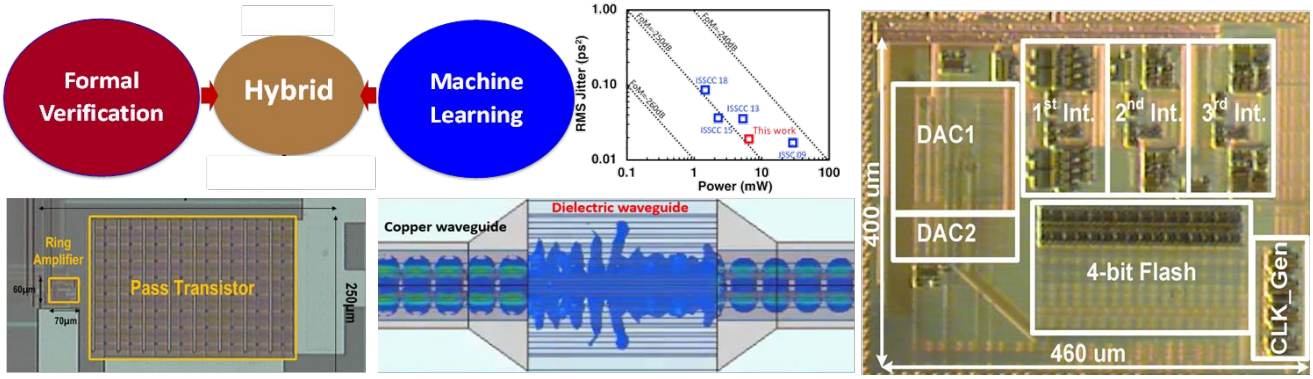


Figure 5. (Top left) Hierarchical analog and mixed-signal verification using hybrid formal and machine learning techniques (P. Li, UC Santa Barbara), (Top center) Performance of new clock multiplier architecture that is immune to frequency drift (A. Niknejad, UC Berkeley), (Bottom left) Ring amplifier based LDO (U. Moon, Oregon State U.), (Bottom center) Simulation of fields inside transitions and a dielectric waveguide (R. Henderson, UT Dallas), (Right) 3rd order continuous-time delta-sigma modulator with excess loop delay compensation using digital information stored on the input parasitic capacitance of a comparator (Nima Maghari, U. of Florida).

TXACE ANALOG RESEARCH FACILITY

The centralized group of laboratories of the Texas Analog Center of Excellence dedicated to analog engineering research and training occupy a ~ 8000-ft2 area on the 3rd floor of the Engineering and Computer Science North building (Figure 6). The facility includes RF and THz, Integrated System Design, Embedded Signal Processing, and Analog & Mixed Signal laboratories as well as CAD/Design laboratory structured to promote collaborative research**.** The unique instrumentation capability includes network analyses and linearity measurements up to 325 GHz, spectrum analysis up to 120 THz, and cryo-measurements down to 2^{o}K. The Center also added a pulsed multiple harmonic load and source pull measurement set up (up to 60 GHz for the third harmonic) and a 325-GHz antenna measurement set up. The close proximity of researchers in an open layout enables natural interaction and compels sharing of knowledge and instrumentation among the students and faculty. The TxACE analog research facility is one of the best equipped electronics laboratories. The laboratory is available for use by TxACE researchers and industrial partners all over the world.

Figure 6. TxACE Analog Research Facility

RESEARCH PROJECTS AND INVESTIGATORS

The Texas Analog Center of Excellence (TxACE) is the largest university analog technology center in the world. Table 1 lists the current principal investigators of the 57 tasks from 27 academic institutions funded by TxACE. Four universities (SMU, Texas A&M, UT Austin, UT Dallas) are from the state of Texas. Twenty are from outside of Texas. Three (Delft University of Technology, University of Twente, and Indian Institute of Tech. Kharagpur) (Figure 7) are from outside of the US. Of the 60 investigators, 21 are from Texas. During the past year, the Center supported 147 Ph.D., 22 M.S., 14 B.S., and 1 high school student. Fourteen Ph.D. and nine M.S. degrees were awarded to the TxACE students.

Investigator	Institution	Investigator	Institution	Investigator	Institution
B. Akin	UT Dallas	J. Hu	Texas A&M	S. Pourkamali	UT Dallas
N. Al-Dhahir	UT Dallas	M. Johnston	Oregon State	S. Prasad	UT Dallas
S. Ang	U Arkansas	C. Kim	U Minnesota	R. Rohrer	SMU
N. Bagherzadeh	UC Irvine	M. Kim	UT Dallas	E. Rosenbaum	UIUC
S. Bhunia	U Florida	G. Lee	UT Dallas	A. Sanyal	U Buffalo
D. Blaauw	U Michigan	J. Lee	UC Irvine	V. Sathe	U Washington
C. Busso	UT Dallas	P. Li	Texas A&M	P. Schaumont	Virginia Tech
A. Chatterjee	Georgia Tech	B. D. Ma	UT Dallas	K. Sengupta	Princeton
D. Chen	Iowa Sate	D. MacFarlane	SMU	M. Seok	Columbia
Y. Chen	Duke University	N. Maghari	U Florida	H. Shichijo	UT Dallas
Z. Chen	U Arkansas	K. Makinwa	Delft University	N. Sun	UT Austin
P. Dasgupta	Indian Inst. Tech	Y. Makris	UT Dallas	M. Swaminathan	Georgia Tech
W. Eisenstadt	U Florida	Y. Mengüç	Oregon State	D. Sylvester	U Michigan
M. Flynn	U of Michigan	U. Moon	Oregon State	G. Temes	Oregon State
R. Geiger	Iowa Sate	S. Mukhopadhyay	Georgia Tech	S .Thompson	U Florida
P. Gui	SMU	B. Nauta	U Twente	M. Torlak	UT Dallas
P. K. Hanumolu	UIUC	A. Niknejad	UC Berkeley	A. Trivedi	U Illinois, Chicago
R. Harjani	U Minnesota	K. K. O	UT Dallas	X. Zhang	Wash., St. Louis
A. Hazra	Indian Inst. Tech.	S. Ozev	Arizona State		
R. Henderson	UT Dallas	S. Palermo	Texas A&M		
S. Hoyos	Texas A&M	S. Pamarti	UCLA		

Table 1. Principal Investigators (May 2018 through April 2019)

Figure 7. Member Institutions of Texas Analog Center of Excellence

SUMMARY OF RESEARCH PROJECTS

The 57 research projects funded through TxACE during 2018-2019 are listed in Table 2 below by the Semiconductor Research Corporation task identification number.

	Task	Thrust	Title	Task Leader	Institution
1	**1836.153**	EE	High-Speed Compact Power Supplies for Ultra-Low-Power Wireless Sensor Applications	Ma, D. Brian	UT Dallas
2	**1836.155**	SS	Development of Wide-Band Vibration Sensors	Pourkamali, Siavash	UT Dallas
3	**1836.158**	FA	Development of Dielectric Waveguides for THz Radiation Applications	MacFarlane, Duncan	SMU
4	**2712.002**	EE/SS	On-line Self-Testing and Self-Tuning of Integrated Voltage Regulators	Mukhopadhyay, Saibal	Georgia Tech
5	**2712.003**	SS	Multi-Modal BIST Design and Test Metrics Evaluation for Analog/RF Circuits	Ozev, Sule	Arizona State
6	**2712.004**	FA	Hierarchical Analog and Mixed-Signal Verification Using Hybrid Formal and Machine Learning Techniques	Li, Peng	Texas A&M
7	**2712.005**	FA	Automated Cross-Level Validation and Debug of Mixed-Signal Systems in Top-Down Design: From Pre-Silicon to Post-Silicon	Chatterjee, Abhijit	Georgia Tech
8	**2712.006**	EE	Robust, Efficient All-Digital SIMO Converters for Future SOC Domains	Sathe, Visvesh S.	U. Washington
9	**2712.007**	EE	High-Resolution Low-Voltage Hybrid ADCs for Sensor Interfaces	Flynn, Michael P.	U. Michigan
10	**2712.008**	EE	Direct-Battery-to-Silicon Power Transfer in Advanced Nanometer CMOS	Harjani, Ramesh	U. Minnesota
11	**2712.009**	EE	Low Power Area Efficient Flexible-rate Energy Proportional Serial Link Transceivers	Hanumolu, Pavan Kumar	UIUC
12	**2712.010**	FA	Ringamp-assisted Circuits/Techniques and Next-generation Ringamps	Moon, Un-Ku	Oregon State
13	**2712.011**	FA	Robust Reliable and Practical High Performance References in Advanced Technologies	Geiger, Randall L.	Iowa State
14	**2712.012**	EE	EDAC and DCDC-Converter Co-Design for Addressing Robustness Challenges in Emerging Architectures	Seok, Mingoo	Columbia

	Task	Thrust	Title	Task Leader	Institution
15	**2712.013**	SS	Reconfigurable MM-Wave Tx Architecture and Antenna Interface with Active Impedance Synthesis in Multi-Port Node-Conjugated Combiner	Sengupta, Kaushik	Princeton
16	**2712.014**	FA	Leveraging CMOS Scaling in High Performance ADCS	Maghari, Nima	U. Florida
17	**2712.015**	SS	Area-Efficient On-Chip System-Level IEC ESD Protection for High Speed Interface ICs	Chen, Zhong	U. Arkansas
18	**2712.016**	EE	3D IC Thermal Management Based on TSV Placement Optimization and Novel Materials	Lee, Jaeho	UC Irvine
19	**2712.017**	SS	Mitigating Reliability Issues in Analog Circuits	Kim, Chris H.	U. Minnesota
20	**2712.018**	SS/EE	Test Techniques to Approach Several Defect-per-billion for Power ICs	Eisenstadt, William R.	U. Florida
21	**2712.019**	SS/EE	Pre-computed Security Protocols for Energy Harvested IoT	Schaumont, Patrick	Virginia Tech
22	**2712.020**	EE	Low-Power Mostly Digital Time-Domain Delta-Sigma ADCs for IoT	Sanyal, Arindam	U. Buffalo
23	**2712.021**	SS	Distributed Silicon Circuits and Sensors in 3D-Printed Systems for Wearable IoT Sensors	Johnston, Matthew	Oregon State
24	**2712.022**	SS	Intrinsic Identifiers for Database-Free Remote Authentication of IoT Edge Devices	Bhunia, Swarup	U. Florida
25	**2712.023**	EE	Ultra-Low-Power Compressive Sensing Techniques for IoT Applications	Sun, Nan	UT Austin
26	**2712.024**	EE	A System-In-Package Platform for Energy Harvesting and Delivery for IoT Edge Devices	Mukhopadhyay, Saibal	Georgia Tech
27	**2712.025**	FA	Reduction of Low Frequency Noise Impact in Nano-Scale CMOS Circuits	O, Kenneth K.	UT Dallas
28	**2712.026**	SS	Fault Characterization and Degradation Monitoring of SiC Devices	Akin, Bilal	UT Dallas
29	**2712.027**	EE	Gate Driving Techniques and Circuits for Automotive-Use GaN Power Circuits	Ma, D. Brian	UT Dallas
30	**2712.028**	EE	High Performance Micro-supercapacitor on a Chip Based on a Hierarchical Network of Nitrogen Doped Carbon Nanotube Sheets Supported MnO2 Nanoparticles	Lee, Gil	UT Dallas

	Task	Thrust	Title	Task Leader	Institution
31	**2712.029**	SS	Novel Super-resolution and MIMO Techniques for Automotive and Emerging Radar Applications	Torlak, Murat	UT Dallas
32	**2712.030**	SS	Performance of Carbon Dioxide (C02) Gas Sensors	Prasad, Shalini	UT Dallas
33	**2712.031**	FA	Adaptive Trimming and Testing of Analog/RF Integrated Circuits (ICs)	Makris, Yiorgos	UT Dallas
34	**2810.002**	SS/EE	Security-Aware Dynamic Power Management for System-on-Chips	Mukhopadhyay, Saibal	Georgia Tech
35	**2810.003**	EE	Integrated Voltage Regulator Management for System-on-Chip Architectures	Zhang, Xuan	Washington Univ.
36	**2810.005**	FA/SS	Circuit Design for ESD and Supply Noise Mitigation	Rosenbaum, Elyse	UIUC
37	**2810.006**	EE	Combating Unprecedented Efficiency, Noise and Frequency Challenges in Modern High Current Integrated Power Converters	Ma, D. Brian	UT Dallas
38	**2810.007**	FA	Fully Integrated Phase Noise Cancellation Techniques	Niknejad, Ali M.	UC Berkeley
39	**2810.008**	EE	Circuit Techniques for Fast Start-Up of Crystal Oscillators	Pamarti, Sudhakar	UC Los Angeles
40	**2810.009**	EE/FA	Mixed-Signal Building Blocks for Ultra-low Power Wireless Sensor Nodes	Sylvester, Dennis M.	U. Michigan
41	**2810.010**	EE	GS/s ADC Based Cycle-to-Cycle Closed-Loop Adaptive Smart Driver for High-Performance SiC/GaN Power Devices	Gui, Ping	SMU
42	**2810.011**	EE	Micro-Power Analog-to-Digital Data Converters for Sensor Interfaces	Temes, Gabor	Oregon State
43	**2810.012**	EE	NPSense - Nano-Power Current Sensing	Makinwa, Kofi	Delft University
44	**2810.013**	FA	Frequency-Domain ADC-Based Serial Link Receiver Architectures for 100+Gb/s Serial Links	Palermo, Samuel M.	Texas A&M
45	**2810.014**	FA	Deep Learning Solutions for ADAS: From Algorithms to Real-World Driving Evaluations	Busso, Carlos	UT Dallas
46	**2810.015**	FA	Demonstration of 120-Gbps Dielectric Waveguide Communication Using Frequency Division Multiplexing (FDM) and Polarization Division Multiplexing (PDM)	O, Kenneth K.	UT Dallas

	Task	Thrust	Title	Task Leader	Institution
47	**2810.016**	SS	Condition Monitoring of Industrial/Automotive Drive Components through Leakage Flux	Akin, Bilal	UT Dallas
48	**2810.017**	SS	Reliability Study of E-mode GaN HEMT Devices	Kim, Moon	UT Dallas
49	**2810.018**	FA	Transition Design for High Data Rate Links at Submillimeter Wave Frequencies	Henderson, Rashaunda	UT Dallas
50	**2810.019**	FA	Design Automation for Coverage Management in Analog and Mixed-Signal SOCs	Dasgupta, Pallab	Indian Institute of Technology Kharagpur
51	**2810.020**	FA	Analog/Mixed-Signal RF Circuit Time Domain Sensitivity and Its Applications	Rohrer, Ronald	SMU
52	**2810.021**	SS	A Collaborative Machine Learning Approach to Fast and High-Fidelity Design Prediction	Hu, Jiang	Texas A&M
53	**2810.022**	SS	A Collaborative Machine Learning Approach to Fast and High-Fidelity Design Prediction	Chen, Yiran	Duke University
53	**2810.023**	SS	Machine Learning Driven Automatic Mixed-Signal Design Verification-Validation for Automotive Applications	Chatterjee, Abhijit	Georgia Tech
54	**2810.024**	FA	Development and Assessment of Machine Learning Based Analog and Mixed-Signal Verification	Li, Peng	Texas A&M
55	**2810.025**	SS	Machine Learning-Based Layout Analysis and Netlist Optimization for Defect Tolerance and Design Robustness to Process Imperfections and Variations	Makris, Yiorgos	UT Dallas
56	**2810.026**	FA	Low Noise Balun Pre-Power Amplifier	Nauta, Bram	U. Twente
57	**2810.027**	SS	Measurement and Modeling of Stress/Strain on Analog Transistor and Circuit Parameters	Thompson, Scott	U. Florida

Table 2: Funded research projects at TxACE by SRC task identification number (FA: Fundamental Analog, EE: Energy Efficiency, SS: Safety, Security and Health Care)

ACCOMPLISHMENTS

In the past year, TxACE has made significant research progress. Table 3 summarizes the number of publications and inventions resulting from the TxACE research during May 2018 to April 2019, while Table 4 lists the major research accomplishments for the Center during the period. The TxACE researchers have published 58 conference papers, 23 journal papers, and 2 books/chapters. They have also made one invention disclosure, filed nine patent applications, and were granted one patent. The list of publications is included as Appendix I. Following the tabulation, brief summaries of each project are provided.

Table 3. TxACE number of publications (May 2018 through April 2019)

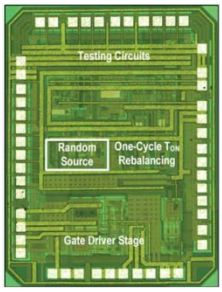
Conference Papers	Journal Papers	Books/Chapters	Invention Disclosures	Patents Filed	Patents Granted
58	23	2	1	9	1

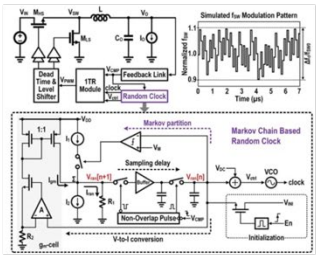
Table 4. Major TxACE Research Accomplishments (May 2018 through April 2019)

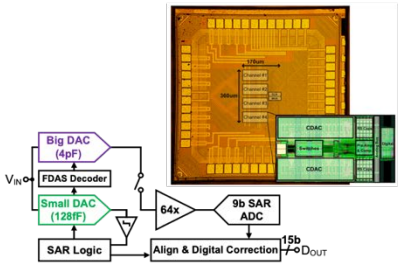
Category	Accomplishment
Energy Efficiency (Circuits)	State-of-the-art low-power ADCs are difficult to drive as they require a filter and an input buffer, and are limited in either resolution or power consumption. To overcome these limitations, the first interleaved noise-shaping SAR ADC that uses the first four-stage ring amplifier is demonstrated. The ADC achieves a measured resolution of 15b. This new class of converters will facilitate and improve sensing and IoT applications. (2712.007, M. Flynn, U. Michigan)
Energy Efficiency (Systems)	The gate driving strength should be low before the starting point of Miller Plateau to reduce di/dt for lower EMI noise. Subsequent to this point, the drive strength should be rapidly increased to achieve a high dv/dt for low power loss. These have been utilized to realize a GaN DC-DC Buck converter with an adjustable gate driver stage in a custom 0.18-μm HV CMOS process that achieves 119% higher peak-EMI attenuation, and 3 times higher V_O-jittering suppression than the state of art. (2810.006, B. Ma, UT Dallas)
Energy Efficiency (Circuits)	Integrated voltage regulation of fine-grained voltage domains is accomplished through use of a resonant-clocked SIMO buck converter and addressing the accompanying challenges of severely degraded load regulation through a novel unified clock-regulator architecture. The first computationally controlled LDO for rapidly settling V_{DD}, and auto-tuning of loop-gain is demonstrated in 65-nm CMOS. (2712.006, V. Sathe, U. Washington)

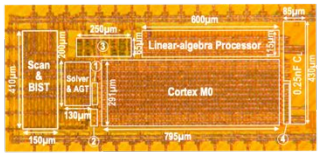
Category	Accomplishment
Energy Efficiency (Circuits)	A VCO-based CT ADC with a record low measured Walden FoM of 8.6fJ/step with a 100-μW power consumption is demonstrated. (2712.020, A. Sanyal, U. Buffalo)
Safety, Security and Health Care (Systems)	Impedance mismatch resulting from variations of antenna impedance reduces the power delivered by mm-Wave power amplifiers. This project seeks to overcome this limitation and the concomitant VSWR events using a multi-port architecture which exploits mutual load-pulling to synthesize optimal impedances under VSWR events. Measurements from a fabricated prototype demonstrate broadband Doherty-like operation with P_{sat}>19dBm and PAE_{peak}>20% across 28GHz to 39GHz, as well as robust tolerance to VSWR events. (2712.013 Sengupta, Princeton)
Safety, Security and Health Care (Systems)	The limited energy storage capacity of IoT devices calls for solutions both for energy harvesting and for efficient uses of the energy soon after the harvest. Pre-computation has been used to demonstrate inherent operations of internet security protocols, such as random number generation and as well as cryptographic key exchange, thereby maximizing energy utilization without sacrificing security. (2712.019 Schaumont, Virginia Tech)
Fundamental Analog (Circuits)	A 3-GHz 8X clock multiplier with a jitter performance that is insensitive to frequency drift without using a continuous frequency tracking loop (FTL) is demonstrated. Using digital calibration techniques, the spurs are effectively suppressed down to -50.9 dBc. Fabricated in 28-nm CMOS technology, this prototype achieves an integrated jitter of 138 fs,rms while consuming 6.5 mW from a 1-V/0.8-V supplies and achieves -249-dB FoM. (2810.007, PI: Ali Niknejad)
Fundamental Analog (Circuits)	High data rate 180-GHz MSK modulated signals for dielectric waveguide communication with an output power of -3.5 dBm are demonstrated using a signal generator fabricated in 65-nm CMOS. Limited by the instrumentation for MSK signal analyses, the eyes of transmitted MSK signals have been verified for a data rate up to 10 Gbps. The spectra of transmitted signals for data rate up to 15 Gbps are also demonstrated. The MSK signal generator provides 5X higher data rate among all the previously reported MSK transmitters at 3X higher carrier frequency. (2810.015, PI: Ken O)

Energy Efficiency Thrust

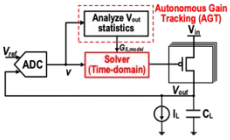


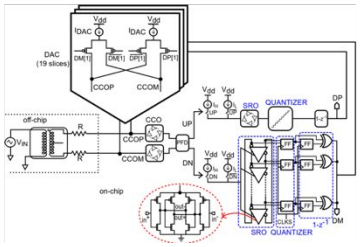


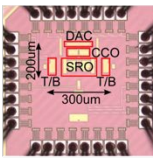




① PMOS headers 80x25µm²
② Clock generator 65x35µm²
③ Comparator bank 65x250µm²
④ Synthetic load 190x12µm²







Category	Accomplishment
Energy Efficiency (Circuits)	State-of-the-art low-power ADCs are difficult to drive as they require a filter and an input buffer, and are limited in either resolution or power consumption. To overcome these limitations, the first interleaved noise-shaping SAR ADC that uses the first four-stage ring amplifier is demonstrated. The ADC achieves a measured resolution of 15b. This new class of converters will facilitate and improve sensing and IoT applications. (2712.007, M. Flynn, U. Michigan)
Energy Efficiency (Systems)	The gate driving strength should be low before the starting point of Miller Plateau to reduce di/dt for lower EMI noise. Subsequent to this point, the drive strength should be increased rapidly to achieve a high dv/dt for low power loss. This observation has been utilized to realize a GaN DC-DC Buck converter with an adjustable gate driver stage in a custom 0.18-µm HV CMOS process to achieve 119% higher peak-EMI attenuation, and 3 times higher V_O-jittering suppression than the state of art. (2810.006, B. Ma, UT Dallas)
Energy Efficiency (Circuits)	Integrated voltage regulation of fine-grained voltage domains is accomplished through use of a resonant-clocked SIMO buck converter and addressing the accompanying challenges of severely degraded load regulation through a novel unified clock-regulator architecture. The first computationally controlled LDO for rapidly settling V_{DD}, and auto-tuning of loop-gain is demonstrated in 65-nm CMOS. (2712.006, V. Sathe, U. Washington)
Energy Efficiency (Circuits)	The goal of this project is to realize a mostly digital, high-order VCO based Delta-Sigma ADC. A prototype of VCO-based CT ADC has a record low measured Walden FoM of 8.6fJ/step with a 100-µW power consumption. (2712.020, A. Sanyal, U. Buffalo)

TASK 1836.153, HIGH-SPEED COMPACT POWER SUPPLIES FOR ULTRA-LOW-POWER WIRELESS SENSOR APPLICATIONS

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SIGNIFICANCE AND OBJECTIVES

Efficient and compact switched-capacitor (SC) voltage regulators are highly desirable for ultra-low-power sensor applications to improve energy efficiency and reduce system form factor. This project is to deliver a wide-input, fully-integrated SC voltage regulator with high efficiency and fast dynamic responses for sensor systems.

TECHNICAL APPROACH

In this project, a 2:1 unit SC cell is proposed to attain multiple conversion ratios (CRs), to handle wide input range and to reduce system complexity. The 2:1 unit cell consists of one flying capacitors and 4 power switches which are all implemented by using NMOS transistors. By using four unit SC cells and swapping the input and the output, the proposed SC voltage regulator achieves 8 high CRs ($\leqslant$0.5 or $\geqslant$2) to support the input range from 0.5V to 5V. A simple hysteretic controller is utilized to improve load regulation and load transient performance.

SUMMARY OF RESULTS

In the last year, the second chip prototype is fabricated by using a BCD process technology to verify the multiple CR reconfigurations and to accommodate the wide input range and low power consumption. The proposed switched-capacitor voltage regulator architecture is shown in Figure 1. Three-stage of SC topology are implemented by using all-NMOS 2:1 unit cells. The bootstrapped gate driver is driven by the input voltage with a rail-sharing technique. Deadtime control and level shifter are optimized to achieve non-overlapping gate signals and fast voltage level shifting. Two-phase interleaving scheme reduces the output ripple, minimizes the output filtering capacitor and reduces the system form factor. An adaptive-pulse (AP) emulated hysteretic controller is proposed in this project to improve the regulation of the output voltage with low quiescent power. Furthermore, by comparing the input with the reference voltage V_{REF}, the CR optimizer, as a feedforward path, selects the proper CR to maintain the efficiency over a wide input range.

Figure 2 illustrates the chip micrograph of the second prototype. This design is fabricated by using a 0.18-µm BCD process with an active area of 2mm×2mm. The pumping capacitors occupy ~60% of the total area with the overall value of 3nF. The hysteretic controller is area-efficient, since only an analog circuit is used. Placing the controller in the center of the chip reduces closk skew. The switching frequency can be modulated from 10kHz to 28MHz depending on the load condition. With the input from 0.3V to 5V, the output voltage varies from 0.9V to 1.2V.

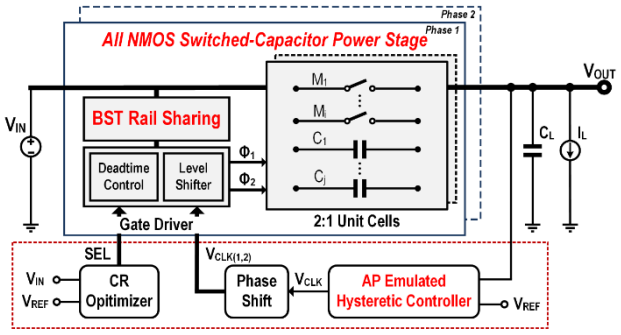

Figure 1. Switched-capacitor voltage regulator for ultra-low-power wireless sensors.

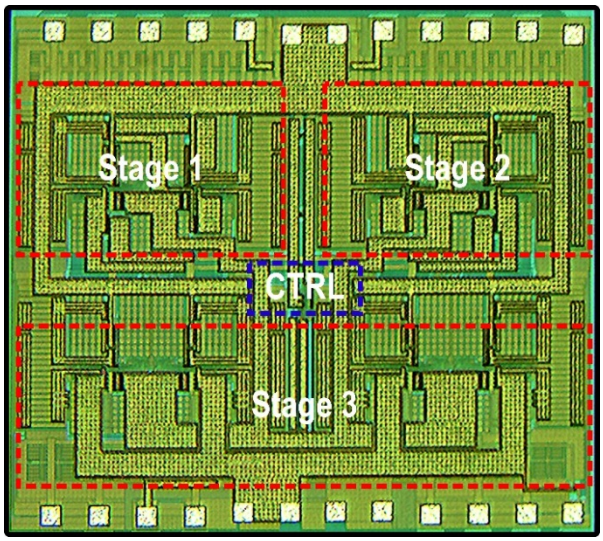

Figure 2. Chip micrograph of the second prototype using a BCD process.

Keywords: Wireless sensor, wide input, switched-capacitor, reconfiguration, bootstrapped gate driver

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

[1] K. Wei and D. Ma, "State-of-the-Art Monolithic Switched-Capacitor Voltage Regulators for Ultra-Low Power Internet of Things," *14th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, pp. 1-4, Nov. 2018.

TASK 2712.002, ON-LINE SELF-TESTING AND SELF-TUNING OF INTEGRATED VOLTAGE REGULATORS

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SIGNIFICANCE AND OBJECTIVES

The proposed research will develop low-complexity algorithms and low-overhead all-digital self-testing and self-tuning architecture for high-frequency IVRs. The research will focus on digitally controlled fully integrated inductive VRs (FIVR), digital low-dropout regulators (DLDO), and power delivery system with FIVR and multiple distributed DLDOs.

TECHNICAL APPROACH

The challenge for testing/tuning of IVRs is the presence of high frequency closed-loop control. The proposed approach is based on the principle that in a system with an IVR and digital core(s), the testing/tuning should focus on system performance rather than the IVR in isolation. We propose to characterize the output voltage variation that ultimately determines the performance of the digital load. We consider large signal perturbations (load and reference steps) to excite the transient noise in the IVR output, and tune the loop of IVR to minimize the noise. Finally, we explore co-tuning of IVR and processor.

SUMMARY OF RESULTS

Performance-based Tuning of Inductive IVR: We have demonstrated auto-tuning of the coefficients of the feedback loop of an inductive integrated voltage regulator (IVR) using an on-chip delay sensor. A 130-nm CMOS test-chip is designed containing a multi-sampled 125-MHz IVR with wire bond inductor, on-die capacitor, and all-digital PID controller powering a parallel Advanced Encryption Standard (AES) engine. The auto-tuning is performed using a Vernier delay line based on-chip delay sensor and an all-digital tuning engine. The measurement results demonstrate up to 5.2% improvement in the maximum operating frequency of the AES core using performance-based auto-tuning.

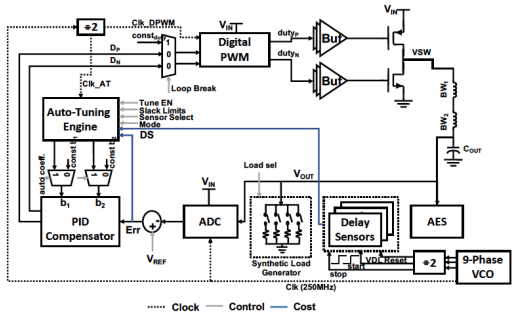

Figure 1. The architecture of performance-based tuning of inductive voltage regulators.

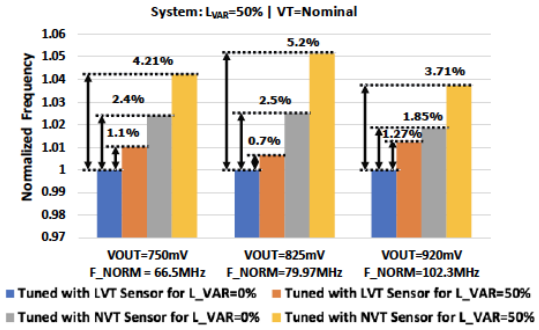

Figure 2. The measurement results showing impact of performance based tuning on performance of an AES.

Aging analysis of Inductive IVR and Digital LDO: Degradation of the transient performance and power conversion efficiency of on-chip VRs due to NBTI has been studied using 130-nm CMOS test-chips. The simulation and measurement show that NBTI induced shifts in the power stage resistance has much smaller effect on IVR compared to DLDO.

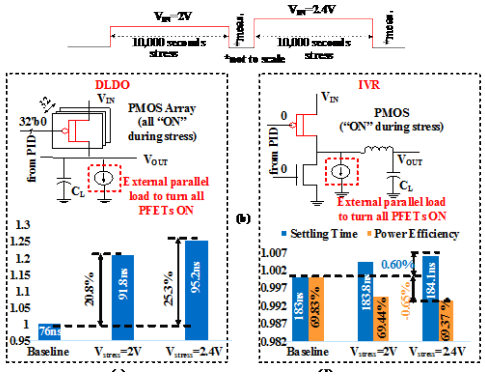

Figure 3: The measurement results showing impact of aging on inductive VR and digital LDO.

Keywords: Integrated voltage regulator, self-testing, and self-tuning.

INDUSTRY INTERACTIONS

Intel, NXP

MAJOR PAPERS/PATENTS

[1] V. Chekuri, A. Singh, N. Dasari and S. Mukhopadhyay, "On the Effect of NBTI Induced Aging of Power Stage on the Transient Performance of On-Chip Voltage Regulators," IRPS 2019.

[2] V. Chekuri, M. Kar, A. Singh, and S. Mukhopadhyay, "Auto-tuning of Integrated Inductive Voltage Regulator using On-chip Delay Sensor to Tolerate Process and Passive Variations," IEEE TVLSI 2019.

TASK 2712.006, ROBUST, EFFICIENT ALL-DIGITAL SIMO CONVERTERS FOR FUTURE SOC DOMAINS

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SIGNIFICANCE AND OBJECTIVES

Suitably designed Single-Inductor Multiple Output converters offer a scalable Integrated Voltage Regulator solution for modern SoCs. This effort seeks to design (1) an all-digital voltage regulation system using a Single-inductor Multiple Output (SIMO) topology for digital SoC domains and (2) Unified Clock and Power (UniCaP) delivery to enable robust SIMO regulation.

TECHNICAL APPROACH

The effort relies on two critical research thrusts toward the targeted goal of realizing a practical SIMO architecture: UniCaP, and the idea of computationally enabled control. UniCaP compensates for the large ripple and poor transient response of SIMO converters when driving digital loads. Computationally enabled control provides rapid (minimal-time) transient response and is thus critical in addressing peak-droop concerns which impact the performance of latency sensitive systems such as microprocessor and streaming applications. We have thus far proceeded on two fronts: (1) a test-chip demonstration of the UniCaP architecture and (2) demonstrated all-digital computational control for rapid, scalable V_{dd} regulation.

SUMMARY OF RESULTS

We recently proved the idea of computational control on a simpler sytem (a digital LDO) in order to demonstrate its capability to deliver rapid stable response [1]. The architecture has resulted in two important contributions, one in terms of hardware performance, and another in terms of design architecture. Computational control has resulted in a digital LDO with the fastest demonstrated settling time to date capable of scaling effectively to advanced process nodes. It has also advanced the state of the art for designing integrated control systems in two important ways: (1) computation can be used to achieve time-optimal control of a system for minimizing settling time, and (2) simple and low-precision statistical analysis and computation can be used to *learn* the loop gain of a closed-loop system regulator based on sampling the autocorrelation of the quantized voltage error. Such an approach avoids worst-case stability margining which typically results in degraded regulator transient response. Instead, the regulator autonomously tunes its loop gain toward the most rapid, yet stable transient response achievable by gain settings. Specifically, the approach analyzes the 1-bit autocorrelation of the sampled voltage error in each cycle, and combined with knowledge of the target output auto-correlation, tunes loop gain to achieve the optimal transient response regardless of variation of V_{in}, V_{out}, and temperature.

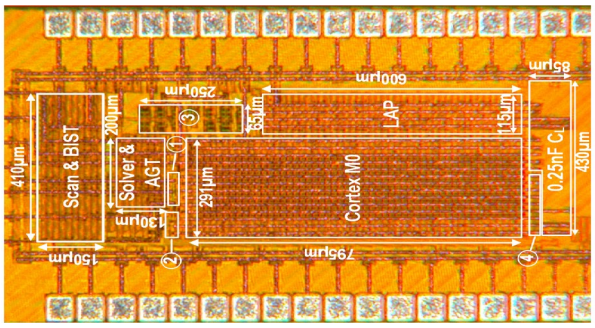

Figure 1. Die photograph of a computationally controlled digital LDO powering a Cortex-M0 microprocessor. The 65nm CMOS test chip demonstrated an LDO with a mean settling time of 2.9 cycles in response to a 0.11ns/6mA load-step.

Another feature critical for rapid LDO response is the ability to update the header code corresponding to a voltage error within the same cycle. Accounting for the sub-cycle loop delay, however, poses a challenge. Computational control once again provides the ability to account for loop delay in such a design. Accurately modeling system behavior in the time domain allows the controller to capture the effect of delayed LDO code update to the headers. In doing so, the controller is able to determine the time-optimal LDO code allocation for minimum settling time. This work can be generalized to maximizing the power supply rejection of the design as well.

Keywords: SIMO, Computational Control Unified Clock and Power, Voltage Regulation.

INDUSTRY INTERACTIONS

Intel, ARM

MAJOR PAPERS/PATENTS

[1] Sun, X et al. "A 0.6-to-1.1V Computationally Regulated Digital LDO with 2.79-Cycle Mean Settling Time and Autonomous Runtime Gain Tracking in 65nm CMOS", ISSCC 2019.

[2] Visvesh S. Sathe “Integrated Voltage and Clock Regulation”. Patent application, 6/2019.

TASK 2712.007, HIGH-RESOLUTION LOW-VOLTAGE HYBRID ADCS FOR SENSOR INTERFACES

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SIGNIFICANCE AND OBJECTIVES

The goal of this research is to extend the state of the art of high resolution sensor interface ADCs through research and development of a hybrid ADC architectures that are also easy to drive.

TECHNICAL APPROACH

A new class of hybrid converters that will facilitate and improve sensing and IoT applications are researched. The needs for these applications are currently unmet since state-of-the-art low-power ADCs are difficult to drive (i.e. requiring filter and input buffer), and are limited in either resolution or power consumption. ADCs for sensors are often implemented as SAR or oversampling ADCs. SAR ADCs achieve excellent energy efficiency but are limited to moderate resolution. Calibration adds complexity and may need to be adjusted with temperature and supply changes. $\Sigma\Delta$ ADCs and incremental converters can achieve higher resolution but are constrained by the requirements of the op-amps and switches.

SUMMARY OF RESULTS

Although tremendous advances have been made on the energy efficiency of ADCs, ADCs are still a bottleneck in many systems because they are difficult to drive and suffer from many other practical limitations. Moreover, SAR ADC energy efficiency drops steadily as the ADC ENOB increases above 10b. The anti-alias filter is another huge challenge to the practical implementation of many systems. If a near-minimum sampling speed is selected to minimize ADC power, then the resulting sharp cutoff anti-alias filter can easily be more challenging to design than the ADC itself.

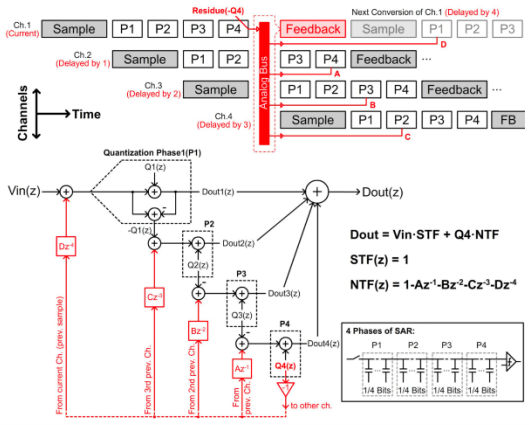

Figure 1. Interleaved noise-shaping architecture.

The Noise-Shaping SAR (NS-SAR) is an emerging ADC architecture that offers both high resolution and high energy efficiency. State-of-the-art NS-SAR ADCs eliminate the need for op-amps, which relaxes design complexity and technology scaling issues. However, existing NS-SAR ADCs, with high FoM, are limited in bandwidth (typically in the MHz range). This makes NS-SAR ADCs unsuitable for applications that need bandwidths in the tens of MHz range, such as wireless communications. Traditionally, high-bandwidth, high-resolution applications utilize pipeline or continuous-time sigma- delta (CT-SD) ADCs, but these architectures are much more power hungry than the NS-SAR. Thus, to increase the bandwidth of NS-SAR ADCs and extend their low-power advantages, this work presents a new time-interleaved noise-shaping SAR (TINS-SAR) architecture that enables higher bandwidth. Although time-interleaving of ADCs is difficult for high resolution, interleaving impairments can be avoided when combining interleaving with noise-shaping. Our prototype 40-nm CMOS TINS-SAR ADC has a measured SNDR of 70.4dB for a 50MHz bandwidth without calibration. It consumes only 13mW and occupies 0.061mm^2, making it a potential substitute for CT-SD ADCs.

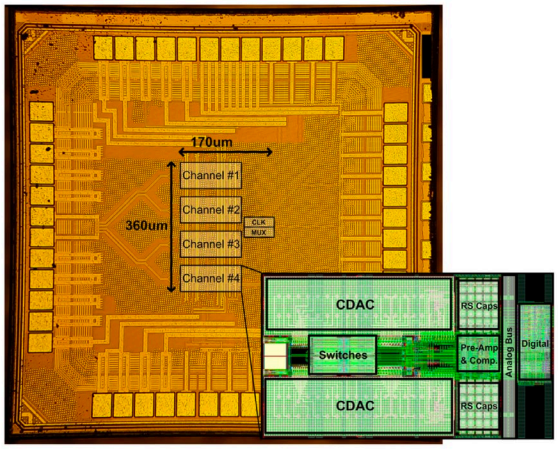

Figure 2. Protoype ADC in 40-nm CMOS.

Keywords: Sigma Delta, ADC, sensor, SAR, IoT

INDUSTRY INTERACTIONS

Texas Instruments, Intel, ARM, NXP

MAJOR PAPERS/PATENTS

[1] L. Jie al., "A 50MHz-Bandwidth 70.4dB-SNDR Calibration-Free Time-Interleaved 4th-Order Noise-Shaping SAR ADC," ISSCC, February, 2019, San Francisco.

TASK 2712.008, DIRECT-BATTERY-TO-SILICON POWER TRANSFER IN ADVANCED NANOMETER CMOS

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SIGNIFICANCE AND OBJECTIVES

The aim is to facilitate direct-battery-to-silicon (DBS) high-tension-power delivery in advanced CMOS processes to bring down delivery losses and area footprint. The key objective is to develop circuit techniques to handle breakdown voltages and implement fine-grain feedforward control for SOCs while making these solutions portable across technology and types of SOCs.

TECHNICAL APPROACH

Deep-submicron technologies have ~1V as the core MOS rated voltages and at-max 2.5V for thick-oxide I/O MOS devices. In order to handle 4+V battery voltage careful stacking/design of devices is required. During the course of the project, we will work on both capacitive and inductive converters. In this part of project, we focused on a new kind of hybrid converter - multi-mode DC-DC converter which can provide a relatively large range of conversion ratio (K=1-13) and handle a large load range (0.5-200mA).

SUMMARY OF RESULTS

During the whole discharging process, the output voltages of lithium-ion battery change from initially 4.2V to fully discharged 2.8V. Also, in an SOC, the voltage requirements continue to decrease, i.e., 0.75V (14nm) and 0.6V (6nm). The consequential voltage mismatch between the 4.2-2.8V battery voltage and the desired sub-1V preferred for the low power SOCs necessitates efficient voltage conversion techniques.

To accommodate this wide range of DC-DC conversion ratios (K) (between 1 to 13), we implemented a direct battery to silicon multi-mode hybrid switching regulator system in 65-nm CMOS. The proposed DC-DC converter has three modes of operations, namely - 4 level buck (for K=5-13), resonant (K=1 & 2) and soft switching (for K=3 & 4) as illustrated in Fig. 1. Fig. 2 shows the block diagram and chip micrograph for the multi-mode DC-DC converter. As the figure shows, a 13-level modified-ADC selects the mode of operation of this converter. By utilizing the optimal converter mode for each input-output voltage ratio, the efficient conversion of power can be achieved. Fig. 3 shows the efficiency vs. output voltage and battery voltage for three load currents. Our multi-mode DC-DC converter can achieve a peak efficiency of 86.6% and handle a load range of 0.5-200mA at a peak power density of 0.3W/mm^2.

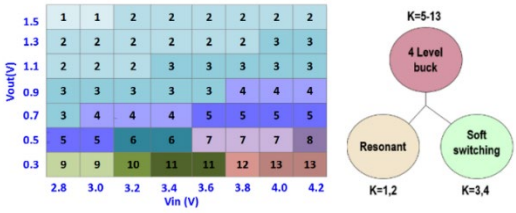

Figure 1. (Left) Different conversion ratios for output vs. input voltages (Right) Three modes of hybrid DC-DC.

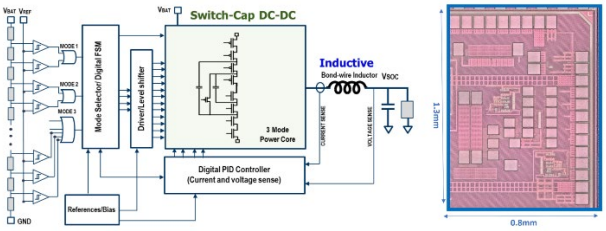

Figure 2. Architecture and chip micrograph of the proposed multi-mode DC-DC converter for DBS in standard CMOS.

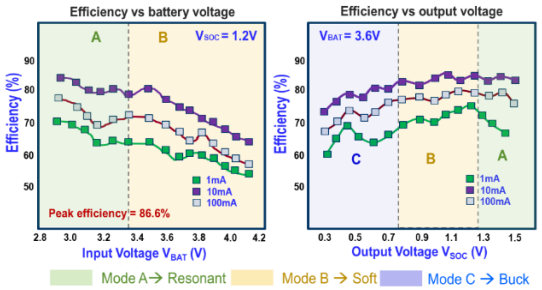

Figure 3. (Left) Efficiency vs battery voltage V_{bat} for 3 current levels at fixed V_{out}. (Right) Efficiency vs output voltage V_{soc} for three current levels at fixed battery voltage.

Keywords: power mgmt, hybrid multimode DC-DC

INDUSTRY INTERACTIONS

NXP, Intel

MAJOR PAPERS/PATENTS

[1] Harjani et al."A Multi-Mode DC-DC Converter for Direct Battery-to-Silicon High Tension Power Delivery in 65nm CMOS", CICC 2019

[2] Harjani, R., "Fully Tunable Software Defined DC-DC Converter with 3000X Output Current & 4X Output Voltage Range 2010", CICC 2017

[3] Harjani, et al." A Smart-Offset Analog LDO with 0.3V Minimum Input Voltage and 99.1% Current Efficiency", A-SSCC, Nov 2017

[4] Harjani, et al., "Ultra High Density Integrated Composite Capacitor", US patent # 9,812,457, Issued Nov 7, 2017 [Patent]

TASK 2712.009, LOW POWER AREA EFFICIENT FLEXIBLE-RATE ENERGY PROPORTIONAL SERIAL LINK TRANSCEIVERS

PAVAN HANUMOLU, UNIVERSITY OF ILLINOIS, HANUMOLU@ILLINOIS.EDU

SIGNIFICANCE AND OBJECTIVES

Rapid on/off transceivers offer an attractive means to reduce power consumption in network switches and mobile interfaces. Implemented in 65-nm CMOS, the prototype receiver turns on in less than 10ns from a completely off state and recovers clock and data from the received signal subjected to 20-dB channel loss.

TECHNICAL APPROACH

Figure 1 shows a block diagram of the proposed half-rate receiver. It consists of a CTLE, 3-tap DFE, baud-rate CDR, and circuitry to support rapid on/off operation. The proposed phase detector(PD) uses a new timing function, $f(t)=h_0-h_1$, that enables baud-rate CDR operation. Note h_0 and h_1 represent the cursor and first post-cursor of the channel pulse response, respectively. Compared to Mueller-Muller PD, the proposed PD requires only half the number of samplers and performs better when channel loss is high. The potential error propagation was avoided by adopting duobinary encoding/decoding scheme. Phase sweeping is performed implicitly by digitally adding a frequency offset to the DCO and the CDR can find the optimal phase within 100UI.

SUMMARY OF RESULTS

Fabricated in a 65-nm CMOS, the receiver achieves error-free operation (BER < 10^{-12}) when recovering 12Gb/s PRBS31 data. The receiver is characterized using a channel (19-inch PCB trace and 2-m coaxial SMA cable) that has a measured insertion loss of 20dB at Nyquist frequency.

The measured bathtub plots show DFE improves clock phase margin to about 0.18UI at a BER of < 10^{-11}. The measured JTOL curve has a corner frequency of about 30MHz with PRBS7 and BER < 10^{-11}. Phase noise of the 6GHz recovered clock shows an integrated jitter (10kHz to 100MHz) of 377fsrms.

The receiver consumes 45.7mW and 3.7mW in the ON and OFF states, respectively, achieving 3.8pJ/bit of energy efficiency in the ON state. The receiver turned on in less than 10ns (18ns including checker latency) even in the presence of ±1300ppm of frequency difference between the received data and the oscillator (see Fig. 2). This large error-free lock in range can compensate frequency drift of the oscillator in the OFF state caused by voltage/temperature variations.

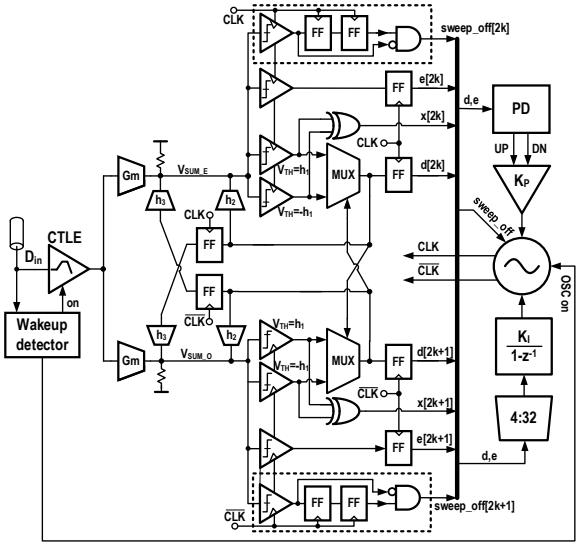

Figure 1. Proposed half-rate receiver architecture.

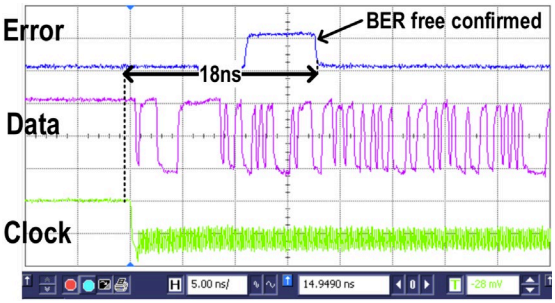

Figure 2. Measured turn-on behavior.

Keywords: CDR, Baud-rate, Rapid on/off, Burst-mode

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] D. Kim et al., "A 12Gb/s 10ns turn-on time rapid on/off baud-rate DFE receiver in 65nm CMOS", Journal of Solid State Circuits (in preparation).

TASK 2712.012, EDAC AND DCDC-CONVERTER CO-DESIGN FOR ADDRESSING ROBUSTNESS CHALLENGES IN EMERGING ARCHITECTURE

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SIGNIFICANCE AND OBJECTIVES

The goal of this project is investigate techniques on EDAC and DC-DC converter co-design for the post-Moore's law era where aggressive architectures and circuits will be explored to continue the performance and energy-efficiency scaling while ensuring robustness and reliability.

TECHNICAL APPROACH

We will devise the following techniques: (i) direct error regulation to make DVS energy-efficient and fully-digital while miniaturizing capacitor sizes in the integrated switched-capacitor converter; (ii) EDAC+Converter for non von-Neumann and parallel architecture, such as error correction scheme for super-V_t circuits performing no instruction replay, and techniques for in and around embedded memory; (iii) EDAC+DVS for clock domain crossing to simplify clock distribution and generation.

SUMMARY OF RESULTS

During this year, we have worked on mainly two projects. First, we have been working on the design of single-inductor-multiple-output (SIMO) converter for a sub-milliwatt digital system-on-chip (SoC) that requires multiple DVFS domains. It uses only *one* off-chip inductor for multiple outputs for improved area efficiency and power conversion efficiency (PCE) over using multiple switched capacitor DC-DC converters and linear regulators. To minimize the off-chip component count, we aim to integrate all the output capacitors on a chip by *minimizing the capacitor's size to ~200 pF per output*.

Fig. 1 shows the architecture of the proposed SIMO converter. It employs a single inductor and produces 10 output voltage, any value between 0.8 to 0.4V from 1-V input. The converter can support a total of 1 mA or 100 µA/output, which are sufficient for emerging ultra-low-power digital SoCs. The output capacitor is only 200 pF per output, yet supporting the ripple of 10% of the output voltage. *The simulated PCE with parasitic annotated netlists is ~85% in a 65-nm CMOS*.

We create multiple fast and power-efficient control loops to reduce output capacitor size yet maximize the PCE. The first is the output control loops each of which controls one output. It regulates the output voltage to a target level by turning on and off the output switches (V_{SWO1} to V_{SWON} in the figure). To enable low-power but accurate control, this control loop employs asynchronous voltage hysteresis comparator per output. The second is the inductor duty cycle loop, which controls the duty cycle of the main switches (V_{MSWP} and V_{MSWN}) to supply the same amount of current used by all the outputs. The converter is being designed using a 65-nm CMOS process.

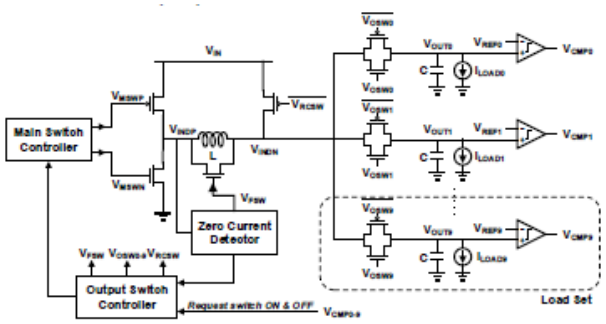

Figure 1. Architecture of the single-inductor 10-output DC- DC converter for an ultra-low-power (sub-milliwatt) SoC which needs multiple voltage domains for various building blocks.

In the second project, we have worked on the EDAC based clock domain crossing technique. We have analyzed and simulated the challenges in clock domain crossing in near- and sub-threshold digital circuits. In particular, we simulated the metastability in a FIFO which is commonly-employed for clock domain crossing. We devised a new EDAC based circuit that can detect the metastability and correct the resulted error automatically at low timing overhead. We just taped out the test chip.

Keywords: near- and sub-V_t digital SoC, SIMO power converter, EDAC, clock domain crossing, metastability

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] S. Kim et al., "A Near-Threshold Spiking Neural Network Accelerator with a Body-Swapping based In-Situ Error Detection and Correction," IEEE Transactions on VLSI Systems (TVLSI), 2019.

[2] S. J. Kim et al., "A 67.1-ps FOM, 0.5-V-Hybrid Digital LDO With Asynchronous Feedforward Control Via Slope Detection and Synchronous PI With State-Based Hysteresis Clock Switching," IEEE Solid-State Circuits Letter (SSCL), 2019.

TASK 2712.016, 3D IC THERMAL MANAGEMENT BASED ON TSV PLACEMENT OPTIMIZATION AND NOVEL MATERIALS

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SIGNIFICANCE AND OBJECTIVES

3D ICs offer advantages in performance and power consumption, but heat dissipation challenges remain unsolved due to the stacked configuration. The project objective is to enable efficient thermal management by optimizing the thermal TSV (TTSV) placement with respect to area, peak temperature, and wirelength and exploring various TSV design parameters.

TECHNICAL APPROACH

We have developed a simulated annealing (SA)-based algorithm that can optimize the floorplan of 2D or 3D ICs with varying TTSV area overheads and dimensions. For optimization of a 3D multicore processor, the SA-based algorithm is used to optimize area, wirelength, and temperature of a single core. Then, a hierarchical approach is used to generate the core layer floorplan based on the symmetric operation of the optimized single core and to complete the whole floorplan of 3D IC including heat sinks, interconnects, and cache layers and others. The impact of TTSVs on peak temperature and wirelength of 3D ICs is evaluated.

SUMMARY OF RESULTS

A Nehalem-based 3D multicore processor (3D Nehalem) is constructed to evaluate the floorplan optimization method. BARNES benchmark is used for thermal simulation because of its maximum power density. Splash-2 benchmarks are also used. For the non-optimized TTSV placement, TTSVs are added between cores without further optimization. For the optimized case, the placement and aspect ratio of IC blocks and TTSVs are varied during the optimization process, and TTSVs are placed between IC blocks inside the core. Figure 1 shows that the peak temperature is monotonically reduced with an increasing TTSV area overhead and the peak temperatures of 3D Nehalem with TTSV placement optimization (green and blue) are significantly reduced compared to that of the non-optimized case (red).

While the use of TTSVs reduces the peak temperature and ensures reliable operation, it can increase the distance between IC blocks, or wire length, and wire latency. Our multi-variable optimization algorithm found that the total wire length of the optimal floorplan is not directly proportional to the amount of TTSV usage. Instead, as the TTSVs area overhead increases, the wire length can either increase or decrease depending on the TTSV arrangement in the optimized floorplan. For BARNES, the Itlb block is the hotspot that has the maximum temperature among the IC blocks. With no TTSV, Itlb is surrounded by other IC blocks for heat dissipation. During the TTSV placement optimization, TTSVs are placed around Itlb for heat removal, which increases the wirelength by enlarging the distance between IC blocks. As the TTSV area overhead becomes larger (over 10 %), Itlb is moved to the edge of the core. Some of the TTSVs are located at the core edge as well, which facilitates heat transfer without further increasing the wirelength.

Our simulations show that optimally placed TTSVs can effectively reduce the peak temperature with moderate sacrifices in wirelength and area. Depending on the threshold temperature and the allowed TTSV area overhead, different TTSV dimensions and area overheads can be chosen during the design process.

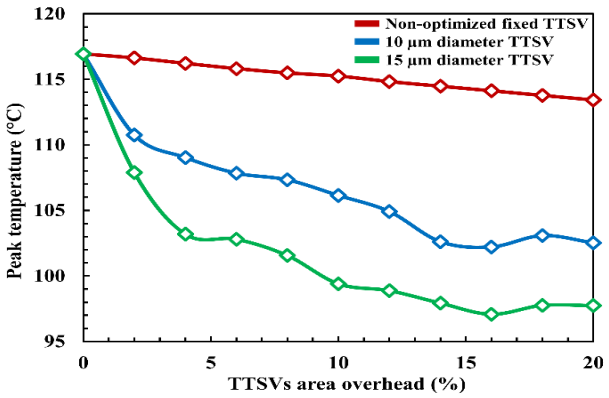

Figure 1. Peak temperatures of 3D Nehalem with/without TTSV placement optimization indicating the performance enhancement is possible through floorplan optimization. The pitch size of TTSV is 40 µm.

Keywords: 3D ICs, Thermal TSVs, Floorplan Optimization

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] A. Alqahtani, Z. Ren, J. Lee, and N. Bagherzadeh, “System Level Analysis of 3D ICs with Thermal TSVs”, ACM J. Emerg. Technol. Comput. Syst. 14.3 (2018): 37.
[2] Z. Ren, A. Alqahtani, N. Bagherzadeh, and J. Lee “Thermal TSV Optimization and Hierarchical Floorplanning for 3D Integrated Circuits” (Under review of IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.).

TASK 2712.018, TEST TECHNIQUES TO APPROACH SEVERAL DEFECT-PER-BILLION FOR POWER ICS

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SIGNIFICANCE AND OBJECTIVES

Existing LDO and Buck converter power IC test techniques examine and model chip performance through external terminals. This work designed, simulated and tested power IC subcircuits using additional bare-die test points to improve part failure rates. The goal is test yield enhancement by culling power ICs with outlier subcircuit performance.

TECHNICAL APPROACH

Task researchers demonstrated the use of internal IC test points to determine subcircuit performance inside of 65-nm CMOS LDOs and Buck Converters. Bare-die power IC probing will allow the measurement of DC, small-signal response and precise control of low and high temperature wafer measurements. Analyses, simulations and measurements of custom-designed LDO and buck converters will be performed in order to prove these new test concepts. A functional LDO IC was fabricated in 65-nm CMOS and used to characterize on-chip power IC control loop gain and phase response. A new 65-nm CMOS LDO test IC and a buck converter test IC have been submitted for fabrication.

SUMMARY OF RESULTS

This year, the researchers 1) Performed preliminary measurements of the LDO Test IC, 2) Designed a 65-nm CMOS buck Converter with enhanced testing and 3) Developed a new “servo loop” method of testing on-chip LDO control loop gain and phase. A 65-nm CMOS LDO Test IC was fabricated and packaged. The bench testing of the circuits provided the LDO load regulation and line regulation, and also great 65-nm process performance feedback for the design of a buck converter test IC. Preliminary bench test showed a functional 65-nm CMOS LDO with all the built-in test features working. The band gap reference output voltage was higher than simulation and the amplifiers required more bias voltage during measurement than in simulation. The 65-nm CMOS design kit PDK lacked analog output pads and the ones created at UF had a maximum output current of 40-50-mA. This limited the LDO output to 40-50-mA. Nevertheless, the LDO test is being used to demonstrate all the anticipated methodologies proposed in the project deliverables. A new methodology, an LDO on-chip control loop response "servo loop" test has been successfully created, simulated and measured with up to 90-dB gain with DC test. Implementation on load board for extensive AC and temperature testing is in progress. Test jigs, and software will be developed for thorough packaged testing on an ATE tester both at UF and at TI. An on chip programmable current sink was add to the LDO chip for enhanced testing controllability. Unfortunately, experiments showed the on-chip load is always on which limits the LDO pad output current.

The buck IC testing strategy is to use extra probe points for DC and analog test on the die before packaging. The researchers were guided to develop a buck converter test IC with an advanced ACM-based control loop design by the task liaisons. The researchers have designed and performed layout the buck converter characterization and subcircuit test IC in the UMC 65-nm CMOS process which was submitted for fabrication. The block diagram, schematics of example subcircuits and test features of the buck converter IC are shown in Figure 1.

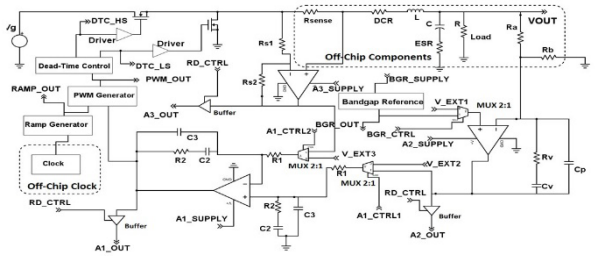

Figure 1. Buck converter test IC block diagram showing enhanced subsystem and power FET testability.

Keywords: Test, Analog, Power, LDO, Buck Converter

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] A. Tulsiram, W. Eisenstadt, Development of LDO Testing and Fault Detection for Ultra Low Defects, IEEE NATW’18, Essex, VT., May 8, 2018.

[2] A. Tulsiram, “Test Techniques to Approach Several Defect-Per-Billion,” SRC Techcon 2018, Austin, TX, Sept. 16-18.

TASK 2712.019, PRE-COMPUTED SECURITY PROTOCOLS FOR ENERGY HARVESTED IOT

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SIGNIFICANCE AND OBJECTIVES

An energy-harvesting IoT device has a limited energy-storage capacity. Cryptographic applications can use pre-computing techniques to instantly use the harvested energy. Pre-computed results are stored efficiently and securely in non-volatile memory. We demonstrate that precomputed cryptography improves the latency in Internet security protocols.

TECHNICAL APPROACH

The feasibility and efficiency of the proposed techniques will be evaluated through an end-to-end demonstrator with an energy-efficient micro-controller and with a wireless communications front-end. We develop techniques to spread out computations over time by reformulating cryptographic algorithms as capable of generating coupons, which are precomputed portions of the algorithm. We propose techniques for coupon generation and their secure storage in non-volatile, possibly off-chip memories. We also consider and optimize the impact of precomputed security protocols on the communication cost and the storage cost. We validate the proposed approach by constructing a prototype implementation on an energy-harvesting oriented microcontroller-based platform.

SUMMARY OF RESULTS

When a computing platform temporarily loses power, it stores its current state in a checkpoint, such that it can recover and continue execution at the point just before storing the checkpoint. A checkpoint also holds pre-computed results (or coupons) to support the execution of a single cryptographic algorithm over multiple power-loss events. We performed a detailed security analysis of storing checkpoints in non-volatile memory. Also, a checkpoint also holds pre-computed results. We identify three possible scenarios that can threaten the security of the checkpointing process: a checkpoint may be snooped (eavesdropped upon), a checkpoint may be spoofed (tampered), and a checkpoint may be replayed. Each of these attacks can lead to loss of information security on the IoT device, or loss of control.

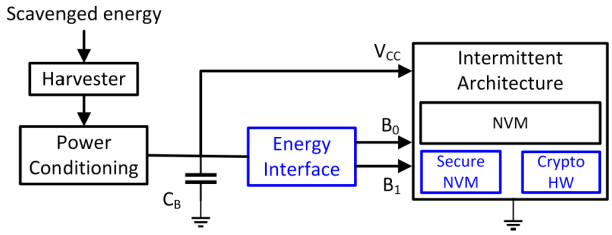

Figure 1. Architecture support for Secure Intermittent Computing builds on secure NVM, hardware crypto acceleration, and a two-bit harvester interface.

To protect checkpoints, we propose the Secure Intermittent Computing protocol (SICP) [1]. SICP encrypts checkpoints in standard NVM, possible off-chip (Figure 1). SICP requires a small secure (tamper-free) NVM protected against unauthorized access. SICP prevents snooping, spoofing, and replay of checkpoints. Also, SICP itself is resistant to power loss, and it ensures the proper ordering of checkpoints. SICP uses authenticated encryption (AEAD). A prototype implementation on Texas Instruments MSP430FR5994 requires 355 ms and 455 ms to store and restore a 2-kilobyte checkpoint securely respectively. The operation of SICP is driven through an energy interface (Figure 1), which drives pre-computing, check-point creation, and power control for the intermittent architecture [2]. We investigated the feasibility of supporting secure intermittent computing without the use of cryptography, and we summarized these requirements in SIA (Secure Intermittent Architecture) [3].

In the final phase of the project, we plan to demonstrate a secure communications link between an intermittent system and a non-intermittent system.

Keywords: Cryptography, energy-harvesting, NVM applications, intermittent computing, MSP430

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] A. Krishnan et al., “Secure Intermittent Protocol: Protecting State against Power Loss,” DATE 2019.

[2] A. Krishnan et al., “Hardware Support for Secure Intermittent Architectures,” ESSA 2019.

[3] D. Dinu et al., “SIA: Secure Intermittent Architecture for Off-the-Shelf Resource-constrained Microcontrollers,” HOST 2019.

TASK 2712.020, LOW-POWER MOSTLY DIGITAL TIME-DOMAIN DELTA-SIGMA ADCS FOR IOT

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SIGNIFICANCE AND OBJECTIVES

The aim of this project is to develop low-power, delta-sigma ADCs for IoT. A purely VCO-based highly digital architecture is investigated in this project. The target is to design high-order, digital delta-sigma ADC with power consumption less than 100uW.

TECHNICAL APPROACH

A modified digital phase-locked loop (DPLL) architecture is used for the proposed ADC design. The analog input perturbs the digitally controlled oscillator (DCO) phase and the DPLL changes the DCO control word to cancel out the phase perturbation. Thus, the DCO control word acts as a quantized representation of the analog input. Ring oscillators are used as DCO and DPLL loop filter, resulting in highly digital architecture and high-order quantization noise shaping. The merits of the proposed ADC are a) no nonlinearity calibration b) excess loop delay can be compensated without requiring auxiliary DAC, and c) inherent DAC mismatch shaping.

SUMMARY OF RESULTS

We fabricated a second-generation 65-nm prototype of the proposed VCO-ADC. Compared to our first-generation prototype [1], the second-generation prototype improves the walden FoM by more than 17x. *The prototype ADC achieves an walden FoM of only 8.6fJ/step and is the first reported CT VCO-ADC to achieve sub-ten fJ walden FoM.*

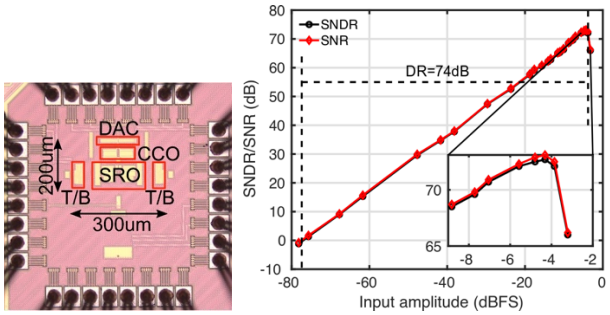

Figure 1. Prototype VCO-ADC and dynamic range plot.

Our second-generation ADC prototype uses a PMOS current-steering DAC to bias the first VCO integrator and replaces the combination of NMOS current-steering DAC and PMOS cascode tail current source for biasing first VCO integrator. Replacement of NMOS DAC+PMOS current source by PMOS DAC reduces both noise and power consumption. We also reduced the quantizer step size by a factor of 6, which reduced the center frequency of first VCO integrator, in turn, reducing VCO thermal noise and power. The reduction of in-band noise also allowed us to reduce ADC sampling frequency while maintaining ADC bandwidth, thus further reducing power. Compared to our first generation prototype, the second generation prototype has 10x lower power consumption while improving SNDR by 6dB.

Figure 1 shows the die photograph of our second-generation ADC as well as the measured dynamic range. The ADC has a dynamic range of 74dB at 1.5MHz bandwidth. We measured 5 ADC chips at different voltage and temperature corners from 0.9-1.1V and 0-50°C. The measured SNDR varied from 69-73dB without any calibration. Table I shows a performance summary of the prototype VCO-ADC.

Table 1. Performance summary.

Tech (nm)	Fs (MHz)	BW (MHz)	Power (mW)	SNDR (dB)	FoM_w (fJ/step)
65	32.6	2.3	0.1	70.2	8.6
		1.5	0.1	72.7	9.9

For the next report period, we will design a third-order VCO-ADC. We will use a MASH technique to increase the order of noise shaping by adding another VCO stage after the second-order ADC. We will add digital calibration circuit to correct inter-stage gain mismatch in the MASH ADC. We will also design novel phase-domain quantization error extraction circuits to extract quantization error of the first stage ADC.

Keywords: ADC, VCO, DPLL, Delta-Sigma, Noise-shaping

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] A. Jayaraj et al., "Highly Digital Second-Order ΔΣ VCO ADC,'', accepted to IEEE TCAS-I, 2019.
[2] M. Danesh et al.,''Ring Oscillator based Delta-Sigma ADCs," (Invited) IEEE ICECS, Dec, 2018, Bordeaux, France.

TASK 2712.023, ULTRA-LOW-POWER COMPRESSIVE SENSING TECHNIQUES FOR IOT APPLICATIONS

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SIGNIFICANCE AND OBJECTIVES

In the era of IoT, huge numbers of sensors are to be deployed. Area and power efficiency are extremely important for the IoT sensors, especially for multi-channel sensor systems. To significantly reduce area, save power and lowering data rate for easier wireless transmission, we apply compressive sensing theory to ADC design aiming for IoT sensors.

TECHNICAL APPROACH

To efficiently apply compressive sensing (CS) theory in multi-channel data conversion systems, a fully-passive CS scheme embedded inside SAR CDAC is proposed. To alleviate the dynamic range loss due to passive summation in the proposed CS scheme, a passive residue amplification is proposed. To support signals that does not fit for the sparsity requirement for CS, an orthogonal sampling based multi-channel conversion mode is available without added circuit complexity.

SUMMARY OF RESULTS

Fig.1 shows the proposed multi-channel CS-based ADC framework. M-channel input signals $(\overrightarrow{s_1}, \overrightarrow{s_2}, \dots \overrightarrow{s_M})$ are first multiplied with pseudo-random binary sequences (PRBS) $(\overrightarrow{p_1}, \overrightarrow{p_2}, \dots \overrightarrow{p_M})$, respectively, and then summed together to be converted by the ADC. The output data $\overrightarrow{y_D}$ is then used to reconstruct the quantized signal of each channel $(\overrightarrow{s_1^*}, \overrightarrow{s_2^*}, \dots \overrightarrow{s_M^*})$ off-chip. To mitigate the noise performance degradation brought by passive voltage averaging during the CS encoding process, we proposed a passive residue amplification technique which adds a passive gain of 2 during SAR conversion.

Fig. 2 shows the schematic of the proposed 4-channel CS-based SAR ADC with a passive amplification technique. The MSBs of the SAR CDAC along with the residue boosting capacitor are split evenly for 4-channel sampling. Before reconfiguration $(\Phi_R = 0)$, the boosting capacitor (C_B) is connected in parallel with the SAR CDAC to assist with sampling. After reconfiguration $(\Phi_R = 1)$, C_B is stacked on CDAC to passively amplify the residue voltage.

The proposed multi-channel CS SAR ADC is designed in a 40-nm CMOS technology. The design is sent for fabrication. The active area of the design is 0.055mm^2. Simulated under 1V supply and 1MS/s sampling rate, the ADC consumes 6.67µW where comparator, CDAC and digital logics consumes 1.5µW, 1.37µW and 3.8µW, respectively. With a single channel input at Nyquist rate, the SNDR is simulated to be 69.3 dB, resulting in a Walden-FoM of 2.82fJ/conv-step. When the proposed passive residue amplification technique is disabled, the SNDR drops to 65.4 dB, demonstrating the effectiveness of the proposed technique. Operating in CS mode, 4-channel sparse signals are recovered by SL0 algorithm. Operating in an orthogonal sampling mode, the output signal of each channel is recovered by multiplying the ADC output with the respective channel encoding sequence and digitally filtered by a 10th order IIR filter.

For future works, the possibility of applying the proposed fully-passive compressive sensing framework into IoT image sensor is being studied.

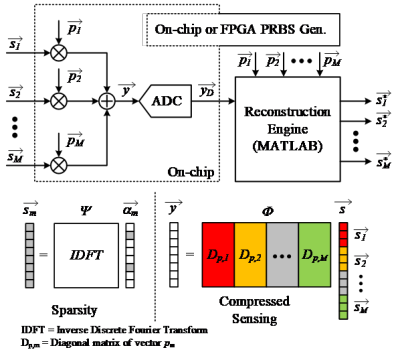

Figure 1. Proposed Multi-channel CS-based ADC framework.

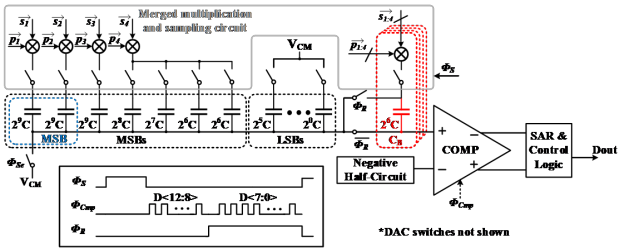

Figure 2. Proposed 4-channel CS-based SAR ADC with passive residue amplification technique.

Keywords: compressive sensing, wireless sensor front-end, IoT applications, ultra-low-power data converter, multi-channel ADC

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] W. Guo et al., "A Fully Passive Compressive Sensing SAR ADC for Low-Power Wireless Sensors," in IEEE Journal of Solid-State Circuits, vol. 52, no. 8, pp. 2154-2167, Aug. 2017.

TASK 2712.024, A SYSTEM-IN-PACKAGE PLATFORM FOR ENERGY HARVESTING AND DELIVERY FOR IOT EDGE DEVICES

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MADHAVAN SWAMINATHAN, GEORGIA INSTITUTE OF TECHNOLOGY

SIGNIFICANCE AND OBJECTIVES

The proposed research aims to design a System-In-Package (SIP) based energy delivery system for powering wireless sensor nodes and IoT edge devices. We propose to develop a multi-chip SIP, with multiple energy transducers, on-package passives (magnetic core inductor and high-density capacitor), a power management unit (PMU) with a boost/buck voltage regulator (VR), and the load device.

TECHNICAL APPROACH

We will develop the architecture of the proposed system-in-package based energy harvesting and delivery system. We will design and fabricate an on-package inductor for the proposed energy delivery system. We will design, fabricate a test the power management unit of the proposed SiP. The power management unit will consist of a boost/buck regulator to harvest from multiple sources and powering multiple output domains. Finally, we will design, fabricate, and characterize the multi-chip SiP to demonstrate the proposed energy-harvesting system. The SiP will integrate the PMU and passives designed in this program with an off-the shelf energy harvester and in-house designed load device.

SUMMARY OF RESULTS

Tape-out of PMU Test-chip: We have taped out a test-chip in 65-nm CMOS for a self-powered system using on-chip or off-chip photodiodes. The design includes on-chip photodiodes for harvesting, a boost regulator with system based MPPT, and an encryption engine as a load.

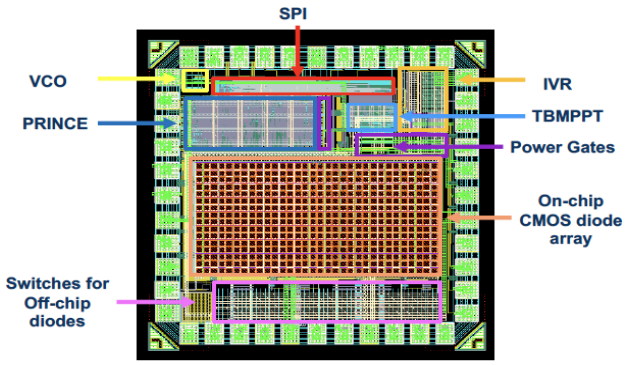

Figure 1. Full-chip layout of the PMIC test-chip.

Fabrication of Inductors: We have fabricated initial designs of a planar spiral inductor for the PMU. These inductors were fabricated using screen-printing on a copper-backed, Kapton polyimide substrate Based on measurements for the initial designs, the change in the inductor's response due to bending must be improved. In these measurements, the inductance varied significantly depending on the amount the inductor is bent. Therefore, further improvements in the inductor's design are required.

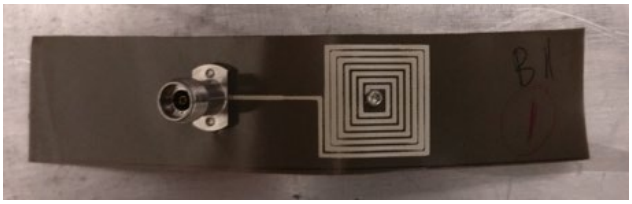

Figure 2. Top view of fabricated inductor sample.

Keywords: Integrated voltage regulator, self-testing, and self-tuning.

INDUSTRY INTERACTIONS

Intel

MAJOR PAPERS/PATENTS

[1] E. Lee, et. al, "A System-In-Package based Energy Harvesting for IoT Devices with Integrated Voltage Regulators and Embedded Inductors," Electronic Component and Technology Conference (ECTC), 2018.

[2] S. Sivapurapu, et. al, "*Multi-physics Modeling Characterization of Aerosol Jet Printed Transmission Lines,*" 2018 IEEE MTT-S International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization (NEMO), Reykjavik, 2018, pp. 1-4.

TASK 2712.027, GATE DRIVING TECHNIQUES AND CIRCUITS FOR AUTOMOTIVE-USE GAN POWER CIRCUITS

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SIGNIFICANCE AND OBJECTIVES

In high switching frequency GaN power converters, high driving current is necessary to reduce the gate driving signal rising time. But the drastic di/dt and dv/dt transitions induce high switching node voltage and current spikes. It will induce V_{DS} breakdown of GaN. The proposed gate driver both supports high switching frequency operation and improves system reliability.

TECHNICAL APPROACH

To mitigate switching node voltage and drain current spikes during high-side GaN turn-on transition and to reduce high frequency EMI noise, an adaptive tri-slope gate driving scheme is proposed. Instead of solely using a conventional fixed current gate driving scheme, through sensing load current I_O and input voltage V_{IN} level, three different driving currents are predefined to provide a tri-slope charging profile of high side GaN FET. It can not only realize short gate driving signal rising time but also reduce switching node voltage and current spikes.

SUMMARY OF RESULTS

The proposed GaN driving stage with adaptive tri-slope gate driver is shown in Fig. 1. The gate capacitance of high side GaN FET M_H includes gate-source capacitance C_{gs} and miller capacitance C_{gd}. The parasitic inductance and resistance are present at the source and drain terminals of M_H. The basic operation scheme of the adaptive tri-slope gate driver is shown in Fig. 2.

When the driving signal V_{PWM} goes high, V_{GL} changes to low. Then V_{DH} is triggered high by a high speed up level shifter. In an adaptive tri-slope gate driver, V_{GH} starts to get charged initially with a current of I_{M1}, which is inversely proportional to I_O. After V_{GH} reaches the threshold voltage V_{th}, M_H starts conducting and drain current I_{DH} rises. For a high I_O, a low I_{M1} is modulated. V_{GH} charges from V_{th} to V_{MP} within a time period of t_{p1} until M_H enters the Miller plateau region. At t_2, I_{DH} reaches the peak value of inductor current. The slew rate of I_{DH} can be modulated by adjusting the gate charge current I_{M1}. If I_O is low, I_{M1} is modulated high to charge V_{GH}. Therefore, the period that V_{GH} rises from V_{th} to V_{MP} is reduced to t_{p1}' ($<t_{p1}$). In the second phase, V_{SW} rises with a gate charge current of $I_{M1}+I_{M2}$ until V_{SW} reaches V_{IN}. For low V_{IN}, V_{SW} is charged up to V_{IN} earlier resulting in a shorter t_{p2}' ($<t_{p2}$). In this way, the rising slopes of I_{DH} and V_{SW} are adaptively adjusted. The overshoot voltage spike and ringing at V_{SW} are greatly suppressed, protecting GaN FETs from V_{DS} breakdown. As V_{GH} goes slightly higher than $2V_{th}$, V_{GH} is charged up by a large charge current, $I_{M1}+I_{M2}+I_{M3}$. With a much faster charging in t_{p3} period, V_{GH} settles quickly to ensure low conduction loss. In addition to these gate driving techniques, one two-phase double step-down GaN power converter will be designed for high frequency DC-DC power conversion.

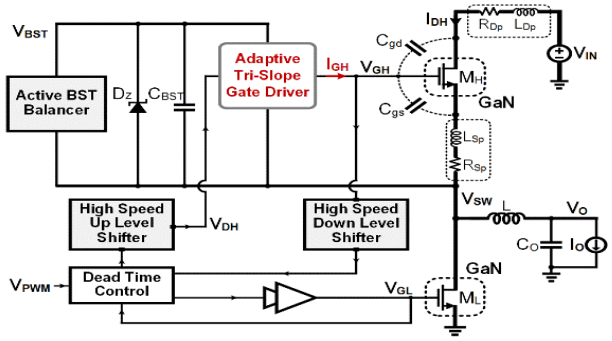

Figure 1. GaN driving stage with adaptive tri-slope gate driver.

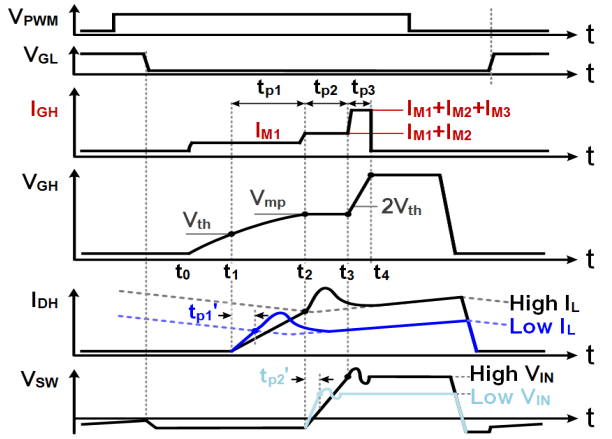

Figure 2. Operation scheme of adaptive tri-slope gate driver.

Keywords: GaN driver, ringing suppression, tri-slope gate driving, high switching frequency, high efficiency

INDUSTRY INTERACTIONS

Texas Instruments, NXP, IBM

MAJOR PAPERS/PATENTS

[1] D. Yan et al., "Integrated Single-Stage Bi-directional UPS with One-Cycle Mode Switching and Active Deadtime Control for Automotive Electronics," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 2081-2085.

TASK 2712.028, HIGH PERFORMANCE MICRO-SUPERCAPACITOR ON A CHIP BASED ON A HIERARCHICAL NETWORK OF NITROGEN DOPED CARBON NANOTUBE SHEETS SUPPORTED MNO_2 NANOPARTICLES

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SIGNIFICANCE AND OBJECTIVES

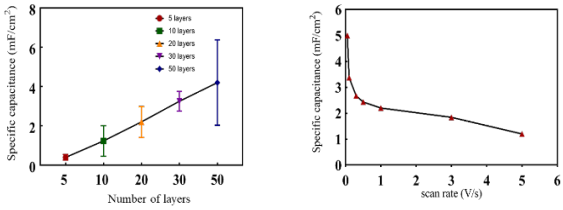
This work is focused on characterization and improvement of electrochemical performance of micro supercapacitors.

TECHNICAL APPROACH

In order to study the performance of the micro-supercapacitors, carbon nanotube sheets were stacked on insulating substrates to avoid leakage current. We used micro glass slides. Using a plasma patterning approach micro-supercapcitors with an interspacing of 140 μm were fabricated and were tested via cyclic voltammetry, electrochemical impedance spectroscopy and charge/discharge tests. We also studied the effect of number of CNT layers (or thickness) on the performance of the microsupercapcitors. In another study, manganese oxide was deposited on the active areas of the device with ten layers to improve the specific capacitance and energy density.

SUMMARY OF RESULTS

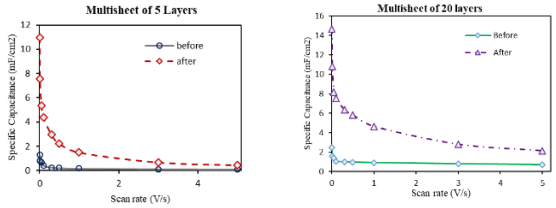
Micro supercapacitors based on a horizontal CNT sheet with interdigital structure are being characterized for the first time. Energy storage devices were chacratrized using an aqueous solution of Na_2SO_4. We will continue the experiments with doping and all solid state device on flexible substrates, and long term stability of the devices will be investigated (over 10,000 cycles). Here the performance of variable CNT multisheet layers (5-50 layers) at scan rate of 50mV/s is demonstrated in Figure 1. As shown, adding more layers of CNT sheets as expected increases the specific capacitance due to an increase of active materials to store more charges in pores. Each data points are averaged over five devices with the same thickness. Figure 1(b) reveals a high rate capability of 1.2mF/cm^2 for a 50-layer device at scan rate of 50mV/s (higher than what is reported so far for CNT based devices). The active surface area of the devices was 0.21cm^2 with 12 fingers in total. Manganse oxide was electrodposited via a three-electrode system using the CNT sheet as a working electrode, and a platinum wire and Ag/AgCl as counter and reference electrodes, respectively. The measured results for devices with multisheet of 5 and 20 layers are presented in Figure 2.



(a) (b)

Figure 1. (a) Specific capacitance as a function of CNT sheet thickness (5 to 50 layers); and (b) scan rate (from 50 mV/s to 5 V/s) for liquid electrolyte.

Enhancement of specific capacitance (one order of magnitude) is due to synergistic effect of pseudo capacitance coming from oxide and double layer capacitance from carbon nanotube sheets and comparable to most recent works on thin film supercapcitor devices.



(a) (b)

Figure 2. (a) Specific capacitance as a function of CNT sheet thickness (5 layers) and scan rate (from 50mV/s to 5V/s) for liquid electrolyte before and after MnO_2 deposition, (b) (20 layers)

Keywords: Carbon nanotube sheet, microsupercapacitor, metal oxide, micro-device, energy storage

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Provisional patent entitled “A facile method to pattern novel structure of carbon nanotube sheets in micro-scale on a chip, sensors, transparent electrodes, and optoelectronic devices,” USPTO (62/748,506), Oct. 2018.

[2] B. Dousti et al., “Miniaturized electrochemical supercapacitor with patterned horizontally aligned carbon nanotube sheets , Oral presentation to ECS meeting, May 26-30, 2019.

TASK 2810.002, SECURITY-AWARE DYNAMIC POWER MANAGEMENT FOR SYSTEM-ON-CHIPS

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SIGNIFICANCE AND OBJECTIVES

The proposed research investigates the energy-security trade-offs associated with Dynamic Power Management (DPM). The proposed effort will develop methodology to characterize security implications of DPM in SoCs and design circuit/system techniques to co-optimize security and energy-efficiency of DPM.

TECHNICAL APPROACH

This effort will purse a cross-layer approach to understand the energy-security trade-offs in Dynamic Voltage Frequency Scaling (DVFS). First, we will design power domains that are secure against power-/EM- side-channel analysis by leveraging the distributed integrated voltage regulators. Next we will investigate energy-security trade-off at the chip level by focusing on the DVFS controller and algorithm. Finally we will explore an integrated approach considering secure power domains and secure DVFS controllers.

SUMMARY OF RESULTS

Power and Electromagnetic Side-Channel Security using Digital Low-droput Regulator: We have demonstrated improved power and electromagnetic (EM) side channel attack (SCA) resistance of a 128-bit AES engine via an on-die security-aware all-digital low-dropout regulator (DLDO). Power and EM side-channel measurements of the designed 130-nm CMOS test-chip demonstrates 3579× increase in the minimum number of traces required to disclose 80% bytes of the encryption key with only 10.4% performance loss of the AES engine.

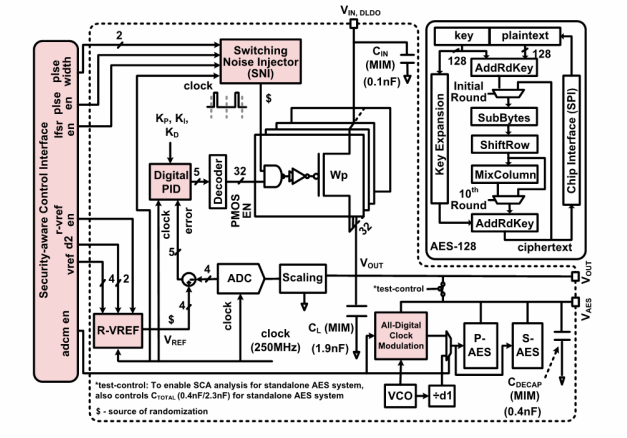

Figure 1. Architecture for digital LDO based power and electromagnetic emission side channel security.

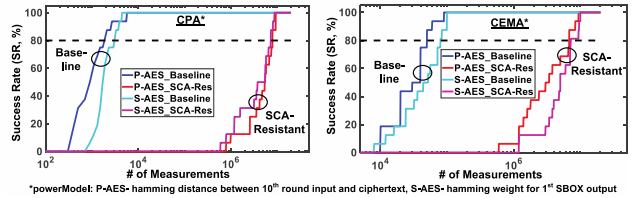

Figure 2. Power and EM-based SCA measurement results.

Fault-Attack Prevention using All-digital Clock Modulation: We have experimentally demonstrated that an on-chip integrated fast all-digital clock modulation (F-ADCM) circuit can be used as a countermeasure against supply glitch and temperature variations-based fault injection attacks (FIA). F-ADCM modulates clock edges in presence of DC/transient supply glitches and temperature variations to ensure correct operation of the underlying cryptographic circuit. With a testchip manufactured in a 130-nm CMOS technology, we first demonstrated an inexpensive methodology to conduct a fault attack on hardware implementation of a 128-bit advanced encryption standard (AES) engine using externally controlled supply glitches. Next, we showed that with F-ADCM circuit, it is no longer possible to inject supply/temperature glitch-based faults even after 10 million encryptions across varying operating conditions.

Keywords: secure, side-channel, dynamic power management, integrated voltage regulator, dynamic voltage frequency scaling

INDUSTRY INTERACTIONS

Intel, IBM

MAJOR PAPERS/PATENTS

[1] A. Singh, et. al., "Improved Power/EM Side Channel Attack Resistance of 128-bit AES Engines with Random Fast Voltage Dithering," *IEEE* JSSC*, Feb. 2019*

[2] N. Chawla, et. al., "Extracting side-channel leakage from round unrolled implementations of lightweight ciphers," IEEE HOST, 2019.

[3] A. Singh, et. al, "A 128b AES Engine with Higher Resistance to Power and Electromagnetic Side-Channel Attacks Enabled by a Security-Aware Integrated All-Digital Low-Dropout Regulator," *IEEE ISSCC* 2019.

[4] A. Singh, et. al, "Mitigating Power Supply Glitch based Fault Attacks with Fast All-Digital Clock Modulation Circuit," DATE, March 2019.

TASK 2810.003, INTEGRATED VOLTAGE REGULATOR MANAGEMENT FOR SYSTEM-ON-CHIP ARCHITECTURES

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SIGNIFICANCE AND OBJECTIVES

We propose to investigate the implication of integrated voltage regulators (IVRs) from a holistic system-level power optimization perspective that is able to account for higher-level temporal workload and spatial chip-wide execution characteristics in order to achieve maximum efficiency in future heterogeneous systems.

TECHNICAL APPROACH

We start with developing an accurate and fast circuit-level IVR analytical modeling tool called Ivory that performs static and dynamic analysis and design space exploration for IVR-enabled power delivery system (PDS). We then characterize the power activities and supply variations across different IP blocks to capture their performance and power trade-offs under different power delivery solutions. Finally, we will thoroughly explore feedback-directed prediction-enhanced optimization, and will develop scheduling algorithms and techniques at the firmware and operating system to make efficient use of IVRs.

SUMMARY OF RESULTS

We developed Ivory, a design space exploration tool capable of providing accurate conversion efficiency, static performance characteristics, and dynamic transient responses of IVR-enabled PDS, facilitating rapid trade-offs exploration at the early design stage.

Voltage stacking (VS) is another novel PDS configuration that can fundamentally improve power delivery efficiency (PDE) by series-stacking multiple voltage domains to eliminate explicit step-down voltage conversion and reduce energy loss along power delivery path. However, VS suffers aggravated supply noise from imbalanced current, preventing its adoption in mainstream systems.

We start by developing an analytical model to capture the essential noise behaviors in VS. It allows us to identify the dominant noise contributors are low-frequency residual current and high-frequency global current. Charge-recycling IVRs can be used to mitigate these two types of supply voltage noise. To guarantee the worst case supply voltage noise, charge-recycling IVRs have to incur a large on-chip area overhead, which is not practical in real applications. We propose two practical VS system solutions: hybrid regulation [1] and control theory based power management [2], which can guarantee the worst supply noise with the acceptable on-chip area. Hybrid regulation adopts an off-chip charge-recycling voltage regulator module for slow and persistent current imbalances of large magnitudes and an on-chip distributed charge-recycling IVR to deal with fast transient current imbalances with smaller magnitudes. Control theory based power management models the VS as a dynamic system and uses the feedback control theory to manage power consumption at the architecture level to avoid huge imbalance reducing the burden of charge-recycling IVRs. Moreover, we also evaluated the compatibility of advanced power saving techniques in VS systems [3]. The comparison of proposed VS systems and other power delivery systems is shown in Table 1.

Table 1. Power delivery system comparison.

PDS Configuration	Eff.	Die Area	Reliable
Single layer VRM	79.9%	N/A	Yes
Single layer IVR	85.8%	172.3mm^2	Yes
VS IVR (worst)	92%	88.3(921) mm^2	No(Yes)
VS hybrid [1,3]	93.5%	82.4mm^2	Yes
VS power manage [2]	92.3%	105.8mm^2	Yes

Our next step is to refine Ivory to enable hierarchical composition of the PDS network, as well as to analytically formulate the PDS vulnerability to side channel attacks with and without IVRs. Our enhanced model will be able to analytically evaluate the risk of information leakage and fault injection attacks via shared power delivery resources.

Keywords: integrated voltage regulator, power delivery system, voltage stacking, power efficiency, security

INDUSTRY INTERACTIONS

Intel, IBM, ARM

MAJOR PAPERS/PATENTS

[1] Zou, An, et al. "Efficient and reliable power delivery in voltage-stacked manycore system with hybrid charge-recycling regulators." 2018 DAC, San Francisco, CA, USA.

[2] Zou, An, et al. "Voltage-Stacked GPUs: A Control Theory Driven Cross-Layer Solution for Practical Voltage Stacking in GPUs." 2018 MICRO, Fukuoka, Japan.

[3] Zou, An, et al. "Voltage-Stacked Power Delivery Systems: Reliability, Efficiency, and Power Management" 2019 TCAD (in preparation)

TASK 2810.006, COMBATING UNPRECEDENTED EFFICIENCY, NOISE AND FREQUENCY CHALLENGES IN MODERN HIGH CURRENT INTEGRATED POWER CONVERTERS

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SIGNIFICANCE AND OBJECTIVES

There is a classic design trade-off between EMI noise and power efficiency in switching power circuits. To minimize the EMI emission while limiting the increase of switching loss, a gate switching techniqes with low di/dt and high dv/dt is needed. For this, an adaptive Miller Plateau sensing is proposed here. Moreover, a continuous spread-spectrum modulation (C-RSSM) technique is developed to further reduce EMI. Meanwhile, a one-cycle on-time rebalancing scheme mitigates RSSM-induced output jittering effect.

TECHNICAL APPROACH

To implement the adaptive Miller Plateau detection for independent control of low di/dt and high dv/dt, a low power isolated negative voltage sensor is designed to detect the deep negative voltage $-V_{FW}$, avoiding the severe reliability issues induced by the conduction of parasitic junction transistors. Moreover, a dynamic error compensator is used to sense the on-voltage (V_{DSON}) of the low side GaN switch, eliminating the error between V_{MP} and V_{FW} due to the asymmetrical GaN device structure. At the same time, a C-RSSM is proposed to improve the EMI attenuation by eliminating the finite frequency resolution issue in conventional discrete RSSM (D-RSSM).

SUMMARY OF RESULTS

To achieve adaptive Miller Plateau sensing, an emulated Miller Plateau tracking (EMPT) scheme is proposed. Fig. 1 shows the circuit implementation, including a low power isolated negative voltage sensor and a dynamic error compensator. During the current freewheeling period, the switching node V_{SW} is discharged to a deep negative voltage $-V_{FW}$. Direct sensing of such a high negative voltage may turn on the parasitic junction transistors due to high leakage current, leading to high power consumption and reliability issues.

To combat these issues, an isolated sensing capacitor, C_{sen} is inserted to detect the step-down transition of V_{SW} from $-V_{DSON}$ to $-V_{FW}$ at the instant when M_L is turned off. Then its magnitude, $V_{FW}-V_{DSON}$, is converted by a V-to-I subtractor. The dynamic error compensation is added based on GaN model to calibrate the slight mismatch between V_{MP} and V_{FW} due to the asymmetrical drain-source structure of GaN FET.

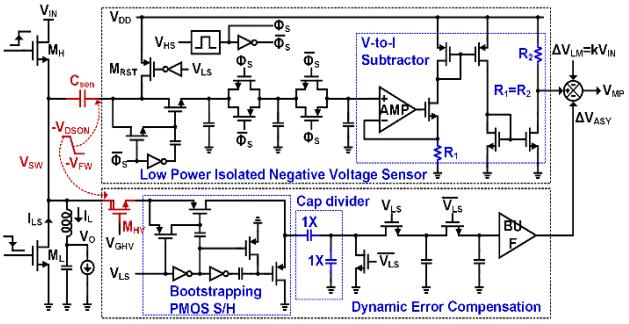

Figure 1. Circuit implementation of EMPT scheme.

To further suppress EMI , SSM techniques are explored, which distribute the energy at the switching frequency and its harmonics into a broader frequency range through frequency modulation. Here, a C-RSSM is proposed to spread the spurious noise continuously and uniformly. As illustrated in Fig. 2, although conventional D-RSSM could achieve similar peak EMI reduction with a wider modulation range, it elevates noise floor significantly due to spectral overlap. In the proposed C-RSSM, peak EMI is effectively attenuated at the minimal cost of noise floor elevation.

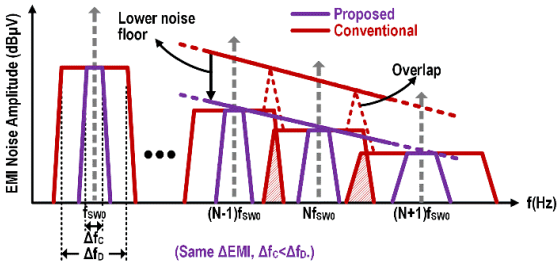

Figure 2. EMI spectrum plot by applying RSSM techniques.

In the following year, the adaptive MP sensing technique will be applied to balance EMI noise and power efficiency. For C-RSSM scheme, a Markov-chain-based random clock generator will be implemented.

Keywords: di/dt and dv/dt control, adaptive MP sensing GaN FET, C-RSSM, one-cycle on-time rebalacning

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Y. Chen and D. Ma, "An 8.3MHz GaN power converter using Markov continuous RSSM for 35dBμV conducted EMI attenuation and one-cycle T_{ON} rebalancing for 27.6dB V_O jittering suppression," ISSCC, Feb. 2019.

TASK 2810.008, CIRCUIT TECHNIQUES FOR FAST START-UP OF CRYSTAL OSCILLATORS

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SIGNIFICANCE AND OBJECTIVES

High-Q crystal oscillators (XOs) are notorious for being extremely slow at start-up. Their long start-up time increases the average power consumption in duty-cycled systems such as Internet-of-Things. The objective of this work is to reduce the start-up time with minimal energy consumption.

TECHNICAL APPROACH

Previously, we demonstrated the fastest reported XO start-up (~100 cycles only, ~15x faster than prior art [1]) using resonator pre-energization in a Pierce topology using a low-Q injection oscillator for a precisely-calculated, short injection duration, T_{inj}. Our last report described a method that adapts T_{inj} (using to a coarse temperature sensor) to maintain quick startup even with +/-9,000ppm injection frequency mismatch. In the current review period, we theoretically analyzed various injection strategies e.g., single-tone, chirp and dithered frequency injection, and ours. In addition, we also extended our precise injection quick startup technique to a new series resonance 32-kHz XO based on DC-only amplification.

SUMMARY OF RESULTS

Our theoretical analysis is based on the premise that the efficacy of a given injection technique – i.e., both the startup time and the sensitivity to injection frequency mismatch – depends strongly on the power spectral density (PSD) of the injection signal. We had shown earlier that, in our technique, the small T_{inj} results in an injection signal with a wide-band PSD: wide enough to overlap the narrow crystal resonance even in the presence of large frequency mismatch. Even for techniques that chirp or dither the injection frequency, the injection signal has a wide band PSD. The difference, however, lies in how wide band the injection signal PSD is, and to a lesser degree, its shape. Our analysis, described in [1], quantified this aspect. For instance, chirping can result in a much wider band PSD than our technique, and hence, can tolerate a larger injection frequency error. However, it still takes longer for the oscillator to startup, as shown in Figure 1. As a result, chirping also requires proportionately higher startup energy than our technique. In the next review period, we will investigate an optimum "injection profile" (Figure 2) derived from this analysis, to simultaneously reduce startup time (and hence, startup energy) and improve tolerance to injection frequency errors. As shown, the injection frequency is "chirped", but in discrete steps, and at each step, a very short, precise injection duration will be employed.

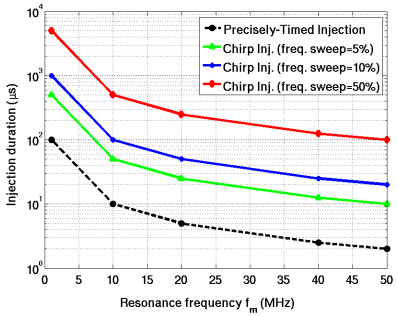

Figure 1. Optimal injection duration of precisely-timed injection technique compared to the chirp injection technique versus oscillation frequencies.

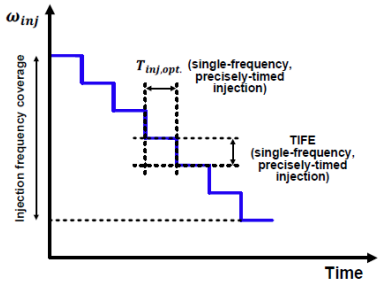

Figure 2. Proposed injection profile.

Furthermore, in this review period, we extended the quick startup technique to a new XO topology, one that employs DC-only sustaining amplifiers and series resonance operation. We achieved the lowest reported power consumption of 0.55-nW for a 32-kHz XO [2].

Keywords: start-up time, crystal oscillators, low power, oscillator sustaining amplifiers, real time clocks

INDUSTRY INTERACTIONS

Intel

MAJOR PAPERS/PATENTS

[1] H. Esmaeelzadeh, "Low-Energy Clock Generation for IoT Applications," Ph.D. Thesis, UCLA, 2019.

[2] H. Esmaeelzadeh, S. Pamarti, "A 0.55nW/0.5V 32kHz Crystal Oscillator Based on a DC-Only Sustaining Amplifier for IoT," ISSCC 2019.

TASK 2810.009, MIXED-SIGNAL BUILDING BLOCKS FOR ULTRA-LOW POWER WIRELESS SENSOR NODES

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DAVID BLAAUW, UNIVERSITY OF MICHIGAN

SIGNIFICANCE AND OBJECTIVES

This project develops novel and state-of-art performing ultra-low power mixed-signal circuits, suitable for IoT systems. This includes timekeeping circuits, amplifiers, and CMOS-based sensors.

TECHNICAL APPROACH

The most challenging ultra-low power circuit components are mixed-signal circuits such as timers, clock sources, sensing and interface circuits (e.g., temperature sensors and low-noise amplifiers). Some of these cannot be duty cycled (e.g., timers), while others require both low noise and low power (e.g., amplifiers), which are traditionally mutually exclusive. This work proposes new ULP designs for: 1) crystal oscillator based real time clocks (RTCs), 2) temperature-compensated wakeup timers, 3) temperature sensors, and 4) front-end low-noise amplifiers.

SUMMARY OF RESULTS

We proposed a 32-kHz crystal oscillator (XO) with duty-cycled energy injection. The design techniques we proposed are: (1) NMOS-only pulsed driver to realize 71% injection efficiency; (2) duty-cycled pulses of energy injections at peaks and valleys of the XO waveform to greatly reduce the dynamic power of the control circuits; (3) a current reference with switched-capacitor resistance and ultra-low leakage switches to provide precise current in the presence of PVT variations; (4) a constant-delay clock slicer to both convert the sinewave XO waveform to a square wave and generate delays for timing of the energy injection. Figure 1 shows the architecture of the proposed 32-kHz crystal oscillator.

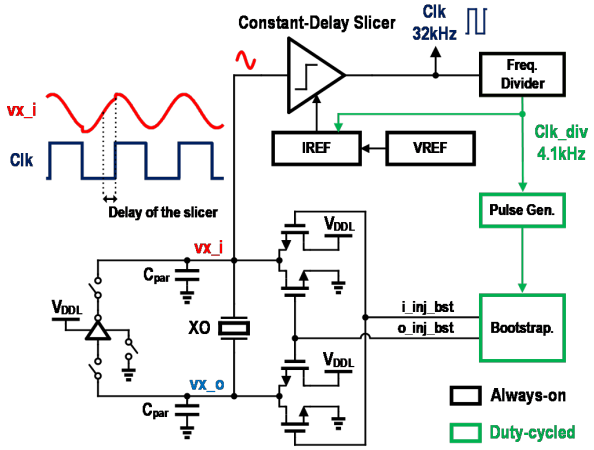

Figure 1. Architecture of the proposed crystal oscillator.

The proposed XO is designed in a 40-nm CMOS process and the layout area including the start-up circuit is 0.02 mm^2. With two power supplies, 0.5V and 0.15V, ECS-1X5X crystal, 1pF load capacitance, and 141mV oscillation amplitude across the crystal, the simulated power consumption is 0.47nW at 25°C, which is the lowest for the reported 32-kHz crystal oscillators.

Keywords: CMOS, crystal oscillator, ultra-low power

INDUSTRY INTERACTIONS

NXP

MAJOR PAPERS/PATENTS

TASK 2810.010, GS/S ADC BASED CYCLE-TO-CYCLE CLOSED-LOOP ADAPTIVE SMART DRIVER FOR HIGH-PERFORMANCE SIC/GAN POWER DEVICES

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SIGNIFICANCE AND OBJECTIVES

Silicon-Carbide and Gallium-Nitride power devices can be driven at high frequencies but the gate drivers for these devices suffer from a tradeoff between electromagnetic interferences (EMI) and power efficiency. The objective of this research is to demonstrate a SiC/GaN driver that can maximize the power efficiency while meeting the EMI requirements.

TECHNICAL APPROACH

We propose a smart gate driver capable of evaluating the EMI and minimize EMI over the entire frequency band. At low frequencies, a low-frequency noise compression (LNC) circuit generates a dithered driving signal to significantly compress the noise spectrum. At high frequencies, Gaussian transition is implemented by regulating the gate driving strength of GaN device which can theortically eliminate the harmonic noise above the first pole frequency. With these two approaches, the proposed driver chip can meet the EMI requirements over the entire band. A GS/s ADC is designed and utilized to evaluate the EMI.

SUMMARY OF RESULTS

A. Overall Topology of the Proposed Gate Driver and Operation Principle

Figure 1(a) depicts a schematic of a typical half-bridge buck converter with the proposed smart gate driver. A LNC circuit provides a jittered PWM signal with a compressed noise level at low freqencies. To precisely track the trajectory of the Gaussian reference, six gate-driving modules operate back-to-back throughout the switching-on duration.

A resistive divider is connected to the switching node to sample switching node waveform, V_{sw} and provides a feedback signal. By comparing the feedback signal with a Gaussian reference, a Gaussian transition on the switching node is implemented.

A GS/s ADC [1-2] is included in the system level to monitor the ringing which reflect the EMI levels. According to the ringing magnitudes, the driving strength of the GaN device can be adjusted to balance the EMI level and power efficiency cycle-by-cycle.

B. Simulation Results of Voltage/Current waveform at Switching Node.

The proposed driving circuits is implemented using a 0.18-µm BCD Process as shown in Fig. 1 (b). The measured peak EMI noise over a wide frequency range from 2MHz to 500MHz is shown in Fig. 2. As can be seen, when using Gaussian regulation (b), the Gaussian spectrum envelope is observed, which shows a dip around 100MHz. Due to the imperfection of Gaussian switching in the real design, three noise lobes below -40dBm are observed. Combined with the dithering scheme (c), the peak EMI reduction at mid-frequency range from 100MHz to 200MHz is more than 15dB. Above 250MHz, the measured EMI noise level is -65dBm (41.99dBuV) approaching the background noise level.

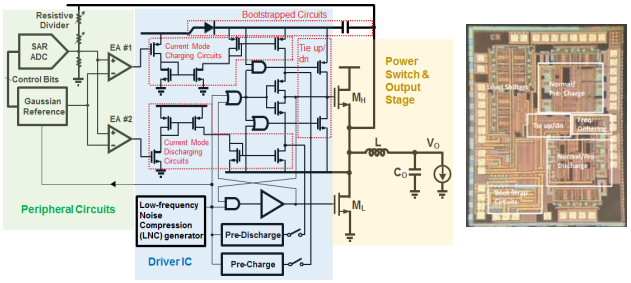

Figure 1. (a) Architecture of a half-bridge buck converter with the smart gate driver. (b) chip microphotograph.

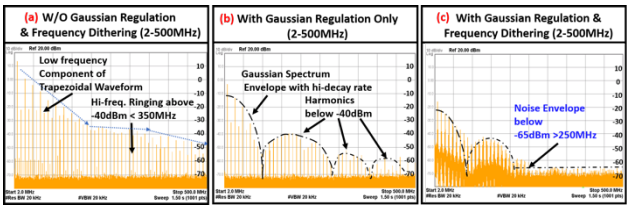

Figure 2. Measured EMI noise over a frequency range from 2MHz to 500MHz.

Keywords: GaN driver, Gaussian transition regulation, high-speed ADC, smart driver, EMI regulation

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] K. Sun et al., "A 56 GS/s 8-bit time-interleaved ADC with ENOB and BW enhancement techniques in 28 nm CMOS", IEEE JSSC 2019.

[2] G. Wang et al., "A 43.6-dB SNDR 1-GS/s 3.2-mW SAR ADC with Background Calibrated Fine and Coarse Comparators in 28 nm CMOS", IEEE TVLSI 2019.

TASK 2810.011, MICRO-POWER ANALOG-TO-DIGITAL DATA CONVERTERS FOR SENSOR INTERFACES

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SIGNIFICANCE AND OBJECTIVES

Sensors using MEMS (Micro Electro Mechanical System) have many applications in automotive electronics, IoT, and communications. They allow the fabrication of electronics and mechanical devices on the same silicon chip. MEMS interface circuits require data converters with high accuracy and power efficiency. This project is developing such analog-to-digital converters.

TECHNICAL APPROACH

We have developed a novel active noise-shaping SAR ADC. It is based on a two-capacitor DAC, embedded in a high-accuracy digitally corrected circuit. To mitigate the effects of non-idealities noise filtering, correlated double sampling and correlated level shifting are used. These techniques correct the non-idealities of the opamp used. Also, to cancel the affects of mismatches and parasitic capacitors, the complete circuit is calibrated using a novel bit-by-bit digital correction technique. This process accurately calculates the conversion error for each bit. These errors are then saved in a look-up table, and used to enhance the conversion accuracy.

SUMMARY OF RESULTS

The simplified circuit of the active noise-shaping SAR A/D converter is shown in Figure 1. The circuit includes the two-capacitor DAC (C1 and C2), the amplifier with integrating capacitors (C3), correlated double sampling capacitors (C4) and correlated level shfting capacitors (CLS). By saving the conversion residue in C3, first-order error shaping is achieved. Higher order error shaping can also be economically obtained by using a few additional capacitors and switches.

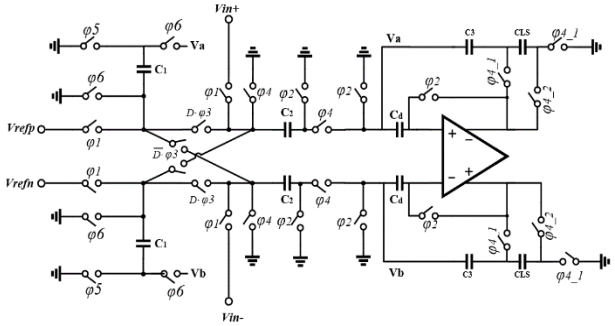

Figure 1. Simplified circuit diagram of the active noise-shaping SAR ADC.

The calibration process consists of converting the ADC into a single-bit incremental analog-to-digital converter. Feeding in digital codes, each containing a single bit '1' and all others equal to '0', the actual weights of all bits can be accurately acquired in digital form. These results can then be stored, and during conversion used to correct the digital outputs. The calibration need not be performed for all the bits, only a limited number of the most significant ones. Even a small number of corrected bits improves the SNR, but not the harmonic distortion. Table 1 illustartes the improvement achieved for increasing number of calibrated bits.

Table 1. Calibration with different numbers of bits.

# of MSBs calibrated	SNR(dB)	SNDR(dB)
1	92.9	63.7
2	91.6	73.6
3	92.9	73.0
4	94.6	90.2
5	97.9	89.1
6	98.5	96.4
7	98.5	96.3

The device implementing our latest design is now in the final simulation and early layout phase. We plan to complete the hardware design next. Afterwords, more involved systems, based on higher order algorithms, will be designed. They are in the planning phase.

Keywords: active noise-shaping SAR ADCS, ADCs for MEMS, high-accuracy ADCs, sensor interfaces.

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

[1] Shi, L., Zhang, Y. Wang, Y. Kareppagoudr and Temes, G.C., "A 13b ENOB Noise Shaping SAR ADC with a Two-Capacitor DAC," IEEE International Midwest Symposium on Circuits and Systems, Windsor, Ont, August 5-8, 2018.

[2] Shakya, J. and Temes, G.C., "Predictive Noise-Shaping SAR ADC," IEEE Internat. Circuits and Systems Symp., Sapporo, Japan, 2019.

TASK 2810.012, NPSENSE – NANO-POWER CURRENT SENSING

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SIGNIFICANCE AND OBJECTIVES

Battery fuel gauges usually employ a shunt-based Current-Sensing System (CSS). State-of-the-art CSSs consume µWs of power to achieve the required performance. However, many IoT or wearable applications require power consumption in the sub-µW range. This project aims to develop nano-power CSSs suitable for battery fuel gauges.

TECHNICAL APPROACH

State-of-the-art CSSs employ Discrete-Time Delta-Sigma Modulators (DTΔΣMs) to digitize the voltage across an integrated shunt resistor. A logical way to reduce power would be to explore the use of Continuous-Time Delta-Sigma Modulators (CTΔΣMs) for this task, since they typically require up to 5x less power due to their relaxed settling requirements. From the point-of-view of accuracy, however, this will be quite challenging, since resistor mismatch may then become the limiting factor. Furthermore, switching transients and glitches may also degrade accuracy. Further reductions in power consumption can be achieved by the use of aggressive duty-cycling at the circuit level e.g. in reference voltage generation and bias circuits.

SUMMARY OF RESULTS

This report presents a first step towards nano-power CSSs. The proposed architecture (shown in single-ended form in Fig. 1) digitizes the voltage drop across an integrated shunt resistor with a 1st-order incremental Continuous-Time Delta-Sigma Modulator (CTΔΣM).

The choice of a 1st order modulator is motivated by the fact that it only requires a sinc[1] decimation filter. Such a filter has a uniform response, which means that short current pulses will be properly averaged by the CSS irrespective of when they occur.

Another key feature of the modulator is that its summing node is implemented by a Capacitively-Coupled Instrumentation Amplifier (CCIA) [H. Jiang, L-SSC '18]. This leads to improved gain accuracy (set by cap ratios), allows it to handle beyond-the-rail input common-Mode voltages, and relaxes the noise requirements of the RC integrator, thus reducing the power needed to drive it.

In order to reduce the required sampling frequency F_s, we propose to use an 8-tap FIR-DAC in the modulator feedback path. This behaves very much like a 3-bit DAC but, being inherently linear, does not require the use of data-weighted averaging, whose logic can be quite power hungry. A small drawback is the need for an extra compensation path to deal with the increased delay in the feedback path.

In the proposed CSS, the main source of gain error is the TCR of the integrated shunt. In previous work [L.Xu, ISSCC '18], we have shown that this can be adequately compensated by using a PTAT reference voltage. However, there will still be some residual error, since the TCR of an integrated shunt is not exactly PTAT and is somewhat non-linear. In this work, we propose to suppress this error, by implementing a piece-wise linear compensation scheme based on the ΔV_{BE} and V_{BE} voltages generated by a standard PTAT biasing circuit.

We plan to tapeout the proposed design in September. The target specifications are shown in Table 1.

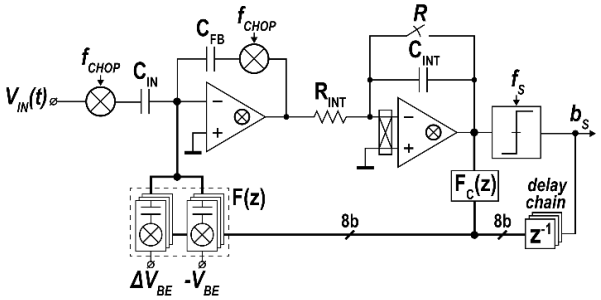


Figure 1. Simplified Single-Ended Circuit Architecture.

Table 1. Expected Comparison Table.

	[1]	[2]	This Proposal
V_{SUPPLY}	1.3 - 1.7 V	1.5 - 2V	**1.8 V**
I_{SUPPLY}	13 µA	10.9 µA	**1 µA**
Range	±5A	±4A	**±4A**
ICMR	0 - 0.75	0 - 25 V	**0 - 5 V**
Gain Error	±0.3%	±0.9%	**±0.5%**
Resolution	200 µA	150 µA	**350 µA**
BW/T_{CONV}	10 ms	2 ms	**62.5 ms**
Offset (I_{BAT})	4 µA	40 µA	**40 µA**
Temp. Range	-55°C to + 85°C	-40°C to + 85°C	**-40°C to + 85°C**
Shunt	10 mΩ (on chip)	10 mΩ (on chip)	**10 mΩ (on chip)**
Poly. Cal.	Yes	No	**No**
Tech.	130 nm	180 nm HV	**180 nm**

Keywords: current-sensing, continuous-time, shunt-based, capacitivaly-coupled, fir-dac

INDUSTRY INTERACTIONS

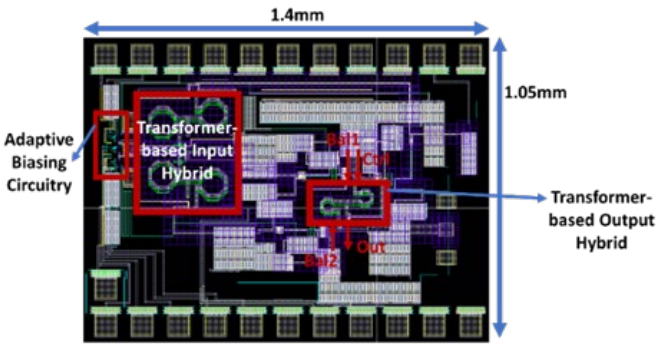
Texas Instruments, NXP

MAJOR PAPERS/PATENTS

[1] S.H. Shalmany et al, "A ± 36A integrated current-sensing system with a 0.3% gain error and a 400-µA offset from −55°C to 85°C," *J. Solid-State Circuits*, vol. 52, is. 4, pp. 1034–1043, Apr. 2017.

[2] L. Xu et al, "A ±4A High-Side Current Sensor with 0.9% Gain Error from −40°C to 85°C Using an Analog Temperature Compensation Technique," *J. Solid-State Circuits*, vol. 53, is. 12, pp. 3368 – 3376, Dec. 2018.

Safety, Security and Health Care Thrust



Category	Accomplishment
Safety, Security and Health Care (Systems)	Impedance mismatch resulting from variations of antenna impedance reduces the power delivered by mm-Wave power amplifiers. This project seeks to overcome this limitation and the concomitant VSWR events using a multi-port architecture which exploits mutual load-pulling to synthesize optimal impedances under VSWR events. Measurements from a fabricated prototype demonstrate broadband Doherty-like operation with P_{sat}>19dBm and PAE_{peak}>20% across 28GHz to 39GHz, as well as robust tolerance to VSWR events. (2712.013 Sengupta, Princeton)
Safety, Security and Health Care (Systems)	The limited energy storage capacity of IoT devices calls for solutions both for energy harvesting and for efficient uses of the energy soon after the harvest. This task seeks to use such energy for pre-computing various aspects required for performing cryptographic operations at IoT nodes. Pre-computation has been used to demonstrate inherent operations of internet security protocols, such as random number generation and as well as cryptographic key exchange, thereby maximizing energy utilization without sacrificing security. (2712.019 Schaumont, Virginia Tech)
Safety, Security and Health Care (Systems)	This task focuses on head pose estimation, which is paramount for gaze identification, in order to facilitate coordination between the vehicle and driver. Specifically, this project explores the use of deep learning-based algorithms in fusing multiple sensor modalities (i.e., various types of cameras) to estimate the driver's visual attention in real-world conditions. Results using data collected across 5 drivers confirm the efficacy of the proposed models. (2810.014, Busso & Al-Dahir, UT Dallas)

TASK 1836.155, DEVELOPMENT OF WIDE-BAND VIBRATION SENSORS

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SIAVASH.POURKAMALI@UTDALLAD.EDU

SIGNIFICANCE AND OBJECTIVES

The objective of this research is to design, implement, characterize and optimize a low power chip-scale vibration sensor that can operate over a wide range of frequency from DC to 10kHz with a resolution of 1mg or better.

TECHNICAL APPROACH

The aim of this research is for the vibration sensors to be realized in an existing CMOS technology by adding minimal modifications. The plan is to carve out part of the CMOS processed electronic chips as the mechanical components which would respond to vibrations in the form of bending. This would generate the tensile and compressive stresses on different locations on the chip. These stresses can then be detected by placing an integrated piezo resistors (e.g. n-well resistors) at the maximum stress locations. The proposed vibration sensor is comprised of an array of several piezoresistive cantilevers each covering a narrow frequency range (~15-100Hz) in the close vicinity of its resonance frequency (Figure 1).

SUMMARY OF RESULTS

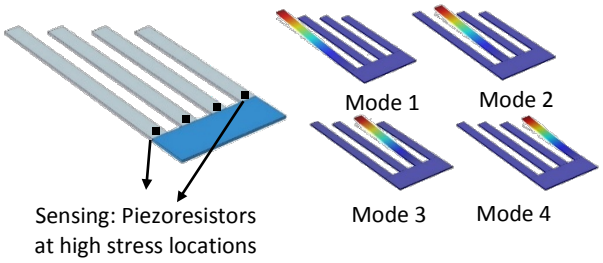

Figure 1. Eigen frequency and mode shapes for 4 integrated cantilevers, each covering a small portion of the targeted frequency spectrum.

Figure 2 shows a processed chip after performing a few metal and silicon etch steps (post-CMOS MEMS processing) to form the suspended cantilevers on the chip. The post-CMOS processing was minimal and straight forward as it did not include any lithography steps. To measure the effect of vibrations on the CMOS chips, a speaker/sub-woofer was used to create sinusoidal vibrations at different frequencies using a network analyzer. The vibration frequency was swept over the appropriate frequency range and the vibration response for the integrated cantilevers were recorded. Maximum sensitivity of ~5.3mV/V.g was achieved for the longest cantilever at its resonance frequency of ~7.2kHz as shown in Figure 2.

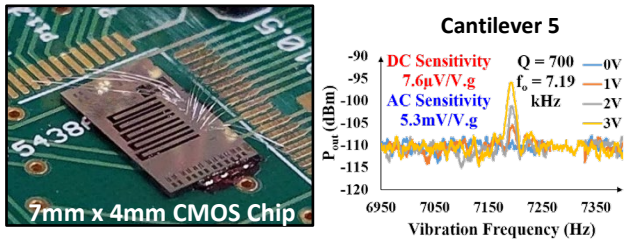

Figure 2. Image of the post-CMOS MEMS processed and wire-bonded integrated cantilevers along with the response to vibrations at different frequencies for the longest cantilever (Cantilever 5).

Figure 3 shows the measured frequency spectrum for the same cantilever. The noise floor is measured to be around -90dBm/Hz. Considering the 10dB noise figure of the interfacing amplifier, the actual noise floor of the device is estimated to be around -100dBm/Hz$^{1/2}$, i.e. 2.2uV/Hz$^{1/2}$. This translates to a sensor output noise level of 0.44mg/Hz$^{1/2}$/V.

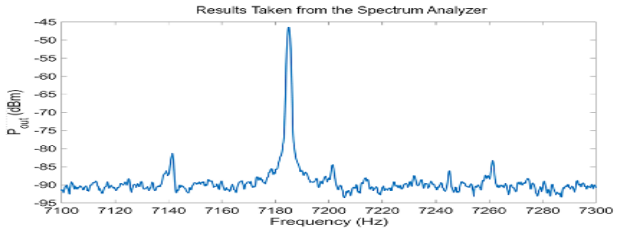

Figure 3. Measured frequency spectrum for the 7.1 kHz cantilever of Figure 2 showing noise floor of 2.2uV/Hz$^{1/2}$, i.e. 0.44mg/Hz$^{1/2}$/V.

The measured DC and AC sensitivities for the different cantilevers, show that it possible to detect vibrations with resolution below the 1mg target with bias voltages as low as 1V. A large number of integrated cantilevers can be integrated on a single chip covering a wide range of frequencies.

Keywords: high sensitivity, vibration sensor, low power, CMOS-MEMS integration, wide bandwidth

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Kumar V. et.al, "A Low power CMOS-MEMS Vibration Spectrum Analyzer", IFCS 2018.
[2] Abbasalipour A. et al., "Thermal Piezoresistive Resonant Mass Balance Implemented in a Standard CMOS Process," IFCS 2018.

TASK 2712.002, ON-LINE SELF-TESTING AND SELF-TUNING OF INTEGRATED VOLTAGE REGULATORS

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SIGNIFICANCE AND OBJECTIVES

The proposed research will develop low-complexity algorithms and low-overhead all-digital self-testing and self-tuning architecture for high-frequency IVRs. The research will focus on digitally controlled fully integrated inductive VRs (FIVR), digital low-dropout regulators (DLDO), and power delivery system with FIVR and multiple distributed DLDOs.

TECHNICAL APPROACH

The challenge for testing/tuning of IVRs is the presence of high frequency closed-loop control. The proposed approach is based on the principle that in a system with an IVR and digital core(s), the testing/tuning should focus on system performance rather than the IVR in isolation. We propose to characterize the output voltage variation that ultimately determines the performance of the digital load. We consider large signal perturbations (load and reference steps) to excite the transient noise in the IVR output, and tune the loop of IVR to minimize the noise. Finally, we explore co-tuning of IVR and processor.

SUMMARY OF RESULTS

Performance-based Tuning of Inductive IVR: We have demonstrated auto-tuning of the coefficients of the feedback loop of an inductive integrated voltage regulator (IVR) using an on-chip delay sensor. A 130-nm CMOS test-chip is designed containing a multi-sampled 125-MHz IVR with wire bond inductor, on-die capacitor, and all-digital PID controller powering a parallel Advanced Encryption Standard (AES) engine. The auto-tuning is performed using a Vernier delay line based on-chip delay sensor and an all-digital tuning engine. The measurement results demonstrate up to 5.2% improvement in the maximum operating frequency of the AES core using performance-based auto-tuning.

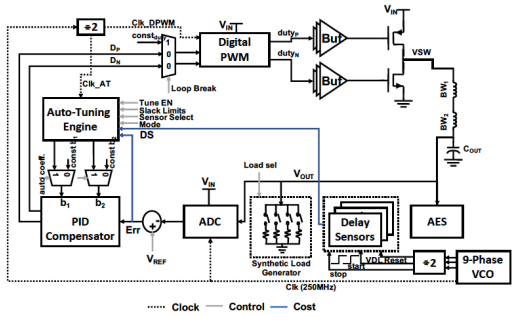

Figure 1. The architecture of performance-based tuning of inductive voltage regulators.

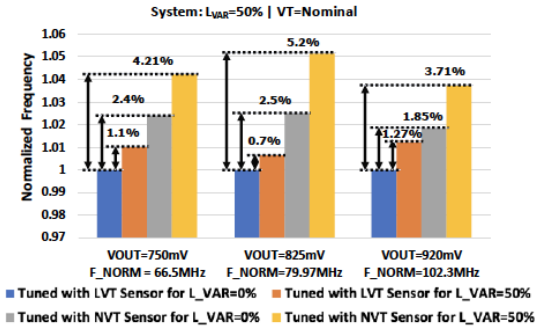

Figure 2. The measurement results showing impact of performance based tuning on performance of an AES.

Aging analysis of Inductive IVR and Digital LDO: Degradation of the transient performance and power conversion efficiency of on-chip VRs due to NBTI has been studied using 130-nm CMOS test-chips. The simulation and measurement show that NBTI induced shifts in the power stage resistance has much smaller effect on IVR compared to DLDO.

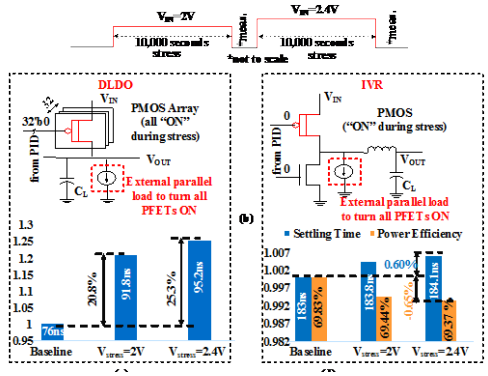

Figure 3: The measurement results showing impact of aging on inductive VR and digital LDO.

Keywords: Integrated voltage regulator, self-testing, and self-tuning.

INDUSTRY INTERACTIONS

Intel, NXP

MAJOR PAPERS/PATENTS

[1] V. Chekuri, A. Singh, N. Dasari and S. Mukhopadhyay, "On the Effect of NBTI Induced Aging of Power Stage on the Transient Performance of On-Chip Voltage Regulators," IRPS 2019.

[2] V. Chekuri, M. Kar, A. Singh, and S. Mukhopadhyay, "Auto-tuning of Integrated Inductive Voltage Regulator using On-chip Delay Sensor to Tolerate Process and Passive Variations," IEEE TVLSI 2019.

TASK 2712.003, MULTI-MODAL BIST DESIGN AND TEST METRICS EVALUATION FOR ANALOG/RF CIRCUITS

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SIGNIFICANCE AND OBJECTIVES

This project aims at (a) designing a library of BIST blocks that can be re-designed with minimal effort, (b) developing measurement techniques that do not rely on detailed knowledge of internal BIST parameters, and (c) developing a BIST advisor toolflow for system-level BIST insertion and evaluation.

TECHNICAL APPROACH

We have divided this problem into two parallel threads. First, we have developed a library of BIST components, including a gain measurement unit, a phase mismatch measurement unit, a PRBS injection unit, a cross correlator, and a programmable OPAMP-less ADC. Second, the BIST advisor toolflow takes into account multiple BIST options and evaluates them in terms of fault coverage and hardware cost to provide viable options for the designers.

SUMMARY OF RESULTS

We have built a library of BIST components, some of which have been taped out and tested. A BIST ADC needs to be versatile to meet multiple resolution/bandwidth requirements for self-test. We developed an OSR (Over Sampling Ratio) independent dynamic zoom ADC which can be used in wireless communication applications. Figure 1 shows the block diagram of the proposed dynamic-zoom passive ADC. It consists of a 5-b interpolating flash ADC and a simultaneously free-running passive second order single-bit ΔΣ modulator. At the positive clock edge, the interpolating ADC outputs a coarse conversion and yields a 31-b thermometer code. During the same clock phase, the digital logic prepares two sets of driving options for ΔΣ DACs. At the negative clock edge, the single-bit ΔΣ modulator operates and based on the modulator output, selects the driving bits for the DAC, which completes one cycle of operation. This architecture presents a viable option for BIST applications which may require wider bandwidth and lower OSR.

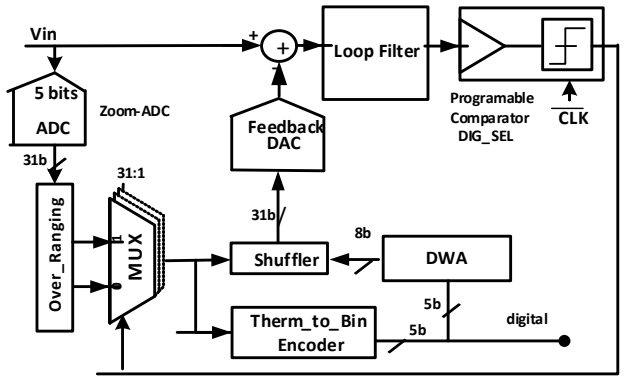

Figure 1. ADC architecture.

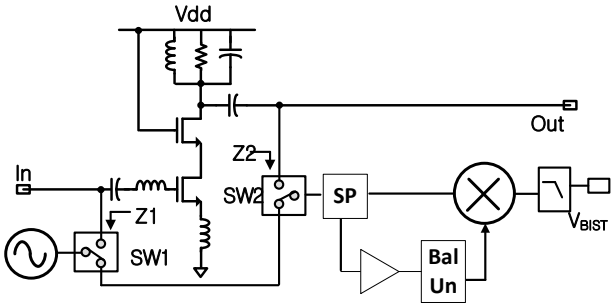

Figure 2. BIST for gain measurement.

The BIST system for gain measurement consists of a signal generator, a measurement circuit, and switches and traces to direct the signal flow. Figure 2 shows how a DUT is modified to include the BIST circuit. There are three configurations. The first configuration is the BIST loop, where the BIST signal source is connected to the measurement system. The second configuration is the BIST/DUT loop, where the test signal source drives the input of the DUT, and the output of the DUT drives the measurement system. The third configuration is the normal operation mode, where the DUT input and output are connected to functional input and output nodes and the BIST circuits are turned off to save power.

Keywords: Analog BIST, Fault Simulation

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

[1] Mehmet Ince, Ender Yilmaz, Wei Fuy, Joonsung Parky, Krishnaswamy Nagarajy, LeRoy Winemberg, and Sule Ozev, "Digital Built-in Self-Test for Phased Locked Loops to Enable Fault Detection" ETS 2019.

2712.013, RECONFIGURABLE MM-WAVE TX ARCHITECTURE AND ANTENNA INTERFACE WITH ACTIVE IMPEDANCE SYNTHESIS IN MULTI-PORT NODE-CONJUGATED COMBINER

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SIGNIFICANCE AND OBJECTIVES

This report summarizes the recent results in design of a mm-Wave Load Modulated Balanced Amplifier (LMBA) to allow for broadband and back-off efficient architectures addressing the 5G bands.

TECHNICAL APPROACH

We apply a generalized a mutual load pulling network synthesis approach to investigate architectures for broadband, linear and energy efficient PAs for 5G applications. In particular, we are investigating a RF-in and RF-out load modulated balanced PA in the 30-40 GHz range.

SUMMARY OF RESULTS

To overcome the bandwidth limitations of Doherty, we investigate load modulated balanced PAs (LMBA) with quadrature hybrid combining. The method builds on the hybrid-based design of a balanced amplifier where the control signal is injected at the isolated port instead of terminating that port by 50 Ω. The resultant achievable efficiency of the LMBA is shown in Fig.1(b).

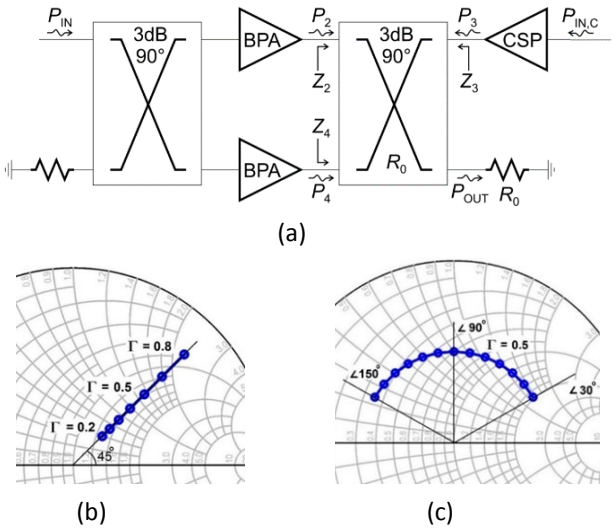

Figure 1. LMBA Concept at RF frequencies (Quaglia, et.al., TMTT2018) (a) Architecture (b) Load Modulation at constant phase of 45° (c) Load Modulation at constant amplitude of 0.5

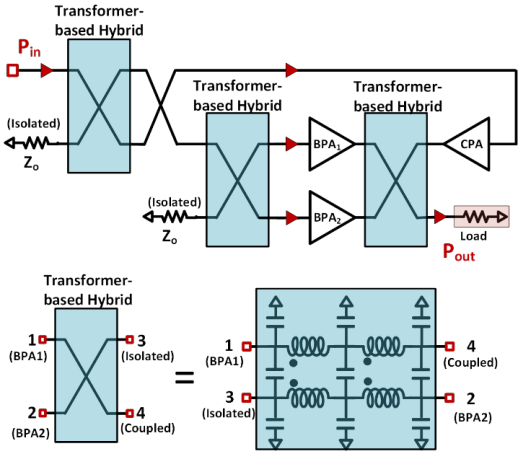

Figure 2. Schematic of LMBA. Transformer-based multi-order hybrid is employed for wideband match and phase generation

The high-level circuit schematic of the LMBA implemented in the work is shown in Fig.2. Here $BPA_1 = BPA_2 = 2 * CPA$. We used the transformer-based hybrid for wideband match, minimum loss and compact area as opposed to the quarter-wave transmission lines. Chip layout is shown in Fig. 3.

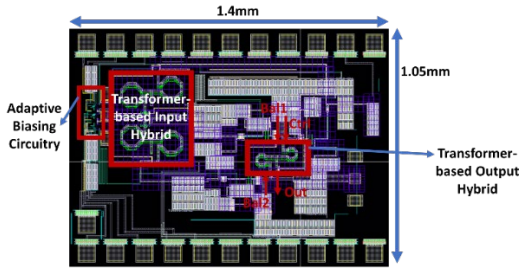

Figure 3. Layout of the mmWave LMBA across 28/37GHz

Keywords: mmWave, PA, broadband, load modulation, 5G

INDUSTRY INTERACTIONS

Texas Instruments, Intel, NXP

MAJOR PAPERS/PATENTS

[1] C.R.Chappidi and K.Sengupta, "A 26-42 GHz Broadband, Back-off efficient and VSWR Tolerant CMOS Power Amplifier Architecture for 5G Applications," *IEEE Symp. on VLSI, June 2019, Kyoto, Japan.*

TASK 2712.015, AREA-EFFICIENT ON-CHIP SYSTEM-LEVEL IEC ESD PROTECTION FOR HIGH SPEED INTERFACE ICS

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SIMON ANG, UNIVERSITY OF ARKANSAS

SIGNIFICANCE AND OBJECTIVES

Area-efficient, low-capacitance, on-chip system-level IEC ESD protection solutions for high-speed interface ICs will be designed, fabricated and characterized. Novel designs of IEC ESD structures will be provided for cost-effective system-level ESD protection of high-speed interface ICs.

TECHNICAL APPROACH

To reduce the total ESD device areas and parasitic capacitance, our approach is to utilize the inherent parasitic PNP structure in the high-side ESD diode as a parallel path to shunt the ESD discharge current. The key for this approach is to understand and adjust the ESD characteristics of substrate parasitic PNP structures.

SUMMARY OF RESULTS

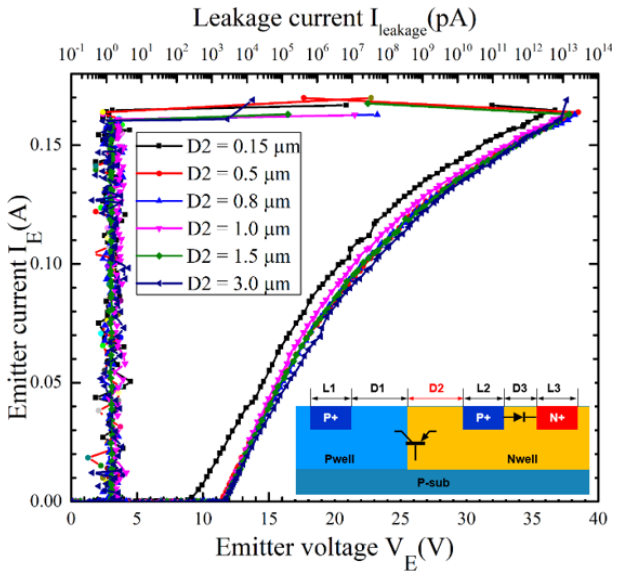

Figure 1. TLP characteristics of parasitic PNP structure in ESD diode. The insert shows the cross section of ESD diode.

The effects of geometry parameters (D1, D2, L1, L2, etc. in Fig. 1) on current gain, triggering voltage (V_{t1}) and on-resistance of the parasitic PNP inside the P+/N-well diode have been studied. Silvaco TCAD device simulation has been performed to understand the relationship between the geometry parameters and charaterisics of the parasitic PNP. The test structures fabricated using the UMC 65-nm CMOS and process B are characterized with a transmission line pulse (TLP) system and DC-IV measurements.

With the experimental results along with the TCAD simulations, it can be observed that the triggering voltage (V_{t1}) of parasitic PNP is greatly affected by D2 (i.e., the P+ diffusion to the P-well distance) (Fig. 1). V_E is the applied emitter voltage of PNP structure. The current gain of the parasitic PNP is extracted to physically explain the effects of D2 on V_{t1}. Additionally, the scalability of failure current (I_{t2}) has been studied in terms of the device width and the periphery of P+ inside of P-well. Good scalability of I_{t2} is observed from the TLP characteristics. Moreover, current is injected into the base of PNP during the TLP testing to study the effect of transient current injection through the power supply during ESD events.

In addition, the island-type ESD diode structures are designed with different geometry parameters to compare with finger-type diodes. The optimization on the metallization is designed to reduce the total capacitance of the ESD structures for high speed applications. Different routing methods with high-level metals are utilized on both island and finger-type ESD diodes. The primary ESD protection structures are also connected with various optimized ESD diodes in the process B to observe the influence of parasitic PNP on the I_{t2} of ESD structure.

Next step is to develop the ESD structure with the optimized diode such that all the ESD characteristics are within the appropriate ESD protection window. Additional ESD protection structures will be developed to verify the effectiveness of the whole ESD protection.

Keywords: ESD, PNP, Parasitic, IEC, TCAD

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Z. Chen, et al, “Area-efficient IEC ESD Protection for High Speed Integrated Circuits”, provisional patent filed
[2] Z. Chen, et al, “Study of Voltage Overshooting of Gate-Coupled Silicon Controlled Rectifier on HBM Protection”, 40th EOS/ESD Symposium, Reno, NV, 2018
[3] S. Madhusoodhanan, et al, “Analysis of Gate-Coupled SCR on HBM Protection Under Voltage Overshoot”, Journal of Electrostatics, under review
[4] P. Lai, et al, “Investigation of ESD Protection in SiC BCD Process”, 2019 WiPDA conference, accepted

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SIGNIFICANCE AND OBJECTIVES

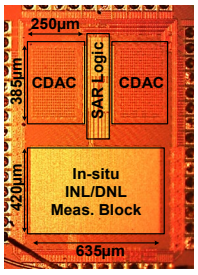
Short term instability effects caused by fast V_{th} stress and recovery become more critical in advanced technologies. This issue can be detrimental to the performance of ADCs even for a fresh chip. The objective of this work is to develop novel in-situ ADC characterization techniques and perform detailed reliability measurements.

TECHNICAL APPROACH

We designed a counter based measurement circuit for in-situ characterization of DNL and INL of a successive-approximate-register (SAR) ADC. An array of counters collects the histogram of the ADC output code for a triangular input voltage. Since the ADC operation and data transfer operation are separated in time, the DNL and INL results are immune to noise in the measurement setup. Using the proposed characterization method, we studied short-term bias temperature instability (BTI) effects in a SAR-ADC under different operating conditions.

SUMMARY OF RESULTS

We demonstrated a counter based measurement circuit for precise characterization of ADC DNL and INL (Figs. 1 and 2) in a 65-nm CMOS process. Using the proposed method, we studied short-term device instability issues in a 10-bit SAR-ADC (Figs 3 and 4). Results confirm that subtle DNL shifts as small as 0.05 LSB can be detected using the proposed method under different duty cycles, operating frequencies, and comparator types.



Process		65nm GP CMOS
Core / IO supply		1.2V / 2.5V
ADC resolution		10-bit
DNL (max)	vs Con. (w/o SRAM)	0.88 LSB (1.23 LSB improv.)
Read Out Data Volume	vs Con.	1/64 (for 32 samples/code)
Tr. count of on-chip measurement block		94,208 (Counters only)
DNL		+0.34 / -0.88 LSB @ 1MHz
INL		+1.67 / -1.41 LSB @ 1MHz
Total chip area		0.57mm^2

Figure 1. SAR-ADC die photo and chip feature summary.

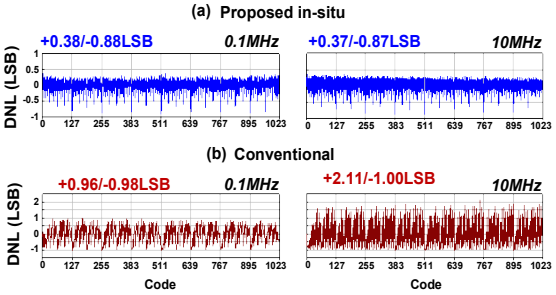
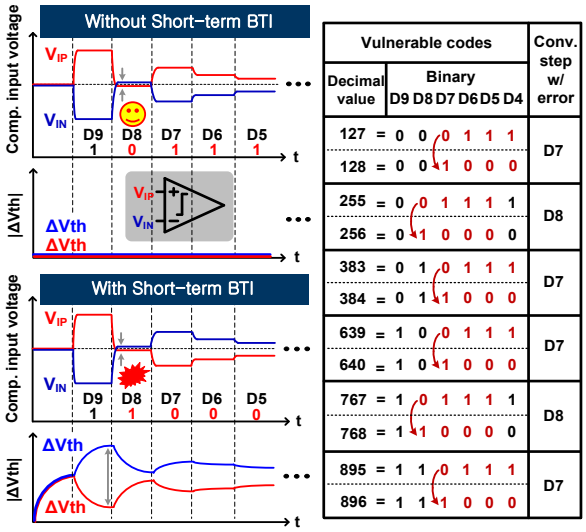


Figure 2. Proposed counter-based in-situ INL and DNL measurement circuit is immune to package or board level noise effects.



Vulnerable codes											Conv. step w/ error
Decimal value		Binary D9	D8	D7	D6	D5	D4				
127	=	0	0	0	1	1	1				D7
128	=	0	0	1	0	0	0				
255	=	0	0	1	1	1	1				D8
256	=	0	1	0	0	0	0				
383	=	0	1	0	1	1	1				D7
384	=	0	1	1	0	0	0				
639	=	1	0	0	1	1	1				D7
640	=	1	0	1	0	0	0				
767	=	1	0	1	1	1	1				D8
768	=	1	1	0	0	0	0				
895	=	1	1	0	1	1	1				D7
896	=	1	1	1	0	0	0				

Figure 3. Illustration of codes that are vulnerable to short term BTI effects in a 10 bit SAR-ADC. Codes ending with a pattern of 0111… can get misinterpreted as the neighboring code which ends with a pattern of 1000….

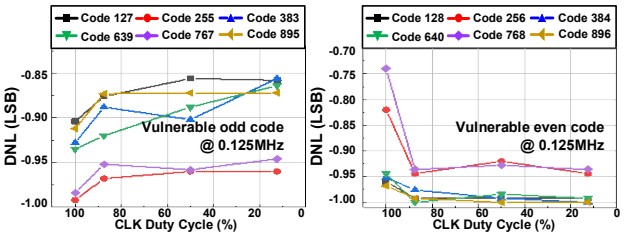


Figure 4. DNL measured under different duty cycles for the most vulnerable codes; (left) codes ending with 0111…; (right) codes ending with 1000….

Keywords: SAR-ADC, bias temperature instability, in-situ measurements, INL, DNL

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] G. Park et al., "A Counter based ADC Non-linearity Measurement Circuit and Its Application to Reliability Testing", CICC, April 2019, San Jose, California

[2] N. Pande et al., "Investigating the Aging Dynamics of Diode-connected MOS Devices using an Array-based Characterization Vehicle in a 65nm Process", IRPS, March 2019, Monterey, California

TASK 2712.018, TEST TECHNIQUES TO APPROACH SEVERAL DEFECT-PER-BILLION FOR POWER ICS

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SIGNIFICANCE AND OBJECTIVES

Existing LDO and Buck converter power IC test techniques examine and model chip performance through external terminals. This work designed, simulated and tested power IC subcircuits using additional bare-die test points to improve part failure rates. The goal is test yield enhancement by culling power ICs with outlier subcircuit performance.

TECHNICAL APPROACH

Task researchers demonstrated the use of internal IC test points to determine subcircuit performance inside of 65-nm CMOS LDOs and Buck Converters. Bare-die power IC probing will allow the measurement of DC, small-signal response and precise control of low and high temperature wafer measurements. Analyses, simulations and measurements of custom-designed LDO and buck converters will be performed in order to prove these new test concepts. A functional LDO IC was fabricated in 65-nm CMOS and used to characterize on-chip power IC control loop gain and phase response. A new 65-nm CMOS LDO test IC and a buck converter test IC have been submitted for fabrication.

SUMMARY OF RESULTS

This year, the researchers 1) Performed preliminary measurements of the LDO Test IC, 2) Designed a 65-nm CMOS buck Converter with enhanced testing and 3) Developed a new “servo loop” method of testing on-chip LDO control loop gain and phase. A 65-nm CMOS LDO Test IC was fabricated and packaged. The bench testing of the circuits provided the LDO load regulation and line regulation, and also great 65-nm process performance feedback for the design of a buck converter test IC. Preliminary bench test showed a functional 65-nm CMOS LDO with all the built-in test features working. The band gap reference output voltage was higher than simulation and the amplifiers required more bias voltage during measurement than in simulation. The 65-nm CMOS design kit PDK lacked analog output pads and the ones created at UF had a maximum output current of 40-50-mA. This limited the LDO output to 40-50-mA. Nevertheless, the LDO test is being used to demonstrate all the anticipated methodologies proposed in the project deliverables. A new methodology, an LDO on-chip control loop response "servo loop" test has been successfully created, simulated and measured with up to 90-dB gain with DC test. Implementation on load board for extensive AC and temperature testing is in progress. Test jigs, and software will be developed for thorough packaged testing on an ATE tester both at UF and at TI. An on chip programmable current sink was add to the LDO chip for enhanced testing controllability. Unfortunately, experiments showed the on-chip load is always on which limits the LDO pad output current.

The buck IC testing strategy is to use extra probe points for DC and analog test on the die before packaging. The researchers were guided to develop a buck converter test IC with an advanced ACM-based control loop design by the task liaisons. The researchers have designed and performed layout the buck converter characterization and subcircuit test IC in the UMC 65-nm CMOS process which was submitted for fabrication. The block diagram, schematics of example subcircuits and test features of the buck converter IC are shown in Figure 1.

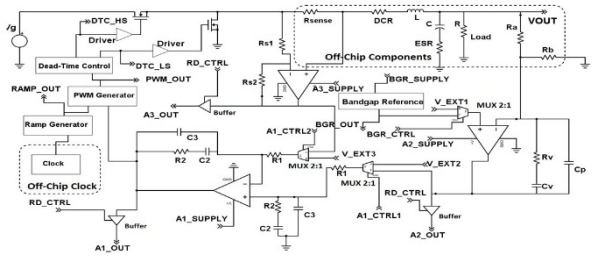

Figure 1. Buck converter test IC block diagram showing enhanced subsystem and power FET testability.

Keywords: Test, Analog, Power, LDO, Buck Converter

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] A. Tulsiram, W. Eisenstadt, Development of LDO Testing and Fault Detection for Ultra Low Defects, IEEE NATW’18, Essex, VT., May 8, 2018.

[2] A. Tulsiram, “Test Techniques to Approach Several Defect-Per-Billion,” SRC Techcon 2018, Austin, TX, Sept. 16-18.

TASK 2712.019, PRE-COMPUTED SECURITY PROTOCOLS FOR ENERGY HARVESTED IOT

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SIGNIFICANCE AND OBJECTIVES

An energy-harvesting IoT device has a limited energy-storage capacity. Cryptographic applications can use pre-computing techniques to instantly use the harvested energy. Pre-computed results are stored efficiently and securely in non-volatile memory. We demonstrate that precomputed cryptography improves the latency in Internet security protocols.

TECHNICAL APPROACH

The feasibility and efficiency of the proposed techniques will be evaluated through an end-to-end demonstrator with an energy-efficient micro-controller and with a wireless communications front-end. We develop techniques to spread out computations over time by reformulating cryptographic algorithms as capable of generating coupons, which are precomputed portions of the algorithm. We propose techniques for coupon generation and their secure storage in non-volatile, possibly off-chip memories. We also consider and optimize the impact of precomputed security protocols on the communication cost and the storage cost. We validate the proposed approach by constructing a prototype implementation on an energy-harvesting oriented microcontroller-based platform.

SUMMARY OF RESULTS

When a computing platform temporarily loses power, it stores its current state in a checkpoint, such that it can recover and continue execution at the point just before storing the checkpoint. A checkpoint also holds pre-computed results (or coupons) to support the execution of a single cryptographic algorithm over multiple power-loss events. We performed a detailed security analysis of storing checkpoints in non-volatile memory. Also, a checkpoint also holds pre-computed results. We identify three possible scenarios that can threaten the security of the checkpointing process: a checkpoint may be snooped (eavesdropped upon), a checkpoint may be spoofed (tampered), and a checkpoint may be replayed. Each of these attacks can lead to loss of information security on the IoT device, or loss of control.

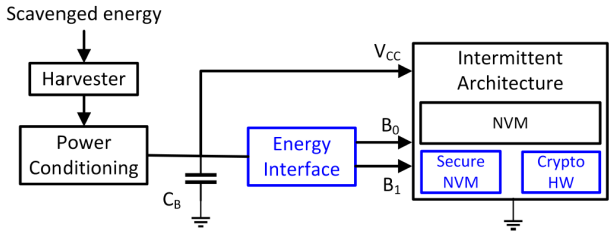

Figure 1. Architecture support for Secure Intermittent Computing builds on secure NVM, hardware crypto acceleration, and a two-bit harvester interface.

To protect checkpoints, we propose the Secure Intermittent Computing protocol (SICP) [1]. SICP encrypts checkpoints in standard NVM, possible off-chip (Figure 1). SICP requires a small secure (tamper-free) NVM protected against unauthorized access. SICP prevents snooping, spoofing, and replay of checkpoints. Also, SICP itself is resistant to power loss, and it ensures the proper ordering of checkpoints. SICP uses authenticated encryption (AEAD). A prototype implementation on Texas Instruments MSP430FR5994 requires 355 ms and 455 ms to store and restore a 2-kilobyte checkpoint securely respectively. The operation of SICP is driven through an energy interface (Figure 1), which drives pre-computing, check-point creation, and power control for the intermittent architecture [2]. We investigated the feasibility of supporting secure intermittent computing without the use of cryptography, and we summarized these requirements in SIA (Secure Intermittent Architecture) [3].

In the final phase of the project, we plan to demonstrate a secure communications link between an intermittent system and a non-intermittent system.

Keywords: Cryptography, energy-harvesting, NVM applications, intermittent computing, MSP430

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] A. Krishnan et al., “Secure Intermittent Protocol: Protecting State against Power Loss,” DATE 2019.

[2] A. Krishnan et al., “Hardware Support for Secure Intermittent Architectures,” ESSA 2019.

[3] D. Dinu et al., “SIA: Secure Intermittent Architecture for Off-the-Shelf Resource-constrained Microcontrollers,” HOST 2019.

TASK 2712.021, DISTRIBUTED SILICON CIRCUITS AND SENSORS IN 3D-PRINTED SYSTEMS FOR WEARABLE IOT SENSORS

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YIĞIT MENGÜÇ, OREGON STATE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

There is an emerging set of applications that require stretchable, compliant electronics – including wearable devices, instrumented fabrics, and soft robots with distributed sensors and computation. In this project, we are working to demonstrate a fundamentally new method for fabrication of stretchable, 3D-printed objects containing distributed sensors and silicon ICs.

TECHNICAL APPROACH

Developing stretchable electronics faces two primary challenges: integration of active semiconductor devices in elastic substrates, and providing stretchable and conductive interconnects. In this project, we combine 3D printing of liquid metal materials and silicone rubber with PCB fabrication techniques to build solid 3D objects with electronic components distributed throughout. Silicon integrated circuits, used for computation, sensing, and actuation, will be connected through liquid metal conductors confined to 3D microfluidic channels. Through additive, layer-by-layer construction, electronic devices can be inserted and connected throughout the 3D structure. We will also develop compact models for the interconnects, which will be used to design adaptable front-end circuits for stretchable interconnect interfaces.

SUMMARY OF RESULTS

In the previous project year (Year 2), we have demonstrated progress (Fig. 1) in printing stretchable circuits using discrete components, extended strain testing of liquid metal paste material, and started development of a compact modeling framework for stretchable interconnects. Specific outcomes included:

- Demonstrated printing of sensors and analog and digital interconnects using discrete active and passive components (published IEEE Sensors J. [1]).
- Extended testing of stretchable interconnects, demonstrating <5% change in resistance over 10,000 stretch cycles (accepted to FLEPS 2019 [2]).
- Compact modeling framework for Cadence-compatible modeling of stretchable metal interconnects (R,C) under static and dynamic strain conditions (accepted to FLEPS 2019 [3]).

In the next project period, we will focus on printing yield and resolution using liquid metal paster, in parallel with development of adaptive circuit interfaces for chip-to-chip communication over stretchable interconnects. Additional details are available in SRC project reports.

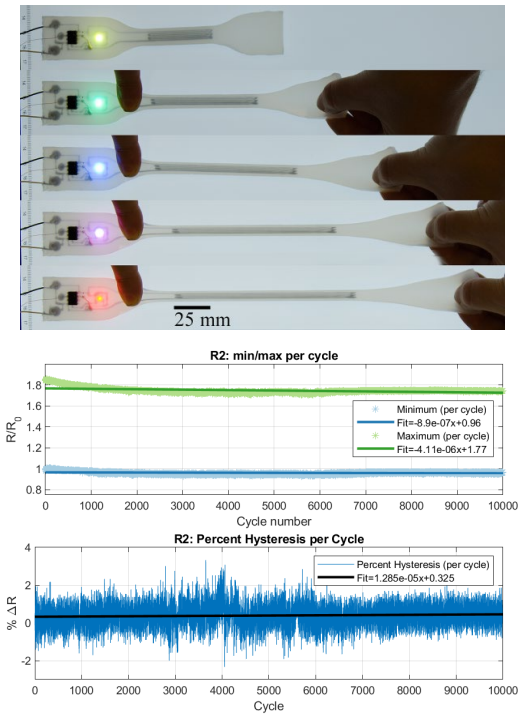

Figure 1. Printed stretchable strain sensor circuit (top) with active and passive components [1]; 10,000 cycle strain data (bottom) for stretchable liquid metal paste interconnect [4].

Keywords: Stretchable electronics; 3D printing; wearable devices; packaging; sensor interfaces

INDUSTRY INTERACTIONS

Texas Instruments, Intel, IBM

MAJOR PAPERS/PATENTS

[1] C. Votzke, U. Daalkhaijav, Y. Mengüç, and M.L. Johnston, "3D-printed liquid metal interconnects for stretchable electronics," *IEEE Sensors Journal*, 2019.

[2] C. Votzke, K. Clocker, Y. Mengüç, and M.L. Johnston, "Electrical characterization of stretchable printed liquid metal interconnects under repeated cyclic loading," Accepted to 2019 FLEPS, Glasgow, Scotland.

[3] K. Clocker, C. Votzke, Y. Mengüç, and M.L. Johnston, "Compact modeling of stretchable printed liquid metal electrical interconnects," Accepted to 2019 FLEPS, Glasgow, Scotland.

[4] C. Votzke, U. Daalkhaijav, Y. Mengüç, and M.L. Johnston, "Highly-stretchable biomechanical strain sensor using printed liquid metal paste," 2018 BioCAS, Cleveland, OH, Oct. 2018.

TASK 2712.022, INTRINSIC IDENTIFIERS FOR DATABASE-FREE REMOTE AUTHENTICATION OF IOT EDGE DEVICES

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AMIT RANJAN TRIVEDI, UNIVERSITY OF ILLINOIS AT CHICAGO

SIGNIFICANCE AND OBJECTIVES

Physically unclonable functions (PUFs) are widely used for authentication, however, require dedicated hardware and large signature database. We discuss intrinsic and database-free authentication scheme using back-end capacitors. We also introduce a current PUF based novel PCB authentication method to protect PCBs from counterfeiting/cloning attacks.

TECHNICAL APPROACH

We show that an Analog-to-Digital converter (ADC) can be modified for back-end capacitor based authentication in addition to its regular functionality. Metal-oxide-metal (MOM) capacitors are the preferred for ADC applications and mismtach characteristics of MOM capacitors depend significantly on the process parameters. On the other hand, through circuit-level simulation and also physical measurements we observe that the supply current eminently fluctuates depending on the overall in-circuit switching activities, which is utilized to authenticate PCBs.

SUMMARY OF RESULTS

Capacitive DAC is an integral part of SAR ADC architecture and is a source of large number of MOM capacitor samples. We have modified the ADC architecture (Figure 1) to provide individual access to MOM capacitors in capacitive DAC without affecting normal data conversion functionality. Additionally, we use C_{OF} capacitance for mismatch statistics based signature extraction. Authentication signature extraction is based on the fact that capacitor mismatch profile follows Gaussian statistics and we determine the fraction of capacitors at tail of the statistics. N_{AC} (C_{OF}) denotes the fraction of capacitors on the mismatch statistics at a given C_{OF}. Next, we determine $N_{AC,Avg}$ using N_{AC} (C_{OF}) from all the authentic ICs [Figure 2(a)]. This results in a distintive distance distribution as shown in Figure 2(b). It does not require database storage.

We have also developed a current-based IC and PCB authentication technique. The experimental setup is depicted in Figure 3. The experiments are run over 20 different PCBs for 4 different supply voltages and temperatures and for different LFSR lengths (16, 64, 256, and 1024 bits). The plots of percentage bit errors from every operating points are illustrated in Figure 4.

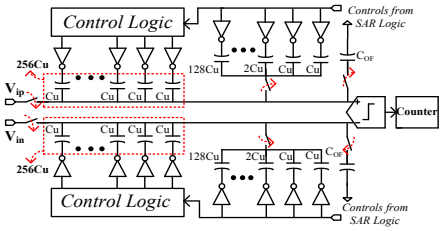
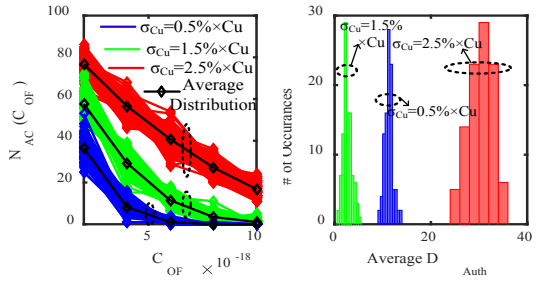


Figure 1. Modified SAR ADC architecture which allows MOM capacitor mismatch characteristics extraction.



(a) (b)

Figure 2. (a) Mismatch statistics based signature extraction, (b) Weighted distance based signature for authentication.

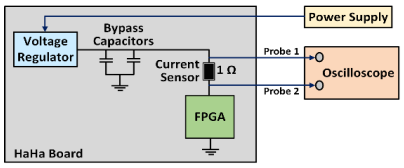
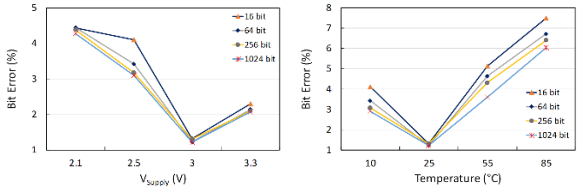


Figure 3. Block diagram of experimental setup for current based IC and PCB authentication.



(a) (b)

Figure 4. (a) V_{supply} variation result, (b) Temp variation results.

Keywords: SAR ADC, database-free authentication, PUF, Hamming distance, PCB Authentication

INDUSTRY INTERACTIONS

Texas Instruments, Intel, IBM

MAJOR PAPERS/PATENTS

[1] A. Shylendra et al., "An Intrinsic and Database-free Authentication by Exploiting Process Variation in Back-end Capacitors," in IEEE TVLSI, pp. 1253-1261, June 2019.

TASK 2712.026, FAULT CHARACTERIZATION AND DEGRADATION MONITORING OF SIC DEVICES

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SIGNIFICANCE AND OBJECTIVES

Harsh operating environment and high temperature swings introduce die and packaging related degradations in SiC MOSFETs. A comprehensive device health state monitoring approach is crucial for robust operation of SiC based systems. In this study, viable aging precursors for devices including Miller plateau voltage, conduction voltage drop and others are characterized over time.

TECHNICAL APPROACH

To accelerate the device aging process, DC power cycling is employed in this study. To fully characterize static device parameter change over its lifetime, an automated curve tracer B1506A from Keysight is used to take periodic parametric test of the samples. On the other hand, in order to investigate aging effect during turn-on and turn-off transients, double pulse tests are also conducted.

SUMMARY OF RESULTS

The operation principle of the DC power cycling test in this study is illustrated in Figure 1. The load current I_L is applied to heat up the DUT, and is removed during the cooling down period.

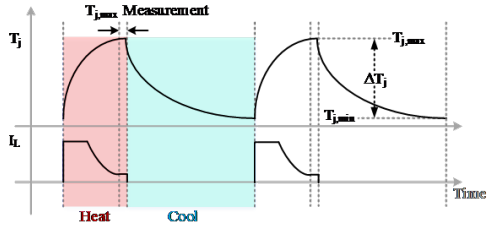

Figure 1. Accelerated aging operation principle.

Viable aging precursors are determined by means of both static and transient tests. The drain-source resistance change in saturation region versus aging cycle is included in Figure 2. As observed, when low V_{gs} is applied to the gate (+5V), the drain-source resistance increases by over 160Ω, providing an adequate margin for high resolution device aging assessment.

Furthermore, the body-diode forward voltage shift pattern is investigated. As shown in Figure 3, a positive increment of 100mV is observed over lifetime.

In Figure 4, device's Miller plateau voltage shows an increasing trend of 0.5V throughout degradation process.

Based on the thermal-triggered fatigue charateriazation, corresponding on-board aging detection approaches can be developed for SiC device state of health monitoring.

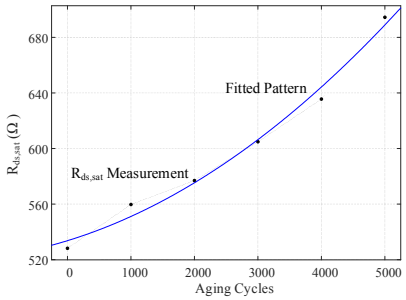

Figure 2. Device drain-source resistance variation at 5V V_{gs}.

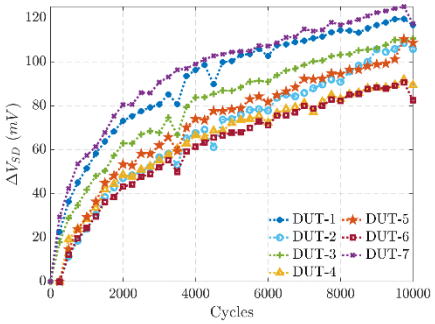

Figure 3. Body diode voltage drop variation over aging.

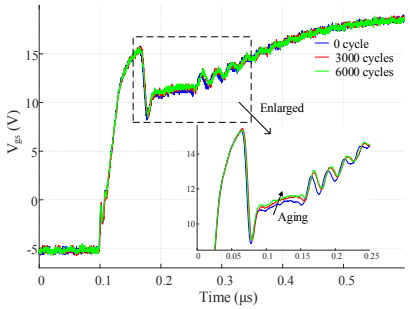

Figure 4. Thermally triggered V_{mp} increasing of SiC MOSFET.

Keywords: aging precursor, power cycling, SiC device

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] UTD/SRC 19032, "A complete condition monitoring method for SiC semiconductor devices"

[2] UTD/SRC 19045, "A Novel On-board SiC MOSFET Condition Monitoring Technique for Aging Detection"

[3] "Degradation Assessment and Precursor Identification for SiC MOSFETs under High Temp Cycling", IEEE Transactions on Industry Applications, 2019

TASK 2712.029, NOVEL SUPER-RESOLUTION AND MIMO TECHNIQUES FOR AUTOMOTIVE AND EMERGING RADAR APPLICATIONS

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SIGNIFICANCE AND OBJECTIVES

The primary challenge of a cost-effective and low-complexity near-field millimeter-wave (mmWave) imaging system is to achieve high-resolution with as few antenna elements as possible. In the past year, a novel near-field mmWave imaging solution that combines 2-D sparse MIMO arrays and SAR is proposed and experimentally verified.

TECHNICAL APPROACH

In this research, we propose a high-resolution mmWave imaging system combining two-dimensional (2-D) MIMO arrays with SAR, along with a novel Fourier based image reconstruction algorithm using sparsely sampled aperture data. The proposed algorithm is verified by both simulation and processing real data collected with our mmWave imager prototype utilizing commercially available 77-GHz radar sensors. The experimental results confirm that our complete solution presents a strong potential in high-resolution imaging with a significantly reduced number of antenna elements.

SUMMARY OF RESULTS

MIMO array configurations can be used to reduce the hardware cost, software complexity, and data acquisition time. Our imaging setup is based on a sparse MIMO array, which is scanned mechanically in a plane as shown in Fig. 1. The radar waveforms transmitted by the MIMO array sample the continuous x-y plane. The imaging system working at a specific frequency range can be used to image targets with unknown sizes and proximity. Thus, our goal in this research is to obtain the alias-free wavenumber spectrum within the visible region. Due to sparsity of MIMO array and subsampling of the scene, the visible region can contain multiple aliasing components. We analyzed the effect of sparse sampling experimentally.

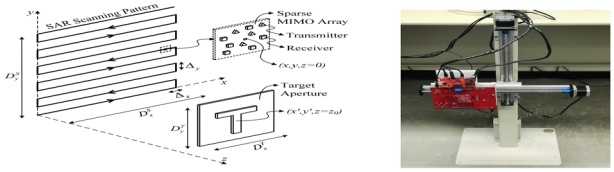

Figure 1. Left: The corner reflector is placed at 30cm away from the SAR scanner. Right: Two-axis motorized mmWave imager.

Figure 2. Left: Imaging scenario with multiple objects concealed in a cardboard box:. Right: Reconstructed image.

In this research, we propose a method for a sparse MIMO-SAR configuration to perfectly reconstruct alias-free images based on a multichannel combining technique using properly chosen complex gains.

A mmWave imaging prototype system has been built using commercial off-the-shelf (COTS) components to validate the proposed image reconstruction techniques and theoretical relationships established between image and wavenumber domains. The prototype system consists of a mmWave radar, a two-axis mechanical scanner, a motor controller, and a host personal computer (PC). The mmWave radar is a combination of three hardware modules from Texas Instruments: (1) IWR1443-Boost, (2) mmWave-Devpack, and (3) TSW1400 boards as shown in Fig. 1 (right).

The reconstruction quality of the imaging systems is described by the point spread function (PSF). We measure the PSF of our system using a corner reflector. Then, simulations are performed to examine the potential of proposed algorithms. Finally, the experimental image results of uncovered and concealed targets are provided in Fig. 2. The results show that the prototyped system is able to achieve high image quality with a significantly reduced number of antenna elements, thus making the system more affordable.

Keywords: mm-Wave radar, FMCW, SAR imaging, image reconstruction, X-Y scanner

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] M. E. Yanik and M. Torlak, "Near-Field MIMO-SAR Millimeter-Wave Imaging With Sparsely Sampled Aperture Data," *IEEE Access*, vol. 7, pp. 31801-31819, March 2019.

[2] M. E. Yanik and M. Torlak, "Near-Field 2-D SAR Imaging by Millimeter-Wave Radar for Concealed Item Detection," *IEEE Radio and Wireless Symposium*, pp. 1-4, Jan. 2019, Orlando, FL.

TASK 2712.030, PERFORMANCE OF CARBON DIOXIDE (CO_2) GAS SENSORS

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SIGNIFICANCE AND OBJECTIVES

In this work, we demonstrate the binding interaction of CO_2 within the RTIL using attenuated total refelectance-infrared (ATR-IR) spectroscopy. Furthermore, we demonstrate a portable CO_2 sensor for real-time monitoring of high concentrations of CO_2 upto 15,000 ppm using electrochemical technqiues.

TECHNICAL APPROACH

The docking of CO_2 between the RTIL moieties of EMIM[TF2N] was evaluated using ATR-IR spectroscopy. A custom closed environmental test system consisting of a gas mixer was used, wherein, the RTIL sensors were exposed to mixtures of N_2 and CO_2 with known concentrations. The sensor was first saturated with nitrogen to obatin the nitrogen ATR-FTTIR spectra . This was then followed by saturating the sensor with CO_2. CO_2 displaced the N_2 and demostrated C-O intercations with the cationic moetiy of the RTIL. A portable CO_2 sensor prototype was developed by integrating the CO_2 sensor with TI MSP430. Chronoamperometry was used to capture the CO_2 interaction and report in real-time.

SUMMARY OF RESULTS

The docking of CO_2 between the cationic and anionic moieties was validated using fourier transform infrared spectroscopy (FTIR). Baseline characteristic spectra of the RTIL by purging N_2 was captured. Fig. 1 demonstrates peaks at 2400 cm^{-1} and 3200 cm^{-1} when N_2 gas saturated the RTIL. Furthermore, the characteristic doublet peaks of CO_2 is observed when the RTIL was subjected to electrochemical voltage and was saturated with CO_2. The doublet peak at 2275 cm^{-1} indicates anti-symmetric stretching of CO_2 and the doublet peak at 3100 cm^{-1} indicates stretching of C-O bonds. These confirm the docking of the CO_2 between the moieties of RTIL through physisorption.

This docking of CO_2 in RTIL was leveraged to develop a RTIL based portable sensor. A calibration curve for the protable sensor prototype was developed by testing various concentrations in the range between 0 and 15,000ppm. Fig. 2(a) shows the calibration curve of the sensor prototype. The sensor prototype was then compared against a standard IR based CO_2 device (Vaisala, GMW90). The performance of prototype device was comparable to that of the standard. The portable CO_2 prototype demonstrated better repeatability at higher CO_2 concentrations as compared to the standard. Furthermore, the CO_2 sensor device has a wider dynamic range up to 15,000 ppm than the lab standard with a dynamic range of up to 8,000 ppm.

This work demonstrates the first electrochemical CO_2 prototype device with a wide dynamic range that can rapidly report CO_2 concentrations in real-time.

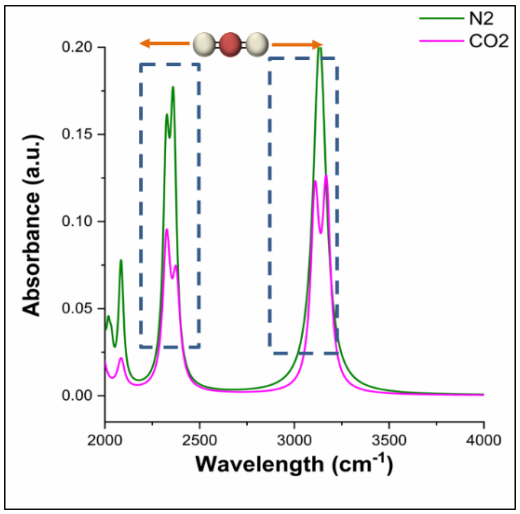

Figure 1. ATR-IR spectroscopy characterization binding of CO_2 between RTIL cationic and anionic moieties

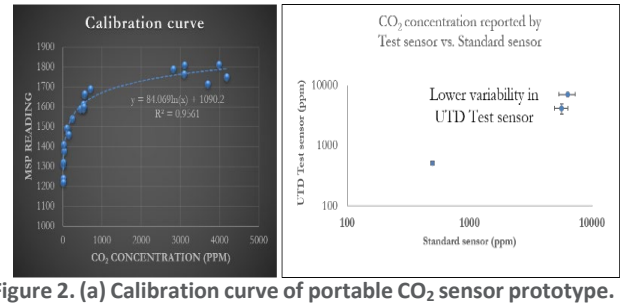

Figure 2. (a) Calibration curve of portable CO_2 sensor prototype. (b) Performance comapraison of CO_2 sensor prototype with standard CO_2 device

Keywords: Electrochemical Impedance spectroscopy, CO_2 sensing

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Bhide, A., Jagannath, B., Graef, E., Willis, R., & Prasad, S. (2018). *ECS Transactions*, *85*(13), 751-765.

TASK 2810.002, SECURITY-AWARE DYNAMIC POWER MANAGEMENT FOR SYSTEM-ON-CHIPS

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SIGNIFICANCE AND OBJECTIVES

The proposed research investigates the energy-security trade-offs associated with Dynamic Power Management (DPM). The proposed effort will develop methodology to characterize security implications of DPM in SoCs and design circuit/system techniques to co-optimize security and energy-efficiency of DPM.

TECHNICAL APPROACH

This effort will purse a cross-layer approach to understand the energy-security trade-offs in Dynamic Voltage Frequency Scaling (DVFS). First, we will design power domains that are secure against power-/EM- side-channel analysis by leveraging the distributed integrated voltage regulators. Next we will investigate energy-security trade-off at the chip level by focusing on the DVFS controller and algorithm. Finally we will explore an integrated approach considering secure power domains and secure DVFS controllers.

SUMMARY OF RESULTS

Power and Electromagnetic Side-Channel Security using Digital Low-droput Regulator: We have demonstrated improved power and electromagnetic (EM) side channel attack (SCA) resistance of a 128-bit AES engine via an on-die security-aware all-digital low-dropout regulator (DLDO). Power and EM side-channel measurements of the designed 130-nm CMOS test-chip demonstrates 3579× increase in the minimum number of traces required to disclose 80% bytes of the encryption key with only 10.4% performance loss of the AES engine.

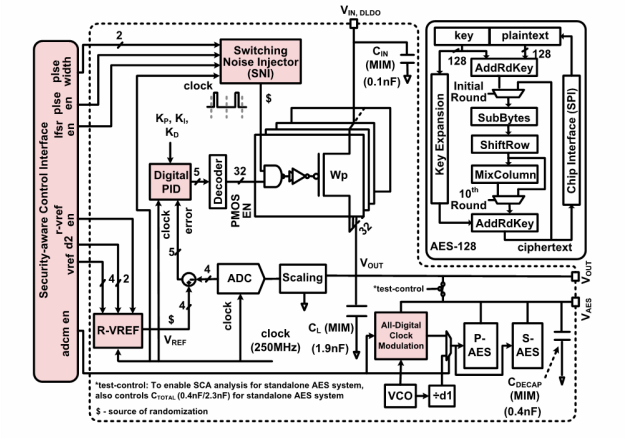

Figure 1. Architecture for digital LDO based power and electromagnetic emission side channel security.

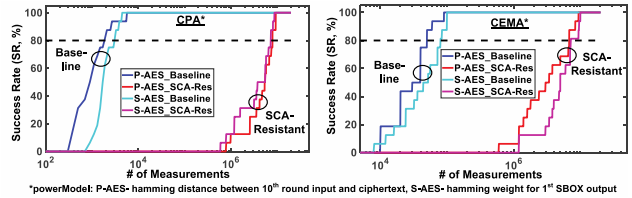

Figure 2. Power and EM-based SCA measurement results.

Fault-Attack Prevention using All-digital Clock Modulation: We have experimentally demonstrated that an on-chip integrated fast all-digital clock modulation (F-ADCM) circuit can be used as a countermeasure against supply glitch and temperature variations-based fault injection attacks (FIA). F-ADCM modulates clock edges in presence of DC/transient supply glitches and temperature variations to ensure correct operation of the underlying cryptographic circuit. With a testchip manufactured in a 130-nm CMOS technology, we first demonstrated an inexpensive methodology to conduct a fault attack on hardware implementation of a 128-bit advanced encryption standard (AES) engine using externally controlled supply glitches. Next, we showed that with F-ADCM circuit, it is no longer possible to inject supply/temperature glitch-based faults even after 10 million encryptions across varying operating conditions.

Keywords: secure, side-channel, dynamic power management, integrated voltage regulator, dynamic voltage frequency scaling

INDUSTRY INTERACTIONS

Intel, IBM

MAJOR PAPERS/PATENTS

[1] A. Singh, et. al., "Improved Power/EM Side Channel Attack Resistance of 128-bit AES Engines with Random Fast Voltage Dithering," *IEEE* JSSC*, Feb. 2019*

[2] N. Chawla, et. al., "Extracting side-channel leakage from round unrolled implementations of lightweight ciphers," IEEE HOST, 2019.

[3] A. Singh, et. al, "A 128b AES Engine with Higher Resistance to Power and Electromagnetic Side-Channel Attacks Enabled by a Security-Aware Integrated All-Digital Low-Dropout Regulator," *IEEE ISSCC* 2019.

[4] A. Singh, et. al, "Mitigating Power Supply Glitch based Fault Attacks with Fast All-Digital Clock Modulation Circuit," DATE, March 2019.

TASK 2810.005, CIRCUIT DESIGN FOR ESD AND SUPPLY NOISE MITIGATION

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SIGNIFICANCE AND OBJECTIVES

This project seeks to develop (1) IC-level power distribution networks that promote power integrity even in the presence of power-on ESD, and (2) biasing strategies for IO circuits that boost ESD resilience, thereby enabling high-speed IO circuits to meet both performance requirements and ESD target levels.

TECHNICAL APPROACH

This work identifies ESD-induced reliability hazards, including latch-up, and evaluates solutions. The investigations focus on integrated voltage regulators, rail clamp circuits, and high-speed IO. Promising solutions will be implemented in silicon. Additionally, the group continues to develop on-chip noise sensors that are most sensitive to ESD-induced noise. Experiments will be performed to establish whether ESD noise can be distinguished from other disturbances (e.g., supply brown out, simultaneous switching noise) or a bonafide reset signal. Such sensors can aid in mitigation of ESD-induced soft failures.

SUMMARY OF RESULTS

In simulation and analysis, we have demonstrated that ESD protection circuits intended for system-level protection (i.e., power-on ESD) can reduce the amplitude of simultaneous switching noise by several hundred millivolts. A test chip was designed to validate the analysis and is currently being fabricated. The on-chip supply noise and ESD resilience of the IC will be measured.

System-level ESD can reach the IO pins of an IC, especially if the IC is linked to an external connector. The ESD current induces noise on the IO supply and that noise propagates to the other on-chip supplies via the PDN (power distribution network). Measurement results on two test chips showed that, in some cases, the use of an integrated voltage regulator will mitigate the noise on the non-IO supplies. We have carried out a detailed analysis of those results.

Keywords: ESD, latch-up, integrated voltage regulator, simultaneous switching noise, rail clamp

INDUSTRY INTERACTIONS

Texas Instruments, NXP, Intel

MAJOR PAPERS/PATENTS

[1] Y. Xiu, N. Thomson and E. Rosenbaum, “Measurement and simulation of on-chip supply noise induced by system-level ESD,” *IEEE Transactions on Device and Materials Reliability*, vol. 19, no. 1, pp. 211-220, 2019.

TASK 2810.014, DEEP LEARNING SOLUTIONS FOR ADAS: FROM ALGORITHMS TO REAL-WORLD DRIVING EVALUATIONS

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NAOFAL AL-DHAHIR, THE UNIVERSITY OF TEXAS AT DALLAS

SIGNIFICANCE AND OBJECTIVES

Investigate deep-learning-based algorithms and evaluate their performance using fusion of sensing technologies (regular cameras, infrared imagers, RADAR) to estimate the driver's visual attention in real-world driving conditions. The project explores novel probabilistic models of visual attention, creating shared representation across multiple sensing technologies.

TECHNICAL APPROACH

We analyze alternative sensing technologies suitable for head pose estimation for in-vehicle applications, creating novel visual attention models (gaze). We perform real-world driving tests to evaluate alternative sensors that are appropriate for head pose estimation, benchmarking the results with the Fi-Cap device. We develop novel probabilistic models of the visual attention of the drivers describing confidence regions of the gaze given the position and orientations of the driver's head using deep learning. We propose multimodal deep learning frameworks to fuse sensor data using shared layer representation between modalities, creating robust and accurate solutions regardless of the environment.

SUMMARY OF RESULTS

The effort this year focussed on visual attention maps with convolutional neural networks (CNNs) using (1) head pose information, and (2) eye appearance models. We also made progress on data collection.

1) We have created a probabilistic relationship between head pose and gaze using deep learning (Fig. 1). In our formulation, the continuous gaze angles are converted into intervals and the grid of the quantized angles is treated as an image for dense prediction. We rely on CNNs with upsampling to map the six degrees of freedom of the orientation and position of the head into gaze angles. The proposed model obtains very promising results. The architecture offers an appealing and general solution to convert regression problems into dense classification problems.

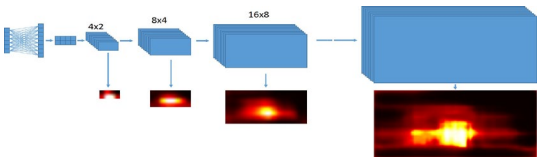

Figure 1. An image is generated after each upsampling. The output at each stage is optimized through back propagation.

2) We evaluated an alternative approach to estimate visual attention using appearance based models for gaze estimation. We proposed a novel method to predict the gaze using downsampling and upsampling of CNNs. A key novelty of the proposed model is that it produces a probabilistic map describing the gaze distribution as opposed to predicting a single gaze direction. We convert the regression problem into a classification problem, predicting the probability at the output instead of a single direction. The framework relies in a sequence of downsampling followed by upsampling to obtain the probabilistic gaze map (Fig. 2). We observe that our proposed approach works better than a regression model in terms of prediction accuracy, without any calibration or adaptation to the target user.

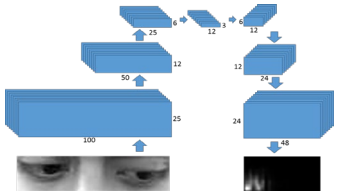

Figure 2. Block diagram of our framework, which relies on max-pooling layers followed by upsampling CNN layers.

3) Data collection: We finalized the protocol for data collection using multiple sensors, which was approved by the *internal review board* (IRB). We collected 5 drivers.

Accomplishments for the following year:

1) Data collect: we aim to collect 80-100 drivers

2) We will explore fusing approaches for visual attention estimation using depth and regular cameras

3) We will explore fusing visual attention models created with head pose information and eye appearance

Keywords: ADAS, head pose estimation, deep learning, visual attention, multimodal sensing

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] S. Jha and C. Busso, "Probabilistic estimation of the gaze region of the driver using dense classification," in IEEE ITSC 2018, Maui, HI, USA, November 2018.

[2] S. Jha and C. Busso, "Estimation of gaze region using two dimensional probabilistic maps constructed using convolutional neural networks," in IEEE ICASSP 2019, Brighton, UK, May 2019.

TASK 2810.016, CONDITION MONITORING OF INDUSTRIAL/ AUTOMOTIVE DRIVE COMPONENTS THROUGH LEAKAGE FLUX

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SIGNIFICANCE AND OBJECTIVES

Condition monitoring of electrical motors are performed by using various parameters. In this research, the usage of current and stray magnetic field around motors for identifying fault signature is studied for bearing fault and inter-turn short circuit. These two are most common fault types in electric motors.

TECHNICAL APPROACH

Electromechanical energy conversion in electrical motors takes place via magnetic field. Any fault occurred in a motor is more likely to have fault signatures in its air gap magnetic fields. Since it is not possible to obtain the magnetic field variation in airgap of motors, the stray magnetic fields around motors that reflects the variation in airgap magnetic fields are promising parameters for diagnostic of motor faults.

SUMMARY OF RESULTS

A bearing fault was artificially created in a permanent magnet synchronous motor (PMSM) and the measurements of stray magnetic fields are shown in Fig.1 which have strong and multiple signatures. These measurements are more effective than stator current analysis for PMSM.

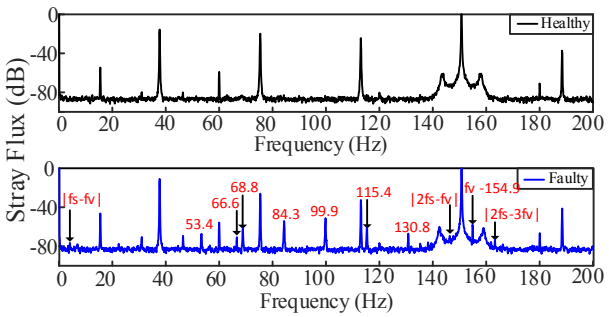
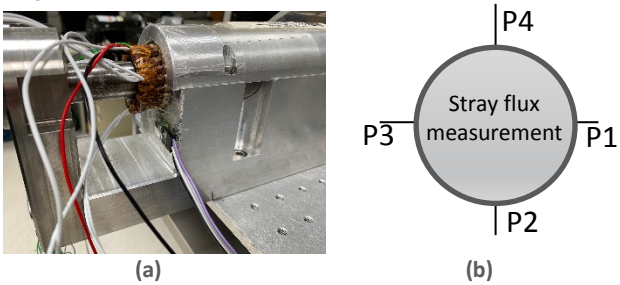


Figure 1. Bearing fault signatures in stray magnetic field of PMSM.



(a) (b)

Figure 2. (a) PMSM motor with fluxgate EVM. (b) Flux measurement positions.

An inter-turn circuit fault is created in a PMSM with a fault provision for 1 turn, 2 turn and 5 turn short circuit. The stray flux around the end winding region are monitored with a help of fluxgate sensor. The fluxgate sensor is placed around the end winding region at different positions to identify the location of fault as shown in Fig. 2(b). Fig. 3 shows the variation of fundamental component of stray magnetic field density when motor has 5 turns shorted compared to the healthy stator winding at different operating speeds under the no load condition. It can be clearly seen that the stray magnetic field at the fault location increases significantly with speed due to the increase of fault current.

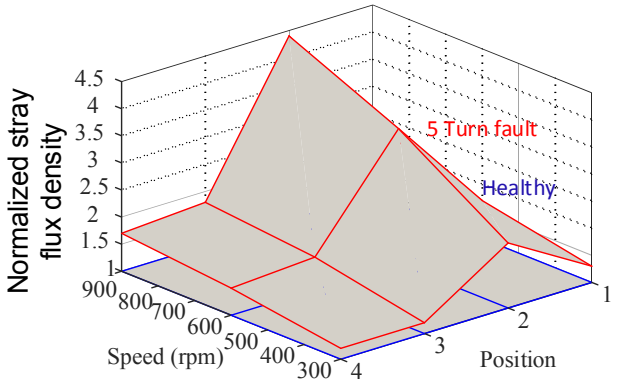


Figure 3. Stray flux density at different positions.

Since there is significantly lower current flowing in motors under the no load condition the stray fields are dominated by the fault current and they are a reliable fault signature.

Keywords: stray magnetic flux, PMSM, bearing fault, inter-turn short circuit fault

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] "A Comprehensive Analysis of Short-Circuit Current Behavior in PMSM Interturn Short-Circuit Faults," IEEE Transactions on Power Electronics, 2018.

[2] "Advanced Severity Monitoring of Inter Turn Short Circuit Faults in PMSMs," IEEE Transactions on Transportation Electrification, 2019

[3] "A Wavelet-Based Fault Diagnosis Approach for Permanent Magnet Synchronous Motors", IEEE Transactions on Energy Conversion, 2018

TASK 2810.017, RELIABILITY STUDY OF E-MODE GAN HEMT DEVICES

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HISHASHI SHICHIJO, THE UNIVERSITY OF TEXAS AT DALLAS

SIGNIFICANCE AND OBJECTIVES

AlGaN/GaN High Electron Mobility Transistors (HEMTs) have emerged as the most promising candidates for high-voltage power switching applications. This project is to investigate the gate TDDB of commercial p-GaN gate E-mode HEMTs by high resolution TEM/STEM and *in-situ* TEM coupled with the electrical characterization over bias voltage and temperature.

TECHNICAL APPROACH

The recently discovered time dependent dielectric breakdown (TDDB) of E-mode GaN HEMTs with a forward biased gate is being studied using commercially available devices. The location and nature of the breakdown percolation paths will be determined by high resolution transmission electron microscopy/scanning transmission electron microscopy (HR TEM/STEM) and will be correlated with the electrical TDDB data. In addition, in-situ TEM/STEM will be conducted to understand the electrical break down mechanism in detail.

SUMMARY OF RESULTS

In this reporting period, a hysteresis in I_G-V_G characteristics was discovered by sweeping the gate voltage from 0 V up to 7.5V and then sweeping it back down. Most of the EPC2016 devices showed some degree of hysteresis. Figure 1 shows an example of the observed hysteresis. It is noted that the device is not damaged during the sweep as the gate current below the hysteresis during up and down sweep stays unchanged. We believe the hysteresis is due to the floating potential and impact ionization in the p-GaN layer, but further studies are needed to confirm the mechanism. This hysteresis also shows up as an occasional jump in the gate current during the TDDB stress test as shown in Figure 2.

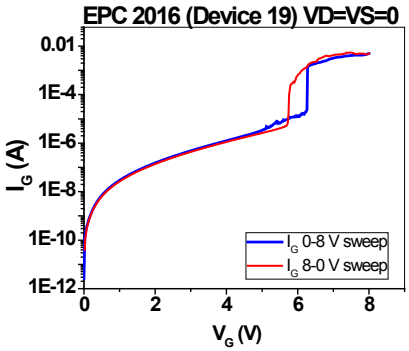

Figure 1. Gate current vs. gate voltage characteristics of EPC2016 eGaN HEMT device.

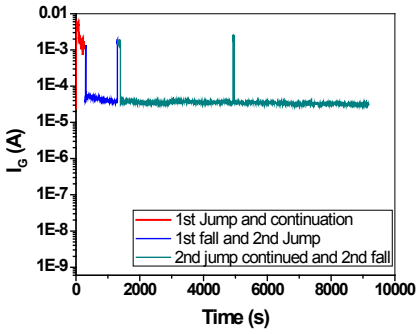

Figure 2. I_G versus time during the TDDB stress test of an EPC2016 eGaN HEMT.

Some devices were subjected to TDDB testing at V_G=7.5V. Figure 3 is a Weibull plot of the six devices tested. T63% lifetime is $9.9x10^4$ seconds. We are investigating the reason for the early fails of the 3 devices.

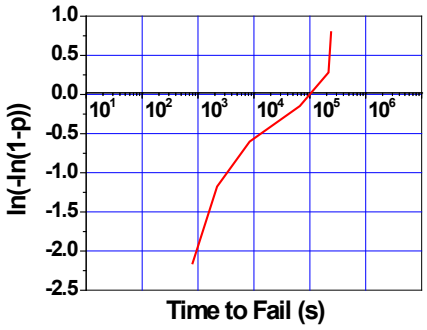

Figure 3. Weibull plot of six EPC2016 devices tested at V_G=7.5V.

More in-depth studies of device behaviors as stressed with various gate voltage are in progress. Detailed microstructural analysis for failed devices by high-resolution TEM/STEM is in progress. Also, photo emission studies on the EPC GaN HEMT devices under operation are being pursued.

Keywords: E-mode GaN HEMT device, reliability, failure mechanism

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

TASK 2810.021, A COLLABORATIVE MACHINE LEARNING APPROACH TO FAST AND HIGH-FIDELITY DESIGN PREDICTION

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YIRAN CHEN, DUKE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

The objective of this work is to predict pre-routing timing performance of a circuit with accuracy close to post-routing signoff analysis but with substantially less runtime. Such prediction will allow designers and circuit optimization tools to quickly and reliably evaluate early design solutions, and thereby accelerate overall design convergence.

TECHNICAL APPROACH

The pre-routing timing prediction is a machine learning-based approach. Machine learning models for net delay slew are constructed and trained. Overall circuit timing analysis is obtained by circuit traversal using the machine learning models in place of conventional lookup tables. The contributions include feature design for the models and evaluation of different machine learning engines.

SUMMARY OF RESULTS

Net-based delay and slew models share the same features, which are elaborated as follows.

• Driver and sink capacitance: Driver output capacitance is generally proportional to its driving strength. Total sink capacitance presents load to the driver.

• Distance between driver and the target sink: Our model predicts delay and slew of one sink at a time, and this sink is called target sink. The horizontal and vertical distances from the driver of the target sink is generally proportional to the corresponding wire delay.

• Max driver input slew: Here, slew rate is defined to be the signal transition time. As different types of logic gates may have different number of input pins, we use the maximum slew among all input pins of net driver as a feature. This is to accommodate that a machine learning model normally requires a fixed input size.

• Context sink locations: When a model is applied to estimate the delay/slew of the target sink of a net, the other sinks are called context sinks. We capture the characteristics of context sink locations with statistical signatures. One is the median location of all context sinks, which tells roughly how far the context sinks are from the driver. The other is the standard deviations of context sink locations in x-y coordinates.

Linear regression, neural network and random forest methods are evaluated and the random forest shows the best result. The error distribution from the random forest method is compared with a commercial tool in Figure 1.

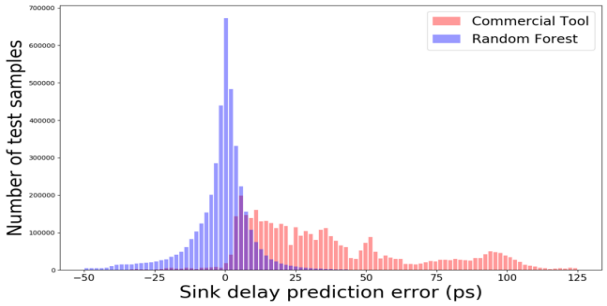

Figure 1. Error distribution of sink delay prediction.

Table 1 compares the number of critical paths k, total negative slack (TNS) in ns, and Receiver Operating Characteristic (ROC), with 1 as the best value. The last row shows the average among the 8 ITC 99 circuits. Our model is 30X faster than PrimeTime but 3X slower than the commercial tool.

Table 1. Timing prediction comparison.

PrimeTime		Commercial Tool			Random Forest		
k	TNS	k	TNS	ROC	k	TNS	ROC
4	-0.14	28	-5.33	0.29	15	-1.37	0.74
24	-0.90	114	-22.4	0.72	41	-5.51	0.94
4	-0.04	42	-5.78	0.37	26	-1.20	0.75
39	-9.05	150	-144	0.71	78	-40.4	0.90
49	-7.73	759	-368	0.80	57	-10.1	0.89
116	-48.5	330	-412	0.68	243	-152	0.90
53	-17.5	343	-299	0.69	184	-85.7	0.94
73	-22.2	459	-383	0.63	148	-68.2	0.96
45	**-13.3**	**278**	**-205**	**0.61**	**99**	**-45.5**	**0.88**

In next year, we will focus on improving timing prediction and routability prediction for digital and analog circuits.

Keywords: timing analysis, machine learning, design prediction, delay/slew model, random forest

INDUSTRY INTERACTIONS

IBM, ARM, NXP, Mentor, A Seimens Business

MAJOR PAPERS/PATENTS

[1] E. C. Barboza, N. Shukla, Y. Chen and J. Hu, “Machine Learning-Based Pre-Routing Timing Prediction with Reduced Pessimism,” Design Automation Conference, 2019, Las Vegas, NV.

TASK 2810.022, A COLLABORATIVE MACHINE LEARNING APPROACH TO FAST AND HIGH-FIDELITY DESIGN PREDICTION

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JIANG HU, TEXAS A&M UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

The objective of this work is to predict pre-routing timing performance of a circuit with accuracy close to post-routing signoff analysis but with substantially less runtime. Such prediction will allow designers and circuit optimization tools to quickly and reliably evaluate early design solutions, and thereby accelerate overall design convergence.

TECHNICAL APPROACH

The pre-routing timing prediction is a machine learning-based approach. Machine learning models for net delay slew are constructed and trained. Overall circuit timing analysis is obtained by circuit traversal using the machine learning models in place of conventional lookup tables. The contributions include feature design for the models and evaluation of different machine learning engines.

SUMMARY OF RESULTS

Net-based delay and slew models share the same features, which are elaborated as follows.

• Driver and sink capacitance: Driver output capacitance is generally proportional to its driving strength. Total sink capacitance presents load to the driver.

• Distance between driver and the target sink: Our model predicts delay and slew of one sink at a time, and this sink is called target sink. The horizontal and vertical distances from the driver of the target sink is generally proportional to the corresponding wire delay.

• Max driver input slew: Here, slew rate is defined to be the signal transition time. As different types of logic gates may have different number of input pins, we use the maximum slew among all input pins of net driver as a feature. This is to accommodate that a machine learning model normally requires a fixed input size.

• Context sink locations: When a model is applied to estimate the delay/slew of the target sink of a net, the other sinks are called context sinks. We capture the characteristics of context sink locations with statistical signatures. One is the median location of all context sinks, which tells roughly how far the context sinks are from the driver. The other is the standard deviations of context sink locations in x-y coordinates.

Linear regression, neural network and random forest methods are evaluated and the random forest shows the best result. The error distribution from the random forest method is compared with a commercial tool in Figure 1.

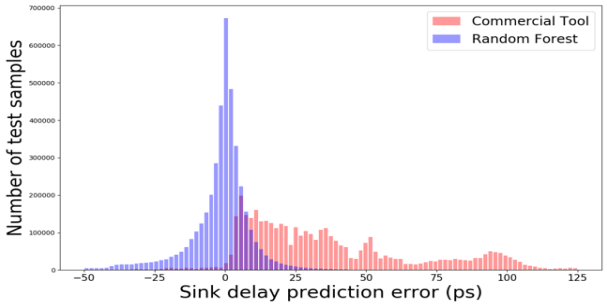

Figure 1. Error distribution of sink delay prediction.

Table 1 compares the number of critical paths k, total negative slack (TNS) in ns, and Receiver Operating Characteristic (ROC), with 1 as the best value. The last row shows the average among the 8 ITC 99 circuits. Our model is 30X faster than PrimeTime but 3X slower than the commercial tool.

Table 1. Timing prediction comparison.

PrimeTime		Commercial Tool			Random Forest		
k	TNS	k	TNS	ROC	k	TNS	ROC
4	-0.14	28	-5.33	0.29	15	-1.37	0.74
24	-0.90	114	-22.4	0.72	41	-5.51	0.94
4	-0.04	42	-5.78	0.37	26	-1.20	0.75
39	-9.05	150	-144	0.71	78	-40.4	0.90
49	-7.73	759	-368	0.80	57	-10.1	0.89
116	-48.5	330	-412	0.68	243	-152	0.90
53	-17.5	343	-299	0.69	184	-85.7	0.94
73	-22.2	459	-383	0.63	148	-68.2	0.96
45	**-13.3**	**278**	**-205**	**0.61**	**99**	**-45.5**	**0.88**

In next year, we will focus on improving timing prediction and routability prediction for digital and analog circuits.

Keywords: timing analysis, machine learning, design prediction, delay/slew model, random forest

INDUSTRY INTERACTIONS

IBM, ARM, NXP, Mentor, A Seimens Business

MAJOR PAPERS/PATENTS

[1] E. C. Barboza, N. Shukla, Y. Chen and J. Hu, “Machine Learning-Based Pre-Routing Timing Prediction with Reduced Pessimism,” Design Automation Conference, 2019, Las Vegas, NV.

TASK 2810.023, MACHINE LEARNING DRIVEN AUTOMATIC MIXED-SIGNAL DESIGN VERIFICATION-VALIDATION FOR AUTOMOTIVE APPLICATIONS

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SIGNIFICANCE AND OBJECTIVES

To facilitate rapid turnaround silicon design, the goal is to create accurate behavioral models of transistor netlists of mixed-signal designs to facilitate fast system simulation, to debug multiple design bugs with fine granularity and to perform diagnosis of design bugs down to the physical layout level.

TECHNICAL APPROACH

The technical approach rests on: (a) machine learning assisted algorithms for automatic generation of behavioral models from low level design abstractions (silicon-physical layout-transistor level netlist) that are extremely accurate in modeling minor differences between observed and expected circuit behavior, (b) accurate *modeling of the effects of manufacturing process variations on the performance specifications* and yield of mixed-signal ICs, (c) learning driven - hypothesis based *algorithms for detecting, modeling and diagnosing multiple design discrepancies* (bugs) in submodules of a design, both pre-silicon as well as post-silicon and (d) algorithms for *diagnosing design bugs down to specific areas of a layout.*

SUMMARY OF RESULTS

For multiple design bug diagnosis, consider the reference model description shown in Figure 1. It consists of a graph of nodes representing modules that are connected together to implement a specific function (graph may contain feedback). Debugging is performed hierarchically. First the set of buggy modules is identified. Then an identical debugging procedure is applied to the expanded netlist (represented as a graph) of each buggy module. The procedure is applied repetitively to smaller domains of the netlist using machine learning algorithms until multiple equivalent solutions emerge at the lowest level of circuits detail, that need to be resolved manually. The debugging algorithm at any level of the above process is as follows.

Learning kernels are attached in parallel to all the nodes in the signal flow graph (SFG) of the system. Figure 1 shows such a scenario for a phase locked loop (PLL) circuit. A suite of generated tests is used to stimulate the design and the weights of the learning kernels are updated in parallel to minimize the error signal magnitude at the output of Figure 1 (error between the observed output of the circuit with the learning kernels attached and the actual observed output of the physical circuit). The *core idea is that the error signal is minimized when the learning kernels attached to the buggy modules replicate the corresponding bug effects*. Note, aliasing can happen and this can be minimized using game theoretic hypotheses (what if scenarios) and monitoring descent gradients of the kernel coefficients and influencing these towards more likely solution scenarios during training. In the end, the kernels with the most active contributions to the error signal of Figure 1 are the likely sources of design bugs. Use of this debugging approach alone is expected to result in a 10X debugging time speedup. Preliminary experiments conducted on an RF transceiver indicate that high diagnostic accuracy can be achieved.

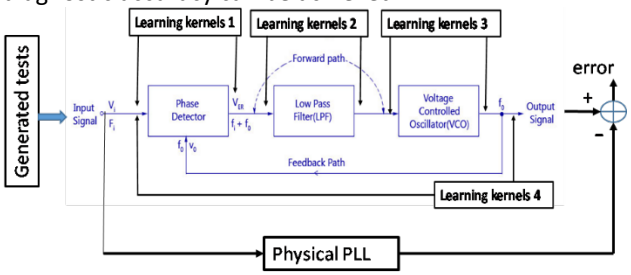

Figure 1. Multiple bug diagnosis using game theoretic hypotheses.

Keywords: mixed-signal, behavioral modeling, design debug, machine learning, design diagnosis

INDUSTRY INTERACTIONS

Texas Instruments, Intel, NXP

MAJOR PAPERS/PATENTS

[1] B. Muldrey and A. Chatterjee, "Automatic Model Generation for Mixed-Signal Systems Using Adversarial Stimulus Generation and Behavior Learning," ACM Transactions on Design Automation of Electronic Systems, submitted.

TASK 2810.025, MACHINE LEARNING-BASED LAYOUT ANALYSIS AND NETLIST OPTIMIZATION FOR DEFECT TOLERANCE AND DESIGN ROBUSTNESS TO PROCESS IMPERFECTIONS AND VARIATIONS

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SIGNIFICANCE AND OBJECTIVES

This project addresses two pressing needs of the industry: (i) Methodologies to identify sensitive layout topologies which result in hard-to-detect defects and affect yield. (ii) Gate-level optimization tools which not only generate netlists optimized for area and power but can also absorb process variations that cause deviations from acceptable performance.

TECHNICAL APPROACH

We leverage the power of Machine Learning (ML) in the proposed tasks: **(i) Layout analysis:** We use ML and synthetic pattern generation tools to explore a large design space and list all sensitive patterns for a given technology node, and also provide coverage and confidence metrics which ascertain the manufacturability of a given layout. **(ii) Netlist optimization:** We are developing methods to synthesize or locally transform a given netlist to maximize defect tolerance. Such methods will use ML entities trained on netlist-level features, along with several novel synthesis heuristics. An overview of the proposed work is shown in Figure 1.

SUMMARY OF RESULTS

Machine Learning-Based Layout Analysis: The coverage and confidence estimation methods to be developed through this project are aimed towards enabling or improving the State-Of-The-Art (SOTA) in various layout-level defectivity analysis methods such as hotspot detection, library risk assessment, etc. In the first phase of this project, we focussed on ML-based Hotspot Detection, wherein, we highlighted the common fallacies pervasive in the community, the pitfalls in the benchmarks which led to such fallacies. We also provided marching orders to improve the overall quality of Hotspot Detection [1]. Specifically, we showed that the most widely used ICCAD-2012 benchmarks lacked both the Hard-To-Classify (HTC) patterns and the Truly Never Seen Before (TNSB) patterns necessary to test the effectiveness of hotspot detection methods. To fill this void, we introduced and publicly released a new set of benchmarks. Furthermore, we tested the SOTA methods using the new benchmarks and found that they are neither capable of detecting TNSB patterns nor effective in reducing false alarms. We also demonstrated that synthetic pattern generation and design space exploration methods, proposed herein, provide significant improvements in TNSB hotspot detection and false alarm reduction.

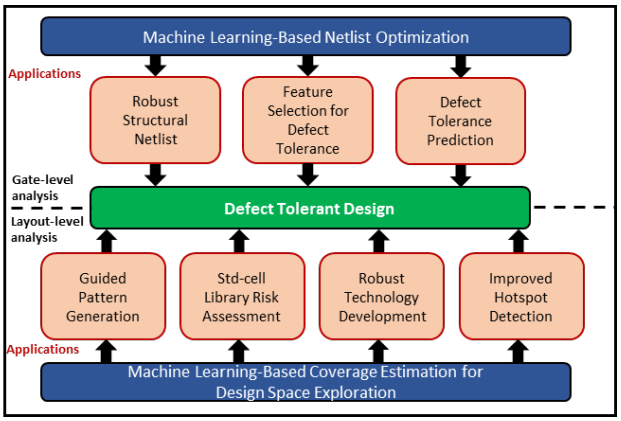

Figure 1. Machine Learning-Based Methods for Defect Tolerant and Robust Designs.

Machine Learning-Based Netlist Optimization: The proposed methods are aimed at transforming the design netlists to subsume the effects of latent defects occurring due to process imperfections and variations. They require an efficient means to quantify the defect tolerance of multiple functionally equivalent but structurally diverse netlists. Therefore, we introduced a probabilistic defect tolerance metric based on delay defect injection and simulation to quantify the percentage of observable defects at the netlist output. We explored the implications of defect tolerance from the perspective of library cell analysis, as well as netlist cell delay analysis, thereby seeking to formalize a comprehensive defectivity metric which considers various levels of netlist design. By quantifying the netlists on their defect tolerance, we intend to identify structural and functional netlist features that contribute towards the defect tolerance of these netlists, which can be exploited to transform our synthesis tools to generate robust netlists.

Keywords: Layout analysis, Coverage and confidence estimation metrics, Netlist optimization, Defect tolerance

INDUSTRY INTERACTIONS

Intel, Mentor, A Seimens Business

MAJOR PAPERS/PATENTS

[1] G. R. Reddy, K. Madkour, and Y. Makris, “Machine Learning Based Hotspot Detection: Fallacies, Pitfalls, and Marching orders”, ICCAD, 2019 (Accepted)

TASK 2810.027, MEASUREMENT AND MODELING OF STRESS/STRAIN ON ANALOG TRANSISTOR AND CIRCUIT PARAMETERS

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SIGNIFICANCE AND OBJECTIVES

In analog circuits, threshold voltage differences of millivolts can determine the performance/yield. Packaged stress can approach or exceed 100 MPa that can lead to 5-10% device parameter shifts. The goal of this work is to understand stress/strain effects on LDMOS, BJT and analog circuits.

TECHNICAL APPROACH

Measure key analog transistor parameters using a 4-point bending flexure wafer bending jig. Measure fundamental parameters such as deformation potential to develop models for threshold voltage shift and band gap changes. Use the measured data in device and circuit simulaitons (1) to improve R_{on} of LDMOS by > 25% using process induced strain and (2) improve bandgap reference voltage shift due to included strain.

SUMMARY OF RESULTS

Strained enhanced R_{on} has been measured for compression and tensile stress in both the longitudinal and transverse channel directions. This data are now being compared to LDMOS strained enhanced R_{on} device simulations

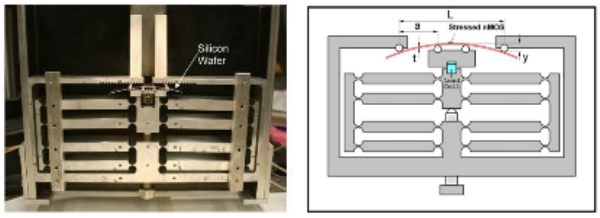
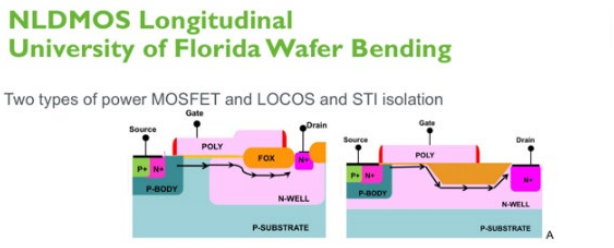


Figure 1. Four point wafer bending flexture measurement setup.

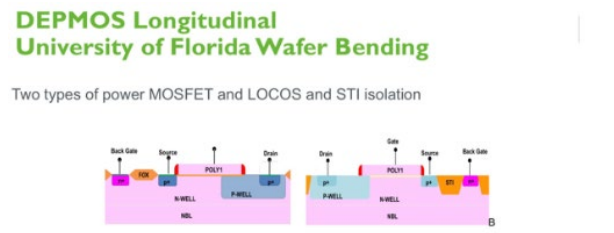
Using 4-point wafer bending data and device simulation, we have proposed three techniques to enhanced LDMOS performance with process induced strain. The process induced strain is generated using SiGe, capping layer and STI process induced strain. The goal of the simulations is to identify an LDMOS in which R_{on} can be improved by 25% using the process induced strain.



NLDMOS Longitudinal π (x 10^{11} Pa^{-1})

	LOCOS	LOCOS	STI	STI
	Low VG	High VG	Low VG	High VG
4 point bend	-23	-13	-37	-9
Expectation	--	-31		-31

Figure 2. 4-point wafer bending data on LDMOS showing strained enhanced R_{on}.



DEPMOS Longitudinal π (x 10^{11} Pa^{-1})

	LOCOS	LOCOS	STI	STI
	Low VG	High VG	Low VG	High VG
4 point bend	55	50	52	42
Expectation	--	71	--	71

Figure 3. 4-point wafer bending data on LDMOS showing strained enhanced R_{on}.

Keywords: strained Silicon, strained LDMOS, stress enhanced mobility, process induced strain

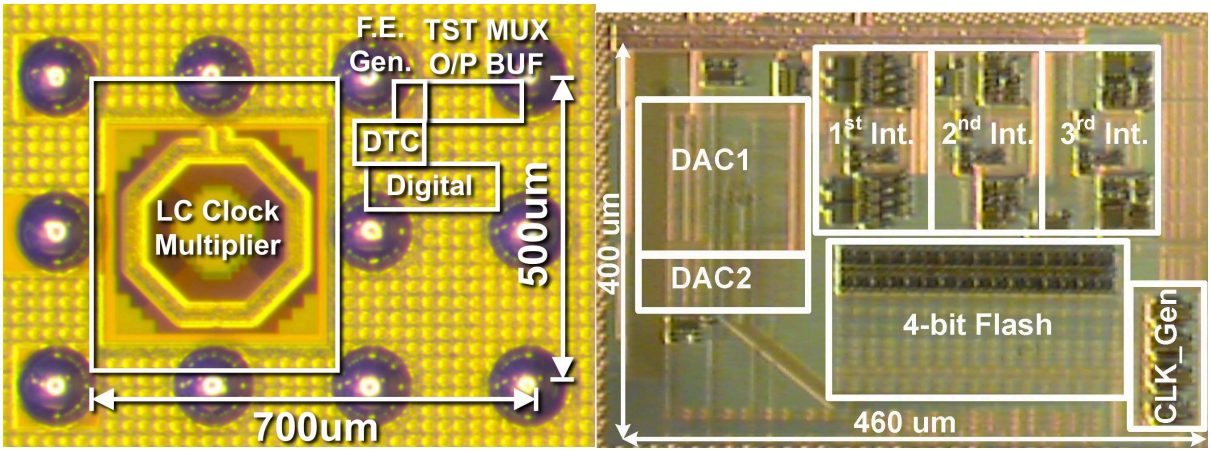
INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] J. Habar et al., SRC Poster "Strain effects on Analog Circuits," (Invited) 2010 VLSI-TSA, May, 2019, University of Santa Barbara, CA, USA.

Fundamental Analog Thrust



Category	Accomplishment
Fundamental Analog (Circuits)	A 3-GHz 8X clock multiplier with a jitter performance that is insensitive to frequency drift without using a continuous frequency tracking loop (FTL) is demonstrated. Using digital calibration techniques, the spurs are effectively suppressed down to -50.9 dBc. Fabricated in 28-nm CMOS technology, this prototype achieves an integrated jitter of 138 fs,rms while consuming 6.5 mW from a 1-V/0.8-V supplies and achieves -249-dB FoM. (2810.007, PI: Ali Niknejad)
Fundamental Analog (Circuits)	Excess loop delay (ELD) compensation using digital information stored on the input parasitic capacitance of a comparator is proposed to obviate the need for a dedicated ELD compensation circuit. The non-linear parasitic capacitance is linearized by maintaining the input transistor pair always in one region of operation. A 3rd order continuous-time delta-sigma modulator fabricated in a 0.13-µm CMOS process is used to validate the concept. The prototype ADC operates at 500 MHz sampling frequency, and achieves a peak SNDR of 74.4 dB and a peak SNR of 76.2 dB over a 15-MHz bandwidth while consuming 10.1 mW from a 1.2-V supply. (2712.014, PI: Nima Maghari)
Fundamental Analog (Circuits)	High data rate 180-GHz MSK modulated signals for dielectric waveguide communication with an output power of -3.5 dBm are demonstrated using a signal generator fabricated in 65-nm CMOS. Limited by the instrumentation for MSK signal analyses, the eyes of transmitted MSK signals have been verified for a data rate up to 10 Gbps. The spectra of transmitted signals for data rate up to 15 Gbps are also demonstrated. The MSK signal generator provides 5X higher data rate among all the previously reported MSK transmitters at 3X higher carrier frequency. (2810.015, PI: Ken O)

TASK 1836.158, DEVELOPMENT OF DIELECTRIC WAVEGUIDES FOR THZ RADIATION APPLICATIONS

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SIGNIFICANCE AND OBJECTIVES

The task comprises the design, fabrication, characterization and application of square dielectric waveguides for the propagation of THz and near-THz radiation using a "holey" fiber structure to engineer the refractive index profile and thereby support high-speed data transmission for interconnection between integrated circuits and between boards.

TECHNICAL APPROACH

Four waveguides with different geometries were designed, fabricated and tested for system integration: A solid core/holey cladding square THz waveguide for polarization division multiplexing (PDM); A vortex waveguide for space division multiplexing; A holey core/cladding structure, inspired from a vortex waveguide, for low loss PDM application; A hollow waveguide for low loss transmission. In addition to low loss geometries, low loss dielectrics such as TOPAS COC, quartz, and PTFE were studied.

SUMMARY OF RESULTS

The waveguide was designed using Beam Prop simulation package of Rsoft and fabricated using a custom built oven to preserve the square geometry. The waveguide was made of TOPAS (0.2 dB/cm material loss at 250 GHz). Fabricated waveguide was simulated considering fabrication defects. The simulation shows a confined mode across 180 GHz to 360 GHz despite manufacturing defects. Mode profile of the waveguide was mapped using a vector network analyzer (VNA) working at 220 GHz to 325 GHz and is in agreement with the simulation. The waveguide loss was measured using the same VNA and compared with the simulated data as shown in Table 1. Design, fabrication and characterization of the waveguide are presented in publications [1,2].

Table 1. A comparison among material loss, simulated, and measured waveguide loss.

Waveguide structure	loss [dB/cm]	Source	200 GHz	300 GHz
Holey core	Material	Literature	0.19	0.23
	Waveguide	Simulation	0.19	0.25
		Experiment	0.22	0.26

To further increase the channel capacity, the first THz vortex fiber was proposed. Fig. 1 (b, f) show the simulated and fabricated waveguide. The vortex waveguide design allowed further studying of the effect of hole sizes to beam propagation. Design, fabrication and characterization of the vortex fiber is detailed in [2].

Next, a holey core/cladding design, inspired from vortex THz waveguide, was proposed to lower the loss. A holey cladding forces the beam to travel in the core while creating low loss propagation with a holey core. This design shows a 0.15 dB/cm loss reduction compared to a square solid core holey cladding dielectric THz waveguide. Eight square waveguides form the core and cladding. The four cladding corner squares were eliminated to increase the core-confinement. The waveguide was assembled using commercially available capillaries. The operating frequency was chosen to be 90 GHz to 100 GHz due to available quartz sizes. Measurements show a fiber loss of 0.22 dB/cm. The significant loss difference between measurement and simulation is attributed to the coupling loss. A summary of the loss values are shown in Table 2.

Table 2. A comparison among material loss, simulated, and measured waveguide loss.

Waveguide structure	loss [dB/cm]	Source	90 GHz	100 GHz
Holey core/cladding	Material	Literature	0.05	0.05
	Waveguide	Simulation	0.03	0.04
		Experiment	0.22	0.19

In summary, four waveguides are provided for a 300-Gbps communication system, a holey cladding TOPAS waveguide, a quartz holey core/cladding, and a hollow PTFE waveguide. Each design outperforms the others in characteristics such as loss, coupling efficiency, mode isolation, operation bandwidth, and flexibility.

Keywords: Dielectric losses, Submillimeter waveguides, THz waveguide

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PUBLICATIONS

[1] N. Aflakian, T. LaFave Jr, R. M. Henderson, K. K. O, and D. L. MacFarlane, "Square dielectric interconnect for chip-to-chip THz communication," *IEEE Texas Symp. Wireless & MW. Circ. & Sys*. (2017).

[2] N. Aflakian, T. LaFave Jr, S. Ashrafi, K. O and D. L. MacFarlane, "Vortex dielectric waveguide," *Appl. Opt* 56 (25) 7123-7129 (2017).

TASK 2712.004, HIERARCHICAL ANALOG AND MIXED-SIGNAL VERIFICATION USING HYBRID FORMAL AND MACHINE LEARNING TECHNIQUES

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SIGNIFICANCE AND OBJECTIVES

Due to inherent complex behaviors and stringent requirements in analog and mixed-signal (AMS) systems, verification becomes a key bottleneck in the product development cycle. We are seeking to demonstrate Bayesian optimization (BO) based approaches to the challenging problem of verifying AMS circuits with stringent low failure requirements.

TECHNICAL APPROACH

At the heart of the proposed BO approaches is a delicate balancing between two competing needs: exploitation of the current statistical model for quick identification of highly-likely failures and exploration of undiscovered design space so as to detect hard-to-find failures within a large parametric space. We simultaneously leverage multiple optimized acquisition functions to explore varying degrees of balancing between exploitation and exploration. This approach is named *pBo* and is able to detect rare failures which other techniques fail to identify, and also do so with significantly improved efficiency.

SUMMARY OF RESULTS

We further build in a mechanism into the BO process to detect multiple failure regions and provide higher coverage, which is named *pHBCO.* The proposed BO approaches are readily parallelizable.

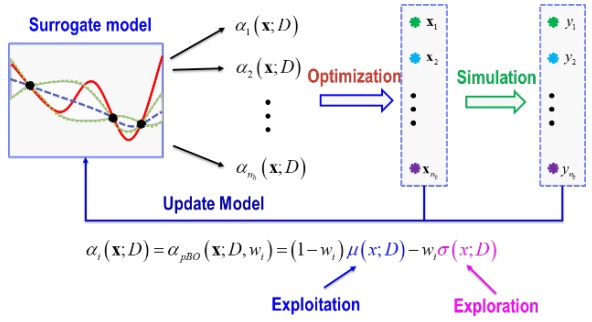

Figure 1. Parallel BO with multiple acquisition functions.

Figure 1 illustrates the proposed parallel multi-acquisition BO approach. Instead of using a single acquisition function, we simultaneously make use of multiple acquisition functions which have a different balancing between exploitation and exploration. These acquisition functions are solved and lead to multiple sampling location at each BO step. The diversity of these multiple acquisition functions are leveraged to enhance the robustness of BO w.r.t rare failure detection.

We consider an amplifier with 15 process variations, and with three specifications in Table 1. We compared our pBO and PHCBO approaches with BO methods with a single acquisition function including EI, PI, and LCB as well as the Monte Carlo method (MC) and the recent smart sampling technique (SSS). pBO and PHCBO outperform all other methods significantly. Our experiments show pBO and PHCBO are very effective in finding very rare failures and multiple failure regions which existing statistical sampling techniques and other BO techniques can miss.

Table 1. Comparison of several methods on failure detection of a differential amplifier. # Sim: # of training (simulation) samples used by each method; # 1st Failure Hit: # of samples used for finding the first true failure; # Failures (# Failure Regions): # of failures (failure regions) found.

Spec	Target	Method	# Sim	Worst Case	1st Failure Hit	# Failures	# Failure Regions	Runtime
GBW	22MHz	MC	600,000	28.7MHz	-	0	0	228h10m48s
		SSS	6,000	37.8MHz	-	0	0	1h59m33s
		EI	$50_{init}+350_{seq}$	24.6MHz	-	0	0	15m41s
		PI	$50_{init}+350_{seq}$	25.2MHz	-	0	0	15m58s
		LCB	$50_{init}+350_{seq}$	21.9MHz	161	240	1	15m23s
		pBO	$50_{init}+5\times70_{batch}$	21.9MHz	**66**	228	1	**11m49s**
		pHCBO	$50_{init}+5\times70_{batch}$	**20.5MHz**	**66**	181	4	**11m40s**
Gain	2.5dB	MC	600,000	7.16dB	-	0	0	228h10m48s
		SSS	6,000	13.61dB	-	0	0	1h59m33s
		EI	$50_{init}+350_{seq}$	3.75dB	-	0	0	16m01s
		PI	$50_{init}+350_{seq}$	2.17dB	282	74	5	15m53s
		LCB	$50_{init}+350_{seq}$	2.17dB	264	137	1	16m47s
		pBO	$50_{init}+5\times70_{batch}$	2.17dB	**109**	232	3	**11m18s**
		pHCBO	$50_{init}+5\times70_{batch}$	**1.80dB**	**109**	209	**10**	**11m56s**
CMRR	10dB	MC	600,000	11.42dB	-	0	0	228h10m48s
		SSS	6,000	16.57dB	-	0	0	1h59m33s
		EI	$50_{init}+350_{seq}$	11.79dB	-	0	0	16m03s
		PI	$50_{init}+350_{seq}$	11.52dB	-	0	0	16m08s
		LCB	$50_{init}+350_{seq}$	11.52dB	-	0	0	16m29s
		pBO	$50_{init}+5\times70_{batch}$	**7.48dB**	**376**	**20**	4	**12m01s**
		pHCBO	$50_{init}+5\times70_{batch}$	**7.48dB**	**376**	**20**	4	**11m39s**

Keywords: Machine learning, formal verification, hybrid verification, analog and mixed-signal.

INDUSTRY INTERACTIONS

Intel, Texas Instruments, NXP

MAJOR PAPERS/PATENTS

[1] H. Hu, Q. Zheng, Y. Wang, and P. Li, "HFMV: Hybridizing Formal Methods and Machine Learning for Verification of Analog and Mixed-Signal Circuits," IEEE/ACM DAC, 2018.
[2] H. Hu, P. Li, and J. Z. Huang, "Parallelizable Bayesian Optimization for Analog and Mixed-Signal Rare Failure Detection with High Coverage," IEEE/ACM ICCAD'18.
[3] H. Lin et al, "Sparse Relevance Kernel Machine-Based Performance Dependency Analysis of Analog and Mixed-Signal Circuits," in Machine Learning in VLSI CAD, 2019.

TASK 2712.005, AUTOMATED CROSS-LEVEL VALIDATION AND DEBUG OF MIXED-SIGNAL SYSTEMS IN TOP-DOWN DESIGN: FROM PRE-SILICON TO POST-SILICON

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SIGNIFICANCE AND OBJECTIVES

In top-down design, the models for mixed-signal functions are specified in a hierarchical manner. A key issue is that of establishing equivalence between behaviors across different design levels including fabricated silicon. Designs need to be de-bugged as early on in the design cycle as possible to minimize silicon respins.

TECHNICAL APPROACH

A *completely automated* algorithmic framework based on collaborative test stimulus generation and behavior learning is proposed for systematic debug of mixed-signal systems in the *presence of unknown (buggy) circuit behavior*. The proposed approach allows: (a) rapid detection and diagnosis of (*unknown*) logical and electrical bugs with minimal amount of computational effort using directed search strategies, (b) automatic generation of bug models using learning algorithms that can be fed back to the designer for design error correction and (c) fine grained diagnosis of design bugs down to individual design macro-blocks or sets of modules of minimum size.

SUMMARY OF RESULTS

A key contribution over the last year has been in the development of an adversarial stimulus generation vs. behavior learning algorithm in which a population of test stimuli is used to expose divergent behaviors between a high level model and its transistor level implementation while an underlying machine learner tries to minimize such divergence. Specifically, repeated observations of the dynamics of a pair of systems stimulated in unison (high vs. low level circuit description) are made across the population of stimulus considered. A statistical model describing their disagreement is constructed. The tails of the disagreement distribution represent high-risk, low-occurrence corners of the system's operational space. Our approach rapidly identifies the tail-regions of this distribution and generates a population of test stimuli likely to drive the systems into these regions. In doing so, they reveal valuable information (maximal behavior divergence) via simulation. The stimuli and response data are then used to train SVM regressors that augment the high level behavioral model concerned in an additive sense (see Figure 1) in such a way as to minimize the observed behavior divergence. The procedure is repeated iteratively through multiple stimulus generation and learning loops until no further divergent behaviors can be exposed by stimulus generation. At this point an augmented high level behavioral model is obtained that captures all transistor level behaviors with virtually zero error. Note that the procedure can also be used to extract behavioral models directly from fabricated silicon (in this case the low level circuit description above is the underlying hardware itself).

The method has been validated on RF transceiver designs, LDOs, PLLs and gain controlled amplifiers.

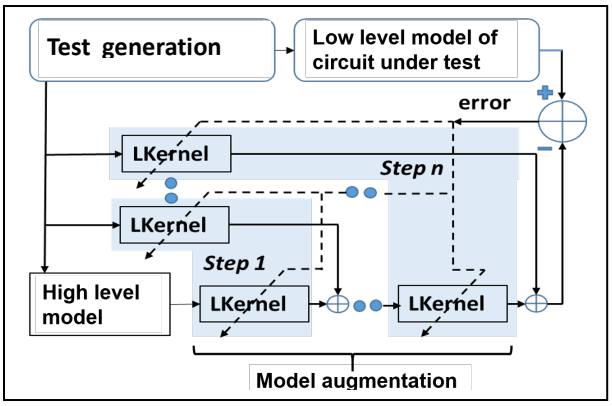

Figure 1. Automatic model generation approach.

Keywords: mixed-signal, behavioral modeling, design debug, machine learning, stimulus generation

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] B. Muldrey and A. Chatterjee, "Mixed signal design validation using reinforcement learning guided stimulus generation for behavior discovery," VLSI Test Symposium, 2019.

[2] B. Muldrey and A. Chatterjee, "Automatic Analog Behavioral Model Generation: Adversarial Adaptive Stimulus Generation and Machine Learning for Maximal Behavior Coverage," submitted to ICCAD 2019.

TASK 2712.010, RINGAMP-ASSISTED CIRCUITS/TECHNIQUES AND NEXT-GENERATION RINGAMPS

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SIGNIFICANCE AND OBJECTIVES

Analog-to-digital converters operating with gigasample clock rates are valued for eliminating baseband and IF downconversion in RF receiver signal chains. Interleaved achitectures are common but suffer from interleaving artifacts and scale with the performance of the single core. Therefore, optimized and power-efficient single-channel ADC architectures are requried for technology advancement.

TECHNICAL APPROACH

This effort seeks to improve the scalability and power efficiency of single-channel ADCs through the use of ring amplifier based ADCs with greater than 12b ENOB. A recent and prominent scalable circuit, the ring amplifier is a three-stage inverter based dynamic amplifier that can perform high-accuracy switched-capacitor amplification quickly and with properties of noise filtering.

SUMMARY OF RESULTS

Fig. 1 shows the basic schematic of a three stage pipeline ADC consisting of sub-ADC, DAC, and residue amplifier (RA). Typical pipelines utilize 1st order digital gain calibration also shown. The pipelined ADC utilizes RA in between MDAC stages in order to relax the noise requirements of the sub-ADCs. Throughput is also increased by simultaneously performing conversion and sampling in MDAC1 and MDAC2.

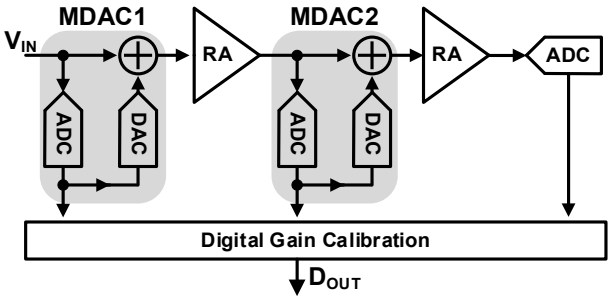

Figure 1. A three stage pipeline ADC.

Smaller pipelines using fewer MDACs have advantages in the form of less active circuitry. However, smaller pipelines require amplification to have a higher gain in order to accommodate the additional quantization of each MDAC stage. The higher gain requirement is necessary to amplify the smaller residue of a high quantization stage back to the full-scale for the following stage. Faster amplifier settling time is also desired to relax the timing requirements of the MDAC stages.

Fig. 2 shows the ac and transient response of a ring amplifier designed and simulated in a 22-nm CMOS process. The ring amplifier is designed with a 0.9-V supply voltage and the MDAC supplying the input step uses a reference voltage of 800mV. A DC loopgain of 60dB is shown for a closed loop gain of 16.

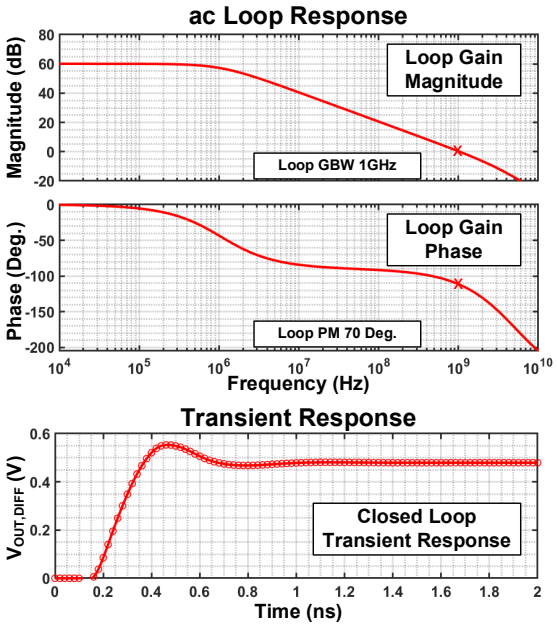

Figure 2. Small-signal ac and transient response of the ring amplifier with MDAC stage.

Going forward, we would like to move forward with the implementation of a single-channel RF ADC prototype in a 22-nm process.

Keywords: Ring amplifier, Single-Channel, RF ADC, High Speed

INDUSTRY INTERACTIONS

Texas Instruments, NXP, Intel

MAJOR PAPERS/PATENTS

[1] S. Leuenberger et al., "Emperical study of the settling behavior of ring amplifiers for pipeline ADCs," ISCAS 2018.
[2] P. Venkatachala et al. "Passive compensation for improved settling and large signal stabilization of ring amplifiers," ISCAS 2018.

TASK 2712.011, ROBUST RELIABLE AND PRACTICAL HIGH PERFORMANCE REFERENCES IN ADVANCED TECHNOLOGIES

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DEGANG CHEN,IOWA STATE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

Objective is to develop circuits that express the bandgap voltage at the output with a single electrical trim at standard test temperature and to adapt all-electrical trim to an on-demand run-time trim without requiring external test equipment. Significance is in development of references with lower temperature dependence.

TECHNICAL APPROACH

Our approach to the first objective is to revisit the issue of expressing the bandgap voltage at the output of a circuit directly rather than focusing on expressing the bandgap voltage only at an inflection temperature. Our approach to meet the second objective will be to identify what additional information can be obtained from correlated reconfiguration of a circuit in which the bandgap voltage and temperature are tightly intertwined in the device characteristics and design variables. Two test chips will be designed to obtain experimental verification of the performance of the new precision reference circuits.

SUMMARY OF RESULTS

Two new bandgap reference circuits that ideally express the bandgap voltage at the output have been created. In contrast to the existing approaches that provide curvature correction to partially correct for a nonlinear Tln(T) term that has been a nemesis for bandgap references for over 3 decades, these two new circuits are designed to eliminate the nonlinear Tln(T) term. These may be the first two circuits that actually express the bandgap voltage of silicon at the output.

One is based upon a dc current bootstrapping approach and is shown in Fig. 1. The second is based upon a dc voltage bootstrapping approach and is shown in Fig. 2.

The current bootstrapping circuit was fabricated in a 130-nm CMOS process. A Fluke Microbath Thermometer Calibrator was used to make measurements. Initial measured results were disappointing with the temperature dependence of the offset voltage of the operational amplifiers and the limited digital trim range of R_1 and R_3 contributing to a rather large temperature coefficient. With a low offset external op amp placed in parallel with one of the integrated op amps, the measured TC over an 80°C window was 14 ppm/°C. Though much better, the performance is still limited by the digital trim resolution of the resistors.

The voltage bandgap expression circuit has been designed and fabricated in a 65-nm CMOS process. Simulation results suggest performance at the sub 1 ppm/°C level is possible though the voltage bootstrapping approach. This approach may offer potential for achieving a TC below 0.1ppm/°C.

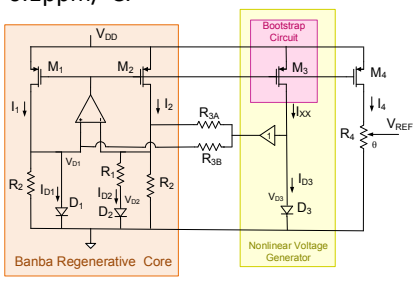

Figure 1. Current Bootstrapped Bandgap Extractor Reference.

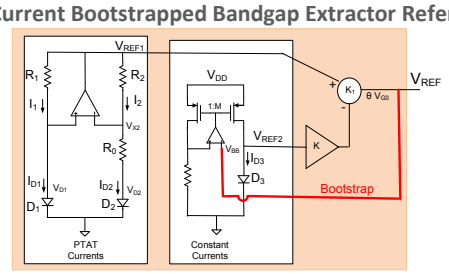

Figure 2. Voltage Bootstrapped Bandgap Extractor Reference.

Keywords: bandgap reference, diode model, curvature-compensation, voltage reference, bandgap separator

INDUSTRY INTERACTIONS

Texas Instruments, Intel, NXP

MAJOR PAPERS/PATENTS

[1] D. Chen and Z.Liu,Patent 10,359,801 "Voltage reference generator with linear and non-linear temperature dependency elimination ", issued July 23, 2019.

[2] Vijayalakshmi Naganadhan, "Analysis and Implementation of a V_{GO} Extraction Circuit", MS Thesis, Iowa State University, May 2019.

[3] Liu, N., Geiger, R.L., and Chen, D., "Bandgap Voltage V_{GO} Extraction with Two-temperature trimming for designing Sub-ppm°/C Voltage References", ISCAS, May 2019.

TASK 2712.014, LEVERAGING CMOS SCALING IN HIGH PERFORMANCE ADCS

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SIGNIFICANCE AND OBJECTIVES

We have revised all our previous fabrication from last year. We expect to receive the prototypes in Summer 2019 for ISSCC preparation. The prototypes include: Digital Correlated-Level Shifting Pipelined ADC, Correlated Dual-Loop (CDL) Delta Sigma (also filed for patent), and Contiguous-Time Delta-Sigma ADC with a 3-step double-noise shaping quantizer.

TECHNICAL APPROACH

The brief technical approach for the three prototype ADCs are as follows. (1) CDL Delta-Sigma: A new variation on Sturdy-MASH modulators which have been widely used. The structure will eliminate the need for quantizer error extraction which is a critical limiting factor in continuous-time multi-loop delta-sigma ADCs. (2) Digital CLS: targeting pipelined ADCs, this technique leverages the traditional CLS (Correlated Level Shifting) but removes the loading from the opamp and shifts it to digital domain by quantizing the next stage early. (3) 3-Step Quantizer: using time/phase frequency to quantize the signal in delta-sigma ADCs.

SUMMARY OF RESULTS

The detail design of CDL Delta-Sigma and the 3-step noise-shaping quantizer CT-DSM have been discussed in previous reports. This report outlines the innovation on the Digital-CLS pipelined ADC as shown in Fig. 1. The idea follows the traditional CLS with one major difference. In CLS, the amplification phase is divided into two sub phases, i.e. coarse and fine. In the traditional CLS, during the coarse phase the output of the Multiplying DAC (MDAC) stage is sampled during the residue amplification via a capacitor (C_{CLS}). In the fine phase, the C_{CLS} will be connect in series with the feedback capacitor of the amplifier to level shift the output and to enhance the settling accuracy of the opamp. The drawback of this is that C_{CLS} will impose capacitive loading during the coarse phase and will slow down the response of the opamp.

In contrast, the proposed Digital-CLS will eliminate the loading on the opamp. The concept follows the same phases as illustrated in Fig .1. However, in this case, the output of the first MDAC is quantized by the second stage MDAC at the end of the coarse phase. We note that this operation is always done in a traditional MDAC with a minor difference. it is done when the output of the 1st MDAC has settled. Given that the MADC stages will have only few-quantization bits (1-5), for the 2nd MDAC quantizer, the complete settling of its input, (output of the 1st MDAC) may not be necessary. We leverage this to effectively sample the second MDAC early (during coarse settling phase). The sampled digital code, which is a coarse approximation of the 1st stage output, will then drive a capacitive DAC in series with the output of the first MDAC in the fine settling phase. The overall effect is similar to the traditional CLS, with the efficiency of CLS depending on the number of bits in the second MDAC. As a result, not only the output of the second stage is available in advance which simplifies the timing, but also the gain, swing and linearity of the first MDAC is substantially improved, making this structure suitable for nanoscale CMOS where both dynamic range and opamp gain is hard to achieve.

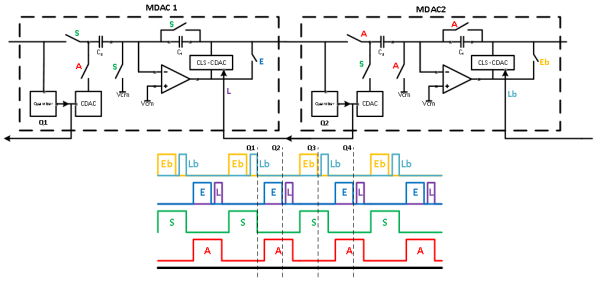

Figure 1. The proposed Digital CLS and its timing diagram.

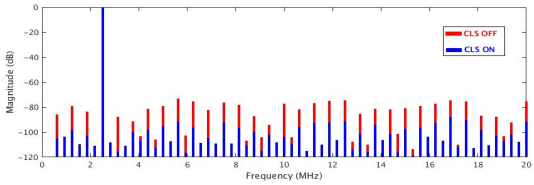

Figure 2. Simulated FFT using all transistor level.

Table 1. Performance summary based on full transistor level simulation of the D-CLS chip.

Fs	SNDR with D-CLS	SNDR w/o D-CLS	Pwr.	Tech.
40MHz	74dB	63dB	12mW	65nm

Keywords: Analog-to-Digital Converter, Quantization, Correlated Level Shifting, Low-Power, Scalable CMOS.

INDUSTRY INTERACTIONS

Texas Instruments, Intel, NXP

MAJOR PAPERS/PATENTS

[1] Changsok Han, "Correlated Dual Loop Delta Sigma Modulator", filed to patent, May 2018.
[2] C. Han et al, “A CT Delta-Sigma Modulator with Self-ELD Compensated Quantizer”, IEEE CICC 2018.

TASK 2712.025, REDUCTION OF LOW FREQUENCY NOISE IMPACT IN NANO-SCALE CMOS CIRCUITS

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SIGNIFICANCE AND OBJECTIVES

This project is investigating approaches to incorporate an on-chip measurement capability and post-fabrication configurable minimum size transistor arrays to reduce the low frequency noise impact in RF and analog circuits. This approach may be more effective for reducing low frequency noise impact than increasing the transistor size.

TECHNICAL APPROACH

Using transistors with lower noise through post fabrication selection, and approaches for integrating a highly sensitive noise measurement circuit in a frequency synthesizer commonly found in RF and millimeter wave transmitter and receiver will be investigated. Intelligent search algorithms will be applied to select the combinations with low frequency noise with the minimum number of measurements. Approaches to increase the operating frequency of VCO and the factors that limit the maximum operating frequency are being investigated. Lastly, feasibility to extend this technique to other circuits is being investigated.

SUMMARY OF RESULTS

The number of intended dopants and un-intended defects in a minimum sized device is reduced with technology scaling. One missing dopant or having an additional or fewer defect can dramatically increase or decrease the threshold voltage, current and noise. A 4.3-GHz voltage controlled oscillator (VCO) that embraces the variability of nano-scale transistors to reduce its phase noise by taking advantage of reduced low frequency noise of some minimum sized transistors with a fewer defects or traps through post-fabrication selection is reported [1].

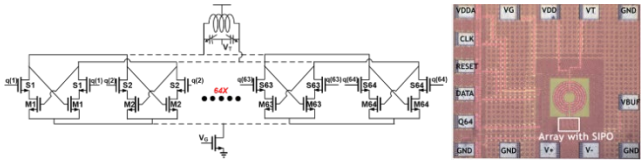

Figure 1. 4.3-GHz voltage controlled oscillator using an array of cross-coupled NMOS transistors.

The VCO (Fig. 1) uses an digitally addressable array of cross-coupled minimum size NMOS transistor pairs for post fabrication selection and is fabricated in 65-nm CMOS. An algorithm based on Hamming distance using the phase noise measurements of ~1,500 combinations was used to identify the combinations that have the record phase noise of -130dBc/Hz at 1-MHz offset from a 4.3-GHz carrier, while consuming 5.2 mW from a 1-V supply.

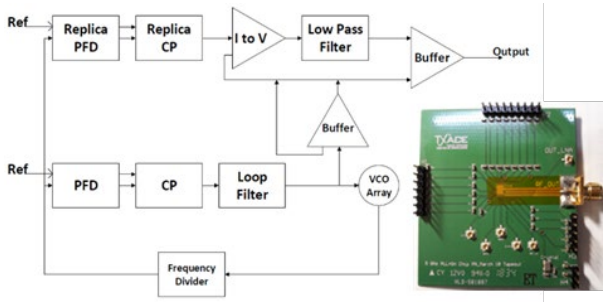

Figure 2. Phase locked loop incorporating a 4.3-GHz voltage controlled oscillator using an array of cross-coupled NMOS transistors and components for on-chip phase noise measurements. Printed circuit board with a PLL IC.

To make this technique practical, an affordable and sufficiently rapid on-chip measurement technique for the phase noise that can resolve noise below -130dBc/Hz for a 4.3-GHz carrier is being researched. Fig. 2 shows a phase locked loop (PLL) including components for measurements of phase noise which has been fabricated in a 65-nm CMOS process. Fig. 2 also includes a photograph of the printed circuit boards with a PLL IC. The PCB's are being used for evaluation of the technique as well as development of algorithms for identification of low noise combinations. An updated version of the PLL IC in 65-nm CMOS that requires an ADC with a reduced dynamic range has also been submitted for fabrication. Applicablilty of this technique to other circuit elements such as a receiver mixer and a baseband amplifier as well as for circuits operating higher operating frequencies are being investigated.

Keywords: low frequency noise, on-chip noise measurements, post-fabrication selection

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] A. Jha et al., "-197dBc/Hz FOM 4.3-GHz VCO Using an Addressable Array of Minimum-Sized NMOS Cross-Coupled Transistor Pairs in 65-nm CMOS," *IEEE Symposium on VLSI Circuits*, pp. 214-215, June 2016, Honolulu, Hi.

TASK 2712.031, ADAPTIVE TRIMMING AND TESTING OF ANALOG/RF INTEGRATED CIRCUITS (ICS)

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SIGNIFICANCE AND OBJECTIVES

As part of the post-fabrication process, the optimum operating voltage (V_{min}) is searched in order to reduce the power consumption of each device. This search is commonly performed on modern mobile devices that rely on finite energy sources. The goal is to adaptively identify the V_{min} by speeding up the search without affecting the yield.

TECHNICAL APPROACH

We proposed a machine learning-based approach that predicts the V_{min} search parameters at the wafer level. This adaptation relies on the process signature of each wafer as it is expressed by its e-test vector. The two parameters that were considered were the starting point of the search as well as the maximum voltage. When chosen adaptivelty, these parameters limit the number of search steps performed, reducing the overall calibration time. Both linear and binary search were explored to cover all the currently performed strategies.

SUMMARY OF RESULTS

An industrial dataset of more than 800 wafers, each with more than 500 devices, was made available by a SRC member company. For each device in the dataset, the traditional linear V_{min} search was performed, and the resulting voltages were recorded. Adaptation of the binary search-based calibration was explored despite the fact that this particular product-ATE setup combination does not allow its immediate utilization and deployment.

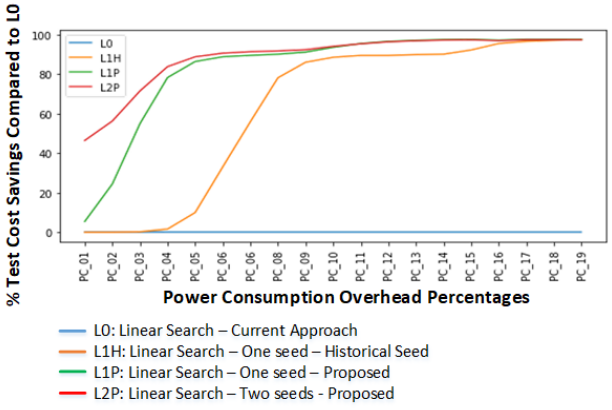

Figure 1. Linear V_{min} search savings.

Figure 1 shows the percentage of cost savings achieved for each of the selected power consumption percentage bounds when a linear search is performed. The L1H curve shows that the use of the historical V_{start} value can achieve up to ~90% cost savings compared to the current static methodology (L0). Unfortunately, these savings start at the expense of 3-4% power consumption overhead and slowly ramp-up to 80% when there is more than 8% overhead. In comparison, our proposed method, which adapts both the V_{start} and V_{high}, achieves ~50% savings at 1% overhead.

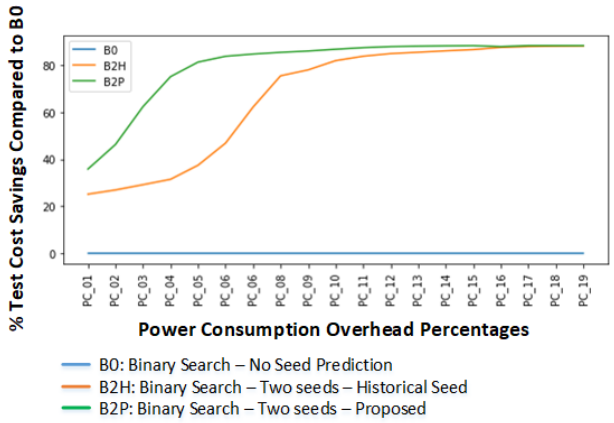

Figure 2. Binary V_{min} search savings.

Similarly to the linear search, a comparison was made against the historical seed and the proposed approach for binary search, as shown in Figure 2. In this case, we were able to achieve 38% test cost savings at the expense of 1% power consumption overhead. These savings continued to increase until they flattened out at approximately 5% overhead, which is considerably sooner compared to historical-based parameter values.

We presented an adaptive, wafer-level, machine learning-based approach to reduce the V_{min} calibration costs, based on the e-test signature of a wafer. This is achieved by adjusting the V_{min} search parameters to reduce the number of search steps without affecting the production yield.

Keywords: adaptive test, post-silicon calibration, machine learning, trimming

INDUSTRY INTERACTIONS

Texas Instruments, NXP, Intel

MAJOR PAPERS/PATENTS

[1] C. Xanthopoulos, D. Neethirajan, S. Boddikurapati, A. Nahar, and Y. Makris, "Wafer-Level Adaptive V_{min} Calibration Seed Forecasting," Design, Automation and Test in Europe (DATE), 2019.

TASK 2810.005, CIRCUIT DESIGN FOR ESD AND SUPPLY NOISE MITIGATION

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SIGNIFICANCE AND OBJECTIVES

This project seeks to develop (1) IC-level power distribution networks that promote power integrity even in the presence of power-on ESD, and (2) biasing strategies for IO circuits that boost ESD resilience, thereby enabling high-speed IO circuits to meet both performance requirements and ESD target levels.

TECHNICAL APPROACH

This work identifies ESD-induced reliability hazards, including latch-up, and evaluates solutions. The investigations focus on integrated voltage regulators, rail clamp circuits, and high-speed IO. Promising solutions will be implemented in silicon. Additionally, the group continues to develop on-chip noise sensors that are most sensitive to ESD-induced noise. Experiments will be performed to establish whether ESD noise can be distinguished from other disturbances (e.g., supply brown out, simultaneous switching noise) or a bonafide reset signal. Such sensors can aid in mitigation of ESD-induced soft failures.

SUMMARY OF RESULTS

In simulation and analysis, we have demonstrated that ESD protection circuits intended for system-level protection (i.e., power-on ESD) can reduce the amplitude of simultaneous switching noise by several hundred millivolts. A test chip was designed to validate the analysis and is currently being fabricated. The on-chip supply noise and ESD resilience of the IC will be measured.

System-level ESD can reach the IO pins of an IC, especially if the IC is linked to an external connector. The ESD current induces noise on the IO supply and that noise propagates to the other on-chip supplies via the PDN (power distribution network). Measurement results on two test chips showed that, in some cases, the use of an integrated voltage regulator will mitigate the noise on the non-IO supplies. We have carried out a detailed analysis of those results.

Keywords: ESD, latch-up, integrated voltage regulator, simultaneous switching noise, rail clamp

INDUSTRY INTERACTIONS

Texas Instruments, NXP, Intel

MAJOR PAPERS/PATENTS

[1] Y. Xiu, N. Thomson and E. Rosenbaum, “Measurement and simulation of on-chip supply noise induced by system-level ESD,” *IEEE Transactions on Device and Materials Reliability*, vol. 19, no. 1, pp. 211-220, 2019.

TASK 2810.007, FULLY INTEGRATED PHASE NOISE CANCELLATION TECHNIQUES

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SIGNIFICANCE AND OBJECTIVES

This research will explore new architectures for frequency multiplication to reduce power consumption and to reduce phase noise. The frequency multipliers are compact, friendly to digital scaling, but suffer from high spurs and phase noise. To correct for these shortcomings, fully integrated digital phase noise calibration and spur suppression are also realized and co-designed with the analog circuitry.

TECHNICAL APPROACH

In the previous reporting period, we proposed phase noise cancellation circuitry that can be cascaded after the clock source in a flexible manner to reduce the impact of phase noise and spurs. In this period we have taken a new direction and are now improving the phase noise by modifying the clock multiplier, which generates a high frequency clock from a lower frequency XTAL reference, a key building block in any analog or digital communication system. The clock reference is used as a pulse generator to excite a high frequency LC tank. Residual AM and PM distortion is removed with digital calibration.

SUMMARY OF RESULTS

A block diagram of the proposed frequency multiplier is shown in Fig. 1. At the core, the clock multiplier uses the clean reference edges to create a short pulse rich in harmonics that excite the fundamental resonance mode of the LC tank. Every pulse injection results in a decaying envelope, which is restored to full logic levels using a limiting amplifier.

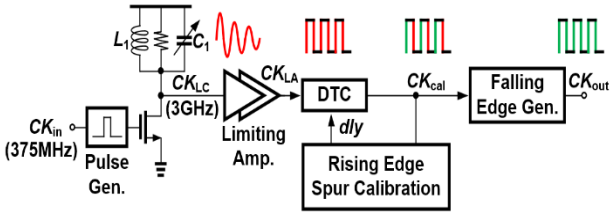

Figure 1. The architecture for the LC tank based clock multiplier.

The architecture has a lot of features in common with an injection-locked clock multiplier, with the exception that it does not use feedback. As such, it does not suffer from finite injection locking bandwidth, which can results in much higher phase noise when the multiplied clock falls outside the resonant frequency, which results in much higher phase noise. The architecture, though suffers from both AM spurs and PM spurs. PM spurs arise due to AM-PM conversion due to the non-linear capacitance in the tank. This manifests itself as non-equal periods in the waveform. These spurs are removed using a digital technique (Fig. 2(a)) whereby a digital-to-time converter (DTC) introduces a fractional delay per period to correct the period mismatch from cycle to cycle. A high speed MUX is used to feed the correct delay per cycle, learned automatically through a calibration step. A measured prototype (Fig. 2(b)) in 28-nm CMOS demonstrates the validity of the proposed technique. A 3-GHz clock is generated with -50.9 dB spurs and a 138fs$_{rms}$ jitter consuming 6.5mW and occupying 0.26mm^2.

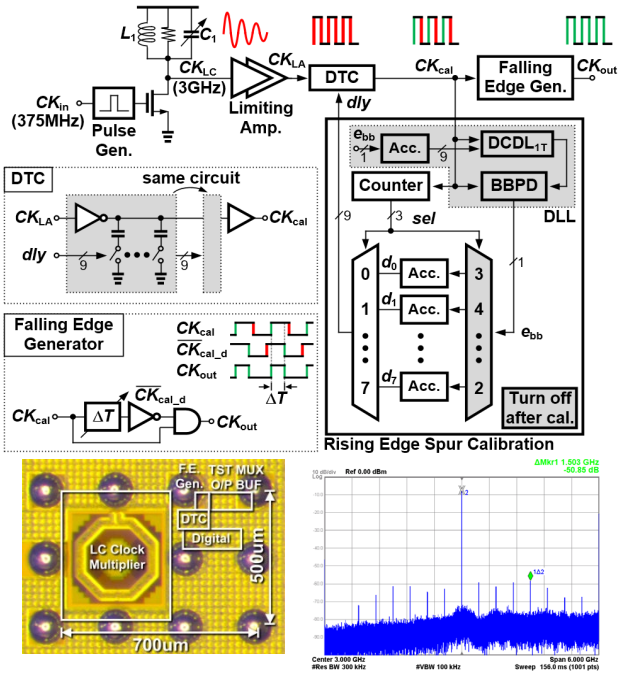

Figure 2. (a-top) Architecture of the digital spur (and phase noise) cancellation circuitry. (b-bottom) Measured spectrum from prototype.

Keywords: spur cancellation, injection-locked clock multiplier, clock multiplier, digital spur suppression

INDUSTRY INTERACTIONS

Intel

MAJOR PAPERS/PATENTS

[1] Y. Li et al., "A 138fsrms-Integrated-Jitter and −249dB-FoM Clock Multiplier with −51dBc Spur Using A Digital Spur Calibration Technique in 28-nm CMOS," *Symposia on VLSI Technology and Circuits (VLSI)*, June 2019.

TASK 2810.009, MIXED-SIGNAL BUILDING BLOCKS FOR ULTRA-LOW POWER WIRELESS SENSOR NODES

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DAVID BLAAUW, UNIVERSITY OF MICHIGAN

SIGNIFICANCE AND OBJECTIVES

This project develops novel and state-of-art performing ultra-low power mixed-signal circuits, suitable for IoT systems. This includes timekeeping circuits, amplifiers, and CMOS-based sensors.

TECHNICAL APPROACH

The most challenging ultra-low power circuit components are mixed-signal circuits such as timers, clock sources, sensing and interface circuits (e.g., temperature sensors and low-noise amplifiers). Some of these cannot be duty cycled (e.g., timers), while others require both low noise and low power (e.g., amplifiers), which are traditionally mutually exclusive. This work proposes new ULP designs for: 1) crystal oscillator based real time clocks (RTCs), 2) temperature-compensated wakeup timers, 3) temperature sensors, and 4) front-end low-noise amplifiers.

SUMMARY OF RESULTS

We proposed a 32-kHz crystal oscillator (XO) with duty-cycled energy injection. The design techniques we proposed are: (1) NMOS-only pulsed driver to realize 71% injection efficiency; (2) duty-cycled pulses of energy injections at peaks and valleys of the XO waveform to greatly reduce the dynamic power of the control circuits; (3) a current reference with switched-capacitor resistance and ultra-low leakage switches to provide precise current in the presence of PVT variations; (4) a constant-delay clock slicer to both convert the sinewave XO waveform to a square wave and generate delays for timing of the energy injection. Figure 1 shows the architecture of the proposed 32-kHz crystal oscillator.

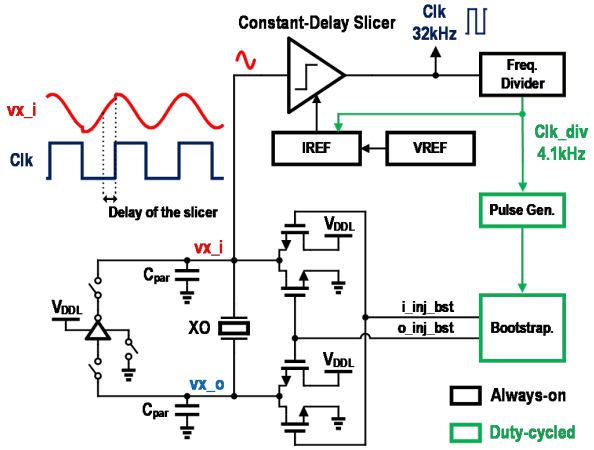

Figure 1. Architecture of the proposed crystal oscillator.

The proposed XO is designed in a 40-nm CMOS process and the layout area including the start-up circuit is 0.02 mm^2. With two power supplies, 0.5V and 0.15V, ECS-1X5X crystal, 1pF load capacitance, and 141mV oscillation amplitude across the crystal, the simulated power consumption is 0.47nW at 25°C, which is the lowest for the reported 32-kHz crystal oscillators.

Keywords: CMOS, crystal oscillator, ultra-low power

INDUSTRY INTERACTIONS

NXP

MAJOR PAPERS/PATENTS

TASK 2810.013, FREQUENCY-DOMAIN ADC-BASED SERIAL LINK RECEIVER ARCHITECTURES FOR 100+GB/S SERIAL LINKS

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SEBASTIAN HOYOS, TEXAS A&M UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

Clock jitter places fundamental performance limitations on common time-interleaved ADC architectures, necessitating clock generation and distribution circuitry that achieve rms jitter of a few hundred femtoseconds. The ADC-based high-speed serial link design techniques in this proposal aim to significantly improve jitter robustness and reduce ADC resolution and digital equalization complexity.

TECHNICAL APPROACH

A new configurable frequency-domain ADC-based receiver serial link architecture is in development that is capable of providing jitter robustness for baseband and coherent multi-tone modulation applications. The receiver utilizes ADCs with novel techniques to improve the configurable SAR sub-ADC speed and efficiency, including a design that utilizes reference pre-emphasis to enhance DAC settling and low-overhead reconfiguration logic to enable per-channel operation with a scalable resolution. Efficient digital reconstruction, equalization, and inter-channel interference filters for symbol detection are also in development.

SUMMARY OF RESULTS

Figure 1 shows the proposed frequency-domain ADC-based receiver [1]. The input CTLE drives the front-end channels that have a mixer for down-conversion, a Bessel low-pass filter, and an ADC for sampling and digitization. These digitized samples are then processed by FIR filters in the DSP and their outputs are combined to either perform symbol estimation in PAM-4 baseband mode or to perform both inter-channel interference (ICI) and ISI cancellation in multi-tone mode. This architecture provides several benefits. First, the mixers perform self-equalization and provide some channel loss compensation, allowing for a reduction in digital equalization complexity. Second, high-frequency noise introduced by the mixers and CTLE is attenuated by the channel filters. Finally, the inclusion of digital receive-side ICI cancellation filters in the proposed 128Gb/s system allows for a 50% improvement in relative channel spacing when compared against a previous 10Gb/s mixed-signal implementation.

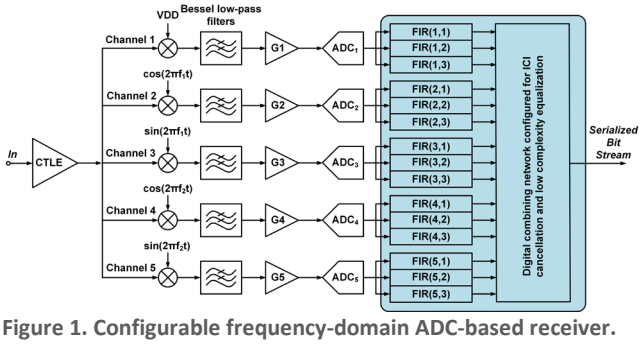

Figure 1. Configurable frequency-domain ADC-based receiver.

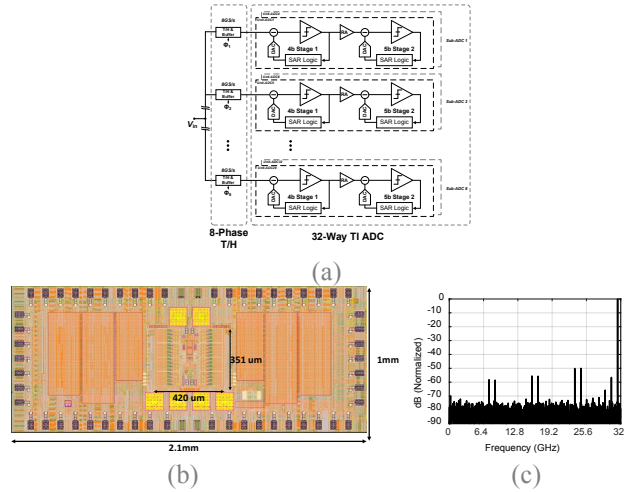

Figure 2. 8-b 64GS/s time-interleaved pipelined-SAR ADC: (a) block diagram, (b) prototype chip layout in Intel's 22nm FinFET process, and (c) simulated output DFT with Nyquist input.

The unit ADCs for the proposed frequency-domain ADC-based receiver were implemented as part of an 8-b 64GS/s time-interleaved ADC that was taped-out in the Intel 22-nm FinFET process (Figure 2). The architecture consists of eight interleaved track and hold bootstrapped switches followed by four pipeline-SAR unit ADCs running at 2 GS/s each. T-coil input terminations are used to extend the 3 dB bandwidth up to 32 GHz. Post-layout simulations indicate a 6.6 ENOB for the complete ADC while consuming 147 mW.

Keywords: analog-to-digital converter, frequency-interleaving, jitter, receiver, serial link

INDUSTRY INTERACTIONS

Intel, Texas Instruments

MAJOR PAPERS/PATENTS

[1] J. C. Gomez Diaz et al., "Jitter-Robust Multicarrier ADC-Based Serial Link Receiver Architecture," (Invited) Accepted in 2019 MWSCAS, August, 2019, Dallas, TX.

TASK 2810.015, DEMONSTRATION OF 120-GBPS DIELECTRIC WAVEGUIDE COMMUNICATION USING FREQUENCY DIVISION MULTIPLEXING (FDM) AND POLARIZATION DIVISION MULTIPLEXING (PDM)

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SIGNIFICANCE AND OBJECTIVES

This project in collaboration with the efforts on transitions and multiplexer/demultiplexer, and on low loss dielectric waveguides for operation at 100-400 GHz seeks to demonstrate 120-Gbps Polarization Division Multilexing and Frequency Division Multiplexing (45-GHz bands around 180 and 315 GHz) communication over a 1-m long dielectric waveguide using CMOS circuits.

TECHNICAL APPROACH

To excite waves at two different frequency bands with two different polarizations in a dielectric waveguide, transmitters for the 180 and 315-GHz bands will be used to drive a cross dipole. The receivers of two bands will be connected to one of the cross dipoles, while the second dipole will be terminated to reduce reflection. These receivers and transmitters will be used to demonstrate FDM operation. For PDM operation, the receiver will be rotated 90 degrees to pick up signals with the second polarization.

SUMMARY OF RESULTS

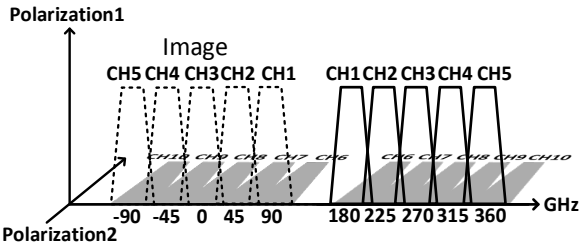

Figure 1. Channel allocation for the proposed dielectric waveguide communication system employing both frequency division multiplexing (FDM) and polarization division multiplexing (PDM). The system can potentially support an aggregated data rate of 300 Gbps [1].

Fig. 1 shows the channel allocation of the proposed dielectric waveguide system consisting of transmitters, a transition and a demultiplexer from the transmitters to a waveguide, a waveguide, a transistion and a multiplexer from a waveguide, and receivers. The system uses five 45-GHz frequency bands spanning 157.5 to 382.5 GHz and supporting two polarization channels for a total of 10 30-Gbps channels for an aggregated data rate of 300 Gbps.

This project in particular seeks to demonstrate 120-Gbps PDM and FDM electronic communication over a 1-m long dielectric waveguide using circuits fabricated in 65-nm CMOS. The 45-GHz bands around 180 and 315 GHz will be utilized for FDM. The transmitters and receivers connected through a diplexer or a combiner to a cross-dipole for the demonstration are shown in Fig. 2.

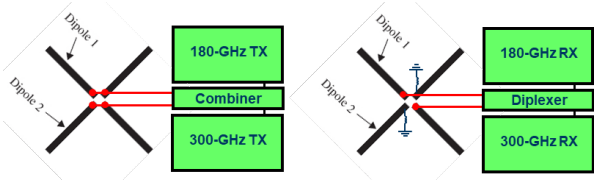

Figure 2. TX and RX chains for PDM and FDM operation with cross-dipoles.

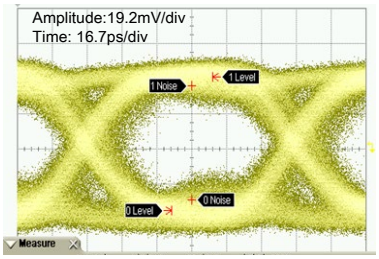

Figure 3. Eye diagram for a 10-Gbps data stream (I channel: 5Gbps PRBS31, Q channel: 5Gbps 1010 pattern)

180 and 315-GHz receiver and transmitter pairs with a diplexer and a cross-dipole have been taped out in 65-nm CMOS. Fig. 3 shows a measured eye diagram of 10-Gbps MSK data stream generated and demodulated by the 180-GHz transmitter and receiver. The transmitters and receivers will be integrated with a multiplexer/demultiplexer, transitions and a low loss holey waveguide (8dB/m) for the multiple channel demonstration utilizing PDM and FDM.

Keywords: dielectric, waveguide, commmunication, millimeter waves

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] Q. Zhong et al., "300-GHz CMOS QPSK Transmitter for 30-Gbps Dielectric Waveguide Communication," *IEEE CICC*, April 2018, San Diego, CA.
[2] Q. Zhong et al., "CMOS Terahertz Receivers," (Invited) *IEEE CICC*, April, 2018, San Diego, CA.

TASK 2810.018, TRANSITION DESIGN FOR HIGH DATA RATE LINKS AT SUBMILLIMETER WAVE FREQUENCIES

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SIGNIFICANCE AND OBJECTIVES

Techniques to excite an integrated on-chip cross-dipole antenna with a broadband dielectric waveguide using a printed circuit board (PCB)-based quadruple ridge waveguide as the transition structure are being investigated. A two-channel aggregate system is designed to operate at 180 and 315 GHz with a 45-GHz bandwidth.

TECHNICAL APPROACH

The technical approach involves desing using ANSYS HFSS simulation of the individual front-end structures which include dual-band dipole antennas, a broadband dielectric waveguide and a broadband metallic quadruple ridge waveguide. Upon completion of the element design, we perform an impedance and electromagnetic field matching optimization to improve the efficieny of the transitions. We extract the S-parameters of the components and import them into a circuit simulator for impedance matching. The quadruple ridge waveguide will include an adapter that will support the dielectric waveguide for a low cost robust interface/socket for high data rate wireline systems.

SUMMARY OF RESULTS

We are developing a metallic quadruple ridge waveguide to provide an electrical and mechanical transition for the high data rate wireline link. We are partnering with the team of Kenneth O on the actual system demonstration. We have designed and fabricated three on-chip dual-band dipole antennas. One set has been designed with the receiver chip and is fully integrated for system demonstration (March 2018). This design allows for one polarization to operate. The second on-chip dual-band dipole is a standalone structure intended for studying the bandwidth and return loss with a minimal size keep out ground area (December 2018). The third antenna was designed in collaboration with Dr. O's team for the transmitter chip used in the simplex wireline system (March 2019). This design allows for horizontal and vertical polarization.

Figure 1 shows a conceptual cross-section from HFSS simulation, with the metallic or copper waveguide/transistion being excited by a dipole antenna (not shown). The radiation from the antenna excites the copper waveguide (at 180 GHz) and continues to a dielectric waveguide. A similar transition is used at the receiver end to guide the signal back to the chip for demodulation and detection.

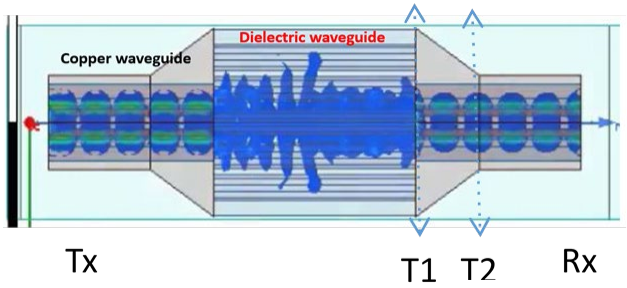

Figure 1. Field propagation using copper waveguide or transistion and dielectric waveguide.

The measured and simulated performance of dielectric waveguide and cross-dipole antenna have been compared, and previously reported. Table 1 summarizes the simulated input impedances for the three structures. The dual-band dipole antenna is converted from a differential to single-ended feed using a wideband balun. The balun effectively transitions the two impedances to 50 Ω. The topas dielectric waveguide has impedances, of 315 and 1200 Ω at 180, and 315 GHz, respectively. We are exploring a transition design optimized at the geometric mean of the impedances and frequencies. The copper waveguide and transition from T1 to T2 will be manufactured using printed circuit board materials. This is in keeping with the technology for the transmitter and receiver control module boards.

Table 1. Simulated impedances of antennas, transitions and waveguide.

Structure	Dual-band dipole	Copper quad-ridge waveguide	Topas dielectric waveguide
Z(Ω)@ 180 GHz	43.6 + j 20	50	315 + j 0.01
Z(Ω)@ 315 GHz	90.1 – j 9.2	50	1196 + j 0.4

Keywords: quadruple ridge waveguide, dielectric waveguide, cross dipole, transition, dual band dipole

INDUSTRY INTERACTIONS

Texas Instruments, IBM

MAJOR PAPERS/PATENTS

[1] N. Afllakian et al., "Functional Performance of a Millimeter Wave Square Holey Dielectric Waveguide," 2019 Radio and Wireless Symposium, Jan. 2019, Orlando, FL.

TASK 2810.019, DESIGN AUTOMATION IN COVERAGE MANAGEMENT IN ANALOG AND MIXED SIGNAL SOCS

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SIGNIFICANCE AND OBJECTIVES

The objective of this task is to design and implement CAD support for coverage management of AMS artifacts in mixed signal SoCs. Towards this goal, we are working toward formal metrics for AMS coverage and developing mechanisms for computing such metrics in standard commercial simulators.

TECHNICAL APPROACH

We have proposed an extension to SystemVerilog coverage artifacts for defining AMS coverage *bins*. This includes the types: range (normal and deglitched), level, *ddt*, glitch, and mode coverage. We also support different monitoring types, such as cross-coverage, timed monitoring, mode specific monitoring, etc. These enable verification engineers to analyze the operating regions of the design from various functional perspectives. A tool has been developed which interfaces with off-the-shelf AMS simulators with standard VPI-callbacks and does an online computation of the different coverage values.

SUMMARY OF RESULTS

We have obtained results on two test-cases, 1) LDO transistor level netlist circuit, and 2) waveform dumps from UVLO, OVLO comparators. On both the test-cases we have computed different coverage types with our tool CoveRT(Coverage Reporting Tool). The results are given in Table 1. By comparing the results of these coverage types among simulations across different process corners and testbenches, one can identify the coverage gaps present during the testing phase.

Table 1. Coverage results on LDO and waveform.

Port	Range	De-glitched Range	Level
LDO_1P8A	-0.01: 2.70	-0.01 : 1.83	0, 1.825, 1.805, 1.785, 1.715, 1.765
FB_OUT	-0.01 : 1.46	-0.01 : 1.02	0, 0.005, 1.015, 1.005, 0.995, 0.985
NRST_1V8	-0.12 : 3.01	-0.12: 3.00	3.005
VREF_LOW	-0.01 : -0.51	-0.01 : 0.50	0.025

A cross coverage between the range of V_{out} and range of the feedback voltage, FB_out, of the LDO is shown in Figure 1. Such cross coverage shows FB_out generally follows the output voltage and the output of the LDO settles at an operating point. Whenever there is a deviation of the output from the set value of 1.8, the feedback voltage, FB_out, also undergoes a similar change and brings the LDO back to its normal operating region.

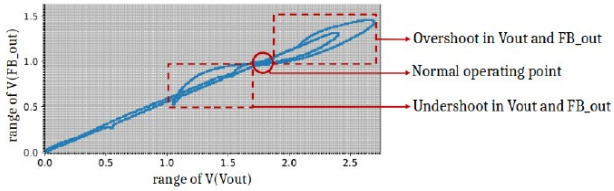

Figure 1. Cross coverage between ranges of V_{out} and FB_out.

A similar figure can also be generated by taking the cross coverage between the range of output voltage and load current. On adding the operating mode (shutdown, startup, regulatory, shortcircuit, drouput) of the LDO as a third parameter to this cross coverage, one can also examine the shortcircuit current of the LDO, i.e., the range of currents which takes the LDO into the shortcircuit mode.

On using the timed monitoring of coverage types, the user is presented with a report containing the total time the signal has spent in each bin in the voltage/current domain, and also the disjoint time intervals that the signal spends in each bin. This report will facilitate verification engineers to distinguish between two or more simulations which are known to produce dissimilar coverage results.

To summarise, we believe that our contribution is rooted at the needs of verification engineers as we have shown through our results how different coverage types and monitoring types can be utilized to verify various functional attributes of AMS systems.

Keywords: analog and mixed signal, coverage management, AMS simulation, cross-coverage, SystemVerilog

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

TASK 2810.020, ANALOG/MIXED-SIGNAL RF CIRCUIT TIME DOMAIN SENSITIVITY AND ITS APPLICATIONS

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SIGNIFICANCE AND OBJECTIVES

Efficiently and effectively model, detect and diagnose faults in Analog/Mixed-Signal/RF integrated circuits.

TECHNICAL APPROACH

As a function of time the overall power delivered to a circuit is equal to the algebraic sum of powers dissipated in all individual elements. Use perceived deviations in step function transient power (current) to indicate the presence and placement of open- and short-circuit faults.

SUMMARY OF RESULTS

If a circuit has n number of faults, present practice is to run n+1 circuit simulations, one for the nominal circuit and the other n with each fault “injected” separately. The aim of this research is employ time domain power transient sensitivity to replace such practice with one to three simulations.

The first four months of this research has produced an ultra fast step function simulator.

Preliminary work has begun on using the simulator to distinguish open- and short-circuit faults on an industry supplied benchmark suite of analog and mixed-signal integrated circuits.

Keywords: Power, Sensitivity, Faults, Open-short

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

TASK 2810.024, DEVELOPMENT AND ASSESSMENT OF MACHINE LEARNING BASED ANALOG AND MIXED-SIGNAL VERIFICATION

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SIGNIFICANCE AND OBJECTIVES

Verification of analog/mixed-signal (AMS) circuits is a long-standing challenge with major bottlenecks such as lack of scalability and lack of guarantee for coverage. Machine learning (ML) may provide a promising solution to these challenges. However, the robustness of ML as it is applied to AMS verification is yet to be fully understood.

TECHNICAL APPROACH

While applying ML to AMS verification may provide a promising solution, the mathematical properties of machine learning algorithms are yet to be fully understood. Studies have demonstrated vulnerability of deep neural networks (DNN) with respect to adversarially chosen input examples. Imperceptible perturbations to inputs (adversarial examples) can lead to incorrect recognition of a DNN image classifier. It may be expected that for AMS verification similar unsoundness of ML may create unintended or even catastrophic outcomes such as escape of design errors. We examine the robustness of various ML models including DNNs by defining a new concept of *global adversarial attacks*.

SUMMARY OF RESULTS

As illustrated in Figure 1, there may exist two types of adversarial attacks: local vs. global. The ML research community focuses the first type where small perturbations around examples in a training dataset are considered to generate adversarial examples, which we refer to as *local*.

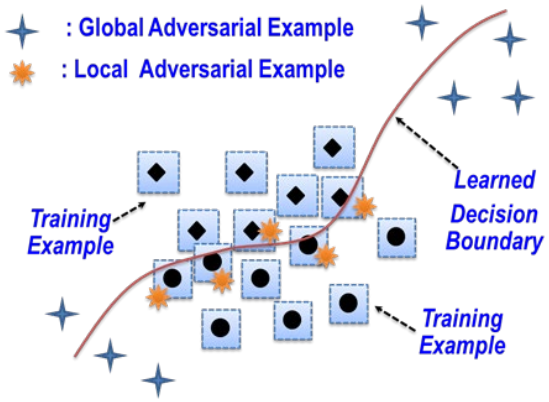

Figure 1. Global vs. local adversarial attacks.

Nevertheless, inputs far away from the training dataset may also cause mispredictions of a trained ML model. This type of global attacks are equally important, particularly for safety-critical applications such as autonomous driving where AMS ICs are deployed. We define such examples as *global adversarial examples*. We will investigate several techniques for evaluating global robustness and generating global adversarial examples for DNNs.

As a first step, we leverage the neural-network Gaussian process (NNGP) model as a bridge between Gaussian Processes (GP) and neural networks (NN). GPs have inherent model prediction uncertainty, which we use as an assessment of global robustness. It has been shown that fully-connected NNs with independent and identically distributed random parameters converge to a GP model (referred to as NNGP here) when the hidden layer width converges to infinity. As such the corresponding NNGP can be used to approximate the robustness of a fully-connected NN.

We train 3-layer NNs (with 1,024 hidden neurons) using 2,000 simulation data points to predict the specifications of an amplifier and an LDO. We use the NNGP model to generate 1,000 global adversarial examples with a large GP prediction variance to attack the NN model. Then, we identify two sets of inputs for which the NNGP model has small and large average variance (Ave. Var). We then assess the average NN error (MSE) with respect to the two sets of the inputs generated using the NNGP in Table 1. Clearly, the inputs with a large average NNGP variance lead to large errors of the NN, indicating the NNGP offers a meaningful assessment of the global robustness of the NN.

Table 1. Assessing Global DNN Robustness using a NNGP model surrogate.

Circuit	NNGP Ave. Var.	NN MSE
Amplifier	3.18E-7	1.37E-10
	6.10E-07	3.48E-10
LDO	6.83E-07	2.64E-08
	1.07E-06	4.17E-08

Keywords: Machine learning, analog and mixed-signal, deep neural networks, robustness, and adversarial attacks

INDUSTRY INTERACTIONS

Intel, Texas Instruments, NXP

MAJOR PAPERS/PATENTS

[1] H. Hu, P. Li, and J. Z. Huang, ""Enabling High-Dimensional Bayesian Optimization for Efficient Failure Detection of Analog and Mixed-Signal Circuits," IEEE/ACM DAC'19.

2810.026, LOW NOISE BALUN PRE-POWER AMPLIFIER

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SIGNIFICANCE AND OBJECTIVES

Off-chip passive baluns are widely used to interface external single-ended RF signals into the differential inputs of an integrated circuit. Such baluns are bulky and lossy. Here, we target an on-chip balun amplifier to overcome these issues and simultaneously achieving linearity and bandwidth performance on par with off-chip passive baluns.

TECHNICAL APPROACH

The technical approach is to address circuit limitations separately and combine suitable circuits at the transistor level. Technical strategies include source degeneration to increase linearity, stacking cascode transistors to achieve the high voltage swing, inductive gain peaking to increase bandwidth, and preliminary package selection to account for its effect on wideband and thermal performance of the balun amplifier. Since the applications include test and measurement equipment, direct RF sampling and wideband radar and sensing, an advanced technology node is chosen as a starting point.

SUMMARY OF RESULTS

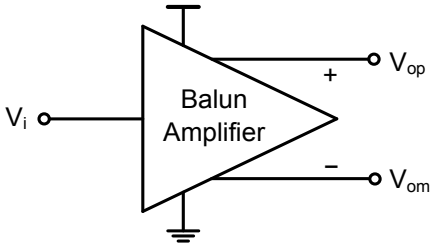

Figure 1. Conceptual diagram of a balun amplifier.

As stated earlier, in this balun amplifier design, linearity and wideband performance equivalent to that of an off-chip passive balun need to be achieved. In order to accomplish this, both feedforward and feedback based techniques can be pursued. Feedback techniques such as resistive degeneration are more robust to PVT variations compared to many feedforward techniques. Another challenge is the degradation of linearity at high frequencies due to parasitic effects. Appropriate compensation techniques need to be incorporated.

Using a 22-nm CMOS technology helps to achieve the high bandwidth. However, techniques such as inductive gain peaking may still be needed to compensate for the parasitic capacitances from transistors and bond pads. Similarly, chip-to-PCB-interface related parasitics such as bondwire inductance, leadframe inductance and capacitance and PCB parasitics can degrade the bandwidth. Hence, the package needs to be chosen in advance and its parasitics should be incorporated in simulations during the design.

Additionally, the package choice will be limited by the required thermal performance since the chip may need to dissipate high power to achieve necessary specifications. MMIC, chip on PCB, short-wire-bond based QFN, wafer-probe measurement may be some of the options which can achieve both high frequency and thermal performance.

Other specifications such as low noise and a hgh output voltage swing are also need to be supported. From an architectural point of view, the noise-canceling LNA is an interesting architectures that can be used to achieve low noise and good input matching. In other balun amplifier topologies noise can be reduced by dissipating more power in the circuit in general. However, the effects on power consumption and thermal performance of the balun amplifier need to be taken into account.

The balun amplifier also has RF PA-like requirements. It needs to achieve power gain and high voltage swing which is not possible with a passive balun. Most applications, especially the ones such as direct RF sampling benefit from power gain and high voltage swing. However, minimum length transistors in 22-nm processes may have gate-oxide-integrity issues with a high voltage swing at the output. Stacking cascode transistors can help to distribute the voltage swing in such cases.

Keywords: balun amplifier, direct RF sampling, Noise-canceling, stacking cascode, wideband.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

APPENDIX I PUBLICATIONS OF TXACE RESEARCHERS

Conference Publications

[1] Kang, W. and Ma, D. B. (2018). State-of-the-Art Monolithic Switched-Capacitor Voltage Regulators for Ultra-Low Power Internet of Things. *International Conference on Solid-State and Intergrated Circuit Technology, Qingdao, China*, **pp**. 1-4, IEEE.

[2] Abasalipour, A., Kumar, V., Ramezany, A. and Pourkamali, S. (2018). Thermal Piezoresistive Resonant Mass Balance Implemented in a Standard CMOS Process. *International Frequency Control Symposium, Olympic Valley, CA*, **pp**. 1-4, IEEE.

[3] Kumar, V., Abbasalipour, A., Ramezany, A. and Pourkamali, S. (2018). A Low-Power CMOS-MEMS Vibration Spectrum Analyzer. *International Frequency Control Symposium, Olympic Valley, CA*, **pp**. 1-4, IEEE.

[4] Chekuri, V., Singh, A., Dasari, N. and Mukhopadhyay, S. (2019). On the Effect of NBTI Induced Aging of Power Stage on the Transient Performance of On-Chip Voltage Regulators. *International Reliability Physics Symposium, Monterey, CA*, **pp**. 1-5, IEEE.

[5] Ince, M., Yilmaz, E. and Ozev, S. (2018). Enabling fast process variation and fault simulation through macromodelling of analog components. *North Atlantic Test Workshop, Essex, VT,* **pp**. 1-6, IEEE.

[6] Shafiee, M., Kitchen, J.N. and Ozev, S. (2018). A built-in self-test technique for transmitter-only systems. *VLSI Test Symposium, San Francisco, CA*, **pp**. 1-6, IEEE.

[7] Hu, H. and Li, P. (2018). A hybrid verification framework for analog and mixed-signal circuits. *SRC Techcon, Austin, TX*.

[8] Hu, H., Li, P. and Huang, J.Z. (2018). Parallelizable Bayesian Optimization for Analog and Mixed-Signal Rare Failure Detection with High Coverage. *International Conference on Computer-Aided Design, San Diego, CA*, **pp**. 1-8, ACM/IEEE.

[9] Hu, H., Zheng, Q., Wang, Y. and Li, P. (2018). HFMV: Hybridizing Formal Methods and Machine Learning for verification of analog and mixed-signal circuits. *Design Automation Conference, San Francisco, CA*, **pp**. 95.1-95.6, ACM/IEEE.

[10] Muldrey, B., Banerjee, S. and Chatterjee, A. (2019). Mixed Signal Design Validation Using Reinforcement Learning Guided Stimulus Generation for Behavior Discovery. *VLSI Test Symposium, Monterey, CA*, **pp**. 1-6, IEEE.

[11] Sun, X., Boora, A.,Zhang, W., Pamula, V. R. and Sathe, V. (2019). 14.5 A 0.6-to-1.1V Computationally Regulated Digital LDO with 2.79-Cycle Mean Settling Time and Autonomous Runtime Gain Tracking in 65nm CMOS. *International Solid- State Circuits Conference, San Francisco, CA*, **pp**. 230-232, IEEE.

[12] Lu, J., Zheng, B. and Flynn, M. (2019). A 50MHz-Bandwidth 70.4dB-SNDR Calibration-Free Time-Interleaved 4th-Order Noise-Shaping SAR ADC. *International Solid-State Circuits Conference, San Francisco, CA*, **pp**. 332-334, IEEE.

[13] Chaubey, S. and Harjani, R. (2018). A Zero Ripple Digital LDO with 0.6V Minimum Input Voltage, 200X Load Range and 98.7% Current Efficiency. *SRC TechCon, Austin, TX*.

[14] Chaubey, S. and Harjani, R. (2019). A Multi-Mode DC-DC Converter for Direct Battery-to-Silicon High Tension Power Delivery in 65nm CMOS. *Custom Integrated Circuits Conference, Austin, TX*, **pp**. 1-4, IEEE.

[15] Kim, D., Choi, W.S., Elkholy, A., Kenney, J. and Hanumolu, P. (2018). A 15Gb/s 1.9pJ/bit sub-baud-rate digital CDR. *Custom Integrated Circuits Conference, San Diego, CA*, **pp**. 1-4, IEEE.

[16] Hu, H., Lee, C., Elshater, A., Dai, Z., Ye, F. and Moon, U. (2019). Simultaneous STF and NTF Estimation in CTΔΣ Modulators with ARMA-Model. *International Symposium on Circuits and Systems, Sapporo, Japan,* **pp**. 1-5, IEEE.

[17] Lee, C., Venkatachala, P.K., ElShater, A., Xiao, B., Hu, H. and Moon, U. (2019). Application of Ring-Amplifiers for Low-Power Wide-Bandwidth Digital Subsampling ADC-PLL. *International Symposium on Circuits and Systems, Sapporo, Japan*, **pp**. 1-5, IEEE.

[18] Lee, C., Venkatachala, P.K., ElShater, A., Xiao, B., Hu, H. and Moon, U. (2019). Cascoded Ring Amplifiers for High Speed and High Accuracy Settling*. International Symposium on Circuits and Systems, Sapporo, Japan,* **pp**. 1-5, IEEE.

[19] Leuenberger, S., Venkatachala, P., ElShater, A., Lee, C., Oatman, M., Muhlestein, J., Xiao, B. and Moon, U. (2018). Passive Compensation for Improved Settling and Large Signal Stabilization of Ring Amplifiers. *International Symposium on Circuits and Systems, Florence, Italy*, **pp**. 1-5, IEEE.

[20] Leuenberger, S., Venkatachala, P., ElShater, A., Lee, C., Oatman, M., Xiao, B. and Moon, U. (2018). An Empirical Study of the Settling Behavior of Ring Amplifiers for Pipeline ADCs. *International Symposium on Circuits and Systems, Florence, Italy*, **pp**. 1-5, IEEE.

[21] Leuenberger, S., Venkatachala, P., ElShater, A., Lee, C., Oatman, M., Xiao, B., Xu, Y. and Moon, U. (2018). Process Invariant Biasing of Ring Amplifiers Using Deadzone Regulation Circuit. *International Symposium on Circuits and Systems, Florence, Italy*, **pp**. 1-5, IEEE.

[22] Liu, N., Geiger, R.L. and Chen, D. (2018). Silicon Bandgap Voltage VGO Extraction for Designing Sub-ppm/℃ Voltage References. *SRC Techcon, Austin, TX*.

[23] Kim, D. and Seok, M. (2018). Better-Than-Worst-Case Design Methodology for a Compact Integrated Switched-Capacitor DC-DC Converter. *International Symposium on Low Power Electronics and Design, Seattle, Washington,* **pp**. 261-266, ACM/IEEE.

[24] Li, J., Chundi, P. K., Kim, S., Jiang, Z., Yang, M., Kang, J., Jung, S., Kim, S.J. and Seok, M. (2018). A 0.78-µW 96-Ch. Deep Sub-Vt Neural Spike Processor Integrated with a Nanowatt Power Management Unit. *European Solid State Circuits Conference, Dresden, Germany*, **pp**. 154-157, IEEE.

[25] Han, C., Kim, T. and Maghari, N. (2018). A continuous-time delta-sigma modulator with self-ELD compensated quantizer. *Custom Integrated Circuits Conference, San Diego, CA*, **pp**. 1-4, IEEE.

[26] Boselli, G., Sankaralingam, R. and Chen, Z. (2018). Study of Voltage Overshooting of Gate-Coupled Silicon Controlled Rectifier on HBM Protection. *Electrical Overstress/Electrostatic Discharge Symposium, Reno, NV*, **pp**. 1-8, IEEE.

[27] Ren, Z., Alqahtani, A., Bagherzadeh, N. and Lee, J. (2018). Thermal Analysis of 3D ICs with TSVs using System Level Simulations. *SRC Techcon, Austin, TX*.

[28] Pande, N., Park, G., Krishnan, S., Reddy, V. and Kim, C. (2019). Investigating the Aging Dynamics of Diode-connected MOS Devices using an Array-based Characterization Vehicle in a 65nm Process. *International Reliability Physics Symposium, Montery, CA*, **pp**. 1-6, IEEE.

[29] Park, G., Kim, M., Pande, N., Chiu, P., Song, J. and Kim, C. (2019). A Counter based ADC Non-linearity Measurement Circuit and Its Application to Reliability Testing. *Custom Integrated Circuits Conference, Austin, TX,* **pp**. 1-4, IEEE.

[30] Tulsiram, A. and Eisenstadt, W. (2018). Development of LDO Testing and Fault Detection for Ultra Low Defects. *North Atlantic Test Workshop, Essex, VT*, **pp**. 1-5, IEEE.

[31] Tulsiram, A. and Eisenstadt, W. (2018). Test Techniques to Approach Several Defect-Per-Billion. *SRC Techcon, Austin, TX.*

[32] Krishnan, A. and Schaumont, P. (2018). Exploiting Security Vulnerabilities in Intermittent Computing. *International Conference on Security, Privacy and Applied Cryptography Engineering, Kanpur, India,* **pp**. 104-124, Springer.

[33] Krishnan, A., Suslowicz, C., Dinu, D. and Schaumont, P. (2019). Secure Intermittent Computing Protocol: Protecting State across Power Loss. *Design Automation and Test in Europe, Florence, Italy,* **pp**. 734-739, IEEE.

[34] Chandrasekaran, S. T. and Sanyal, A. (2018). A Digital PLL Based 2nd-Order ΔΣ Bandpass Time-Interleaved ADC. *International Midwest Symposium on Circuits and Systems, ON, Canada*, **pp**. 286-289, IEEE.

[35] Danesh, M., Chandrasekaran, S. T. and Sanyal, A. (2018). Ring Oscillator Based Delta-Sigma ADCs. *International Conference on Electronics, Circuits and Systems, Bordeaux, France*, **pp**. 113-116, IEEE.

[36] Votzke, C., Daalkhaijav, U., Mengüç, Y. and Johnston, M.L. (2018). Highly-Stretchable Biomechanical Strain Sensor using Printed Liquid Metal Paste. *Biomedical Circuits and Systems Conference, Cleveland, OH*, **pp**. 1-4, IEEE.

[37] Shylendra, A., Bhunia, S. and Trivedit, AR. (2019). An Intrinsic and Database-free Authentication by Exploiting Process Variation in Back-end Capacitors. *International Symposium on Low Power Electronics and Design, Seattle, WA,* **pp**. 44.1-44.6, ACM/IEEE.

[38] Sivapurapu, S., Mehta, C., Chen, R., Jia, X., Zhou, Y., Bellaredj, M., Kohl, P., Huang, T.C., Sitaraman, S. and Swaminathan, M. (2018). Multi-physics Modeling Characterization of Aerosol Jet Printed Transmission Lines. *MTT-S International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization, Reykjavik, Iceland,* **pp**. 1-4, IEEE.

[39] Sivapurapus, S., Mehta, C., Chen, R., Zhou, Y., Jia, X., Bellaredj, M., Kohl, P., Huang, T., Sitaraman, S. K. and Swaminathan, M. (2018). Model Development for Inductors on Flexible Substrates for Integrated Power Delivery Applications. *SRC Techcon, Austin, TX*.

[40] Momson, I., Dong, S., Yelleswarapu, P. and O, K. K. (2018). 300-GHz MSK Receiver for Communication over a Dielectric Waveguide. *SRC Techcon, Austin, TX*.

[41] Yang, F., Ugur, E., Pu, S. and Akin, B. (2019). Design of a High-Performance DC Power Cycling Test Setup for SiC MOSFETs. *Applied Power Electronics Conference and Exposition, Anaheim, CA*, **pp**. 1390-1396, IEEE.

[42] Yang, F., Ugur, E., Pu, S., Xu, C. and Akin, B. (2019). Thermally Triggered SiC MOSFET Aging Effect on Conducted EMI. *Wide Bandgap Power Devices and Applications, Atlanta, GA*, **pp**. 51-55, IEEE.

[43] Yan, D., Ke, X. and Ma, D.B. (2018). Integrated Single-Stage Bi-directional UPS with One-Cycle Mode Switching and Active Deadtime Control for Automotive Electronics. *Energy and Conversion Congress and Exposition, Portland, OR*, **pp**. 2081-2085, IEEE.

[44] Yanik, M and Torlak, M. (2018). Milimeter- Wave near Field Imaging with Two-Dimensional SAR Data. *SRC Techcon, Austin, TX*.

[45] Yanik, M. and Torlak, M. (2019). Near-Field 2-D SAR Imaging by Millimeter-Wave Radar for Concealed Item Detection. *Radio and Wireless Symposium, Orlando, FL,* **pp**. 1-4, IEEE.

[46] Xanthopoulos, C., Neethirajan, D., Boddikurapati, S., Nahar, A. and Makris, Y. (2019). Wafer-Level Adaptive Vmin Calibration Seed Forecasting. *Design, Automation & Test in Europe Conference & Exhibition, Florence, Italy,* **pp**. 1673-1678, IEEE.

[47] Singh, A., Kar, M., Mathew, S., Rajan, A., De, V. and Mukhopadhyay, S. (2019). A 128b AES Engine with Higher Resistance to Power and Electromagnetic Side-Channel Attacks Enabled by a Security-Aware Integrated All-Digital Low-Dropout Regulator. *International Solid- State Circuits Conference, San Francisco, CA*, **pp**. 404-406, IEEE.

[48] Singh, A., Kar, N., Chawla, N. and Mukhopadhyay, S. (2019). Mitigating Power Supply Glitch based Fault Attacks with Fast All-Digital Clock Modulation Circuit. *Design, Automation & Test in Europe Conference & Exhibition, Florence, Italy*, **pp**. 19-24, IEEE.

[49] Zou, A., Leng, J., He, X., Zu, Y., Gill, C., Reddi, V. and Zhang, X. (2018). Voltage-Stacked GPUs: A Control Theory Driven Cross-Layer Solution for Practical Voltage Stacking in GPUs. *International Symposium on Microarchitectur, Fukuoka, Japan*, **pp**. 390-402, ACM/IEEE.

[50] Zou, A., Leng, J., He, X., Zu, Y., Reddi, V. and Zhang, X. (2018). Efficient and Reliable Power Delivery in Voltage-Stacked Manycore System with Hybrid Charge-Recycling Regulators. *Design Automation Conference, San Francisco, CA,* **pp**. 1-6, ACM/ESDA/IEEE.

[51] Chen, Y. and Ma, D. B. (2019). An 8.3MHz GaN power converter using Markov continuous RSSM for 35dBμV conducted EMI attenuation and one-cycle TON rebalancing for 27.6dB VO jittering suppression. *International Solid-State Circuits Conference, San Francisco, CA,* **pp**. 250-252, IEEE.

[52] Zhang, L., Ameri, A., Li, Y., Kuo, N., Anwar, M. and Niknejad, A. (2018). A 37.5-45. lGHz Superharmonic-Coupled QVCO with Tunable Phase Accuracy in 28nm Bulk CMOS. *Asian Solid-State Circuits Conference, Tainan, Taiwan,* **pp**. 223-226, IEEE.

[53] Esmaeelzadeh, H. and Pamarti, S. (2019). 18.4 A 0.55nW/0.5V 32kHz Crystal Oscillator Based on a DC-Only Sustaining Amplifier for IoT. *International Solid-State Circuits Conference, San Francisco, CA,* **pp**. 300-301, IEEE.

[54] Shi, L., Zhang, Y., Wang, Y., Kareppagoudr, M., Sadollahi, M. and Temes, G. (2018). A 13b ENOB Noise Shaping SAR ADC with a Two-Capacitor DAC. *International Midwest Symposium on Circuits and Systems. Ontario, Canada*, **pp**. 153-156, IEEE.

[55] Jha, S. and Busso, C. (2018). FI-CAP: Robust Framework to Benchmark Head Pose Estimation in Challenging Environments. *International Conference on Multimedia and Expo, San Diego, CA*, **pp**. 1-6, IEEE.

[56] Jha, S. and Busso, C. (2018). Probabilistic Estimation of the Gaze Region of the Driver using Dense Classification. *International Conference on Intelligent Transportation Systems, Maui, HI*, **pp**. 697-702, IEEE.

[57] Aflakian, N., Gomez, M., Miller, C., Henderson, R., MacFarlane, D. and O, K. K. (2019). Functional Performance of a Millimeter Wave Square Holey Dielectric Waveguide. *Radio and Wireless Symposium, Orlando, FL,* **pp**. 1-4. IEEE.

[58] Zhong, Q., Choi, W. and O, K. K. (2018). Terahertz RF Front-End Employing Even-Order Subharmonic MOS Symmetric Varactor Mixers in 65-NM CMOS for Hydration Measurements at 560 GHz. *Symposium on Very Large Scale integration Circuits, Honolulu, HI*, **pp**. 211-212, IEEE.

Journal Publications

[1] Erol, O.E. and Ozev, S. (2019). Knowledge-and Simulation-Based Synthesis of Area-Efficient Passive Loop Filter Incremental Zoom-ADC for Built-In Self-Test Applications. *ACM Transactions on Design Automation of Electronic Systems (TODAES),* **vol**. 24, **no**. 1, **art**. 3.

[2] Jeong, J.W., Kitchen, J. and Ozev, S. (2019). On-Chip RF Phased Array Characterization with DC-Only Measurements for In-field Calibration. *IEEE Design and Test*, **vol**. 36, **no**. 3, **pp**. 117-125

[3] Kim, D., Choi, W.S., Elkholy, A., Kenney, J. and Hanumolu, P. (2018). A 15Gb/s 1.9pJ/bit sub-baud-rate digital CDR. *IEEE Custom Integrated Circuits Conference*, **vol**. 54, **no**. 3, **pp**. 685-695.

[4] Kim, S., Cerqueira, J. and Seok, M. (2019). A Near-Threshold Spiking Neural Network Accelerator With a Body-Swapping-Based In Situ Error Detection and Correction Technique. *IEEE Transactions on Very Large Scale Integration Systems,* **vol**. 27, **no**. 8, **pp**. 1886-1896.

[5] Kim, S., Kim, D., Ham, H., Kim, J. and Seok, M. (2018). A 67.1-ps FOM, 0.5-V-Hybrid Digital LDO With Asynchronous Feedforward Control Via Slope Detection and Synchronous PI With State-Based Hysteresis Clock Switching. *IEEE Solid-State Circuits Letters*, **vol**. 1 , **no**. 5, **pp**. 130-133.

[6] Alqahtani, A., Ren, Z., Lee, J. and Bagherzadeh, N. (2018). System-Level Analysis of 3D ICs with Thermal TSVs. *ACM Journal on Emerging Technologies in Computing Systems,* **vol**. 14, **no**. 37, **pp**. 37.1-37.16.

[7] Chandrasekaran, S. T., Jayaraj, A., Danesh, M. and Sanyal, A. (2018). A Highly Digital Second-Order Oversampling TDC. *IEEE Solid-State Circuits Letters*, **vol**. 1, **no**. 5, **pp**. 114-117.

[8] Jayaraj, A., Danesh, M., Chandrasekaran, S. T. and Sanyal, A. (2019). Highly Digital Second-Order ΔΣ VCO ADC. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **vol**. 66, **no**. 7, **pp**. 2415-2425.

[9] Votzke, C., Daalkhaijav, U., Mengüç, Y. and Johnston, M.L. (2019). 3D-Printed Liquid Metal Interconnects for Stretchable Electronics*. IEEE Sensors Journal*, **vol**. 19, **no**. 10, **pp**. 3832-3840.

[10] Shylendra, A., Bhunia, S. and Trivedit, A.R. (2019). An Intrinsic and Database-free Authentication by Exploiting Process Variation in Back-end Capacitors. *IEEE Transactions on Very Large Scale Integration Systems*, **vol**. 27, **no**. 6, **pp**. 1253-1261.

[11] Ugur, E., Dusmez, S. and Akin, B. (2018). An Investigation on Diagnosis-Based Power Switch Lifetime Extension Strategies for Three-Phase Inverters. *IEEE Transactions on Industry Applications*, **vol**. 55, **no**. 2, **pp**. 2064-2075.

[12] Ugur, E., Yang, F., Pu, S., Zhao, S. and Akin, B. (2019). Degradation Assessment and Precursor Identification for SiC MOSFETs Under High Temp Cycling. *IEEE Transactions on Industry Applications,* **vol**. 55, **no**. 3, **pp**. 2858-2867.

[13] Xu, C., Yang, F., Ugur, E., Pu, S. and Akin, B. (2018). Performance degradation of GaN HEMTs under accelerated power cycling tests. *CPSS Transactions on Power Electronics and Applications*, **vol**. 3, **no**. 4, **pp**. 269-277.

[14] Baral, A. and Torlak, M. (2019). Impact of Number of Noise Eigenvectors Used on the Resolution Probability of MUSIC. *IEEE Access,* **vol**. 7, **pp**. 20023-20039.

[15] Yanik, M. and Torlak, M. (2019). Near-Field MIMO-SAR Millimeter-Wave Imaging With Sparsely Sampled Aperture Data. *IEEE Access*, **vol**. 7, **pp**. 31801-31819.

[16] Bhide, A., Jagannath, B., Willis, R., Graef, E. and Prasad, S. (2018). Versatile Duplex Electrochemical Sensor for the Detection of CO2 and Relative Humidity Using Room Temperature Ionic Liquid. *Electrochemical Society Transactions*, **vol**. 85, **no**. 13, **pp**. 751-765.

[17] Singh, A., Kar, M., Mathew, S.K., Rajan, A., De, V. and Mukhopadhyay, S. (2019). Improved Power/EM Side-Channel Attack Resistance of 128-Bit AES Engines With Random Fast Voltage Dithering. *IEEE Journal of Solid-State Circuits,* **vol**. 54, **no**. 2, **pp**. 569-583.

[18] Xiu, Y., Thomson, N. and Rosenbaum, E. (2019). Measurement and Simulation of On-Chip Supply Noise Induced by System-Level ESD. *IEEE Transactions on Device and Materials Reliability*, **vol**. 19, **no**. 1, **pp**. 211-220.

[19] Sun, K., Wang, G., Zhang, Q., Elahmadi, S. and Gui, P. (2019). A 56-GS/s 8-bit Time-Interleaved ADC With ENOB and BW Enhancement Techniques in 28-nm CMOS. *IEEE Journal of Solid-State Circuits,* **vol**. 54, **no**. 3, **pp**. 821-833.

[20] Wang, G., Sun, K., Zhang, Q., Elahmadi S. and Gui, P. (2019). A 43.6-dB SNDR 1-GS/s 3.2-mW SAR ADC With Background-Calibrated Fine and Coarse Comparators in 28-nm CMOS. *IEEE Transactions on Very Large Scale Integration Systems,* **vol**. 27, **no**. 9, **pp**. 1998-2007.

[21] Heydarzadeh, M., Zafarani, M., Nourani, M. and Akin, B. (2018). A Wavelet-Based Fault Diagnosis Approach for Permanent Magnet Synchronous Motors*. IEEE Transactions on Energy Conversion*, **vol**. 34, **no**. 2, **pp**. 761-772.

[22] Qi, Y., Zafarani, M., Bostanci, E. and Akin, B. (2018). Severity Estimation of Interturn Short Circuit Fault for PMSM. *IEEE Transactions on Industrial Electronics*, **vol**. 66, **no**. 9, **pp**. 7260-7269.

[23] Qi, Y., Zafarani, M., Gurusamy, V. and Akin, B. (2019). Advanced Severity Monitoring of Interturn Short Circuit Faults in PMSMs. *IEEE Transactions on Transportation Electrification*, **vol**. 5, **no**. 2, **pp**. 395-404.

Books and Chapters

[1] Lin H., Khan A., Li P. (2019) Sparse Relevance Kernel Machine-Based Performance Dependency Analysis of Analog and Mixed-Signal Circuits. In: Elfadel I., Boning D., Li X. (eds) Machine Learning in VLSI Computer-Aided Design. Springer, Cham

[2] Bhunia, S. and Tehranipoor, M. (2018) Hardware Security: A Hands-on Learning Approach. San Francisco, CA: Elsevier Science & Technology

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