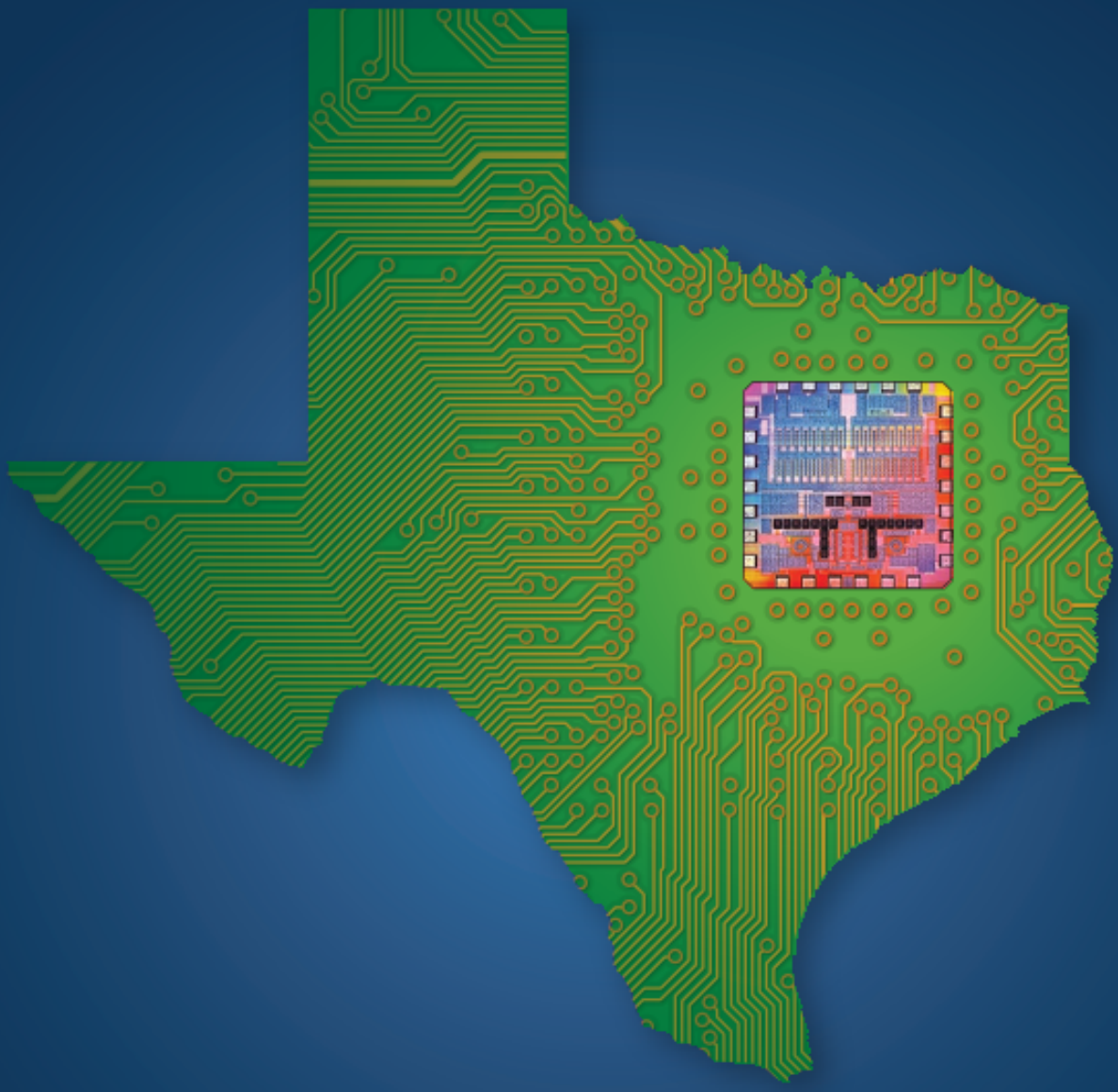


TEXAS ANALOG CENTER OF EXCELLENCE

Annual Report 2014 – 2015

SRC®

TxACE
TEXAS ANALOG
CENTER OF EXCELLENCE

TxACE MISSION

The Texas Analog Center of Excellence seeks to create fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, health care, and public safety and security.

TxACE THRUSTS

- *Safety & Security*
- *Health Care*
- *Energy Efficiency*
- *Fundamental Analog Circuits*

TxACE 2014-2015 ANNUAL REPORT

The Texas Analog Center of Excellence (TxACE), located at the University of Texas at Dallas is the largest analog research center based in an academic institution. Analog and mixed signal integrated circuits engineering is both a major opportunity and challenge. Analog circuitry is emerging as a critical component of nearly every product of the ~$350 billion per year integrated circuits industry, as a part of sensing, actuation, communication, power management and others. Digital integrated circuits such as microprocessors, logic circuits and memories are now integrating analog functions such as input/output circuits, phase locked loops, temperature sensors and power management circuits. It is also common to find microcontrollers with multiple analog-to-digital and digital-to-analog converters. These circuitries impact almost all aspect of modern life: safety and security, health care, transportation, energy, entertainment and many others.

The increasing importance of analog integrated circuits in electronic systems and the emergence of new applications are providing an exciting opportunity. However, the inherent difficulty of the art makes it challenging. Creation of advanced wireless technology and sophisticated sensing and imaging devices depends on the availability of engineering talent for analog research and development. TxACE was established to help translate these opportunities into economic benefits by overcoming the challenge and meeting the need. Support for TxACE has been provided through a collaboration of the state of Texas, Texas Instruments, the Semiconductor Research Corporation, the University of Texas System, and the University of Texas at Dallas.

The research tasks are organized into four research thrust areas: Health Care, Safety and Security, Energy Efficiency and Fundamental Analog. The scope of investigation extends from circuits operating at dc through terahertz, data converters that sample at a few samples/sec to 10's of Giga-samples/sec, ac-to-dc and dc-to-dc converters working at µW to Watts, energy harvesting circuits, protein and DNA sensors and many more. Significant improvement on existing mixed signal systems and new applications are anticipated. Students who have been exposed to hands-on innovative research are forming the leading edge of analog talent flow into the industry. Close collaboration with and responsiveness to industry needs provide focus to the educational experience.

DIRECTOR'S MESSAGE

The Texas Analog Center of Excellence (TxACE) is leading analog research and education. Last year, TxACE researchers published 20 journal and 136 conference papers. They also filed four patent applications. Twenty-two Ph.D. and eighteen M.S. students of TxACE have graduated.

During this period, the Center funded 70 research tasks led by 48 principal investigators from 23 academic institutions, including four international universities. Five universities (SMU, Rice, Texas A&M, UT Austin, UT Dallas) were from the state of Texas. The Center supported 148 graduate and undergraduate students.

The Center accomplished much. There are too many to list all here. A selected list includes demonstrations of a fast power-on-lock LC-PLL with 1ns power-on time, built-in self-test techniques for dc-dc converters, room temperature operation of Quantum Well NMOS transistors fabricated in 45-nm CMOS, and fault diagnosis and identification of permanent magnet motors using fluxgate sensors.

The TxACE laboratory is continuing to help advancing integrated circuit research by making its instruments available to researchers all over the world. The integrated circuits fabrication program is well subscribed and is expanding.

I would like to thank the students, principal investigators and staff for their efforts, and the UT Dallas, the University of Texas System, TI, and SRC, as well as many friends of TxACE all over the world for their generous support. I look forward to another year of working with the TxACE team to make difference in our world through our research, education and innovation.

Kenneth K. O, Director TxACE
Texas Instruments Distinguished Chair Professor
The University of Texas at Dallas

BACKGROUND & VISION

The $350 billion per year integrated circuits industry is evolving into an analog/digital mixed signal industry. Analog circuits are providing or supporting critical functions such as sensing, actuation, communication, power management and others. These circuits impact almost all aspect of modern life including safety and security, health care, transportation, energy, and entertainment. To lead this change, in particular to lead analog and mixed signal technology education, research, commercialization, manufacturing, and job creation, the Texas Analog Center of Excellence was announced by Texas Governor Rick Perry in October 2008 as a collaboration of the Semiconductor Research Corporation, the state of Texas through its Texas Emerging Technology Fund, Texas Instruments Inc., the University of Texas system and the University of Texas at Dallas. The Center seeks to accomplish the objectives by creating fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, healthcare, and public safety and security as well as by improving the research and educational infrastructure.

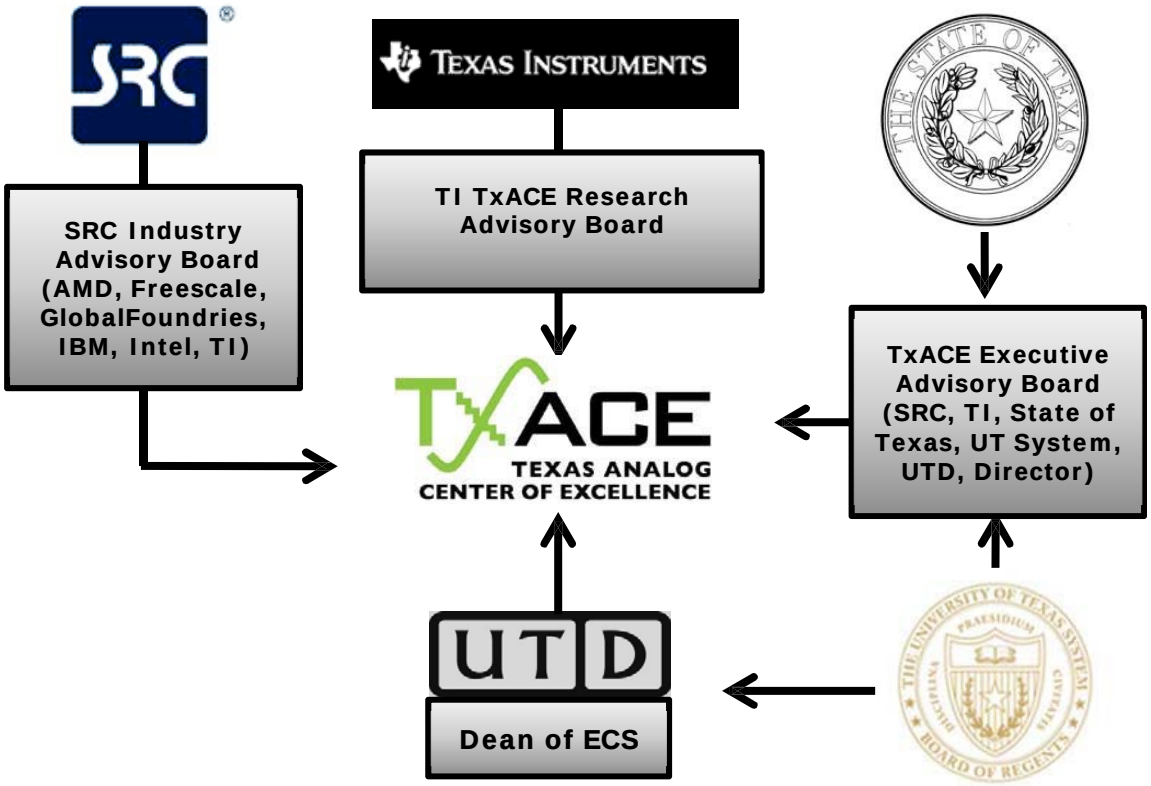


Figure 1: TxACE organization relative to the sponsoring collaboration

CENTER ORGANIZATION

The Texas Analog Center of Excellence is guided by agreements established with the Center sponsors. Members of the industrial advisory boards identify the research needs and select research tasks in consultation with the Center leadership. Figure 1 diagrams the relationship of TxACE to the members of the sponsoring collaboration.

The internal organization of the Center is structured to flexibly perform the research mission while not detracting from the educational missions of the University.

Figure 2 shows the elements of the organization. The TxACE Director is Professor Kenneth O. The research is arranged into four thrusts that comply with the mission of the Center: Safety and Security, Health Care, Energy Efficiency and Fundamental Analog Research. The fourth thrust consists of vital research that cuts across more than one of the first three research thrusts. The thrust leaders are Prof. Brian A. Floyd of North Carolina State University for safety and security, Prof. Yun Chiu of UT Dallas for health care, Prof. D. Ma of the UT Dallas for energy efficiency, and Prof. Ramesh Harjani of the University of Minnesota for fundamental analog research. The thrust leaders form the executive committee. The committee, along with the director, forms the leadership team that works to improve the research productivity of center by increasing collaboration, better leveraging the diverse capabilities of principle investigators of the Center, and lowering research barriers. The leadership team also identifies new research opportunities for consideration by the Industrial Advisory Boards.

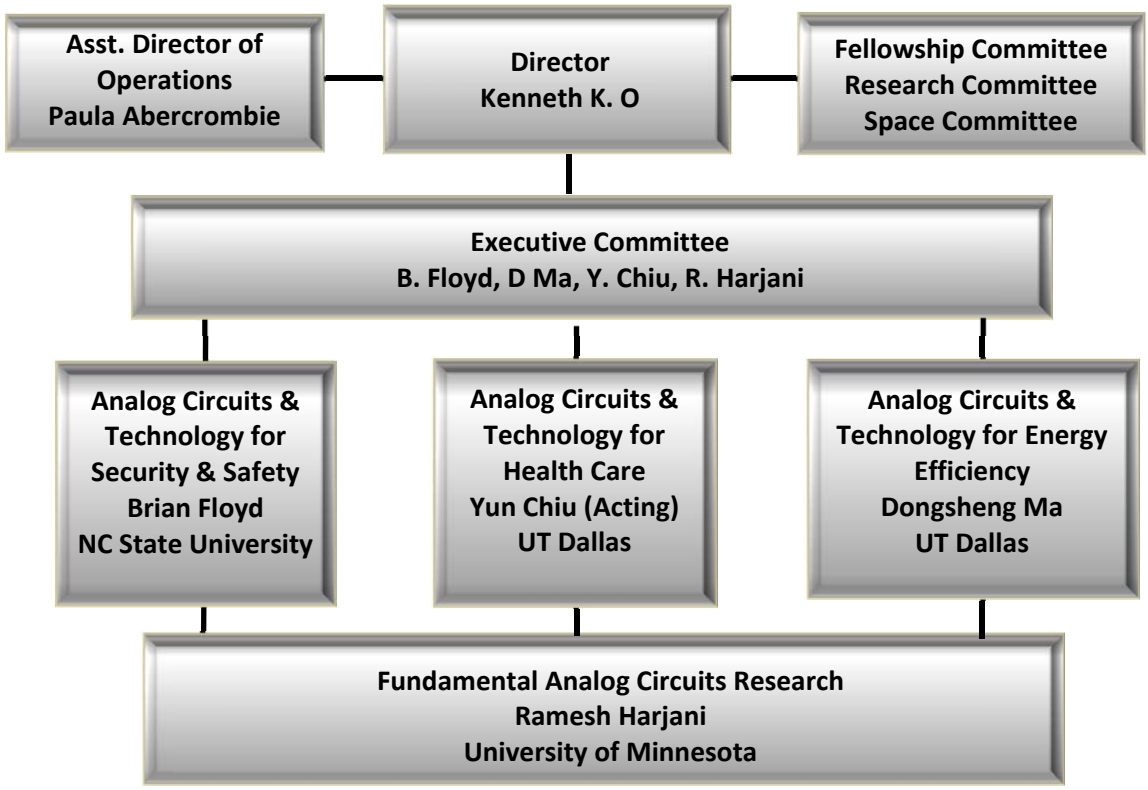


Figure 2: TxACE organization for management of research

PUBLIC SAFETY AND SECURITY

(Thrust leader: Brian Floyd, NC State University)

TxACE is developing analog technology that enhances public safety and security. The projects are intended to 1) enable a new generation of devices that can scan for harmful substances by researching 200-300 GHz silicon ICs for use in spectrometers, and 2) significantly reduce the cost of millimeter wave imaging and on-vehicle radar technology for automotive safety by researching circuit techniques that can improve manufacturing and simplify test and packaging, as well as signal processing techniques that reduce system complexity.

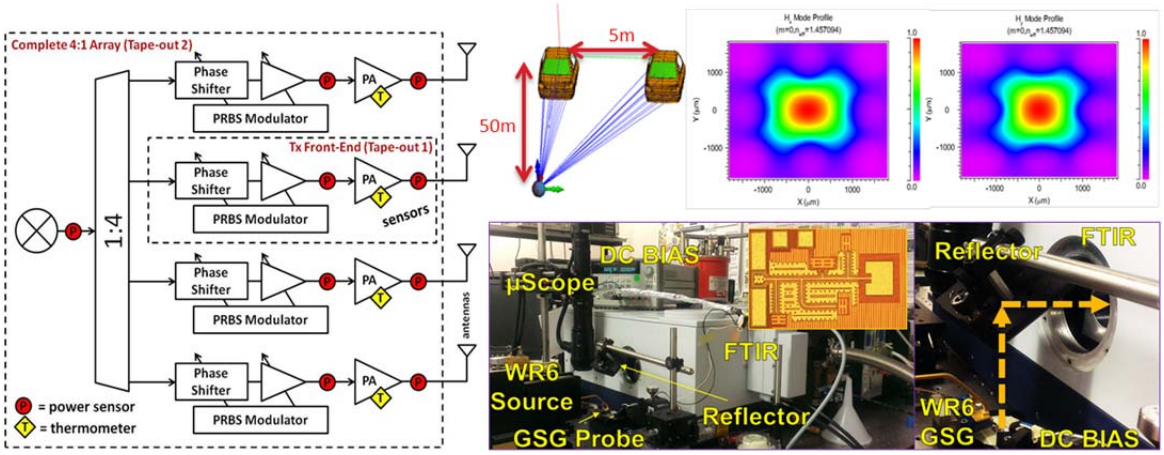


Figure 3: (Left) Efficient phased array testing (B. Floyd, NCSU), (Top middle) 3-D millimeter wave Imaging (Torlak, UT Dallas), (Top right) Dielectric waveguides for 300-Gbps communication (D. Macfarlane, UT Dallas), (Bottom right) 750-GHz signal generation circuit in CMOS and FTIR for spectrum analyses of the circuit (K. K. O and M. Lee, UT Dallas).

HEALTH CARE

(Thrust leader: Yun Chiu (Acting), University of Texas, Dallas)

Analog and RF integrated circuit technology is the essential interface enabling the power, speed and miniaturization of modern digital microelectronics to be brought to bear on an array of medical issues, including medical imaging, patient monitoring, laboratory analyses, bio-sensing and new therapeutic devices. TxACE is working to identify and support analog circuit research challenges that have the potential to enable important health-related applications. More specifically, TxACE is working to address the contact problem of EEG, to develop an affordable rotational spectrometer that can be used in breath analyses for health monitoring, and energy efficient radios for wearable wireless body area networks.

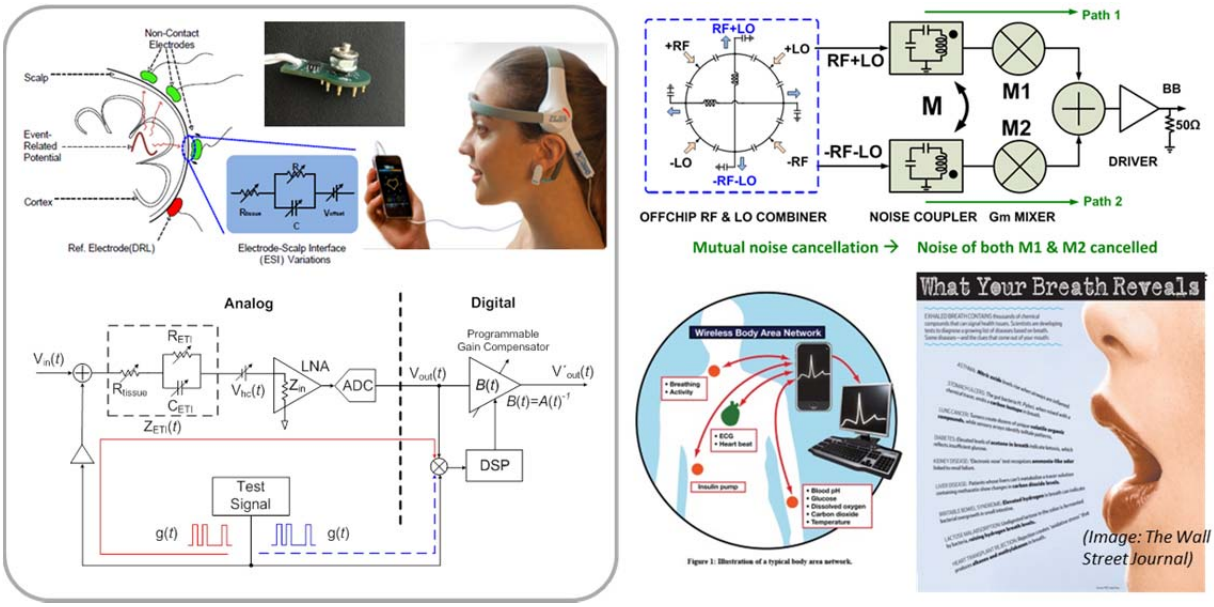


Figure 4: (Left) Adaptive electronics and signal processing for EEG (Y. Chiu and R. Jafari, UT, Dallas), (Top right) Receiver for wearable wireless body area networks (R. Harjani, U. of Minnesota), (Bottom right) Breath analyses using a rotational spectrometer (K. K. O, UT Dallas).

ENERGY EFFICIENCY

(Thrust leader: Dongsheng Brian Ma, UT Dallas)

TxACE is committed to alleviate the global energy problem by improving the energy efficiency of electronic systems as well as by developing analog technologies that can make energy generation and distribution more efficient. The Center is also working to energize and power long-lasting in-situ microscale devices such as wireless microsensors, biomedical implants, and portable microelectronics.

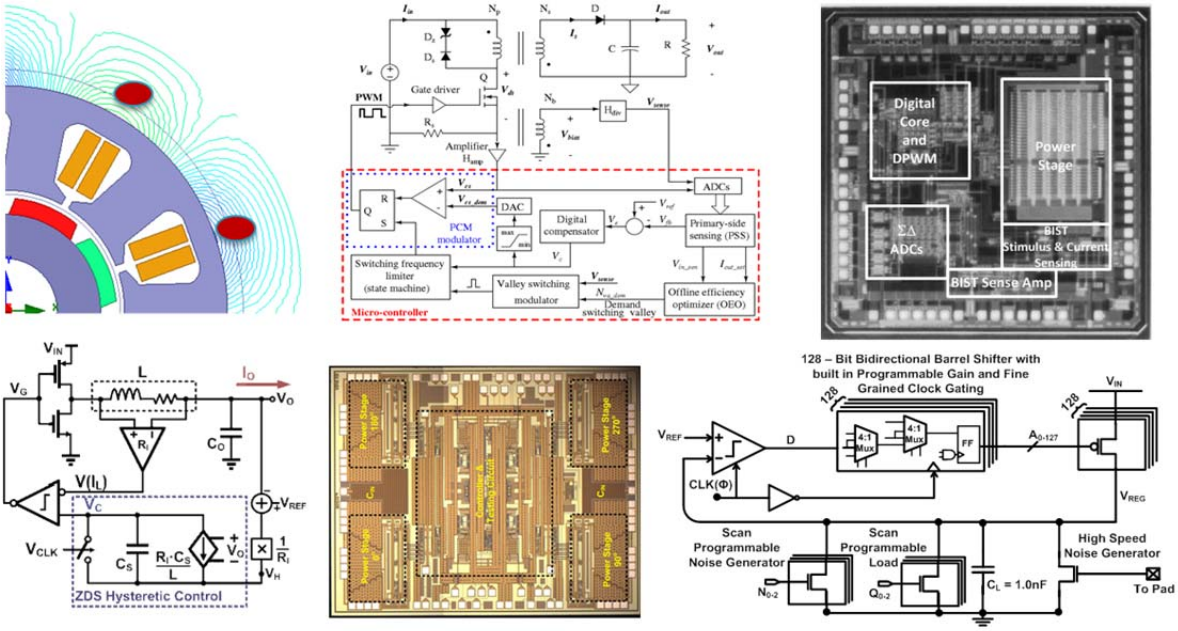


Figure 5: (Top left) Simulated flux leakage in a motor (B. Akin, UT Dallas), (Top center) flyback converter controlled by a microcontroller (J. Ringwood, Maynooth U.), (Top right) DC-DC converter incorporating built-in self test (S. Ozev and B. Bakkaloglu, ASU), (Bottom left) 6-A, 40-MHz Four-Phase ZDS Hysteretic DC-DC Converter with 118mV Droop and 230ns Response Time for a 5A/5ns Load Transient (D. Ma, UT Dallas), (Bottom, right) Digital Low-Dropout Regulator with wide dynamic range (A. Raychowdhury, GaTech).

FUNDAMENTAL ANALOG CIRCUITS RESEARCH

(Thrust leader: Ramesh Harjani, University of Minnesota)

Research in this thrust focuses on cross-cutting areas in Analog Circuits which impact all of the TxACE application areas (Energy Efficiency, Health Care, Public Safety and Security). The list of research includes design of a wide variety of analog-to-digital converters, communication links, temperature sensors and I/O circuits, development of CAD tools, and testing of integrated circuits.

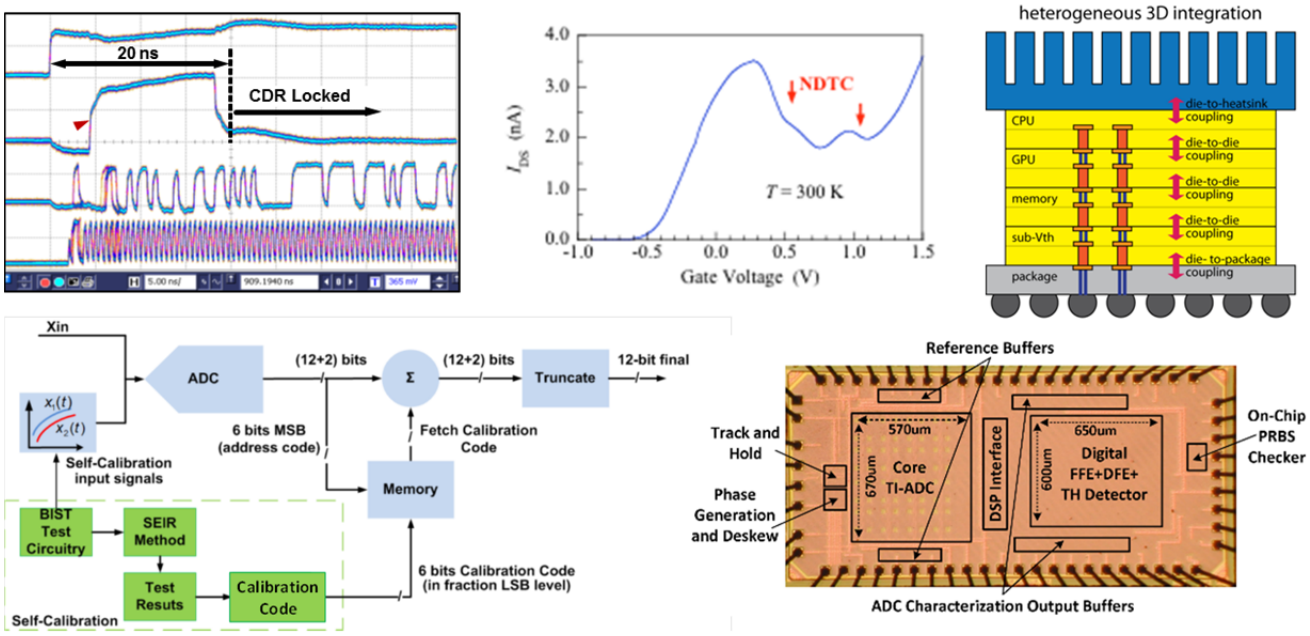


Figure 6: (Top left) 20-ns power-on time, energy-proportional links in 65nm CMOS (P. Hanumolu, UIUC) (Top center) I-V characterization of a resonant tunneling transistor in CMOS at room temperature (M. Lee, UT Dallas), (Top right) 3D integrated heterogeneous system (S. Mukhopadhyay, GaTech, (Bottom left) Built in self testing using an on-chip signal generator for analog-to-digital converter linearity (R. Geiger, Iowa State U.), (Bottom right) a hybrid ADC-based RX which combines equalization embedded in the ADC & dynamically-enabled digital equalization (S. Palermo, TAMU).

TXACE ANALOG RESEARCH FACILITY

The centralized group of laboratories of the Texas Analog Center of Excellence dedicated to analog engineering research and training occupies a ~8000 ft^2 area on the 3rd floor of the Engineering and Computer Science North building (Figure 7). The facility includes RF and THz, Integrated System Design, Embedded Signal Processing, and Analog & Mixed Signal laboratories as well as CAD/Design laboratory structured to promote collaborative research**.** The unique instrumentation capability includes network analyses and linearity measurements up to 325 GHz, spectrum analysis up to 120 THz, and cryo-measurements down to $2^{o}K$. The Center also added a pulsed multiple harmonic load and source pull measurement set up (up to 60 GHz for the third harmonic) and a 325 GHz antenna measurement set up. The close proximity of researchers in an open layout enables natural interaction and compels sharing of knowledge and instrumentation among the students and faculty. The TxACE analog research facility is one of the best equipped electronics laboratories. The laboratory is available for use by TxACE researchers all over the world.

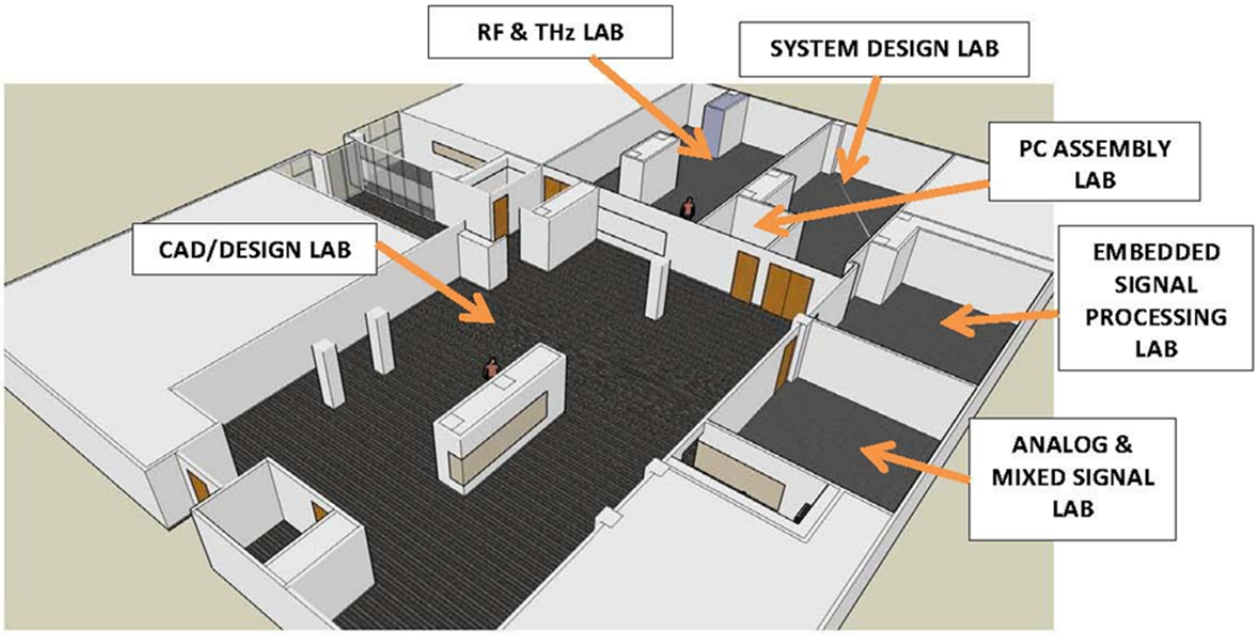


Figure 7: TxACE Analog Research Facility

RESEARCH PROJECTS AND INVESTIGATORS

The Texas Analog Center of Excellence (TxACE) is the largest university analog technology center in the world. Table 1 lists the current principal investigators of the 70 tasks from 23 academic institutions funded by TxACE. Five universities (Rice, SMU, Texas A&M, UT Austin, UT Dallas) are from the state of Texas. Eighteen are from outside of Texas. Four (Seoul National University, Korea; University of Cambridge, United Kingdom; National University of Ireland, Maynooth; and Technion – Israel Institute of Technology) (Figure 8) are from outside of the US. Of the 48 investigators, 19 are from Texas. During the past year, the Center supported 121 Ph.D., 26 M.S. and 1 B.S. students, and 22 Ph.D. and 18 M.S. degrees were awarded to the TxACE students.

Table 1: Principal Investigators (September 2014 through August 2015)

Investigator	Institution	Investigator	Institution	Investigator	Institution
N. Al-Dahir	UT Dallas	P. Hanumolu	UIUC	S. Mukhopadyay	Georgia Tech
B. Akin	UT Dallas	R. Harjani	U Minnesota	A. Niknejad	UC Berkeley
A. Babakhani	Rice U	R. Henderson	UT Dallas	B. Nikolic	UC Berkeley
B. Bakkaloglu	Arizona State	R. Jafari	UT Dallas	K. O	UT Dallas
D. Blaauw	U Michigan	B. Kim	CUNY	S. Ozev	Arizona State
D. Chen	Iowa State	J. Kim	Seoul Nat.	S. Palermo	Texas A&M
Y. Chiu	UT Dallas	P. Kinget	Columbia	S. Pourkamali	UT Dallas
W. Choi	UT Dallas	H. Lee	UT Dallas	A. Raychowdhury	Georgia Tech
F. De Lucia	Ohio State	M. Lee	UT Dallas	J. Ringwood	Nui Maynooth
J. Di	U Arkansas	P. Li	Texas A&M	E. Rosenbaum	UIUC
Y. Eldar	Technion	D. Ma	UT Dallas	J. Roychowdhury	UC Berkeley
B. Floyd	NC State	D. MacFarlane	UT Dallas	M. Saquib	UT Dallas
M. Flynn	U Michigan	Y. Makris	UT Dallas	R. Shi	U Washington
R. Geiger	Iowa State	H. A. Mantooth	U Arkansas	G. Temes	Oregon State
R. Gharpurey	UT Austin	R. McMahon	Cambridge	M. Torlak	UT Dallas
P. Gui	SMU	U.-K. Moon	Oregon State	D. Wentzloff	U Michigan

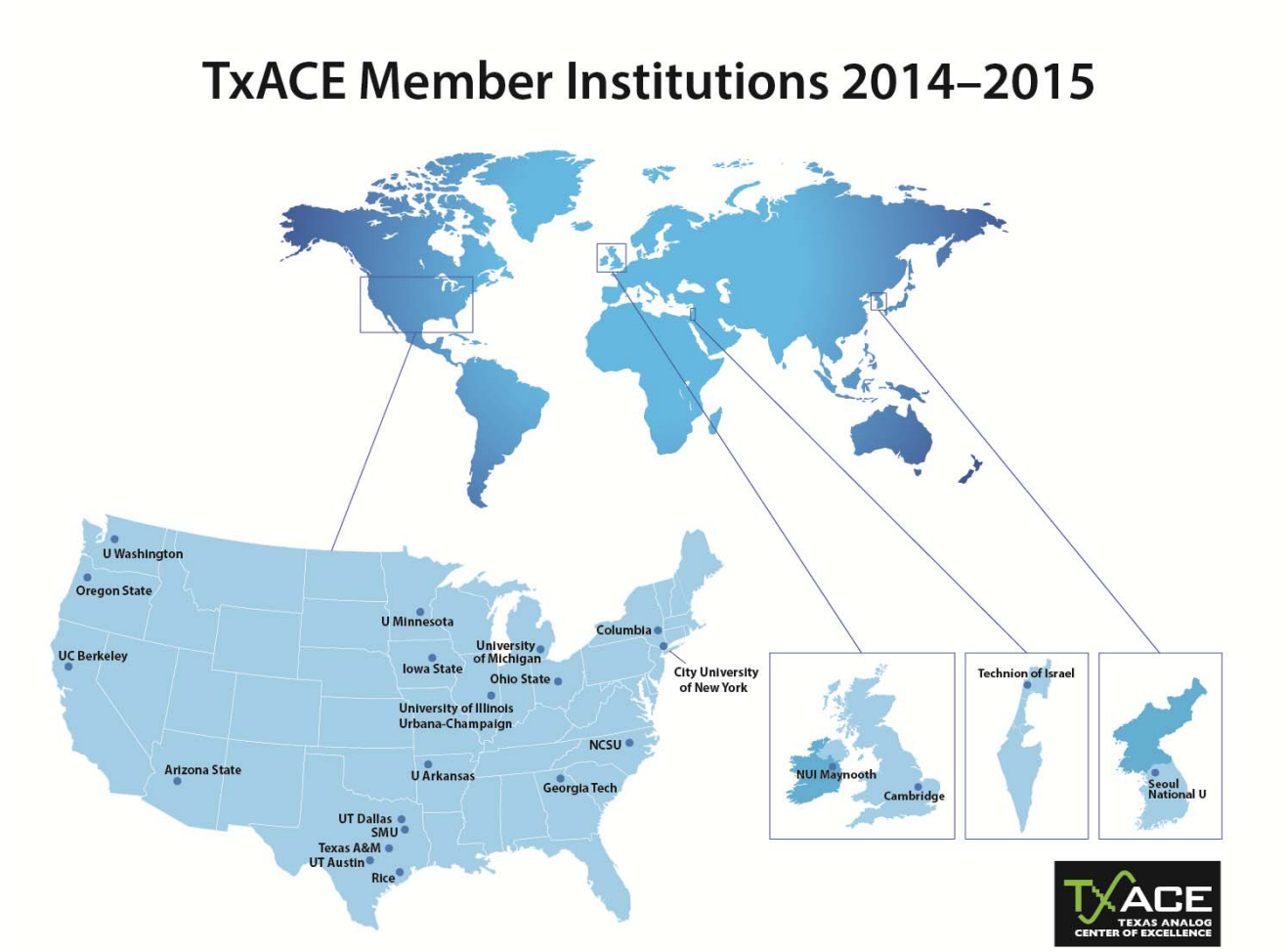


Figure 8: Member institutions of Texas Analog Center of Excellence

SUMMARIES OF RESEARCH PROJECTS

The 70 research projects funded through TxACE during 2014-2015 are listed in Table 2 below by the Semiconductor Research Corporation task identification number.

Table 2: Funded research projects at TxACE by SRC task identification number (FA: Fundamental Analog, EE: Energy Efficiency, HC: Healthcare, S&S: Safety and Security)

	Task	Thrust	Title	Task Leader	Institution
1	1836.069	EE	Electronic Systems for Small-scale Wind Turbines	McMahon, Richard	Cambridge
2	1836.070	EE	Advanced Control of Power Converters	Ringwood, John	National Univ. of Ireland Maynooth
3	1836.075	FA	Design of 3D Integrated Heterogeneous Systems	Mukhopadhyay, Saibal	Georgia Tech
4	1836.076	EE	Ultra-Low Power Delay-Insensitive Asynchronous Circuits	Di, Jia	Univ. of Arkansas/Fayetteville
5	1836.080	FA	Variation-Tolerant Noise-Shaping ADCs With Embedded Digital Bias and V(DD) Scalable from 0.5V to 1.2V for Nanoscale CMOS	Kinget, Peter	Columbia
6	1836.081	EE	Combined Inductive/Capacitive DC-DC Converter	Harjani, Ramesh	Univ. of Minnesota
7	1836.083	S&S	Built-In Test for Millimeter-Wave Phased Arrays	Floyd, Brian	NC State
8	1836.087	FA	A High-Speed Low-Power Clock Data Recovery (CDR)	Gui, Ping	SMU
9	1836.088	EE	Efficient Digital-Intensive Wireless Transmitters Utilizing Switching Mode Pas	Gharpurey, Ranjit	UT Austin
10	1836.093	FA	Variability-Aware, Discrete Optimization for Analog Circuits	Kim, Jaeha	Seoul National Univ.
11	1836.094	S&S	Accurate FSM Approximations of Analog/Rf Systems For Debugging Mixed-Signal Designs	Roychowdhury, Jaijeet	UC Berkeley
12	1836.095	FA	Test Generation for Mixed-Signal Design Verification and Post-Silicon Debugging	Shi, Richard	Univ. of Washington
13	1836.096	FA	Mixed-Signal Design Centering in Deeply Scaled Technologies	Nikolic, Borivoje	UC Berkeley
14	1836.097	FA	Dual-Domain SAR ADCs Incorporating Both Voltage and Time Information	Moon, Un-Ku	Oregon State
15	1836.098	HC	Sub mW Wireless Transceiver Frontends for Body Area Networks	Harjani, Ramesh	Univ. of Minnesota
16	1836.099	EE	Automated Modeling of Switching Regulators	Mantooth, Homer Alan	Univ. of Arkansas/ Fayetteville
17	1836.101	S&S	Sparse 2D MIMO Radar Transceiver Design and Prototyping for 3D Millimeter-Wave Imaging	Saquib, Mohammad	UT Dallas

	Task	Thrust	Title	Task Leader	Institution
18	1836.102	S&S	Superresolution Techniques for 3D Millimeter Wave Radars	Torlak, Murat	UT Dallas
19	1836.103	HC	Reconfigurable Brain Computer Interface	Jafari, Roozbeh	UT Dallas
20	1836.103	HC	Design of Analog Front-End for Reconfigurable Brain Computer Interface	Chiu, Yun	UT Dallas
21	1836.106	EE	IF-Sampling CMOS ADC Front-End with 100-dB Linearity	Chiu, Yun	UT Dallas
22	1836.107	FA	Verification of Multi-State Vulnerable AMS Circuits	Geiger, Randall	Iowa State
23	1836.109	FA	New Paradigms for High-Performance Amplification	Moon, Un-Ku	Oregon State
24	1836.110	EE	Distributed Power Delivery Architecture for 2D and 3D Integrated Circuits	Mukhopadhyay, Saibal	Georgia Tech
25	1836.111	FA	Advanced ADC-Based Serial Link Receiver Architectures	Palermo, Samuel	Texas A&M
26	1836.112	EE	Shortstop: Fast Power Supply Boosting	Blaauw, David	Univ. of Michigan
27	1836.113	FA	Synthesized Cell-Based ADPLL Implementation for Accelerated Design	Wentzloff, David	Univ. of Michigan
28	1836.114	FA	Frequency Shapeable Multichannel ADCs	Eldar, Yonina	Technion
29	1836.115	EE	Analysis and Characterization of Switched-Mode DC-DC Power Converters	Li, Peng	Texas A&M
30	1836.116	EE	Efficient Pa Architectures for Powerline Communications	Gharpurey, Ranjit	UT Austin
31	1836.117	FA	Performance and Reliability Enhancement of Embedded ADCS with Value-Added BIST	Geiger, Randall	Iowa State
32	1836.118	EE	Low Noise, Low Ripple Fully Integrated Isolated DCDC Converters for Signal Chain Applications	Bakkaloglu, Bertan	Arizona State
33	1836.119	S&S	Demonstration of 180-300 GHz Transmitter for Rotational Spectroscopy	O, Kenneth	UT Dallas
34	1836.120	S&S	Evaluation of Frequency and Noise Performance of CMOS 180 – 300 GHz Spectrometer Transmitter and Receiver Components	Lee, Mark	UT Dallas
35	1836.122	S&S	On-Chip Integration Techniques for 180-300 GHz Spectrometers	Henderson, Rashaunda	UT Dallas
36	1836.123	EE	Test Techniques and Fault Modeling for High Voltage Devices and Boards	Kim, Bruce	CUNY
37	1836.124	EE	Study and Analysis of Fast Power-On Clock Multipliers in the Presence of PVT Variations	Hanumolu, Pavan Kumar	UIUC
38	1836.125	FA	10GS/s+ Resolution-Scalable (4-7bits) ADCs	Flynn, Michael	Univ. of Michigan

	Task	Thrust	Title	Task Leader	Institution
39	1836.126	S&S	Design Spin Reduction via Integrated THz Design: Applications, Physics, and System Engineering	De Lucia, Frank	Ohio State
40	1836.127	FA	Precision Test without Precision Instruments	Chen, Degang	Iowa State
41	1836.128	FA	Statistical Analog Design Property Checking	Li, Peng	Texas A&M
42	1836.129	FA	Study Of Burst-Mode Data Recovery for High Loss Channels	Hanumolu, Pavan Kumar	UIUC
43	1836.130	EE	Built-In Self-Test Techniques for Test, Calibration, and Trimming of Power Management Units: PMU-BIST	Ozev, Sule	Arizona State
44	1836.131	S&S	Process Variation Anatomy: A Statistical Nexus Between Design, Manufacturing and Yield	Makris, Yiorgos	UT Dallas
45	1836.132	FA	Fault Coverage Analysis of Analog/Mixed-Signal Tests Based on Statistical Dissimilarity	Kim, Jaeha	Seoul National Univ.
46	1836.133	EE	Energy-Efficient Signal Processing Techniques for Smart Grid Heterogeneous Communications Networks	Al-Dhahir, Naofal	UT Dallas
47	1836.134	FA	Hybrid Two-Step PLLs for Digital SoCs in Nanoscale CMOS	Kinget, Peter	Columbia
48	1836.135	S&S	Sub-Picosecond Synchronization of Widely Spaced Imaging Arrays	Babakhani, Aydin	Rice Univ.
49	1836.136	FA	Injection-Locked Ring Oscillators for Clock Distribution in Manycore Processors	Nikolic, Borivoje	UC Berkeley
50	1836.137	FA	50GS/s and Beyond Frequency-interleaved Energy-Efficient ADCs	Niknejad, Ali	UC Berkeley
51	1836.138	EE	Micro-Power Analog-to-Digital Data Converters	Temes, Gabor	Oregon State Univ.
52	1836.139	EE	Enabling Fully-Integrated VHF CLK-Sync Multiphase Switching Regulators on Silicon	Ma, Dongsheng	UT Dallas
53	1836.140	EE	Embedded & Adaptive Voltage Regulators with Practive Noise Reduction for Digital Loads Under Wide Dynamic Range	Raychowdhury, Arijit	Georgia Tech
54	1836.141	FA	IC Design for Resilience Against System-Level ESD	Rosenbaum, Elyse	UIUC
55	1836.142	EE	Low Power Applications of FRAM	Blaauw, David	Univ. of Michigan
56	1836.143	EE	Design Techniques for Modulation-Agile and Energy-Efficient 60+Gb/s Receiver Front-Ends	Palermo, Samuel	Texas A&M
57	1836.144	EE	High-efficiency High-voltage Power Converters	Lee, Hoi	UT Dallas
58	1836.145	FA	RF and Mixed Signal Quantum CMOS Devices and Circuits	Lee, Mark	UT Dallas
59	1836.146	EE	On-Chip AC-DC Power Conversion with Ground Disturbance Shielding for Environmental Sensing Applications	Ma, Dongsheng	UT Dallas
60	1836.147	S&S	Demonstration of 180 – 300 GHz Receiver for Rotational Spectroscopy	Choi, Wooyeol	UT Dallas

	Task	Thrust	Title	Task Leader	Institution
61	1836.148	FA	50GSPS+ TI Hybrid SAR ADC Array with Comprehensive DDI Calibration	Chiu, Yun	UT Dallas
62	1836.149	EE	Condition Monitoring of PM/IPM Motors through Axial/Radial Leakage Flux	Akin, Bilal	UT Dallas
63	1836.150	S&S	Robust High Resolution Techniques for Millimeter Wave Radars in Complex Environments	Torlak, Murat	UT Dallas
64	1836.151	S&S	Development of Dielectric Waveguides for the Radiation Applications	Macfarlane, Duncan	UT Dallas
65	1836.152	S&S	Feasibility of CMOS Transmitter and Receiver for 500-Gbps Communication over Dielectric Waveguide	O, Kenneth K.	UT Dallas
66	1836.153	EE	High-Speed Compact Power Supplies For Ultra-Low-Power Wireless Sensor Applications	Ma, Dongsheng	UT Dallas
67	1836.154	EE	State of The Health (SOH) for IGBTS: Incipient Fault Characterization and Degradation Monitoring	Akin, Bilal	UT Dallas
68	1836.155	S&S	Development Of Wideband Vibration Sensors	Pourkamali, Siavash	UT Dallas
69	1836.156	S&S	Transition Design for High Data Rate Links at Submillimeter Wave Frequencies	Henderson, Rashaunda	UT Dallas
70	1836.157	EE	CMOS GSPS 12-Bit SAR ADC Array With On-Chip Reference Buffers	Chiu, Yun	UT Dallas

ACCOMPLISHMENTS

TxACE has made significant research progress. Table 3 summarizes the number of publications and inventions resulting from the TxACE research during May 2014 to April 2015, while Table 4 lists the major research accomplishments for the Center during the period. The TxACE researchers have published 136 conference papers and 20 journal papers. They have also filed four patent applications. The list of publications is included as Appendix I. Following the tabulation, brief summaries of each project are provided.

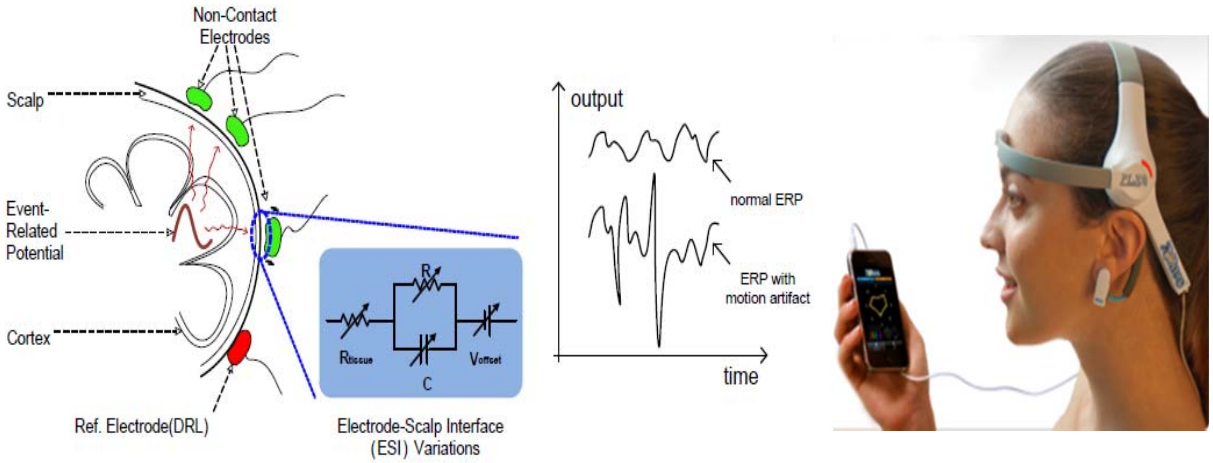
Table 3: TxACE number of publications (May 2014 through April 2015)

Conference Papers	Journal Papers	Invention Disclosures	Patents Filed	Patents Granted
136	20	0	4	0

Table 4: Major TxACE Research Accomplishments (May 2014 through April 2015)

Category	Accomplishments
Fundamental Analog (Test)	Techniques that systematically model and remove measurement uncertainty to reduce test costs of data converters are demonstrated. In particular, the histogram tests are inefficient and the new techniques reduce test time by three orders of magnitude. (1836.127 PI: D. Chen, Iowa State)
Energy Efficiency (Circuits)	High switching frequency of power converters requires minimized gate driver propagation delay dominated by level shifting. A high speed adaptive feedback BST gate driver is proposed. Sub-ns delay dynamic level shifters can accommodate different voltages and achieve a level shifting delay below 250ps. The driver propagation delay is maintained below 2ns and the adaptive dead time is fixed at 1.2ns. (1836.146, PI: D. Ma, UT Dallas)
Energy Efficiency (Circuits)	Inactive periods in energy proportional data links can be of the order of few milliseconds or higher. Temperature and voltage variations during this idle period cause frequency drift in an oscillator. A phase calibration technique that reduces the PLL lock time to < 1ns and the phase drift to ±3ps is demonstrated. (1836.124, PI: P. Hanumolu, University of Illinois).
Health Care (Circuits)	A digital online technique for motion artifact tracking and compensation is demonstrated for electroencephalogram (EEG) monitoring using dry-contact electrodes. This enabled revelation of signals that were previously not able to be detected. (1836.103, PI: Y. Chiu, University of Texas at Dallas).
Security and Safety (Circuits)	A 447-GHz frequency tripler has been demonstrated in 65-nm CMOS using novel varactor structures and providing 0.5-mW output power (-3.2 dBm) with only 15-dB conversion loss. This indicates that 65-nm CMOS can be used to implement the required terahertz guided-wave interconnects. (1836.152, PI: K. O, UT Dallas)
Security and Safety (Circuits)	A serial I/O receiver with multi-level decision feedback equalization has been demonstrated in 65-nm CMOS for PAM4 which employs one FIR tap and two IIR taps for efficient “long-tail” intersymbol interference cancellation. The quarter-rate PAM4 circuit achieves 32 Gb/s with power efficiency of 0.55 mW/Gbps and area of 0.014 mm^2. (1836.143, PI: S. Palermo, Texas A&M)
Security and Safety (CAD)	Techniques have been developed to accurately abstract and formally analyze the SPICE-level dynamics of AMS systems using purely Boolean models. A technique entitled “BEE” has provides eye-diagram analysis for high-speed links with an order of magnitude speed-up over Monte-Carlo analysis with no loss of accuracy. (1836.094, PI: J. Roychowdhury, UC. Berkeley)

Health Care Thrust



Category	Accomplishment
Health Care	A digital online technique for motion artifact (MA) tracking and compensation is demonstrated for electroencephalogram (EEG) monitoring using dry-contact electrodes. The measurement of bio-potential acquisition-path gain (APG) of the electrode-tissue interface is utilized by a digital-domain gain compensator to act in the opposite way to the MA induced APG variation in real time. The remaining baseline additive motion artifact is treated by a digital high-pass filter. These enabled revelation of signals that were previously not able to be detected. (1836.103, PI: Y. Chiu, University of Texas at Dallas).

TASK 1836.098, SUB MW WIRELESS TRANSCEIVER FRONTEND FOR BODY AREA NETWORKS

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SIGNIFICANCE AND OBJECTIVES

The project focuses on developing a low power transceiver frontend to meet the IEEE 802.15.6 Wireless Body Area Networks (WBAN) narrowband specifications from 2360 to 2483MHz.

TECHNICAL APPROACH

Our design approach is to use novel simple architecture which consumes less power, sub-threshold operation, explore optimal partitioning of functions between analog and digital sections, applying injection locking, current reuse techniques to minimize power consumption, partial positive feedback, passive voltage multiplication and dynamic current mode techniques.

SUMMARY OF RESULTS

The overall block diagram of the transceiver is shown in Figure 1. We have designed and fabricated both the TX and RX.

We have taped out and tested the transmitter in IBM 130nm technology. A MUX-based architecture is proposed where modulation occurs at 800MHz (i.e., 1/3rd the RF frequency). The energy efficiency including the estimated power of the PLL is 2.5nJ/bit. Further, this design does not require cap bank calibration, can support a large number of channels (118) even at high GHz frequencies and has no nonlinear phase mapping issues unlike existing IL techniques . The modulation scheme is very precise with measured RMS EVM is 3.21%.

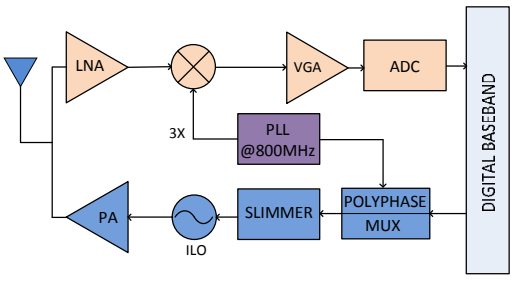

Figure 1: Transceiver architecture

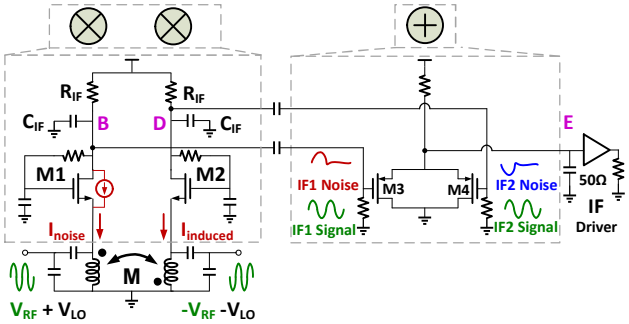

Figure 2: Circuit diagram of the FTMNC mixer

We have taped out and tested a low IF receiver in TSMC 65nm technology. A low power low noise 0.7V mixer first RX frontend is designed which uses passive coupling based frequency translated mutual noise cancellation (Figure. 2). Unlike traditional noise cancelling techniques we perform symmetrical noise cancellation of a fully differential structure where each path cancels the noise of the other at IF. This paper tackles the noise figure and power consumption problems of sub 1V mixers. The FOM is 10dB higher and power consumption is 194µW which is 0.5X lower than the state of the art. This design (Figure 3) improves on all three specifications i.e. FOM, LO power & NF. The full system design is in progress.

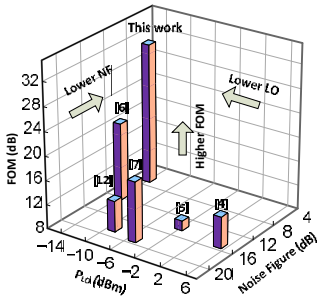

Figure 3: Chart comparing FOM, LO power and NF of RX

Keywords: 802.15.6, WBAN, low power RF, injection locked oscillator, noise cancellation

INDUSTRY INTERACTIONS

Texas Instruments, Intel, Freescale

MAJOR PAPERS/PATENTS

[1] M. Rahman, M. Elbadry, R. Harjani "An IEEE 802.15.6 Standard Compliant 2.5nJ/bit Multiband WBAN Transmitter using Phase Multiplexing and Injection Locking," IEEE Journal of Solid-State Circuits, May 2015.

[2] M. Rahman, R. Harjani "A 0.7V 194µW 31dB FOM 2.3-2.5 GHz RX Frontend for WBAN with Mutual Noise Cancellation using Passive Coupling," IEEE RFIC 2015.

[3] M. Rahman, M. Elbadry, R. Harjani "A 2.5nJ/bit Multiband (MBAN & ISM) Transmitter for IEEE 802.15.6 based on a Hybrid Polyphase-MUX/ILO based Modulator," IEEE RFIC, June 2014.

TASK 1836.103, RECONFIGURABLE BRAIN COMPUTER INTERFACE

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MIKE CHI, UC-SAN DIEGO

SIGNIFICANCE AND OBJECTIVES

Dry EEG electrodes enhance the convenience and wearability of brain computer interface (BCI) systems, but the noise induced due to the skin electrode interface reduces the signal quality compared to that of wet electrodes. The aim is to design a wearable dry contact EEG system that estimates and responds to variations in skin contact impedance across different electrodes as well as motion artifacts in real-time to improve the signal to noise ratio (SNR)/enhance signal processing accuracy.

TECHNICAL APPROACH

Analyses aimed at electrode-skin noise characterization were performed. Several noise models including half-cell noise, motion artifacts and baseline wandering were considered. Several electrode configurations including an electrode module where each individual finger can be sensed simultaneously and a module where fingers can be activated/deactivated based on their noise characteristics using a MUX were designed, developed and validated. Signal processing algorithms based on ICA that remove noisy channels were developed.

SUMMARY OF RESULTS

We analyzed a popular dry electrode design that incorporates several 'finger' shaped contacts and showed how the noise level can be reduced by estimating the contact quality of each finger and reconfiguring the electrode accordingly. We designed custom electrodes and showed the differences in skin interface noise among fingers of the same electrode. Finally, we showed how eliminating the signals from one of more noisy fingers can lead to better correlation with an ideal wet electrode and reduce the amount of noise by 1.6µV on average, which constitutes 11% of the EEG signal.

We designed a methodology to uniformly compare different designs of finger-based dry electrodes to each other and demonstrated with experimental results that designs with a sparser arrangement of fingers were able to penetrate through hair better and were more robust to varying use cases. We also showed that individual fingers on an electrode can each have vastly differing signals due to differing contacts, and in turn, the ones with a bad contact could be picking up more local noise effects. We designed two custom electrodes, the block diagram for one shown in Figure 1, to come to these conclusions and showed through experimental results that the overall signal from a given electrode can be improved by selecting only a subset of fingers with a good contact on the scalp.

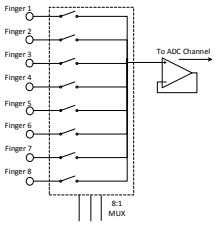

Figure 1: MUX electrode block diagram.

We also created a novel automated artifact-related ICs identification algorithm. The proposed methods take into account both physiological artifacts and non-biological artifacts. An ERP-related clustering method is proposed for physiological artifact-related ICs identification. A quantitative comparison of original EEG signals with reconstructed artifact-free signals shows that the proposed algorithm can effectively enhance the ERP quality for all subjects in the study, even for those that barely display ERPs in the original recordings. Electrode-scalp impedance information was employed for non-biological artifact-related ICs identification. Quantitative comparisons of the proposed algorithm to other methods show that significant performance improvements were achieved using our proposed method compared to four commonly used automatic removal methods for noisy ICs.

Keywords: Dry-contact EEG, BCI, Electrode-skin noise modeling, Electrode reconfiguration, Motion artifact rejection.

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] Zou et al., "Automatic Identification of Artifact-related Independent Components for Artifact Removal in EEG Recordings", 2015, IEEE Journal of BHI.

[2] Nathan, et al., "Reducing the Noise Level of EEG Signal Acquisition through Reconfiguration of Dry Contact Electrodes", 2014 BioCAS, Lausanne, Switzerland.

[3] Jafari, et al., http://bcibench.org/

TASK 1836.103, DESIGN OF ANALOG FRONT-END FOR RECONFIGURABLE BRAIN COMPUTER INTERFACE

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SIGNIFICANCE AND OBJECTIVES

For dry-contact EEG/ECG monitoring, variation of electrode to tissue interface (ETI) impedance due to subject movement leads to motion artifacts (MA) and distorts recorded signals. Compensation is required to help mitigate the effects of MA in Brain-Computer Interface (BCI) devices.

TECHNICAL APPROACH

Our technique incorporates the motion artifact rejection and stabilization (MARS) based on pseudorandom noise (PN) sequence injection to combat detrimental MA effects.

SUMMARY OF RESULTS

Two types of MA are identified – the Additive MA (AMA) which leads to baseline wonder and the Multiplicative MA (MMA) which distorts the signal-acquisition-path gain. AMA can be removed by simple high-pass filtering (HPF), while MMA needs additional compensation.

$$V_{in}(t)=\underbrace{\frac{Z_{in}\|(sC_p)^{-1}}{Z_{in}\|(sC_p)^{-1}+Z_{ETI}(t)}}_{\text{MMA}}\cdot\left[V_1(t)+\underbrace{V_{hc}(t)}_{\text{AMA}}\right]$$

The MARS technique is proposed in this work. A PN sequence is injected to the subject by the analog front-end (AFE) circuit to probe the signal-acquisition-path gain experienced by the bio-potential since the bio-potential see the same acquisition-path gain as PN sequence does. Then the gain variation induced by MMA is estimated by autocorrelation with original PN sequence and then compensated in the digital domain in real time, thereby minimizing the multiplicative distortion caused by the MMA at its origin.

Fig. 1 shows the system diagram of the MARS technique. Fig. 2(a) shows the normalized EEG signal spectra in the alpha-band (8-15 Hz) for the tests with MAs injected by eye open-close movements. We can observe that there is no significant spectral peak in the raw dataset (dot-dashed curve with square symbols), whereas after the AMA correction (dashed curve with triangular symbols), the alpha-band power spectral density (PSD) is enhanced—for instance, the PSD at 11 Hz is improved by 0.168 (from 0.056 to 0.224) and the one at 12 Hz is improved by 0.195 (from 0.050 to 0.245). In contrast, the PSD computed using the proposed technique (i.e., MMA+AMA) revealed two obvious peaks at 11 Hz and 12 Hz—the average PSD values (solid curve with circular symbols) show that the two maximum improvements of 0.505 (from 0.056 to 0.561) and 0.401 (from 0.050 to 0.451) occur at 11 Hz and 12 Hz, respectively. The measurement results demonstrate the improvement from MARS technique. A test chip is also taped-out in a 65-nm CMOS technology and measured.

Keywords: BCI, MA, AFE, MARS, NIC

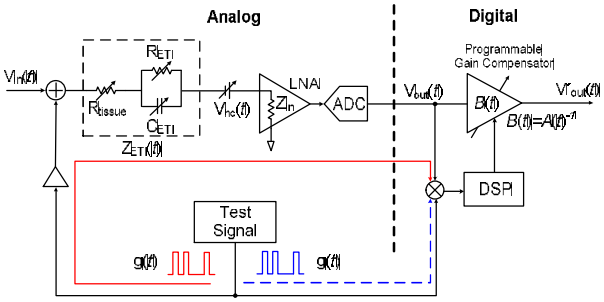


Figure 1: System diagram of the MARS technique.

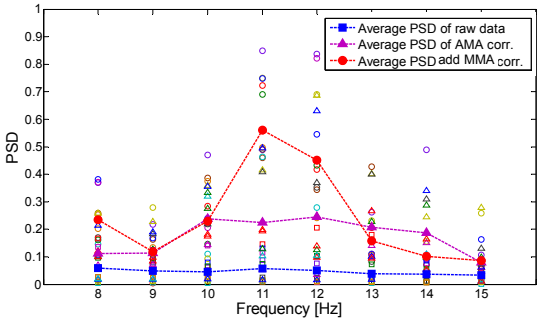


Figure 2: Measured normalized EEG signal spectra in the alpha-band with MAs.

INDUSTRY INTERACTIONS

Texas Instruments, Intel

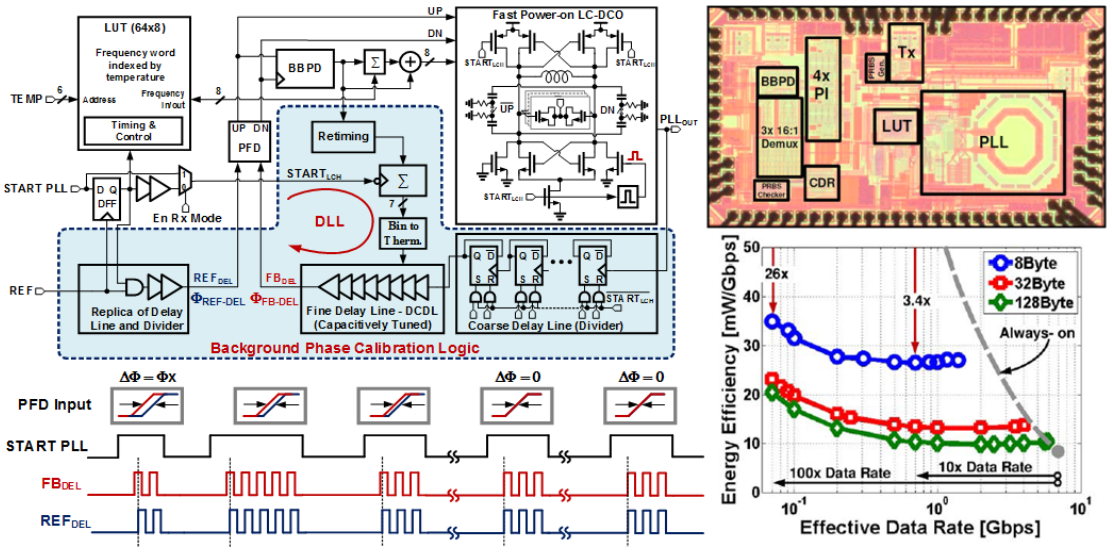
MAJOR PAPERS/PATENTS

[1] J. Song et al., "A Motion-Artifact Tracking and Compensation Technique for Dry-Contact EEG Monitoring System," IEEE Signal Processing in Medicine and Biology Symposium 2014.

[2] J. Song, et al, "A motion-artifact rejection and stabilization (MARS) technique for bioelectronic interface circuits and systems," in SRC TECHCON 2014.

[3] U.S. Patent pending, "Body-driven pseudorandom signal injection for biomedical acquisition channel calibration," Application No. 14/327,283.

Energy Efficiency Thrust



Depiction of Fast Power-on LC-PLL with Background Phase Calibration

Category	Accomplishment
Energy Efficiency	Inactive periods in energy proportional wireline or wireless links can be of the order of few milliseconds or higher. Temperature and voltage variations during this idle period could cause frequency drift in an oscillator. A phase calibration technique that reduces the PLL lock time to < 1ns and the phase drift to ±3ps is demonstrated. With 100mV of DLL supply variation during a power-off state, the error in the phase drift is less than 2ps. (1836.124, PI: P. Hanumolu, University of Illinois).
Energy Efficiency	High switching frequency for a power converter requires minimized gate driver propagation delay, which is dominated by level shifting. A high speed adaptive feedback BST gate driver is proposed. Sub-ns delay dynamic level shifters can accommodate different voltages and achieve a level shifting delay below 250ps. The driver propagation delay is maintained below 2ns and the adaptive dead time is fixed at 1.2ns. (1836.146, PI: D. Ma, UT Dallas)
Energy Efficiency	Self-diagnostics/prognostics capable inverters that can detect and warn users, and predict remaining useful lifetime (RUL) of switches to prevent costly shutdowns are being developed. Die-related electrical properties do not change due to thermal cycling. The on-state resistance for power MOSFETs increases exponentially under repetitive thermal cycles, up to 20%. Due to the differences in the physical structures, the degradation progression is different even for the same type of switches under the same thermal conditions. (1836.154, PI: B. Akin, UT Dallas)

TASK 1836.069, ELECTRONIC SYSTEMS FOR SMALL – SCALE WIND TURBINES

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SIGNIFICANCE AND OBJECTIVES

This project looks at the electrical system of small-scale wind turbines of power ratings up to 5 kW and micro wind turbines (100 W) deployed in Antarctica, with the aim of reducing the cost of this electronics, chiefly by eliminating sensors and replacing them with more advanced control.

TECHNICAL APPROACH

Sensorless control has been proposed to achieve maximum extraction of the power generated by generators driven by small-scale wind turbines. The power extraction is done by controlling the speed of a permanent magnet synchronous generator (PMSG).

Also, micro wind turbine modeling has been done. The model includes generator, wind turbine dynamics and current controller characterization. A simplified sensorless estimation was proposed to calculate the rotor speed. All tests were carried out using real Antarctic wind data.

SUMMARY OF RESULTS

A complete control scheme has been developed to operate a small wind turbine. The system includes a sensorless speed and torque estimation technique, maximum power point tracking algorithm for optimal performance and sliding mode control to drive an IGBT based active rectifier. The entire system was tested successfully under different wind speed profiles.

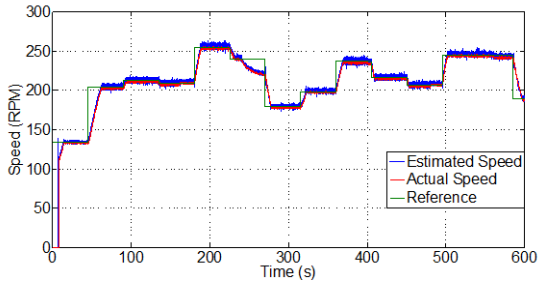

Figure 1: Maximum power point tracking by setting an optimal speed reference according to the wind conditions. Sensorless control was applied

The second stage of this project is focused on the model and control of micro wind turbines used in Antarctica stations by our project partner British Antarctic Survey (BAS). Two particular devices have been studied: Ampair 100 and Rutland 913. Both turbines are designed for battery charging at 12 or 24 V. The study includes mathematical models for the generator coupled to the turbine, a model for the wind turbine dynamics, power coefficient and tip speed ratio characteristics, and characterization of the current design of controller developed by BAS. This control is based on a switching MOSFET that limits the current and voltage to the battery. In addition, a simplified sensorless speed estimation based only on DC measurements was developed. The idea of this algorithm is to use the available hardware without further changes so that it can be implemented straightforwardly in the operating equipment. All the tests were performed using real wind data from Antarctica. The machine models and speed estimation are valuable for future studies such as failure analysis, preventive control and scheduled maintenance.

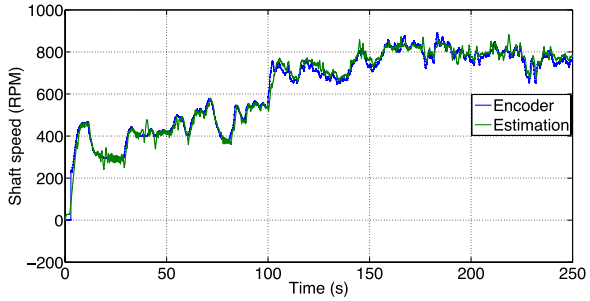

Figure 2: Simplified sensorless speed estimation for micro wind turbines.

Keywords: wind turbines, electrical machine modeling, sensorless control, Antarctica, PM generator

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] D Llano and R McMahon, “Sensorless control for permanent magnet generators associated with a wind turbine emulator test-rig”, PEMC-14, SEPT 2014, Antalya, Turkey.

[2] D Llano and R McMahon, “Single phase grid integration of permanent magnet generators associated with a wind turbine emulator test-rig”, IECON-14, NOV 2014, Dallas, USA.

[3] D Llano and R McMahon, “Torque observer and extended H infinity filter for sensorless control of permanent magnet generator tested in a wind turbine emulator”. EPE-14, August 2014. Lappeenranta, Finland.

TASK 1836.070, ADVANCED CONTROL OF POWER CONVERTERS

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SEAMUS O'DRISCOLL, TI, CORK, IRELAND

SIGNIFICANCE AND OBJECTIVES

This project involves the modeling and control of switched-mode power supplies. Specifically, nonlinear models are developed and an efficient fixed-parameter controller is designed.

TECHNICAL APPROACH

Initially, a comprehensive nonlinear transformer model was developed [1] and various control approaches examined, including robust control [2] and fixed-parameter digital control [3].

SUMMARY OF RESULTS

The novelty of the modeling approach centers on the inclusion of both static nonlinear (hysteresis) characteristics and dynamic (linear) elements, resulting in a model which is both computationally tractable and has high fidelity. The model, a schematic of which is shown in Fig.1, has been validated against experimental data.

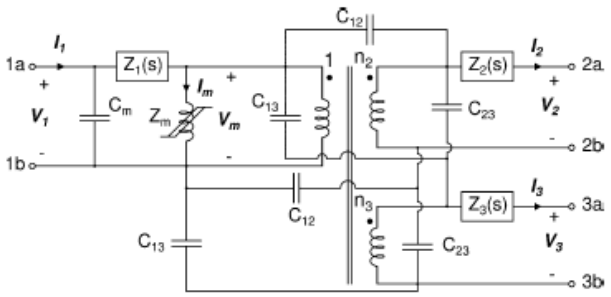

Figure 1: Nonlinear dynamic model of a 3-winding transformer.

The parameters of the model were determined from experimental data, using continuous-time system identification techniques, as shown in Fig.2.

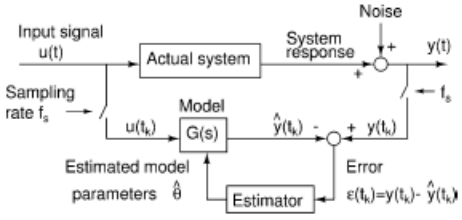

Figure 2: Generic procedure to estimate a model of an actual system from sampled data.

The control solution began with a study that examined the feasibility of using robust control to attempt to provide adequate performance of the power converter over the full operational space. However, this proved virtually impossible, as reported in [2]. The significant variations in system frequency response are shown in Fig.3.

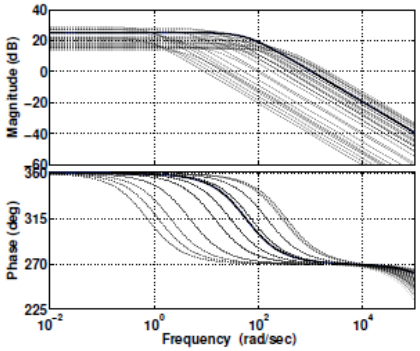

Figure 3: Frequency response of G_{vc} at different working points. The solid line is the nominal plant whitle dotted lines are perturbed plants.

However, an approach based on fixed-parameter, but with a variable sampling period, proved to be attractive both in terms of performance and computational simplicity and was implemented in real time using a TI C2000 microcontroller [3].

Keywords: Power converter, switched-mode, digital control, modeling, robust control

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Trong Vu, T., O'Driscoll, S. and Ringwood, J.V.. *Nonlinear dynamic transformer time-domain identification for power converter applications*. IEEE Transactions on Power Electronics, Vol.29, No.1, pp 318-327, 2014.

[2] Trong Vu, T., O'Driscoll, S. and Ringwood, J.V.. *A feasibility study into the robust control of a variable-frequency wide operating range flyback con*. Proc. Irish Signals and Systems Conf.. Limerick, 2014.

[3] Trong Vu, T., O'Driscoll, S. and Ringwood, J.V.. *Computationally efficient fixed-parameter digital control of power converters*. Proc. Int. Symposium on Industrial Electronics, Istanbul, Turkey, 2014.

TASK 1836.076, ULTRA-LOW POWER DELAY-INSENSITIVE ASYNCHRONOUS CIRCUITS

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SCOTT SMITH AND H. ALAN MANTOOTH, UNIVERSITY OF ARKANSAS

SIGNIFICANCE AND OBJECTIVES

This project will evaluate the integration of MTCMOS power gating with delay-insensitive asynchronous logic for reducing energy consumption in both active and standby modes, as well as explore the ultra-low voltage asynchronous circuit design opportunity.

TECHNICAL APPROACH

Since the spacer cycle of a dual-rail delay-insensitive asynchronous component is equivalent to gating the power of this component and forcing the output to logic 0, these circuits can enter sleep mode after every data cycle, while the circuit is in operation, and the handshaking signals between registers can be used as sleep control signals to control the power gating transistors. This approach has several merits: 1) limiting leakage in both active and sleep modes; 2) alleviating the effort and complexity of designing the sleep signal generation mechanism; 3) reducing the area overhead; and 4) facilitating the tool flow development.

SUMMARY OF RESULTS

The Multi-Threshold NULL Convention Logic (MTNCL) technology incorporates MTCMOS power gating mechanism in NCL, resulting in significant savings in energy consumption without large overhead in area. The second test vehicle is MSP430. A preliminary tapeout has been completed in July 2014. The process used was the GLOBALFOUNDRIES 65nm bulk CMOS process. Both versions of the MSP430 core, i.e., synchronous and MTNCL, were integrated on the testchips excluding memory and peripherals. The chips have come back from the foundry and the chip testing is being carried out. The final tapeout at MOSIS took place in February 2015 using the IBM 8RF-DM 130nm bulk CMOS process. Both versions of the MSP430 core were included. Memory and timers were integrated into each version for fair comparison. In order to reduce pin count, additional I/O logic was designed and incorporated into both chips. The layouts of the synchronous and MTNCL chips are shown in Figures 1 and 2, respectively.

After chips come back in late May, chip testing will take measurements of active energy, leakage power, performance, and voltage scalability. The results will be analyzed and summarized in the final report.

Keywords: MTCMOS, delay-insensitive, asynchronous, ultra-low power, chip testing

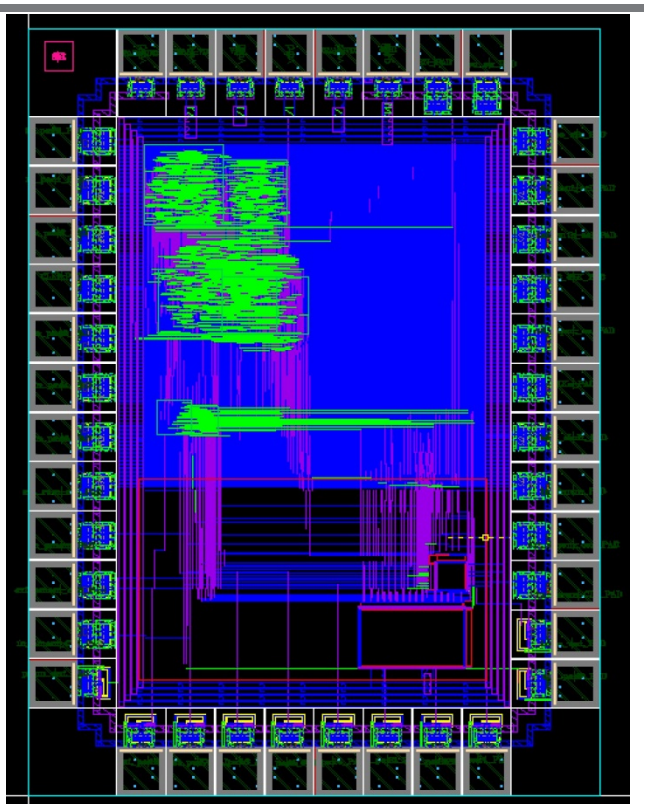

Figure 1: Synchronous MSP430 Test Chip Layout.

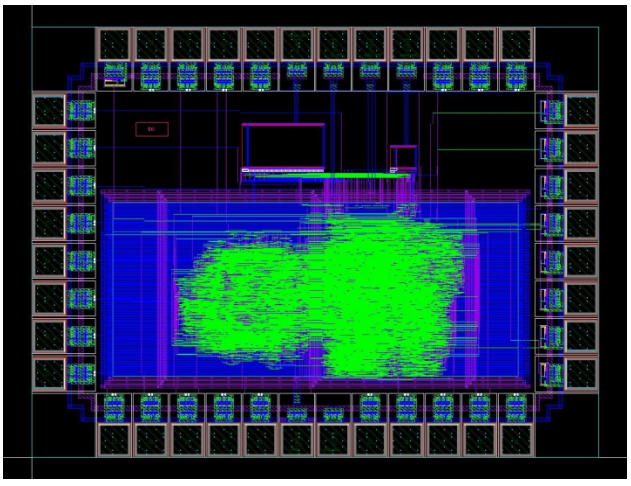

Figure 2: MTNCL MSP430 Test Chip Layout.

INDUSTRY INTERACTIONS

Texas Instruments, Intel, AMD

MAJOR PAPERS/PATENTS

1836.081, COMBINED INDUCTIVE/CAPACITIVE DC-DC CONVERTER

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SIGNIFICANCE AND OBJECTIVES

This project focuses on the design of fully integrated combined inductive/capacitive converters. Inductive converters are used for higher loads and capacitive converters are used for lighter loads. As part of this research we have designed, fabricated and tested a high performance hybrid converter. The current focus is on the design of compact high-efficiency capacitive converters.

TECHNICAL APPROACH

As part of our focus on compact high-efficiency capacitive converters we have developed a unified framework for the design of capacitive series-parallel converters. We are now focused on achieving high power density and wide output load range capacitive converters. A reconfigurable capacitive converter supporting wide output DVS load has been designed in 65nm TSMC process and is due for tape-out in May 2015. To optimize the power conversion, five different voltage conversion ratios (1:1, 2:1, 3:1, 3:2, 4:3) have been implemented, all sharing the same on-chip bucket capacitances and working in time interleaving phases to bring down the output ripple. The output voltage regulation is achieved by an asynchronous state machine based digital control loop. A 27 phase time interleaving has been implemented to mitigate the output ripple without the need of a large explicit output filter capacitor thus improving the power density.

SUMMARY OF RESULTS

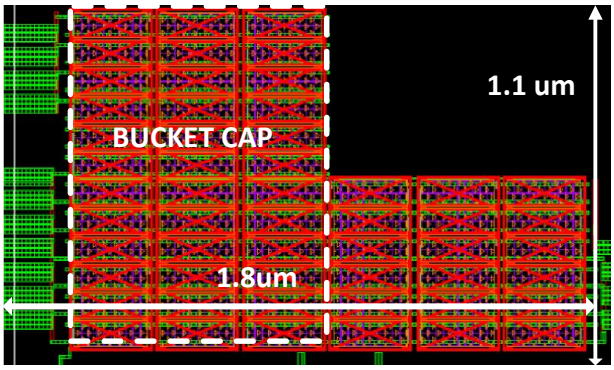

Figure 1: Layout of the design programmable DC-DC converter

Fig. 1 shows the layout of the proposed programmable DC-DC converter. The bucket capacitor occupies the majority of the area and rest is dedicated to the input decoupling capacitor in order to sustain package-based Ldi/dt drops corresponding to 500mA average output current surge of the converter. The fabricated design is expected to be available early fall 2015. The extracted simulation results of the design have been reported in table 1. Peak average power efficiency for 2:1 mode of voltage conversion is 87%. The maximum steady state output voltage ripple is 30mV for 2:1 ratio.

PERFORMANCE PARAMETERS	VALUES
VIN	**1.0V**
VOUT	**0.25V-0.95V**
IOUT	**50uA-500mA**
MAXIMUM RIPPLE	**<=30mV**
PEAK EFFICIENCY	**87%**
POWER DENSITY	**700mW/mm^2**
AREA	**1.3mm^2**

Table 1: Performance parameters after extracted simulations

Each of the five conversion ratios can support the load range of 50uA to 500mA (10^4X) while maintaining average power efficiency greater than 76% and achieving the peak value of 87% for 2:1 mode at 125mA. The digital control loop makes the feedback circuit technology portable and low power consuming. The feedback has the PID flavor realized by the asynchronous digital logic.

Keywords: capacitive converter, programmable conversion ratio, wide output power range, low ripple

INDUSTRY INTERACTIONS

Texas Instruments, Freescale, IBM, Intel

MAJOR PAPERS/PATENTS

[1] S. S. Kudva, S. Chaubey and R. Harjani, “High Power-Density, Hybrid Inductive/Capacitive Converter with Area Reuse for Multi-Domain DVS” IEEE Custom Integrated Circuits Conference, September 2014.

[2] R. Harjani and S. Chaubey, “A Unified Framework for Capacitive Series-Parallel DC-DC Converter Design,” (Invited) IEEE Custom Integrated Circuits Conference, September 2014.

[3] R. Harjani, S. Chaubey, R. Jain (Intel), “Capacitive DC-DC Converter Design” Tutorial at IEEE International Symposium on Circuits and Systems, Lisbon, 2015.

TASK 1836.088, EFFICIENT DIGITAL-INTENSIVE WIRELESS TRANSMITTERS UTILIZING SWITCHING MODE PA'S

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SIGNIFICANCE AND OBJECTIVES

The power efficiency of transmitters continues to pose a critical challenge in the design of portable wireless systems. In this work, wireless transmitters employing RF-PWM with class-D output stages are investigated. RF-PWM is generated using PLL-based, baseband pulse-width modulators, which allows for PWM with high carrier frequencies.

TECHNICAL APPROACH

A fully integrated RF pulse width modulation (RF-PWM) transmitter with a Class-D output stage has been designed. RF-PWM is well suited for use with efficient switching PAs since it is a two-level modulation scheme. It is also well-suited for implementation in deep submicron CMOS technologies, and benefits from device scaling.

The proposed continuous-time RF-PWM generators [2][3] employ PLL-based PWM generation at baseband. Spurious information is localized near harmonics of the carrier, where it can be attenuated by employing low-complexity filters. RF-PWM is generated without an upconverter. Pre-distortion of the baseband signal is employed in order to reduce out-of-band spurs.

SUMMARY OF RESULTS

A PLL-based RF-PWM transmitter with a Class-D PA (Fig. 1) for IoT applications has been designed and implemented in a 65-nm CMOS process. The RF output signal, $x(t) = a(t)\cdot\cos[\omega t + \phi(t)]$, is generated without an upconverter using PLLs. The output signal is linearized by applying an arcsin pre-distortion on the baseband signal.

The architecture uses the difference between two natural sampling PWM signals to provide the RF-PWM signal. A PLL-based PWM generator [1] is used, since it allows for PWM generation without the requirement for ramp signals and comparators, and can thus provide high carrier frequencies. The use of ring oscillators allows for the system to operate over multiple bands, which can be accomplished by changing the reference clock.

The output PWM signals are reshaped within the level shifter and PA driver to prevent shoot-through currents. This is critical to avoid efficiency degradation. These signals subsequently drive differential stacked Class-D PAs that allow operation at 2.4V-supply without excessive device voltage stress.

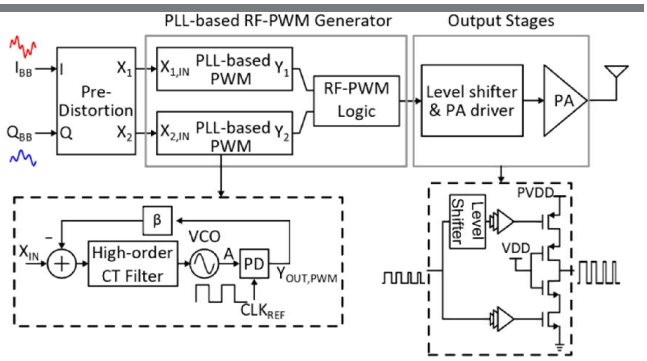

Figure 1: The RF-PWM wireless transmitter

The IC includes the PLL-PWM generators, frequency dividers and the output stage that consists of level shifters, PA drivers, and the Class-D PAs. The pre-distortion block is implemented in digital baseband.

The design was measured with a 1.4-MHz LTE signal with a 6.4-dB PAPR signal, for machine-type-communication (MTC) applications. Results are summarized in Table 1.

Table 1: The summary of the measured results

Technology	65nm CMOS w/ QFN
Frequency [GHz]	2.66
Bandwidth [MHz]	1.4
Peak pout [dBm]	22.4
Peak PAE [%]	46.6
Average P_{out} with 6.4 dB PAR [dBm]	16.1
Average PAE with 6.4 dB PAR [%]	17.5
Active die area [mm^2]	0.48

Keywords: Pulse-width modulation (PWM), phase Locked Loop (PLL), wireless transmitters, switching mode PAs, Intern of Things (IoT).

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] J. Lu, H. Song, and R. Gharpurey, "A CMOS class-D line driver employing a phase-locked loop based PWM generator," IEEE Journal of Solid-State Circuits, vol. 49, pp. 729–739, March 2014.

[2] H. Song and R. Gharpurey, "Digitally Intensive Wireless Transmitter Architecture Employing RF Pulse Width Modulation," IEEE DCAS, Oct. 2014.

[3] H. Song and R. Gharpurey, "Digitally Intensive Transmitter Architecture Employing RF Pulse Width Modulation for IoT applications," IEEE RFIC Symp. 2015.

TASK 1836.099, AUTOMATED MODELING OF SWITCHING REGULATORS

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SIGNIFICANCE AND OBJECTIVES

The goal of this project is to automate the generation of switching regulator models. This will result in models that are more accurate than hand created models and simulate more quickly than other types of models.

TECHNICAL APPROACH

The behavioral models are derived from the PWM switch model that replaces the switching element with a time averaged representation. This drastically reduces simulation time with minimal loss of fidelity.

Automation is accomplished by constrained optimization where it is assumed that the regulator compensation network is the dominating factor. A fully-automated modeling method has been identified in which the frequency response data are analyzed for poles and zeros and the compensation network parameters are back-calculated, from these results the constrained optimization routine can then be applied to optimize the model.

SUMMARY OF RESULTS

This section presents the results of applying the constrained optimization modeling method to the datasheet measurement data. Figure 1 is the opening screen for the modeling tool and demonstrates which parameters must be defined for a basic model.

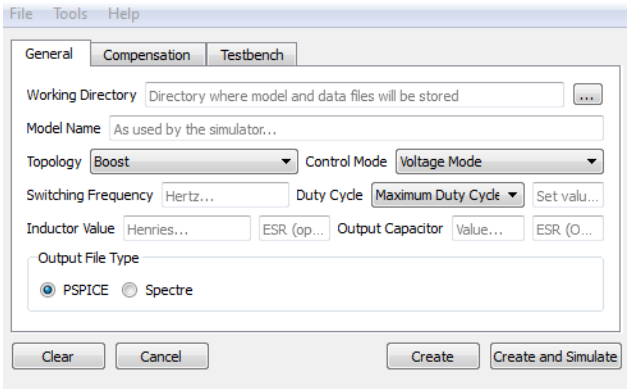

Figure 1. Screenshot of opening screen for modeling tool.

Figure 2 shows a time-domain comparison of datasheet data versus optimized behavioral model simulation data for the Texas Instruments TPS54320 evaluation module.

Figure 3 shows a frequency response graph demonstrating the agreement between simulation and datasheet data for a Freescale MC34713 evaluation module vs simulation model.

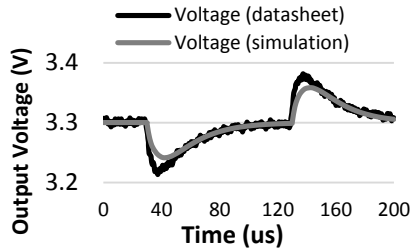

Figure 2. Transient load change comparison for TI TPS54320

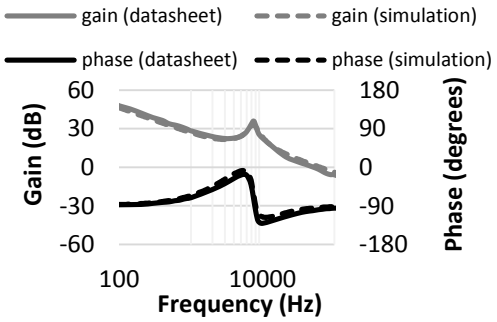

Figure 3. AC phase and gain comparison for Freescale MC34713

These figures clearly demonstrate that the implemented method creates models which not only simulate 1000x faster than models including switching behavior but are also very accurate.

Keywords: switching regulators, behavioral modeling, automation, CAD

INDUSTRY INTERACTIONS

Texas Instruments, Freescale Semiconductor

MAJOR PUBLICATIONS

[1] M. Leonard, *Semi-Automated Switching Regulator Modeling Method and Tool*, M.S. Thesis, Fayetteville, AR: ProQuest Dissertation Publishing, 2015.

TASK 1836.106, IF-SAMPLING CMOS ADC FRONT-END WITH 100-DB LINEARITY

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SIGNIFICANCE AND OBJECTIVES

IF-sampling demands stringent tracking bandwidth and linearity performance of analog-to-digital converters. We present a calibration technique to linearize the CMOS sample-and-hold (S/H) circuits for IF-sampling applications that can potentially achieve a spurious-free dynamic range of over 100 dB.

TECHNICAL APPROACH

A compact derivative-based error model is developed to address the dynamic nonlinearity in CMOS S/H circuits, which is mainly attributed to the nonlinear on-resistance of the MOS transistors. An analog high-pass filter (HPF) derivative-estimation technique is further proposed to obtain direct derivative information (DDI) of the analog input. The S/H error model is also further simplified due to the availability of DDI with reduced digital computing load.

SUMMARY OF RESULTS

In order to verify the derivative S/H dynamic error model and the analog HPF derivative-estimation technique proposed in the previous report, a prototype chip is designated and implemented using GLOBALFOUNDRIES 65nm CMOS LPE process (GF65).

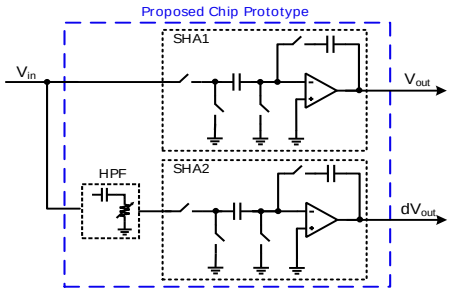

Figure 1: The block diagram of the proposed chip prototype

As shown in Fig.1, the proposed chip prototype consists of two signal paths, which are the main signal path (SHA1) and the HPF derivative estimation path (SHA2). Both signal paths contain a sample/hold amplifier, which feeds the output voltage to two off-chip commercial ADCs.

The final layout of the prototype chip implemented in a GLOBALFOUNDRIES 65-nm CMOS process is shown in Fig. 2, the total chip area is 1mm^2 with 0.152mm^2 active area. In this layout, the routing consists of one poly layer and six different metal layers.

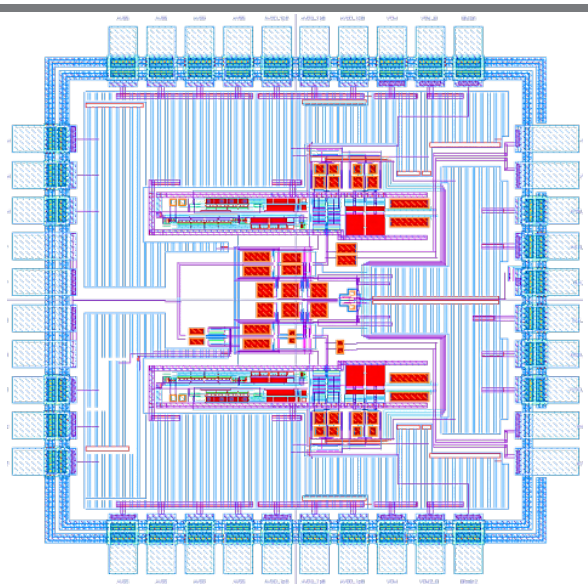

Figure 2: The layout of the prototype chip

The post-layout simulation results shown in Fig. 3 are the post-calibration SFDR performance versus high-pass filter resistance and the quantization resolution of the off-chip ADCs. The SFDR of the main S/H is improved from 70 dB to over 100 dB for input frequencies up to 400 MHz.

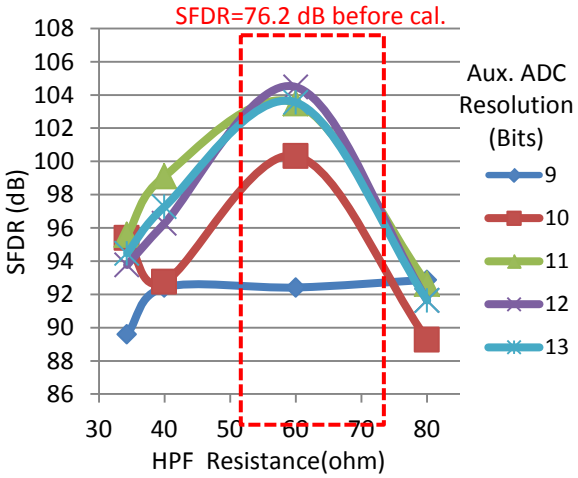

Figure 3: The post-calibration SFDR vs. HPF resistance

Keywords: IF-sampling, calibration, S/H circuit, dynamic nonlinearity, direct derivative information

INDUSTRY INTERACTIONS

Texas Instruments

TASK 1836.110, DISTRIBUTED POWER DELIVERY ARCHITECTURE FOR 2D AND 3D INTEGRATED CIRCUITS

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SIGNIFICANCE AND OBJECTIVES

The primary objective is to design a low-loss, fully integrated, and robust distributed Power Delivery Unit for multicore processors targeting low output voltage from relatively high input voltage. The central innovation is a hybrid down conversion architecture composed of a central switched capacitor (SC) converter and multiple distributed inductive buck (IB) converter.

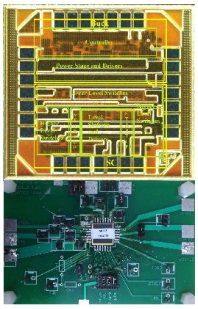
TECHNICAL APPROACH

The hybrid architecture combines the advantages of SC and IB providing following benefits for large down conversion factor: (i) reduced voltage stress across the power FETs compared to a single IB helping integrated DC-DC conversion; (ii) faster response and tighter output regulation compared to a single SC; and (iii) potential for better efficiency compared to a single stage (SC or IB) converter delivering the same output voltage/current as each stage in the hybrid converter operates at reduced conversion ratio and hence, higher efficiency. The circuit innovations are pursued to improve efficiency across wide variation of output voltage and load current.

SUMMARY OF RESULTS

Design of a hybrid converter: A step down converter consisting of a switched capacitor stage followed by an inductive buck stage is designed using low-voltage devices. The SC converter is designed to produce a 4:1 down conversion from an unregulated 4.8V DC supply. The buck regulator is designed in synchronous peak current mode control with load depended variable frequency operation. A novel start-up circuit is designed to prevent voltage overstressing of the devices. The high-frequency (~5Hz) operation of the switched capacitor stage helps to reduce the required flying capacitor; this was important as the flying caps dominate the total capacitance in the hybrid topology. A test-chip is designed and taped-out in 130nm CMOS to study the characteristics of the hybrid converter (Fig. 1). The test-chip includes on-chip decoupling capacitors to minimize the effect of high-frequency noise due to bond wires. The maximum conversion ratio is 16 (4.8V input to 0.3V output).

Measurement Results: The test-chip was measured to ensure functionality and characterize performance (Fig. 2). The measurements demonstrate the hybrid topology can use low-voltage devices for down-converting input voltages much larger than the device breakdown voltage. The measured peak efficiency was 69%.



Package Type	LCC-28 Pin
Package Size	130 mm²
Bondwire Inductance	1.897nH
Bondwire ESR	72mΩ
C_{FLY}	100nF ESR:20mΩ
C_{OUT_SC}	1μF ESR:100mΩ
C_{OUT_BUCK}	1μF ESR:100mΩ
L_{BUCK}	2.2μH ESR:150mΩ
On-chip Decap	500pF

Figure 1: The die-photo and component specifications of the hybrid converter test-chip.

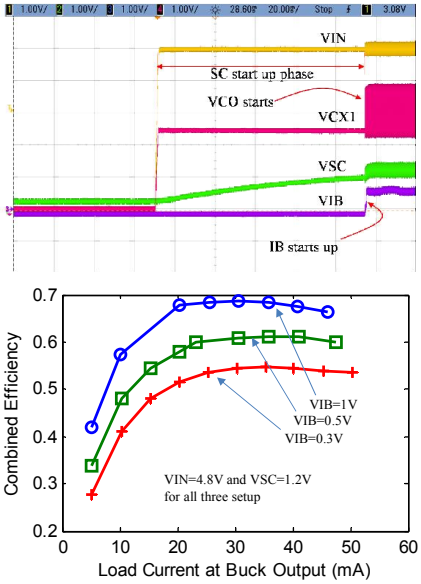


Figure 2: The measurement results showing start-up and efficiency of the hybrid regulators.

Keywords: Integrated converters, hybrid conversion, efficiency, high conversion ratio, packaging

INDUSTRY INTERACTIONS

Intel, IBM, Texas Instruments

MAJOR PAPERS/PATENTS

[1] M. Kar, et. al, "A Scalable Hybrid Regulator For Down Conversion of High Input Voltage Using Low Voltage Devices," submitted to IEEE Transaction on Power Electronics.

[2] M. Kar, et. al, "Impact of Process Variation in Inductive Integrated Voltage Regulator on Delay and Power of Digital Circuits," ISLPED 2014.

TASK 1836.112, SHORTSTOP: FAST POWER SUPPLY BOOSTING

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DENNIS SYLVESTER, UNIVERSITY OF MICHIGAN

SIGNIFICANCE AND OBJECTIVES

Shortstop was previously demonstrate in wirebond [1], but for high-performance applications a flip-chip design is proposed. Controlled-collapse chip connects (C4) are used to interconnect flip-chips with packages. C4 has lower parasitics than wirebond, and therefore we propose a better architecture compatible with C4. We also propose an automatic tuning algorithm.

TECHNICAL APPROACH

An important goal of the Shortstop C4 architecture is improved power delivery. A bottleneck of the wirebond prototype was centrally located power switch headers and footers, which required longer power stripes and a weaker power grid than a traditional design would require. This led to increased IR drop in the power delivery network. To remedy this, Shortstop C4 distributes the power switches across core area on a chip, not unlike standard power gated designs. The switch architecture was redesigned to reduce metallization and number of switches over cores. We also implemented an automatic tuning scheme, where previously delay chains had to be tuned by hand while observing Shortstop results using on-chip samplers.

SUMMARY OF RESULTS

The Shortstop architecture was improved to reduce the number of headers required in the core area and metallization usage in the power grid by contained Vcap and Vdirty power grids within the shared boost block instead of over the core area (Figure 1). Instead an intermediate on-chip Vboost supply is distributed over core areas, which is connected between the boost capacitor and dirty supply within the boost block. This reduces the need for one PMOS head in the core areas at the cost of two PMOS headers in the shared boost block. However, since there are many more cores than shared boost blocks less area is consumed with the core area for power switches.

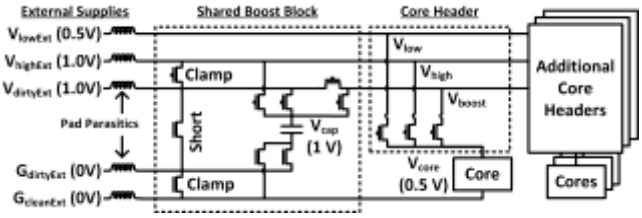

Figure 1: Improved Shortstop architecture.

An analog mixed signal simulation of the automatic tuning algorithm is shown in Figure 2. As this simulation was to validate the algorithm, an arbitrary voltage/timescale was used to match behavioral Verilog with the Spice netlists. However, it shows the tuning algorithm working to minimize boost latency. The core starts by being switched from Vlow to Vhigh directly. After the first steps the core is being switched from Vlow to Vdirty to Vhigh, but before parasitic inductance energize and charge share. This acts as a baseline and in simulation is 65 arbitrary units, denoted as "After First Seek" in Figure 2. The simulation then continues by increasing inductive energize and charge share times. The middle two plots in the figure show the final optimized timings with and without *reversing*, which means the algorithm tries to avoid local minimas. The latency was reduced by approximately 40% from the baseline, for 36 to 40 arbitrary units. The bottom plots in Figure 2 show minimal droop on Vhigh compared to the drop of switching from Vlow to Vhigh directly.

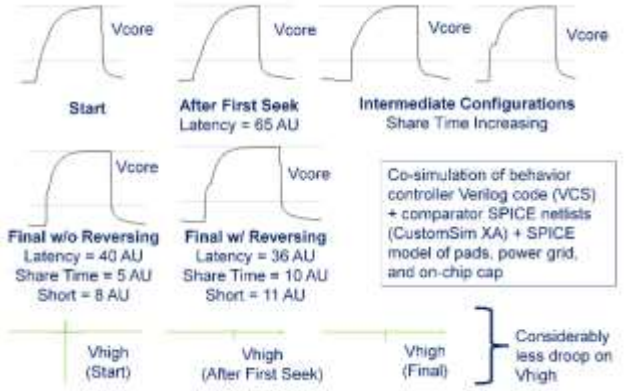

Figure 2: Shortstop C4 tuning simulation. The analog mixed signal validates function of the automatic tuning algorithm to reduce boost latency.

Keywords: Power supply boosting, timing generation, near-threshold computing, dark silicon, dim silicon.

INDUSTRY INTERACTIONS

IBM, Intel

MAJOR PAPERS/PATENTS

[1] N. Pinckney, M. Fojtik, B. Giridhar, D. Sylvester, and D. Blaauw, "Shortstop: An On-Chip Fast Supply Boosting Technique," *IEEE Symposium on VLSI Circuits*, June 2013.

TASK 1836.115, ANALYSIS AND CHARACTERIZATION OF SWITCHED-MODE DC-DC POWER CONVERTERS

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SIGNIFICANCE AND OBJECTIVES

Accurate modeling of DC-DC converters is indispensable for fast design and analysis. Existing PWM converter models have one or several limitations including negligence of key device-level non-idealities, inaccuracy and inflexibility. The goal of this work is to develop a PWM DC-DC converter model that addresses the above challenges.

TECHNICAL APPROACH

We have developed an accurate PWM DC-DC converter model that captures the essential device-level non-idealities such as the forward voltage drop of diode and on-resistance and leakage current of the MOS switch. A nonlinear multi-harmonic approach is taken to model the nonlinear responses of the targeted converter up to a specified order. Our model is general and flexible in the sense that it is applicable to all major converter types including buck, boost, and buck-boost converters. Our model can also smoothly transition between the CCM and DCM operating modes on the fly, making it well suited for low-power converters [1].

SUMMARY OF RESULTS

The proposed PWM DC-DC converter model combines the accuracy of enhanced state-space averaging with the flexibility of PWM switch models and the multi-frequency nature of the generalized models. The proposed model has several salient advantages.

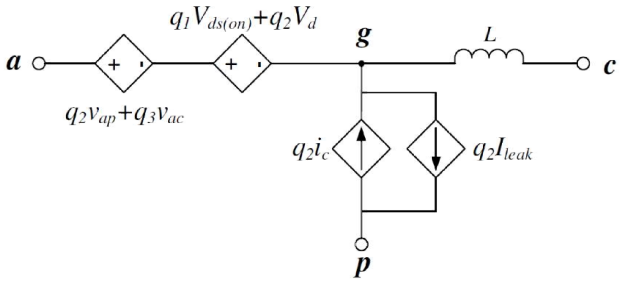

Figure 1: The equivalent model of switch cell with nonlinear device characteristics.

First, the model approximates the actual converter responses by multiple harmonics of ripples up to an arbitrary degree. Second, the model accounts for the effects of device nonlinearities, such as the forward voltage drop of the diode and on-resistance of the MOS switch. Figure 1 illustrates the structure of the proposed model which considers key device-level non-idealities. In addition, an efficient method is provided to evaluate these nonlinearities during the simulation.

The third advantage of the model lies in its generality. Similarly to the PWM switch model, our proposed model is based on the switch cell and can be readily applied to many DC-DC converters including buck, boost and buck-boost converters. It is also general in the sense that both CCM and DCM operations are supported. Finally, the proposed is not only accurate but also efficient. As a result, when applied to several open-loop and closed-loop DC-DC converters, the proposed model generates almost identical responses as the transistor-level simulations with a run-time speed-up of up to one order of magnitude.

Fig. 2 compares our model with respect to transistor-level circuit simulation and the conventional state-space averaging based model for the case of the open-loop simulation of a buck converter. It can be seen that our model provides a response that is almost identical to the transistor-level circuit simulation, capturing both DC and ripples of the converter output accurately.

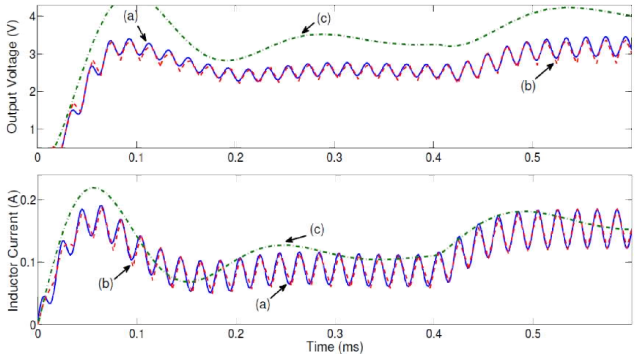

Figure 2: Boost converter model comparison: (a) proposed, (b) transistor-level simulation, and (c) conventional state-space averaging.

Keywords: PWM, DC-DC Converters, DCM, CCM, Modeling, Device non-idealities

INDUSTRY INTERACTIONS

Texas Instruments, Freescale

MAJOR PAPERS/PATENTS

[1] Y. Wang et al., "Multi-Harmonic Nonlinear Modeling of Low-power PWM DC-DC Converters operating in CCM and DCM," submitted to IEEE/ACM ICCAD, Nov. 2015.

TASK 1836.116, EFFICIENT PA ARCHITECTURES FOR POWERLINE COMMUNICATIONS

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SIGNIFICANCE AND OBJECTIVES

Using power lines for communications is highly attractive for several end applications, since in principle, this communication medium allows for cost-effective reuse of existing infrastructure. This research addresses the design of power efficient transmitters for powerline communication systems that support data rates up to several hundreds of kbps.

TECHNICAL APPROACH

A PWM-based design is employed in the transmitter implementation. Critical performance considerations including efficiency, linearity, and spurious emissions are addressed as part of the design. Circuit techniques that ensure power delivery with the relatively low supply voltage allowed in CMOS processes are utilized. To support the signal bandwidths, the switching frequency required of the PWM generator can be of the order of several tens of MHz. A PLL-based PWM generator that avoids the requirement for a ramp and high-speed analog comparator is thus employed in the architecture.

SUMMARY OF RESULTS

The transmitter architectures are aligned with standards defined by CENELEC, FCC and ARIB. The proposed design for wide-bandwidth PLC targets a frequency range of 154-487 kHz with an output signal level of up to 1.6 Vrms in a 10 Ω load. The THD+N requirement beyond the signal band is better than -60 dB. The transmitter is designed to operate with a high peak-to-average ratio (PAR) of the order of 6-10 dB. A switching-amplifier based design is employed, since it can ensure better efficiency over the amplitude range.

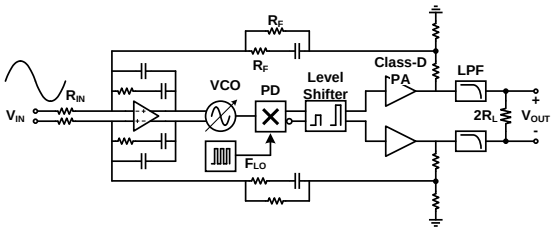

Figure 1: PLL-PWM architecture

A PLL-PWM approach has been designed in a 130 nm CMOS process for the high-bandwidth system (Fig. 1). PWM architectures employing a ramp signal and a comparator are impractical for applications that require high switching speed and good THD (~ - 60dB). This is the case because implementing a precise ramp signal and a high-speed comparator over several tens of MHz is extremely challenging. Therefore, a PWM architecture based on phase-locked loop (PLL) is employed since it allows for high-speed operation [1].

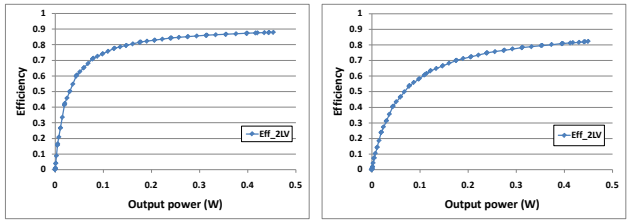

Figure 2: PA simulation results with DC input (Fsw= 60/200 Mz)

A Class-D PA is employed to enhance efficiency at back-off. The simulated peak efficiency of the PA in this design is 88 % when the output power is 450 mW, and the efficiency remains over 70 % until the output power is reduced to under 70 mW at 60 MHz operation frequency. Although the efficiency is slightly reduced when the reference frequency is increased, it still shows significantly better performance compared to a linear-mode PA and can further relax the external filter.

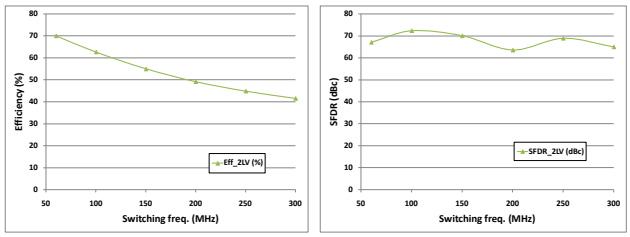

Figure 3: Full simulation results with sinusoidal input

The design is simulated with a 500 kHz sinusoidal input signal (3 dB PAPR) to verify the maximum frequency of the wide-bandwidth PLC application. The peak efficiency of the driver is 70 % at 60 MHz operation frequency. The SFDR is simulated to be greater than 60 dBc regardless of operation frequency.

Keywords: PWM, powerline transmitters, switching mode PAs, class-D PA, power line communications

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] J. Lu et al., “A CMOS class-D line driver employing a phase-locked loop based PWM generator,” IEEE Journal of Solid State Circuits, vol. 49, pp. 729–739, March 2014.

TASK 1836.118, LOW NOISE, LOW RIPPLE FULLY INTEGRATED DC-DC CONVERTERS FOR SIGNAL CHAIN APPLICATIONS

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SIGNIFICANCE AND OBJECTIVES

Fully integrated isolated DC-DC converters are an essential component in power monitoring, biomedical, and motor control applications where ground isolation is required. Compare to bulky discrete transformers, fully integrated transformer based approaches have advantage over reliability, weight, size and noise performance and are more suitable for high precision mixed signal applications.

TECHNICAL APPROACH

In this project, isolated converters that can be integrated with mixed signal building blocks, such as current monitors, ADCs and telecommunication modules will be developed. This converter utilizes an integrated coreless micro-transformer which is driven resonantly at around 100MHz to achieve efficient energy transfer. A peak power point detection method is developed to ensure system operate at optimum frequency while spread spectrum technique is also utilized to realize EMI noise reduction. Not only transformer, full bridge driver, Schottky diodes rectifier, voltage regulator and noise sensing cells are also integrated on the same chip.

SUMMARY OF RESULTS

The fully integrated isolated DC-DC converter utilizes an on-chip transformer to transfer power source across a ground isolation boundary. At secondary side, in order to make rectifier act fast enough for >100 MHz signal, passive type rectifier should be used. An LDO is also utilized to regulate output to high precision voltage.

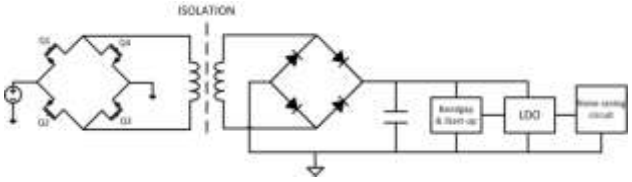

Figure 1: Power transfer block diagram

The Coreless on-chip transformer is a key part of our DC-DC converter. Before fabrication, a transformer 3-D model is analyzed in ANSYS HFSS software. After fabrication, on-chip transformer is mounted on a PCB board and characterized by a network analyzer. Result shows its inductance is higher than the model simulation value and the coupling factor is lower than the simulation value. These differences are due to PCB off chip routings.

For better power transfer efficiency, a series type resonant tank is used to replace a parallel type. Only current flows through the transformer primary side coil can be transferred to the secondary side. A series type resonant tank can force all H-bridge current pass through the inductor, while a parallel type cannot.

On chip EMI noise sensing cells are also added for the second prototype chip. The on-chip EMI noise distribution information can give directions on placing sensitive circuits near the quiet region. A traditional sample and hold noise capture cell cannot differentiate actual noise at certain location and routing noise. To solve this issue, a ring oscillator is used for sensing. It operates at much higher oscillation frequency f and noise frequency is at f_{noise}. These two frequencies mix together and noise information is shown at $f \pm f_{noise}$. Noise information can be obtained by using spectrum analyzer.

Fully integrated version chip is also fabricated. Figure 2 shows the die photo as well as PCB board with packaged chip on board.

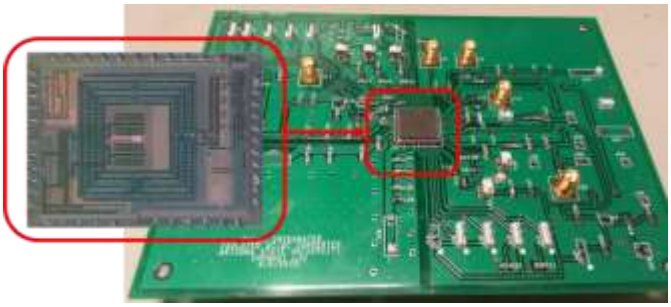

Figure 2: Fully integrated chip mounted on PCB board

Basic chip function test shows the converter can perform the power transfer function across the isolation barrier. The peak power transfer frequency unit works well to find the optimum power transfer frequency. This frequency is around 110MHz which is close to the design target. The rectifier is fast enough for such a high frequency signal. More chip characterization will be done during in the future.

Keywords: EMI, DC-DC, transformer, isolate

INDUSTRY INTERACTIONS

Texas Instruments

TASK 1836.123, TEST TECHNIQUES AND FAULT MODELING FOR HIGH VOLTAGE DEVICES AND BOARDS

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SIGNIFICANCE AND OBJECTIVES

Our project objectives are 1) develop physics-based fault models for LDMOS transistors, 2) develop parasitic device models, 3) modify ATE load boards for high voltage discharge problems, and 4) provide novel low-cost test techniques for high voltage LDMOS devices.

TECHNICAL APPROACH

Lateral DMOS transistors are used in various applications. We have identified new crystal lattice defects in LDMOS transistors. Using positive and negative gate bias voltages, we were able to identify p and n region defects of LDMOS. We worked on computing a multiplication factor (M) to identify defects easily. We evaluated several LDMOS parts to prove our testing techniques. We proved that the simulated results were in good agreement with experimental results with high-voltage apparatus developed in our laboratory. We are continuing to enhance our HVPro software tool to test DIB automation and reduce high-voltage testing to protect personnel.

SUMMARY OF RESULTS

In the previous reporting period, we prototyped a new noise reduction scheme to measure in the nano-amp range. Hardware test measurement apparatus was built to implement the noise reduction scheme [1]. We have developed a low-cost test technique to reduce the Avalanche breakdown voltage. We performed extensive simulations based on the parasitic devices using our fault models. We developed a closed form mathematical expression to describe the LDMOS drain current.

During this reporting period, we have identified a new crystal lattice defect in LDMOS. We developed a new testing scheme to reduce the high Avalanche voltage by applying positive and negative gate bias voltages to diagnose defects in LDMOS transistors. The testing scheme involves applying a positive gate voltage to find p-well defects and a negative bias voltage for n-drift defects. We also provided the Avalanche multiplication factor expression to understand the figure of merit for breakdowns. This expression was useful to see the Avalanche voltages for different LDMOS drivers.

When we applied positive gate bias voltage to the device, we were able to reduce the testing drain voltage down to 400 volts for a 900 volt device. The phenomenon called snapback occurred with the same behavior using a lower breakdown voltage indicated that there is a correlation between the high and low snapback voltages. In fact, we were able to control the snapback voltage which occurs in the Avalanche as shown in Fig. 1 with different gate voltages from 0 to 1.17 volts.

A negative bias technique provides a promising diagnostic tool to find defects in n-drift region of LDMOS. Using this technique, we were also able to reduce the testing voltage down to 400 volts for conventional 900V device.

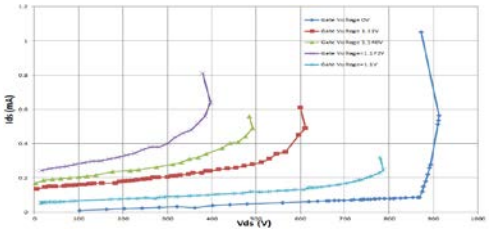

Figure 1: Measurements of LDMOS Drivers with Positive gate Bias Voltages which Reduced Avalanche Voltage Levels.

We have developed other testing methods to reduce the high Avalanche voltage using waveform stimulus and temperature variations. Fig. 2 shows the total LDMOS test algorithms.

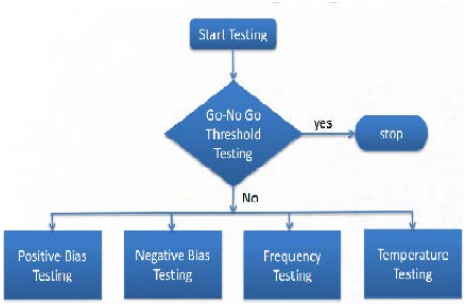

Figure 2: LDMOS Driver Test Algorithm.

Keywords: LDMOS, Structural defects, avalanche voltage, fault model, high voltage

INDUSTRY INTERACTIONS

Texas Instruments, GlobalFoundries

MAJOR PAPERS/PATENTS

[1] Patent: US 8,742,777 B2, "Method and System for testing an Electric Circuit," awarded on June 3, 2014.

[2] B. Kim, S. Mondal, F. Taenzler, K. Moushegian, "A Novel BIST Technique for LDMOS Drivers," Invited Paper in BIST Special Session, *IEEE 57th Midwest Symposium on Circuits and Systems*, College Station, TX, August 2014.

TASK 1836.124, STUDY AND ANALYSIS OF FAST POWER-ON CLOCK MULTIPLIERS IN THE PRESENCE OF PVT VARIATIONS

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SIGNIFICANCE AND OBJECTIVES

Inactivity periods in energy proportional wireline or wireless links can be of the order of few milliseconds or higher. Temperature or voltage variations during this idle period could cause frequency drift in an oscillator which cannot not be corrected by the integral path in nanoseconds time frame. Objective is to make fast power-on-lock frequency multipliers resilient to such errors.

TECHNICAL APPROACH

Proposed research sets out to explore clock multiplying architectures resilient to voltage and temperature variation during off-state by understanding the effect of temperature and voltage variations in an LC oscillator, and designing a fast power-on-lock LC-PLL architecture which is immune to these variations; and achieving immunity by cancelling temperature sensitivity of an LC oscillator with the help of a temperature sensor and a look up table approach.

SUMMARY OF RESULTS

Measured temperature sensitivity of an LC oscillator is approximately -80ppm/deg. A look up table (LUT) based approach is used (Fig. 1). In this approach, LUT maps the die temperature to a frequency control word, which brings the oscillator to the desired frequency at the time of power-on. Conventional PLLs rely on feedback action to force $\Delta\Phi = 0$, and as a result have long lock time. In this work, we seek to reduce lock time by making $\Delta\Phi = 0$ on power-on without using the PLL feedback. A replica of DCDL and divider in REF_{DEL} path helps to maintain phase alignment even in the presence of voltage and temperature variations during long power-off periods. Absolute phase drift of PLL output indicates that proposed phase calibration reduces the PLL lock time to < 1ns and the phase drift to ±3ps (Fig. 2). The capture span is approximately 2-3 time constants of the PLL loop and beyond this span. PLL feedback ensures that the phase doesn't drift beyond ±3ps. With 100mV of DLL supply variation during power-off state, error in the phase drift is less than 2ps. (Fig. 3a). Measured power-on transient of PLL is shown in Fig. 3b.

Keywords: Fast power-on-lock, PLL, LC

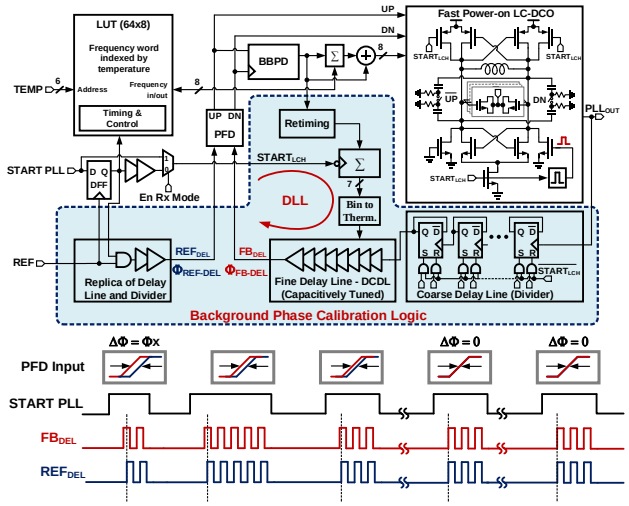

Figure 1: Schematic and timings of fast power-on-lock LC PLL

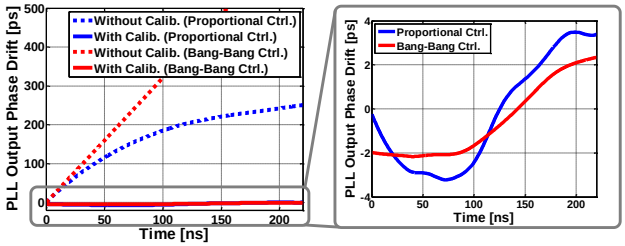

Figure 2: Measured PLL phase drift after 1ns of power-on.

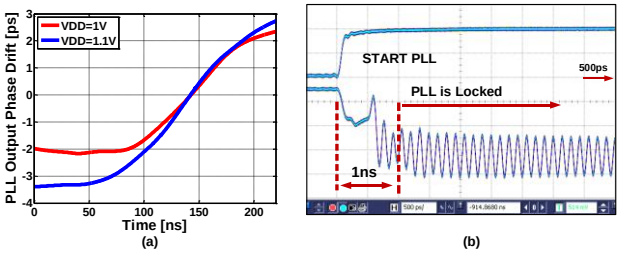

Figure 3: (a) Measured PLL phase drift with 100mV change in the supply of DLL during the off-period. (b) Measured power-on transient of PLL.

INDUSTRY INTERACTIONS

Texas Instruments, Intel, AMD

MAJOR PAPERS/PATENTS

[1] T. Anand *et al*, ISSCC 2015.

[2] T. Anand *et al*, JSSC (under review).

TASK 1836.130, BUILT-IN SELF-TEST TECHNIQUES FOR TEST, CALIBRATION, AND TRIMMING OF POWER MANAGEMENT UNITS: PMU-BIST

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SIGNIFICANCE AND OBJECTIVES

This project aims at development of small-footprint adjustable zoom-ADCs for the on-chip measurement of bandgap reference voltage and development of full loop characterization approaches for PMU/PMIC loops to test, track, and calibrate dynamic performance.

TECHNICAL APPROACH

For the DC measurement approach, we rely on a VCO based converter. VCO converts a DC signal to frequency. Conversion is typically non-linear but within a certain range, linearity can be achieved. The linear range of voltage-to-frequency conversion needs to be carefully adjusted. The slope of voltage-to-frequency conversion determines the sensitivity. Frequency can be measured in two ways: (a) simple on-chip counter with an enable window, and (b) sigma-delta oversampling based approach that converts frequency to phase and measures phase.

SUMMARY OF RESULTS

The target BGR for our application yields a reference voltage around 1.25V. Process variations cause 25% uncertainty in this value. Hence, with a reasonable margin, the overall range of interest for our implementation is 850mV-1.65V. We would like to obtain 13 bits resolution with respect to the 1.65V FS voltage; hence 200µV LSB. The ADC is intended to be used to measure the voltage of several BGR circuits on-chip.

In order to evaluate the performance of the zoom-in ADC, we have implemented two versions. First, we implemented the basic VCO together with the counter using the 0.5-µm single-well CMOS technology. We aimed to limit the digital signal frequency to around 10MHz. The VCO is designed with 7 stages to achieve the frequency target. The frequency step for this VCO is around 8kHz. We used a 15-bit counter to accommodate the opposite process corner for faster VCOs. Total area of the ADC is 0.031 mm^2.

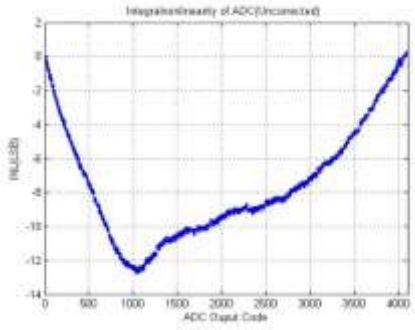

Figure 1: INL of the un-calibrated ADC

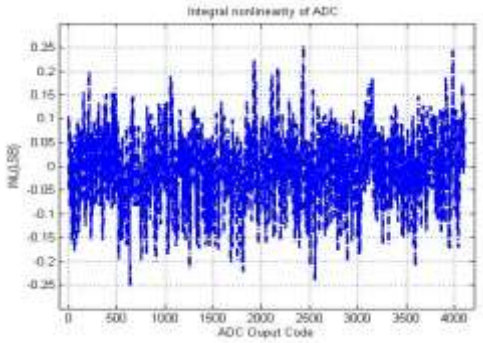

Figure 2: INL of the proposed zoom-in ADC with 4 adaptive calibration inputs (Hardware measurements with 0.5µm)

We then calculate the maximum deviation of the actual ADC response from the approximated curve. Figure 1 shows the INL of un-calibrated ADC. The INL is as large as 13LSB, corresponding to 2.7mV. With the zoom-in approach, the INL of the ADC can be reduced to 0.25LSB, corresponding to 50µV. The INL per code of the proposed ADC is shown in Figure 2. The trade-off is the increase in the test time from 3ms to 5ms, which is negligible.

Keywords: LDO, DC-DC converter, BGR, self-test

INDUSTRY INTERACTIONS

Texas Instruments, India, Freescale

MAJOR PAPERS/PATENTS

[1] N. Beohar, P. Bakliwal, S. Roy, D. Mandal, B. Bakkaloglu, and S. Ozev, “Disturbance-free BIST for Loop Characterization of DC-DC Buck Converters”, IEEE VLSI Test Symp., 2015 (Nominated for best paper award).

[2] O. E. Erol, S. Ozev, C. Suresh, R. Parekhji, and L. Balasubramanian. "On-chip measurement of bandgap reference voltage using a small form factor VCO based zoom-in ADC." IEEE Design, Automation & Test in Europe Conference, pp. 1559-1562, 2015.

[3] L., Tao, C. Fu, S. Ozev, and B. Bakkaloglu. "A built-in self-test technique for load inductance and lossless current sensing of DC-DC converters." IEEE VLSI Test Symposium (VTS), 2014 (Received best paper award).

TASK 1836.133, ENERGY EFFICIENT SIGNAL PROCESSING TECHNIQUES FOR SMART GRID HETEROGENEOUS COMMUNICATION NETWORKS

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BRIAN L. EVANS, UNIVERSITY OF TEXAS AUSTIN, BEVANS@ECE.UTEXAS.EDU

SIGNIFICANCE AND OBJECTIVES

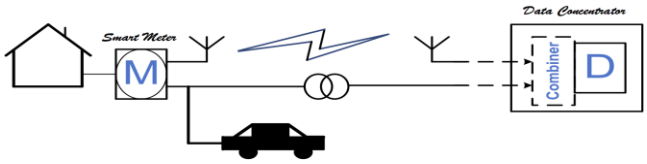
Within a smart grid (SG), we seek to enable reliable and high-speed communications for better monitoring and control of energy usage. We focus on "last mile" bi-directional communications from a concentrator to smart meters using orthogonal frequency division multiplexing (OFDM) based power line communications in the 3-500 kHz band and wireless communications in the unlicensed 902-928 MHz band.

TECHNICAL APPROACH

Performance of narrowband PLC is limited by non-Gaussian interference dominated by periodic impulsive noise. We propose a time-frequency modulation diversity scheme at the transmitter and a diversity demodulator at the receiver robust to combat periodic impulsive noise in narrowband PLC, thus enhancing communication reliability without decreasing data rates.

To further enhance SG communications reliability, we propose PLC/wireless receive diversity combining schemes under the impulsive interference variations over the two links. Assuming OFDM transmissions for both links, we analyze the performance gains using simultaneous data transmission and diversity reception over the 3-500 kHz NB-PLC and the unlicensed 902-928 MHz wireless bands.

SUMMARY OF RESULTS



We investigated the maximal ratio-combining (MRC) scheme for combining the output signals of the NB-PLC and wireless links. The MRC scheme combines the log-likelihood ratios (LLRs) of the received bits over the two links by weighting each link with its SNR. We proposed two techniques for the weight selection; one technique is based on instantaneous SNRs and another technique is based on the noise power spectral density. We showed that, due to the impulsive nature of the interference on both links, the proposed techniques provide better bit error rate (BER) than using the average SNRs when computing the MRC weights.

In addition, we proposed a time-frequency modulation diversity technique to improve transmission robustness in periodic impulsive noise without decreasing data rates. The time-frequency modulation diversity transmitter jointly encodes multiple bits to multiple PSK symbols, and allocates them to different subcarriers in various OFDM symbols (Figure 1). It can be embedded into existing narrowband PLC standards.

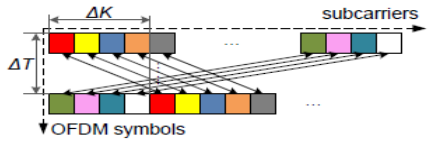


Figure 1: An example of time-frequency modulation diversity. Components of a length-2 modulation diversity code (marked in the same color) are allocated to 2 subcarriers separated in both time and frequency.

At the receiver side, we design a diversity combining demodulator that linearly combines the signals received from the corresponding sub-channels/OFDM symbols with weights inversely proportional to the sub-channels' SNRs. The periodically varying noise power spectrum can be estimated offline based on noise measurements during no-transmission intervals. Alternatively, it can be estimated primarily during data transmission by exploiting its sparsity in the frequency domain and applying sparse Bayesian learning algorithms. In simulations, our proposed transceiver methods achieve 100-1000x reduction in coded BER, while maintaining the same data rates, compared to a conventional NB-PLC system.

Keywords: smart grids, power line and wireless communication, diversity, periodic impulsive noise.

INDUSTRY INTERACTIONS

Texas Instruments, Freescale Semiconductor

MAJOR PAPERS

[1] M. Sayed, Ghadi Sebaali, Brian L. Evans and N. Al-Dhahir, "Efficient Diversity Technique for Hybrid Narrowband-Powerline/Wireless Smart Grid Communications", Invited paper to the 2015 IEEE SmartGridComm. Conference.

[2] M. Sayed, I.-H. Kim, T. Pande, A. Batra and N. Al-Dhahir, "Proposed Frame and Preamble Structure for MIMO Narrowband Power Line Communications" in Proc. 2015 IEEE ISPLC.

TASK 1836.138, MICRO-POWER ANALOG-TO-DIGITAL CONVERTERS

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SIGNIFICANCE AND OBJECTIVES

Micro-power data converters are key components of RFIDs, as well as sensor interfaces needed in medical and environmental applications. Our research develops novel algorithms and architectures for analog-to-digital data converters (ADCs) required in such applications. They are based on incremental data conversion.

TECHNICAL APPROACH

Incremental data converters (IDCs) are highly efficient micro-power ADCs. They are Nyquist-rate ADCs, which utilize noise shaping to obtain accurate output words. Their performance may be enhanced by cascading one or more ADC stages, creating *extended-counting data converters* (EDCs). Our research is on the study, design and implementation of novel micro-power ADCs, particularly IDCs and EDCs, with improved performance. We have already obtained high efficiency power and performance scalable ADCs high dynamic range analog front ends for sensors, including those used in wearable health monitors.

SUMMARY OF RESULTS

A recently developed EDC, which performs as a three-step convertsion is shown in Fig.1.

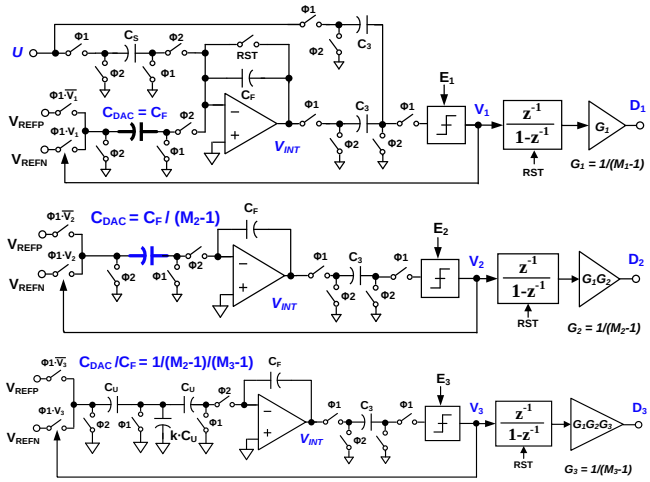

Figure 1: Three-step extended-counting architecture for incremental data conversion.

If the step *i* lasts for M_i clock periods, the final signal-to-quantization noise of the ADC can be estimated from $SQNR \approx 20\log(M_1 \cdot M_2 \cdot M_3)$. For example, OSR=160 (128+16+16) gives SQNR = 90 dB, and OSR = 320 (256+32+32) will result in SQNR = 108 dB SQNR. Fig. 2 illustrates the signal-band spectra for M_1 = 256, M_2 = M_3 = 32.

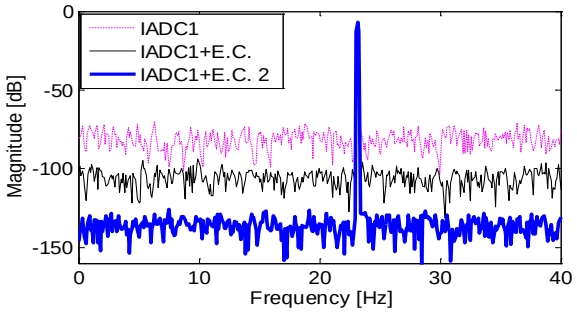

Figure 2: Signal-band spectra of the three-step IDC.

A two-step 3+2 IDC is illustrated in Fig. 3.

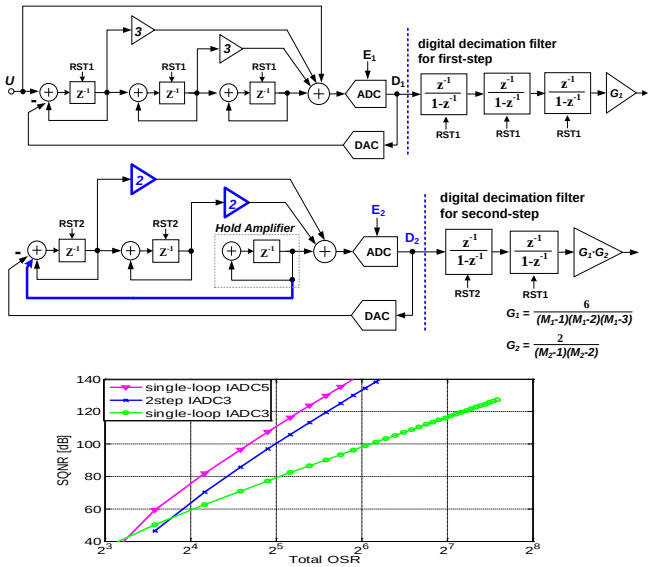

Figure 3: Two-step IDC, and its SQNR comparison with single-loop IDCs.

Keywords: Micro-power A/D, incremental ADC, extended counting ADC, sensor interface, data converter

INDUSTRY INTERACTIONS

Texas Instruments, Freescale

MAJOR PAPERS/PATENTS

[1] Chen, C-H et al., "A micro-power two-step incremental analog-to-digital converter ," IEEE J. of Solid-State Circuits, vol.50, no. 8, Aug. 2015.

[2] Chen, C-H, He, T. and Temes, G.C. "Micro-power incremental ADCs," Proc. Advances in Analog Circuit Design (AACD) Workshop, 2015, pp. 1- 19.

TASK 1836.139, ENABLING FULLY-INTEGRATED VHF CLK-SYNC MULTIPHASE SWITCHING REGULATORS ON SILICON

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SIGNIFICANCE AND OBJECTIVES

Voltage regulators in advanced SoCs systems are demanded to achieve transient speed and power density. Therefore, there has been a need for VHF (30-300 MHz range) multiphase switching regulators. In this project, the PI plans to investigate three major issues: high speed feedback control, clock synchronization and system miniaturization.

TECHNICAL APPROACH

To overcome the above issues and to ensure proper operation of the proposed regulator at VHF, a current-mode zero-delay hysteretic controller is proposed. By using particular characteristics of the proposed controller with a new and accurate, high speed, low-power current sensor, it imparts the fast transient response. Meanwhile, in order to implement interleaved multiphase switching regulators, a simple clock synchronization technique is proposed. It maintains fixed switching frequency based on the hysteretic control. Moreover, from the perspective of system implementation, on-chip magnetic and 3D integration structures are expected to miniaturize the system.

SUMMARY OF RESULTS

To overcome the challenge of the current sensor that operates at VHF, the PI proposes an emulated AC+DC current sensing scheme in Fig. 1(a). The idea is to split the inductor current, I_L, into an average (DC) component and AC ripple part, to amplify each independently, and then to recombine these two. Details on the operation can be explained using Fig. 1(b).

At first, the proposed sensor implements a simple low-power current conveyor circuit to amplify the average I_L, I_{L_AVG}. This is because I_{L_AVG} cannot change rapidly compared with the AC ripple part of I_L owing to physical I_L slew limit. Meanwhile, the voltage of AC ripple, V_{AC}, can be amplified by another passive RC filter. At last, the amplified DC average and AC ripple parts are recombined by coupling V_{AC} into V_{SENS} node through C_C.

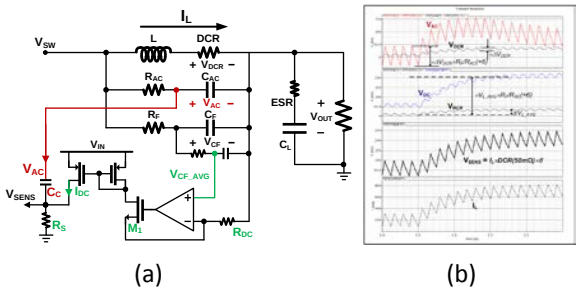

Figure 1: proposed high-speed AC+DC current sensing circuit: (a) Circuit diagram, (b) Simulation results

In Fig. 2, the PI proposes a current-mode zero-delay hysteretic control for fast transient response and clock synchronization. This zero-delay scheme adaptively adjusts its hysteretic window size. During the charge period (DT), the window size should be as wide as necessary for clock synchronization. However, in the course of the discharge period ((1-D)T), hysteretic window is close to zero for delay-less response. To explain details of the operation, first, in the steady state, V_{SENS} rises from V_L during the DT until it hits V_{HYS}. The moment of intersection between V_{SENS} and V_{HYS} determines the start of (1-D)T, and V_{SENS} falls from V_H. During (1-D)T, V_{HYS} down tracks with the same slope of V_{SENS} creating a near zero hysteretic window. Thus, when a load step-up occurs, V_H is rising due to drop in V_{OUT}, and then V_{SENS} can exit hysteretic boundary, achieving quicker system response.

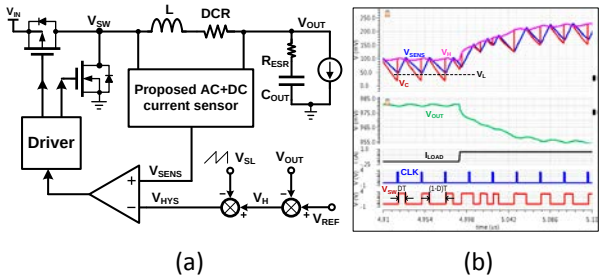

Figure 2: Proposed current-mode zero-delay hysteretic control circuit: (a) Block diagram, (b) Simulation results.

In the following year, by taking advantage of the proposed current-mode zero-delay hysteretic control, a simple clock synchronization technique that achieves cycle-by-cycle regulation in each sub-converter will be used to implement an interleaved multiphase topology.

Keywords: VHF switching converters, multi-phase operation, high-speed feedback control

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] M. Song et al., "A 6A 40MHz Four-Phase ZDS Hysteretic DC-DC Converter with 118mV Droop and 230ns Response Time for a 5A/5ns Load Transient," ISSCC Dig. Tech. Papers, pp. 80-81, Feb. 2014.

TASK 1836.140, EMBEDDED & ADAPTIVE VOLTAGE REGULATORS WITH PROACTIVE NOISE REDUCTION FOR DIGITAL LOADS UNDER WIDE DYNAMIC RANGE

ARIJIT RAYCHOWDHURY, GEORGIA TECH, ARIJIT.RAYCHOWDHURY@ECE.GATECH.EDU

SIGNIFICANCE AND OBJECTIVES

The primary goal of the project is to develop an integrated power flow architecture for fine-grained spatio-temporal voltage distribution and management in microprocessors and SoCs. We investigate through models, simulations, hardware development and experimentation novel control topologies and circuit techniques for efficient wide-dynamic range linear and switched capacitor voltage regulators (VR's).

TECHNICAL APPROACH

This project investigates power flow architecture in microprocessors and SoCs. This will include development of control models and corresponding circuits for digitally implementable integrated linear regulators for fine-grain power management. These models will be calibrated with Silicon implementation and measurements. In the second part of the project we will develop circuits and models for multiple-output switched capacitor voltage regulators for high efficiency and fine-grained spatial voltage distribution. Further, we will provide models and experimental verification of the interaction of VRs across multiple voltage domains both in terms of stability and cross-domain noise coupling.

SUMMARY OF RESULTS

In the last year of the project, we have developed key models to understand the performance and stability conditions of both discrete time and continuous time digital linear regulators. For discrete time regulators linearized models have been used in the z-domain to understand the role of sampling frequency and the output pole position on the overall system dynamics. We have established that over-sampling the system can lead to higher instability and can lead to large overshoots and prolonged ringing. This allows us to provide bounds on the sampling rate for a controlled output step response. Key elements of the designs have been implemented on a PCB and we have established the efficacy of the models. Further, a describing function based non-linear model has been established to understand the limit cycles in the steady state operation of the discrete-time linear regulators. These have also been verified through PCB and silicon (IBM 130nm) development. We have submitted multiple papers based on the results and they are at different stages of acceptance [1-5]. In addition to discrete time LDOs, we have also developed linearized models of continuous time LDOs. Work done jointly with Intel, suggest a PLL like behavior of the continuous-time, phase-locked LDOs and show the change in the gain margin as the output pole traverses a large dynamic range. It shows potential instability at light load conditions and provides key insights to the stability-performance trade-offs in such systems. The results have been presented in a joint publication with Intel [4]. We have also started a work on the multiple-output SCVR. We are currently working on the design of the different SCVR components and are planning to tape-out the key design in IBM 130nm in August 2015.

Keywords: Integrated Voltage Regulator, Low-Power Design, Digital Linear Regulators, Discrete Time Control, Continuous Time Control

INDUSTRY INTERACTIONS

Texas Instruments, Intel, IBM

MAJOR PAPERS/PATENTS

[1] Saad Bin Nasir, Arijit Raychowdhury , "On Limit Cycle Oscillations in Discrete-Time Digital Linear Regulators" presented at Applied Power Electronics Conference and Exposition (APEC), 2015.

[2] Saad B. Nasir andSamantak Gangopadhyay and A. Raychowdhury, "A 130nm fully digital linear drop-out regulator with adaptive control and reduced dynamic stability for wide dynamic range of operation," International Solid State Circuits Conference, February 2015.

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TASK 1836.142, LOW POWER APPLICATIONS OF FRAM

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SIGNIFICANCE AND OBJECTIVES

Compared to popular non-volatile-memory, flash, FRAM has significantly faster write access time, lower write energy, smaller peak current and orders of magnitude better endurance. This report details adiabatic design of Ferroelectric RAM (FRAM) that can reduce the write energy, especially when writing large blocks, which is one of the most common cases.

TECHNICAL APPROACH

The focus of our research is on ultra-low energy FRAM arrays for millimeter-scale sensor-networks. Millimeter-scale sensor-networks wake-up for short intervals, store sensor data, and transmit data intermittently, all with a very long battery life, requiring ultra-low energy non-volatile memories. Other applications like implantable medical devices and energy harvesting applications also have similar characteristics.

The objectives are to optimize FRAM for ultra-low-power operation. To achieve this we propose an adiabatic technique to write into the FRAM. By switching the bit-line (BL) and program-line (PL) capacitances by resonating them with an inductance, the energy is reduced significantly.

SUMMARY OF RESULTS

Figure 1 shows the FRAM array design with adiabatic write capability. To start the resonance PL is stepped to VDD/2, which leads PL0 to resonate between 0 and VDD.

To write new data into a row, the BLs are switched to data adiabatically by controlling the WREN and PLEN, i.e. the starting point and ending point for data '0' is 0 of PL0 and for data '1' is VDD of PL0. Each row needs one and a half cycle of resonance of PL0 to write a new data, with its word-line asserted. The resonance frequency is therefore 1.5x the write frequency. The WL signals are overdriven to (VDD+Vt) to compensate for the Vt drop across the NMOS access transistor.

To maintain the resonance amplitude, a continuous comparator based peak detector is used to monitor PL0. It generates pull-up (PU) and pull-down (PD) pulses to restore the amplitude of resonance at PL0.

Figure 2 shows, the write-energy per bit decreases for longer words in an array before stabilizing. Also, block write (writing multiple rows in series) decreases the write-energy per bit. Block write also amortizes the start-up energy for the resonance. Therefore, writing the whole array gives best energy numbers.

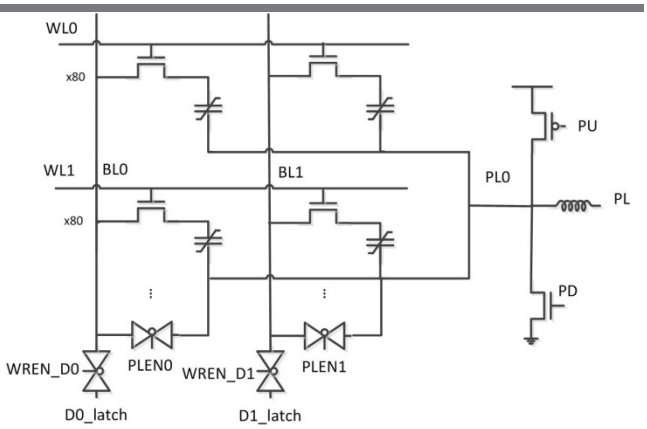

Figure 1: The proposed adiabatic design for FRAM array. Both BL and PL will transition adiabatically for saving energy

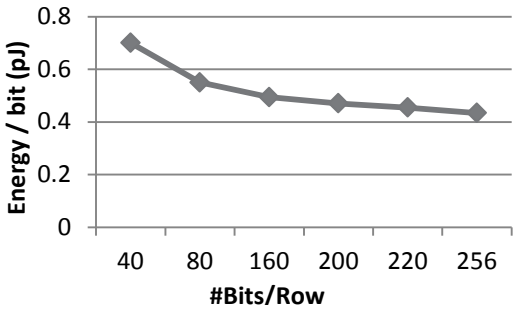

Figure 2: Write energy per bit for increasing number of columns, in an array with 256 rows.

The design supports sharing the inductor between multiple banks of FRAM. This allows us to use a single large discrete inductor.

The adiabatic design reduces write energy per bit by 7x. It also reduces the read energy per bit by 4x. These energy gains allow us to attain a very energy-efficient FRAM.

The circuit implementation of the adiabatic FRAM array has been accomplished. The next phase will involve physical design, test harness design and prototyping of the low-power FRAM.

Keywords: sensor-networks, NVM, FRAM, low-power, adiabatic

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

None

TASK 1836.143, DESIGN TECHNIQUES FOR MODULATION-AGILE AND ENERGY-EFFICIENT 60+GB/S RECEIVER FRONT-ENDS

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SIGNIFICANCE AND OBJECTIVES

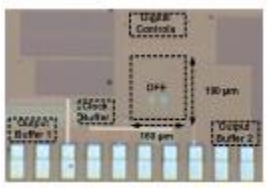
While high-performance I/O circuitry can leverage CMOS technology improvements, unfortunately the bandwidth of the electrical channels used for inter-chip communication has not scaled in the same manner. The high-speed serial link receiver design and modeling techniques proposed here aim to significantly improve interconnect bandwidth density in an energy-efficient manner.

TECHNICAL APPROACH

In order to investigate design trade-offs, a statistical-modeling framework will be utilized to investigate power-optimum equalization partitioning and modulation format for 60+Gb/s signaling environments. This tool will be used to guide the design of a new modulation-agile receiver front-end which includes a multi-level decision-feedback equalizer (DFE) with multiple IIR feedback taps for efficient long-tail ISI cancellation. Adaptive techniques will also be developed to tune key equalization parameters, such as DFE tap time constants/weights and CTLE settings.

SUMMARY OF RESULTS

While receivers with DFEs are now in wide use, architectures which employ a common FIR feedback filter require an ever-growing number of taps to cancel the long-tail ISI found in typical backplane channels. In order to address this, DFEs with IIR feedback filters have been implemented and shown to improve equalization efficiency for RC-limited and backplane channels. A key challenge associated with these architectures involves optimizing the critical IIR feedback path to allow for ISI cancellation beginning at the first post-cursor. Also, while the use of multiple IIR taps can provide for further ISI cancellation, the IIR tap number should be carefully chosen in order to avoid excessive area and power consumption. This project addressed these issues by



(a)

TABLE I: PERFORMANCE SUMMARY

Specification	This Work	[Kim 2007]	[Huang 2011]	[Shahramian 2012]
Data Rate	10 Gb/s	10 Gb/s	6 Gb/s	3.7 Gb/s
Architecture	2-IIR tap	1-IIR tap	1-IIR tap	3-IIR tap
Channel Loss @ Nyquist	35* dB	27* dB	32.7 dB	8 dB
Eye width BER PRBS Code	31 % 10^{-12} PRBS7	28 % 10^{-9} PRBS7	NA 10^{-12} PRBS7	6 % 10^{-12} PRBS7
Supply (V)	1	1	NA	1.2
Power (mW)	9.9	7	4	17.3
Area (mm²)	0.0304	0.0175	0.089**	0.0535
Technology	65-nm	65-nm	90-nm	130-nm

* Including ~2 dB of setup loss.
** Include the area of a whole receiver.

(b)

Figure 1: 10Gb/s DFE with 2 IIR taps: (a) GP 65nm CMOS prototype (b) performance summary.

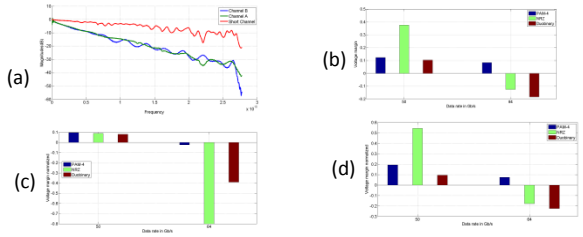


Figure 2: Statistical modeling of 50 and 64Gb/s systems: (a) Channel models with differing loss profiles. Normalized voltage margin for (b) Channel A, (c) Channel B, and (d) Channel C.

implementing a DFE which employs 2 IIR taps to allow for improved long-tail ISI cancellation [1]. Fabricated in GP 65-nm CMOS (Figure 1), the receiver occupies 0.0304 mm^2 area and consumes 9.9 mW while operating at a BER<10^{-12} for 10 Gb/s data passed over a 40-inch FR4 channel with 35 dB loss at 5 GHz.

Under this low BER requirements, transient simulations are impractical. In order to investigate this, this project continues to build upon the PI's statistical-modeling framework for high-speed serial links. This tool is utilized to investigate the optimal equalization partitioning and modulation format for 60+Gb/s signaling environments, relevant for applications such as 400Gb Ethernet. As shown in the 50 and 64Gb/s modeling results of Figure 2, the optimal modulation format is a function of the channel loss profile.

Utilizing more spectrally-efficient modulation that allows for longer unit interval times can relax timing, while also being potentially better suited for a specific channel loss profile, provided that DFE architectures are developed that are agile enough to support multiple modulation formats. To address this, a new high-speed modulation-agile receiver front-end which includes a multi-level decision-feedback equalizer with multiple IIR feedback taps for efficient long-tail ISI cancellation was developed and taped-out in GP 65nm CMOS.

Keywords: decision feedback equalizer, infinite impulse response (IIR) DFE, receiver, serial link

INDUSTRY INTERACTIONS

IBM, Texas Instruments

MAJOR PAPERS/PATENTS

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TASK 1836.144, HIGH-EFFICIENCY HIGH-VOLTAGE POWER CONVERTERS

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SIGNIFICANCE AND OBJECTIVES

This research aims to investigate novel soft-switching techniques, synchronous gate driving techniques, and control schemes to significantly advance power efficiency and power density of today's high-voltage DC-DC converters. These developed converter technologies help greatly lower the cost and the energy efficiency of renewable energy systems, telecom systems, automotive systems, etc.

TECHNICAL APPROACH

A quasi-square-wave (QSW) zero-voltage-switching (ZVS) isolated three-level half-bridge architecture is reported to enable high-voltage isolated converters achieving high power efficiency at high switching frequencies. An integrated synchronous three-level gate driver is also developed to ensure reliability of all eGaN power FETs under a wide input range from 110V to 250V and to reduce propagation delays for high-frequency converter operation. Implemented in a 0.7-µm 700V CMOS-LDMOS process, the proposed gate driver achieves ≤ 18ns propagation delays and enables a 250V 45W isolated three-level converter that achieves the peak power efficiencies of 94.2% and 89.1% at 1MHz and 2MHz, respectively.

SUMMARY OF RESULTS

Fig. 1 shows the structure of the proposed isolated QSW-ZVS three-level converter. Four power FETs M_1 – M_4 and a flying capacitor C_{FLY} connected between SW_1 and SW_3 form the three-level architecture on the primary side of the converter. M_1 and M_4 are driven complementary by input pwm_{14}, while M_2 and M_3 are driven complementary by pwm_{23}. AC current in magnetizing inductance (L_M) of the transformer charges/

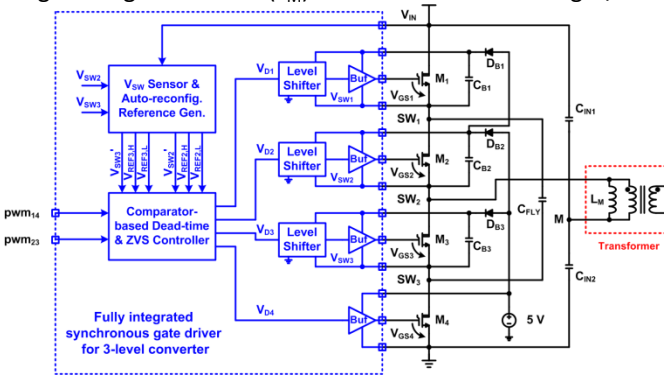

Figure 1: Structure of the proposed three-level synchronous gate driver for isolated QSW-ZVS converter.

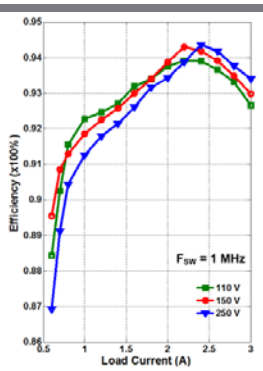

Table1: Comparisons of different HV gate drivers

	LM5113	IRS2011	This Work
High-side floating voltage (V)	100	200	250
Turn-on rising time (ns)	7	25	3
Turn-off falling time (ns)	1.5	15	3
Turn-on delay (ns)	28	60	18
Turn-off delay (ns)	26.5	60	18
Dead-time & ZVS controller	No	No	Yes, accurate
Power Stage	2-level	2-level	3-level

Figure 2: Simulated power efficiency.

discharges the parasitic capacitances of power FETs during the switching transitions to realize ZVS operation.

Implemented in a 0.7-µm 700V CMOS-LDMOS process, the proposed on-chip gate driver was tested with the proposed isolated QSW-ZVS three-level converter. In the converter, 150V eGaN FET (epc2018) was selected as power switches on the primary side to ensure the proper operation of the proposed converter with VDDH up to 250V. The transformer turn ratio is 1.5:1 with the magnetizing inductance of 10µH. Compared to different state-of-the-art on-chip gate drivers in Table 1, the proposed gate driver supports the highest input voltage, improves the turn-on/off delays by at least 3 times, and is the only one capable of supporting 3-level architecture with the dynamic dead-time control for the ZVS operation. Fig. 2 presents the simulated power efficiencies of the proposed converter at different input voltages. The proposed converter achieves the peak power efficiency of 94.2% at V_{IN} of 250V and F_{SW} of 1MHz. Compared to the other isolated converter, the proposed work supports a higher input voltage and a much wider input range, and saves 1.73W power at 2MHz frequency via using the proposed gate driver and the three-level ZVS converter architecture.

Keywords: high-voltage DC-DC converters, isolated converters, on-chip synchronous gate driver, three-level converters, zero-voltage switching.

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] L. Cong and H. Lee, "A 110-250V 2MHz isolated DC-DC converter with integrated high-speed synchronous three-level gate drive," ECCE, Sep., 2015, Montreal, Canada.

TASK 1836.146, ON-CHIP AC-DC POWER CONVERSION WITH GROUND DISTURBANCE SHIELDING FOR ENVIRONMENTAL SENSING APPLICATIONS

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SIGNIFICANCE AND OBJECTIVES

This project is to explore the optimal circuit architecture and operation scheme in achieving on-silicon AC-DC power conversion for environmental sensor applications. The power converter under development should be resilient to ground voltage disturbance, along with high power efficiency and small physical form factor.

TECHNICAL APPROACH

Capacitive power transfer enables the implementation of fully integrated power converters. Monolithic capacitors can be used to transfer AC power and block DC current. Meanwhile, power switches are employed for DC-AC conversion and AC-DC rectification. For a given output power level, the maximum power efficiency is achieved by optimizing these component sizes in order to balance switching and conduction loss hence minimizing the total power loss.

SUMMARY OF RESULTS

In order to achieve high power efficiency, power loss in the switched-capacitor converter should be minimized. The optimization point is equal to the balance point of switching and conduction power loss that are both determined by component sizes and switching frequency.

The switch network and the rectifier consist of power transistors, thus they contribute both conduction loss and switching loss. In a power stage, not only the on-chip capacitors cause conduction loss, but also the bottom-plate parasitic capacitors can produce power loss due to switch charging/discharging.

Conduction loss can manifest itself as a ratio between output voltage drop and load current, or R_{out}. For a given output voltage, the minimum of R_{out} determines the maximum output power level and efficiency. As shown in Fig. 1(a), as output resistance decreases, functions of output power and efficiency are both monotonically increasing. Therefore, given the implementation area constraint, minimizing R_{out} is a critical step for system efficiency optimization.

The relationship between R_{out} and switching frequency, along with corresponding switching power loss is shown in Fig. 1(b). Reducing R_{out} and switching power loss are opposite processes: R_{out} is quadratically decreasing as switching frequency increases, whereas the switching power loss is proportional to the switching frequency. Thus, this conflict on frequency between the conduction loss and switching loss sets the constraint for system efficiency optimization.

Furthermore, the requirement of ground voltage shielding, especially in high-voltage applications, limits the sizes of transfer capacitors. Also, the ratio of bottom-plate parasitic capacitance to the main transfer capacitance is increased with the high-voltage device structure. As shown in Fig. 2, because of the distance between the two capacitor plates for high electric field,

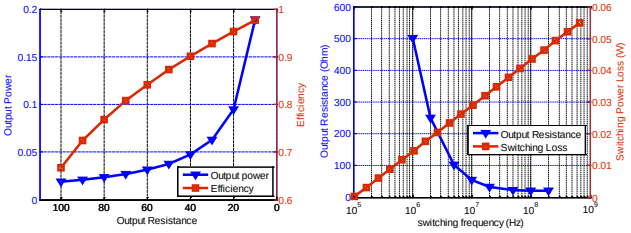

Figure 1: (a) Output power level and power efficiency vs. output resistance, and (b) output resistance and switching power loss vs. switching frequency

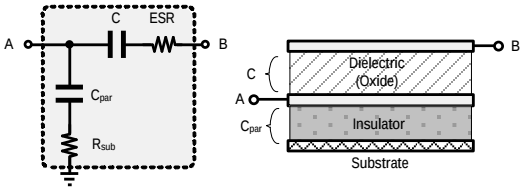

Figure 2: High-voltage capacitor topology

the bottom plate of the high-voltage capacitor combined with the substrate results in a larger size of parasitic capacitor than the main transfer capacitor. It becomes a big portion of switching power loss, especial in the high voltage operation which facilitates low-conduction-loss power transfer. Therefore, special circuit techniques have to be applied to reduce the bottom-plate power loss in this design.

In conclusion, on one hand, the system will be optimized for required power level and efficiency. Novel power stage topologies are being explored to break up the relationship between R_{out} and switching frequency hence to lower the balance point of power loss. Furthermore, device structure and circuit techniques are also being investigated to minimize the impact from parasitics.

Keywords: ground shielding, power efficiency optimization, bottom-plate loss reduction

INDUSTRY INTERACTIONS

Texas Instruments

TASK 1836.149, CONDITION MONITORING OF PM/IPM MOTORS THROUGH AXIAL/RADIAL LEAKAGE FLUX

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SIGNIFICANCE AND OBJECTIVES

In order to avoid costly shutdowns in industrial facilities and minimize safety concerns, PM motors are monitored carefully through leakage flux components using fluxgate sensors. With the sensitivity level, noise immunity, small form factor and low cost, fluxgate sensors have strong potential to transform this technology e.g. by enabling continuous and remote sensing.

TECHNICAL APPROACH

The main flux links stator and rotor components to generate torque, while the leakage flux links only one of these which doesn't contribute to the torque generation. Several leakage flux components exist in motors in and around the motor and shaft. The end winding area can also be recognized as a separate entity as stator end winding leakage flux. These flux components are being monitored through fluxgate sensors developed by TI to identify incipient faults. In addition to the fundamental harmonic, the flux spectrum includes harmonics caused by stator currents, frequency components caused by the asymmetry of supply voltages and various types of other abnormal situations or failures such as eccentricity, stator phase to ground failures, turn to turn short failures of stator winding and rotor winding failures.

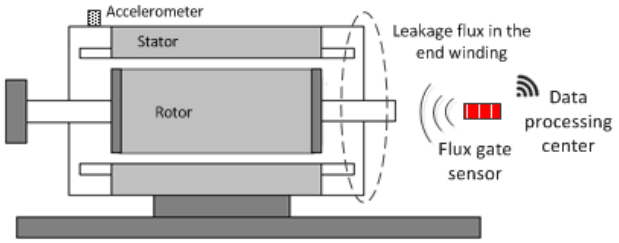

Figure 1: Fault monitoring via fluxgate sensor

SUMMARY OF RESULTS

In order to analyze the leakage flux component for condition monitoring, a comprehensive 2D and 3D finite element analysis has been done through ANSYS Maxwell. In addition, an experimental setup was built to test a 0.4kW servo motor under various fault conditions. Several spots around the motor and shaft have been probed to systematically monitor the leakage components. So far we have investigated broken magnet and eccentricity faults in finite element simulation and identified the fault related patterns in flux density spectrum. In the flux spectrum, the fault patterns can be clearly identified which enables separation of healthy and faulty machines. The difference between the leakage flux behind the slot and behind the tooth is also studied and it is shown that the spectrums of the flux collected from these spots are mainly the same results with different amplitudes. This information is very useful in the case of a machine that may saturate the fluxgate sensor. The same scenarios are repeated experimentally to justify the theoretical findings. As shown below, the fault related signatures significantly increase when the motor has broken magnet or demagnetization issues. The tests are conducted under various torque-speed conditions. It is found that the signatures are mostly torque and speed independent which provides a very unique feature for flux based condition monitoring as the user does not need to design an operating point dependent threshold.

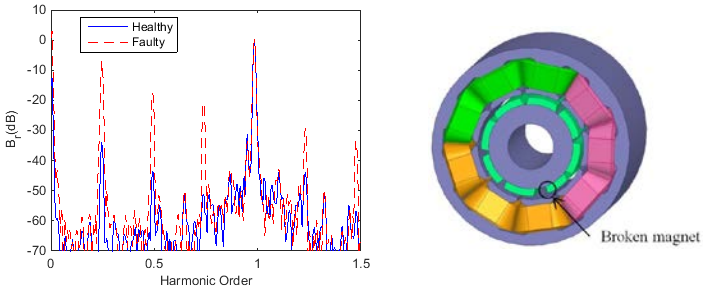

Figure 2: Flux density spectrum of healthy and faulty motors

Keywords: fault diagnosis, condition monitoring, fluxgate sensors, leakage flux spectrum analysis

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Zafarani M, Goktas T, Akin B, "A Comprehensive Analysis of Magnet Defect Faults in Permanent Magnet Synchronous Motors" In Proc. IEEE APEC 2015, NC.

[2] Zafarani M, Goktas T, Akin B,"A Simplified Numerical Approach to Analyze Magnet Defects in Permanent Magnet Synchronous Motors" In Proc. IEEE ECCE 2015, Montreal.

[3] Zafarani M, Goktas T, Akin B,"Separation of Broken Magnet and Static Eccentricity Failures in PMSM" In Proc. IEEE IEMDC 2015, Idaho.

[4] Zafarani M, Goktas T, Akin B,"A Comprehensive Magnet Defect Fault Analysis of Permanent Magnet Synchronous Motors" IEEE Transactions on Industry Apps, 2015, under review.

TASK 1836.153, HIGH - SPEED COMPACT POWER SUPPLIES FOR ULTRA-LOW-POWER WIRELESS SENSOR APPLICATIONS

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SIGNIFICANCE AND OBJECTIVES

Long life-time and autonomous operation are highly desirable characteristics of wireless sensor nodes (WSNs), but there are restrictions on power usage, system volume, and cost. This project is to explore the optimal circuit architectures and operation schemes to achieve fast, compact, and high efficiency DC-DC power conversion for sensor node applications.

TECHNICAL APPROACH

A switched-capacitor (SC) power converter is proposed to supply sensor node systems. With simple compensation scheme, the SC power converter can achieve fast transient response, so that the WSN can quickly enter and exit sleep mode. To maintain high efficiency from light to heavy load, reconfigurable SC topology will be explored and the switching frequency, the power switch size and the flying capacitor size will be optimized. More importantly, the proposed SC power converter can deliver the energy from the environmental energy sources to energy storage elements, leading to low cost of battery replacement for sensor applications.

SUMMARY OF RESULTS

To implement a low-cost, fully-integrated and compact DC-DC conversion for WSN applications, a dual-mode operation SC power converter has been proposed, including energy harvester mode and power mode. The design specifications are summarized in Table 1. To attain a wide input voltage range and a wide output voltage range, both step-up conversion and step-down conversion will be achieved, and the expected SC power stage topology is reconfigurable to obtain multiple conversion ratios (CRs).

Table 1: Design Specifications

Parameters	Specifications	
Operation Mode	Energy Harvester	Power
V_{IN}	0.1-4.5 V	2.5-5.5 V
V_{OUT}	2.5-5.5 V	0.9-3.3 V
Efficiency	≤ 80%	≤ 90%
P_{OUT}	N/A	≤ 10 mA
ΔV_{OUT}	5%	
C_{OUT}	5-10nF	

Switched-capacitor DC-DC power conversion can have different topologies to achieve the specific performance, such as, Dickson charge pump, ladder, Fibonacci and series-parallel topologies. Therefore, one of the critical issues is to determine the most reasonable SC power converter topology for WSN applications. Based on the review of prior research work, Dickson charge pumps are more suitable for the off-chip implementation, especially for step-up voltage conversions. Series-parallel topology charge pumps are better monolithic solution for SC power converter design.

In this project, series-parallel topology is adopted to keep the number of flying capacitors minimal. Our effort also focuses on the conduction loss reduction and on-chip capacitor utilization. Consequently, high power efficiency and high power density will be expected. In terms of the reconfigurable topology, a design strategy is to make charge pump (CP) cells as simple as possible and then use different configurations of CP cells to achieve complex conversion ratios. A fundamental series-parallel CP cell is illustrated in Figure 1.

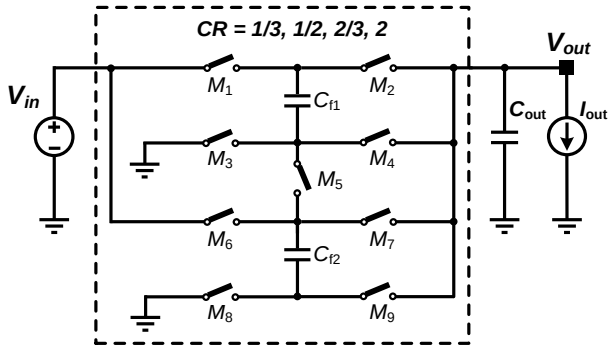

Figure 1: Series-Parallel Charge Pump Cell

The required conversion ratios and corresponding CP cells will be finalized in the next step. Besides, the design parameters of switches and flying capacitors need to be optimized to obtain the optimal power efficiency. The controller design is to improve the performance of transient response and maintain the power efficiency from heavy to light load.

Keywords: wireless sensor node, DC-DC conversion, switched-capacitor, energy harvesting, series-parallel

INDUSTRY INTERACTIONS

Texas Instruments

TASK 1836.154, STATE OF THE HEALTH (SOH) FOR IGBTS: INCIPIENT FAULT CHARACTERIZATION AND DEGRADATION MONITORING

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SIGNIFICANCE AND OBJECTIVES

Development of self-diagnostics/prognostics capable inverters that can detect and warn user, and predict remaining useful lifetime (RUL) of switches to prevent costly shutdowns. The objectives of the study include condition monitoring, degradation detection, and fault prognosis of the power semiconductor devices, and development of control algorithms to provide thermal relief on the degraded switches.

TECHNICAL APPROACH

A multiple switch aging platform, which can expose the power semiconductor devices to accelerated thermal and electrical stresses, is designed to find out the fault signatures that are feasible to be monitored online. The root of the failure modes are identified through failure analysis tools such as SAM results and a safe threshold value is defined for mission critical systems. Methods to monitor the fault precursors using readily available sensors are investigated.

SUMMARY OF RESULTS

Thermal/Power cycling is one of the acknowledged accelerated aging methods. This type of stress causes wear-out in the package mainly due to mismatch of coefficient of thermal expansion, resulting in increased electrical and thermal resistance between the layers at weak spots such as solders, bond-wires, Al metallization etc. In order to find out the fault precursors and I-V parameter shifts, the multiple-switch aging platform has been designed as shown in Fig. 1.

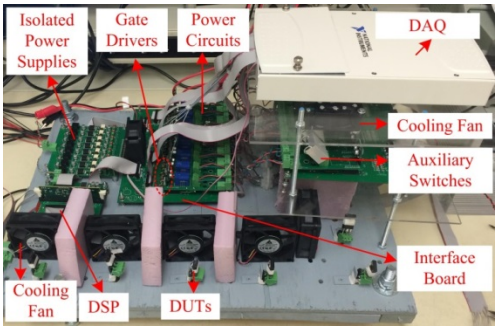

Figure 1: Designed accelerated multiple-switch aging platform.

The outcome of the study shows that die-related electrical properties do not change due to thermal cycling. Due to cracks in bond-wires, voids on the solder joints, both thermal and electrical resistances increase. This increase can be observed from a) on-state resistance, b) body diode voltage drop, and c) gate-source threshold voltage. Similar results are populated on more than 20 power MOSFETs. The failure is typically either open gate/source bond wire.

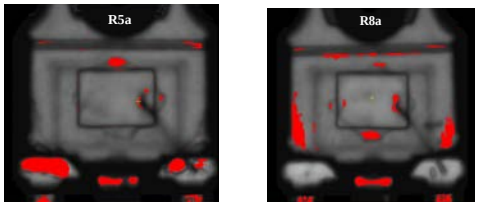

Figure 2: C-SAM results of a) failed device (open gate) b) degraded but functional device.

The results suggest that the on-state resistance for the power MOSFETs increase exponentially under repetitive thermal cycles. Due to the differences in the physical structures, the degradation progression is different even for the same type of switches under same thermal conditions. According to the preliminary results, it is suggested that the on-state resistance increases by about %10-%15 of its initial value. For safety critical mission, end-of-life can be defined as %20 increment from its initial value. The variation is modeled by exponential empirical model which is used in a Kalman Filter.

Keywords: fault diagnostics, fault precursor, power device, remaining useful lifetime, thermal cycling.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] S. Dusmez, and B. Akin, “An Accelerated Thermal Aging Platform to Monitor Fault Precursor On-State Resistance”, in Proc. IEEE IEMDC, Coeur d’Alène, Idaho, USA, 2015.

[2] S. Dusmez, S. A. Huzaif, and B. Akin, "An Active Life Extension Strategy for Power Switches in Interleaved Converters," in Proc. IEEE Annual Meeting of Industry Applications Society, Dallas, Texas, USA, 2015.

[3] S. Dusmez, B. Akin, "Remaining Useful Lifetime Estimation for Degraded Power MOSFETs",in Proc. IEEE ECCE, Montreal, CA, 2015.

[4] S. Dusmez, and B. Akin, "An Active Life Extension Strategy for Thermally Aged Power Switches Based on Pulse-Width Adjustment Method in Interleaved Converters," submitted to IEEE Trans. on Power Electronics, under review.

TASK 1836.157, CMOS GSPS 12-BIT SAR ADC ARRAY WITH ON-CHIP REFERENCE BUFFERS

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SIGNIFICANCE AND OBJECTIVES

ADCs that can deliver GS/s, 12-14 bit performance are of critical demand for applications such as wireless base stations, instrumentations, and software-defined radios, and usually consume more than 500 mW. The target of this work is to time-interleave 4 pipelined two-step SAR ADCs to achieve GSPS throughputs at a 12-bit resolution with a power consumption of less than 50 mW.

TECHNICAL APPROACH

Several techniques are being investigated to improve the performance of the ADC array while maintaining high power efficiency. Split-ADC calibration and direct derivative information (DDI) clock skew calibration will compensate the static errors within one single sub-ADC and the sampling clock skew errors between the four sub-ADCs, respectively. The calibration technique will minimize the input capacitance of the overall ADC to the kT/C noise limit, obviating any power-hungry input buffers. The reference voltage is supplied with on-chip reference buffers and also using a sub-binary DAC structure in the SAR.

SUMMARY OF RESULTS

We expect to implement a 1-GS/s, 12-bit ADC array by interleaving four pipelined SARs using a 65-nm CMOS process. The architecture and calibration setup of the ADC array are shown in Figure 1.

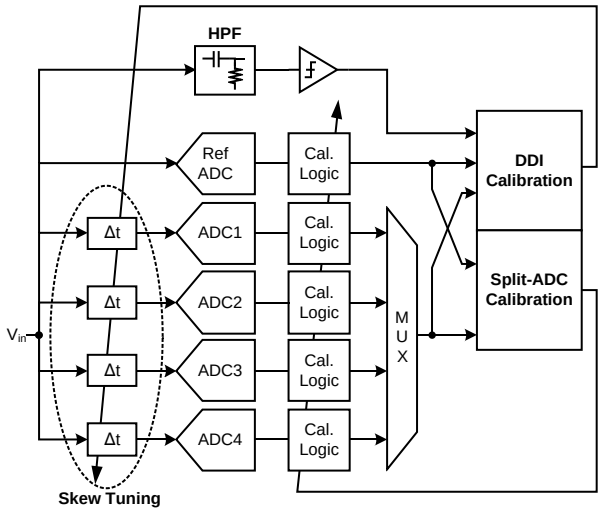

Figure 1: The architecture of the 1-GS/s 12-bit ADC array, which includes 4 single pipelined SAR ADCs.

The split-ADC architecture is adopted to calibrate the DAC mismatch, inter-stage gain error and amplifier nonlinearity in the single channel pipelined SAR ADC [1]. The basic setup includes one additional reference ADC. A pseudorandom bit sequence (PRBS) is injected to the input of the reference ADC. A non-zero error between the reference ADC output and the main ADC array output provides the information for the static calibration.

After the split-ADC calibration is complete, the array should be free of static mismatch errors including offset, gain, and INL/DNL. At this point, the output difference between the reference ADC and the main ADC array is thus only due to the sampling clock skew. The DDI clock skew calibration is implemented next [2]. The input derivative information is derived from a high-pass filter (HPF). Since the output difference can be expressed as

$$E = D_j - D_{ref} = \frac{dV_{in}}{dt} \times \Delta t_j,$$

where D_j is the j^{th} main ADC output and Δt_j is the skew of that same ADC path. Once the E and the input derivative are known, the skew can be estimated.

The single-channel pipelined SAR architecture is based on [3], which demonstrates a 12-bit, 1-bit/cycle, two-step SAR ADC (without interleaving) clocked at 160 MS/s. In order to achieve at least a 250-MS/s throughput for a single-channel SAR ADC, an asynchronous SAR scheme is adopted in both the first and second SAR stages. Separate reference buffers are implemented to provide reference voltages for both stages, preventing potential crosstalk between the various stages in the array.

Keywords: time-interleaved ADC, split-ADC

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

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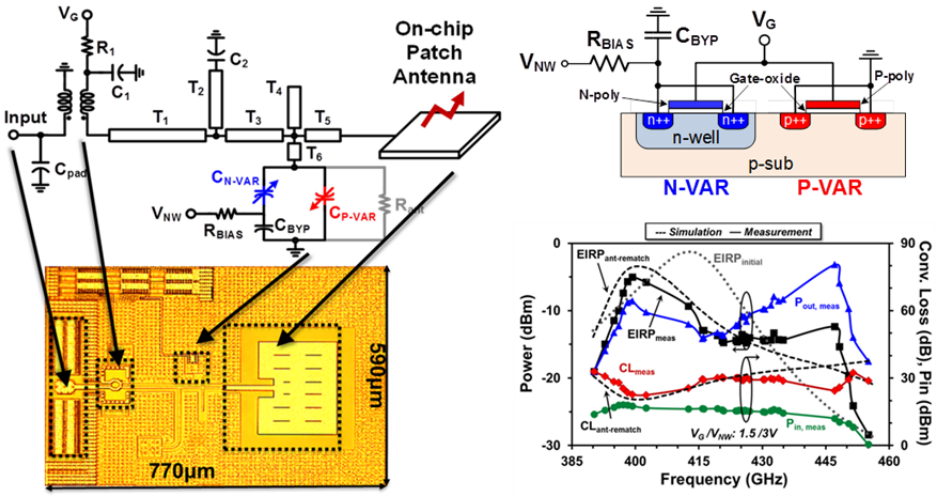
[2] B. Xu et al., "Comprehensive Background Calibration of Time-Interleaved Analog-to-Digital Converters," IEEE Trans. Circuits Syst. I, 2015.

[3] Y. Zhou et al., "A 12 bit 160 MS/s Two-Step SAR ADC With Background Bit-Weight Calibration Using a Time-Domain Proximity Detector," IEEE J. of Solid State Circuits, 2015.

Safety and Security Thrust



Depiction of 447-GHz frequency tripler in 65-nm CMOS for THz waveguide interconnect

Category	Accomplishment
Security and Safety	The increasing bandwidth of silicon integrated circuits may enable waveguide interconnect systems at sub-millimeter-wave frequencies having 200-500 Gb/s throughput. A 447-GHz frequency tripler has been demonstrated in 65-nm CMOS using novel varactor structures and providing 0.5-mW output power (-3.2 dBm) with only 15-dB conversion loss. This indicates that 65-nm CMOS can be used to generate sufficient power for the terahertz guided-wave interconnects. (1836.152, PI: K. O, UT Dallas)
Security and Safety	A serial I/O receiver with multi-level decision feedback equalization has been demonstrated in 65-nm CMOS for PAM4 which employs one FIR tap and two IIR taps for efficient "long-tail" intersymbol interference cancellation. The quarter-rate PAM4 circuit achieves 32 Gb/s with power efficiency of 0.55 mW/Gbps and area of 0.014 mm^2. (1836.143, PI: S. Palermo, Texas A&M)
Security and Safety	Analysis and verification of analog/mixed-signal (AMS) systems is difficult. New techniques have been developed to accurately abstract and formally analyze the SPICE-level dynamics of AMS systems using purely Boolean models. A technique entitled "BEE" has been developed which provides eye-diagram analysis for high-speed links with order of magnitude speed-up over Monte-Carlo analysis with no loss of accuracy. (1836.094, PI: J. Roychowdhury, UC. Berkeley)

1836.083, BUILT-IN TEST FOR POWER-EFFICIENT MILLIMETER-WAVE ARRAYS

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SIGNIFICANCE AND OBJECTIVES

This program will develop orthogonal code-based built-in-test techniques for millimeter-wave arrays, allowing for simultaneous testing of all elements in the array at either circuit or package level, reducing the time and cost of test. Also, circuit and system architectures to increase the power efficiency of a 60GHz phased array will be explored, and a transmitter with BIST will be demonstrated.

TECHNICAL APPROACH

A low-power 60-GHz phased-array transmitter prototype with BIST will be developed in 0.12-µm SiGe BiCMOS technology and scalable code-multiplexed test techniques will be developed for this demonstration platform. CDMA test techniques will be compared to both external test and traditional BIST techniques. Power-efficient PA and phase-shifters will be developed and incorporated into a multi-element 60-GHz phased-array prototype with BIST.

SUMMARY OF RESULTS

Code-Multiplexed Embedded Test Research: Significant advances have been made on the code-multiplexed embedded test (CoMET) in the final year. These approaches allow us to measure the gain and phase variation of each element across the array in parallel or snapshot fashion. The new approach relies on code-modulated interferometric measurement techniques With CoMET, we are able to measure the cross-correlation between each pair of elements within the array. These cross-correlations can be solved numerically for the individual amplitude and phase responses of each element. Alternatively, a calibrated measurement can be performed on a single element and then the code-modulated cross-correlation technique can be used to leverage this calibrated measurement across the array. Our new approach has been validated in behavioral and transistor-level models and the approach is being validated in hardware during summer 2015 using our 60-GHz beamformer.

Beamformer Research: In late 2014, we redesigned our dual-vector Doherty array to fix performance and layout issues in our first-generation design. The layout is shown in Fig. 1 and achieves 17.4-dBm OP_{1dB} per element and 8.8% PAE at 6-dB back-off in simulation.

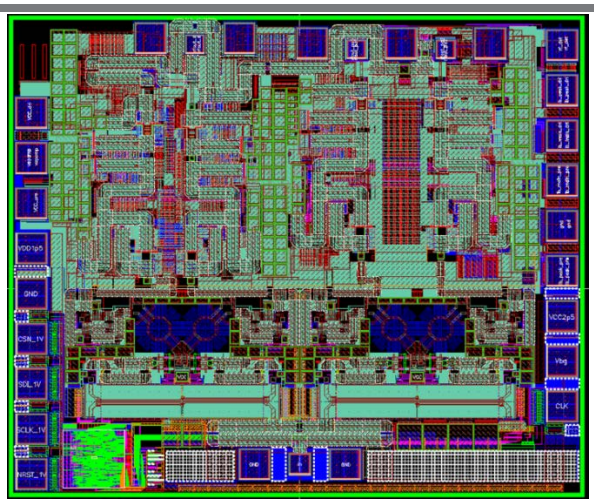

Figure 1: Layout of 60GHz Dual-Vector Doherty Array.

Initial hardware measurements of a Doherty PA breakout show that the PA well, setting a performance record for back-off efficiency at 60 GHz. Also, to the author's knowledge, this may be the first successful silicon mm-wave Doherty demonstration. Measurements on the full Dual-Vector Doherty are in progress and will be completed in summer 2015.

Finally, our dual-vector phase rotator concept has been fully demonstrated through hardware measurements on a 28-GHz circuit prototype [1]. The circuit works well and is able to provide nominally quadrature output signals from a single rotator structure with unique phase and amplitude scaling capabilities. The 4-bit dual-vector rotator was implemented in IBM 0.12-µm SiGe BiCMOS technology and achieves full 360^{o} phase shifting, RMS phase and amplitude errors of < 5 degrees and < 0.8 dB, respectively for both output vectors, and 10-12 dB of gain. Output 1-dB compression points for both quadrature outputs is -6.5 to -4.4 dBm, suitable for directly driving a Doherty amplifier in a 28-GHz beamformer.

Keywords: millimeter-wave, phased-arrays, built-in test, 60GHz, CDMA, power amplifiers

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

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TASK 1836.094, ACCURATE FSM APPROXIMATIONS OF ANALOG/RF SYSTEMS FOR DEBUGGING MIXED-SIGNAL DESIGNS

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ROBERT BRAYTON, UC BERKELEY

SIGNIFICANCE AND OBJECTIVES

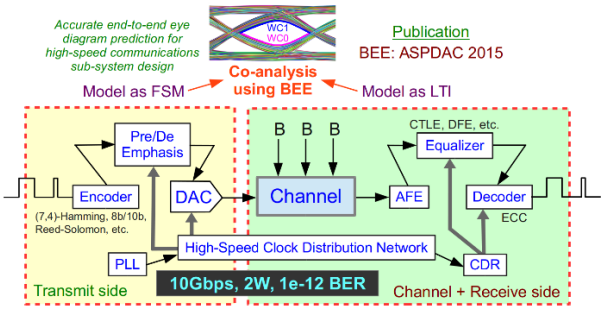
This project aims to develop tools, techniques, and algorithms to automatically generate and efficiently analyze Boolean models (e.g., FSMs, BDDs, AIGs, etc.) that accurately capture the SPICE-level continuous I/O behavior of analog/mixed-signal (AMS) systems. Such models will enable efficient formal analysis, verification, high-speed simulation, validation, and debugging of AMS designs by leveraging existing Boolean analysis tools (e.g., ABC) and hybrid systems frameworks.

TECHNICAL APPROACH

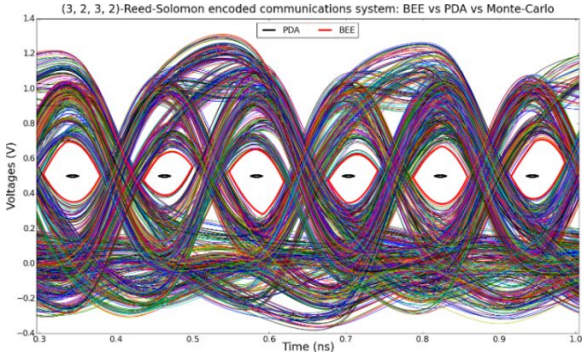
We have developed a suite of techniques for accurate Booleanization and analysis of AMS systems. We discretize the continuous signals in these systems into multi-bit sequences and approximate the underlying analog dynamics using purely Boolean operations on these bits. One such technique, DAE2FSM, is based on Angluin's algorithm from computational learning theory, which we adapted to auto-generate Mealy machine models of SPICE-level AMS designs. Another technique, ABCD-L, relied on eigen-analysis and scalar linear ODE Booleanization for modelling analog effects such as ISI, crosstalk, ringing, etc. in continuous linear systems. Yet another technique, ABCD-NL, was based on separating the DC and TRAN behaviors of non-linear AMS systems for accurate Booleanization. Finally, we developed BEE, a dynamic programming based technique for accurate eye diagram analysis of AMS designs such as high-speed communications sub-systems.

SUMMARY OF RESULTS

We have applied DAE2FSM, ABCD-L, ABCD-NL, and BEE to accurately Booleanize and efficiently analyze/verify a number of AMS designs. For example, the figure below illustrates how BEE is applied to carry out accurate and efficient eye diagram analysis of a modern multi-Gb/s high-speed communications sub-system. The transmit side of such a system (including the encoder and the pre-emphasis/de-emphasis circuitry) is first modelled as a Boolean FSM. The channel and the receive side (which may include equalization circuitry) are then modelled as an LTI system. Finally, BEE is used to carry out FSM/LTI co-analysis to accurately determine the performance of the system (in terms of its end-to-end eye diagram) at a fraction of the cost of Monte-Carlo analysis, and with much less pessimism than existing techniques.



The figure below shows the results obtained by applying BEE to analyze such a system employing a Reed-Solomon encoder. The multi-colored waveforms are Monte-Carlo simulations showing the receive side signal. The red waveforms are the eye diagrams predicted by BEE, which, as the figure shows, perfectly match the Monte-Carlo simulations. The black waveforms are the eye diagrams predicted by PDA, a well-known existing technique. As the figure shows, PDA is highly pessimistic, whereas BEE is exact and accurate. Furthermore, BEE is orders of magnitude faster than (and also more reliable than) Monte-Carlo simulation.



Keywords: AMS verification, accurate booleanization, eye diagram analysis, high-speed simulation, debugging

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] Aadithya, Roychowdhury, et al. BEE, ASPDAC 2015.

[2] Aadithya, Roychowdhury, et al. ABCD-NL, ASPDAC 2014.

[3] Aadithya and Roychowdhury. ABCD-L, DAC 2013.

[4] Aadithya, Roychowdhury, et. al. DAE2FSM, DAC 2012.

TASK 1836.101, SPARSE 2D MIMO RADAR TRANSCEIVER DESIGN AND PROTOTYPING FOR 3D MILLIMETER-WAVE IMAGING

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SIGNIFICANCE AND OBJECTIVES

Multiple-input multiple-output (MIMO) radar technologies are explored for millimeter wave (mm-wave) imaging systems in this project. Three-dimensional (3D) mm-wave imagers are designed in order to obtain images of concealed objects. A two-dimensional (2D) sparse MIMO transceiver array is designed to help attain spatial diversity and reduce the number of transceivers.

TECHNICAL APPROACH

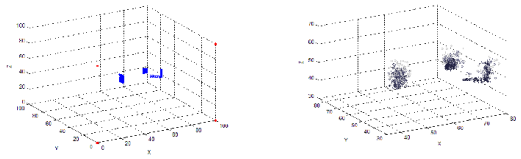
3D mm-wave imagers are designed to obtain images of objects placed behind obstacles or inside closed contours. While the 2D sparse array has a separation in the order of half the wavelength inside an imaging system, several of these "imaging systems" can be placed in the order of several inches apart to obtain localization that leads to 3D images. We showed how a group of imaging sensors located in the close vicinity of a target can provide images respective to their positions, and how this information can be combined to identify a target's presence, location, and shape.

SUMMARY OF RESULTS

We have studied and implemented several schemes to gradually improve the 3D target imaging capability. We first used the angular bin information received from four sensors in constructing the resultant images. Only the presence of point targets can somewhat be estimated based on the angular bins. Therefore, we enhanced our scheme by utilizing the range bins obtained at the four sensors to extract a clearer 3D image. A simple sum-of-pixels was first employed for combining the reflectivity coefficients for each of the pixel values from the four sensors to estimate the likelihood of the presence of a target. More advanced threshold-based interpolation methods were then designed to improve the image.

The effects of the number and location of sensors, and that of objects with different shapes and reflectivity were studied. Changing the orientation of the transceiver arrays has yielded substantial improvement. For example, if the antennas in two sensors are arranged horizontally and that of the other two vertically, the information received from the range and angle bins can complement each other and help reduce the ambiguity.

We have improved the scene simulation to obtain realistic estimates of the environment. A 3D ray tracing simulation was employed, and effects of scattering, diffraction and absorption were accounted for. The resultant 3D image deteriorates with this improved scene simulation. Images are blurrier due to inclination of the surfaces with respect to the sensors and signal strength variations due to varying transmission distances. The sensor orientations and image recovery algorithms, therefore, are redesigned accordingly. With complex and/or larger target objects, the interference between the different sets of range bins are higher and image gets distorted. Remedies that we designed include mathematically formulating the effects of the different sets of waves in order to suppress the interference effects, exploit reflections from surrounding objects, etc.



(a) (b)

Figure 1: Target image (a) and reconstructed image (b) obtained using proposed 3D mm-wave imager.

We enhanced the research efforts from our prior project (1836.036). We had addressed the use of space-time-block-code (STBC) based MIMO radar technology to reduce the cost of mm-wave imaging systems by reducing the number of antennas [1]. In [2], we had proposed the use of multiple imaging systems in sensor network target localization for the purpose of surveillance. In addition to our prior studies, we have shown the effects of varying different parameters of the system, such as the regularization parameter, length of the waveform, number of angular bins, etc.

Keywords: MIMO radar; millimeter wave imaging; sparse transceiver array; spatial diversity; pulsed radar.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS

[1] Sadeque et al., "Waveform Transmission Scheme for MIMO Radar Imaging Based on Space-Time Block Codes," IEEE Transactions on Aerospace and Electronic Systems, Vol. 50, No. 1, January 2014, pp 12-21.

[2] T. Ali et al., "MIMO Radar for Target Detection and Localization in Sensor Networks", IEEE Systems Journal, Vol. 8, No. 1, March 2014, pp 75-82.

TASK 1836.102, SUPERRESOLUTION TECHNIQUES FOR 3D MILLIMETER WAVE RADARS

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SIGNIFICANCE AND OBJECTIVES

This research aims at developing high resolution imaging techniques for millimeter wave radars with the low complexity of silicon implementation. We develop a 3D *joint superresolution* algorithm with an FMCW radar framework, which has gained attention in recent years owing to its application in automotive industry.

TECHNICAL APPROACH

Existing 3D superresolution techniques are inherently slow due to (1) Joint exhaustive search across all the possible dimensions, (2) Size of the covariance matrix used for the subspace based superresolution algorithms. We propose two techniques to reduce the complexity: (1) two-stage detection based on the Fourier transform and beamspace MUSIC which performs faster than the existing algorithms, and (2) a 3D estimator that breaks the problem into lower 2D searches.

SUMMARY OF RESULTS

For an FMCW radar (with modulation index K) and 2D antenna aperture ($L \times M$) collecting reflections from P objects located at (R_p, θ_p, ϕ_p), the noiseless mixer's output signal (N discrete samples) is given by:

$$d(l,m,n) \approx \sum_{1}^{P} \rho_p e^{j2\pi\left[\frac{2KR_p n}{cf_s} + \frac{2(R_p + ld\sin\theta_p\cos\phi_p + md\sin\theta_p\sin\phi_p}{c} + \frac{2f_c R_p}{c}\right]}$$

From the above equation it can be seen that 3D Fourier transform across space and time yields the target locations at lower resolution which depends on system bandwidth and aperture size. Fourier based imaging has the least complexity of the implementation which is $\mathcal{O}(LMN \log LMN)$. Moving towards the superresolution technique increases the implementation cost to $\mathcal{O}(LMN)^3$. This cost can be reduced to $\mathcal{O}(L_b M_b N_b)^3$, (where suffix b denotes lower dimensional subspace) via beamspace projection in space and time. In Fig. 1 we show three closely paced targets in range and angle are being separated using joint a beamspace superresolution technique. We simulate the FMCW radar system at carrier frequency of 77 GHz with 300 MHz of bandwidth and 300 μs of FMCW pulse time.

Data are discretized at sampling frequency of 1.70 MHz and SNR of 10dB. With a 16×16 element antenna array 512 samples are collected in time. Table 1 compares the cost of implementation of different imaging modalities for the aforementioned FMCW system. In another example, we show that 3D estimation problem can be decomposed into three 2D estimation problems without any association ambiguity. The computational complexity is thus reduced to $\approx \mathcal{O}(LM)^3$.

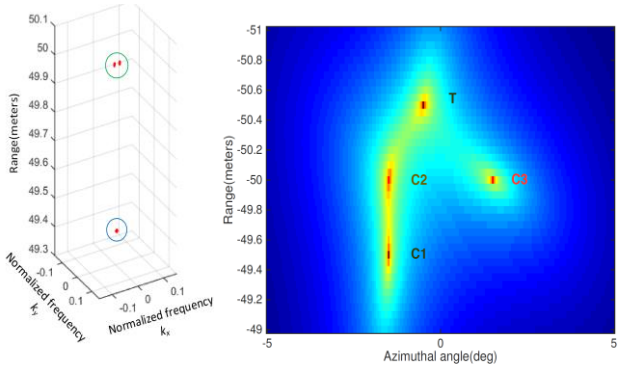

Figure 1: 3D Joint beamspace superresolution (left) and Range-azimuth joint estimation of typical traffic scenario (right)

Table 1: Complexity Comparison

Algorithm	3D Joint	3D Joint beamspace	Three 2D Joint beamspace
Cost ($\mathcal{O}$)	3.2×10^{10}	8.8×10^{5}	4.1×10^{4}

Consider, a 3D typical traffic scenario with three cars separated by distance of 0.5m in range domain and 3^0 in angular domain. Two cars share the same range and azimuthal angle bins and all three cars are at the same elevation. The traffic sign is present at the angle 2^0 above the cars and lie in a different range bin. Hence, with the range-elevation and elevation-azimuth estimation it is not possible to separate the targets without any ambiguity. However, as shown in Fig. 1 (right) 2D range-azimuth estimation of this typical traffic scenario can successfully resolve targets.

Keywords: mm-wave imaging, beamspace projection, superresolution, automotive radar, low complexity

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] S. Patole and M. Torlak, "Low Complexity 3D Joint Superresolution Imaging," (To be submitted) IEEE Trans. on Signal Proc., May 2015.

[2] S. Patole, "Low Complexity Joint Superresolution Algorithms for Millimeter Wave Imaging," accepted, TECHON 2015, Austin, TX.

TASK 1836.119, DEMONSTRATION OF 180-300 GHZ TRANSMITTER FOR ROTATIONAL SPECTROSCOPY

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SIGNIFICANCE AND OBJECTIVES

As part of the effort to help open up high millimeter and sub-millimeter wave frequency range for moderate volume and cost applications, this task is seeking to demonstrate a 180-300 GHz transmitter in CMOS for a rotational spectrometer that can be used to detect harmful molecules in air and to analyze breaths.

TECHNICAL APPROACH

The transmitted power should be ~10-100 µW. The main challenges are increasing the output frequency range, power, and frequency for phase locked signals. To realize a fast scan rate with a 10-kHz step, a fractional-N synthesizer is used. The synthesizer also incorporates a frequency modulation function. The output signal generation using a combination of an N-push technique and frequency multiplication/translation techniques. This task will also help generating the receiver LO signal.

SUMMARY OF RESULTS

Building on the demonstration of 85-127 GHz transmitter (39% tuning range) using a fractional-N PLL (FNPLL) (Figure 1) that generates frequency shift keyed (FSK) signals with a frequency step of 570 Hz and settling time of ~10 µS, a 200-300 GHz transmitter integrated circuit has been designed and submitted for fabrication in a 65-nm CMOS process with 10 metal layers. The top copper layer thickness is ~3 µm and the dielectric layer between the top metal layer and silicon is ~8 µm.

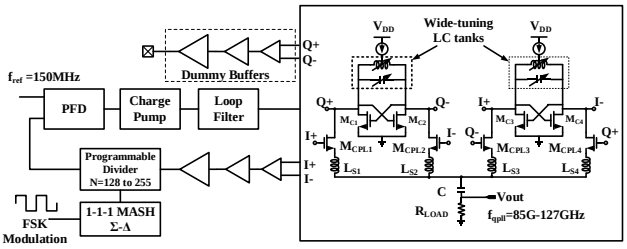

Figure 1: Block diagram of FNPLL including a QVCO with broadband passive coupling and freq. multiplication by 4.

In addition to the FNPLL transmitter, a broadband amplifier, a frequency translation circuit to generate the signals at 200 to 300 GHz, and an on-chip antenna have been incorporated. The prototype includes all the necessary functionality for testing in a rotational spectroscopy set-up. Test structures for the broadband amplifier and frequency translation structures including a frequency doubler and a mixer have also been submitted for fabrication.

Table 1 summarizes the simulated performance of the transmitter.

Table 1: Transmitter simulated performance

Transmitter Specification	Simulated Results
Output Frequency	200 to 300 GHz
Frequency Step or Resolution	5 kHz or 17 bits
Settling Time/Scan Speed	1 mSec / 5 MHz per s
Output Power Available for an on-chip antenna	-15 dBm (@ 200 GHz to 300 GHz)
FM Deviation	100 -1000 kHz
Phase Noise for line width of 30kHz	< -62 dBc/Hz at 1MHz offset @ 300 GHz

In addition, approaches to generate 180 to 300 GHz signals using a QVCO operating at 45 to 75 GHz with passive coupling and frequency multiplication by 4 are being investigated. More specifically, use of switched inductor structures at this frequency range is being investigated.

Keywords: rotational spectrometer, transmitter, CMOS, millimeter-wave.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

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[3] J. Zhang, N. Sharma and K. K. O, "21.5-to-33.4GHz VCO using NMOS Switched Inductors in CMOS," IEEE Microwave and Wireless Components Letters, vol. 24 , no. 7, pp. 478-480 , May 2015.

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TASK 1836.120, EVALUATION OF FREQUENCY AND NOISE PERFORMANCE OF CMOS 180 – 300 GHZ SPECTROMETER TRANSMITTER AND RECEIVER COMPONENTS

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SIGNIFICANCE AND OBJECTIVES

A gas phase absorption spectrometer in the 100 to 1000 GHz frequency range would be extremely valuable to rapidly and precisely assay a wide range of chemical vapors. This project's objective is to quantitatively evaluate passive materials and passive and active devices/circuits for suitability as millimeter-wave components to be integrated into a spectrometer system.

TECHNICAL APPROACH

The 3rd year of this project undertook three tasks: (1) continued use of a Fourier transform spectrometer (FTS) to evaluate dielectric characteristics of passive material components, including high- and medium resistivity silicon and polyethylene naphthalate (PEN); (2) set-up of a quasi-optical 220–330 GHz subharmonic receiver system capable of precision frequency, linewidth, and noise measurements to characterize oscillators broadcasting into free-space; and (3) initial use of the FTS to characterize frequency performance of passive (antenna) and active (CMOS multiplier source) device and circuit components.

SUMMARY OF RESULTS

In collaboration with Dr. Rashaunda Henderson and Dr. Sam Shichijo, we have continued the previous years' work characterizing the high-frequency dielectric index and loss characteristics of dielectric materials to support transmitter/receiver antennas and waveguide circuit connections. Materials' dielectric and loss properties are not typically reported in the literature above 30 GHz. Over the past year we have added high- (8 kΩ-cm) and medium (15 Ω-cm) resistivity silicon and polyethylene naphthalate (PEN) in addition to benzocylcobutene (BCB) and the photoresist SU8. In our modeling efforts to extract index and loss tangent from the measured reflection and transmission spectra, we found a precise modeling of the data requires detailed high-resolution spectra. Such spectra have been measured for all materials and we are in the process of running model fits to the data to derive physical parameters.

For the purposes of testing free-space sub-millimeter wave receivers, a 220 to 330 GHz even harmonic mixer receiver has been set up and characterized. This receiver uses a horn antenna input to receive signals from free-space. A 5 to 20 GHz local oscillator (LO) input is needed, so only an off-the-shelf and relatively low cost microwave LO source is required, rather than an expensive custom sub-millimeter wave LO source. The noise and conversion loss characteristics of this receiver have been measured. Conversion loss (SSB) is between 35 to 45 dB across the 220 to 330 GHz band. This receiver is capable of precision frequency, linewidth, and phase noise measurements of any free-space broadcast oscillator in its band.

Finally, in the past two months we have obtained the first set of terminated antennas from Dr. Henderson's group and the first CMOS frequency multiplier circuit from Dr. O's group. The antennas are modified bowtie antennas nominally terminated in their characteristic impedance and laminated to an anti-substrate mode "mushroom forest." Efforts have begun to use the FTS to measure the receiving band and polarization characteristics of these antennas. The CMOS multiplier circuit is and unpackaged test die, so we have designed and are building a specialized probe station that fit with the optical input requirements of the FTS. The ultimate aim is to broadcast the circuit's output into the FTS where we can make spectral measurements of its fundamental frequency, harmonic and inter-harmonic distortions, and leakage of sub-harmonics.

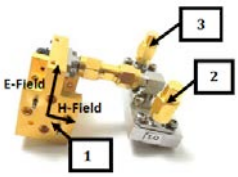

Figure 1: Image of the 220 – 330 GHz mixer. Port 1 is the RF signal input (horn antenna is detached). Port 2 is the LO input (SMA). Port 3 is the IF output (SMA).

Keywords: millimeter-wave, terahertz, spectrometer, dielectric loss, power meter

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

TASK 1836.122, ON-CHIP INTEGRATION TECHNIQUES FOR 180-300 GHZ SPECTROMETERS

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ANDREW BLANCHARD, UT DALLAS

SIGNIFICANCE AND OBJECTIVES

The objectives include the development of novel design and fabrication techniques to integrate 180-300 GHz CMOS-based gas spectrometer transceiver circuits with broadband planar radiators.

TECHNICAL APPROACH

One approach uses coplanar waveguide interconnects to feed a planar bowtie aperture antenna fabricated in a post-IC technology comprised of thick layers of SU-8. SU-8 (ε_r = 3) is a photoresist typically used as a sacrificial layer in micro electro-mechanical systems (MEMS) processing. In a parallel effort to facilitate early assessment of the transmitter and receiver circuits and to ease processing issues, a second approach involves the use of on-chip dipole antennas that have been included in our collaborator's (Ken O & Wooyeol Choi) most recent chip tapeout. These traditional on-chip dipole antennas have 10% operating bandwidth. We are fabricating an artificial magnetic conductor (AMC) on a FR4 laminate that will be placed below the chip with the integrated dipole. An array of metallic patches (0.020 mmm on a side) will be distributed on the grounded laminate substrate to increase the antenna bandwidth.

SUMMARY OF RESULTS

To date, the standalone antenna has been fabricated with return loss measurements covering 180-300 GHz, but no radiation performance has been obtained. We have two methods to characterize the antennas. One involves the use of a FTIR system with our collaborator, Mark Lee. The spectral transmission characteristics of the antennas can be obtained from 150 to 7500 GHz. In order to measure the antenna properties, the radiator must be terminated in it's design impedance.

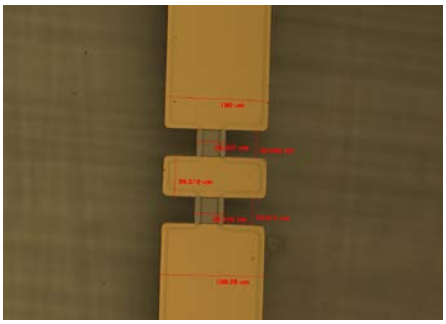

Figure 1: Two TaN resistors in parallel with 50 Ω CPW pad.

We have completed the fabrication of thin-film resistors to aid in characterizing the properties of the fabricated planar aperture bowtie antennas. Figure 1 shows a set of two 100 Ω tantalum nitride (TaN) resistors in parallel with the signal and ground of a coplanar waveguide pad. This zero length line is used to characterize the TaN sheet resistance and process lithography. The resistors were fabricated on polyethylene naphthalate (PEN) (εr = 2.9) film and incorporated with the antenna feed (Figure 2). Figure 3 shows the return loss of the terminated antenna from 220 to 325 GHz. The return loss is below 10 dB across the entire band. With the acquisition of a spherical scanner system we will measure the radiation pattern of the antenna using near field techniques.

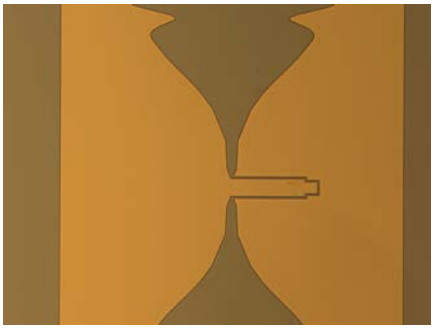

Figure 2: Fabricated bowtie aperture antenna with CPW feed.

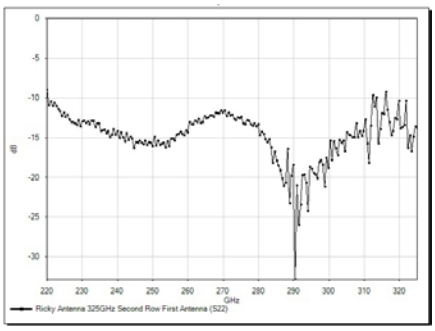

Figure 3: Measured return loss of TaN terminated antenna.

Keywords: aperture antennas, SU-8, CPW, post-IC, radiation pattern, TaN thin film resistors

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] J. Arzola, C. Miller & R. Henderson, "40 GHz laminate power divider circuits using integrated resistors," 2015 IEEE International Microwave Symposium.

TASK 1836.126, DESIGN SPIN REDUCTION VIA INTEGRATED THZ DESIGN: APPLICATIONS, PHYSICS, AND SYSTEM ENGINEERING

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CHRISTOPHER F. NEESE, OHIO STATE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

The objective of this project is to develop a THz System Engineering Tool that allows for analysis of systems based on the characteristics of their building blocks and to validate it by applications to systems of interest. These systems include CMOS gas sensors and systems for process diagnostics and control.

TECHNICAL APPROACH

This effort includes: (1) Diagnostics and process control in semiconductor plasma reactors using commercially available III-V systems, and (2) in parallel and the longer term, the development of CMOS systems for this application, as well as more generally for gas sensors. Tying this together is a computationally based THz System Evaluation Tool, which is designed to be a general tool for use by less system oriented CMOS developers.

SUMMARY OF RESULTS

Our THz SET was originally written in WaveMetrics Igor Pro and consists of a library of functions and data structures. Figures 1 and 2 show an example of an input panel and outputs. However, simulations require writing Igor Pro code. We are in the process of converting it to the more user friendly and available Python language. Additionally, we are including a GUI interface. As an example and portability test, we are applying it to the CMOS spectrometer being fabricated by UTD. We will work with their personnel to test its portability into the CMOS community.

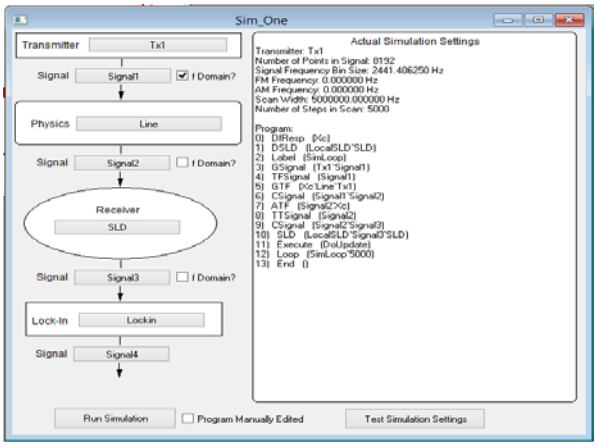

Figure 1: Input panel and block diagram generated by it for an FM modulated THz spectrometer with phase sensitive detection.

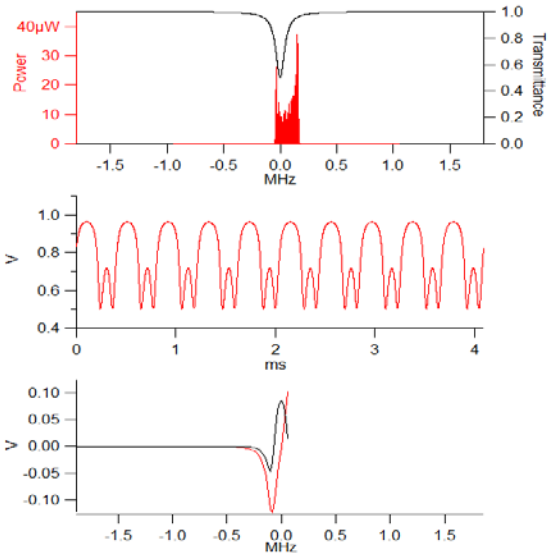

Figure 2: Absorbance relative to FM spectrum of source (top panel). Output before phase sensitive detector (middle panel). Output of phase sensitive detector (lower panel).

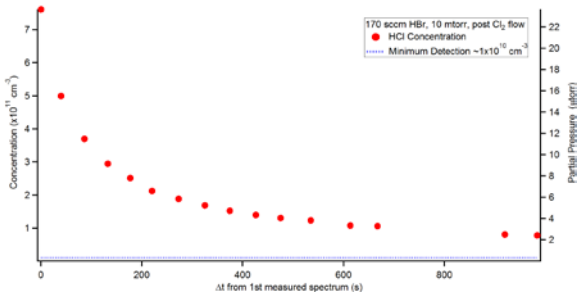

Figure 3: HBr reaction residence in reactor.

We have also applied the THz SET to a semiconductor plasma reactor sensor. Figure 3 shows experimental results from that system.

Keywords: submillimeter, terahertz, spectroscopy, plasmas, semiconductors

INDUSTRY INTERACTIONS

Applied Materials, Texas Instruments, IBM, Intel

MAJOR PAPERS/PATENTS

[1] Submillimeter absorption spectroscopy in semiconductor manufacturing plasmas and comparison to theoretical models, Y. H. Helal et al., 70th Int. Symp. on Mol. Spect, Urbana, IL, 2015.

TASK 1836.131, PROCESS VARIATION ANATOMY: A STATISTICAL NEXUS BETWEEN DESIGN, MANUFACTURING & YIELD

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SIGNIFICANCE AND OBJECTIVES

In semiconductor manufacturing, electrical tests (e-tests) are collected on silicon wafers for process monitoring purposes. We investigate the utility of correlations between these e-tests and probe tests in predicting yield. Then, we extend this correlation for accurate yield prediction during fab-to-fab production migration.

TECHNICAL APPROACH

We developed a yield prognosis method, which relies on e-test and probe test measurements of a device from a source fab, where it is currently produced, as well as the e-test profile of a target fab, where it is being migrated.

The first step is to build a correlation model which expresses parametric yield of a wafer as function of its e-test measurement vector. Fig. 1 depicts such correlation. We employed Multivariate Adaptive Regression Splines (MARS) to build this model. To predict parametric yield in the target fab during fab-to-fab production migration, a simple approach would be to train a model in the source fab and directly apply it to the e-test profile of target fab, which can be obtained from a prior device. This approach is called *model migration*. The accuracy of this method is limited, however, because the distribution of e-tests in the source and target fabs are different.

To improve the prediction accuracy, we proposed the *predictor calibration* technique. In this method, the e-test distribution of the target fab is calibrated based on the e-test distribution of the source fab. This calibration transforms the e-tests of the target fab to what they would have looked like if the target fab wafers had been produced in the source fab. To make this transformation accurate, several aspects of the distribution, such as its mean, variance, skewness and kurtosis, need to be calibrated. Then, the model which is trained in the source fab can be applied to the calibrated e-tests in order to make a more accurate prediction of parametric yield.

SUMMARY OF RESULTS

The results of our method for predicting parametric yield when migrating production of a device from a source to a target fab are shown in Fig. 2. These charts show the normalized prediction error for the model *migration* and the proposed *predictor calibration* approaches. In each histogram, the horizontal axis is the prediction error, while the vertical axis shows the percentage of probe tests that are predicted within a given error range.

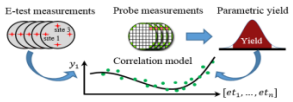

Figure 1: E-test/yield correlation model.

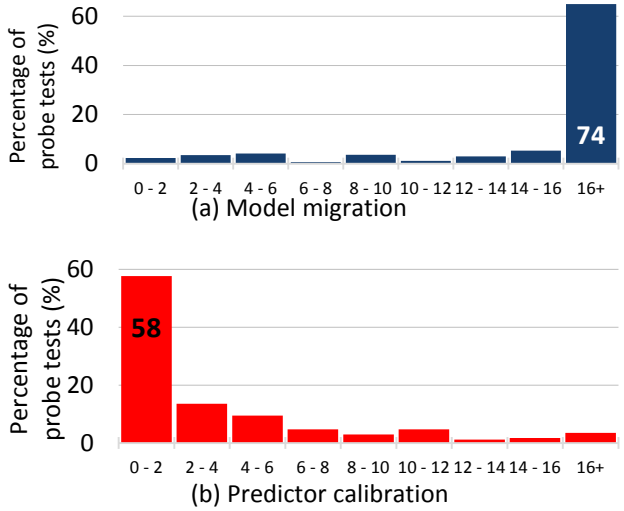

Figure 2: Fab-to-fab yield prediction error

For example, the first bar shows the percentage of probe test measurements whose average yield prediction error is between 0 and 2%, which is 3% for model migration. Higher concentration on the left side indicates lower probe test yield prediction error. In model migration, around 74% of probe measurements have more than 16% prediction error, which translates to 124 out the 168 probe tests in our dataset. In contrast, predictor calibration achieves yield prediction error below 2% for 58% of the probe test measurements and outperforms model migration, enabling accurate parametric yield prediction during fab-to-fab production device migration.

Keywords: process variation, parametric yield prediction, production migration, predictor calibration

INDUSTRY INTERACTIONS

Texas Instruments, Intel, GlobalFoundries

MAJOR PAPERS/PATENTS

[1] A. Ahmadi et al., "Yield prognosis for Fab-to-Fab product migration," IEEE VLSI Test Symposium, 2015.

[2] A. Ahmadi et al., "Yield Forecasting in Fab-to-Fab production migration Based on Bayesian Model Fusion," submitted to IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2015.

TASK 1836.135, SUB-PICOSECOND SYNCHRONIZATION OF WIDELY SPACED IMAGING ARRAYS

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SIGNIFICANCE AND OBJECTIVES

Tight synchronization of a distributed array with widely-spaced sparse elements is a key enabler in coherent combining of signals in space. The objective of this project is to build a wireless synchronization link capable of synchronizing a master node to multiple slave nodes with timing jitter of 500fsec in less than 10nsec.

TECHNICAL APPROACH

In order to implement imaging radars with high angular resolution, we use sub-8psec impulses to synchronize the wireless nodes. Achieving synchronization with accuracy of 500 fsec requires a low-noise receiver which has two antennas to separate the LOS signals from NLOS signals and is capable of distinguishing the actual zero crossings from the ringing effects. One synchronization approach is locking a VCO to the input repetition rate by injecting one of its strongest frequency components so that the clock can be used to sample the time-domain input signal. As another approach, we use a nonlinear circuit to derive the repetition rate of the impulse train.

SUMMARY OF RESULTS

In order to synchronize the receiver with the impulse radiator, we have proposed and implemented two different architectures.

In the first architecture, we use injection-locking oscillators to lock an output clock to 1/N of the input frequency component from the LNA. The input amplifier is tuned at the center frequency of the radiated impulse to amplify its strongest frequency component and derive the repetition rate out of it. This architecture is shown in Figure 1, with a divide-by-eight injection-locked frequency divider. We have implemented this architecture in a 65nm CMOS process and it is currently being tested to demonstrate the performance of the synchronization part as well as the sampler.

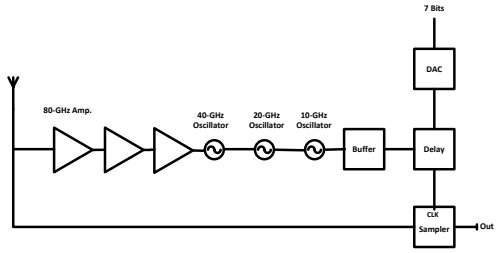

Figure 1: The architecture for an impulse receiver based on injection locking

In our second proposed circuit, we are using the fact that the frequency tones included in a repetitive impulse train are separated from each other by a difference equal to the repetition rate. Thus, we can use a mixer, to mix two or more of these tones and produce an output signal synchronized with the impulse train repetition rate. We need a non-linearity that gets a combination of various frequency components (such as a pulse) and produces the 1/T component at the output. This block can be a simple diode or a bipolar transistor that has a non-linear characteristic. Note that a conventional Gilbert cell mixer cannot be used here since there is no large-signal LO signal that turns a transistor on and off. We only have one input signal (the received impulse train) and we would like to mix its various frequency components with each other. Thus, for this purpose, a single bipolar transistor is needed. The overall architecture of this synchronization system is shown in Figure 2 and it has been implemented in a 130-nm SiGe BiCMOS process.

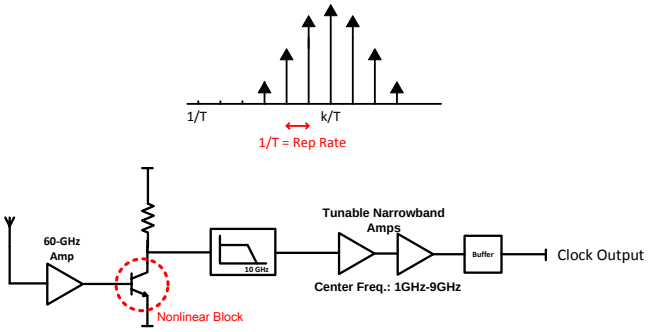

Figure 2: (a) The concept and (b) the architecture of an impulse-based clock synchronization circuit

Keywords: wireless time synchronization, millimeter-wave, low-noise receiver, ultra-short pulses, imaging arrays

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] H. Aggrawal, A. Babakhani, “A 40GS/s Track-and-Hold amplifier with 62dB SFDR3 in 45nm CMOS SOI”, 2014 IEEE MTT-S International Microwave Symposium.

TASK 1836.147, DEMONSTRATION OF 180-300 GHZ RECEIVERS FOR ROTATIONAL SPECTROSCOPY

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SIGNIFICANCE AND OBJECTIVES

One of the key components for low-cost rotational spectrometers, which can be employed for harmful gas detections and breath analyses, is a sub-mm-wave CMOS transceiver. Since ~10 μW can be transmitted into the gas under test, highly sensitive receivers are required. In this task, the development of wideband integrated receivers for rotational spectrometers will be investigated.

TECHNICAL APPROACH

A highly-integrated and wideband receiver is proposed and designed in a 65-nm CMOS process. The receiver is based on a 2nd-harmonic passive mixer. An LO driver amplifier and an intermediate frequency low noise amplifier followed by an AM detector are co-designed and integrated with the mixer to maximize sensitivity. A wideband RF/LO/IF combining and isolation structure is proposed and designed. Integration and co-optimization of wideband radiators is also investigated. The performance of the receiver will be evaluated in a spectrometer system.

SUMMARY OF RESULTS

Figure 1 depicts the block diagram of the proposed receiver architecture. In the spectrometer system, the RF input signal is amplitude-modulated and frequency-swept from 180- to 300 GHz. Since gain is not practical at RF frequency, a mixer-first architecture is employed. To lower the LO frequency requirements, 2nd-harmonic mixer topology is used. In 65-nm CMOS process, power amplification up to ~130 GHz is possible using a differential amplifier topology with a neutralization capacitors. However, wideband amplifiers at LO frequencies is inefficient in area and power. By choosing IF of 15-25 GHz, an RF signal at 200-280-GHz can be down-converted using an LO chain operating at ~120 GHz with a moderate bandwidth.

Even with the proposed high-IF architecture, the RF bandwidth of the mixer should be wide-enough to cover spectrometer frequency range. The receiving antenna should be able to handle the wide frequency range. The antenna itself can be made to have a sufficient bandwidth (Task: 1836.122). However, the interconnect between the receiver and an external antenna has limited bandwidth and operation frequency range. To overcome these limitations, an on-chip antenna is co-designed with the mixer. A differentially-fed antenna is optimized with the RF wideband hybrid. Simulated antenna gain is greater than 0 dB from 180-300 GHz frequency range.

The proposed receiver is implemented in a 65-nm CMOS process. Table I summarizes simulated receiver performance.

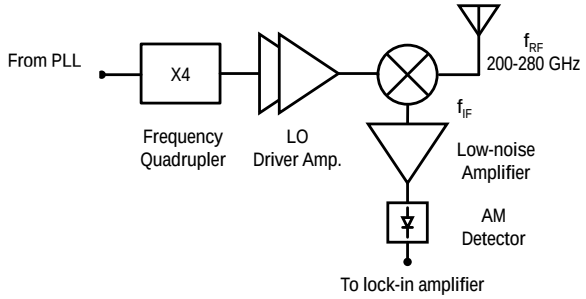

Figure 1: The receiver block diagram. IF of 15 to 25 is employed for wideband operation with narrowband LO and IF amplifiers.

Table 1: Simulated receiver performance

Antenna gain	Conversion gain	Noise figure	Detector NEP	LO PA	
				P_{out}	PAE
0-7 dB	14.5 dB	16.2 dB	2 pW/√Hz	5 dBm	20%

Keywords: integrated receiver, on-chip radiator, passive mixer, rotational spectroscopy, wideband receiver

INDUSTRY INTERACTIONS

Texas Instruments

TASK 1836.150, ROBUST HIGH RESOLUTION TECHNIQUES FOR MILLIMETER WAVE RADARS IN COMPLEX ENVIRONMENTS

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SIGNIFICANCE AND OBJECTIVES

In this task we concentrate on applications of super resolution algorithms in dynamic environments with multipath and interference. Our aim is to develop signal processing techniques so that robust imaging algorithms can be designed.

TECHNICAL APPROACH

When object to be imaged is moving in addition to its position we have the velocity parameter associated with it. Velocity is not only an additional parameter to estimate but also offers a way to separate the road clutter and other multipath reflections. This is useful especially in the case of automotive radars. Conventional estimation technique includes 2D Fourier transform to find a range-Doppler plot. However, resolution of Fourier transform for range-Doppler plot depends on the bandwidth, FMCW pulse time and number of FMCW pulses used for an estimation. Use of superresolution techniques allow us to resolve closer and smaller Doppler frequencies with limited resources.

SUMMARY OF RESULTS

Along with the reflections from the objects to be imaged, additional reflections are received from the road, curb and other unwanted objects. This is known as clutter. As clutter is often stationary it can be separated from the useful reflections in the velocity domain. However, it is important to resolve closely spaced Doppler frequencies for better control over clutter rejection algorithm. For example, in an automotive radar it is important to separate slowly moving pedestrian from a stationary roadside object.

For the FMCW radar (with modulation index K), the 2D signal collected across slow time p and fast time n, from Q objects located at R_q and moving with velocity v_q is given by:

$$d(n,p) \approx \sum_{1}^{Q} \rho_p e^{j2\pi}\left[\frac{(K\tau_q + f_{dq})n}{f_s} + (\tau_q + pTf_{dq})\right]$$

Here ρ_p is object's reflectivity, $\tau_q = \frac{2R_q}{c}$ is the roundtrip time delay and $f_{dq} = \frac{2v_q}{\lambda}$ is the corresponding Doppler frequency shift. From the equation, if we neglect the Doppler within the chirp 2D-FFT can yield range-Doppler estimation. However, more accurate estimation can be obtained if 2D joint superresolution techniques are used.

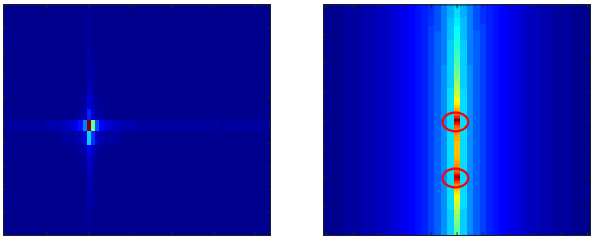

Figure 1: Range-Doppler plot using 2D FFT (left) and Range-Doppler joint superresolution (right)

The 2D data collected using the stated equation are processed for spatial smoothing and a covariance matrix is formed. A 2D MUSIC algorithm is applied for the range-Doppler joint estimation.

In Fig.1 we show two targets which are at the same distance of 10m from the radar. They are closely spaced in velocity domain with the corresponding Doppler shifts separated by 20Hz. We simulate the FMCW radar system at carrier frequency of 77 GHz with 300 MHz of bandwidth and 300 μs of FMCW pulse time. The data are discretized at SNR of 20dB and 64 samples are collected in each slow and fast time domain. Doppler resolution using traditional FT technique is $\frac{1}{PT}$=52.08Hz. Hence, these two objects cannot be separated in velocity domain. Whereas, using 2D joint MUSIC at 20 dB of SNR, we can see objects at two different speeds. Owing to the ability of this algorithm to resolve closely spaced Doppler frequencies as well as to detect smaller values, we can also deploy it detect micro-Doppler, which is useful in the industrial applications such as vibration analysis and biomedical applications such as heartbeat detection.

To reduce the complexity of implementation of these algorithms we propose to use beamspace projection. In addition we can design the projection beams in such a way that the interference from the unwanted objects is filtered.

In order to make the imaging algorithms more robust multiple antennas can be used at the transmitter, with the transmit beamforming or orthogonal transmit waveforms.

Keywords: mm-wave imaging, doppler estimation, superresolution, automotive radar, clutter reduction

INDUSTRY INTERACTIONS

Texas Instruments

TASK 1836.151, DEVELOPMENT OF DIELECTRIC WAVEGUIDES FOR THZ RADIATION APPLICATIONS

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SIGNIFICANCE AND OBJECTIVES

The task comprises the design, fabrication, test and application of novel dielectric waveguides for the propagation of THz and near-THz radiation using "holey" fiber structures to engineer the macroscopic refractive index profile and thereby supporting high-speed data transmission to provide interconnection between electronic chips and boards.

TECHNICAL APPROACH

The primary design technique is the Finite Difference Time Domain (FDTD) simulation. The material chosen is a cyclic olefin copolymer (COC) with an index of refraction of 1.5258 and a measured attenuation of <0.1 dB/cm (two orders of magnitude lower than metal waveguides) in the frequency band of interest. The fabrication platform comprises a ring of four individual heating elements enclosed in a convective shield. These elements are driven by an adjustable variac, and are instrumented with thermocouples for process control. The apparatus includes a take up spindle driven by a speed controllable DC motor.

SUMMARY OF RESULTS

The researchers work during the first year concentrated on (1) developing a robust, manufacturable design for a low loss, broadband waveguide that offers high packing density and supports both states of polarization; (2) developing a fabrication platform; and (3) the drawing of a multitude of waveguides in order to define a repeatable fabrication process. The particular waveguide design and its adherence to the data interconnect application is novel, and is the topic of a manuscript that will be prepared for publication this summer.

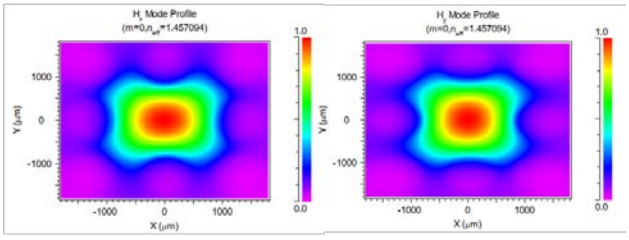

Figure 1: FDTD calculations of an 8-hole square fiber that offers robust performance over band and state of polarization. This design represents the current generation of waveguides under development in this project.

Figure 1 shows FDTD simulations for modes of s and p polarizations in a square holey waveguide at 1480 microns. The design shows robust performance and reasonable fabrication tolerances. Figure 2 shows the current waveguide fabrication platform.

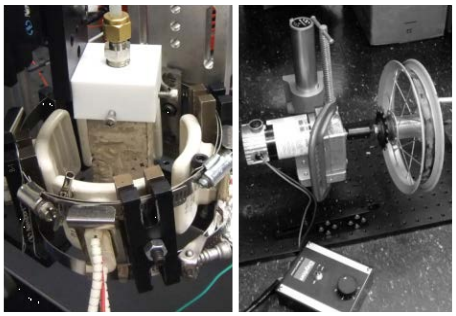

Figure 2: Second generation waveguide drawing apparatus. In Summer 2015 a third generation platform will be developed.

Figure 3 shows recent results of the eight hole waveguide. Work is being performed to refine the recipe for these waveguides.

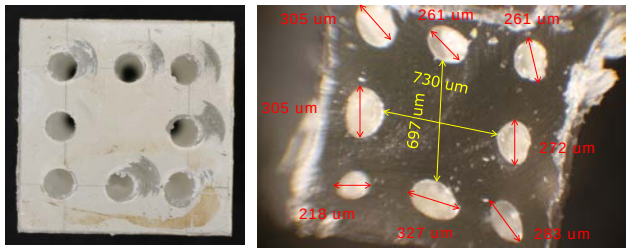

Figure 3: Photograph of a preform and Optical Micrograph of a drawn eight hole waveguide based on the design in Fig. 1 and using the drawing apparatus in Fig. 2. This waveguide is ready for functional test in the Kilby Lab at Texas Instruments.

In Year 2 the researchers will (1) functionally characterize the current generation of fabricated waveguides; (2) use these results to refine the modeling; (3) improve the fabrication platform to match the square geometry of the waveguides; (4) draw second generation waveguides; and (5) functionally test the improved waveguides.

Keywords: THz, interconnects, holey waveguides.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Nafiseh Aflakian, Naixin Yang, Timothy LaFave, Ken O and Duncan MacFarlane, "Polarization insensitive broadband holey waveguides for sub-THz interconnects," manuscript in preparation.

TASK 1836.152, FEASIBILITY OF CMOS TRANSMITTER AND RECEIVER FOR 500-GBPS COMMUNICATION OVER DIELECTRIC WAVEGUIDE

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SIGNIFICANCE AND OBJECTIVES

The increasing bandwidth of silicon integrated circuits technology is enabling a waveguide interconnection system using sub-millimeter waves that can support communication at 500-Gbps and higher. If successful, this technology will provide a bandwidth approaching that of optical systems, while bypassing the photonic component integration and coupling/packaging challenges of optical systems.

TECHNICAL APPROACH

This project in conjunction with the efforts on developing transitions and dielectric waveguides will investigate the feasibility of 500 Gbits/sec electronic communication over a 1-m dielectric waveguide using circuits fabricated in 65-nm CMOS. Use of a combination of frequency division multiple access (FDMA) (Five frequency channels), polarization division multiple access (PDMA) and a higher order signal modulation scheme will be investigated. To demonstrate the feasibility, a 120-Gbps demonstration circuit incorporating two frequency bands and two polarization modes will be implemented. Based on the results, implementation plans for a 500-Gbps dielectric waveguide communication system will be formulated.

SUMMARY OF RESULTS

Figure 1 shows a conceptual diagram of the dielectric waveguide system. It consists of transmitter, a transition/launch from the transmitter to a waveguide, a waveguide, a transition/launch from a waveguide to a receiver, and a receiver.

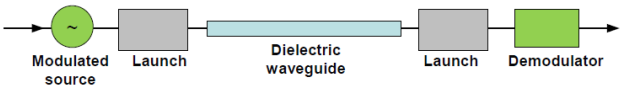

Figure 1: Conceptual diagram of the dielectric waveguide communication system.

Table 1 lists key assumptions/targets and summarizes the link margin analysis for 30-Gbps 1-m communication over a channel (1 frequency channel with a given polarization). Assuming power generated by the transmitter of -8 dBm and receiver noise figure of 28 dB, link margin of ~8 dB is projected. Since a key factor limiting the link margin is the transmitter power generation. Approaches to efficiently generate the signals at 300 GHz and higher as well as approaches to realize a receiver with sufficiently low noise figure in CMOS are being investigated.

Table 1: Link margin analyses and key performance targets

Frequency (THz)	0.18 to 0.36	Thermal noise density (dBm/Hz)	-174
Range (m)	1	Noise figure of receiver (dB)	28
TX power to transition (dBm)	-8	Bandwidth (bits/s (dB-Hz)) 30Gbps	105
Propagation loss	2.5	E_b/N_o	15
RX transition loss (dB)	3.5	Sensitivity (dBm)	-26
TX transition loss (dB)	3.5	Link margin (dB)	8.5
Received power (dBm)	-17.5		

Figure 2 shows the frequency tripler that was used to generate -3.2 dBm of power at 447 GHz in a 65-nm CMOS process with 10 metal layers. It utilizes an accumulation mode symmetric varactor (n-type and p-type varactors in parallel) structure to achieve conversion loss of 15.2 dB. For signal generation at higher than the f_{max} of transistors, this varactor-mode frequency multiplication should have higher conversion efficiency. The input to the multiplier is a 12-dBm 149-GHz signal which can be generated in 65-nm CMOS. This indicates it will be possible to generate the required carriers with sufficient power in 65-nm CMOS. As a matter of fact, it can be higher than the required and it should be possible to increase the link margin.

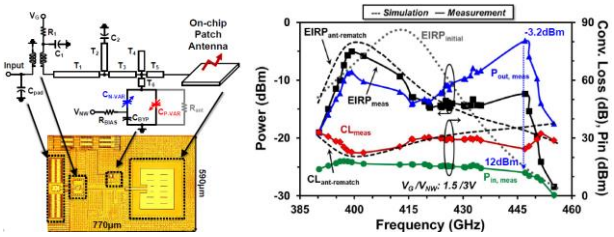

Figure 2: (Left) Circuit schematic and die photograph of a frequency tripler used to generate a 447-GHz signal. (Right) conversion loss and Effective Isotropic Radiated Power (EIRP) versus output frequency.

Keywords: dielectric, waveguide, communication, sub-millimeter, waves

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Z. Ahmad, I. Kim, and K. K. O, "0.39-0.45THz Symmetric MOS-Varactor Frequency Tripler in 65-nm CMOS," Accepted to 2015 RFIC Symposium.

[2] Z, Ahmad and K. K. O, "0.65-0.73THz Quintupler with an On-Chip Antenna in 65-nm CMOS," Accepted to 2015 IEEE VLSI Symposium on Circuits.

TASK 155, DEVELOPMENT OF WIDEBAND VIBRATION SENSORS

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SIGNIFICANCE AND OBJECTIVES

The objective of this project is to design, implement, and optimize a very low power CMOS integrated vibration sensor that can operate over a wide range of frequency from DC to 20kHz, with a resolution of 1mG or better. Both piezoresistive and MEMS resonant strain gauges are under investigation.

TECHNICAL APPROACH

The goal is for the sensors to be realized without adding any extensive modifications to an existing TI CMOS process platform. The plan is to utilize the processed thinned-down electronic chips as the mechanical component itself. The thinned-down chip would respond to vibrations in the form of bending that induces tensile and compressive stresses on different locations of the chip. The stress can be detected by strategically placing piezoresistors or MEMS resonators at the maximum stress locations. Readout circuitry will be integrated on the same chip along with the sensor components.

SUMMARY OF RESULTS

COMSOL Finite element analysis for a variety of sensor dimensions and designs was carried out to obtain stress/strain amplitudes resulting from vibrations as well as sensor frequency response and bandwidth. Extensive simulations were performed to determine optimal chip dimensions, mounting and other design parameters. It turned out that achieving 1mG sensitivity using non-silicon piezoresistors would be quite challenging. Figure 1 shows the COMSOL simulation of a chip modified for maximizing sensitivity. After the CMOS process, a deep trench would be etched on the backside of the chip exactly underneath the strain gauges, so that the sensing elements experience the maximum stress on the chip due to vibrations. To further improve the sensitivity of the sensor, an added mass of a highly dense material can be glued to the free end of the chip as shown.

TI LBC8LV CMOS process was chosen for fabrication of the first set of sensors. The process was thoroughly studied to develop an understanding of the process flow, design rules, and different available layers and capabilities. This process contains silicon-chrome resistors that are highly stable over temperature and would therefore be a good option for implementation of the strain gauges. For this first run a number of simple test structures with both Si-Cr and n-well resistors configured in wheatstone bridges were included on a 2x2mm^2 chip. In addition, some MEMS test structures were also added to this preliminary layout to assess the ability to create suspended structures out of a standard CMOS process with minimal post-processing.

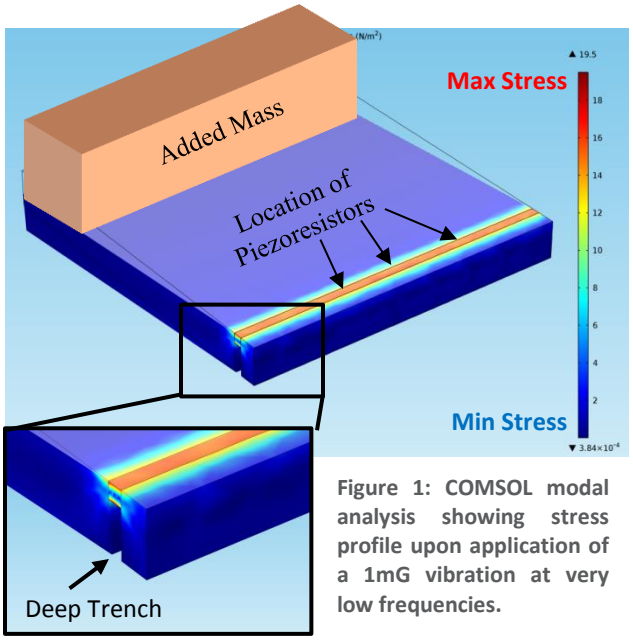

Figure 1: COMSOL modal analysis showing stress profile upon application of a 1mG vibration at very low frequencies.

Keywords: vibration sensor, low power, CMOS MEMS integration, high sensitivity, piezoresistive sensing, MEMS resonator.

INDUSTRY INTERACTIONS

The UTD team has had frequent interactions with Texas Instruments personnel in regards to the development of the proposed ideas and evaluating various TI processes for implementation. Dr. Ajit Sharma and Dr. Terry Sculley from TI Kilby labs and Dr. Patrick Oden from TI DLP division have been working closely with the UTD team.

MAJOR PAPERS/PATENTS

TASK 1836.156, TRANSITION DESIGN FOR HIGH DATA RATE LINKS AT SUBMILLIMETER WAVE FREQUENCIES

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SIGNIFICANCE AND OBJECTIVES

The objectives of this research are to design and fabricate transitions that interconnect RF signals (180 to 360 GHz) generated from CMOS transceiver integrated circuits (ICs) to dielectric waveguide for high data rate communication links.

TECHNICAL APPROACH

The collaborative research seeks to provide an all-electronic solution to high data rate communication systems. By utilizing the increased bandwidth of silicon integrated circuits along with the design of dielectric waveguides, the project aims to demonstrate data rates up to 500 Gbps for a distance of up to 1 meter. This specific project focuses on the design of a broadband transition that interfaces between the on-chip antennas used to carry the RF signals and the dielectric waveguide used to transport the signal over the 1 meter distance. The IC will be mounted onto a package that will emulate a broadband horn reflector. This reflector will interface with a holey-fiber designed using high performance polymers as shown in Figure 1.

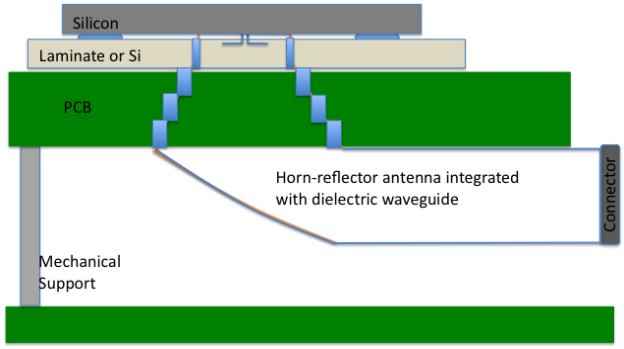


Figure 1: Concept of transition between IC and waveguide.

SUMMARY OF RESULTS

The research has involved the simulation and design of a horn reflector antenna, which we believe will be instrumental in serving as a broadband transition from the dielectric waveguide to the integrated circuit. Extensive simulations have been conducted in ANSYS HFSS to understand the parameter space associated with the horn reflector.

Ten multiband transceivers will have carrier frequencies ranging from 180 to 360 GHz. The signals will be multiplexed on-chip and fed through the transition which is depicted as a horn in Figure 1. Using the capability of printed circuit board multilayer manufacturing processes, we have been studying waveguides similar to substrate integrated waveguide (SIW) where vias are placed at distances less than a $\lambda/10$ along the transmission line length. It effectively looks like a metallized waveguide although does not require full metallization. We will be creating a square waveguide as shown in Figure 2. The guide has dimensions of inner diameter = 480 μm, outer diameter = 840 μm, with vias of 80 μm, ε_r = 3, thickness of 200 μm.

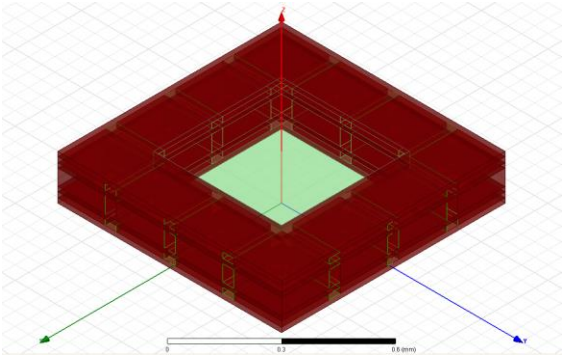


Figure 2: FR4 square waveguide realized with stacked vias.

The performance of the simulated waveguide is shown in Figure 3 where the cutoff frequency is 180 GHz and the insertion loss (IL) is 0.02 dB at 200 GHz.

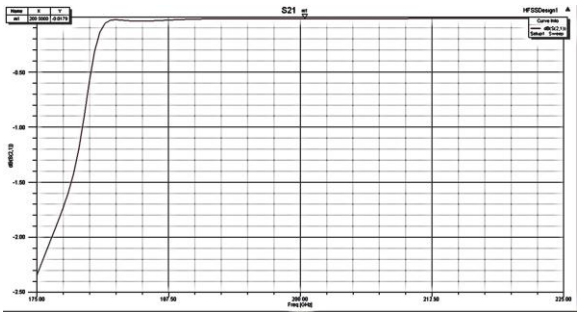


Figure 3: Simulated IL of square waveguide up to 225 GHz.

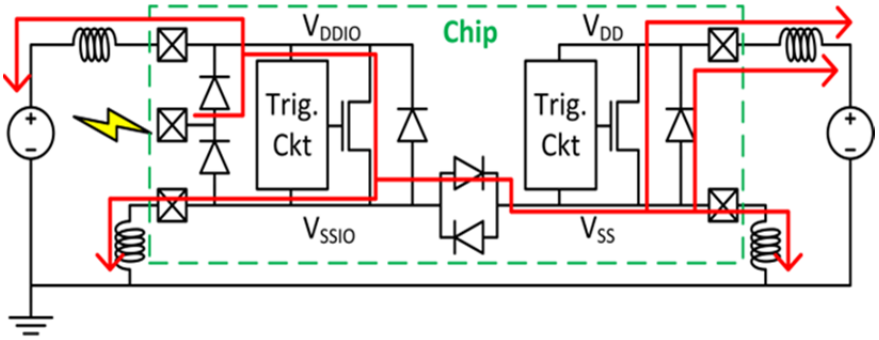
Keywords: horn reflector antenna, dielectric waveguide, printed circuit board

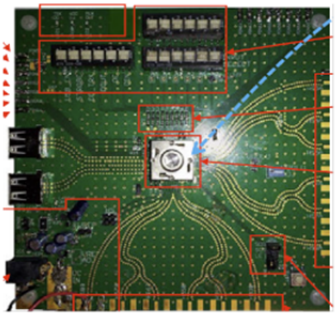
INDUSTRY INTERACTIONS

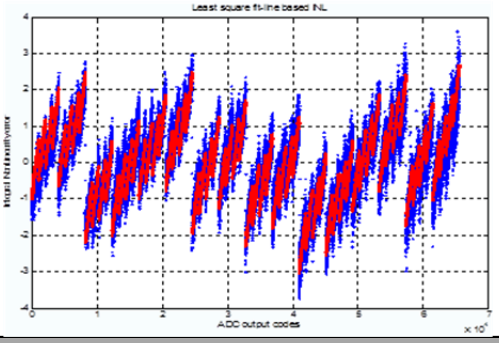
Texas Instruments

MAJOR PAPERS/PATENTS

Fundamental Analog Thrust







Category	Accomplishment
Fundamental Analog	System-level ESD is quite different from component-level ESD reliability yet IC designers are asked to build-in system-level ESD resilience. This is particularly true for systems with multiple power domains. Using data from fabricated system-level designs researchers have developed new models for system-level ESD failure and have shown that ground bounce may be the critical failure mechanism. (1836.141 PI: E. Rosenbaum, Urbana-Champaign)
Fundamental Analog	In general, testers have to be more accurate than the device under test for quality assurance increasing the production test costs for data converters. Techniques that systematically model and remove measurement uncertainty to reduce test costs are demonstrated. In particular, the histogram tests are inefficient and the proposed techniques reduce test time by three orders of magnitude. These techniques have been validated in production by a member company. (1836.127 PI: D. Chen, Iowa State)

1836.075, DESIGN OF 3D INTEGRATED HETEROGENEOUS SYSTEM

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SUNG-KYU LIM, GEORGIA INSTITUTE OF TECHNOLOGY

SIGNIFICANCE AND OBJECTIVES

The objective of this research is to address the challenges to 3D integration of highly different circuits/systems in varying technologies, power profiles, operating voltage, and clock domains through the 3D technology using Through-Silicon-Via (TSV) technology.

TECHNICAL APPROACH

The performance, power, and reliability of a 3D-Integrated Heterogeneous System (3D-IHS) depend on the functionality, power profile, and frequency of individual dies; the non-uniformity in their physical environments; die-to-die coupling; and die-to-package coupling. This research is working to develop design methods for the 3D-IHS and transform them into design tools.

SUMMARY OF RESULTS

Design of Gate-Level Monolithic 3D-IC [1]: In a gate-level monolithic 3D IC (M3D), all the transistors in a single logic gate occupy the same tier, and gates in different tiers are connected using nano-scale monolithic inter-tier vias. This design style has the benefit of the superior power-performance quality offered by flat implementations (unlike block-level M3D), and zero total silicon area overhead compared to 2D (unlike transistor-level M3D). In our work published at ISLPED'14, we develop, for the first time, a complete RTL-to-GDSII design flow for gate-level M3D. Our tool flow is based on commercial tools built for 2D ICs and enhanced with our 3Dspecific methodologies. We use this flow along with a 28nm PDK to build layouts for the OpenSPARC T2 core. Our simulations show that at the same performance, gate-level M3D offers 16% total power reduction with 0% area overhead compared to commercial quality 2D IC designs.

Design of Block Level Monolithic 3D-IC [2]: In our work published at DAC'14, we study the power vs. performance tradeoff in block-level monolithic 3D IC designs. Our study shows that we can close the power-performance gap between 2D and a theoretical lower bound by up to 50%. We model the inter-tier performance variations caused by a low temperature manufacturing process on the non-bottom tiers. We also model an alternate manufacturing process, where highly resistive tungsten interconnects are used on the bottom tier to withstand a high temperature process on the non-bottom tiers. We propose a variation-aware floor planning technique that makes our design more tolerant to these variations. We demonstrate that our design methods can help us obtain high quality designs even under inter-tier performance variations.

Thermal Behavior of Monolithic 3D IC[3]: In another work published at DAC'14, we present a comprehensive study of the unique thermal behavior in monolithic 3D ICs. In particular, we study the impact of the thin inter-layer dielectric (ILD) between the device tiers on vertical thermal coupling. In addition, we develop a fast and accurate compact full-chip thermal analysis model based on a non-linear regression technique. Our model is extremely fast and highly accurate with an error of less than 5%. This model is incorporated into a thermal-aware 3D-floorplanner that runs without significant runtime overhead. We observe up to 22% reduction in the maximum temperature with insignificant area and performance overhead.

Asynchronous Interface for Die-to-Die Communication in 3D ICs: We have designed and analyzed an asynchronous FIFO to enable die-to-die communication between multiple dies operating at different VDD and frequency in a heterogeneous 3D IC. Different partitioning method for FIFO has been investigated: (i) split FIFO - where the read/write circuits of the FIFO are split between two dies and (ii) FIFO on reading die – where the FIFO is placed in the reading core die; and (iii) FIFO on writing die - where the FIFO is placed in the reading core die. The effect of process variations in the individual dies (die-to-die variation) i.e. the logic blocks sending/receiving data as well as the FIFO circuits are considered. The analysis shows the splitting the FIFO equally between two dies results in a lower footprint; however, increases power consumption.

Keywords: 3D IC, monolithic 3D IC, post-silicon tuning, signal integrity, variation, ultra low power (ULP)

INDUSTRY INTERACTIONS

Intel, IBM

MAJOR PAPERS/PATENTS

[1] S. Samal et al, "Fast and Accurate Thermal Modeling and Optimization for Monolithic 3D ICs," DAC 2014.

[2] S. Panth et al, "Power-Performance Study of Block-Level Monolithic 3D-ICs Considering Inter-Tier Performance Variations," DAC 2014.

[3] S. Panth et al, "Design and CAD Methodologies for Low Power Gate-level Monolithic 3D ICs," ISLPED 2014.

TASK 1836.080, VARIATION-TOLERANT NOISE-SHAPING ADCS WITH EMBEDDED DIGITAL BIAS AND VDD SCALABLE FROM 0.5V TO 1.2V FOR NANOSCALE CMOS

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SIGNIFICANCE AND OBJECTIVES

We demonstrated different analog circuits down to 0.5V in earlier works. However, it is necessary to have further techniques to analog interfaces with flexible supplies in deep-submicron CMOS processes. We investigate digital circuit techniques to supply-scalable continuous-time sigma-delta modulators for getting the benefits and handling challenges of nano-scale short-channel devices.

TECHNICAL APPROACH

A pulse-controlled common-mode feedback circuit is proposed to overcome the large area cost associated with a conventional RC common-mode feedback circuit for supply-scalable operations. The amplifier with the pulse-controlled common-mode feedback implemented in a low power/leakage CMOS process operates at a supply voltage from 0.6V to 1.2V. A VCO-based amplifier with zero compensation is proposed to replace conventional amplifiers in analog circuits. The VCO-based amplifier has a huge DC gain without any significant associated penalties on its unity-gain bandwidth and area. A 4th-order 40-MHz active-UGB-RC filter implemented with the VCO-based amplifier offers a wide bandwidth, superior linearity and small area.

SUMMARY OF RESULTS

The circuit implementation and die photo of the fully-differential amplifier with PC CMFB are shown as Fig. 1.

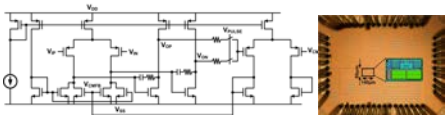

Figure 1: Circuit and die photo of the amplifier

The performance of the amplifier is summarized in Table 1 demonstrating that the amplifier with the PC CMFB in low power/leakage CMOS technology has a small area and suitable for flexible supply operation.

Table 1: Performance summary of the amplifier with PC CMFB

Technology	65nm CMOS		
V_{THN}/V_{THP}	0.36V/-0.44V		
Active Area	0.01mm^2		
Supply Voltage	0.6V	0.9V	1.2V
Common-mode Voltage	0.3V	0.45V	0.6V
Power Consumption	1.21mW	1.94mW	3.07mW
Output Noise PSD (nV/Hz$^{0.5}$)	21.5	26.1	30.3
Maximum Input Signal for 1% THD	-2.3dBm	3.8dBm	6.1dBm

The architecture and die photo of the filter using the VCO-based amplifier with zero compensation are shown in Figure 2.

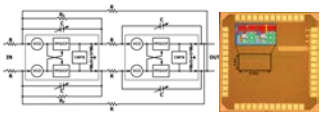

Figure 2: Architecture and die photo of the filter.

The performance comparison of the filter is summarized in Table 2 demonstrating that the active-UGB-RC filter using the proposed VCO-based amplifier offers a wide bandwidth and has superior linearity than filters using conventional amplifiers or ring-oscillator integrators. The filter has a small area and a competitive figure of merit particularly when considering the contribution of area.

Table 2: Performance comparison of the filter

	[1]	[2]	[4]	[5]	[6]	This work
Supply Voltage	0.55V	1.2V	1.0V	1.0V	1.5V	1.2V
Topology	Gm-C	Active-UGB-RC	Active-RC	Active-RC	Active-RC	Active-UGB-RC
BW (MHz)	7	11	10	20	19.7	40
Order	4	4	5	5	5	4
Noise (nV/Hz$^{0.5}$)	23.6	11	143	52	30	96
Out-of-band IIP3	-	-	-	8dBm	-	22.5dBm
In-band IIP3	8.7dBm	21dBm	21.3dBm	26dBm	18.3dBm	27.3dBm
Power (mW)	2.9	14.2	4.6	7.5	11.25	7.8
Area (mm^2)	0.29	0.9	0.25	1.53	0.2	0.07
Technology	90nm	130nm	120nm	130nm	130nm	55nm
FoM (fJ×mm^2)	0.15	0.099	0.22	0.23	0.068	0.02

Keywords: VCO-based amplifier, digital circuit technique, supply-scalable amplifier, pulse-controlled common-mode feedback, continuous-time sigma delta modulator

INDUSTRY INTERACTIONS

Texas Instruments, Freescale Semiconductor

MAJOR PAPERS/PATENTS

[1] C.-W. Hsu and P. R. Kinget, "A 40MHz 4th-order Active-UGB-RC Filter using VCO-Based Amplifiers with Zero Compensation," IEEE European Solid-State Circuits Conference, Sep. 2014.

[2] C.-W. Hsu and P. R. Kinget, "A Supply-Scalable Differential Amplifier With Pulse-Controlled Common-Mode Feedback," IEEE Custom Integrated Circuits Conference, Sep. 2014.

[3] C.-W. Hsu and P. R. Kinget, “Digital In-situ Biasing Technique,” IEE Electronics Letters, accepted, 2015.

TASK 1836.087, A HIGH-SPEED LOW-POWER CLOCK DATA RECOVERY (CDR)

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SIGNIFICANCE AND OBJECTIVES

We propose a low-voltage low-power 25Gb/s serial link receiver in a 65nm CMOS technology. Novel circuit techniques are proposed to enable the receiver to operate under 0.6V (nominal supply voltage of 1.2V) for low power consumption with a power efficiency of <2mW/Gb/s.

TECHNICAL APPROACH

Novel circuit techniques are proposed to enable low-voltage and low-power operation of a 25Gb/s serial link receiver. At the center of the receiver is a low-phase-noise VCO employing a two-tank transformer-feedback technique to achieve large signal swing under V_{DD} of 0.6V. The proposed two-tank VCO improves the qualify factor and lowers the phase noise with an ultra-low-supply voltage. Gate-biasing techniques are utilized in the varactors and capacitor array to ensure a wide tuning range of the VCO. Forward-body-biasing technique is proposed in the bang-bang phase detector to achieve large signal swing under V_{DD}=0.6V for low BER.

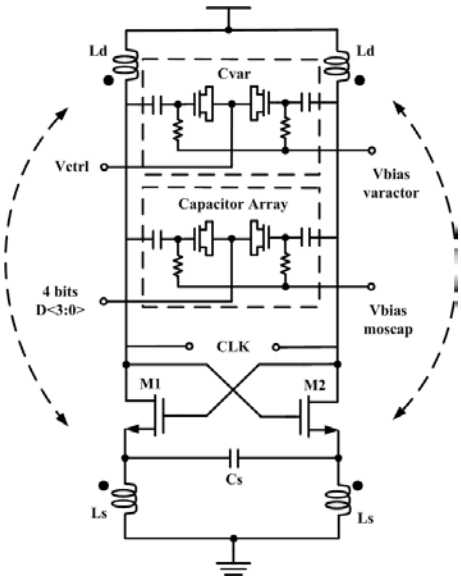

Figure 1: Proposed low-phase-noise two-tank transformer-feedback-based VCO

SUMMARY OF RESULTS

We implemented a 25Gb/s serial link receiver using 65nm CMOS with the proposed circuit techniques so that the entire receiver can be operated at V_{DD}=0.6V for low power operation and for compatibility with digital circuitry with decreasing V_{DD}. The receiver including the Continuous-Time Linear Equalizer (CTLE) consumes 55mW at 25Gbps, achieving a power efficiency of <2mW/Gb/s.

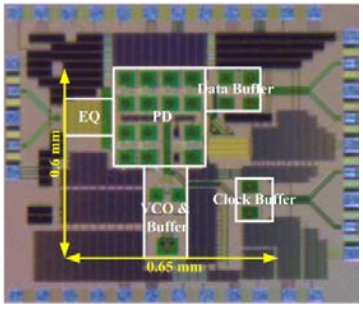

Figure 2: Chip microphotograph of the 25Gb/s serial link receiver

TABLE1 MEASUREMENT PERFORMANCE SUMMARY

Data Rate	24.12 Gb/s – 26.07 Gb/s
Supply Voltage Vdd	0.6V (Nominal 1.2V)
Power Consumption	48.8mW
Recovered Clock Jitter	0.23 ps, rms; 4.62 ps, pp
Recovered Data Jitter	0.91 ps, rms; 7.62 ps, pp
Area	0.6 x 0.65 (mm^2)
Technology	65nm CMOS

Keywords: clock data recovery (CDR), low voltage, low power, serial link receiver

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] S. Guo, et al., "A Low-Voltage Low-Power 25 Gb/s Clock and Data Recovery with Equalizer in 65 nm CMOS," IEEE RFIC 2015.

[2] G. Wu, et al., "A 1-16 Gb/s All Digital Clock and Data Recovery with a Wideband, High-Linearity Phase Interpolator," *IEEE Transactions on VLSI* in press.

[3] T. Xi, et al.," Low-Phase-Noise 54GHz Quadrature VCO and 76GHz/90GHz VCOs in 65nm CMOS," IEEE RFIC 2014.

TASK 1836.093, VARIABILITY-AWARE, DISCRETE OPTIMIZATION FOR ANALOG CIRCUITS

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SIGNIFICANCE AND OBJECTIVES

While analog circuit optimizers, that can automatically size transistors in a circuit according to a prescribed performance metric, can be an effective productivity tool for analog, yet the reality is that their adoption into the mainstream flows has been rather slow. Exploiting the inherent uncertainty in IC process, this task aims to explore the use of discrete optimization techniques for realizing a fast, deterministic optimizer that can perform quick, incremental 'what-if' analysis.

TECHNICAL APPROACH

While analog design parameters are typically of continuous values, we assert that such a continuous design space can be effectively covered with a set of finite, coarsely-spaced, discrete points by exploiting the inherent variability in the IC technology. Our expectation is that a discrete optimizer can solve many of the problems faced with the existing, continuous optimizers for analog circuits.

However, since one weakness of a discrete optimization approach is its poor scaling with the problem dimensionality, various approaches have been investigated, including a predictive global search algorithm and a hierarchical optimization approach based on Pareto-front extraction.

SUMMARY OF RESULTS

Previously, we have proposed three novel algorithms to leverage a discrete optimization technique while mitigating its limitation in dimensionality scaling [2]: an isotropic discretization scheme, a stochastic hill-climbing algorithm, and an incremental Monte Carlo simulation algorithm. We have demonstrated that these algorithms are effective in finding the optimal design [2] as well as exploring the design trade-offs such as yield-aware Pareto fronts [3].

This year, we have completed the implementation of a new, predictive global search algorithm in the discretized design space [1],[4]. The optimizer starts with a set of randomly chosen pilot samples and builds a yield-aware response-surface model to predict the outcome of the unexplored design candidates. Then, it evaluates the most promising candidates to provide the better outcome and updates the response surface model. The process continues until the probability of finding the better outcome drops below a certain threshold. The key advantage of this approach is that 1) the discretized design space provides a notion of coverage, as the number of design candidates within any given area is finite, and 2) the optimizer finds the optimum solution fairly early in the process, rather than reaching it at the very last step, enabling quick interactions with the designers (Figure 1).

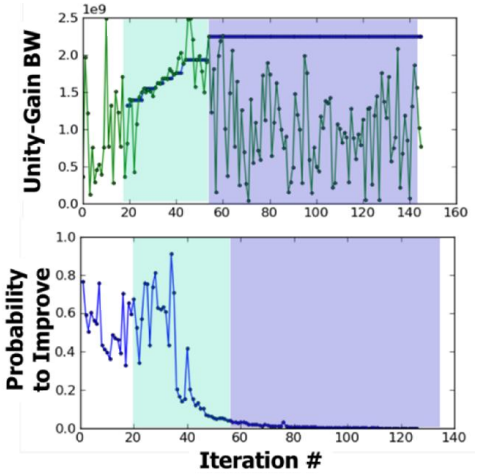

Figure 1: The search process of the predictive global circuit optimizer, demonstrating the early discovery of the optimum point and comprehensive coverage of the design space.

Keywords: analog circuit synthesis, circuit optimization, discrete optimization, predictive global optimization.

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

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[2] S. Jung, J. Lee, and J. Kim, "Variability-Aware, Discrete Optimization for Analog Circuits," Trans. on Computer-Aided Design, 2014.

[3] S. Jung, J. Lee, and J. Kim, "Yield-Aware Pareto-Front Extraction for Discrete, Hierarchical Optimization of Analog Circuits," Trans. on Computer-Aided Design, 2014.

[4] J. Kim, et al., "Discretization and Discrimination Methods for Design, Verification, and Testing of Analog/Mixed-Signal Circuits," Custom Integrated Circuits Conf., 2013.

TASK 1836.095, TEST GENERATION FOR MIXED-SIGNAL DESIGN VERIFICATION AND POST-SILICON DEBUGGING

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SIGNIFICANCE AND OBJECTIVES

We work towards the development of transformative theory, techniques, and tools for generating test benches and vectors used to drive circuit simulation for mixed-signal design verification and post-silicon debugging. The generated test vectors are minimal length, and can sensitize the worst-case errors in embedded analog blocks in digital-intensive analog designs.

TECHNICAL APPROACH

The proposed methodology utilizes automated silicon-faithful behavioral modeling, which generates abstracted behavioral models from a transistor netlist. The key technical components are: (1) to incorporate design-specific functional, performance and reliability factors in automated model generation for design functional verification and post-silicon debugging (2) to represent a complex mixed-signal integrated circuit by a system-level signal path diagram based on automatically generated behavioral models (3) to generate the candidate test benches and vectors based on signal types and signal path diagrams (4) to use optimization to derive the minimal length simulation vectors for verification and debugging.

SUMMARY OF RESULTS

Through discussions with industry liaisons at Intel and TI, one sub-problem of the principal goal that is currently under investigation, is the generation of minimal length test vector that will maximize instantaneous current in analog and mixed-signal circuit. The proposed method finds application in burn-in test during High Volume Manufacturing (HVM) test phase.

An automated tool has been developed to identify path activation conditions of the Channel-connected component (CCC) through localized circuit simulation of the components. A flow that formulates the extracted path activation conditions as a weighted satisfybility modulo theory (SMT) problem has been developed. A preliminary case study of representative mixed-signal circuit demonstrates that the EDA tool underdevelopment is effective in identifying DC bias conditions and digital configurations that will yield high current in either selected metal wire or the power line [1].

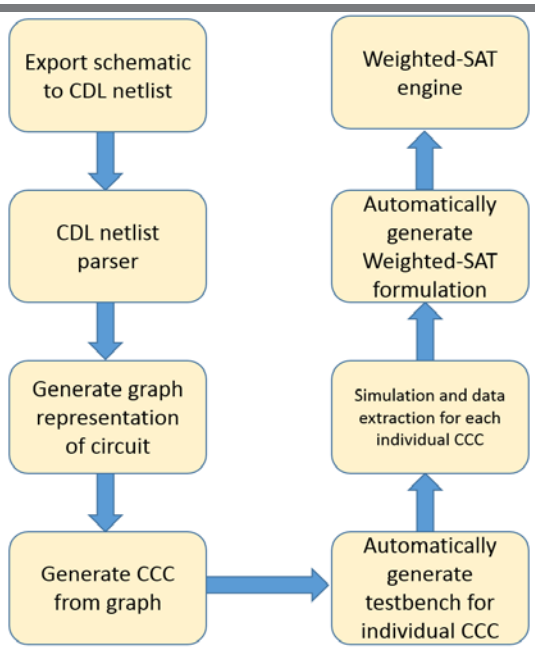

Figure 1: An automated flow for identifying current maximization condition for a mixed-signal circuit [1]

The automated EDA flow described in [1] will be applied industry test circuit provided by the industry liaisons at TI and Intel.

The next step is to investigate representing a complex mixed-signal circuit by a system-level signal path diagram based on automatically generated behavioral models. With the behavioral models and the weighted SMT formulation, we will develop techniques to generate minimal-length verification tests to sensitize potential failure in an integrated analog block.

Keywords: post-silicon debugging, verification, test generation, behavioral model

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] Chong Li, "Test generation for maximum instantaneous current in analog and mixed-signal circuit", SRC TECHCON, Sep 2015, Austin, TX.

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TASK 1836.096, MIXED-SIGNAL DESIGN CENTERING IN DEEPLY-SCALED TECHNOLOGIES

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SIGNIFICANCE AND OBJECTIVES

A methodology for robust design of high-performance analog circuit blocks in highly-scaled technologies is being investigated, to enable rapid yield ramp-up in scaled technologies.

TECHNICAL APPROACH

We are developing a methodology that enables centering with respect to technology variability of high-performance mixed-signal signal designs in as few as one design iteration. It is based on the components, which are developed simultaneously:

- Instrumenting critical design components to accurately monitor impact of process variability on their performance.
- Creating a dedicated set of representative circuit primitives for their full variability characterization.
- Extracting a variability model from the test structures; building simplified Spice models to predict the distribution spread of critical components.

These components enable centering of critical analog blocks, such as clock and data recovery loops and high-performance data converters.

SUMMARY OF RESULTS

We have developed an algorithm based on backward propagation of variability to improve yield prediction capability of existent models. The algorithm uses the equation below, where e_i is the measurement data and p_j the parameter values, to update the parameter variation values, including parameter correlations in the model.

$$\sigma^2_{\Delta e_k} = \sum_{k=1}^{n} \left(\frac{\partial e_i}{\partial p_k} \right)^2 \sigma^2_{\Delta p_k} + 2 \sum_{(u,v)} \frac{\partial e_i}{\partial p_u} \frac{\partial e_i}{\partial p_v} \mathrm{cov}(\Delta p_u, \Delta p_v)$$

This underdetermined system is solved using a constrained LMS method to limit the solution space. Figure 1 shows the results of this method (red) compared against MC simulation results (blue). This algorithm is applied to data extracted from representative test structures and building blocks to hierarchically capture variability and propagate distributions from devices, via components to systems.

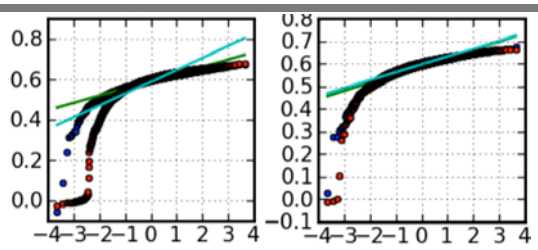

Figure 1: Simulated QQ plots of the VTH distribution using the conventional solution (left) and the constrained LMS solution (right).

To illustrate this approach we have designed test structures to center comparators, which are key components of mixed-signal systems such as clock-and-data recovery loops. These structures target characterizing offset and impulse sensitivity functions, which are then related to variability measured by I-V data of individual devices.

Two test chips have been designed. One test chip has been sent out for fabrication in 28nm FDSOI process which contains large comparator arrays for measuring distributions of offsets, impulse sensitivity functions and transistor I-V characteristics (Figure 2). The second test chip, designed in 28nm HPM technology contains a set of SRAM sense amplifiers.

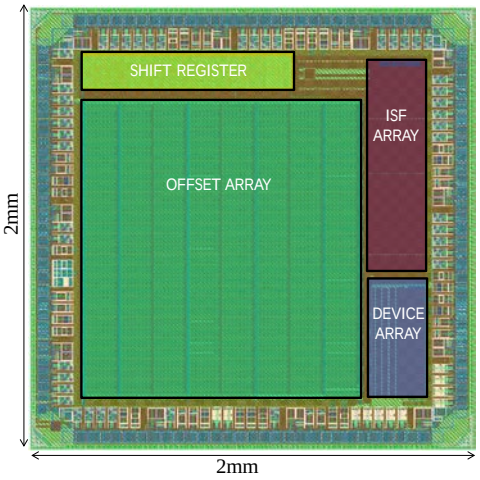

Figure 2: Layout of the 28nm test chip.

Keywords: CMOS, variability, yield, design optimization, clock and data recovery.

INDUSTRY INTERACTIONS

Intel

TASK 1836.097, DUAL-DOMAIN SAR ADCS INCORPORATING BOTH VOLTAGE AND TIME INFORMATION

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SIGNIFICANCE AND OBJECTIVES

The purpose of this work is to use a combination of voltage- and time-domain information to improve SAR ADC design. One objective is signal-proportional energy consumption, meaning that periods of low signal activity consume very little energy. A second objective is to extend use of SAR ADCs to delta-sigma modulators.

TECHNICAL APPROACH

A conventional SAR algorithm resets the capacitive feedback DAC between conversions. While some output codes consume more capacitor switching energy than others, the average energy over many conversions is not correlated to signal activity; quantizing a DC input is equally expensive as quantizing a full-scale Nyquist-rate input.

To achieve signal-dependent energy consumption, the major concept is that the DAC begins with the output of the previous conversion result, rather than being reset. For low-activity signals, the conversion consumes very low energy (and complete in fewer cycles). Of course, for high-activity signals it will be more expensive than the conventional algorithm.

SUMMARY OF RESULTS

Several new techniques were proposed for predictive SAR algorithms, taking advantage of periods of low signal activity to reduce power consumption. The work in [1] modifies a previous LSB-first SAR ADC [2] to avoid unnecessarily large DAC switching events. The modification causes the LSB switching steps to sometimes be repeated, which achieves better energy efficiency and faster conversion times when processing the low-activity for which LSB-first SARs are intended.

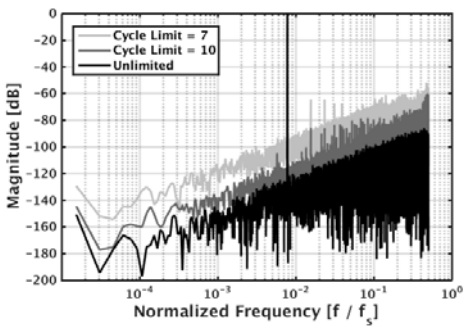

Figure 1: Effects of limiting LSBFQ bitcycles in DSM are increased noise floor and distortion (shown for 10b).

Another innovative result was the use of LSB-first SAR quantizer (LSBFQ) in a delta-sigma ADC [3]. For a high multibit DSM (Delta Sigma Modulator) with a high oversampling ratio, the quantizer processes a signal with relatively low activity and the LSBFQ is shown to be an ideal solution. In order to avoid clocking the quantizer significantly faster than the rest of the circuit, it is provided a fixed number of comparison cycles then interrupted regardless of whether the conversion has fully completed. In the relatively rare events that the LSBFQ is cut off, it is equivalent to injecting more quantization error into the loop filter and is filtered/shaped without significantly degrading the SNDR. This result is shown in Figure 1.

The final contribution towards adaptive SAR algorithms is the selectable starting bit SAR presented in [4]. Depending upon the signal activity, the best-case energy efficiency is sometimes achieved through a conventional MSB-first conversion, sometimes through an LSB-first conversion, and sometimes by beginning with some intermediate SAR bit. The index of the starting bit can be chosen by the designer to optimize the energy-efficiency for the target application, providing improved flexibility. It should be noted that the conventional SAR and LSBFQ become special cases of this generalized SAR solution.

Keywords: SAR, LSB-first, energy-efficient, adaptive, time-domain

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

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[2] F. Yaul et al., "A 10b 0.6nW SAR ADC with Data-Dependent Energy Savings Using LSB-First Successive Approximation," *IEEE ISSCC*, pp. 198-199, Feb. 2014.

[3] A. Waters et al., "A Delta-Sigma ADC Using an LSB-First SAR Quantizer," *IEEE ISCAS*, May 2015.

[4] J. Leung et al., "Selectable Starting Bit SAR ADC," *IEEE ISCAS*, May 2015.

[5] S. Leuenberger et al., "A Single Opamp 2nd-Order Delt-Sigma ADC with a Double Integrating Quantizer," *IEEE ISCAS*, May 2015.

TASK 1836.107, VERIFICATION OF MULTI-STATE VULNERABLE AMS CIRCUITS

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SIGNIFICANCE AND OBJECTIVES

The objective is to develop a systematic procedure that detects presence or absence of multiple equilibrium operating modes in basic AMS circuits that can be used to verify that circuits are void of Trojan operating modes. This will prevent fabrication of circuits that fail when they enter a Trojan model.

TECHNICAL APPROACH

A mapping of a netlist description of the resistive representation of an AMS circuit to a graphical representation that preserves feedback loops has been developed for determining if the circuit is vulnerable to the existence of multiple stable equilibrium points. In this phase of the project, emphasis has been placed on studying analog circuits that are vulnerable to multiple dynamic modes of operation. A prototype oscillator and filter circuits have been identified that have more than one stable dynamic mode of operation whereby one mode of operation is the desired mode and the other mode or modes represent Trojans in the circuit.

SUMMARY OF RESULTS

One circuit that can exhibit multiple dynamic modes of operation is the Wien-Bridge oscillator shown in Fig. 1. By making slight changes in the nonlinearity of the Finite Gain Amplifier block, the oscillator can be made to exhibit two or more stable modes of oscillation. Triggering between the different modes can occur by setting different initial conditions on the two capacitors. Two modes of oscillation for a slight change in the amplifier nonlinearity are shown in Fig. 2.

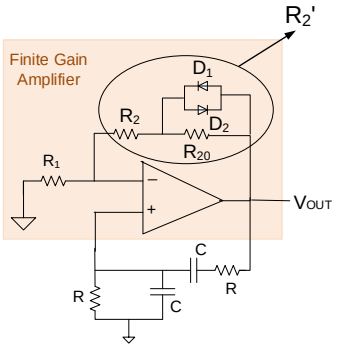

Figure 1: Wien-Bridge Oscillator with Multiple Dynamic Modes of Oscillation

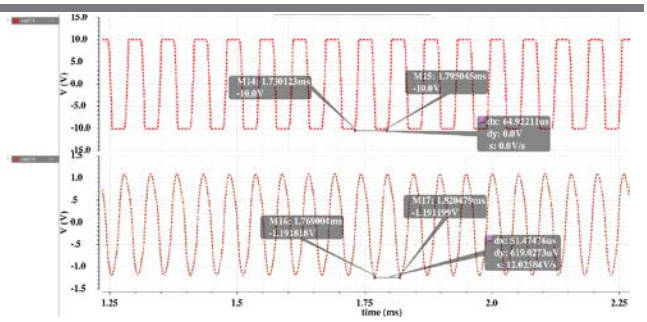

Figure 2: Two Stable Dynamic Modes of Oscillation

Other filter and oscillator circuits have been designed that also have two or more dynamic modes of operation. One Sallen and Key type filter structure behaves as a filter under one set of initial conditions and as an oscillator under a different set of initial conditions.

The undesired dynamic modes of operation can be extremely difficult to detect with existing simulation and verification tools thereby creating a concern for undetected design oversights and a vulnerability for adversarial insertion of analog hardware Trojans.

Keywords: dynamic modes of operations, Wien-bridge oscillator, trojan states, verification, analog hardware trojans

INDUSTRY INTERACTIONS

Texas Instruments, Freescale, Intel

MAJOR PAPERS/PATENTS

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[2] Z. Liu et al., “Identification and break of positive feedback loops in Trojan States Vulnerable Circuits”, ISCAS, pp. 289-292, May 2014.

[3] S. Liu et al., “A Graphical Method for Identifying Positive Feedback Loops Automatically in Self-Biasing Points”, NAECON, pp. 384-390, July 1014.

[4] Y. Wang et al., “Hardware Trojan State Detection for Analog Circuit and Systems”, NAECON, pp. 364-367, July 1014.

[5] Z. Liu et al., “Feedback Loops and Trojan States: Hardware Threats to Trusted Analog Circuits”, GOMAC, St. Louis, pp. 431-434, March 2015.

TASK 1836.109, NEW PARADIGMS FOR HIGH-PERFORMANCE AMPLIFICATION

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SIGNIFICANCE AND OBJECTIVES

Amplifiers are increasingly power hungry and difficult to build in nanoscale CMOS. This has created a serious crisis that affects us all, particularly in the era of SoCs. The techniques presented offer new paradigms for scalable high-performance amplification in a variety of applications.

TECHNICAL APPROACH

Ring amplifiers are one such high performance amplifier that can meet the needs of a scalable amplifier. Although ring amplifiers possess many of the desired features of a scalable amplifier, there are still unknown design details about them. In particular their noise performance has not been determined. By first determining the noise performance of a ring amplifier particular in its relation to the deadzone. Using this knowledge the deadzone can be designed to improve amplifier noise performance.

SUMMARY OF RESULTS

Typically, in traditional operational amplifiers the bandwidth is typically proportional to the 1st stage transconductance while the input referred noise density is inversely proportional. Since, noise power is the integral of the noise power spectral density over all frequencies improving noise performance comes at the cost of increased load or compensation capacitors to reduce the bandwidth while maintaining a low noise density.

The bandwidth of a ring amplifier is not as easily understood. This is because during amplification it is variable, but in a ring amplifier it can be generalized that the bandwidth will go from high to low. The major effort in this work has been how to design the ring amplifier that this effect can be maximized.

The major defining feature of the ring amplifier is its deadzone. It is also one of the most important parameters for a designer to control. Therefore, the noise of a ring amplifier was investigated to its deadzone. When compared with the same deadzone sweep but instead looking at amplifier performance it was found that in order to maximize both distortion and noise performance the deadzone should be moved from small (high bandwidth) to large (small bandwidth). This new dynamic deadzone is used to improve noise performance in low feedback factors.

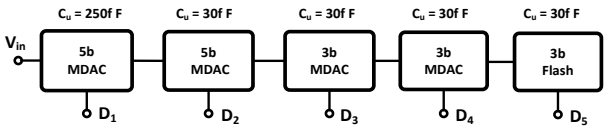

Figure 1: Structure of 15b Pipeline ADC with 1b redundancy

An ADC was designed to test this theory. It is a 15b resolution pipeline ADC. Of note is the fact that compared to the previous ring amplifiers based ADC this one was designed to not be thermal noise limited. Figure 1 shows the overall structure of this ADC. It was designed to have 8 pF of sampling capacitance. Overall the sampling speed of 10 MHz. Extracted results show a power consumption of approximately 2mW. This ADC was taped out in 180-nm CMOS.

The 1st and 2nd stages of the Pipeline ADC are of higher resolution then the rest of the stages in order to demonstrate the effectiveness of the dynamic deadzone as show in Figure 2. Without the dynamic deadzone either the amplifier will not settle fast enough or the noise performance will be degraded

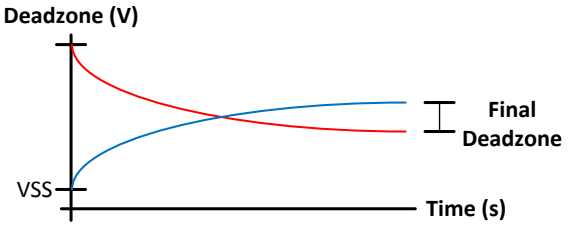

Figure 2: Dynamic Deadzone Waveforms

Keywords: ring amplifier, noise performance, high resolution, scalable amplification.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] F. Farahbakhshian et al., "Stochastic Approximation Register ADC," *IEEE NEWCAS*, June, 2014.

[2] B. Hershberg et al., "The Ring Amplifier: Scalable Amplification with Ring Oscillators," AACD, April 2014.

TASK 1836.111, ADVANCED ADC-BASED SERIAL LINK RX ARCHITECTURES

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SIGNIFICANCE AND OBJECTIVES

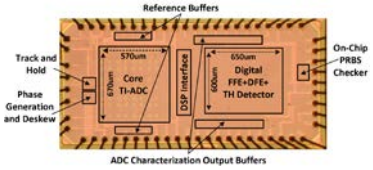
While CMOS technology scaling allows for the efficient implementation of powerful on-chip DSP algorithms for equalization and symbol detection, ADC-based receivers are generally more complex and consume higher power. The proposed ADC-based serial link techniques aim to significantly improve interconnect bandwidth density in an energy-efficient manner.

TECHNICAL APPROACH

In order to investigate design trade-offs, a novel statistical-modeling framework for advanced ADC-based serial links will be developed. This tool will be used to guide the design of a new hybrid ADC-based receiver architecture which combines in a power optimum manner equalization embedded in the ADC and dynamically power-gated digital equalization based on threshold detection, with an ultimate target data rate in excess of 25Gb/s. The statistical modeling framework and receiver prototypes will be leveraged to investigate the performance of the hybrid ADC architecture with multi-level modulation schemes (duobinary, PAM4, PAM8, etc.) and error correction coding.

SUMMARY OF RESULTS

In order to relax ADC-based RX power and complexity, partial equalization can be embedded inside the ADC and not be limited by the ADC resolution. To explore this, a 6b 10GS/s SAR ADC with embedded 2-tap FFE and 1-tap DFE was implemented in a GP 65nm CMOS process and achieved 4.56b ENOB at 0.48pJ/conv. [1]. While this provides improved BER, additional eq. is generally required to support channels with loss >30dB. This is addressed in an energy-efficient manner with a new hybrid ADC-based RX architecture which combines embedded ADC equalization and dynamically-enabled digital eq. based on threshold detection [2]. In this scheme, the ADC output is considered as a reliable decision if the value exceeds a threshold, which can also serve as an indication that further eq. is necessary on a sample-by-sample basis. A 10Gb/s RX prototype with a 3-tap analog FFE embedded inside a 6-bit asyn. SAR ADC and a dynamically-enabled digital 4-tap FFE and 3-tap DFE was fabricated in GP 65nm CMOS (Figure 1). The RX compensates for up to 36.4dB loss with 30mW savings in the digital eq. power and an overall power <90mW.



(a)

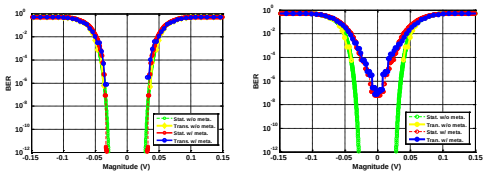
Specification	[1]	[2]	[3]	This Work	
Technology	65nm	65nm	40nm	65nm	
Power Supply (V)	N/A	1.1	N/A	1	
ADC Structure	Flash	Variable V_{REF} Flash	Rectifier Flash	TI-SAR	
Pre-Equalization	4 taps FIR (@ TX)	HPF + 2 taps FFE	N/A	Embedded 3-tap FFE	
Post-Equalization	2-tap FFE + 5-tap DFE	5-tap DFE	Adaptive FFE+DFE	4-taps FFE + 3 taps DFE	
Sampling Rate (GS/s)	12.5	10	8.5-11.5	10	
Resolution (bit)	4.5	4	6	6	
ENOB (bit)	N/A	N/A	4.86	4.74	
Input Range (V_{pp})	N/A	0.6	N/A	1	
Area (mm^2)	0.45	0.29	0.82	0.81	
Compensated Channel Loss	-24dB @ 12.5GS/s	-29dB @ 10GS/s	-34dB @ 10.3GS/s	-25.3dB @ 10GS/s	-36.4dB @ 10GS/s
ADC Power (mW)	150	93	195	79	
DSP Power (mW)	85	37	N/A	8	10
Power Efficiency (pJ/bit)	30.7*	13	19	8.7	8.9

* Includes both the TX+RX

(b)

Figure 1: 10Gb/s hybrid ADC-based receiver: (a) GP 65nm CMOS prototype, (b) performance summary.

An ADC-based statistical modeling methodology to analyze the BER impact of ADC metastability was developed [3]. In order to model metastability error propagation through a digital FFE, a partial-bit mapping approach is proposed that generates the error PDF at the FFE output. BER degradation due to metastability is evaluated with 10Gb/s NRZ signaling over a 32" backplane channel (Figure 2) and an RX that consists of a 6-bit ADC followed by a 3-tap digital FFE.



(a) (b)

Figure 2: Transient and statistical simulation BER bathtub curves with comparator τ=16.3ps for (a) flash, (b) aSAR.

Keywords: analog-to-digital converter, ADC-based receiver, embedded equalization, energy efficient

INDUSTRY INTERACTIONS

Freescale, Intel, Texas Instruments

MAJOR PAPERS/PATENTS

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[2] Shafik et al., "A 10Gb/s Hybrid ADC-Based RX with 3-Tap Analog FFE and Dynamically-Enabled Digital Equalization in 65nm CMOS," IEEE ISSCC, Feb. 2015.
[3] S. Cai et al., "Statistical Modeling of Metastability in ADC-Based Serial I/O Receivers," IEEE EPEPS, Oct. 2014.

TASK 1836.113, SYNTHESIZED CELL-BASED ADPLL IMPLEMENTATION FOR ACCELERATED DESIGN

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SIGNIFICANCE AND OBJECTIVES

This 3-year program focuses on developing "cell-based" all-digital PLLs that can be synthesized from a cell library, implemented using existing automatic place and route (APR) tools, and then digitally calibrated. The end result will be a set of PLL architectures described in HDL which can be adapted to a wide range of performance requirements.

TECHNICAL APPROACH

All-Digital Phase-locked loops (ADPLLs) are widely used as clock generators in advanced digital systems, eliminating several of the downsides of traditional PLLs. Previous work has demonstrated that integer-N ADPLLs can be implemented using digital synthesis and automatic place-and-route (APR) tools, resulting in a simplified and easily customizable design flow. Our next goal is the development of fractional-N frequency synthesizers which leverage novel architectural and implementation improvements. These new designs will be synthesizable using standard CAD tools, and will be prototyped in a series of test chips in advanced CMOS processes.

SUMMARY OF RESULTS

While previous investigations during this project have shown that it is possible to automate the physical design of a digitally controlled oscillator (DCO) using a cell-based methodology, this approach presents some challenges. Since cells are custom designed, it is desirable to be able to reuse cells as much as possible to hit different target specifications.

We have designed and fabricated a test chip containing synthesized oscillators in a number of configurations, in order to assess the effects of different variables on oscillation frequency, relative tuning range, and especially phase noise. Since modelled phase noise has been shown to not always be consistent in this type of oscillator, this test chip will allow us to extract general trends which will inform the design of future synthesized oscillators.

The chip contains 3 copies of a baseline 8-stage ring oscillator with switchable tristate buffers for tuning. Variations of the baseline circuit which will be tested include changing the number of oscillator stages, changing the number of tristate buffers inserted for tuning, and changing the number of parallel elements at each stage. Because each of these variations affects both the drive current and capacitance of the oscillator, the effect on phase noise may differ from expectations. Testing of this chip will be done in July 2015. Additionally, a methodology for quickly generating these sorts of test structures has been developed, allowing them to be quickly inserted into chips in future process technologies.

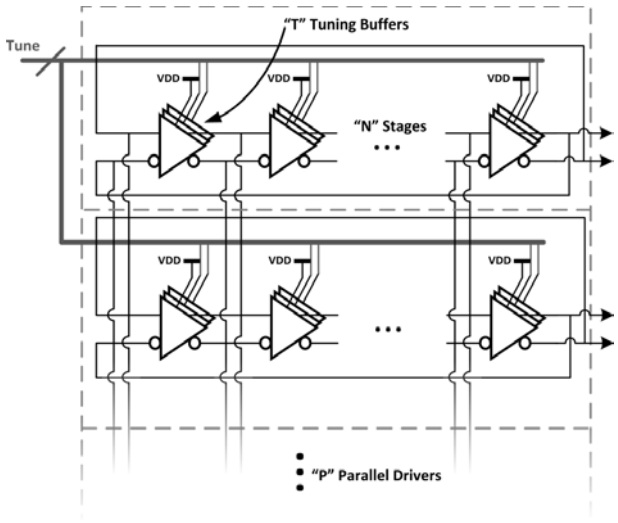

Figure 1: Oscillator schematic showing which variables are varied on the chip. N, T, and P represent swept variables.

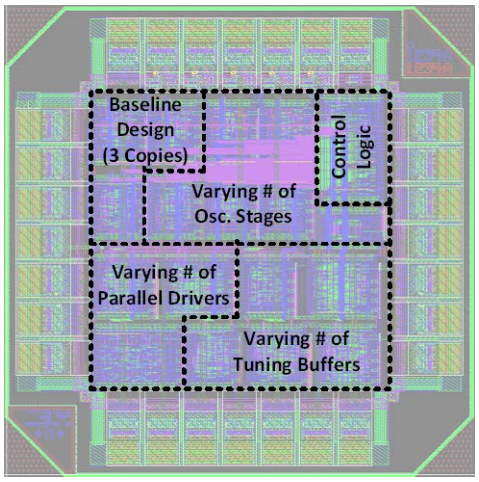

Figure 2: Floorplan showing the different variable blocks which make up the test chip.

Keywords: VLSA (Very Large Scale Analog), ADPLL, CMOS, frequency synthesizer, fractional-N

INDUSTRY INTERACTIONS

Texas Instruments, Intel, Freescale

TASK 1836.114, FREQUENCY SHAPEABLE MULTICHANNEL ADCS

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SIGNIFICANCE AND OBJECTIVES

We focus on the fundamental sampling limits of multichannel ADC sampling for cognitive radio and radar, when exploiting the signal structures in the frequency, time and spatial domains. We bridge between theory and practice by implementing prototypes of our proposed ADCs.

TECHNICAL APPROACH

Cognitive radio applications: In light of the ever-increasing demand for new spectral bands and the underutilization of those already allocated, the concept of Cognitive Radio (CR) has emerged. Opportunistic users could exploit temporarily vacant bands after detecting the absence of activity of their owners. One of the crucial tasks in the CR cycle is therefore spectrum sensing and detection which has to be precise and efficient. Yet, CRs typically deal with wideband signals whose Nyquist rates are very high. In this research, we consider spectrum sensing from sub-Nyquist samples and tackle several challenges posed by CRs such as robustness to noise, fading, and shadowing. We expand our approach to a network of CRs and consider joint spectrum sensing and direction of arrival estimation (DOA) as well.

Chip implementation: together with our collaborators at Stanford we have continued investigating various aspects of a chip design that can implement the developing algorithms achieving minimal sampling rate.

Sub-Nyquist radar: We consider sub-Nyquist sampling for pulse radar Doppler applications as well. We allow for a reduced time-on-target by transmitting non-uniformly spaced pulses and pave the way to sub-Nyquist cognitive radar by considering transmitted and received pulses with dynamic support composed of several narrow bands.

SUMMARY OF RESULTS

CR challenges spectrum sensing into dealing with very noisy wideband signals in an efficient and reliable way. Besides, sub-Nyquist sampling of such signals, which alleviates the burden both on the analog and the digital side, decreases the SNR. We therefore propose to exploit cyclostationary characteristics of communication signals to ensure better robustness to noise. Our cyclic spectrum reconstruction algorithm from sub-Nyquist samples is shown to outperform energy detection at low SNRs and is able to estimate very reliably the input transmissions carrier frequencies and bandwidths.

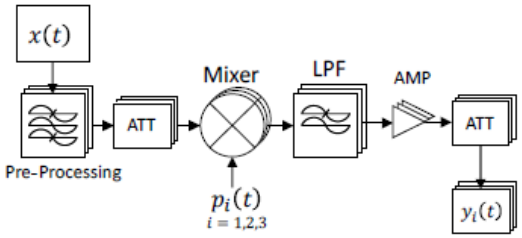

Figure 1: The analog design of one channel of the analog front-end of the Cognitive Radio system.

We then extend our sub-Nyquist sampling approach to a network of CRs, where several receivers collaborate to jointly sense the spectrum, overcoming their individual issues of fading and shadowing. We develop both a centralized and a distributed cooperation algorithm. Simulations show that our algorithms outperforms other approaches. Moreover, estimating the DOA of each detected transmission can be considerably beneficial to CR applications to exploit spatial as well as frequency sparsity. We derive a joint DOA and carrier frequency recovery of several transmissions as well as signal reconstruction from sub-Nyquist samples.

Last, we further exploit the structure of pulse Doppler radar signals to reduce the time-on-target and be able to detect targets in several directions during a single coherent processing interval. Moreover, to comply with cognitive radar requirements, we extend the sub-Nyquist pulse Doppler radar to allow for transmission and reception of several narrow frequency bands whose support vary with time. Such a system allows us to disguise the transmitted signal or cope with overloaded spectrum by using a smaller portion of it.

Keywords: ADCs, sub-Nyquist sampling, cognitive radio, spectrum sensing, radar

INDUSTRY INTERACTIONS

Texas Instruments, Intel, AMD

MAJOR PAPERS/PATENTS

[1] D. Cohen and Y. C. Eldar, ”Cyclic Spectrum Reconstruction from Sub-Nyquist Samples”, IEEE Globecom, Dec. 2014.

[2] D. Cohen, Y. C. Eldar, G. Leus, "Universal Lower Bounds on Sampling Rates for Covariance Estimation", IEEE ICASSP, Apr. 2015.

TASK 1836.117, PERFORMANCE AND RELIABILITY ENHANCEMENT OF EMBEDDED ADCS WITH VALUE-ADDED BIST

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SIGNIFICANCE AND OBJECTIVES

The objectives are to develop procedures for implementing parametric BIST of ADCs with minimal area overhead, to use on-chip test results to enhance performance by digitally calibrating the ADC, and to experimentally demonstrate the BIST and BIST-based calibration on the ADC12 internal to the TI MSP 430 microcontroller.

TECHNICAL APPROACH

Working with engineers at TI, the Functionally Related Excitation (FRE) approach to testing using a Stimulus Error Identification and Removal (SEIR) algorithm will be adapted to a BIST solution. The FRE/SEIR approach was developed in conjunction with TI on a previous SRC project. On-chip FRE signal generators using the shift operator will be developed for test signal generation and existing on-chip computation resources will be utilized to minimize the area overhead required to implement the SEIR algorithm. Target area overhead is at most 10% of the area of the existing uncalibrated ADC that is currently in high-volume production.

SUMMARY OF RESULTS

A block diagram showing the BIST capability and the BIST-based calibration is shown in Fig. 1 with a target 12-bit ADC. Two additional bits of resolution have been added to the SAR ADC to allow for a 2-bit improvement in linearity with the BIST-based calibration. The final output is then decimated back to 12 bits after calibration.

The signal generator will be a current ramp based integrator comprised of the output from a simple regulated cascode current source charging a nonlinear capacitor. With the FRE/SEIR approach, linearity of the ramp is of little concern. To manage the size of the integration capacitor, a series of faster-rising ramps will be used instead of a single ramp. A second-generation level-spreading ramp generator using a dithered integration starting voltage was developed to maintain approximately uniform density of the input signal throughout the input range of the ADC. A critical component is the shift generator which must have a constant shift. The second-generation shift generator of Fig. 2 that provides rail-to-rail output using correlated level shifting (CLS) and that provides the constancy needed for testing 14-bit ADCs has been designed.

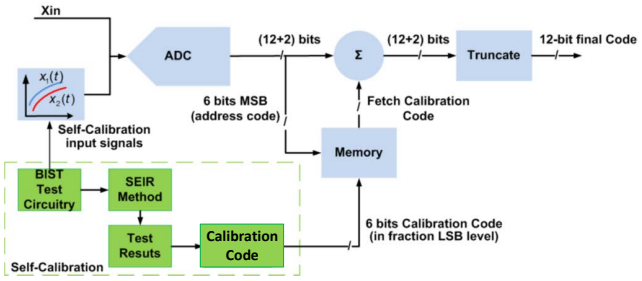

Figure 1: Block Diagram of ADC with BIST-Based Calibration and Value-Added BIST

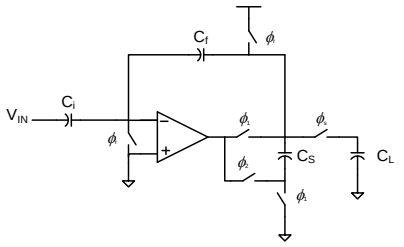

Figure 2: FRE shift generator using correlated level shifting for rail-to-rail outputs

Keywords: ADC BIST, self-calibration, analog testing, FRE signal generators, SEIR testing, shift-generators

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

In this custom-funding project, details about the ADC used for experimental verification are proprietary property of TI thus precluding publication of key technical details of the project. Two publications that discuss principles used in this research follow.

[1] X. Zhang et. al., "A Calibration Technique for SAR Analog-to-Digital Converter Based on INL Testing with Quantization Bits and Redundant Bit," 2015 IEEE Int. Symp.on Circuits and Systems (ISCAS), pp. 3024-3027, May, 2015.

[2] H. Meng et al., "A Simple Ramp Generator with Level Spreading for SEIR based ADC BIST Circuit," IEEE Midwest Symp. On Circuits and Systems (MWSCAS), pp. 53-56, Aug., 2015.

TASK 1836.125, 10GS+/S RESOLUTION-SCALABLE (4-7BITS) ADCS

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SIGNIFICANCE AND OBJECTIVES

This research will develop and demonstrate new techniques that enable energy efficient, high speed, moderate resolution analog-to-digital conversions. High sampling rate will be achieved without using time-interleaving, thus no calibration is needed and making the system design easier. This energy efficient ADC with very fast operation speed will facilitate and improve communication applications.

TECHNICAL APPROACH

The new scheme exploits the delay of on-chip transmission lines to implement a pipeline and thereby avoid the use of power hungry sample-and-hold or MDAC stages. Because this scheme is intended for moderate resolution, the stages do no need to provide gain; instead the comparators zoom into the signal value. Although, the delay between stages is independent of the sampling rate, the delay does need to be long enough so that the stage n decision is resolved in time to set up the comparator reference voltage of stage n+1. We relax this critical decision path in the pipeline by using two comparators in all stages after the first.

SUMMARY OF RESULTS

As shown in Figure 1, the input signal and the clock signal propagate down a matched pair of transmission lines. The delay of the transmission line allows time for a stage decision to be made at stage (n) before the signal and clock edge reach the next stage (n+1).

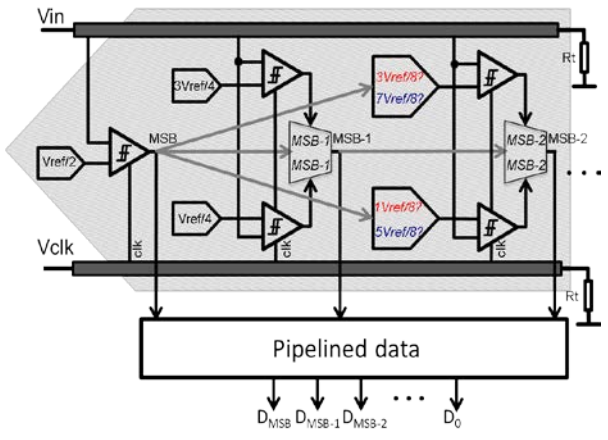

Figure 1: ADC top level block diagram

The two high speed comparators of stage (n+1) are setup with two pre-computed reference values corresponding to both possible decisions of stage (n). When stage (n) makes a decision, we select which of the two comparator outputs of stage (n+1) is appropriate. This allows the reference voltages for the comparators in stage (n+1) to be configured before a decision is made by stage (n). The DAC in each stage is calibrated according to the attenuation on the transmission line.

One design challenge is the physical realization of the slow-wave characteristic transmission lines; the other is the achievement of high speed, low power active circuits. In the first prototype ADC, we added equally-spaced floating metal strips underneath the transmission line, thus artificially increasing the effective dielectric constant of the transmission line. However, since both clock signal and input signal are differential, the physical size of the lines has to be optimized so that the chip is area efficient. Meanwhile, the differential transmission line structure (Figure 2) will handle the electromagnetic coupling between lines much better. At 5GHz (Nyquist frequency) the attenuation of the delay cell is less than 0.5dB. At 10GHz (sampling rate) the attenuation is around 1.6dB for one delay cell. This alleviates the design challenge of the clock buffer that generates full swing CMOS clock. In addition, the new prototype ADC employs 1-bit redundancy that corrects errors from the first two stages. The spectrum plot of fundamental and harmonic tones after FFT is as shown (Figure 2).

Tapeout of the 40-nm prototype is planned for October 2015. The layout is almost completed.

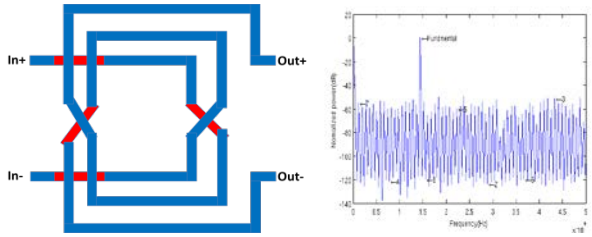

Figure 2: Differential inductor (left) and Spectrum plot (right)

Keywords: on-chip low-dispersion transmission-line, travelling wave, no time-interleaving, very-high-speed ADC, energy-efficient

INDUSTRY INTERACTIONS

Texas Instruments, IBM, Freescale

TASK 1836.127, PRECISION TEST WITHOUT PRECISION INSTRUMENTS

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RANDY GEIGER, IOWA STATE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

Accurate spectral analysis is widely needed in IC characterization and final test. Ideal IEEE standard test requires accurate instruments and accurate test control, resulting in expensive equipment, complex test setup, demanding maintenance, TTM delays, and high test cost. The objective of this research is to develop new spectral test algorithms to remove IEEE standard requirements, deliver accurate full spectrum test results, and greatly reduce test equipment cost, TTM delays, and test time.

TECHNICAL APPROACH

The task of accurate spectral testing is re-examined as a weakly nonlinear signal and system identification problem. Techniques from statistical signal processing are carefully incorporated to ensure that the new test algorithms effectively extract all useful information available in the collected data and that the achieved test accuracy levels are near the theoretical limits. An innovative iterative time-frequency domain processing technique is utilized to achieve the best accuracy and time efficiency trade-off, in which accurate sine wave identification is done in the frequency domain but identified component removal is done in the time domain. This ID and correction technique also enables us to directly work with the small signal components coming from various sources of distortion under test.

SUMMARY OF RESULTS

The final goal of the project is to be able to eliminate all the stringent requirements in the ideal IEEE standard spectral testing. These requirements include: perfectly coherent sampling, accurate amplitude control, high purity sine wave stimulus, and jitter-free sampling clock signal. During the first year, we have published two IEEE Transactions papers, one ITC paper and one VTS paper, introduced FIRE method for removing non-coherency, the FERARI method for both non-coherency and amplitude clipping, and an efficient jitter and noise separation method for accurate SNR testing.

During the second year, we published two journal papers and 7 conference papers. The following results are presented in these publications: a comparative study of state of the art methods for dealing with non-coherent sampling and how each method should be applied; an algorithm for simultaneously dealing with non-coherent sampling and amplitude clipping; an algorithm for simultaneously dealing nonlinear sine source and non-coherent sampling; an algorithms for simultaneous AC and DC test with dramatic test time reduction; an algorithm for accurate SNR test in the presence of clock jitter, a method for clock jitter separation and characterization; and a method for generating ultra-pure sine wave signals for high resolution ADC testing.

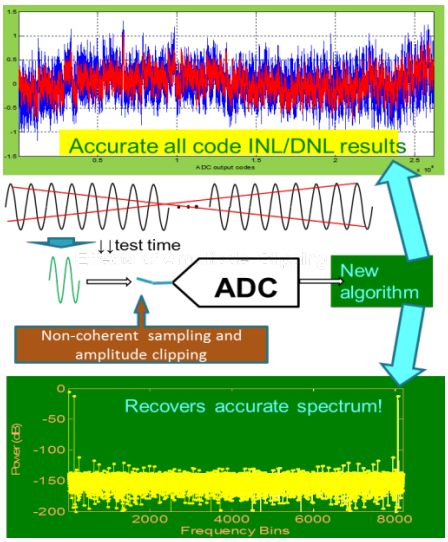

Figure 1: The ITC 2014 test method allows the use of a short data set with non-coherent sampling and amplitude clipping to achieve accurate all code INL/DNL test and accurate full spectrum test.

Keywords: AC test, spectral test, non-coherent sampling, amplitude clipping, jitter, noise, pure sine wave

INDUSTRY INTERACTIONS

Texas Instruments, Freescale

MAJOR PAPERS/PATENTS

[1] Sudani, Xu, Chen, IEEE D&T 2015.
[2] Xu, Sudani, Chen, IEEE TIM 2014.
[3] Xu, Chen, ITC 2014.
[4] Xu, Duan, Chen, VTS 2015.
[5] Xu, Chen, ISCAS 2015.
[6] Duan, et al, ISCAS 2015.
[7] Xu, Chen, ISCAS 2015.
[8] Zhuang, et al, MWSCAS 2015.
[9] Zhuang, Chen, TECHCON 2015.

TASK 1836.128, STATISTICAL ANALOG DESIGN PROPERTY CHECKING

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SIGNIFICANCE AND OBJECTIVES

Statistical learning based methods are very appealing for analog verification and failure diagnosis as they tend to scale well for large analog and mixed-signal designs. However, to be truly efficient, it is highly desirable to develop efficient learning techniques for design property checking and failure rule extraction with limited data.

TECHNICAL APPROACH

Machine learning is promising for addressing analog design and verification challenges. We develop a novel active learning guided approach, based on support vector machine (SVM) for characterizing circuit performance with significant reduction on the amount of data needed. In a related direction, diagnosing out-of-specification failures in mixed-signal circuits has become increasingly challenging due to: (1) failures caused by interactions between input-signal conditions and design uncertainties, and (2) the need to identify critical input and uncertainty conditions that cause these regions. We propose a simulation-driven approach that uses ensemble learning to extract if – then rules that naturally solve both problems.

SUMMARY OF RESULTS

Under our SVM framework as shown in Fig. 1, to select the optimal query simulation instance at a time, we rank the candidate simulation instances according to a probabilistically weighted goodness metric that is computed by rigorously evaluating potential reduction of version space if the instance were queried. As such, our active learning scheme intelligently selects query instances which are expected to act as support vectors throughout the iterative classifier training process, hence avoids committing wasteful queries and significantly reduces the required training data and the overall training cost. Our experimental studies have shown that the proposed active learning technique is able to dramatically reduce the size of the training data, leading to significant reduction of the overall training cost by up to one order of magnitude [3].

We leverage the approximate property checking technique developed in [2] to enable extraction of failure rules. By ranking, pruning and clustering these rules, we then construct a compact set of failure rules which can be directly employed for pre-silicon debug, as demonstrated on a phase-locked loop circuit illustrated in Fig. 2 [1]. Furthermore, these regions can be used to guide test pattern generation and/or assist with post-silicon debug.

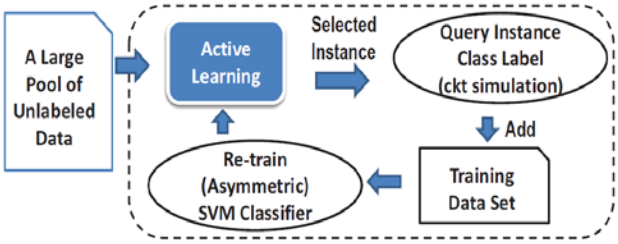
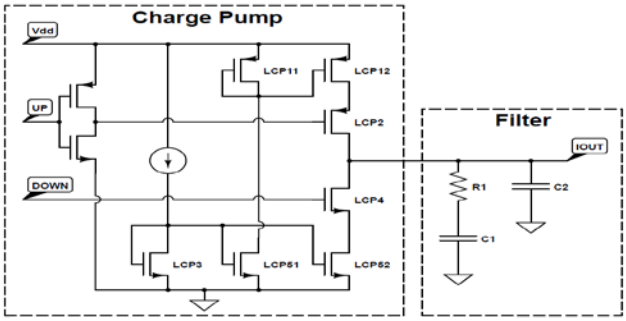


Figure 1: Active-learning guided support vector machine (SVM) based analog performance modeling and property checking.



1. $LCP3 \leq A$ where A is the nominal value.
2. $C2 \leq B$ where B is the nominal value.
3. $LCP3 \leq C \,\&\, LCPx > D$ where $x \in \{2, 5\}$.
4. $LCP11 \leq E \,\&\, LCP12 > F$.

Figure 2: Identified dominant failure rules for a charge-pump PLL.

Keywords: Statistical learning, analog verification, analog failure analysis, active learning, support vector machine, ensemble learning.

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] Mukherjee et al., "Leveraging pre-silicon data to diagnose out-of-specification failures in mixed-signal circuits," IEEE/ACM DAC, 2014.

[2] Mukherjee et al., "Approximate property checking of mixed-signal circuits," IEEE/ACM DAC, 2014.

[3] Lin et al., "Circuit Performance classification with active learning guided sampling for support vector machines," accepted to IEEE Trans. CAD, 2015.

[4] Lin et al., "Parallel hierarchical reachability analysis for analog verification," IEEE/ACM DAC, 2014.

TASK 1836.129, STUDY OF BURST-MODE DATA RECOVERY FOR HIGH LOSS CHANNELS

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SIGNIFICANCE AND OBJECTIVES

Proposed research sets out to explore burst mode data recovery techniques applicable to receivers used in I/O links operating over high loss channels. These techniques can be used in conjunction with fast on-off circuit techniques to realize I/O link architectures with "energy-proportional" behavior. Use of highly digital techniques and applicability to a wide variety of receiver equalization architectures is also emphasized.

TECHNICAL APPROACH

The technical approach exploits the slow-varying nature of the channel characteristic of typical PCB channels. By estimating its pulse response, it is possible to compute the channel output for a known data sequence. By storing the estimated response and transmitting a known bit sequence at the beginning of the burst-mode data transfer operation fast phase locking can be achieved.

SUMMARY OF RESULTS

Receivers operating over high loss channels commonly employ discrete time equalization techniques such as decision feedback equalization (DFE) and feed-forward equalization (FFE). The equalization coefficients for DFE and FFE are typically adapted using a variant of least mean squares (LMS) adaptation algorithm. The equalizer coefficients generated by LMS adaptation can be utilized to estimate the pulse response at the sampling instant. Furthermore, digital interpolation can be used to estimate the pulse response at the intermediate time instants (Fig. 1).

This estimated pulse response can be utilized to compute the response of the channel for a known bit-sequence (Fig. 2). This sequence can be used as preamble for burst mode data to do fast phase locking.

Keywords: fast turn-on, digital voltage regulator, rapid on-off biasing

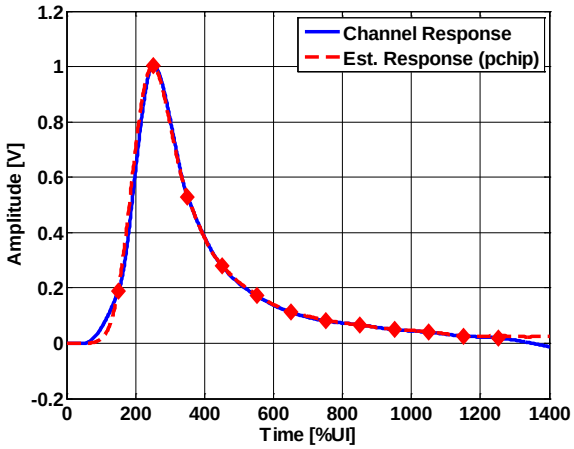

Figure 1: Estimated pulse response using LMS adaptation coefficients and interpolation.

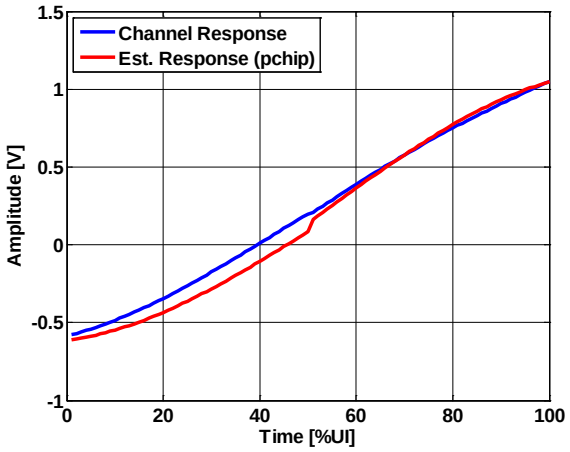

Figure 2: Estimated 0-to-1 transition edge for 0011 bit pattern passed through channel having a pulse response as shown in Fig.1.

INDUSTRY INTERACTIONS

Texas Instruments, Intel, AMD

MAJOR PAPERS/PATENTS

TASK 1836.132, FAULT-COVERAGE ANALYSIS OF ANALOG/MIXED-SIGNAL TESTS BASED ON STATISTICAL DISSIMILIARITY

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SIGNIFICANCE AND OBJECTIVES

The number of mixed-signal ICs escaping production screening is sharply rising due to the increasing use of digital circuits within analog systems. This task aims to develop a systematic way to quantitatively measure the fault coverage of a given analog/mixed-signal circuit test. This is a key pre-requisite to the automatic generation of efficient analog/mixed-signal test suites or patterns that can achieve high defect coverage and short testing time.

TECHNICAL APPROACH

This task will explore ways of quantitatively measuring the fault coverage of an analog/mixed-signal test suite leveraging various statistical discrimination methods.

For instance, a test is said to cover a fault when the fault causes large enough difference in the test's response that can be distinguished from the normal statistical variations of the circuit due to global process, voltage, and temperature (PVT) variations and local transistor-to-transistor mismatches.

In addition, the correlations among the test responses can be utilized in various ways, for instance, to enhance the effective coverage of a given test suite and to estimate the statistical distributions with a small number of Monte-Carlo samples.

SUMMARY OF RESULTS

An initial study has been conducted that quantifies the test coverage of some representative analog/mixed-signal circuits over basic catastrophic stuck-short/open faults. Despite the simplistic assumptions made, the results demonstrate that the fault coverage analysis based on statistical discrimination can be an effective way to measure the fault coverage of a given test suite and guide the composition of an efficient test suite. For instance, the analysis shows that all the stuck-open/short faults in an 8-bit digitally-controlled phase interpolator can be covered with only 5 different delay measurement tests. The analysis can also identify redundant components in the circuit.

This year, an incremental, min-max search algorithm is devised to find a minimal set of tests that achieves the desired algorithm. This algorithm accounts for the cross-correlation among the tests and is more efficient than an exhaustive, combinatorial search algorithm.

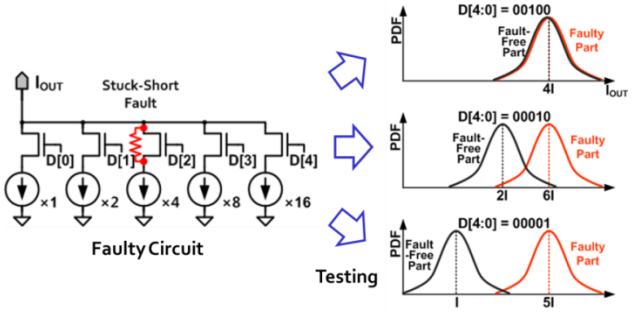

Figure 1: Determining fault coverage based on variability distribution.

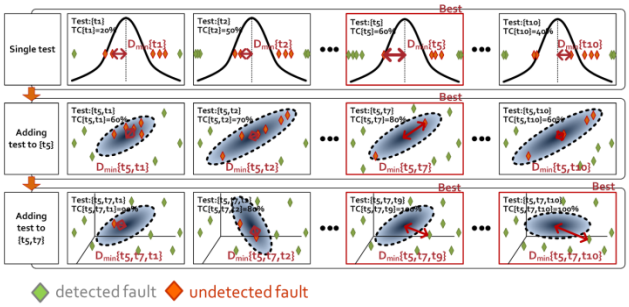

Figure 2: Efficient test compaction algorithm that finds the minimal set of tests with the desired coverage.

Keywords: analog/mixed-signal circuits, production tests, fault coverage analysis, test compaction, automatic test pattern generation.

INDUSTRY INTERACTIONS

Texas Instruments, Intel, and GlobalFoundries.

MAJOR PAPERS/PATENTS

[1] S. Youn, C. Gu, and J. Kim, "Probabilistic Bug Localization for Analog/Mixed-Signal Circuits using Probabilistic Graphical Models," Design Automation Conf. (DAC), June 2014.

[2] S. Jung, J. Lee, and J. Kim, "Variability-Aware, Discrete Optimization for Analog Circuits," Trans. on Computer-Aided Design, 2014.

[3] S. Jung, J. Lee, and J. Kim, "Yield-Aware Pareto-Front Extraction for Discrete, Hierarchical Optimization of Analog Circuits," Trans. on Computer-Aided Design, 2014.

[4] J. Kim, et al., "Discretization and Discrimination Methods for Design, Verification, and Testing of Analog/Mixed-Signal Circuits," Custom Integrated Circuits Conf., 2013.

TASK 1836.134, HYBRID TWO-STEP PLLS FOR DIGITAL SOCS IN NANOSCALE CMOS

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SIGNIFICANCE AND OBJECTIVES

Phase-locked Loops (PLLs) are an integral part of today's electronic communication and computation systems. Their performance and optimization is critical to overall system performance. The objective of this project is to study the replacement of LC VCOs (voltage-controlled oscillators) with bulky on-chip inductors with compact ring oscillators, while still preserving the overall PLL performance. This calls for development of a hybrid two-step PLL.

TECHNICAL APPROACH

The overall frequency conversion is divided into two cascaded stages. The first stage is an ultra-low noise wide-band PLL which generates a high quality, high frequency reference for the second stage. A novel hybrid phase-frequency detector is proposed to achieve this low noise, high ratio reference frequency multiplication. The wide loop bandwidth allows the usage of compact ring oscillators. The second stage, a fractional-N PLL, provides the required fine resolution. Due to the low-ratio multiplication, it has much reduced noise impact. Also a novel fractional-N quantization noise suppression mechanism is proposed using an auxiliary sub-sampling phase detector.

SUMMARY OF RESULTS

The usage of large bandwidth (>3MHz) in the PLLs reduces the noise impact of the VCOs. This enables the usage of ring oscillators in spite of their poorer phase noise performance, in comparison with LC oscillators. The large BW also helps in shrinking the loop filter area, further reducing the area of the PLL. The VCO noise of the first stage can further be reduced by introducing a frequency divider (M) as shown in Fig.1. Increasing N_1 and M in tandem while keeping N_1/M constant decreases the first stage VCO noise contribution. Thus N_1 = 80 and M = 8 are chosen. For a given output frequency, $N_1.N_2/M$ is fixed. Therefore, keeping $N_1.N_2/M$ constant while increasing N_1/M and reducing N_2, reduces the in-band contribution of the second PLL. The minimum value of N_2 is chosen to be 20. A further reduction in N_2 is limited by the quantization error of the second stage. The PLL reference is at 50 MHz and output is tunable from 7.5-10 GHz. The phase noise plot obtained using verilog-A simulations is shown in Fig.1. The output of the PLL is filtered by a 3 MHz high pass filter (HDMI specification). The resulting output has a simulated total jitter of 0.97 ps_{RMS}.

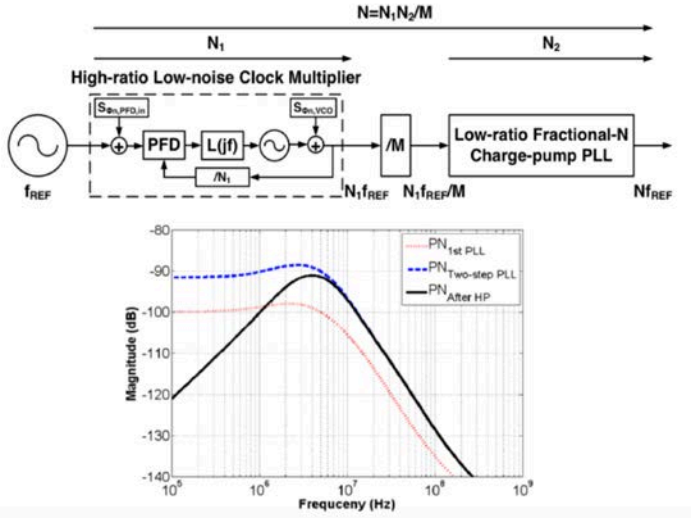

Figure 1: The block diagram of the proposed two step PLL and simulated phase noise plot.

Keywords: PLLs, sub-sampling, phase detectors, ring oscillators, two-step PLL.

INDUSTRY INTERACTIONS

Intel Corporation, Texas Instruments, GlobalFoundries

TASK 1836.136, INJECTION-LOCKED RING OSCILLATORS FOR CLOCK DISTRIBUTION IN MANYCORE PROCESSORS

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SIGNIFICANCE AND OBJECTIVES

Technology scaling has enabled integration of many independent processing elements on a single die or in a same module. Energy-efficient circuit design for synchronization of manycore processors, based on both traditional techniques and injection-locked ring oscillators is the objective of this work.

TECHNICAL APPROACH

We are developing a low-overhead global clock distribution scheme for manycore processors and heterogeneous SoCs based on ring oscillators and injection-locked ring oscillators (ILROs). A hard-coupled ILRO can multiply its output frequency, reducing the power overhead of the global clock distribution network. In other words, by routing a low frequency global clock and then multiplying up to obtain the core clock, we can minimize overall power consumption.

SUMMARY OF RESULTS

We have developed a baseline design for clock generation in manycore processors, based a delay-locked loop (DLL) and a phase-picking clock generator, Fig 1. A ~2GHz reference clock is distributed to DLLs, which generate 16 uniformly-distributed clock phases. Phase-picking clock generator picks the appropriate phase for each clock cycle, based on an information from the timing replica path.

The design, implemented in 28nm ultra-thin body and BOX fully-depleted silicon-on-insulator (UTBB FDSOI) technology is fully functional and occupies 32µm x 30µm, Fig. 1. Generated clock frequency is in the range 550-2260MHz at 1V and 100-625MHz at 0.5V.

While this design's size and power are appropriate for a medium-sized core, the overhead of distributing a high-frequency clock to a very small core, or for a system with many cores may be high. Our on-going research targets three areas: (1) very compact ring-oscillator based PLLs for clock generation, (2) ILRO-based local clock generation, as shown in Figure 2, and (3) synchronization between clock domains.

To generate local clocks within processing cores integer-N clock multiplication scheme will be used, followed by rotating phase picking/interpolation.

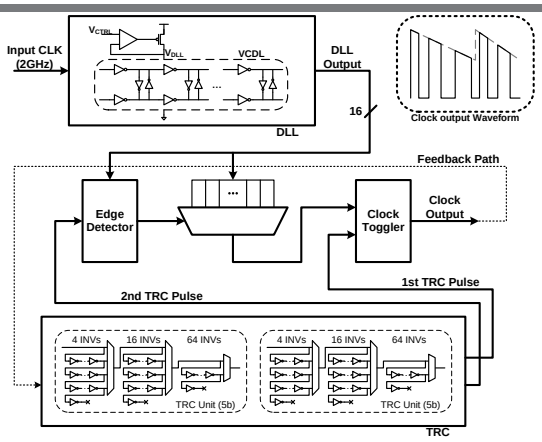

Figure 1: DLL-based clock generation.

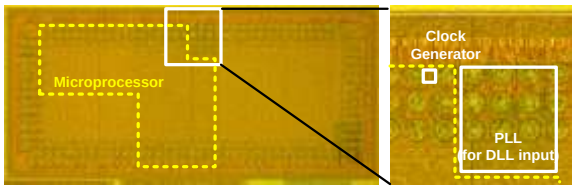

Figure 2: Chip photo.

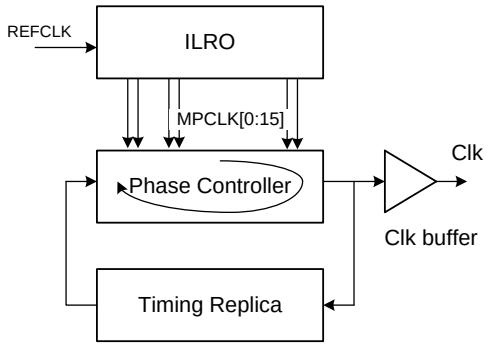

Figure 3: Injection-locked ring-oscillator clock generator.

The concept of local clock generation is based on a local controller that is picking the right phase for the core, based on timing replica circuits, illustrated in Figure 2. In the example design, the controller can chose to pick any of the 16 clock phases, thus adjusting the clock in a wide range. If finer resolution of the clock is needed, interpolation between the phases can be used.

Keywords: CMOS, clock, manycore, DLL, PLL.

INDUSTRY INTERACTIONS

Intel, AMD, Freescale, GlobalFoundries

TASK 1836.137, 50GS/S AND BEYOND FREQUENCY-INTERLEAVED ENERGY-EFFICIENT ADCS

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SIGNIFICANCE AND OBJECTIVES

This research explores a novel ADC technique referred to as frequency-interleaved analog-to-digital conversion (FI-ADC) for improving the performance of very high-speed ADCs. Performance of conventional high-speed ADCs is ultimately limited by jitter and we aim to determine if and how the FI-ADC can mitigate the jitter sensitivity of high-speed ADCs.

TECHNICAL APPROACH

One of the key focuses of this work was to develop a comprehensive model for comparing the FI-ADC to the time-interleaved ADC (TI-ADC). A quantitative analysis was performed in addition to system-level simulations that compare the two architectures. The simulations support the theoretical findings and additionally provide further insight into the conditions under which the FI-ADC outperforms the TI-ADC. The second focus of this research was the development of a fully integrated FI-ADC system with 25GHz of bandwidth (50 GS/s) and 6b of resolution. For the first phase, a 25 GHz channelizing front-end was taped out. The front-end performs channelization, downconversion, filtering and LO generation/distribution. The next phase will focus on optimization of front-end power consumption and sub-ADC integration.

SUMMARY OF RESULTS

One of the key results from this work is the detailed analysis of the impact of jitter and phase noise on the FI-ADC. Previous works have commented on the reduced jitter sensitivity of the FI-ADC due to the reduced bandwidths presented to the sampling network, but have failed to provide an analysis of the impact of phase noise introduced during the downconversion which occurs in each passband channel. Quantitative analysis shows that the phase noise of the LOs used for downconversion plays a critical role in determining if the FI-ADC outperforms the TI-ADC. In general, the FI-ADC has great potential to improve performance for high input frequencies but may sacrifice performance at lower frequencies depending on the implemented architecture.

Figure 1 shows a comparison of the SNR vs. input frequency for the two architectures. For our design, the FI-ADC outperforms the TI-ADC, improving the SNR at Nyquist by 15dB. In the general case, this improvement is closer to 10dB. The further im

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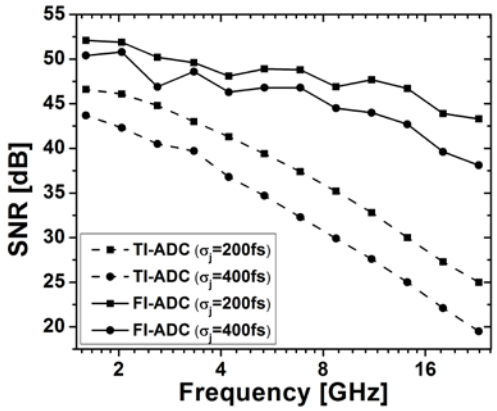

Figure 1: System-level simulations of the FI-ADC and TI-ADC.

architecture is due to the inherent filtering in the tuned LO buffers. This filtering is not performed on the sampling clock.

A wideband FI-ADC analog front end (AFE) was taped out in a 65nm CMOS process. The AFE is responsible for channelizing and downconverting the wideband signal before presenting it to the baseband sub-ADCs assigned to each channel. In addition, the AFE must generate the multiple LO signals needed for mixing. By utilizing a front-end distributed amplifier and high-frequency harmonic rejection mixers, the AFE is capable of distributing and channelizing a 25 GHz signal with sufficient SNR and linearity for a 5-6b system. The AFE achieves an IIP_3 of +5dBm and peak output SNDR of 34 dB for a 25 GHz input signal, which equates to 5.3b ENOB.

The current FI-ADC AFE utilizes power hungry circuits for LO generation/distribution. Alternative approaches, such as using class D switching amplifiers for LO buffers, will be investigated. This is part of a more general study of the relation between power consumption of LO buffers/distribution and the impact on mixer performance.

In general, future work will focus on continuing wideband channel measurements, reducing AFE power consumption, and sub-ADC integration.

Keywords: high-speed ADC, frequency-interleaved, channelized front-end, wideband receiver

INDUSTRY INTERACTIONS

Texas Instruments, Intel

TASK 1836.141, IC DESIGN FOR RESILIENCE AGAINST SYSTEM-LEVEL ESD

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SIGNIFICANCE AND OBJECTIVES

System-level ESD reliability is uncorrelated with component-level ESD reliability yet IC designers are asked to build-in system-level ESD resilience. This project's objective is to develop integrated circuit designs that are resilient to power-on ESD and a behavioral model of the IC that can be used for system ESD design.

TECHNICAL APPROACH

ESD testing of a prototype system containing a custom test chip is used to ascertain the causes of ESD-induced soft failures. The effect of reverse body bias on latchup susceptibility during system-level ESD is studied using measurements and circuit-level simulation. Latchup rules for the body bias nets will be developed. The relation between ESD rail clamp design variables and PDN stability is analyzed. A methodology is being developed to construct a behavioral model of the pin-level response to system-level ESD using measurement data but no proprietary information about the circuit design.

SUMMARY OF RESULTS

With the aid of a custom CMOS test chip, a variety of ESD-induced soft failures were observed. Glitches at input pins result from bounce of the on-chip power supply relative to the board-level supply. The two power supplies are decoupled by the bond-wire impedance. This result suggests that on-chip filtering of the input signal will not be effective for eliminating glitches. A new test chip that will facilitate evaluation of that hypothesis is currently being fabricated.

Bit flips in an on-chip shift register were observed following system-level ESD. Measurements suggest that some of these errors are due to glitches at input pins, while the rest are due to noise generated on chip. The new test chip will provide additional information about the upset susceptibility of registers based on the location and design style.

In principle, high impedance circuit nodes are vulnerable to upset by minority carrier substrate current. Logic errors at high impedance circuit nodes were not observed during IEC 61000-4-2 system-level ESD testing but were observed during ISO 10605 testing. The latter is a longer duration electrostatic discharge.

In chips with multiple power supply domains, ground bounce can cause the polarity of a supply domain to reverse, with latch-up resulting after recovery. This phenomenon was observed in both simulation and measurement. Ground bounce is a consequence of the bond-wire inductance and thus this finding is expected to be package-dependent.

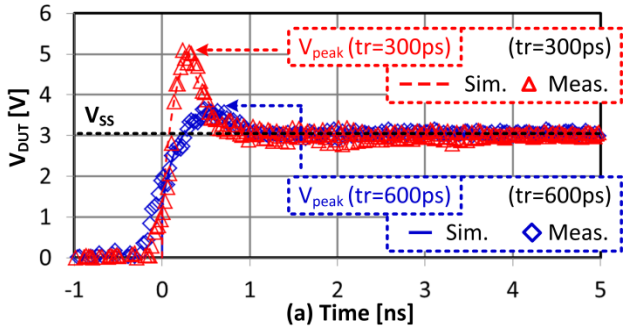

Figure 1: ESD diodes subjected to fast current pulses show transient voltage overshoot due to delayed conductivity modulation of the ohmic regions. A PWL-TR model accurately represents the transient response of this ESD device, as well as larger ESD protection circuits.

Mobile equipment (i.e., a battery operated system) was found to be immune to ESD-induced hard failures but hard failures are observed in "tethered" equipment that is not protected by transient voltage suppressor devices. The Industry Council on ESD Target Levels has proposed using circuit-level modeling and simulation to design for robustness against hard failures. This requires behavioral models of ICs. The PWL-TR (piecewise linear with transient relaxation) method was developed for accurate behavioral modeling of an IC's I-V and transient responses to ESD (Fig. 1). The motivation was to provide a method for "black box" modeling of the transient response of non-linear ESD protection devices. However, board-level measurements indicate that the observable transient response may be limited by the package parasitics, which are linear elements.

The system-level ESD test bed provides the current return path and this must be included in the ESD circuit simulation. A distributed model of the test bed was developed.

A 65nm test chip is currently being fabricated; it will be used for further study of soft failures at input circuits and in registers. This test chip contains a variety of ESD noise detectors. An additional test chip is being designed for a latchup study.

Keywords: ESD, latch-up, soft failures, modeling

INDUSTRY INTERACTIONS

Freescale, GlobalFoundries, Texas Instruments

TASK 1836.145, RF AND MIXED SIGNAL QUANTUM CMOS DEVICES AND CIRCUITS

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SIGNIFICANCE AND OBJECTIVES

This project pioneers a path towards explicit quantum mechanical operation in industrial CMOS by demonstrating a new class of quantum MOS devices and circuits. This work will develop understanding of quantum MOS device physics and incorporation of such devices into RF and mixed-signal circuits operating at or near room temperature.

TECHNICAL APPROACH

This project introduces quantum well (QW) NMOS transistors showing quantum transport characteristics in the form of negative differential transconductances (NDTCs). A main focus is to understand how to make QW NMOS devices useful in circuits designed to exploit the NDTCs. An important goal is to develop a QW NMOS device model adaptable into SPICE and Verilog circuit models. Complete NDTC characteristics have been measured on a set of QW NMOS transistors fabricated by Texas Instruments on a 45-nm CMOS process. This data have been imported into a look-up table, and some oscillator and folding amplifier circuits are being designed and simulated based on the measured NDTC characteristics.

SUMMARY OF RESULTS

Over the first full year of this project we have completed detailed transfer characteristic measurements of a set of QW NMOS devices fabricated by TI in a 45-nm CMOS technology. Of particular importance is the discovery of some devices and bias conditions that show clear negative differential transconductance (NDTC) characteristics up to room temperature (300 K), a shown in Fig. 1, whereas 230 K was previously the highest temperature at which NDTC was observed. The ability to generate NDTCs at room temperature is a critical milestone towards the acceptance of QW devices and circuits into mainstream technology.

We also completed a study of the gate length and temperature dependencies of the NDTC phenomena. Gate length dependence shows a correlation of the channel length with the number of NDTCs as well as with the gate voltage (V_G) spacing between NDTCs. The V_G spacing between multiple NDTCs suggests a parabolic QW potential profile. The temperature dependence is consistent with partial freeze-out of carriers against a degenerately doped background. These results have furthered understanding of the quantum device physics.

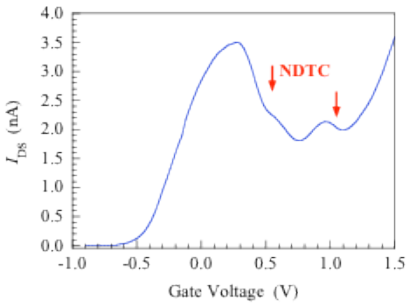

Figure 1: Drain-source current vs. gate voltage for a 40 nm QW NMOS transistor at room temperature. Red arrows indicate regions of NDTC.

Finally, the empirical data have been structured into a device look-up table usable in SPICE and Verilog circuit simulations. From this, simple circuits, such as a fundamental oscillator, a folding amplifier ADC input, and a three level oscillator (see Fig. 2) have been designed and simulated to take explicit advantage of the NDTC in a QW NMOS.

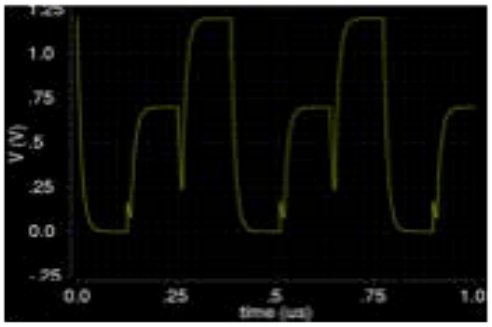

Figure 2: Verilog simulation of a 3 state oscillator circuit using the NDTC characteristics of QW NMOS transistors.

Keywords: quantum devices, quantum circuits, negative differential conductance, quantum well, quantum CMOS

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

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TASK 1836.148, 50GSPS+ TI HYBRID SAR ADC ARRAY WITH COMPREHENSIVE DDI CALIBRATION

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SIGNIFICANCE AND OBJECTIVES

Time-interleaving is an effective way to increase analog-to-digital conversion speed. Path mismatches, especially dynamic mismatch (skew, bandwidth mismatches), tend to limit the linearity of the array. This work introduces a technique using simple passive components to extract the input derivative information to calibrate the dynamic path mismatches in TI-ADC arrays.

TECHNICAL APPROACH

Passive high-pass filters (HPF) are used to obtain various input derivatives which are then quantized into 1-bit digital forms. This direct derivative information (DDI) is correlated with the error signal which is the difference between the outputs of each sub-ADC in a TI-ADC array and a reference ADC to extract the dynamic mismatch profiles. The learned results are fed back to the analog domain to correct the errors at its origin.

SUMMARY OF RESULTS

TI-ADC arrays with both dynamic and static path mismatches are modeled in MATLAB. Both single-tone and multi-tone inputs are used to train the calibration apparatus. Similar results have been obtained in both cases.

A 32-GS/s 6-bit TI-ADC is currently under development. Preliminary simulation results show over a 30-dB SNDR with a power consumption of less than 50 mW. Table 1 compares our projected silicon results to a few state-of-the-art designs.

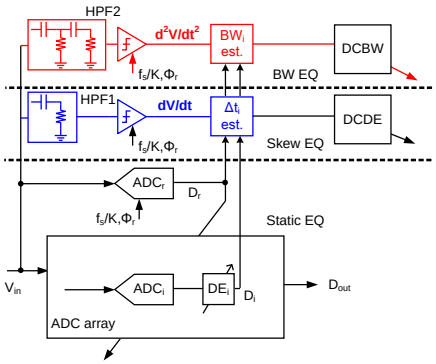

Figure 1: proposed TI-ADC system with skew and bandwidth mismatch calibration

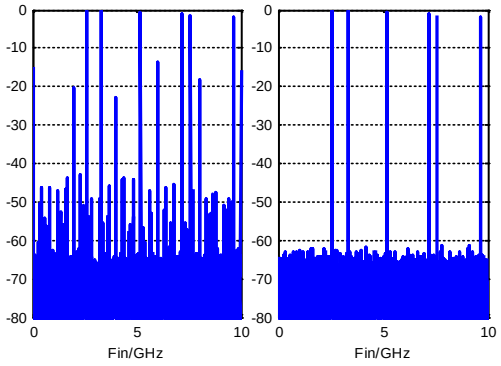

Figure 2: multi-tone input test before (left) and after (right) calibration

	Ours	VLSI13-IBM	ISSCC14-IBM	ISSCC14-ST	ISSCC14-CMU
Tech	**28nm**	32nm SOI	32nm SOI	28nm SOI	32nm SOI
Fs(GS/s)	**32**	8.8	90	10	20
SNDR(dB)	**33**	38.5	33	33.8	30.1
Power (mW)	**50**	35	667	32	69.5
Area (mm^2)	**0.06**	0.025	0.45	0.009	0.25

Table 1: Performance Comparison (projected)

Keywords: TI-ADC, calibration, hybrid SAR, reference-ADC equalization, direct derivative information

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

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Conference Publications

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