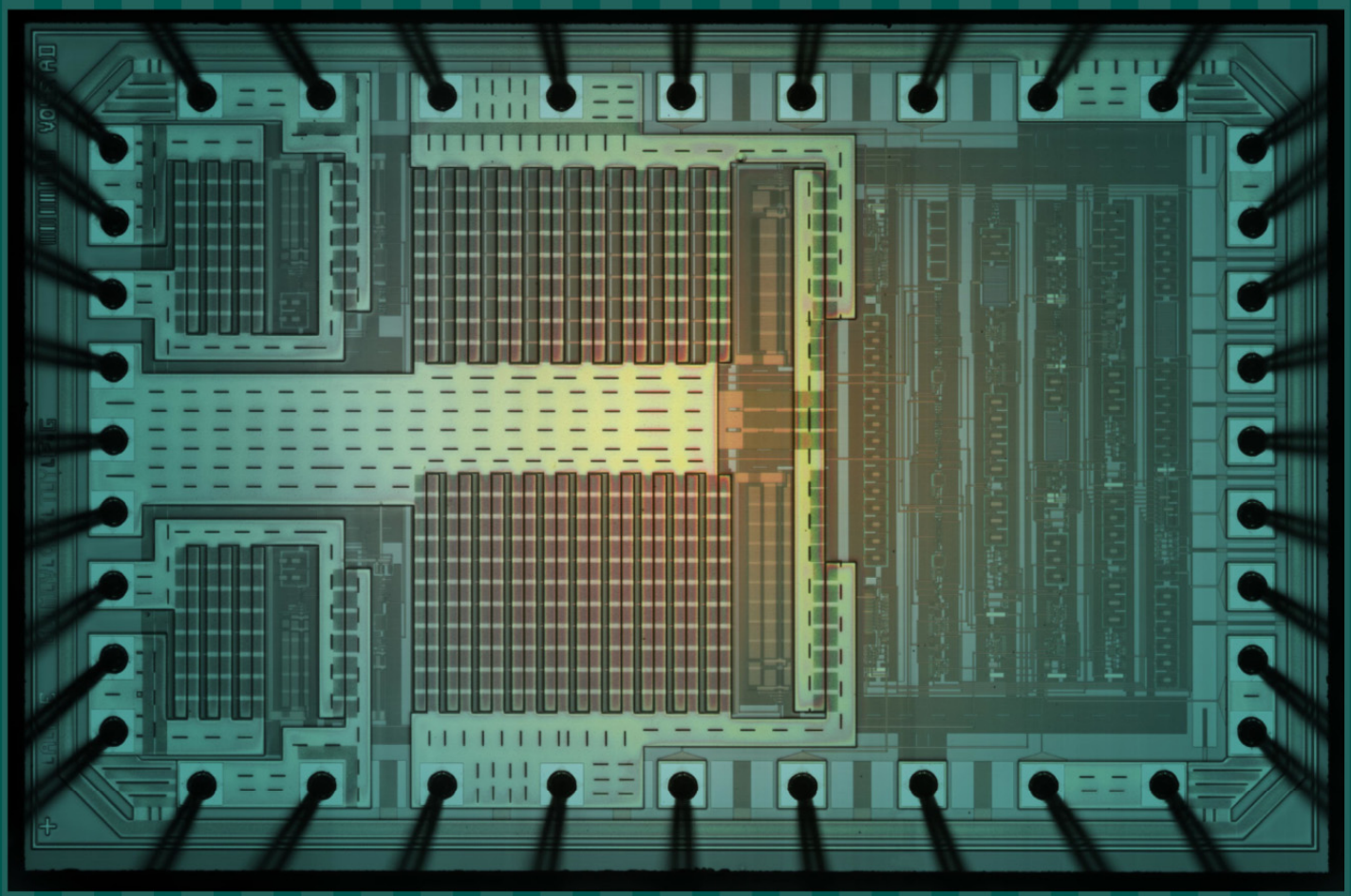
TEXAS ANALOG CENTER OF EXCELLENCE



ANNUAL REPORT 2012-2013

TxACE
TEXAS ANALOG
CENTER OF EXCELLENCE

SRC

TxACE MISSION

The Texas Analog Center of Excellence seeks to create fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, health care, and public safety and security.

TxACE THRUSTS

- *Safety & Security*
- *Health Care*
- *Energy Efficiency*
- *Fundamental Analog Circuits*

TxACE 2012-2013 ANNUAL REPORT

The Texas Analog Center of Excellence (TxACE), located at the University of Texas at Dallas is the largest analog research center based in an academic institution. Analog and mixed signal integrated circuits engineering is both a major opportunity and challenge. Analog circuitry is emerging as a critical component of nearly every product of a ~$300 billion per year integrated circuits industry, as a part of sensing, actuation, communication, power management and others. Digital integrated circuits such as microprocessors, logic circuits and memories are now integrating analog functions such as input/output circuits, phase locked loops, temperature sensors and power management circuits. It is also common to find microcontrollers with multiple analog-to-digital and digital-to-analog converters. These circuitries impact almost all aspect of modern life: safety and security, health care, transportation, energy, entertainment and many others.

The increasing importance of analog integrated circuits in electronic systems and the emergence of new applications are providing an exciting opportunity. However, the inherent difficulty of the art makes it challenging. Creation of advanced wireless technology and sophisticated sensing and imaging devices depends on the availability of engineering talent for analog research and development. TxACE was established to help translate these opportunities into economic benefits by overcoming the challenge and meeting the need. Support for TxACE has been provided through a collaboration of the state of Texas, Texas Instruments, the Semiconductor Research Corporation, the University of Texas System, and the University of Texas at Dallas.

The research tasks are organized into four research thrust areas: Health Care, Safety and Security, Energy Efficiency and Fundamental Analog. The scope of investigation extends from circuits operating at dc through terahertz, data converters that sample at a few samples/sec to 10s of giga-samples/sec, ac-to-dc and dc-to-dc converters working at µW to Watts, energy harvesting circuits, protein and DNA sensors and many more. Significant improvement on existing mixed signal systems and new applications based on this circuit research are anticipated. Students who have been exposed to hands-on innovative research are forming the leading edge of analog talent flow into industry. Close collaboration with and responsiveness to industry needs provide focus to the educational experience.

DIRECTOR'S MESSAGE

The Texas Analog Center of Excellence (TxACE) is leading analog research and education. Last year, TxACE researchers published 36 journal and 95 conference papers. They also made four invention disclosures and filed a patent application. One patent has been granted. Twenty-five Ph.D. and 9 M.S. students of TxACE have graduated.

I am thrilled to report that 5 papers from TxACE have won the best of session award at the 2013 SRC Techcon. I would like to congratulate K. Flores, J. Sankman, S. Muralidharan, E. Tabasy and S. Youn, and their collaborators. I would also like to congratulate Prof. Y. Chiu and his students of UTD for winning the best paper award at IEEE CICC 2012, Prof. P. Li and his students of TAMU for winning the best paper award at ICCAD 2012, Prof. Y. Makris and his students of UTD for their Best Paper Award at the ACM/IEEE DATE'13, and Prof. Ma and his students of UTD for the Outstanding Presentation Award at APEC 2013.

During the past year, the Center supported 57 principle investigators from 30 academic institutions including four international universities. Six universities (Rice, SMU, Texas A&M, Texas Tech, UT Austin, UT Dallas) were from the state of Texas. The Center supported 67 research tasks and 139 graduate and undergraduate students.

The TxACE laboratory is continuing to extend its capability. The Center was awarded ~$1 million by the Defense University Research Instrumentation Program last year to augment the high frequency measurement capabilities. The TxACE high frequency circuit characterization tools are helping to lower a critical barrier for advancing millimeter and sub-millimeter wave integrated circuit technology.

The integrated circuits fabrication program is continuing to grow. We supported one 65-nm CMOS run. We are planning two 65-nm and two 130-nm runs in the upcoming year. As I look forward, it is certain that we will have more frequent runs from an increasing number of foundries.

The Center had another outstanding year of accomplishments. I would like to thank the students, principal investigators, staff, and the generous support of the state of Texas, UT Dallas, the University of Texas System, TI, and SRC, as well as many friends of TxACE all over the world. I look forward to working with the TxACE team to make difference in our world through our research, education and innovation.

Kenneth K. O, Director TxACE
Texas Instruments Distinguished Chair
The University of Texas at Dallas

BACKGROUND & VISION

For many years semiconductor electronics was driven by digital logic. This led to the digital revolution that we are all familiar with: impacting things from computational power to high definition digital television. For the next 20 years, analog and mixed signal semiconductor technology is expected to drive progress as electronics continues to bridge the gap between the analog real world and the digital information infrastructure.

To lead this change, in particular to lead analog and mixed signal technology education, research, commercialization, manufacturing, and job creation, the Texas Analog Center of Excellence was formally announced by Texas Governor Rick Perry in October 2008 as a collaboration of the Semiconductor Research Corporation, the state of Texas through its Texas Emerging Technology Fund, Texas Instruments Inc., the University of Texas system and the University of Texas at Dallas. The Center seeks to accomplish these objectives by creating fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, healthcare, and public safety and security as well as by improving the research and educational infrastructure.

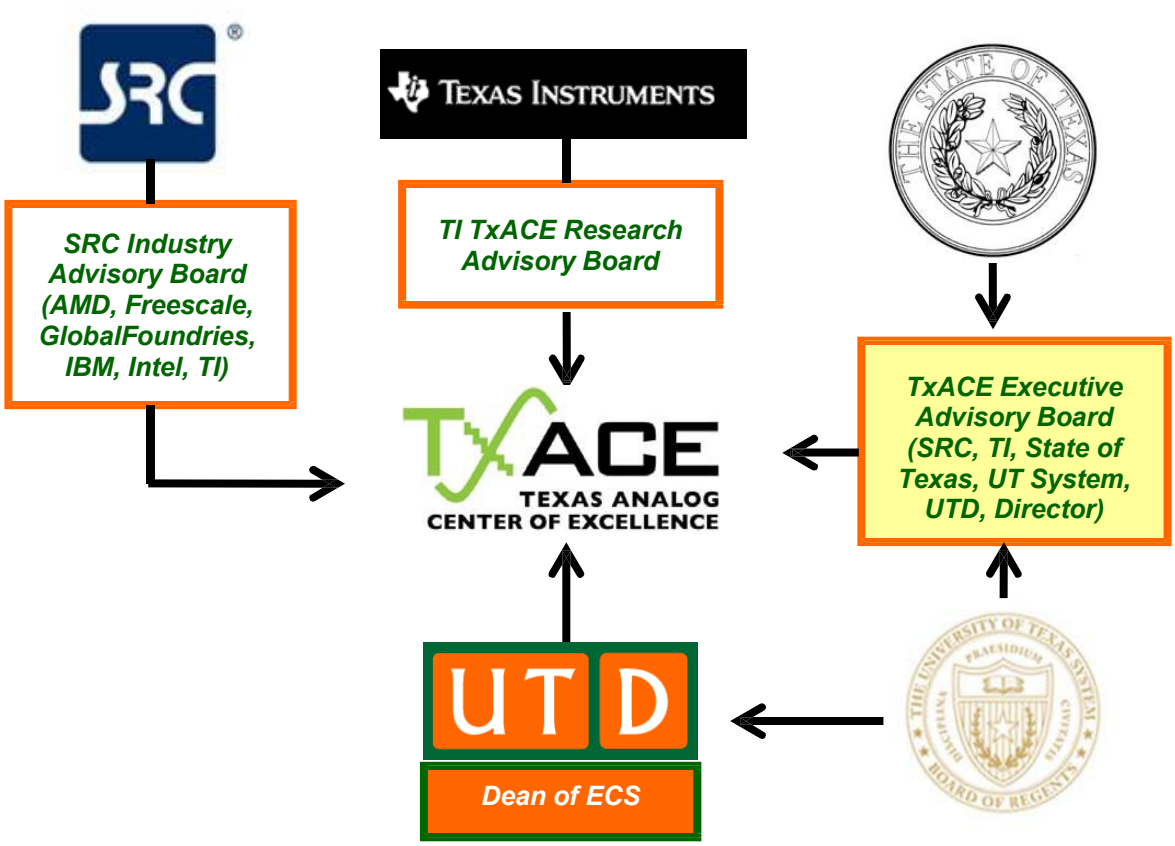


Figure 1: TxACE organization relative to the sponsoring collaboration

CENTER ORGANIZATION

The Texas Analog Center of Excellence is guided by agreements established with the Center sponsors. Members of the industrial advisory boards identify the research needs and select research tasks in consultation with Center leadership. Figure 1 diagrams the relationship of TxACE to the members of the sponsoring collaboration.

The internal organization of the Center is structured to flexibly perform the research mission while not detracting from the educational missions of the University.

Figure 2 shows the elements of the organization. The TxACE Director is Professor Kenneth O. The research is arranged into four thrusts that comply with the mission of the Center: Safety and Security, Health Care, Energy Efficiency and Fundamental Analog Research. The fourth thrust consists of vital research that cuts across more than one of the first three research thrusts. The thrust leaders are Prof. Brian A. Floyd of North Carolina State University for safety and security, Prof. Arjang Hassibi from UT Austin for health care, Prof. D. Ma of the UT Dallas for energy efficiency, and Prof. Ramesh Harjani of the University of Minnesota for fundamental analog research. The thrust leaders and Prof. Yun Chiu of the UT Dallas form the executive committee. The committee, along with the director, forms the leadership team that works to improve the research productivity of center by increasing collaboration, better leveraging the diverse capabilities of principle investigators of the Center, and lowering research barriers. The leadership team also identifies new research opportunities for consideration by the Industrial Advisory Boards.

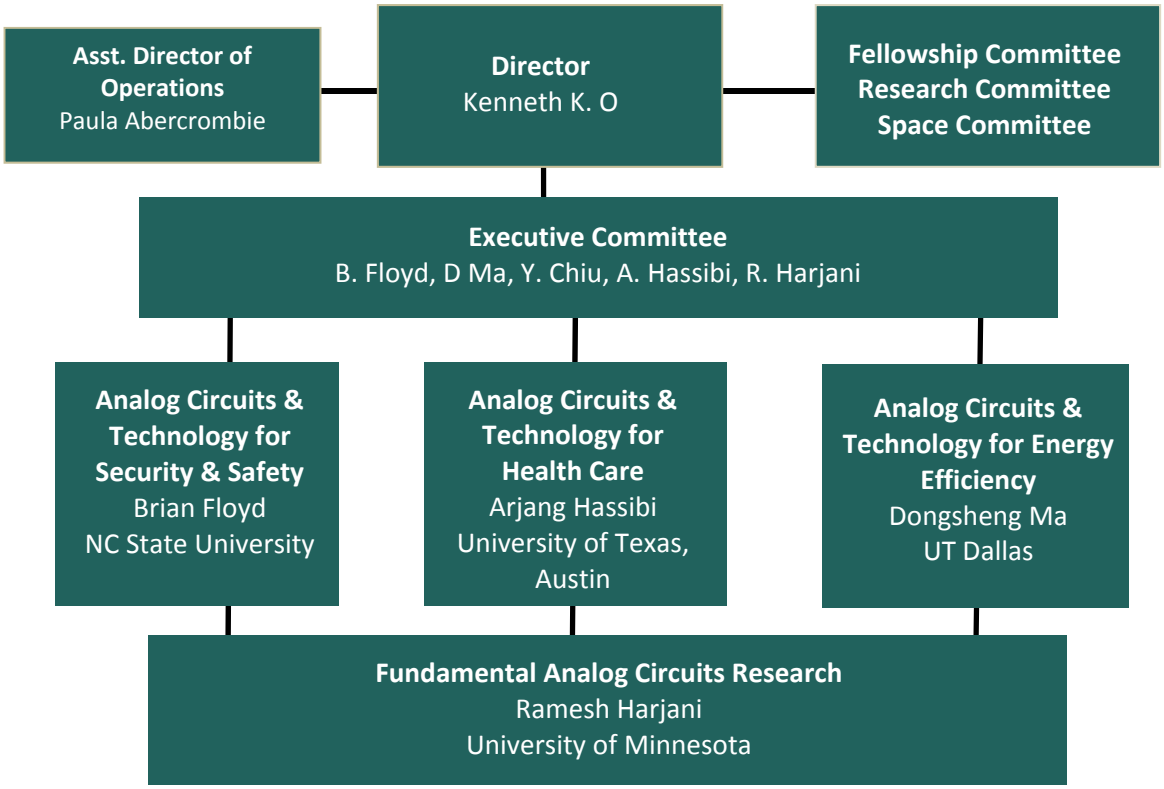


Figure 2: TxACE organization for management of research

PUBLIC SAFETY AND SECURITY

(Thrust leader: Brian Floyd, NC State University)

TxACE is developing analog technology that enhances public safety and security. The projects are intended to 1) enable a new generation of devices that can scan for harmful substances by researching 200-300-GHz silicon ICs for use in spectrometers, and 2) significantly reduce the cost of on-vehicle radar technology to improve automotive safety by researching circuit techniques that can improve manufacturing, and lower test and packaging costs.

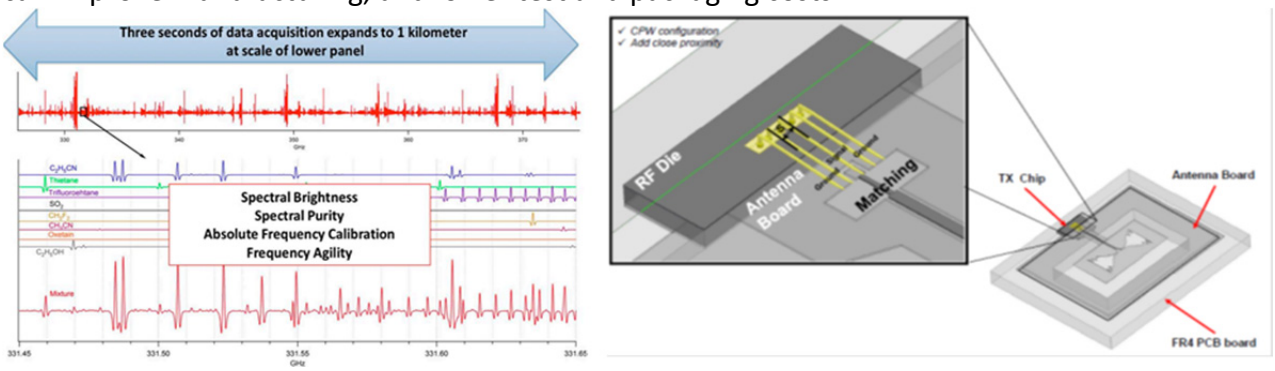


Figure 3: (Top) Rotational spectrum around 300 GHz that can be used in gas detection for safety and security applications. (D. De Lucia, Ohio State) and (Bottom) Transmitter prototype for rotational spectroscopy (O, Henderson, Blanchard, UTD).

HEALTH CARE

(Thrust leader: Arjang Hassibi, University of Texas, Austin)

Analog and RF integrated circuit technology is the essential interface enabling the power, speed and miniaturization of modern digital microelectronics to be brought to bear on an array of medical issues, including medical imaging, patient monitoring, laboratory analyses, bio-sensing and new therapeutic devices. TxACE is working to identify and support analog circuit research challenges that have the potential to enable important health-related applications. As part of this, TxACE has started a new effort to address the contact problem of EEG.

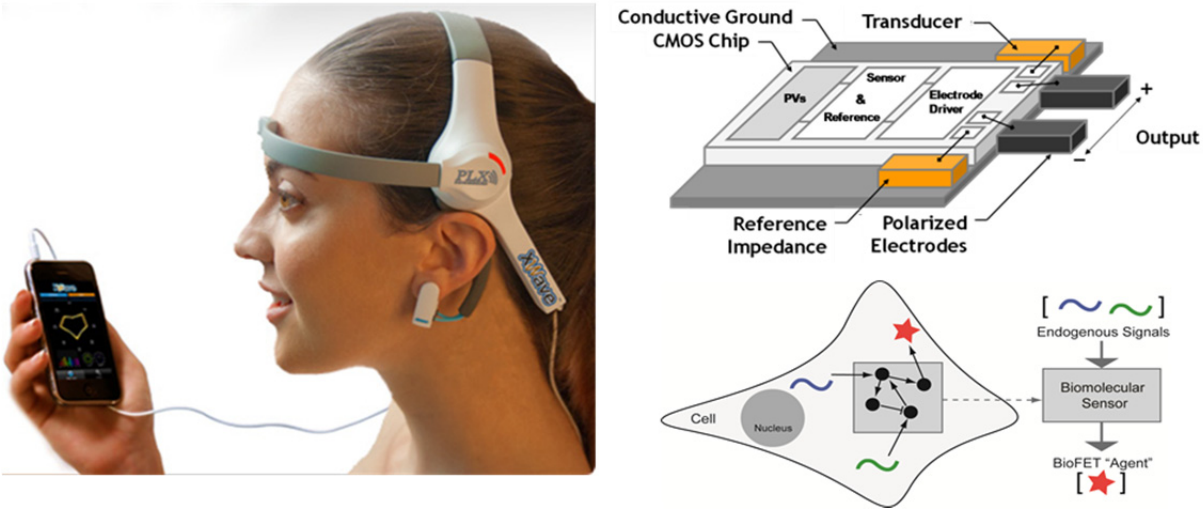


Figure 4: (Left) Electronics and signal processing for EEG, reconfigurable dry contacts for EEG (R. Jafari, UT, Dallas), (Right top) Photo-voltaic powered implantable medical sensor compatible to MRI (A. Hassibi, UT, Austin) and (Right bottom) Biomolecular sensor responding to endogenous signals and producing an output for an external device for conversion to an electrical signal (L. Bleris, UTD).

ENERGY EFFICIENCY

(Thrust leader: Dongsheng Brian Ma, UT Dallas)

TxACE is committed to alleviate the global energy problem by improving the energy efficiency of electronic systems as well as by developing analog technologies that can make energy generation more efficient. The Center is also working to energize and power long-lasting in-situ microscale devices such as wireless microsensors, biomedical implants, and portable microelectronics.

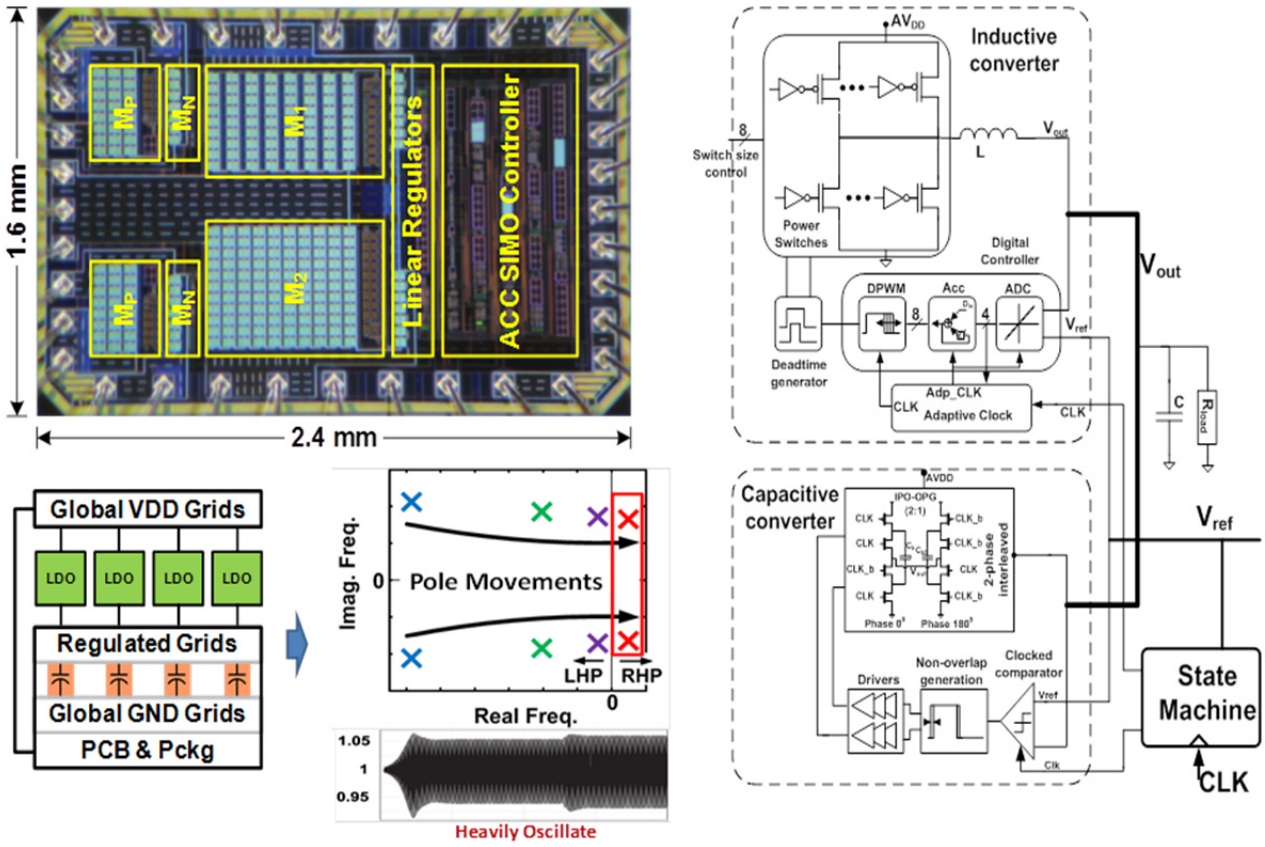


Figure 5: (Top left) Cross-regulation free single inductor multiple output DC-DC converter with nano-second load transient response (D. Ma, UT, Dallas), (Right) Combined Inductive/Capacitive DC-DC Converter for Efficient Dynamic Voltage Scaling with high efficiency over a wide output power range (R. Harjani, U. Minnesota), (Left bottom) Power distribution network instability is resulted with an increasing number of integrated LDOs. Simulation capability, system-oriented design models, and optimization-based design methodologies to enable efficient design space exploration for large PDNs with multiple integrated voltage regulators are being developed (P. Li, TAMU).

FUNDAMENTAL ANALOG CIRCUITS RESEARCH

(Thrust leader: Ramesh Harjani, University of Minnesota)

Research in this thrust focuses on cross-cutting areas in Analog Circuits which impact all of the TxACE application areas (Energy Efficiency, Health Care, Public Safety and Security). The list of research includes design of a wide variety of analog-to-digital converters, communication links, temperature sensors and I/O circuits, development of CAD tools, and testing of integrated circuits.

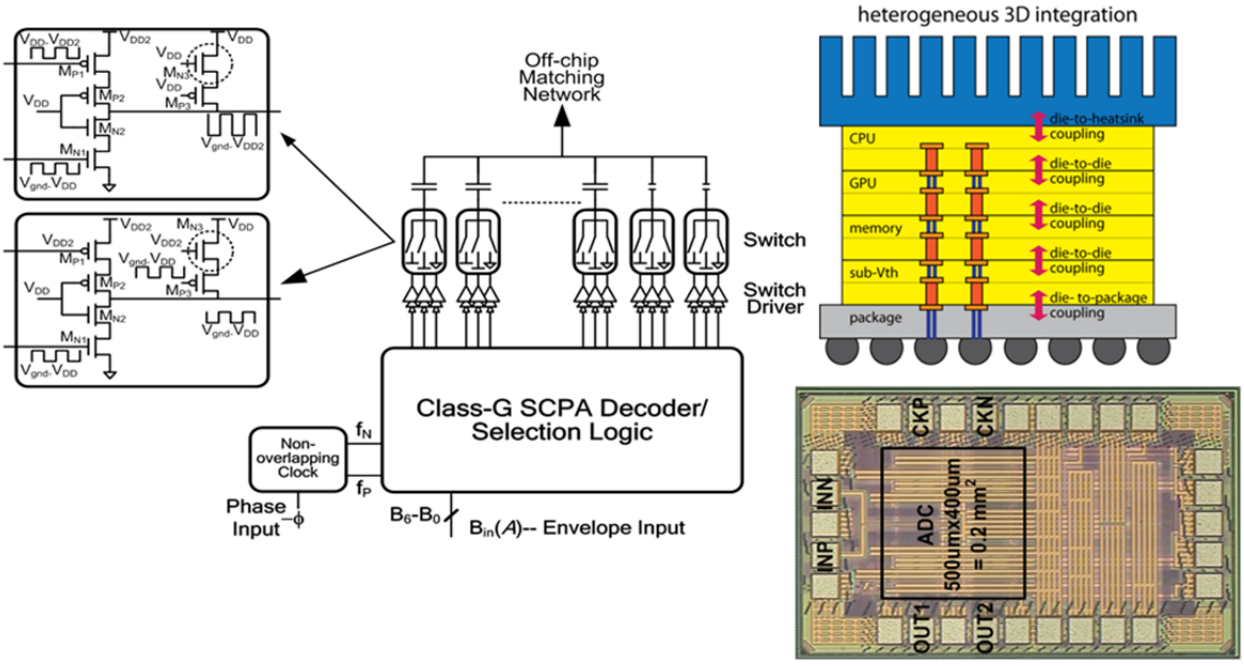


Figure 6: (Left) Class-G Switched Capacitor Power Amplifier which delivers a peak (average) output power of 24.3 (16.8) dBm with a peak (average) PAE of 44% (33%) for an *IEEE 802.11g* signal with an EVM of 2.9 % at 2.4 GHz (D. Allstot, UC, Berkeley), (Right, top) 3D Integrated Heterogeneous System (S. Mukhopadhyay, GaTech), (Left bottom) 10 GS/S four way time interleaved 6b ADC with FOM of 197 fJ/Conv. step (J. Liu, UT Dallas).

TXACE ANALOG RESEARCH FACILITY

The centralized group of laboratories of the Texas Analog Center of Excellence dedicated to analog engineering research and training occupies a ~8000 ft^2 area on the 3rd floor of the Engineering and Computer Science North building (Figure 7). The facility includes RF and THz, Integrated System Design, Embedded Signal Processing, and Analog & Mixed Signal laboratories as well as CAD/Design laboratory structured to promote collaborative research**.** The unique instrumentation capability includes network analyses and linearity measurements up to 325 GHz, spectrum analysis up to 20 THz, and cryo-measurements down to 2^{o}K. Last year, the researchers of TxACE have received approximately $1 million dollar through the Defense University Research Instrumentation Program to establish a dedicated multiple harmonic load and source pull measurement set up including pulsed measurement capabilities (up to 67 GHz for the third harmonic) and an antenna measurement set up that will allow measurements up to 325 GHz. The close proximity of researchers in an open layout enables natural interaction and compels sharing of knowledge and instrumentation among the students and faculty. The TxACE analog research facility is one of the best equipped electronics laboratories. The laboratory is available for use by TxACE researchers all over the world.

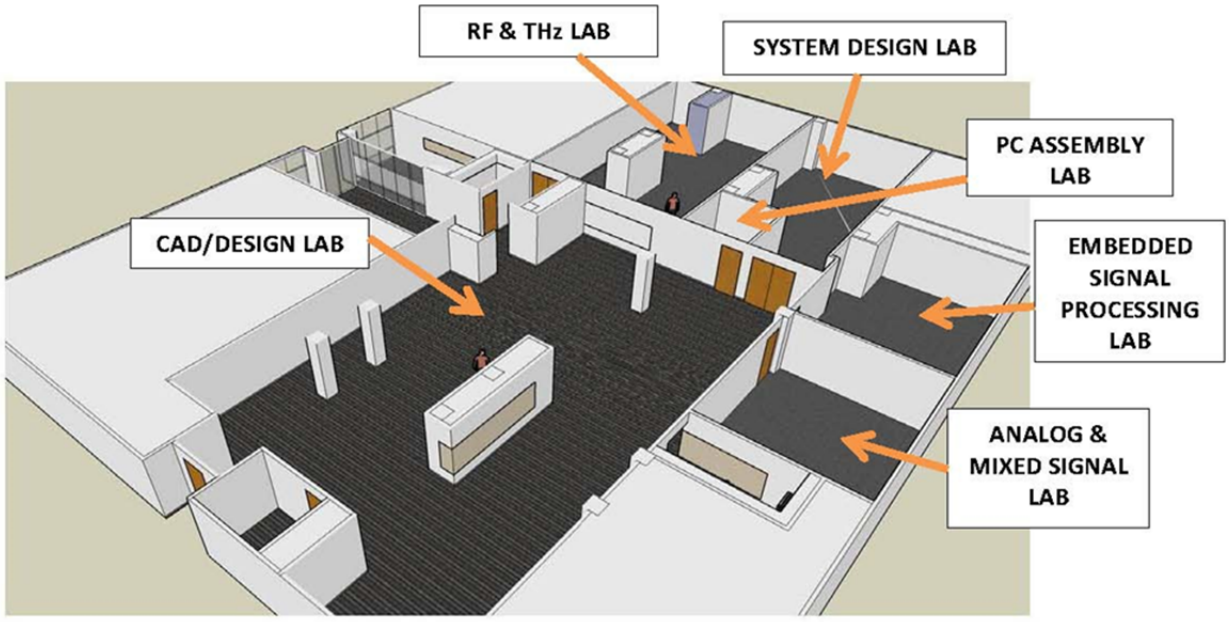


Figure 7: TxACE Analog Research Facility Sketch

RESEARCH PROJECTS AND INVESTIGATORS

The Texas Analog Center of Excellence (TxACE) is the largest university analog technology center in the world. Table 1 lists the current principal investigators of the 67 tasks from 30 academic institutions funded by TxACE. Six schools (Rice, SMU, Texas A&M, Texas Tech, UT Austin, UT Dallas) are from the state of Texas. Twenty-six are from outside of Texas. Four (Seoul National University, Korea; University of Cambridge, United Kingdom; National University of Ireland, Maynooth; and Technion – Israel Institute of Technology) (Figure 8) are from outside of the US. Of the 67 investigators, 23 are from Texas. During the past year, the Center supported 134 Ph.D. and 5 M.S. students, and 25 Ph.D. and 9 M.S. degrees were awarded to the TxACE students.

Table 1: Principal Investigators (September 2012 through August 2013)

Investigator	Institution	Investigator	Institution	Investigator	Institution
D. Allstot	U Washington	R. Gharpurey	UT Austin	H.A. Mantooth	U Arkansas
E. Alon	UC Berkeley	P. Gui	SMU	Y. Makris	UT Dallas
D. Akinwande	UT Austin	P. Hanumolu	UIUC	R. McMahon	Cambridge U
A. Apsel	Cornell	R. Harjani	U. Minnesota	U.-K. Moon	Oregon State U
B. Bakkaloglu	Arizona State	A. Hassibi	UT Austin	B. Murmann	Stanford U
B. Banerjee	UT Dallas	M. Hella	RPI	S. Mukhopadhyay	Georgia Tech
D. Blaauw	U Michigan	R. Henderson	UT Dallas	B. Nikolic	U Cal-Berkeley
L. Bleris	UT Dallas	R. Jafari	UT Dallas	K. O	UT Dallas
W. Burleson	U Mass	B. Kim	CCNY	V. Oklobdzija	NM State U.
A. Chatterjee	Georgia Tech	C. Kim	U Minnesota	S. Ozev	Arizona State
Y. Chiu	UT Dallas	J. Kim	Seoul Nat. U	S. Palermo	Texas A&M U
F. De Lucia	Ohio State U	P. Kinget	Columbia U	J. Ringwood	Nui Maynooth
J. Di	U Arkansas	F. Koushanfar	Rice University	J. Roychowdhury	UC Berkeley
Y. Eldar	Technion	M. Lee	UT Dallas	M. Saquib	UT Dallas
K. Entesari	Texas A&M U	C. Li	Texas Tech U	R. Shi	U. Washington
B. Evans	UT Austin	D. Lie	Texas Tech U	V. Stojanovic	MIT
B. Fahimi	UT Dallas	P. Li	Texas A&M U	M. Torlak	UT Dallas
B. Floyd	NC State U	J. Liu	UT Dallas	E. Vogel	Georgia Tech
R. Geiger	Iowa State U	D. Ma	UT Dallas	D. Wentzloff	U Michigan

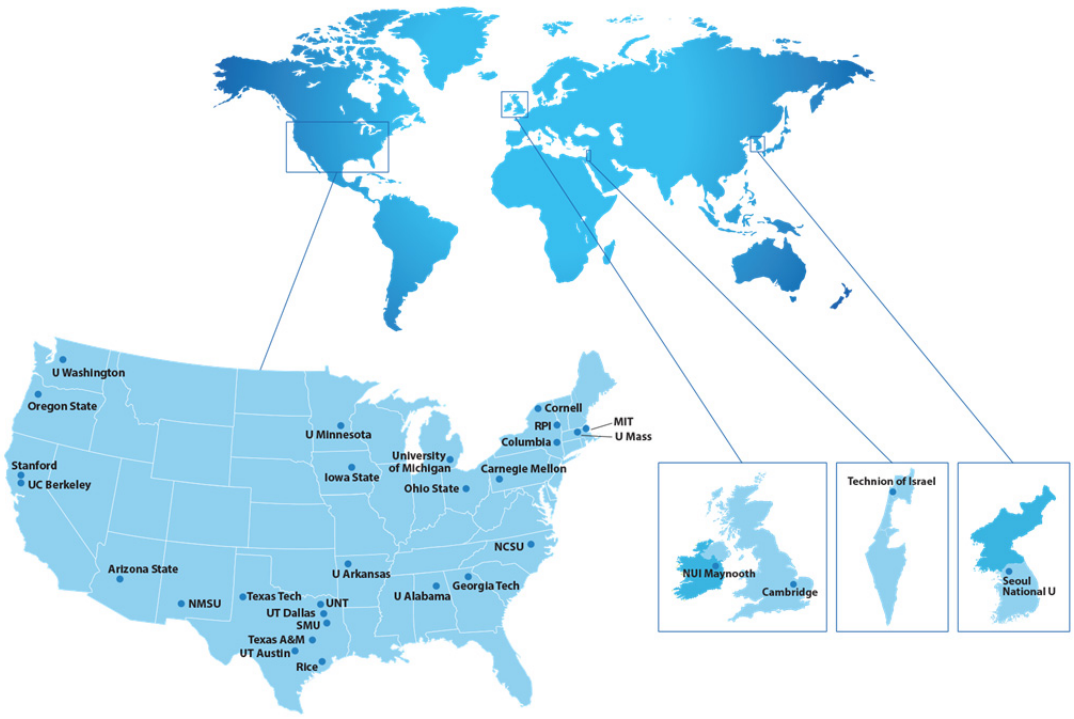


Figure 8: Member institutions of Texas Analog Center of Excellence

SUMMARIES OF RESEARCH PROJECTS

The 67 research projects funded through TxACE during 2012-2013 are listed in Table 2 below by the Semiconductor Research Corporation task identification number.

Table 2: Funded research projects at TxACE by SRC task identification number (FA: Fundamental Analog, EE: Energy Efficiency, HC: Healthcare, S&S: Safety and Security)

	Task	Thrust	Title	Task Leader	Institution
1	1836.039	S&S	UxIDs: Unclonable Mixed-Signal Integrated Circuits Identification	Koushanfar, Farinaz	Rice Univ.
2	1836.048	S&S	Millimeter and Submillimeter Gas Sensors: System Architectures for CMOS Devices	De Lucia, Frank	Ohio State
3	1836.055	HC	SPICE Models and Analog Circuits for Nanoscale Silicon Chemical- and Biological-Sensors	Vogel, Eric M.	Georgia Tech
4	1836.057	FA	High Accuracy All-CMOS Temperature Sensor with Low-Voltage Low-Power Subthreshold MOSFET Front-End and Performance-Enhancement Techniques	Li, Changzhi	Texas Tech
5	1836.058	FA	Hierarchical Model Checking for Practical Analog/Mixed-Signal Design Verification	Li, Peng	Texas A&M
6	1836.059	FA	Power-Efficient 10-20GS/s ADCs for High-Speed Communications	Liu, Jin	UT Dallas
7	1836.060	EE	Design Techniques for Scalable, Sub-1mW/Gbps Serial I/O Transceivers	Palermo, Samuel	Texas A&M
8	1836.061	HC	Analog Computing in Human Cells	Bleris, Leonidas	UT Dallas
9	1836.062	EE	System-Level Models and Design of Power Delivery Networks with On-Chip Voltage Regulators	Li, Peng	Texas A&M
10	1836.063	EE	Powerline Communications for Enabling Smart Grid Applications	Evans, Brian L.	UT Austin
11	1836.064	HC	Ultra-Low-Power Analog Front-End IC Design for Implantable Cardioverter Defibrillator (ICD) Devices	Lie, Donald	Texas Tech
12	1836.066	HC	A Fully-Integrated CMOS Platform for Microwave-Based Label-Free DNA Sensing	Entesari, Kamran	Texas A&M
13	1836.067	S&S	Characterization of CMOS Basic Building Blocks for Sub-THz Wideband Transmitters	Hella, Mona	RPI
14	1836.068	EE	Global Convergence Analysis of Mixed-Signal Systems	Kim, Jaeha	Seoul National Univ.
15	1836.069	EE	Electronic Systems for Small-Scale Wind Turbines	McMahon, Richard	Univ. of Cambridge
16	1836.070	EE	Optimum Control of Power Converters	Ringwood, John	NUI Maynooth
17	1836.071	HC	Design of Photovoltaic (PV) Power Harvesting CMOS ICs	Hassibi, Arjang	UT Austin
18	1836.072	S&S	Low Cost Test of High Speed Signals	Chatterjee, Abhijit	Georgia Tech

	Task	Thrust	Title	Task Leader	Institution
19	1836.074	S&S	Sub-45nm Circuit Design for True Random Number Generation and Chip Identification	Burleson, Wayne	Univ. of Mass/Amherst
20	1836.075	FA	Design of 3D Integrated Heterogeneous Systems	Mukhopadhyay, Saibal	Georgia Tech
21	1836.076	EE	Ultra-Low Power Delay-Insensitive Asynchronous Circuits	Di, Jia	Univ. Arkansas/Fayetteville
22	1836.077	FA	Statistical Characterization of Circuit Aging	Kim, Chris	Univ. of Minnesota
23	1836.078	FA	High-Resolution, Charge-Based A/D Converters for Nano-CMOS Technologies	Murmann, Boris	Stanford
24	1836.079	S&S	CMOS THz Detection	Hella, Mona	RPI
25	1836.080	FA	Variation-Tolerant Noise-Shaping ADCs with Embedded Digital Bias and VDD Scalable from 0.5V to 1.2V for Nanoscale CMOS	Kinget, Peter	Columbia
26	1836.081	EE	Combined Inductive/Capacitive DC-DC Converter for Efficient Dynamic Voltage Scaling	Harjani, Ramesh	Univ. of Minnesota
27	1836.082	S&S	Low-Cost Energy-Efficient 60GHz Transceivers with Built-In Self Test (BIST)	Alon, Elad	UC Berkeley
28	1836.083	S&S	Built-In Test for Power-Efficient Millimeter-Wave Phased Arrays	Floyd, Brian	NC State
29	1836.084	S&S	Single Set-up Detailed Testing of Wireless Transceiver Front-Ends Using Digital Processing	Ozev, Sule	Arizona State
30	1836.085	EE	CMOS Switched-Capacitor Power Amplifier Techniques	Allstot, David	Univ. of Washington
31	1836.086	FA	Variation Tolerant Calibration Circuits for High Performance I/O	Apsel, Alyssa	Cornell
32	1836.087	FA	A High-Speed Low-Power Reference-less Clock-Data-Recovery (CDR)	Gui, Ping	SMU
33	1836.088	EE	Efficient Digital-Intensive Wireless Transmitters Utilizing Switching Mode PAs	Gharpurey, Ranjit	UT Austin
34	1836.089	EE	Low-Power Comparator Elements for A/D Converters and High-Speed I/Os	Oklobdzija, Vojin	N. Mexico St
35	1836.090	EE	Digitally-Enhanced Clocking Strategies to Improve Energy-Efficiency of Serial Links	Hanumolu, Pavan Kumar	Oregon St
36	1836.091	S&S	Interconnects on Flexible Plastic Substrates	Akinwande, Deji	UT Austin
37	1836.092	S&S	A Model-View-Controller (MVC) Platform for Adaptive Test	Makris, Yiorgos	UT Dallas
38	1836.093	FA	Variability-Aware, Discrete Optimization for Analog Circuits	Kim, Jaeha	Seoul National Univ.
39	1836.094	S&S	Accurate FSM Approximations of Analog/RF Systems for Debugging Mixed-Signal Designs	Roychowdhury, Jaijeet	UC Berkeley
40	1836.095	FA	Test Generation for Mixed-Signal Design Verification and Post-Silicon Debugging	Shi, Richard	Univ. of Washington
41	1836.096	FA	Mixed-Signal Design Centering in Deeply Scaled Technologies	Nikolic, Borivoje	UC Berkeley
42	1836.097	FA	Dual-Domain SAR ADCs Incorporating Both Voltage and Time Information	Moon, Un-Ku	Oregon State

	Task	Thrust	Title	Task Leader	Institution
43	1836.098	HC	Sub mW Wireless Transceiver Frontends for Body Area Networks	Harjani, Ramesh	Univ. of Minnesota
44	1836.099	EE	Modeling of Analog and Switching Circuits	Mantooth, Homer Alan	Univ. Arkansas/Fayetteville
45	1836.100	EE	Test Techniques and Fault Modeling for High Voltage Devices and Boards	Kim, Bruce	UA/Tuscaloosa
46	1836.101	S&S	Sparse 2D MIMO Radar Transceiver Design and Prototyping for 3D Millimeter-Wave Imaging	Saquib, Mohammad	UT Dallas
47	1836.102	S&S	Superresolution Techniques for 3D Millimeter Wave Radars	Torlak, Murat	UT Dallas
48	1836.103	HC	Reconfigurable Brain Computer Interface	Jafari, Roozbeh	UT Dallas
49	1836.104	EE	Fault Tolerant Drive Module for Double Stator Switched Reluctance Motor Drive (DSSRM)	Fahimi, Babak	UT Dallas
50	1836.105	EE	Cross-Regulation-Free Single-Inductor Multiple-Output DC-DC Power Converters with Nano-Second Load Transient Response	Ma, Dongsheng	UT Dallas
51	1836.106	EE	IF-Sampling CMOS ADC Front-End with 100-dB Linearity	Chiu, Yun	UT Dallas
52	1836.107	FA	Verification of Multi-State Vulnerable AMS Circuits	Geiger, Randall	Iowa State
53	1836.108	EE	Performance-Oriented DVS-Compatible Single-Inductor Multiple-Output Power Converters	Ma, Dongsheng	UT Dallas
54	1836.109	FA	New Paradigms for High-Performance Amplification	Moon, Un-Ku	Oregon St
55	1836.110	EE	Distributed Power Delivery Architecture for 2D and 3D Integrated Circuits	Mukhopadhyay, Saibal	Georgia Tech
56	1836.111	FA	Advanced ADC-Based Serial Link Receiver Architectures	Palermo, Samuel	Texas A&M
57	1836.112	EE	Shortstop: Fast Power Supply Boosting for Energy-Efficient, High-Performance Processors	Blaauw, David.	Univ. of Michigan
58	1836.113	FA	Synthesized Cell-Based ADPLL Implementation for AcceleratedDesign	Wentzloff, David	Univ. of Michigan
59	1836.114	FA	Frequency Shapeable Multichannel ADCs	Eldar, Yonina	Technion
60	1836.115	EE	Analysis and Characterization of Switched-Mode DC-DC Power Converters	Li, Peng	Texas A&M
61	1836.116	EE	Efficient PA Architectures for Powerline Communications	Gharpurey, Ranjit	UT Austin
62	1836.117	FA	Performance and Reliability Enhancement of Embedded ADCs with Value-Added BIST	Geiger, Randall	Iowa State
63	1836.118	EE	Low Noise, Low Ripple Fully Integrated Isolated DCDC Converters for Signal Chain Applications	Bakkaloglu, Bertan	Arizona State
64	1836.119	S&S	Demonstration of 180-300 GHz Transmitter for Rotational Spectroscopy	O, Kenneth	UT Dallas

	Task	Thrust	Title	Task Leader	Institution
65	1836.120	S&S	Evaluation of Frequency and Noise Performance of CMOS 180 – 300 GHz Spectrometer Transmitter and Receiver Components	Lee, Mark	UT Dallas
66	1836.121	S&S	Demonstration of 180 – 300 GHz Receiver for Rotational Spectroscopy	Banerjee, Bhaskar	UT Dallas
67	1836.122	S&S	On-Chip Integration Techniques for 180-300 GHz Spectrometers	Henderson, Rashaunda	UT Dallas

ACCOMPLISHMENTS

TxACE has made significant research progress. Table 3 summarizes the number of publications and inventions resulting from the TxACE research during September 1, 2012 to August 31, 2013, while Table 4 lists the major research accomplishments for the Center during the period. The TxACE researchers have published 95 conference papers and 36 journal papers. They have also made 6 invention disclosures and filed one patent application. One patent was granted. The list of publications is included as Appendix I. Following the tabulation, brief summaries of each project are provided.

Table 3: TxACE number of publications (September 2012 through August 2013)

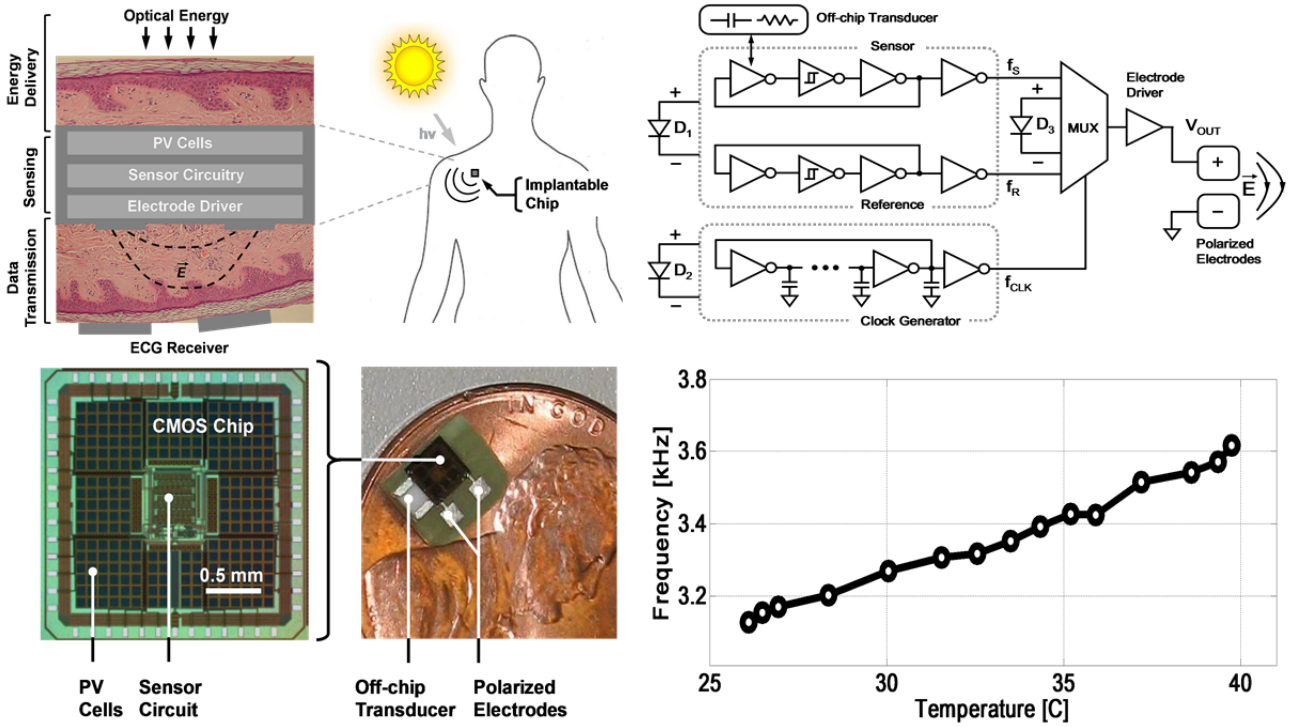
Conference Papers	Journal Papers	Invention Disclosures	Patents Filed	Patents Granted
95	36	6	1	1

Table 4: Major TxACE Research Accomplishments (September 2012 through August 2013)

Category	Accomplishments
Fundamental Analog (Circuits)	ADC-based high-speed serial links aim to improve interconnect bandwidth density in an energy-efficient manner. Embedding the normally required channel equalization within the ADC has the potential for significant power savings. The first 10Gs/s ADC with embedded FFE/DFE that achieves a BER of 10^9 at 10Gb/s over a 10" channel is demonstrated. The 6bit ADC has an FOM (0.48pj/c-s) that is as competitive as the FOM of plain vanilla ADCs that operate at that speed. (1836.111, PI: S. Palermo, Texas A&M University).
Fundamental Analog (Circuits)	Successive approximation register (SAR) ADCs have the potential to consume the lowest power and can be made to operate at reasonably high speeds by using time interleaving (~10Gsps). However, this requires extremely small capacitor values. Measurements from a 65nm CMOS process show excellent matching (σ) of 1.2% for 0.45fF capacitors with a Pelgrom coeff. of ~0.85% at 1fF. This opens up the field for extremely low power high-speed ADCs using SARs. (1836.078, PI: B. Murmann, Stanford University)
Fundamental Analog (CAD)	Discretization of the analog design space exploiting the inherent variability in the IC process can lead to a fast, deterministic optimizer that can perform quick, incremental 'what-if' analyses. This research has been able to justify the exploration of discrete spaces even for analog designs allowing a new era of analog CAD tools that can utilize efficient algorithms and approaches that have up until now been relegated to digital CAD tools. (1836.085, PI: J. Kim, Seoul National University)
Energy Efficiency (CAD)	A hybrid stability margin concept and the associated stability checking method for power distribution networks with integrated linear low-dropout voltage regulators (LDOs) are demonstrated. It employs a localized LDO design methodology that optimizes individual LDOs locally while ensuring the network-level stability. (Task ID 1836.062, Peng Li, Texas A&M University)
Energy Efficiency (Circuits)	An inductive and capacitive combined converter provides efficient regulation over the wide power range demanded by the DVS operation. The converter is fully integrated with passives constructed on chip, using an IBM 32nm SOI process. The converter attains a maximum efficiency of 85.5% in the high power range using the inductive converter. The capacitive converter achieves a peak efficiency of 79%. The power density of the entire chip is 8.8W/mm^2. (1836.081, PI: R. Harjani, University of Minnesota)
Energy Efficiency (Circuits)	The project seeks to operate the link at an energy-efficient supply voltage and leverage the link inactivity periods to reduce the power consumption, with specific focus on fast locking clock generation circuits. A prototype chip demonstrated a 2.5GHz fast power-on clock multiplier, which achieves 10ns power-on time (3 reference cycles). (1836.090, Pavan Kumar Hanumolu, Oregon State University)
Health Care (Circuits)	Designed and experimentally validated a new multi-finger dry electrode system for EEG and ECG applications that dynamically varies the number and arrangements of its fingers to compensate for the non-idealities and the electrode-skin interface as well as motion artifacts. (1836.103, PI: R. Jafari, University of Texas at Dallas)

Category	Accomplishments
Health Care (Circuits)	Demonstrated a single chip cardioverter defibrillator (ICD) analog front-end IC (AFE) for implantable devices. Moreover, the level of integration has been significantly improved by including the instrumentation amplifiers (INAs), filters, VGAs, and SAR ADCs in addition to the AFE components. (1836.064, PI: D. Y. C. Lie, Texas Tech University)
Health Care (Circuits)	Demonstrated a fully-integrated photovoltaic (PV) driven energy harvesting IC for implantable device application. The measurements demonstrate that ~1μW/mm^2 of photodiode area can be harvested by CMOS-integrated diodes beneath 3-5 mm of soft tissue. This level of power is then used to run an oscillator-based sensor and also transmit its output signal to the surface of the skin to be picked up by conventional ECG electrodes and devices. (1836.071, PI: A. Hassibi, University of Texas at Austin)
Security and Safety (Circuits)	Adaptive test is challenging for analog and RF testing. A statistical model was developed which combines both intra-die and inter-die modeling approaches for reducing test cost in analog/RF ICs. Also, a spatial decomposition method was developed under the model view controller framework for breaking down the variation of a wafer to its spatial constituents. (1836.092, PI: Y. Makris, Univ. Texas, Dallas)
Security and Safety (Circuits)	Low-cost CMOS technology can potentially be used to realize sub-millimeter-wave and Terahertz receivers and transmitters for imaging applications. A terahertz SPICE model was developed which can predict the responsivity and noise performance of 65nm FETs, and the model was validated with 200GHz measurements. (1836.079, PI: M. Hella, RPI)
Security and Safety (Circuits)	Physically unclonable functions (PUFs) were developed which exploit layout variations of gate pitches near “forbidden pitches” to achieve higher uniqueness for the PUF, and a test chip was fabricated in 45nm CMOS. (1836.074, PI: W. Burleson, Univ. Mass, Amherst)
Security and Safety (Circuits)	Demonstrated THz spectroscopic measurement of absolute concentrations of plasma constituents and their temperatures in an Applied Materials Plasma reactor for semiconductor manufacturing. (1836.048, PI: F. De Lucia, Ohio State University)

Health Care Thrust



Summary of Accomplishments

Category	Accomplishment
Health Care	Designed and fabricated and the entire cardioverter defibrillator (ICD) analog front-end IC (AFE) for implantable devices in a single chip and experimentally validated its performance by applying proper test benches for the prototype IC. Moreover, the level of integration has been significantly improved from previous designs by including the instrumentation amplifiers (INAs), filters, VGAs, and SAR ADCs in addition to the AFE components. (1836.064, PI: D. Y. C. Lie, Texas Tech University). Publication: W. Hu, *et al.*, *IEEE Trans. Circuits and Systems* – I (TCAS-I), 60, 7, pp. 1726-1739 (2013)
Health Care	Demonstrated a fully-integrated photovoltaic (PV) driven energy harvesting IC for implantable device application. The measurements demonstrate that ~1µW/mm^2 of photodiode area can be harvested by CMOS-integrated diodes beneath 3-5 mm of soft tissue. This level of current (and power) is then used to power up an oscillator-based sensor and also transmit it output signal to the surface of the skin to be picked up by conventional ECG electrodes and devices. (1836.071, PI: A. Hassibi, University of Texas at Austin) Publication: S. Ayazian, V. A. Akhvan, E. Soenen, and A. Hassibi, "A Photovoltaic-Driven and Energy-Autonomous CMOS Implantable Sensor," *IEEE Transactions on Biomedical Circuits and Systems,* 6-4, pp. 336-343 (2012).
Health Care	Designed and experimentally validated a new multi-finger dry electrode system for EEG and ECG applications that dynamically varies the number and arrangements of its fingers to compensate for the non-idealities and the electrode-skin interface as well as motion artifacts. (1836.103, PI: R. Jafari, University of Texas at Dallas) Publication: Y. Zou *et al.*, "Score-base Adaptive Training for P300 Speller Brain Computer Interface," 2013 *IEEE ICASSP*.

TASK 1836.055, SPICE MODELS AND ANALOG CIRCUITS FOR NANOSCALE SILICON CHEMICAL- AND BIOLOGICAL-SENSORS

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SIGNIFICANCE AND OBJECTIVES

Nanoscale chemical and biological sensors have been demonstrated, but little attention has been given to SPICE models and support circuitry. This project will develop physically realistic SPICE models for the sensor device. SPICE model creation will be followed by design of suitable support circuitry for a complete system.

TECHNICAL APPROACH

The design of circuits to support the biological sensor will require a suitable SPICE model which comprehends the unique properties of this device. Generating such a SPICE model in turn requires a thorough understanding of the physics of the sensor and its operating environment. To improve the understanding of the biosensor device physics and generate the necessary data for a suitable SPICE model, a combination of theoretical analysis and TCAD modeling is being utilized. With a SPICE model available, reference support circuits are being developed including novel neuromorphic detection circuits.

SUMMARY OF RESULTS

A schematic of the sensor element under study is shown in Figure 1 [1]. Studies during the first year of this project provided understanding of the device physics of the biosensor configuration. We then developed the first ever SPICE model for these types of sensors and developed a novel transient simulation methodology to simulate the effect of sensor noise on a differential pair amplifier detection circuit. An example of the noisy output of a sensor is shown in Figure 1(c). In this final year, we explored novel neuromorphic circuits [2] to detect biosensor signals in large amounts of noise.

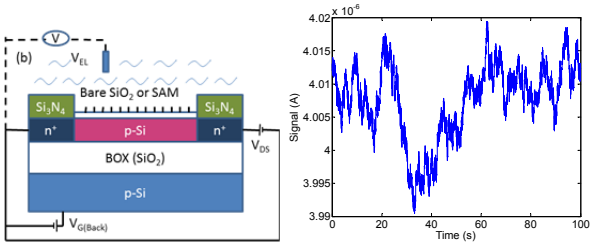
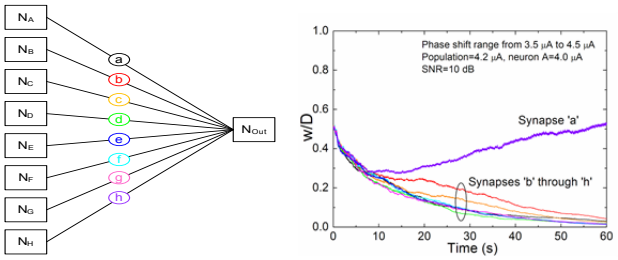


Figure 1: (a) Sensor cross-section with measurement circuit. (b) Example of the noisy output signal of a sensor.

Neural networks perform efficiently at tasks involving pattern recognition and classification in large datasets. A biosensor microarray with a large number of surface functionalizations would provide a large set of imprecise and noisy data (i.e. artificial olfaction). Neurons naturally perform auto-zeroing or sampling-like noise reduction. We have recently developed and SPICE modeled neuromorphic circuits which exhibit learning rules similar to biology [2]. We have simulated a neural network as shown in Figure 2. The input to the neurons is a phase modulated signal representing the amount of detected species for an individual sensor. In this example, only neuron A has input from a functionalized sensor. Neurons B-H have input from reference sensors that are exposed to the electrolyte, but are not functionalized such that they do not respond to the target species



Because of the phase difference between the target neuron A and the reference neurons, the weight of the synapse associated with neuron A easily detects the presence of the species even with the large amount of noise shown in Figure 1 (b).

Keywords: Chemical, Biological, Sensor, SPICE, Neuromorphic.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] E. M. Vogel, "Fabrication, Characterization, and Modeling of Silicon-on-Insulator Field-Effect-Transistor Nanoribbon Biosensors," Biosensors and Bioelectronics, Chicago, IL, June 18, 2013.

[2] A. Subramaniam, K. D. Cantley, G. Bersuker, D. Gilmer, and E. M. Vogel, "Spike-timing-dependent Plasticity using Biologically Realistic Action Potentials and Low-temperature Materials," IEEE Transactions on Nanotechnology **12**, 450 – 459 (2013).

TASK 1836.061, ANALOG COMPUTING IN HUMAN CELLS

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SIGNIFICANCE AND OBJECTIVES

The objective of this project is the implementation of molecular circuits capable of responding to specific cellular disease-related signals and producing accordingly outputs that can be quantified using external devices.

TECHNICAL APPROACH

We are working on a general framework for bridging endogenous cellular to extracellular information (Figure 1), using programmable reagents that are prepared according to the tissue type and disease. Our multi-component RNA- and protein- based biosensor circuits are able to: (a) detect complex conditions related to abnormal expression of a number of molecular signals (microRNA and transcription factor) in human cells, (b) upon detection release biologically active modules in order to transduce the information to external devices.

SUMMARY OF RESULTS

Complex combinations of abnormally expressed microRNAs are an excellent indicator of cell state. A system capable to detect these conditions may be used as a highly selective tool for diagnosis and treatment.

We have implemented direct and inverter microRNA sensors. Both sensors have restriction enzyme sites within the 3'UTR, on both sides of the microRNA targets, to permit rapid replacement of the microRNA under study. We engineered sensors for miR16, miR17, miR21, miR10b, miR29a, miR34a, miR34b, miR34c, miR146a, miR192, miR194, miR210, miR215, miR221.

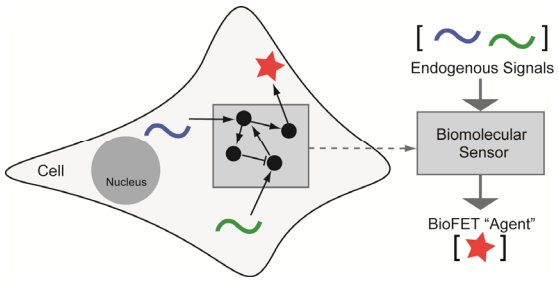

Figure 1: The biomolecular sensor responding to endogenous signals and producing an output for an external device.

We process endogenous information using sophisticated synthetic circuits. As an example, we studied the effect of negative feedback regulation (Figure 2) on cell-wide (extrinsic) and gene-specific (intrinsic) sources of uncertainty [1]. Our experiments reveal that negative feedback reduces extrinsic noise while slightly increasing intrinsic noise. Importantly, negative feedback reduces the total noise. By comparing these results to simple regulation, we showed that negative feedback is the most efficient way to reduce extrinsic fluctuations by introducing a sole additional regulatory wiring.

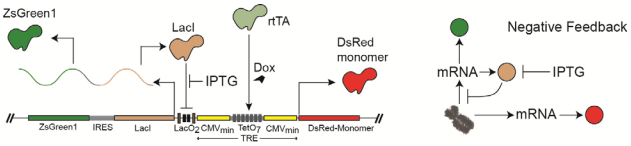

Figure 2: Negative feedback architecture.

To connect to an external device, we have been testing proteins that can transduce endogenous information outside of a cell. In particular, we constructed genetic circuits that produce human chorionic gonadotropin (hCG). The technology built around sensing hCG is available commercially and is used as a diagnostic tool for pregnancy. HCG is a unique hormone produced endogenously during homeostasis only when an ovum is fertilized by a sperm. Most pregnancy technology resides in a variant of an ELISA test for the hCG protein. We engineered synthetic circuits that produce hCG in the presence and absence of selected microRNAs.

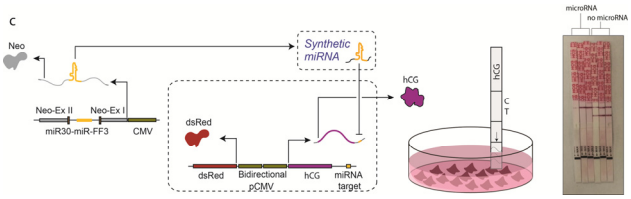

Figure 3: hCG mediator for external sensing. Experiments were performed using human kidney cells. Results show the correct reading for the "no microRNA" and "microRNA" cases.

For control experiments illustrated in Figure 3, we used transient transfections to deliver two synthetic circuits into the cells. With the first circuit we control the level of a synthetic microRNA while the second circuit produces the hCG protein under the microRNA regulation. In the absence of the microRNAs the circuit product hCG accumulated in the media. Using hCG test strips we received a verification that the hormone is present in the media.

Keywords: **Synthetic biology, biosensors, microRNA**.

MAJOR PAPERS/PATENTS

[1] Shimoga, V., White, J., Li, Y., E. Sontag, L. G. Bleris. Synthetic mammalian transgene negative autoregulation. Nature/EMBO Molecular Systems Biology, 9:670, 2013.

[2] Guinn, M., Li, Y., L. G. Bleris. A 2-input Decoder Circuit in Human Cells. The International Workshop on Bio-Design Automation (IWBDA), June 2013.

TASK 1836.064, ULTRA-LOW POWER ANALOG FRONT-END IC DESIGN FOR IMPLANTABLE CARDIOVERTER DEFIBRILLATOR (ICD) DEVICES

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SIGNIFICANCE AND OBJECTIVES

The significance and objectives of the project are to design ultra-low-power analog front-end (AFE) ICs for implantable cardioverter defibrillator (ICD) devices and other biosensors. Since the AFE circuits must *always* stay on, it is critical to design with both system-level and circuit-level techniques to reduce power dissipation

TECHNICAL APPROACH

We have performed both SPICE simulation and measurement on the proposed entire AFE channel IC, which includes a couple of designs of the differential instrumentation amplifiers (INAs), differential band-pass filters (BPFs), differential-to-single-end variable gain amplifiers (VGAs), and single-ended successive approximation register (SAR) ADCs. The power consumption is reduced by designing low-power blocks on the circuit level, and by combining two channels on the system level. From the SPICE simulation results, our works are comparable with the state-of-the-art ones. The entire AFE IC only consumes <2 μA and may provide more gain and frequency settings among other works.

SUMMARY OF RESULTS

In this 3rd year effort, our focus has been on improving the integration of the entire AFE IC channel and setting up of the proper test bench for the AFE IC characterization. Moreover, two instrumentation amplifiers (INAs), filters, VGAs, SAR ADCs and entire AFE channels IC have been taped out. As shown in Fig. 1, a typical AFE circuitry for an ICD/bio-sensor can have an INA, a filter, a VGA and an ADC.

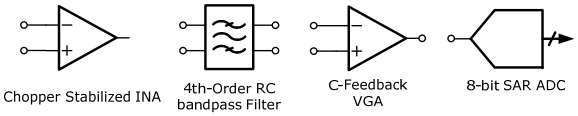

Fig. 1 Circuit blocks used in the designed ICD AFE IC.

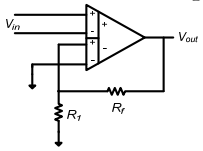

Fig. 2 A DDA-based INA topology used in this work

A chopper-stabilized INA is designed based on the Differential Difference Amplifier (DDA) topology as shown in Fig. 2, which can achieve high common-mode rejection ratio (CMRR) since its CMRR is theoretically only dependent on the mismatches of the input port (i.e., resistors mismatches for the feedback/gain setting should only influence the closed-loop gain).

A block level diagram of the INA is shown in Fig. 3, where it includes a selective feedback arrangement controlled using two control signals, making the INA possible for two gain modes (i.e., 20/40 dB). The output chopper modulator is realized using two chopper switches with CMOS devices to relieve the charge injection and clock feed-through issues. A chopper modulation frequency of 5 kHz was used. For simplicity, the block level in Fig. 3 shows the switches as one combined unit.

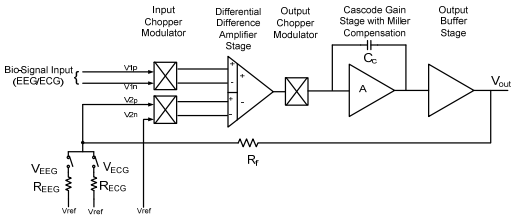

Fig. 3 A block diagram of the chopper stabilized INA

The measure current consumption of the AFE IC is 1.4-2 µA and half of it comes from the INA. The SPICE simulated integrated input-referred noise of the AFE in the worst case is 6 µVrms. The integrated bandwidth of INA is 300 Hz and that of filters and VGA is 1 kHz. While calculating the noise of the filter chain referred to the AFE IC, we use an INA gain of 20 dB rather than 40 dB to avoid the possibility of signal saturation/compression. The die size is 3300x1300 µm^2 as shown in Fig. 4.

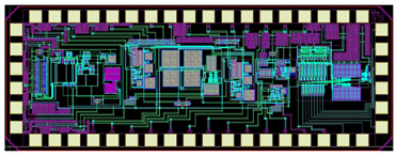

Fig. 4 The layout of the proposed entire AFE IC channel.

Keywords: analog front-end (AFE) integrated circuit (IC), implantable cardioverter defibrillator (ICD), SAR (successive approximation register) ADC, sub-threshold CMOS, ultra-low-power sensor

INDUSTRY INTERACTIONS

Texas Instruments, IBM and Freescale

MAJOR PAPERS/PATENTS

[1] W. Hu, *et al.,* IEEE Trans. Circuits and Systems – I (TCAS-I), 60, 7, pp. 1726-1739 (2013)

[2] W. Hu *et al.,* Proc. IEEE MWSCAS, pp. 1196-1199, (2012)*; Invited.*

TASK 1836.066, TITLE (A FULLY-INTEGRATED CMOS PLATFORM FOR MICROWAVE-BASED LABEL-FREE DNA SENSING)

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SAMUEL PALERMO, TEXAS A&M UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

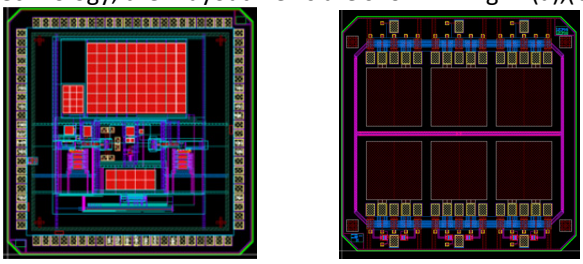
Implementation of cheap and compact sensors/systems to probe biochemicals and their interactions, at the molecular level, in point-of-care settings. Broadband, *bulk/volumetric* measurements of complex permittivity of liquid phase chemicals and solutions of small biomolecules can indicate molecular structure/conformation (chip#1). *Surface* charge measurements can indicate affinity-based interaction of probes/targets in DNA assays (chip#2).

TECHNICAL APPROACH

Employing CMOS lumped-circuit, broadband dielectric spectroscopy systems. In chip#1, bulk/volumetric measurements are done with *relatively wide-gap*, planar, interdigitated, fringing-field capacitive sensors. The detected oscillation frequency shift of a MUT-loaded, sensing ring oscillator (*relative* to unloaded, *reference* ring oscillator) varies with *both* load conductance (G) *and* capacitance (C). C and G are mapped to MUT polarization and dielectric loss, respectively. In chip#2, stand-alone, *very narrow-gap* (to detect changing *surface* charge with occurrence of hybridization), interdigitated sensors are built on CMOS, then coated with gold (to graft DNA probes) using post-processing. RF/microwave detection avoids electrode polarization and dielectric loss of water

SUMMARY OF RESULTS

Both chips are under fabrication using 180 nm CMOS technology, their layout views are shown in Fig 1. (a),(b).

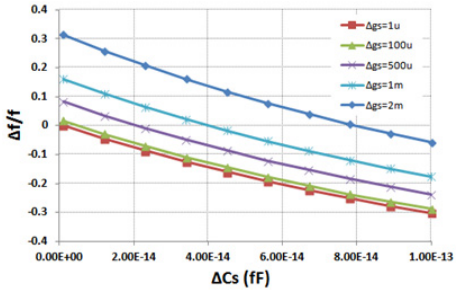


(a) (b)

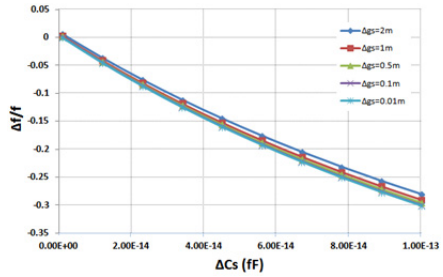
Figure 1: CAD layout view of (a) chip#1, and (b) chip#2

Chip#1 will be tested directly after fabrication with standard chemicals. Chip#2 is planned to be post-processed by Intel (see industry interactions) after fabrication and bio-tests for DNA detection will be performed with the aid of Biology Department in TAMU to characterize the bio-sensor. After successful characterization of both chips, the bio-sensors implemented in chip#2 will be merged to the CMOS electronics implemented in chip#1 with proper modifications (to occur in Fall 2013 and Winter 2014)

Fig. 2 illustrates the concept behind complex permittivity detection in chip#1 using ring oscillators and an amplitude locked-loop (ALL). In Fig. 2 (a), the detected relative frequency shift depends on both G and C (ALL: OFF). In Fig. 2 (b) the relative frequency shift is desensitized to changes in load conductance (ALL: ON)



(a)



(b)

Figure 2: Complex permittivity detection (chip#1).

Keywords: Biosensor, frequency synthesizer

INDUSTRY INTERACTIONS

Intel

MAJOR PAPERS/PATENTS

[1] El-Hadidi, O., Elkholy, M., Helmy, A.A., Palermo, S., and Entesari, K., "A CMOS Fractional-N PLL-Based Microwave Chemical Sensor with 1.5% Permittivity Accuracy," *Microwave Theory and Techniques, IEEE Transactions on*, (Accepted for publication).

TASK ID 1836.071, DESIGN OF PHOTOVOLTAIC (PV) POWER HARVESTING CMOS ICS

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SIGNIFICANCE AND OBJECTIVES

Energy autonomous ICs that can harvest energy from environment are an enabling technology for autonomous sensors. The existing integrated energy harvesting systems generally require off-chip transducer elements that cannot be monolithically integrated using CMOS. We plan to create Standard CMOS-embedded photovoltaic (PV) cells, as energy harvesters, and demonstrate their applicability in biomedical implantable sensor devices.

TECHNICAL APPROACH

The general idea is to take advantage of the existing on-chip photodiodes of CMOS processes as photovoltaic (PV) energy-harvesting photocells to power up an on-chip sensor (see Fig. 1). Specifically, a CMOS IC is designed to harvest µW's of power from the ambient light passing through the soft tissue to perform real-time sensing and transmit the acquired data to the skin surface in a neuromorphic fashion and by using a set of in-vivo polarized electrodes (1). The signal is then picked up by a set of conventional ECG electrodes. An implantable sensor built on this principle is MRI compatible as it requires no RF coil or antenna and contains no paramagnetic material.

SUMMARY OF RESULTS

In the year 3 of this project, we have focused on demonstrating the functionality of the complete system *in-vitro* which includes the CMOS PV cell, the on-chip ring oscillator-based sensor, and the neuromorphic transmitter system. To perform the tests, as shown in Fig. 2, we generally placed the chip beneath a model tissue system (mainly bovine soft tissue) and measured the characteristics of the system including the delivered power and the transmitted/received signals. Our measurements demonstrated that the chip can harvest ~ 1µW/mm^2 of current under bright light conditions beneath 3-5 mm of soft tissue (including skin). Our measurements also demonstrated that, coupling factor between the electrodes is sufficient to pick up the signal by conventional ECG electrode system (2).

Keywords: Photovoltaic, Implanted Devices, Sensor, CMOS, Energy Harvesting

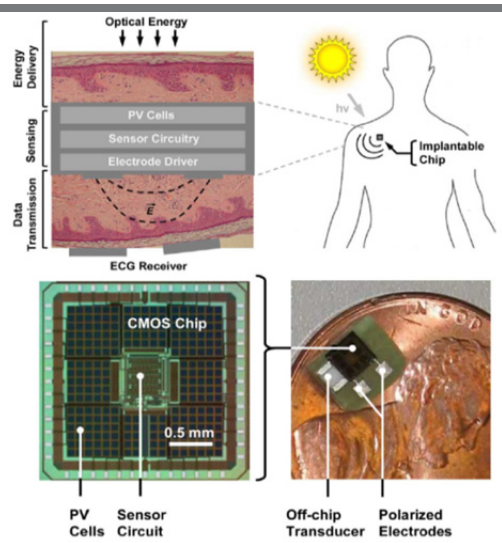

Figure 1: A PV-driven energy-autonomous CMOS sensor.

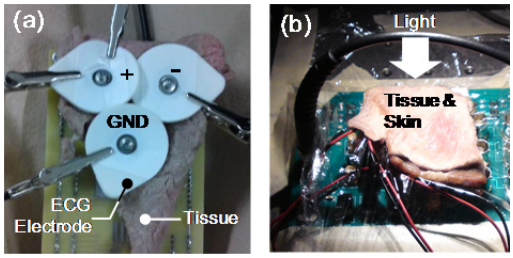

Figure 2: Setups to (a) evaluate subcutaneous-to-surface electrode coupling and (b) in-vitro measurements.

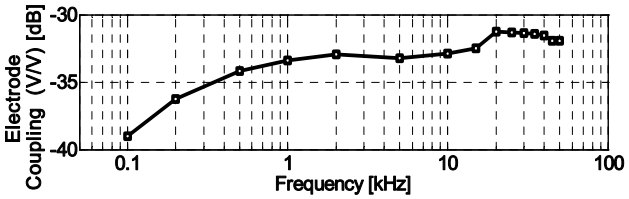

Figure 3: The measured subcutaneous-to-surface coupling factor for the polarized electrodes.

INDUSTRY INTERACTIONS

Texas Instruments, Freescale Semiconductor, and Intel

MAJOR PAPERS/PATENTS

[1] S. Ayazian, V. A. Akhvan, E. Soenen, and A. Hassibi, "A Photovoltaic-Driven and Energy-Autonomous CMOS Implantable Sensor," *IEEE Transactions on Biomedical Circuits and Systems)*, 6-4, pp. 336-343 (2012).

TASK 1836.098, SUB mW WIRELESS TRANSCEIVER FRONTEND FOR BODY AREA NETWORKS

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SIGNIFICANCE AND OBJECTIVES

The standard for Wireless Body Area Networks (WBAN) is slowly coalescing in the form of IEEE 802.15.6. The project will focus on developing a sub mW transceiver frontend to meet the 802.15.6 narrowband specifications from 2360 to 2483MHz.

TECHNICAL APPROACH

Our design approach is to use novel simple architecture which consumes less power, sub-threshold operation, explore optimal partitioning of functions between analog and digital sections, applying injection locking, current reuse techniques to minimize power consumption, partial positive feedback, passive voltage multiplication and dynamic current mode techniques.

SUMMARY OF RESULTS

The overall block diagram of the transceiver is shown in Figure 1. We have taped out the transmitter in IBM 130nm technology which has a MUX based modulator for π/2 DBPSK and π /4 DQPSK. The MUX will have all phases available at its input and based on the message data it will route the appropriate phases. This simple architecture eliminates ADC and mixer in traditional transmitters and consumes less power.

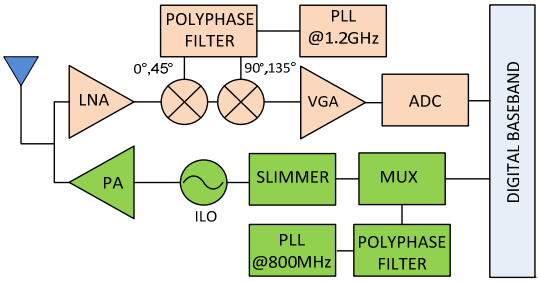

Figure 1: Transceiver architecture

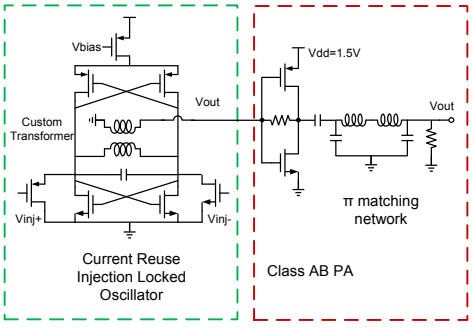

Figure 2: Current reuse ILO inductively coupled to Class AB PA

The PLL runs at 1/3rd the RF frequency subsequently followed by a poly-phase filter which generates all the 8 phases for π/4 DQPSK modulation. A switch based phase MUX selects the proper phase according to baseband data. A pulse slimmer is used to enhance the 3rd harmonic of the selected phase to which the injection locked oscillator locks. As shown in Figure 2 the injection locked oscillator is a current reuse PMOS NMOS oscillator with a transformer load which helps passive differential to single ended conversion. The power amplifier is a single ended self-biased class AB amplifier with a raised VDD of 1.5V. Unlike conventional MUX based architectures, the PLL, poly-phase filter and MUX operate at 1/3rd RF frequency and hence this drastically reduces power consumption. A π matching network is used to match to 50 ohm antenna impedance. The PA has IIP3 of 4.6dBm and ILO has phase noise of -112 dBc/Hz at 1 MHz offset. The power consumption in simulations is 2.1mW which is approximately 3X lesser than the state of the art.

A direct conversion receiver based on quadrature sub-harmonic passive mixing is being designed as shown in Figure 1. The basic idea is to multiply the RF signal by LO and then subsequently by its π/2 shifted replica so that effectively it is multiplying by single LO at twice the frequency. As a result problems of direct conversion like DC offset, LO mixing is solved and the PLL runs at half the RF frequency saving power.

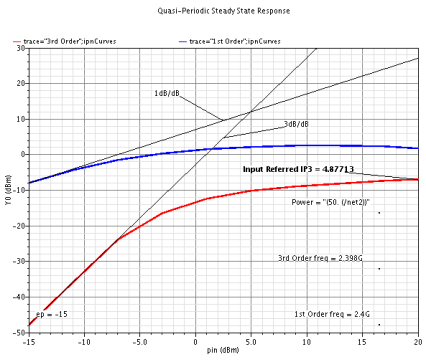

Figure 1: IIP3 of PA shown as 4.8dBm

Keywords: 802.15.6, WBAN, low power RF, sub-threshold RF, injection locked oscillator.

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

TASK 1836.103, RECONFIGURABLE BRAIN COMPUTER INTERFACE

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MIKE CHI, UC-SAN DIEGO & COGNIONICS

SIGNIFICANCE AND OBJECTIVES

The aim is to design a wearable dry contact EEG system that estimates and responds to variations in skin contact impedance across different electrodes as well as motion artifacts in real-time in order to improve the signal to noise ratio (SNR)/enhance signal processing accuracy.

TECHNICAL APPROACH

The common mode rejection of each electrode contact is measured and this information is used in three ways: i) As a metric to compare different designs of dry contact probes ii) As a feedback to a multiplexer to switch on/off fingers on the electrode to improve the contact and iii) As a feedback to a least means squared (LMS) adaptive filter to model motion artifacts and reject them.

SUMMARY OF RESULTS

We evaluated different finger-based dry electrodes that varied the number and arrangement of fingers on the PCB and determined that sparser distributions of fingers showed better contact on average on multiple trials with different subjects due to more effective penetration through hair. We designed, built and validated the operation of an electrode that incorporated a multiplexer to switch on/off fingers. In order to use the feedback signal to reconfigure effectively, the difference in signals across different finger contacts needs to be better understood. To this end, we designed an electrode that collects 8 fingers' data into 8 different channels so that the signals from the fingers can be combined together in the digital domain to simulate different multiplexer combinations for the same time domain data.

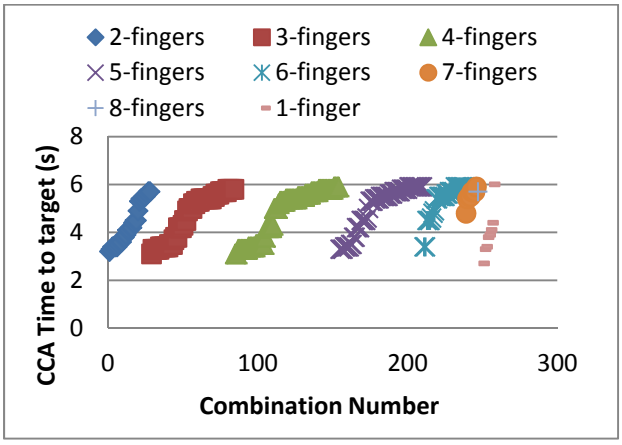


Figure 1: CCA time to target for various finger combinations

Performance in the steady state visually evoked potential (SSVEP) EEG task was used as a metric to compare the SNR of different finger combinations. In general, the SNR is higher if the target frequency observed by the user can be identified faster in time. We used CCA to identify the target frequency and Figure 1 shows the time taken in seconds to recognize the target frequency. It can be observed that even though this is just one electrode placed on one part of the head, the variance in contact between individual fingers leads to significant performance difference. For example, one of the 2-finger combinations needs only 3.2 seconds to identify the target whereas one of the 7-finger combinations due to the influence of fingers with bad contact takes as much as 5.9 seconds. An efficient algorithm to find the best combination is currently being investigated.

For the motion artifact rejection, we are currently working with ECG signals before moving on to EEG signals in future. Any motion is likely to change the contact of the electrode, which in turn will be reflected in the common mode feedback signal. We confirmed that the correlation of the feedback signal with the motion artifact was as high as 0.6 for some movements. This is sufficient for it to be used as a feedback to an LMS adaptive filter to model the motion artifacts and subsequently reject them as shown in Figure 2.

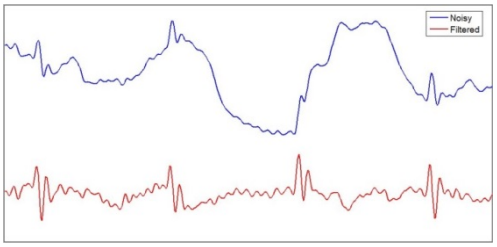


Figure 2: ECG with motion artifacts (shown in blue) and the corrected clean ECG signal (shown in red)

Keywords: Dry EEG, Contact Impedance, BCI, Reconfigurable, Motion Artifact.

INDUSTRY INTERACTIONS

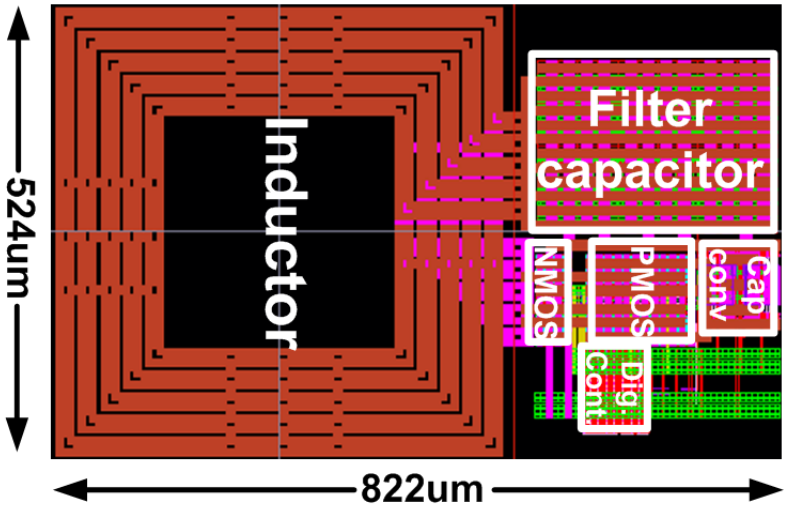
Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] Y. Zou et al., Score-base Adaptive Training for P300 Speller Brain Computer Interface, 2013 IEEE ICASSP.

[2] V. Nathan et al., A 16-channel Bluetooth Enabled Wearable EEG Platform. 2013 ACM Wireless Health.

[3] O. Dehzangi et al., Simultaneous Classification of Motor Imagery and SSVEP EEG Signals, 2013 IEEE Neural Engineering.



A Combined Inductive/Capacitive DC-DC Converter

Summary of Accomplishments

CATEGORY	ACCOMPLISHMENT
Energy Efficiency	An inductive and capacitive combined converter provides efficient regulation over the wide power range demanded by the DVS operation. The converter is fully integrated with passives constructed on chip, using an IBM 32nm SOI process. The converter attains a maximum efficiency of 85.5% in the high power range with the inductive converter operational. The capacitive converter achieves a peak efficiency of 79%. The power density of the entire chip is 8.8W/mm^2. (1836.081, PI: R. Harjani, University of Minnesota) Publication: S. S. Kudva et al., "Fully Integrated Capacitive DC-DC Converter with All Digital Ripple Mitigation Technique," IEEE Journal of Solid State Circuits, August 2013.
Energy Efficiency	The project seeks to operate the link at an energy-efficient supply voltage and leverage the link inactivity periods to reduce the power consumption, with specific focus on fast locking clock generation circuits. A prototype chip demonstrated a 2.5GHz fast power-on clock multiplier, which achieves 10ns power-on time (3 reference cycles). (1836.090, Pavan Kumar Hanumolu, Oregon State University) Publication: T. Anand et al., "A 2.5GHz 2.2mW/25µW On/Off-State Power 2ps$_{rms}$ Long-Term-Jitter Digital Clock Multiplier with 3-Reference-Cycles Power-On Time," 2013 ISSCC, February, 2013, San Francisco, USA.
Energy Efficiency	A hybrid stability margin concept and the associated stability checking method for power distribution networks with integrated linear low-dropout voltage regulators (LDOs) are demonstrated. It employs a localized LDO design methodology that optimizes individual LDOs locally while ensuring the network-level stability. Key circuit level design considerations and trade-offs involved in stability ensuring LDO design have also been investigated. (Task ID 1836.062, Peng Li, Texas A&M University) Publication: S. Lai, B. Yan, P. Li, "Stability assurance and design optimization of large PDNs with multiple on-chip LDOs," IEEE/ACM ICCAD, Nov. 2012 (**Best Paper Award**).

TASK 1836.060, DESIGN TECHNIQUES FOR SCALABLE SUB-1mW/GBPS SERIAL I/O TRANSCEIVERS

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SIGNIFICANCE AND OBJECTIVES

Interface architectures which allow for high data rates at improved power efficiency levels are required to satisfy the growing I/O bandwidth in power-constrained environments. This project aims to improve the power efficiency of serial I/O transceivers to sub 1mW/Gbps for data rates ranging from 5-20Gbps.

TECHNICAL APPROACH

The project utilizes a source-synchronous architecture with ultra-low-power driver, receiver, and clocking circuits that operate over a wide range of supply voltages. The key design techniques developed in this work include:

- Supply-scalable circuits to enable dynamic power management.
- A hybrid voltage-mode driver with low-complexity, high-resolution current-mode equalization.
- High multiplexing factor transmitter and receiver architectures capable of "near-threshold" operation
- Novel injection-locked ring oscillator de-skew with low bandwidth CDR for compensation of thermal drift and multi-phase static timing offsets

SUMMARY OF RESULTS

High-speed serial I/O energy efficiency must improve in order to enable continued scaling of these parallel computing platforms in applications ranging from data centers to smart mobile devices. A low-power forwarded-clock I/O transceiver architecture (Figure 1) was developed which employs a high degree of output/input multiplexing, supply-voltage scaling with data rate, and low-voltage circuit techniques to enable low-power operation. The transmitter utilizes a 4:1 output multiplexing voltage-mode driver along with 4-phase clocking that is efficiently generated from a passive poly-phase filter. The output driver voltage swing is accurately controlled from 100–200mVppd using a low-voltage pseudo-differential regulator that employs a partial negative-resistance load for improved low frequency gain. 1:8 input de-multiplexing is performed at the receiver equalizer output with 8 parallel input samplers clocked from an 8-phase injection-locked oscillator that provides more than 1UI de-skew range. In the transmitter clocking circuitry, per-phase duty-cycle and phase-spacing adjustment is implemented to allow adequate timing margins at low operating voltages. Fabricated in a general purpose 65 nm CMOS process (Figure 2), the transceiver achieves 4.8–8 Gb/s at 0.47–0.66 pJ/b energy efficiency for V_{DD}=0.6–0.8 V [1].

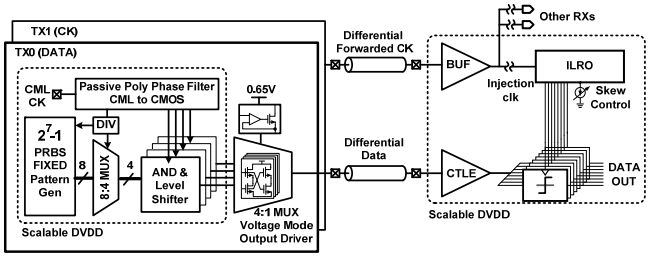
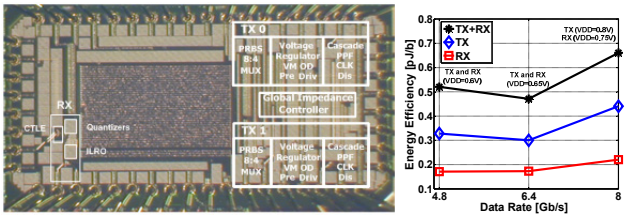


Figure 1: Low-power source synchronous transceiver [1].

The ever-increasing demand for I/O bandwidth not only pushes data-rate, but also energy-efficiency because of total link power budget. However, there is an almost direct trade-off between speed and efficiency. Faster links require more equalization, and all but purely passive equalizers eats rapidly into total power budget once data-rate goes beyond 10Gb/s. Currently under development are power efficient I/O circuit architectures capable of operation at sub-1mW/Gbps in the 16-20Gbps range. These include a low-voltage transmitter with efficient impedance-modulated equalization, a source-synchronous quarter-rate receiver with efficient clocking and on-line phase tracking, and a low-voltage decision-feedback equalizer (DFE) with a novel charge-based latch. Prototypes of these three serial IO modules have been fabricated in a GP 65nm CMOS process, with testing about to begin.



(a) (b)

Figure 2: Low-power source-synchronous transceiver [1]: (a) 65nm CMOS prototype (b) performance summary.

Keywords: High-speed I/O, injection-locked oscillator, transmit equalization, voltage-mode driver.

INDUSTRY INTERACTIONS

Freescale, Intel, Texas Instruments

MAJOR PAPERS/PATENTS

[1] Y.-H. Song et al., "A 0.47-0.66pJ/bit, 4.8-8Gb/s I/O Transceiver in 65nm CMOS," IEEE JSSC, May 2013.

TASK 1836.062, SYSTEM-LEVEL MODELS AND DESIGN OF POWER DELIVERY NETWORKS WITH ON-CHIP VOLTAGE REGULATORS

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SIGNIFICANCE AND OBJECTIVES

The design of power delivery networks (PDNs) is a key avenue and a challenge for achieving power efficiency. We develop simulation tools, models and holistic system design strategies to achieve the optimal system performance trade-offs, and facilitate joint design optimization of active voltage regulators, converters, and passive on-die power grids.

TECHNICAL APPROACH

One of the key focuses of this work is to optimize power delivery by identifying, analyzing and leveraging opportunities that involve with joint optimization of active regulator/converter circuits and passive distribution sub-networks. We are building simulation capability, system-oriented design models, and optimization-based design methodologies to enable efficient design space exploration for large PDNs with multiple integrated voltage regulators. This holistic design approach will shed new insights on interactions between key components of modern power delivery networks and help achieve the best system-level design tradeoffs between supply noise, power efficiency, area overhead and stability.

SUMMARY OF RESULTS

Recently, we have been primarily addressing the stability design challenge for distributed active on-chip voltage regulation, a significant current design trend. Placing multiple voltage regulators onto the die is an effective way for distributed on-chip voltage regulation and provides significant benefits in suppressing various types of supply noise. However, the complex interactions between the active voltage regulators and the large passive sub-network may render the complete power delivery network (PDN) unstable (see for example Figure 1). While traditional stability measures such as phase margin are not applicable to PDNs with a huge number of loops, brute-force analysis of network stability can be impractical due to the huge network complexity.

We present a hybrid stability margin concept and the associated stability checking method for PDNs with integrated linear low-dropout voltage regulators (LDOs). With theoretical rigor, the proposed approach is local in the sense that the stability of the entire network can be efficiently examined through a hybrid stability constraint that is defined locally for individual LDOs (Figure. 2). In the same spirit, we propose a localized LDO design methodology that optimizes individual LDOs locally while ensuring the network-level stability. Key circuit level design considerations and trade-offs involved in stability ensuring LDO design have also been investigated.

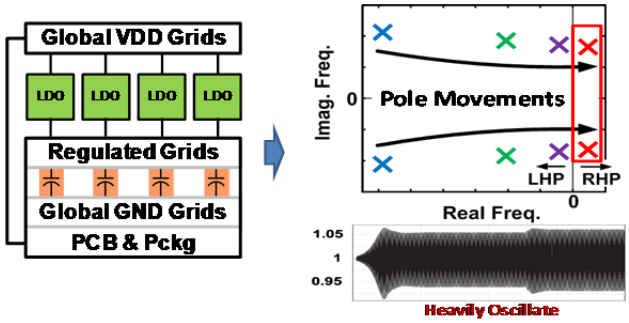

Figure 1: A PDN with distributed LDOs. PDN instability is resulted as an increasing number of LDOs are integrated.

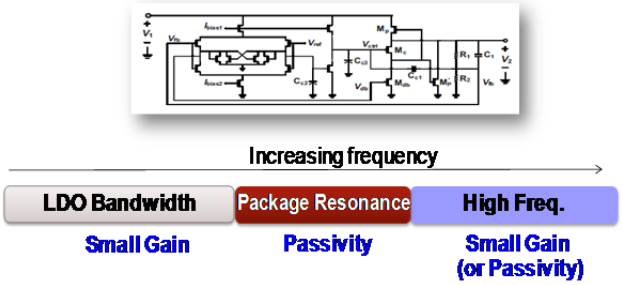

Figure 2: Ensuring stability by hybrid stability: exploiting small gain and passivity across different frequency bands.

Future work will investigate a general stability-centric design methodology.

Keywords: Power delivery, distributed voltage regulation, LDO, hybrid stability, locality.

INDUSTRY INTERACTIONS

Texas Instruments, Intel, AMD, IBM

MAJOR PAPERS/PATENTS

[1] S. Lai, B. Yan, P. Li, "Stability assurance and design optimization of large PDNs with multiple on-chip LDOs," IEEE/ACM ICCAD, Nov. 2012 (**Best Paper Award**).

[2] Z. Zeng, S. Lai and P. Li, "IC power delivery: voltage regulation and conversion, system-level co-optimization and technology implications," ACM TODAS, Mar. 2013.

[3] S. Lai and P. Li, "A power-efficient on-chip linear regulator assisted by switched capacitors for fast transient regulation," IEEE ISQED, Mar. 2013.

TASK 1836.063, POWERLINE COMMUNICATIONS FOR ENABLING SMART GRID APPLICATIONS

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SIGNIFICANCE AND OBJECTIVES

Powerline communication (PLC) systems have been deployed to provide two-way communications between local utilities and smart meters for smart grid applications. Communication performance of PLC systems is limited by non-Gaussian noise. In this project, we aim to improve communication efficiency and reliability of PLC systems in non-Gaussian noise.

TECHNICAL APPROACH

We first study the structure of powerline noise by statistically analyzing and modeling the noise properties in both time and frequency domains, based on several field measurements. We then study transmitter and receiver techniques to improve the communication throughput and reliability in the presence of non-Gaussian noise. We develop real-time PLC testbeds to take noise measurements, and to quantify communication performance vs. complexity tradeoffs of various noise mitigation algorithms.

SUMMARY OF RESULTS

Our field measurements with Aclara and Texas Instruments on outdoor medium-voltage (MV) and low-voltage (LV) power lines have shown that cyclostationary noise is the dominant noise component in the 3--500 kHz band for narrowband PLC (Figure 1). Based on field measurements, we propose a linear periodically varying system model to characterize the temporal and spectral properties of the noise. The proposed noise model has been accepted to IEEE P1901.2 standard.

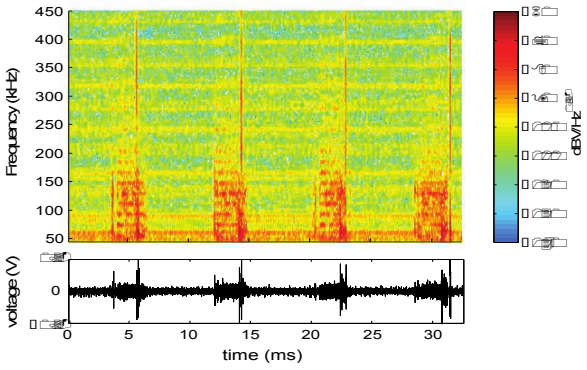

Figure 1: Spectrogram and time-domain trace of powerline noise collected at a LV site near St. Louis, Missouri USA.

To improve the robustness of PLC systems in the presence of cyclostationary noise, we propose noise mitigation algorithms at PLC receivers, which estimate and subtract the noise from received signals. In simulations, our proposed methods have achieved up to 6dB SNR gains over conventional PLC systems (Figure 2).

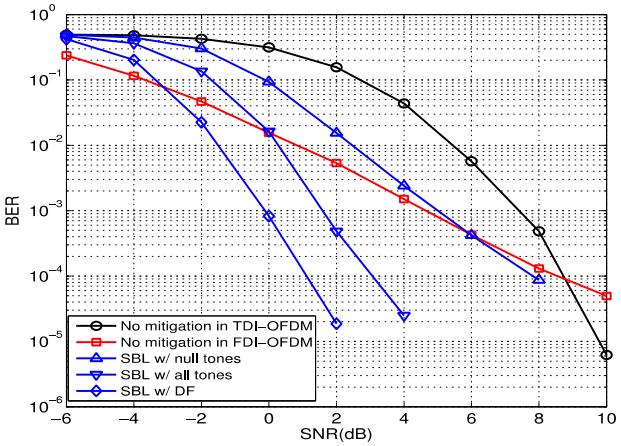

Figure 2: Coded bit error rate (BER) performance of our proposed sparse Bayesian learning (SBL) algorithms in comparison with conventional PLC systems with frequency-domain (FDI) or time-domain (TDI) interleaving.

We have developed three testbeds in the project:

(1) Real-time PLC testbed to evaluate communication performance vs. complexity tradeoffs of various transmitter and receiver algorithms;

(2) Real-time FPGA implementation of a PLC receiver over an impulsive noise channel; and

(3) G3-PLC testbed for powerline noise measurement.

Keywords: powerline communications, smart grid, cyclostationary noise, noise mitigation, testbed

INDUSTRY INTERACTIONS

Texas Instruments, Freescale

MAJOR PAPERS/PATENTS

[1] Lin et al, "Impulsive Noise Mitigation in Powerline Communications Using Sparse Bayesian Learning", *IEEE JSAC,* 2013.

[2] Nassar et al, "Local Utility Powerline Communications in the 3-500 kHz Band: Channel Impairments, Noise, and Standards", *IEEE Signal Processing Magazine,* 2012.

[3] Nieman et al, "FPGA Implementation of a Message-Passing OFDM Receiver for Impulsive Noise Channels", *IEEE Asilomar* 2013.

TASK 1836.068, GLOBAL CONVERGENCE ANALYSIS OF MIXED-SIGNAL SYSTEMS

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SIGNIFICANCE AND OBJECTIVES

Today many modern mixed-signal systems including oscillators, phase-locked loops, and DC-DC converters suffer from fatal start-up failures due to ill-defined initial states, yet their existence is extremely difficult to detect using brute-force simulation approaches. This task aims to find practical tools and methodologies to prevent such global convergence failures (GCF).

TECHNICAL APPROACH

This task seeks practical methods rather than a rigorous mathematic proofing method to establish the global convergence of a general, large-scale mixed-signal system. The task has addressed the problem mainly in two directions: (1) a simulation-based analysis that can detect the existence of global convergence failures; and (2) a methodology that can effectively prevent the occurrence of these failures. For instance, the cluster split detection algorithm looks for an initial state that can lead to a false convergence [1] and the indeterminate state ('X') elimination algorithm guides the designers where to add resets by extending the notion of 'X' in digital to analog circuits [1]-[3].

SUMMARY OF RESULTS

The initial cluster split detection (CSD) algorithm developed in the first and second year had a problem of high computational costs for large mixed-signal systems. Moreover, it is expected that the number of points required would grow exponentially with the space dimension, i.e. the number of circuit nodes, since it tries to explore the initial state space of the circuit with a finite set of randomly chosen points.

However, we devised an algorithm that can significantly reduce the computational complexity of the CSD by merging two close simulation trajectories into one [5]. Also, it is shown that the effective dimensionality of the circuit's state space is much lower than the apparent dimensionality of the state space [4] and the problem size can be reduced by eliminating the circuit state variables that converge to specific values.

Figure 1 shows the evolution of the number of trajectories after merging in case of verifying a phase-locked loop and a DC-DC converter, respectively. It demonstrates that the number drops sharply as the simulation progresses, making the CSD effective for large-scale systems as well. Table 2 lists the execution time of verifying the global convergence of various mixed-signal systems using CSD. Even though the circuit size increases by 4.9× from a DCO to a DC-DC converter, the execution increases only by 9×, which is a much more moderate increase than the expected exponential scaling.

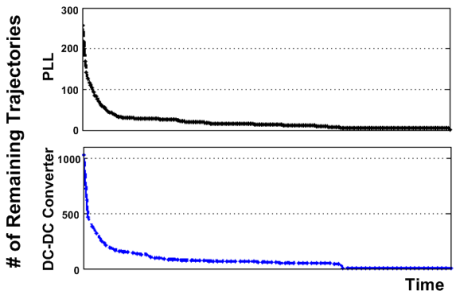

Figure 1. The number of remaining trajectories after merging versus simulation time, in the case of a PLL and DC-DC converter.

	DCO		PLL		DC-DC
	GCF	NO GCF	GCF	NO GCF	No GCF
# of Circuit Nodes	145	145	359	359	3295
# of Initial Sample Trajectories	512	512	512	512	512
# of Clusters Reported	3	1	2	1	1
Total Execution Time	36.1 min	73.2 min	49.3 min	3.1 hour	14.9 hour

Table 2. Performance summary in verifying the global convergence property of digitally-controlled oscillators, phase locked loops and a DC-DC converter using the proposed CSD algorithm.

Keywords: global convergence, start-up failures, mixed-signal systems, circuit simulation, formal analysis.

INDUSTRY INTERACTIONS

Texas Instruments, Inc. and Intel Corporation.

MAJOR PAPERS/PATENTS

[1] S. Youn, J. Kim, M. Horowitz, "Global Convergence Analysis of Mixed-Signal Systems," ACM/IEEE Design Automation Conference (DAC), June 2011.

[2] S. Youn, J. Kim, M. Horowitz, "Preventing Global Convergence Failures in Mixed-Signal Systems by Eliminating Indeterminate States," Frontiers in Analog Circuit Synthesis and Verification (FAC), July 2011.

[3] S. Youn and J. Kim, "Preventing Global Convergence Failures in Mixed-Signal Systems via Indeterminate State ('X') Elimination," to be published, IEEE Trans. Circuits and Systems-I, 2013.

[4] S. Youn and J. Kim, "Establishing Global Convergence for Mixed-Signal Systems," SRC TECHCON, Sept. 2013.

[5] S. Youn and J. Kim, "Global Convergence Analysis in Mixed-Signal Systems via Cluster-Split Detection," in preparation, IEEE Trans. Circuits and Systems-I, 2013.

TASK 1836.069, ELECTRONIC SYSTEMS FOR SMALL SCALE WIND TURBINES

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DANILO LLANO, UNIVERSITY OF CAMBRIDGE, DXL20@CAM.AC.UK

SIGNIFICANCE AND OBJECTIVES

This project looks at the electrical system of small-scale wind turbines of power ratings up to 5 kW, with the aim of reducing the cost of this electronics, chiefly by eliminating sensors and replacing them with more advanced control. Advance control will also increase the reliability of the whole system.

TECHNICAL APPROACH

Advanced control has been proposed to achieve maximum extraction of the power generated by generators driven by small-scale wind turbines. The power extraction is done by controlling the speed of a permanent magnet synchronous generator (PMSG). The output from the generator is rectified with a Voltage Source Inverter (VSI) onto a fixed voltage DC link, potentially offering a low cost solution with adaptable control possibilities. The VSI was designed and tested to offer a low cost and compact design. At the same time, Fuzzy logic, Port-Controlled Hamiltonian, PI and Sliding Mode controllers have been experimented to control the PMSG.

SUMMARY OF RESULTS

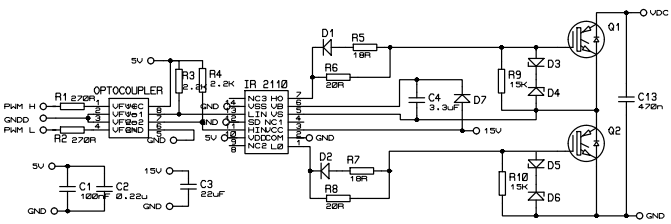
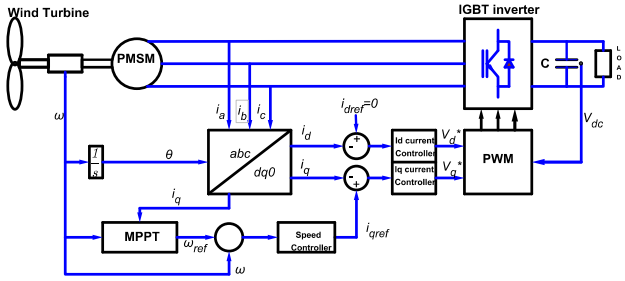


Figure 1: The architecture of one leg of the designed VSI.

A low cost VSI was designed and tested at the laboratory in addition to the previously reported emulator test rig. IGBTs rated at 600V and 30A were used as switching



The basic structure to control the generator is presented in Figure 2. The current I_d is set to zero and the current I_q depends on the speed reference. In the case of fuzzy logic, sliding mode and Port-Controlled Hamiltonian controllers the I_q control is not required. The speed control regulates the I_q current as well. By controlling the speed it is possible to control the power extracted from the wind turbine. In this stage the control techniques will be based on a position sensor.

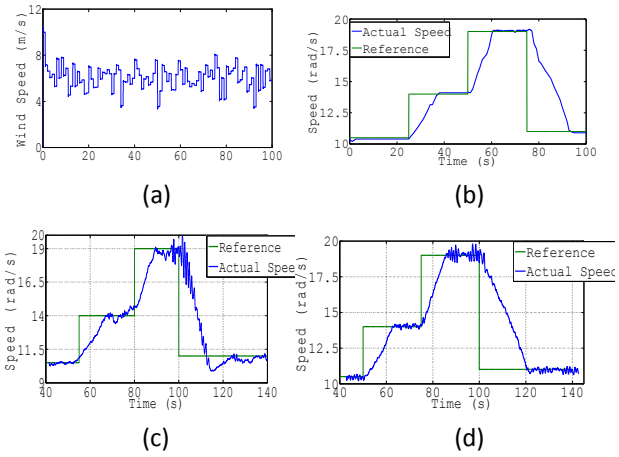


Figure 3: (a) Wind profile used for simulation and experiments. (b) Speed by using sliding mode control (simulation). (c) Speed by using Fuzzy control (experimental) (d) Speed by using sliding mode control (experimental).

Simulations in Simulink and experiments in the emulator test rig were carried out. The main aim of the simulations and experiments was to verify that the designed controllers could track a speed reference even under gusty wind conditions. In Figure 3 the speed responses show a large rise time. It is not possible to reduce this rise time because it is limited by the large inertia of the wind turbine (20kgm^2) and the uncontrolled wind torque.

Later, the sensorless control and grid integration of the system will be explored. Also, minimum cost implementations of the sensorless control schemes will be looked at.

Keywords: PMSG, VSI, fuzzy logic, Port-Controlled Hamiltonian, small wind

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

TASK 1836.070, OPTIMUM CONTROL OF POWER CONVERTERS

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SIGNIFICANCE AND OBJECTIVES

The main target is to adopt an accurate model for a Flyback converter and based on which proposes an all-digital control solution that is capable of being implemented within a microcontroller. In addition to system stability, other control issues, such as efficiency maximization and robust performance, would also be addressed.

TECHNICAL APPROACH

Two major steps, consisting of converter modeling and control design, are carried out one after another. The first stage focuses on experimentally determining and verifying Flyback transformer model by means of system identification approach. Both linear and nonlinear behavior of the transformer are taken into account and integrated into a single model. In the second phase, a primary side regulation (PSR) technique is adapted to fit with the digital implementation and to be less prone to system variations. Three control techniques, i.e. robust compensator, adaptive compensator and digital PI compensator, are applied to the PSR Flyback converter. Results are verified with C200 microcontroller.

SUMMARY OF RESULTS

Transformer modeling has been investigated intensively. However, most of the studies focus either on identifying the high frequency winding model with linear core assumption or on modeling nonlinear properties of a specific magnetic material. Therefore, our approach presented in [1], subsequently extended in [2], is the only one tries to integrate both nonlinearity and winding effect in to a unified model, as illustrated in Fig. 1, and estimate the model parameter using the experimental data and time-domain system identification.

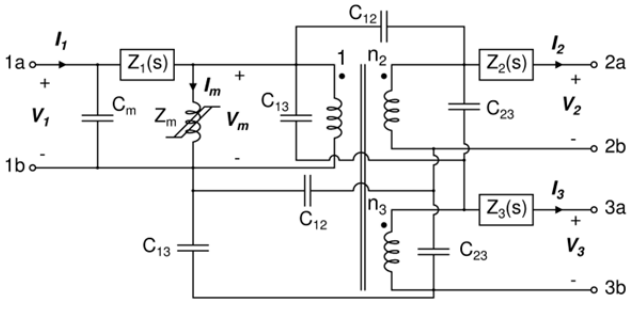

Figure 1: Nonlinear dynamic model of 3-winding Flyback transformer which is capable of reproducing both magnitude and frequency nonlinearity

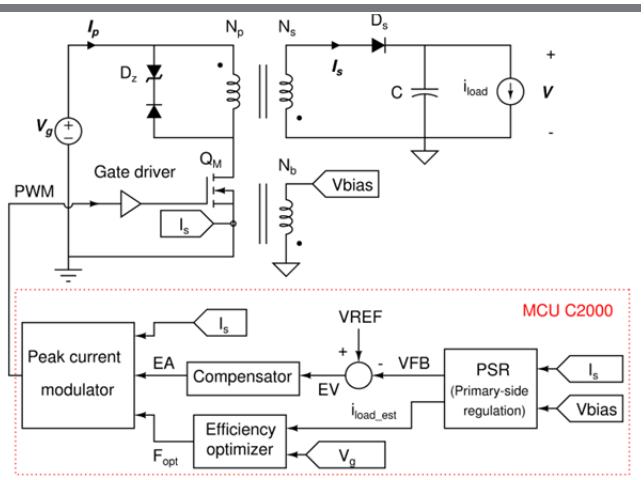

Figure 2: Proposed all-digital control for a Flyback converter. The PSR block is a modified version of the method in [3], while the compensator would be designed to achieve both robust stability and performance at all operating conditions.

While continuous-time control for Flyback converter is well known, a digital counterpart is not fully considered. Therefore we proposed a digital control structured as plotted in Fig. 2. The PSR scheme, which is suggested in [3] to cope with a wide operating range, would be modified and implemented as the PSR block in Fig. 2. Some future works consist of (a) comparing the performance, stability and complexity of three different control methods, (b) implementing the proposal in C2000

Keywords: Primary side regulation, digital control, Flyback converter, transformer model, system identification

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] T. T. Vu, S. O'Driscol, and J. V. Ringwood, "3-winding Flyback transformer model extraction using time-domain system identification", Proc. IEEE SPEEDAM, pp. 458-463, Jun. 2012

[2] T. T. Vu, S. O'Driscol, and J. V. Ringwood, "Nonlinear dynamic transformer time-domain identification for power converter application", IEEE Trans. on Power Electron., vol. 29, no. 1, pp. 318 – 327, Jan. 2014

[3] T. T. Vu, S. O'Driscol, and J. V. Ringwood, "Primary-side sensing for a Flyback converter in both continuous and discontinuous conduction mode", Proc. Irish Signal and System conference, Maynooth, June 2012

TASK 1836.076, ULTRA-LOW POWER DELAY-INSENSITIVE ASYNCHRONOUS CIRCUITS

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SCOTT SMITH AND H. ALAN MANTOOTH, UNIVERSITY OF ARKANSAS

SIGNIFICANCE AND OBJECTIVES

This project will evaluate the integration of MTCMOS power gating with delay-insensitive asynchronous logic for reducing energy consumption in both active and standby modes, as well as explore the ultra-low voltage asynchronous circuit design opportunity.

TECHNICAL APPROACH

Since the spacer cycle of a dual-rail delay-insensitive asynchronous component is equivalent to gating the power of this component and forcing the output to logic 0, these circuits can enter sleep mode after every data cycle, while the circuit is in operation, and the handshaking signals between registers can be used as sleep control signals to control the power gating transistors. This approach has several merits: 1) limiting leakage in both active and sleep modes; 2) alleviating the effort and complexity of designing the sleep signal generation mechanism; 3) reducing the area overhead; and 4) facilitating the tool flow development.

SUMMARY OF RESULTS

Delay-insensitive asynchronous logic like the NULL Convention Logic (NCL) utilizes dual-rail encoding to achieve delay-insensitivity. A NCL system consists of delay-insensitive combinational logic sandwiched between NCL registers, which use handshaking signals to coordinate circuit behavior. NCL circuits are comprised of 27 threshold gates and MTCMOS power gating structure is implemented inside each threshold gate. In order to maintain delay-insensitivity and maximize leakage saving, a series of innovations including early-completion detection, sleep-enabled register and completion detection unit design, have been applied. Incorporating MTCMOS power gating mechanism in NCL (denoted as MTNCL) has the potential to result in significant savings in energy consumption without large overhead in area.

Two AES cores have been designed in MTNCL and synchronous, respectively, using IBM 130nm 8RF-DM process. Both cores follow the same architecture where as many components are reused between encryption and decryption as possible. The top-view of the MTNCL AES core is shown in Fig. 1. Both cores are capable of performing 128-bit key encryption and decryption. The synchronous design was synthesized using IBM regular-V_t standard cell library under a timing constraint that is the same as the speed of MTNCL design, which is 150MHz. Corner cases were considered during synthesis. I/O shifting logic was inserted to reduce the number of pins required. The chip was fabricated at MOSIS.

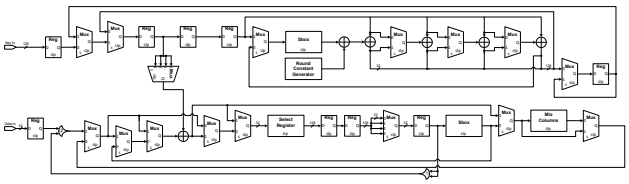

Figure 1: Top-view of the MTNCL AES core.

Table 1 shows the area comparison between the two cores. Due to the elimination of input-completeness requirement, the MTNCL design is even smaller than the synchronous counterpart.

Table 1: Area Comparison between Two AES Cores

	Sync.	MTNCL	MTNCL Saving %
Gate Count	5,462	11,022	
Total Transistor Width (μm)	51,181	34,279	33%
Layout Area (μm^2)	272,644	252,996	7%

Table 2 shows the active energy per operation comparison. Since there is a leakage problem with the I/O pads, leakage measurements are so high that they mask active energy. The numbers shown in Table 2 were calculated by subtracting leakage from total energy measured. MTNCL shows savings in both encryption and description. Another test vehicle, a MTNCL MSP430, is being designed to be fabricated for the next year.

Table 2: Active Energy per Op Comparison

	Sync.	MTNCL	MTNCL Saving %
Encryption (nJ)	0.446	0.305	31.6%
Decryption (nJ)	0.679	0.263	61.3%

Keywords: MTCMOS, delay-insensitive, asynchronous, ultra-low power, CAD tool

INDUSTRY INTERACTIONS

Texas Instruments, Intel, AMD

MAJOR PAPERS/PATENTS

[1] M. Hinds et al., "An Asynchronous Advanced Encryption Standard Core Design for Energy Efficiency," accepted to Journal of Low Power Electronics.

[2] B. Sparkman et al., "An Asynchronous AES Core Design for Low Power," accepted to 2013 SRC TechCon.

TASK 1836.081, COMBINED INDUCTIVE/CAPACITIVE DC-DC CONVERTER FOR EFFICIENT DYNAMIC VOLTAGE SCALING

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SIGNIFICANCE AND OBJECTIVES

Dynamic voltage scaling (DVS) is one of the techniques used to tackle increased power dissipation problem in integrated systems. Our aim is to not only build efficient voltage regulators to support DVS over a wide power range but also make them fully integrated to support multiple independent DVS domains.

TECHNICAL APPROACH

We employ a combine the inductive and capacitive converter to provide efficient regulation over the wide power range demanded by the DVS operation. The inductive converter with digital pulse width modulation based control supports the higher output power and the capacitive converter with single bound hysteretic control supports the lower power range. A controller selects the appropriate converter based on the operating condition.

The converter is fully integrated with passives constructed on chip. A 2nH stacked inductor was custom designed in top two metal layers of the interconnect stack and the filter capacitor built using the deep trench capacitors.

SUMMARY OF RESULTS

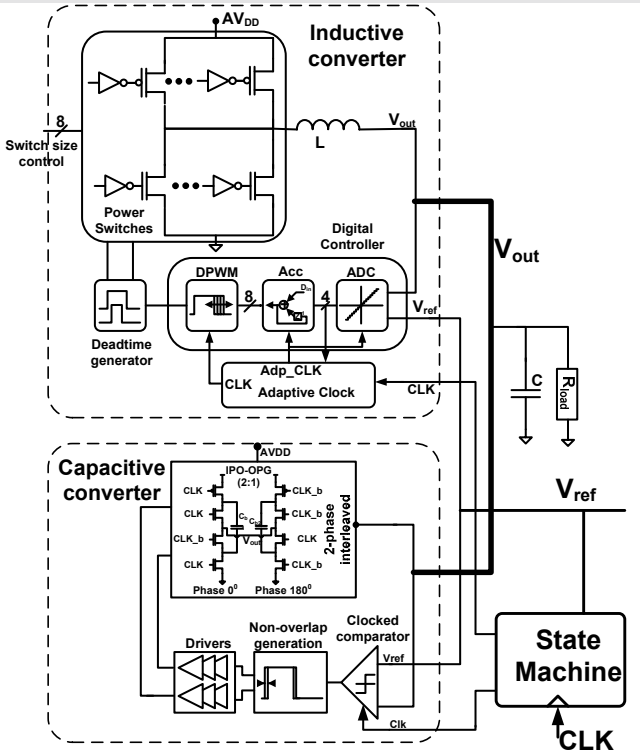

Figure 1: Combined inductive/capacitive converter

The combined inductive/capacitive converter shown in Figure 1 was taped out in IBM 32nm SOI process. (Currently being tested) The converter supplies a maximum power of 300mW and occupies a total area of 0.43mm^2. The inductor occupies 70% of the area of the converter. By re-using the area underneath the inductor, by placing digital circuits we attain a power density of 8.8W/mm^2.

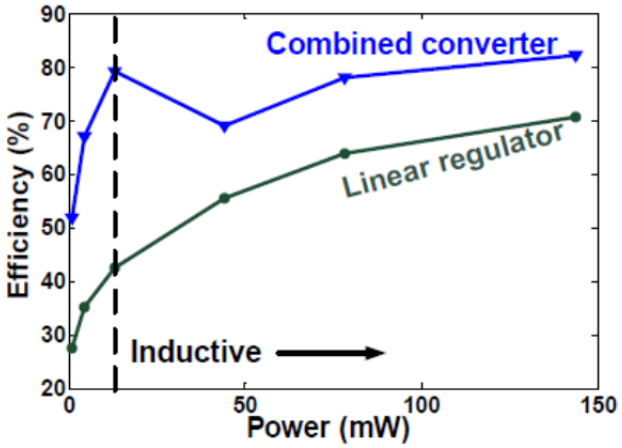

Figure 2: Efficiency of the converter stressed using a DVS type load profile

The converter attains a maximum efficiency of 85.5% in the high power range with the inductive converter operational. The capacitive converter achieves a peak efficiency of 79%. Figure 2 shows the efficiency of the converter, when it is stressed using a DVS type load. Our converter achieves higher efficiency than the theoretical efficiency of a linear regulator for same loading profile.

Keywords: Dynamic Voltage scaling, fully integrated converter, combined inductive /capacitive converter, stacked inductor

INDUSTRY INTERACTIONS

Intel, Freescale semiconductor, IBM

MAJOR PAPERS/PATENTS

[1] J. Wibben et al., "A High Efficiency DC-DC Converter Using 2nH Integrated Inductors," IEEE Journal of Solid State Circuits, April, 2008.

[2] S. S. Kudva et al., "Fully Integrated On-Chip DC-DC Converter with a 450x Output Range," (Invited) IEEE Journal of Solid State Circuits, August 2011.

[2] S. S. Kudva et al., "Fully Integrated Capacitive DC-DC Converter with All Digital Ripple Mitigation Technique," (Invited) IEEE Journal of Solid State Circuits, August 2013.

TASK 1836.090, DIGITALLY-ENHANCED CLOCKING STRATEGIES TO IMPROVE ENERGY-EFFICIENCY OF SERIAL LINKS

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SIGNIFICANCE AND OBJECTIVES

The goal of the proposed research is to explore and invent techniques to improve the energy efficiency of serial links by an order of magnitude. Specifically, this research will focus on co-designing system-level power management schemes with digitally-enhanced clocking circuit architectures to simultaneously achieve low-power operation and robustness to process variability, leakage, and low supply voltage.

TECHNICAL APPROACH

The technical approach is based on operating the link at an energy-efficient supply voltage and leveraging the link inactivity periods to reduce the power consumption. The specific focus of this effort would be the design of fast locking clock generation circuits. To this end, we seek to employ highly digital circuit architectures that leverage self-calibration to speed up the lock time. In one possible approach the oscillator tuning characteristic is determined and upon power up, appropriate control word is loaded into the oscillator, thus acquiring instantaneous frequency lock.

SUMMARY OF RESULTS

Phase acquisition time of a phase-locked loop (PLL) is limited by their loop bandwidth which is typically restricted to one-tenth of the reference frequency. Multiplying injection locked oscillators (MILO) has inherent limitation which trades locking time with spurs at the output. Multiplying delayed locked loop (MDLL) based multipliers can achieve fast locking with excellent jitter performance (Fig. 1). During power-off the frequency information is stored in the accumulators. During power-on, the frequency of VCO is rapidly restored using Nyquist DACs in the coarse integral path which brings the oscillator to a coarse frequency lock, and fine integral path which brings the oscillator to the desired frequency. The proportional path consisting of edge replacement logic passes a clean reference edge every reference cycle and achieves instantaneous phase lock. At 2.5GHz, the multiplier turns-on in 10ns (Fig. 2,3).

In the following year we seek to further investigate fast power-on transmitters including voltage mode drivers and strive to implement a prototype test chip in a deep sub-micron CMOS process.

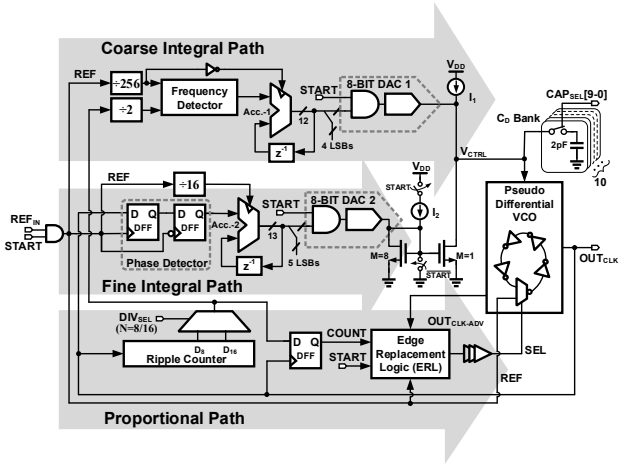

Figure 1: 2.5GHz fast power-on clock multiplier.

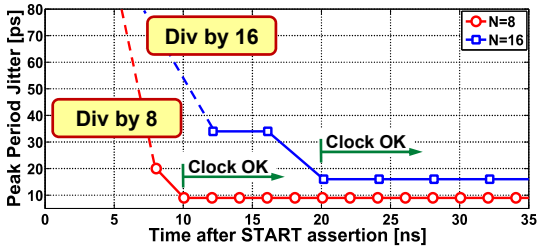

Figure 2: Measured settling time for divide by 8 and 16.

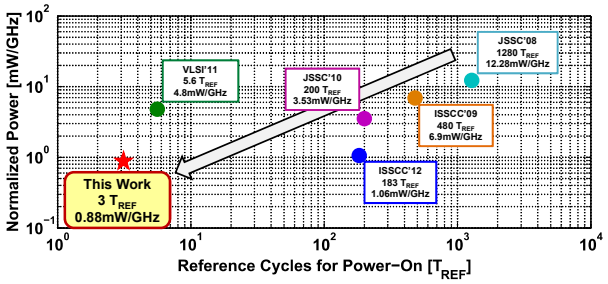

Figure 3: Comparison with other clock multipliers

Keywords: fast frequency locking, MDLL, PLL, FLL

INDUSTRY INTERACTIONS

IBM, Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] T. Anand et al., "A 2.5GHz 2.2mW/25µW On/Off-State Power 2ps$_{rms}$ Long-Term-Jitter Digital Clock Multiplier with 3-Reference-Cycles Power-On Time," 2013 ISSCC, February, 2013, San Francisco, USA.

TASK 1836.099, BEHAVIORAL MODELING OF SWITCHING CONVERTERS

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SIGNIFICANCE AND OBJECTIVES

Simulating switching power converters at the transistor level or with transient models is very time consuming. Development of more complex electronic products requires faster models. The objective of this project is to create a method of model creation that reduces modeling efforts to only a few hours or less and simulation time by multiple orders of magnitude.

TECHNICAL APPROACH

Switching circuits, such as many common power converter topologies, can take a very long time for SPICE-like simulators to simulate due to the many simulation steps introduced by the switches. A well-established solution to this problem is to use an *averaged model* approach in which the switching element is averaged over time and thereby linearized. This allows simulation to be performed much more quickly (seconds versus hours or days). The developed modeling method is unique in that an averaged model can be easily generated from either a data sheet, measured data or simulated netlist in a reasonable amount of time.

SUMMARY OF RESULTS

Both voltage and current mode control PWM averaged models have been developed in Verilog-A and PSpice.

A thorough investigation into methods to improve the accuracy of PWM switch averaged models up to the Nyquist frequency is the subject of current work.

A series of models have been developed for commercial circuits. Figs. 1-3 show the model structure and performance comparisons for a Texas Instruments TPS54320 current mode controlled buck converter.

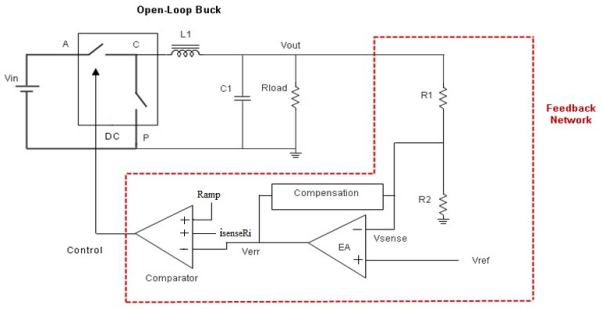

Figure 1: The model structure of the TI TPS54320 obtained using a PWM switch averaged model.

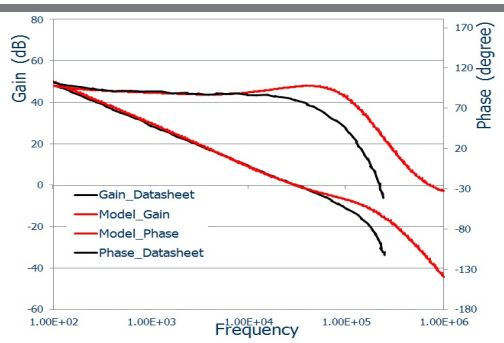

Figure 2: AC response comparison of the TPS54320, with model in red and circuit in black.

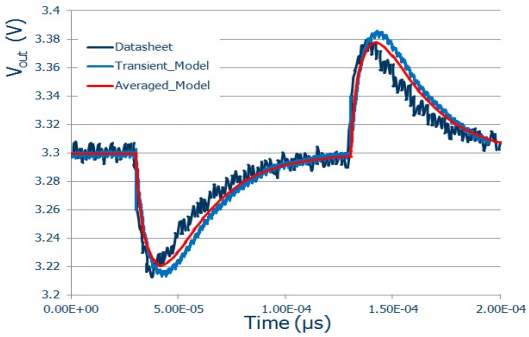

Figure 3: Transient response comparison of the TI TPS54320.

Table 1: Simulation Time Comparison (1 ms transient setup)

	Circuit	Transient Model	Averaged Model	Improvement
CPU Time	N/A	370 s	0.1 s	3700 X

Transient error of less than 1% can be achieved by using PWM switch averaged model. AC performance up to half of the switching frequency still needs to be improved. The simulation speed comparison in Table 1 shows three orders of magnitude time reduction compared with transient model.

A Regulator Model Generator tool has been built which can generate converter models in both PSpice and Verilog-A format.

Keywords: Behavioral modeling, switching converter, CAD, Averaged model

INDUSTRY INTERACTIONS

Noam Teutsch, Sara Rogers, TI; Mukesh Ranjan, Intel

MAJOR PAPERS/PATENTS

[1] R. Mao, M. Leonard, M. Francis, Alan Mantooth, "Semi-Automatic Generation of PWM Switch Averaged Models for Switching Regulators," Accepted to *TechCon*, Austin, TX, 2013.

TASK 1836.104, FAULT TOLERANT INVERTER MODULE FOR DSSRM DRIVE

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SIGNIFICANCE AND OBJECTIVES

The motivation behind this task is to engineer a solution for stationary placement of power switches in power converters which can allow for a dynamic circuit topology thereby elevating the size, cost, and complexity issues associated with current technology. The dynamic relocation is attained through piezoelectric (PE) actuation which will generate new opportunities in effective thermal management and reduced part converter topologies for substantial saving in developmental cost and the required footprint.

TECHNICAL APPROACH

A four phase converter is used for a case study, where current in each coil is controlled by one individual asymmetric bridge. Fig.1 shows the proposed model of a PE actuator with the same purpose. The actuator consists of a central fixed copper contact head and four peripheral movable copper contact heads. Each peripheral contact head is bonded to a PE bimorph beam. Upon being actuated, PE bimorphs experience deflection via inverse piezoelectric effect and A physical contact can be created between central and peripheral contact heads to complete the circuit for the corresponding phase. Each beam can be controlled via voltage activation. The model was simulated in ANSYS software using finite element method for simulations.

SUMMARY OF RESULTS

Finite element method of the simplified PE actuator was applied for modal analysis, static analysis, and transient analysis.

First, modal analysis was performed to retrieve the natural frequencies and different modes of operation. With an intention to operate in non-resonant mode, natural frequencies were avoided and deflection direction was matched with the fundamental mode of vibration of the beam to maximize the desired deflection.

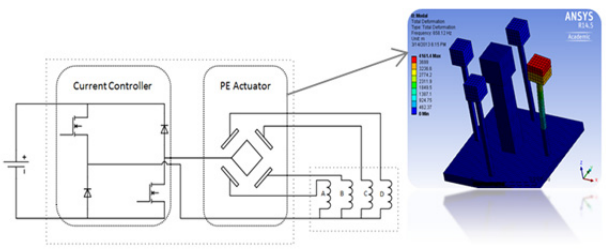

Figure 1: Converter with Piezoelectric Actuator Model.

Moreover, blocked force and tip deflection are two very important parameters determined through static analysis. The blocked force results in deflection upon movement being allowed. The maximum attainable deflection determines the gap that can be maintained between the two copper contact heads, hence, governs the amount blocking voltage that can be safely maintained when the copper heads are not in contact. For the actuating PE beam depicted.

In addition, transience time is another parameter of interest for the design of the actuator. Considering non-resonant mode operation, for every actuating pulse signal, the time taken by the actuating PE beam to attain steady state deflection determines the speed of the system (Actuation time).

Finally, the design limitations observed from FEA analyses are: power transfer capacity – determined by total deflection and size, and actuation time. Realizing the geometric dependence of these parameters, optimal point of operation was determined by observing the effect of modification of each geometrical dimension. Table 1 displays the optimized measured parameters for the PE actuator model.

Table 1: Parameters of optimized PE actuator model

Deflection (um)	Actuation Time (ms)	Conduction Current (A)	Blocking Voltage (V)
37.085	8.4	6.2	111.26

In conclusion, a new dynamic actuating topology is introduced to eliminate the redundancy from the conventional converter topologies, resulting in increase of size and cost efficiency. Exploiting the piezoelectric properties of the piezoelectric crystals, an electromechanical system is designed to create such dynamic switching effects. Power limitation with decreasing size and speed limitation with increasing size creates a tradeoff between attainable power transfer and frequency of operation. A test bed of the proposed model will be built and tested in future.

Keywords: Piezoelectric, Power Converters, DSSRM, Actuation Time, Deflection

MAJOR PAPERS/PATENTS

[1] Vasic, D.; Costa, F.; Sarraute, E., "A new MOSFET & IGBT gate drive insulated by a piezoelectric transformer," Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual , vol.3, no., pp.1479,1484 vol. 3, 2001 ???????

TASK 1836.105, CR-FREE SIMO DC-DC POWER CONVERTERS WITH NANO-SECOND LOAD TRANSIENT RESPONSE

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SIGNIFICANCE AND OBJECTIVES

The output voltage ripple of modern switching power converters is desired to be low in high-performance systems. Meanwhile, the load transient response and dynamic voltage scaling (DVS) tracking speed are expected to be fast. A switching converter with both improved steady-state and dynamic performances is highly demanded.

TECHNICAL APPROACH

By using adaptive current compensation (ACC) technique, both the load transient response and DVS tracking speed of switching power converter can be significantly improved without increasing the switching frequency or reducing the filtering inductance. The proposed control method obviates large ESR for filtering capacitor. Therefore, the low output voltage ripple can be achieved simultaneously. The switching frequency is also stabilized to avoid generating randomized switching noise spectrum. Moreover, the high power efficiency is maintained since the load current is dominated by the output current of switching converter in steady state.

SUMMARY OF RESULTS

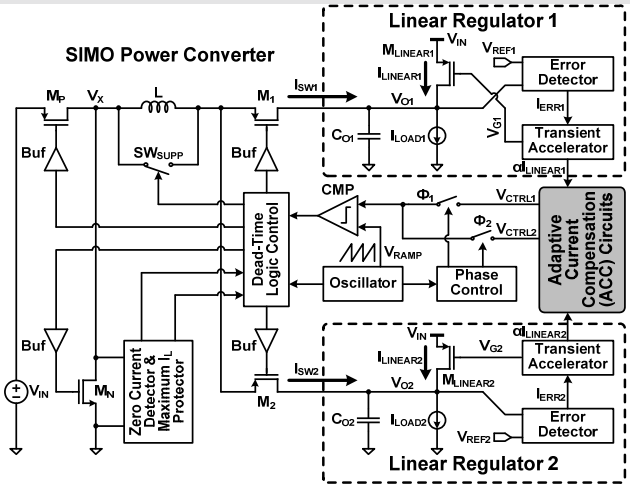

Figure 1: System block diagram of the proposed analog SIMO power converter.

Slow load transient response and potential cross-regulation effect are two major performance barriers for single-inductor multiple-output (SIMO) power converters. To overcome these barriers, this project proposes a parallel-structured hybrid SIMO power converter with an adaptive current compensation (ACC) technique, as illustrated in Fig. 1. With the employment of new and compact linear regulators, the proposed ACC technique improves both the step-up/down transient responses significantly without the needs on advanced controls or high switching frequency. The interactive duty ratio changes between sub-converters are also avoided due to the fast recovery during load transition periods. Cross-regulation effect is thus minimized.

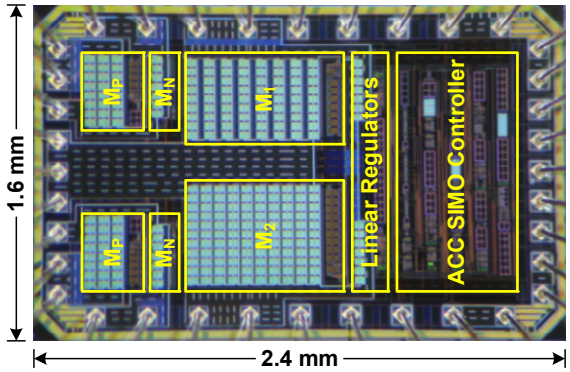

Figure 2: Chip Micrograph.

The proposed hybrid SIMO converter is fabricated with a 0.35-µm CMOS process. The chip micrograph is shown in Fig. 2 with an active die area of 2.24 mm^2. The power transistors M_P and M_N are split and placed symmetrically for easy routing and better power current balancing. The input voltage is 3 V. The two output voltages are regulated at 1.8V and 1.2V, respectively. The inductor value is 1 µH, while the two filtering capacitors are both 22 µF. Each sub-converter is capable of delivering 100-mA load current. Due to the proposed ACC technique, both the step-up/down load transient responses have been improved. For the step-up load change, when the load currents of both sub-converters switch from 10 to 100 mA, the maximum undershoot voltages are 15 mV and 9.8 mV respectively. Both of the outputs recover within 50.3 ns. For the step-down load change, on the other hand, the maximum overshoot voltages of 32.9 mV and 23.3 mV are measured, when the load currents quickly drop from 100 to 10 mA. It takes 7.5 µs and 8.8 µs for the sub-converters to recover.

Keywords: adaptive current compensation, SIMO converter, cross regulation, fast transient response

INDUSTRY INTERACTIONS

TI, Intel, AMD

MAJOR PAPERS/PATENTS

[1] Y. Zhang, D. Ma, “A fast-response hybrid SIMO power converter with ACC and Minimized CR,” submitted to IEEE JSSC.

TASK 1836.106, IF-SAMPLING CMOS ADC FRONT-END

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SIGNIFICANCE AND OBJECTIVES

For IF-sampling applications, the front-end sampler is traditionally designed with bipolar transistors and high supply voltages, which make the integration of the front-end circuits a challenging task in scaled CMOS technologies with low supply voltage. We propose a digital calibration technique to linearize the front-end circuits of IF-sampling ADCs.

TECHNICAL APPROACH

In order to linearize a sample-and-hold (S/H) circuit for IF-sampling, a complete derivative error model is developed to address the odd-order and even-order harmonic distortions stemming from the tracking nonlinearity of the sampling switch. The proposed error model is tested and verified by calibrating a simulated S/H circuit in TI 65-nm technology and a 16-bit ADC evaluation board.

SUMMARY OF RESULTS

Dynamic nonlinearity is dominant at high frequencies for CMOS S/H circuits, which is mainly due to the nonlinear switch resistance. The switch resistance of a traditional bootstrap architecture (shown in the Figure 1) is

$$R_{on} = 1\Big/\mu C_{ox}\frac{W}{L}\left(V_{gs}-V_{th}-\frac{1}{2}V_{ds}\right) \quad (1)$$

The traditional bootstrap circuit always bootstraps between the input node and the gate of the sampling switch. Meanwhile, the current direction is constantly varying during the tracking phase. Because of this, the drain and the source of the sampling switch regularly swap positions between the input and the output nodes. This differentiates the analysis into two cases shown in Figure 1. Based on the above understanding, we derived a derivative error model capturing the dynamic nonlinearity of the sampling switch for both cases as

$$V_{in} = V_{out} + \tau_0\frac{dV_{out}}{dt} + \tau_1\left|\frac{dV_{out}}{dt}\right|\frac{dV_{out}}{dt} + \tau_2\left(\frac{dV_{out}}{dt}\right)^2 + \tau_3\left|\frac{dV_{out}}{dt}\right| \quad (2)$$

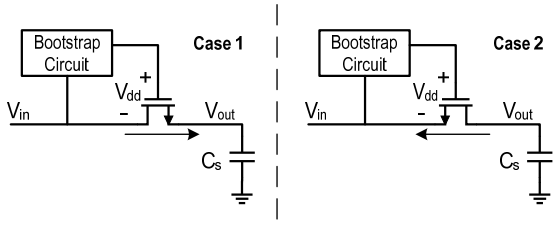

Figure 1: Two cases of the sampling switch in tracking phase

An S/H circuit using TI 65-nm technology is simulated and calibrated with the proposed model. The input frequency is as high as 407 MHz and the SFDR is improved by over 40 dB. The sample rate is 100 MHz.

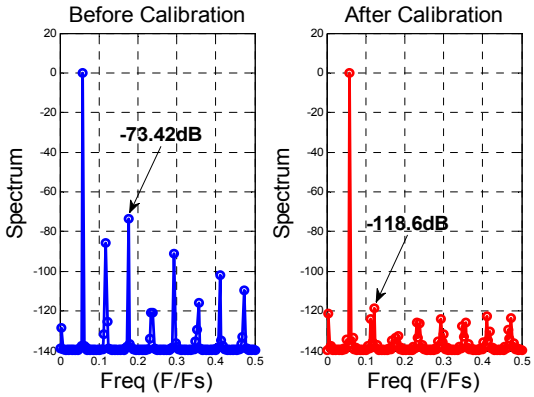

Figure 2: Simulation result of nonlinearity calibration

Secondly, a 16-bit AD9268 CMOS ADC evaluation board is measured and calibrated with the proposed model. The input frequency shown in Figure 3 is 206 MHz and the SFDR is improved by over 20 dB. The sample rate is 70 MHz.

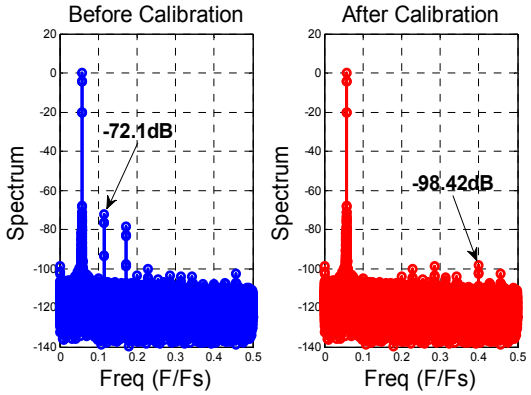

Figure 3: Measurement result of nonlinearity calibration

In the following year, we will investigate the validity of the proposed technique further with custom-designed CMOS S/H circuits and test structures to verify our calibration model and the potential effectiveness of the proposed technique.

Keywords: IF-sampling, digital calibration, sample-and-hold, input buffer, split-ADC, offset double conversion

INDUSTRY INTERACTIONS

Texas Instruments

TASK 1836.110, DISTRIBUTED POWER DELIVERY ARCHITECTURE FOR 2D AND 3D INTEGRATED CIRCUITS

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SIGNIFICANCE AND OBJECTIVES

The primary objective is to design a low-loss, fully integrated, and robust distributed Power Delivery Unit for multicore processors targeting low output voltage from relatively high input voltage. The central innovation is a hybrid down conversion architecture composed of a central switched capacitor (SC) converter and multiple distributed inductive buck (IB) converter.

TECHNICAL APPROACH

The hybrid architecture combines the advantages of SC and IB providing following benefits for large down conversion factor: (i) reduced voltage stress across the power FETs compared to a single IB helping integrated DC-DC conversion; (ii) faster response and tighter output regulation compared to a single SC; and (iii) potential for better efficiency compared to a single stage (SC or IB) converter delivering same output voltage/current as each stage in the hybrid converter operates at reduced conversion ratio and hence, higher efficiency. The circuit innovations are pursued to improve efficiency across wide variation of output voltage and load current.

SUMMARY OF RESULTS

Design and tape-out of a single stage hybrid converter: A Dickson topology with conversion ratio of 7:1 has been chosen as SC stage. An input voltage of 10V has been used for the design. The SC generates an output voltage between 1.42V to 1.15V and the buck output varies between 1.1V to 0.2V. A ring oscillator based VCO has been used to generate the clock signals for the SC. A resistor string based startup network is used and the finite ramp time of the input voltage has been utilized to generate an auto startup signal. Clamping circuits have been used across different voltage domains to ensure device stress remains within limit during startup, shut down or load transient. The SC frequency is modulated with load current to minimize loss at low load currents and for ultra-low load current, an externally enabled PFM mode has been added. A peak current mode control based buck topology is designed. Frequency adaptive variable slope compensation is used in the design. For managing efficiency across load, variable operating frequency and variable MOS width are considered. A test-chip is designed and taped-out in 130nm CMOS to study the characteristics of the hybrid converter (Figure 1). The maximum conversion ratio designed to be 50 (10V input to 0.2V output). The test chip will be back in end of August 2013 and will be measured in early Fall 2013.

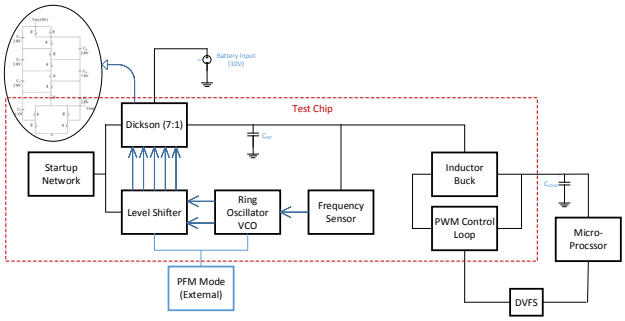

Figure 1: The overall topology of the hybrid converter.

Simulation methodology to study the effect of various packaging scenarios: A methodology has been developed to study the effect of packaging scenarios for voltage regulator (VR), processor, and loop filter on the PDN impedance and regulator performance. The frequency domain analysis studies the VR design considerations for different packaging conditions. The methodology is used to study the potential and challenges of integrating an inductor based DC-DC converter based voltage regulator module (VRM) as a separate die with processor for high-performance power delivery network (PDN). The effects of VR design and integration scenarios (on-board, on-package, or on-die) of the LC loop filter are studied.

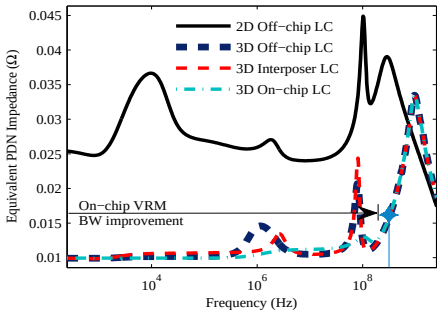

Figure 2: Simulation of PDN impedance for various integration scenarios for processor, VR, and loop filter.

Keywords: integrated converters, hybrid conversion, efficiency, high conversion ratio, packaging

INDUSTRY INTERACTIONS

Texas Instruments, Intel, IBM, and AMD

MAJOR PAPERS/PATENTS

[1] S. Carlo et. al, “On the Potential of 3D Integration of Inductive DC-DC Converter for High-Performance Power Delivery,” DAC 2013.

TASK 1836.112 SHORTSTOP: FAST POWER SUPPLY BOOSTING

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DENNIS SYLVESTER, UNIVERSITY OF MICHIGAN

SIGNIFICANCE AND OBJECTIVES

Fast boosting of supply rails is critical for near-threshold computing to improve performance-constrained energy efficiency. A novel supply boosting technique, called Shortstop, boosts a 3nF core in 26ns while maintaining acceptable supply voltage droops. The innate parasitic inductance of a dedicated dirty supply rail is used as a boost-converter and combined with an on-chip boost capacitor.

TECHNICAL APPROACH

Shortstop adds a second "dirty" supply rail and an on-chip boost capacitor to rapidly boost the core. The key idea is to transition the cores to high voltage using the dirty supply, thereby decoupling the transition from the clean high voltage supply and isolating other cores from supply droop. In addition, we use the dirty supply's wirebond/C4 innate parasitic inductance in a boost converter arrangement, thereby exploiting this inductance as an asset rather than barrier to fast supply transitions. Finally, on-chip decoupling capacitance is configured as a boost capacitor, further aiding supply transition.

SUMMARY OF RESULTS

Shortstop is validated in a 28nm CMOS test chip measuring 3.9 mm^2 (Figure 1). The chip is wirebonded to an 88-pin QFN package and a 108-pin ceramic PGA package with two wirebond lengths to vary package parasitics.

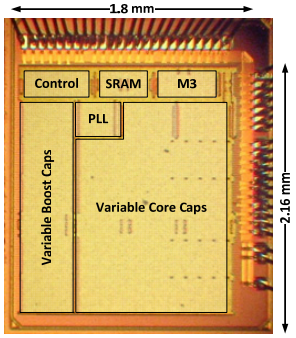

Figure 1: Die shot of 28nm test chip.

Figure 2 shows silicon measurements comparing boosting time for the included ARM Cortex-M3 core using a baseline PMOS header based approach and Shortstop. The 1-pin baseline assumes Shortstop's hardware overhead can be amortized across multiple cores and hence is negligible, while the 2-pin baseline is a conservative estimate where the number of dirty supply pins equals the number of high supply pins. For the M3 core, boost latency and droop are improved by 1.7× and 6×, respectively.

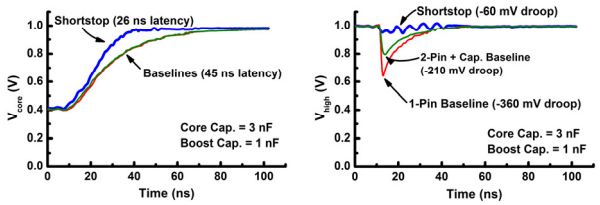

Figure 2: Measured rail voltages for 3 nF core (QFN package).

Figure 3 compares supply droop and boost latency, defined by rise time within 10% of Vdd, for the baselines and Shortstop across different emulated core sizes. As core size decreases, Shortstop exhibits slightly increased gains against baselines, while supply droop is relatively constant at 6× and 3× for the 1-pin and 2-pin baseline, respectively. For a 15 nF core (an Intel Atom-sized core), boost latency is improved by 1.6× in addition to a 6× droop reduction.

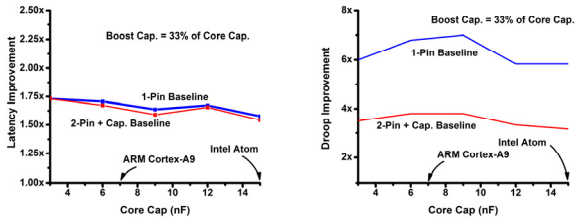

Figure 3: Measured latency/droop improvement for varying core cap. (QFN package).

Finally, Shortstop maintained a 1.4× latency improvement and 4× droop reduction across the three packages tested. As package parasitics decrease, the baseline latency and droop improves but this is balanced by decreased parasitics on the dirty supply which shortens boost time to energize the parasitic inductance.

Keywords: Near-threshold computing, low-power, energy-efficiency, on-chip power supplies, core supply boosting.

INDUSTRY INTERACTIONS

Intel

MAJOR PAPERS/PATENTS

[1] N. Pinckney et. al., "Shortstop: An On-Chip Fast Supply Boosting Technique," IEEE Symposium on VLSI Circuits, June 2013.

TASK 1836.115, ANALYSIS AND CHARACTERIZATION OF SWITCHED-MODE DC-DC POWER CONVERTERS

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SIGNIFICANCE AND OBJECTIVES

Switched-mode DC-DC power converters are ubiquitously used for critical power processing in many applications ranging from analog/mixed-signal ICs, microprocessors, SoCs and embedded systems. This project aims to develop techniques and methodologies to analyze and design switched-mode DC-DC converts while addressing key design challenges associated with power efficiency and power integrity.

TECHNICAL APPROACH

The design of DC-DC converters involves examining multiple topological choices and trading off between achievable design specifications, design/control complexity, and cost. Such design analysis is critically dependent on accurate analysis of dynamical operations of the converter and various losses. Simulation of DC-DC converters at the full schematic/extracted layout level is confronted by huge cost due to the design complexity.

We will develop methods for efficient simulation and characterization of switched-mode DC-DC converters. Dedicated envelope-following algorithms will be developed for simulation of DC-DC converters without any significant loss of accuracy. Furthermore, we will develop behavioral models to guide the design process.

SUMMARY OF RESULTS

In the first six months of this project, we have been developing a transistor-level simulation environment for switching DC-DC power converters. As a result, a base-line time-domain envelope-following simulation algorithm is being implemented. Several techniques associated with simulation and modeling of switching converters have been proposed and planned.

A key focus of this project is on the development of new time-domain envelope following (EF) analysis algorithms for DC-DC converters. Developing new time-domain methods is key to simulating hard switching activities of the converter in order to accurately predict the converter performance with good robustness and efficiency. In this regard, the envelope-following methods are good algorithmic fit for dealing with the challenges brought by the dynamics with widely spread time scales that exist in a switching converter. Furthermore, it is also critical to develop algorithms that can be seamlessly applied to converters operated with complex control and modulation schemes under both a fixed and variable switching frequency, e.g. under PWM vs. PFM modulations, as shown in Figure 1.

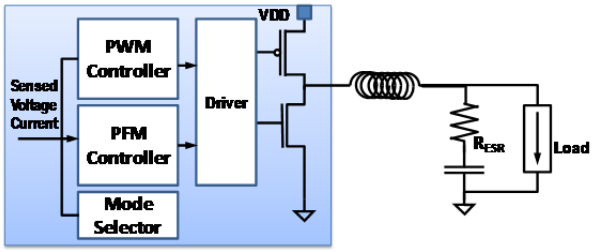

Figure 1: A DC-DC converter with PWM/PFM control.

To this end, issues such as precise sampling of the envelope, determination of EF cycle step length, and simulation robustness and accuracy are general challenges for any EF-type analysis, but nevertheless, become particularly more pronounced for the EF analysis of switching converters. To address these challenges, we will leverage design knowledge and exploit the resulting numerical structure of the EF problem formulation to achieve the desired level of simulation efficiency and robustness. This approach is illustrated in Figure 2 for the case of tracking the envelope of the PFM mode with a variable switching period.

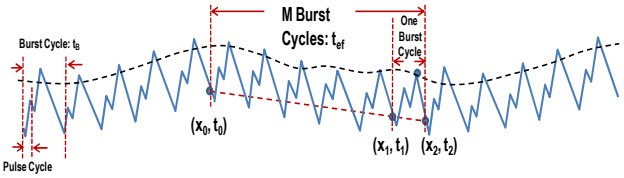

Figure 2: Time-domain envelope following method for tracking the PFM mode.

We will take one step forward by extracting design-oriented behavioral models that are better suited for providing design insights. These models will capture time-averaged behavior of the converter, hence providing good estimation of the envelope. Furthermore, current/voltage ripples will be accounted in the model. The models will be in the form of extracted closed-form expressions and provide a basis for reasoning about the circuit dynamics, control, ripples, and stability of a converter design.

Keywords: switched-mode DC-DC converters, simulation, envelope-following algorithm, behavioral modeling, design guidance

INDUSTRY INTERACTIONS

Texas Instruments, Freescale

TASK 1836.116, EFFICIENT PA ARCHITECTURES FOR POWERLINE COMMUNICATIONS

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SIGNIFICANCE AND OBJECTIVES

Using power lines for communications is highly attractive for several end applications, since in principle, this communication medium allows for cost-effective reuse of existing infrastructure. This research addresses the design of power efficient transmitters for powerline communication systems that support data rates up to several hundreds of kbps.

TECHNICAL APPROACH

A PWM-based design will be utilized in the transmitter implementation. Critical design considerations including efficiency, linearity, and spurious emissions will be addressed. Since the switching frequency for the PWM generator can be of the order of several tens of MHz, a PLL-based PWM generator that avoids the requirement for a ramp will be considered for the implementation. The feasibility of the transmitter in a deep submicron process such as a 65nm process will be investigated. The potential for using longer channel-length CMOS such as 130nm through architectural optimization, such as the use of a higher-order loop filters will be studied.

SUMMARY OF RESULTS

The architecture of the PLL-based pulse-width modulator is shown in Fig. 1. This architecture has been verified as part of a different project, in an IC implementation. This design provides a peak output power of 1.2 W in a 6.8 Ohm load, with a 4.8 V supply. The design achieves a THD of -65 dB with a switching frequency up to 20 MHz, for input bandwidth up to several tens of kHz. The peak efficiency is measured at 83% for an output power larger than 1W for a switching frequency of 10 MHz.

We are currently investigating the potential use of this approach for a signal bandwidth of 40-480 kHz, with signal peak-to-average ratio of 10 dB. The design targets include a 1V-rms signal level into a 2 Ohm load, with an output noise level of -65dBc at 535 kHz.

VCO non-linearity has been determined to be a key contributor to harmonic and intermodulation products in the design. In order to reduce even-order non-linearity, a differential VCO topology has been investigated. A macro-model of a PLL-PWM system that employs a third-order loop filter with PLL reference frequency of 15 MHz, for an output switching frequency of 30 MHz has been simulated. The macomodel is currently being optimized to support input bandwidth up to 1 MHz. Circuit-level design based on the macromodel is being performed.

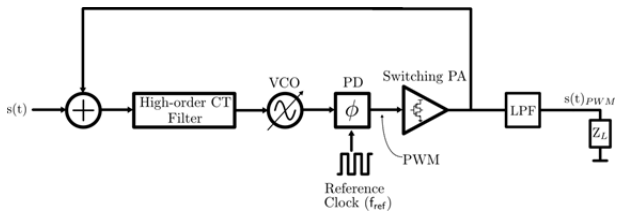

Figure 1: Architecture

Keywords: PWM, digital powerline transmitters, switching mode PAs.

INDUSTRY INTERACTIONS

Texas Instruments

TASK 1836.118, LOW NOISE, LOW RIPPLE FULLY INTEGRATED DC-DC CONVERTERS FOR SIGNAL CHAIN APPLICATIONS

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SAYFE KIAEI, ARIZONA STATE UNIVERSITY, SAYFE@ASU.EDU

SIGNIFICANCE AND OBJECTIVES

Fully integrated isolated DC-DC converters are an essential component in power monitoring, biomedical, and motor control applications where ground isolation is required. State of art approaches utilize resonant mode converters with bulky transformers, but due to high noise, size and weight, discrete transformer based approaches are not suitable for fully integrated mixed signal applications.

TECHNICAL APPROACH

In this project, isolated converters that can be integrated with mixed signal building blocks, such as current monitors, ADCs and telecommunication modules will be developed. A fully integrated dc-dc converter is made possible by integrating the low noise power converter with on-chip coreless transformer. Mature IC processing techniques produce high quality insulation layers, and integrated dc-dc converters typically have superior isolation rating and higher reliability than those with discrete transformers. We would also utilize closed look calibration techniques that can track the peak power transfer frequency of the integrated transformer, overcoming the impact of process variation on efficiency and noise of the system.

SUMMARY OF RESULTS

The fully integrated isolated DC-DC converter architecture is represented in Figure 1. Example input and output voltage are shown with 200V isolation. At the primary side, a transformer is utilized to transfer power source across a ground isolation boundary. At secondary side, a rectifier and a voltage regulator are required to provide high quality power supply to following circuits.

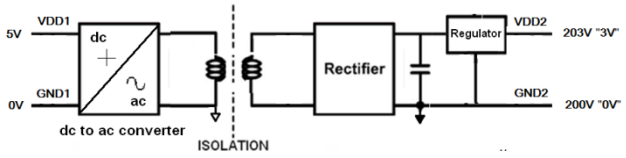


Figure 1: Power transfer block diagram

Previously reported resonant type power converters have suffered from higher noise and require follow on linear regulators. On a single chip solution, where the mixed signal die have to be powered at a much higher ground potential, EMI interference may affect surrounding signal chain circuits' dynamic range. In order to solve this issue, we proposed a novel power source generator with lower EMI noise and high efficiency.

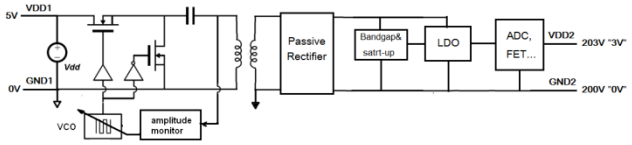


Figure 2: Fully integrated isolated converter circuits diagram

As shown in Figure 2, bottom plate switching capacitor with controllable switching frequency is utilized to generate primary side power source. Note that transformer sees the same capacitor value regardless capacitor switching frequency. This means system has stable frequency response and we can realize highest power transfer efficiency by sweeping VCO frequency.

At the start-up of the converter, VCO frequency will be digitally stepped up by a closed control loop. On the secondary side, the envelope power will be measured and logged. At the frequency where the peak power is detected, the VCO frequency is locked. An amplitude monitor is utilized to make sure system work at this optimum frequency.

At secondary side, in order to make rectifier act fast enough for >100 MHz signal, passive type rectifier should be used. A LDO is also utilized to regulate output to high precision voltage.

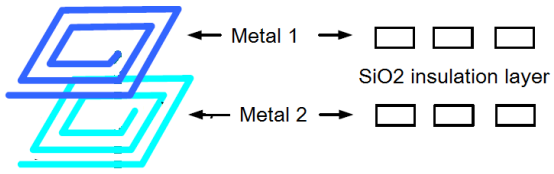


Figure 3: On-chip transformer structure and cross section

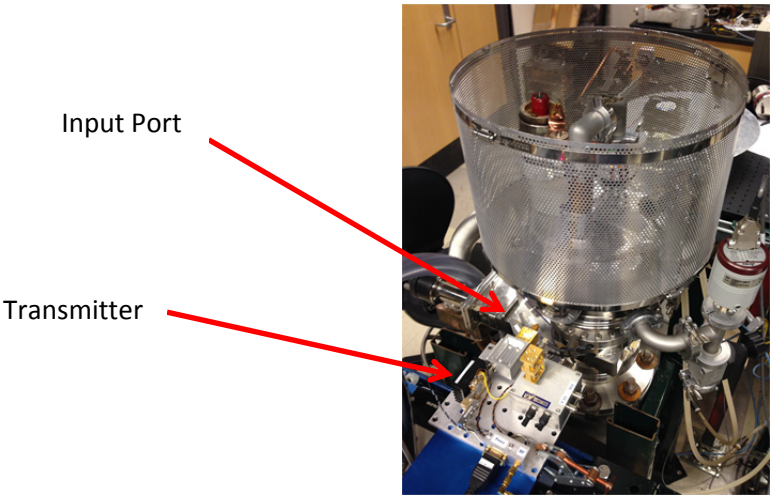
On-chip transformer is implemented as stacked spirals as shown in Figure 3. Metal layers from mature IC process could be easily patterned to the designed shape. Isolation between two ground domains is provided by the insulation layers between the primary coil and secondary coil. SiO2 naturally acts as insulation layer between two metal layers and it can provide over 800V/um breakdown strength. Also, a faraday cage will be added to further reduce EMI from the transformer.

Keywords: EMI, DC-DC, transformer, switch-cap, isolate

INDUSTRY INTERACTIONS

Texas Instruments

SAFETY AND SECURITY THRUST



Applied Materials test reactor with a rotational spectrometer

Summary of Accomplishments

CATEGORY	ACCOMPLISHMENT
Security and Safety	Adaptive test is challenging for analog and RF testing. A statistical model was developed which combines both intra-die and inter-die modeling approaches for reducing test cost in analog/RF ICs. Also, a spatial decomposition method was developed under the model view controller framework for breaking down the variation of a wafer to its spatial constituents. (1836.092, PI: Y. Makris, Univ. Texas, Dallas) Publication: K. Huang, N. Kupp, J. Carulli, and Y. Makris, "Handling discontinuous effects in modeling spatial correlation of wafer-level analog/RF tests," 2013.
Security and Safety	Low-cost CMOS technology can potentially be used to realize sub-millimeter-wave and Terahertz receivers and transmitters for imaging applications. A terahertz SPICE model was developed which can predict the responsivity and noise performance of 65nm FETs, and the model was validated with 200GHz measurements. (1836.079, PI: M. Hella, RPI) Publication: Gutin, A.; Nahar, S.; Hella, M.; Shur, M., "Modeling Terahertz Plasmonic Si FETs With SPICE," Terahertz Science and Technology, IEEE Transactions on , In Press.
Security and Safety	Physically unclonable functions (PUFs) were developed which exploit layout variations of gate pitches near "forbidden pitches" to achieve higher uniqueness for the PUF, and a test chip was fabricated in 45nm CMOS. (1836.074, PI: W. Burleson, Univ. Mass, Amherst) Publication: Raghavan Kumar and Wayne Burleson, "Litho-Aware and Low Power Design of a Secure Current Based PUF", Accepted at International Symposium on Low Power Electronics and Design, 2013.
Security and Safety	Demonstrated THz spectroscopic measurement of absolute concentrations of plasma constituents and their temperatures in an Applied Materials Plasma reactor for semiconductor manufacturing. (1836.048, PI: F. De Lucia, Ohio State University) Publication: Y. H. Helal, C. F. Neese, J. A. Holt, F. C. De Lucia, P. R. Ewing, P. J. Stout, M. D. Armacost, "Submillimeter spectroscopic diagnostics in a semiconductor processing plasma," 68th International Symposium on Molecular Spectroscopy, Columbus, 2013.

TASK 1836.039, UXIDS: UNCLONABLE MIXED-SIGNAL INTEGRATED CIRCUITS IDENTIFICATION

FARINAZ KOUSHANFAR, RICE UNIVERSITY, FARINAZ@RICE.EDU

SIGNIFICANCE AND OBJECTIVES

This project devised the concept, architecture, building blocks, silicon implementation, and authentication protocol for the first current-based Strong PUF, called UxID. The new authentication protocol is created to be error-resilient and secure against the security attacks. Thorough analysis and evaluations of the UxID and its security have been performed.

TECHNICAL APPROACH

A general abstraction of Strong PUF architecture was created and used for devising the UxID architecture [2]. Candidate circuits for realizing the blocks were designed. Using HSPICE simulations, we selected the best building blocks and architecture in terms of power, area, performance and statistical properties. A fully custom UxID chip was designed and implemented in IBM 9LP 90nm CMOS. Unfortunately, because of the operational sensitivities UxID responses had errors and were prone to security attacks including reverse engineering. We introduced SlenderPUF, a lightweight Strong PUF authentication protocol that is robust to errors and resilient against attacks [1,4,5].

SUMMARY OF RESULTS

Figure 1 demonstrates our abstraction of the strong PUF architecture which identified three major building blocks shown in different colors: (current) variability generation, selection & combining, and comparison. The implementation of the building blocks is also demonstrated on the figure. The building blocks were selected from a set of candidate blocks. The criteria for selecting the building blocks included form factor, power consumption, PUF operability and statistical PUF properties. These properties were carefully evaluated using extensive set of HSPICE simulations that also provided the best operation point for UxID [2].

We custom designed the cells and went through all the steps for IC tapeout. Post-layout simulation confirmed the PUF operability and statistical challenge/response properties. All of our simulations and chip design were done in IBM CMOS 9FLP (90nm) technology. Our layout used 6 metal stacks. We sent out the chip for fabrication and packaging through the MOSIS/SRC joint program. We set up and wrote a program on FPGA which in effect performs the scan chain operation to input the challenges and output the responses serially in and out the PUF structure.

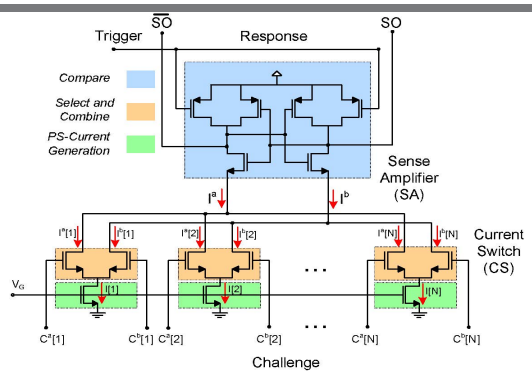


Figure 1- the architecture and building blocks of UxID.

Orthogonal to the chip design and Fabrication, we created the SlenderPUF protocol [1]. In this protocol, a trusted party has access to a model of the PUF responses, and authentication is performed by matching the substrings of physical responses against the model's responses. Therefore, the secret is never communicated over the channel. We have shown that string matching is inherently robust to errors, excluding the need for additional costly error correction, fuzzy extractors, or hash modules. The low overhead and practicality of the protocol are evaluated and confirmed by FPGA hardware implementation [4,5].

Future directions for this project include alternative Strong PUF circuits, and more comprehensive attack analysis and protocol development.

Keywords: Authentication, Current sensor, Physical Unclonable Function (PUF), Security, error correction

INDUSTRY INTERACTIONS

IBM, Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1]Rostami et al. "SlenderPUF: a light-weight, robust and secure Strong PUF by substring matching," TrustED, 2012

[2]Majzoobi et al. "Ultra-low power current-based PUF", ISCAS, 2011

[3]Ruhrmair et al. "Security based on physical unclonability and disorder", Chapter in Introduction to Hardware Security and Trust, 2011

[4]Majzoobi et al. "Robust and reverse-engineering resilient PUF authentication and key-exchange by substring matching," Patent submitted to Rice, 2013

[5]Rostami et al. "Lightweight and secure PUF authentication by pattern matching," Submitted to IEEE Trans. on Emerging topics in Computing, 2013.

TASK 1836.048, MILLIMETER AND SUBMILLIMETER GAS SENSORS: SYSTEM ARCHITECTURES FOR CMOS DEVICES

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SIGNIFICANCE AND OBJECTIVES

The objective of this project is to develop approaches to compact and inexpensive gas sensors based on millimeter and submillimeter (mm/submm) spectroscopy and implemented in CMOS technology. The dramatic cost, size, and power savings of CMOS will make this attractive sensor competitive in the mass market.

TECHNICAL APPROACH

We have demonstrated that powerful and unique sensors in the mm/submm spectral region are now practical. This task (coordinated with other tasks that will provide the necessary CMOS antennas, receivers, and transmitters) seeks to develop and demonstrate architectures appropriate for the mass market. This will be accomplished by an iterative interaction between our sensor design background, the development of an intermediate approach based on mass-market technology, and the CMOS design teams. New applications will be developed and demonstrated.

SUMMARY OF RESULTS

This project is designed to interface with and provide system guidance to three CMOS development projects at UT-D. These projects are to develop a probe source for the gas sensor, a sensitive heterodyne receiver, and antennas to transmit the microwave power from the source, through the gas interaction region, and onto the detector.

Because the transmitter is also required as a local oscillator for the receiver, it will be delivered to us first. It has been designed and fabricated by the UT-D team. We are currently working with them as they finalize the interface with our spectrometer control systems. We expect delivery of this system this summer and a spectroscopic demonstration shortly thereafter. While the CMOS receiver is being finalized, we will use one of our laboratory heterodyne receivers.

Last year we reported a project with Applied Materials to demonstrate the power of THz rotational spectroscopy for diagnostics and process control in semiconductor plasma reactors. This has been successful, and we are currently finalizing the design of a system for use on their production reactors at their research facility in California.

More specifically, we have shown that absolute

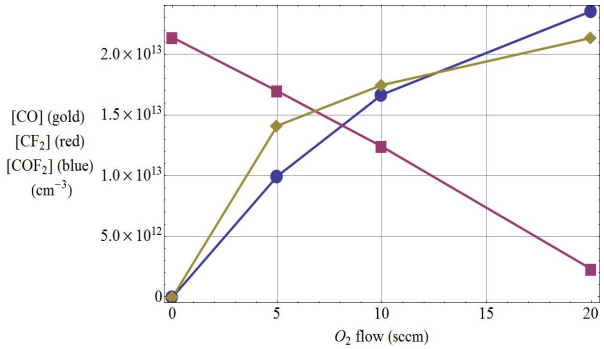

Figure 1. Measured absolute concentrations (/cm^3) of molecules and free radicals in a semiconductor processing plasma.

concentrations of constituents of these plasmas can be measured and related to the processing parameters chosen (e.g. feed gas flow rates, plasma discharge power, pumping speeds, etc). For example, In Fig. 1 the C_4F_8 flow is held constant, as the O_2 flow rate is varied. This graph shows the conversion of the initial CF_2 fragments into CO and COF_2 with increasing O_2 flow rates.

In a related experiment, the C_4F_8 was terminated and the decay of the COF_2 used as a measure of the cleaning rate of O_2 on the discharge residues in the reactor.

It was also shown that THz spectroscopic measurements could be used to remotely measure the rotational/translational temperature of the plasma.

Keywords: compact submillimeter spectroscopic gas Sensor

INDUSTRY INTERACTIONS

Texas Instruments, IBM, Applied Materials

MAJOR PAPERS

[1] C. F. Neese, I. M. Medvedev, G. M. Plummer, A. Frank, C. Ball, and F. C. De Lucia, "A Compact Submillimeter/Terahertz Gas Sensor with Efficient Gas Collection, Preconcentration, and ppt Sensitivity," *IEEE Sensors, vol. 12, pp. 2565-2574, 2012.*

[2] Y. H. Helal, C. F. Neese, J. A. Holt, F. C. De Lucia, P. R. Ewing, P. J. Stout, M. D. Armacost, "Submillimeter spectroscopic diagnostics in a semiconductor processing plasma," 68th International Symposium on Molecular Spectroscopy, Columbus, 2013.

TASK 1836.067, GUIDELINES FOR OPTIMAL DESIGN OF SUB-THZ SOURCES

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SIGNIFICANCE AND OBJECTIVES

Owing to the low f_{MAX} of 65nm CMOS process, it is extremely challenging to achieve high output power using fundamental frequency generation or amplification. The primary focus of this work is to generate high power at lower frequency using power amplifiers and power combiners and then use frequency doublers to generate the required power at sub mm-wave and THz frequencies (180-240GHz).

TECHNICAL APPROACH

The top level design topology along with the power budget is shown in Fig.1. Since the input power available from the measurement setup is limited to a maximum of 0dBm at 100GHz, a high gain amplifier is realized by adding a three-stage pre-amplifier to the core power amplifier. The pre-amplifier is designed using a single-ended common-source amplifier topology with shunt-stub microstrip transmission lines for inter-stage matching and delivers 5dBm to the single ended to differential power splitter. The core amplifier is designed as a cascaded four stages fully differential common-source amplifier using transformer matching. For increasing the output power of the amplifier, the sizes of the transistors are increased in the successive stages. The core amplifier delivers 16dBm at 100GHz to the passive frequency doubler that is realized using varactors.

SUMMARY OF RESULTS

The novel single ended to two-way differential power splitter is designed using coupled line theory as shown in Fig.2. The design saves chip area and has lower loss than prior published results.

The pre-amplifier and the core amplifier are designed independently and matched to the power combiners/splitters. For the single-ended pre-amplifier stages, a combination of p-well MOS capacitors and MIM capacitors are used to provide an effective AC ground. The effect of loss in the AC ground is less pronounced in the differential core amplifier due to the presence of virtual ground at the nodes of symmetry. The size of the varactor in the frequency doubler is optimized based on the series resistance and the total capacitance. Two identical balanced frequency doublers are employed to avoid breakdown of varactors resulting from high voltage swing. The output power is then combined at 200GHz.

All the passive structures are EM simulated using Sonnet. Large signal parameters are performed on the transmitter with P_{IN}=0dBm.

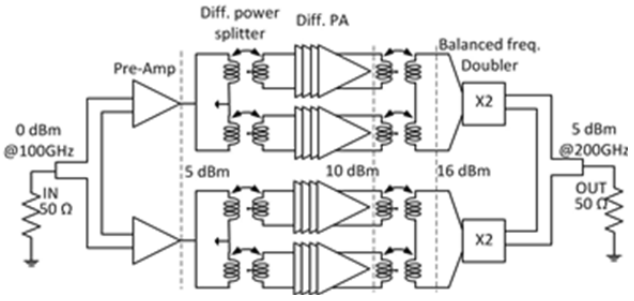

Figure 1: Schematic of 200GHz transmitter with power budget.

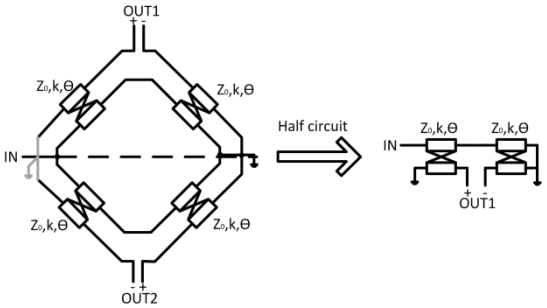

Figure 2: Design of novel single-ended to two way differential power splitter/combiner.

The extracted simulation results are summarized in the table below.

Table 1: Extracted Simulation Results

Frequency (GHz)	Bandwidth (%)	Output Power (dBm)	DC Power (W)	Tech.
200	7.5	6	0.4	65nm CMOS

Keywords: THz, Power Amplifier, Power Combiner, sub THz Transmitter, Frequency Multiplier.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Sriram Muralidharan, Kefei Wu, Mona Hella, "*High Power Transmitter Architecture for sub-THz frequencies using 65-nm CMOS technology* ", SRC TECHCON 2013.

[2] Sriram Muralidharan, Kefei Wu, Mona Hella, "Compact, Low-loss, Symmetric mm-wave and sub-THz PowerCombiner/Divider", US Provisional Patent Application No. 61/781,284

TASK 1836.072, LOW COST TEST OF HIGH SPEED SIGNALS

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SIGNIFICANCE AND OBJECTIVES

With increasing speeds of communication systems, the cost of testing high speed devices (10 GHz and beyond) for noise and distortion is becoming prohibitive. In addition, acquisition of high speed signal waveforms poses significant challenges. In this task, low cost scalable solutions for future high speed test and signal integrity characterization are developed.

TECHNICAL APPROACH

In this task, the cost of high speed test instrumentation is reduced by using incoherent undersampling and back end signal processing. Incoherent sampling techniques do not require complicated clock synchronization circuits and hence, lead to reductions in the cost and complexity of high speed test instrumentation. While direct undersampling based systems are limited in bandwidth up to the bandwidth of the track and hold amplifier, techniques such as bandwidth interleaving are used to break the bandwidth bottleneck using broad band mixers to down convert signal components beyond the track and hold bandwidth to lower frequency band where they can be sampled by the track and hold amplifier.

SUMMARY OF RESULTS

I

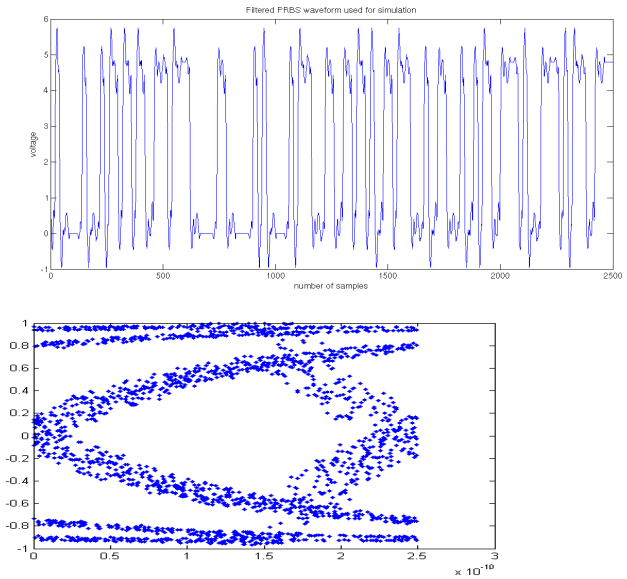

Figure 1: Reconstructed 2^7 -1 PRBS waveform using incoherent under-sampling (left); Reconstructed eye for random bit stream using incoherent under-sampling (right)

Low cost scalable solutions for high frequency test signal waveform acquisition have been demonstrated that are robust to variations in signal phase and do not require precise phase synchronization at high frequencies. It is possible to reconstruct, with high accuracy, complex periodic signal waveforms ranging from multi-tone signals to pseudo random bit sequences (PRBSs). In Fig 1 (left) we show the reconstructed eye for a 127 bit PRBS waveform. Reconstruction is performed using time domain analysis methods that give O(log(N)) improvement per iteration over Fourier domain reconstruction (N= no of samples). In Fig. 1 (right), a reconstruction of the eye for a random bit stream is shown. Also using the proposed techniques, jitter measurement and separation of random, periodic and crosstalk components were demonstrated.

Keywords: High speed test, waveform acquisition, under-sampling, jitter measurement, eye monitoring

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] N. Tzou, D. Bhatta, S. Hsiao, and A.Chatterjee. Periodic Jitter and Bounded Uncorrelated Jitter Decomposition Using Incoherent Undersampling, Design Automation and Test Europe, DATE 2013, IEEE March 2013 , pp 1667

[2] D. Bhatta, A. Bannerjee, S. Deyati, N. Tzou, and Chatterjee A. Time domain reconstruction of signal envelope for high speed rf test setup using incoherent undersampling. In Latin American Test Workshop, LATW March 2013,

TASK 1836.074, SUB-45NM CIRCUIT DESIGN FOR TRUE RANDOM NUMBER GENERATION AND CHIP IDENTIFICATION

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CHRISTOF PAAR, UNIVERSITY, RUHR UNIVERSITAT BOCHUM

SIGNIFICANCE AND OBJECTIVES

This report presents our work on improving the quality of Physically Unclonable Functions from a chip fabrication point of view. As Lithography is one of the main sources of process variations, it has been manipulated to suppress systematic variations in order to improve the uniqueness of PUFs.

TECHNICAL APPROACH

The concept of forbidden pitches has been exploited in this work for improving a PUF's quality. Near forbidden pitches, the gate structures that are printed onto the wafer are highly sensitive to pitch variations. By using forbidden pitches constructively, the extent of manufacturing variations are improved. To validate the results, a current-based PUF architecture shown in Figure 1 is used. The current-generation transistors are broken using a lithographic simulation framework and aligned at pitches closer to forbidden zone. The framework computes the dimensions of the printed contour and obtains the critical dimension distribution to be used in circuit simulations.

SUMMARY OF RESULTS

As stated earlier, the lithographic simulation framework computes the critical dimension distribution, which acts as a component of the process variation model in circuit simulations. This is done by performing an aerial image simulation over the PUF layout under the presence of various sources of lithographic variations such as dose, defocus, resist thickness etc. The obtained process variation model 's statistics are shown in Table 1. The table shows the model for both inter-die and inter-wafer variations. For capturing inter-wafer variations, we used the wafer-tilt effect along with the other sources of variations.

Table 1: Statistical Parameters of CD distribution

	Die	Wafer
Mean	44.5nm	44.8nm
Std. deviation	10nm	8nm

By running circuit simulations, the performance metrics of the PUF circuit is evaluated. Since the proposed litho-aware scheme targets at improving inter-die and inter-wafer uniqueness of a PUF circuit, an extensive set of

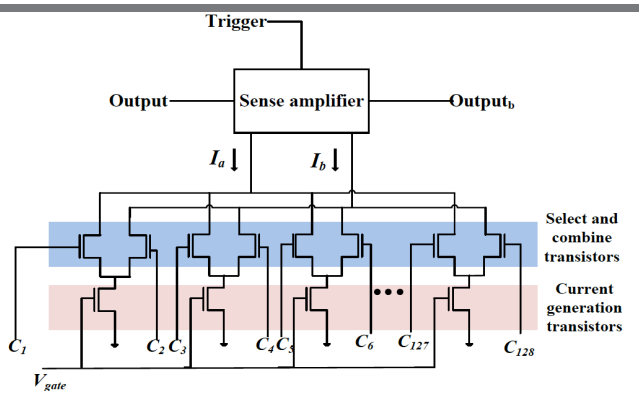

Figure 1: Current based PUF architecture used in this work. The external challenges decide the fraction of current added by a single stage. The final currents I_a and I_b are compared to generate a single bit response.

Table 2. Uniqueness validation results

Type of simulation	Type of PUF	Uniqueness (%)
Die	Base design	46
	Litho-aware design	49
Wafer	Base Design	33
	Litho-aware design	38

circuit simulations were performed. Since a challenge produces a single bit response, 128 challenges were grouped together to form a challenge set. The responses of 128 challenges were grouped together to form a 128-bit response. The results are tabulated in Table 2. We also show the performance metrics of a current based PUF designed using a conventional approach (Base Design) for comparison purposes. To the authors' knowledge, this is the first work on improving inter-wafer uniqueness from a chip fabrication level.

Keywords: sub-wavelength lithography, forbidden pitches, hardware security, current PUF, process variations

INDUSTRY INTERACTIONS

Intel, IBM, AMD

MAJOR PAPERS/PATENTS

[1] Raghavan Kumar and Wayne Burleson, "Litho-Aware and Low Power Design of a Secure Current Based PUF", Accepted at International Symposium on Low Power Electronics and Design, 2013.

TASK ID# 1836.079, CMOS THZ DETECTION

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SIGNIFICANCE AND OBJECTIVES

This task investigates the use of CMOS technology for THz detection in both imaging and communication applications. In that regard, modeling of FET plasmonic devices is performed together with the design of broadband antennas and wide bandwdith amplifiers. The main focus is to achieve bandwidth enhanced designs to support very high bit rate data communications with THz carrier frequency.

TECHNICAL APPROACH

We have developed a THz spice model based on the distributed FET channel [1]. The parameters used in the spice model are extracted from the measured dc characteristics of the FETs fabricated in 65 nm TI process. The model can be used to predict and optimize the device response in different circuit conditions.

We have designed antenna structures with an extended bandwidth to allow the use of the THz link for communications. These antennas include parasitic half wave, parasitic quarter wave and E shaped patch. The half and quarter wave patch antennas have a parasitic patch in the nearest metal level to the actual one to introduce two close by resonant points and thus increase the bandwidth. The E shaped patch introduces slots in the conventional patch antenna to introduce a nearby resonant frequency. The considered structures are shown in Fig.1. The comparative study based on the simulation results of these antennas in IBM 130nm technology are shown in Table I.

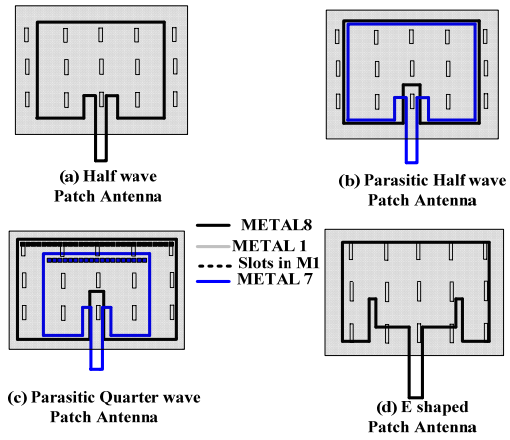

Figure 1: Antenna structure – (a) Conventional Half Wave Patch (a) Parasitic Half wave (b) Parasitic Quarter wave (c) E shaped Patch Antenna.

For the amplifier design, we have followed active feedback topology with inductive peaking to achieve ~15 GHz bandwidth with 28 dB gain (with buffer). The amplifier performance is limited by the input pole of the first stage interfacing with the detector since the detector acts as a very high resistance at the bias point for maximum response. Therefore, the first stage uses an f_T doubler configuration to decrease the input capacitance followed by a shunt shunt feedback amplifier to decrease both the input and output impedance..

SUMMARY OF RESULTS

The antenna simulation results are tabulated in Table I based on the simulation results in full 3D EM simulator HFSS.

Parameter	Regular Patch	Parasitic Half Wave Patch	Parasitic Quarter Wave Patch	E Shaped Patch
Size	316x245	260x235.3	320x119.3	400x241.5
Size	100%	79%	49%	124.7%
Efficiency	65.7%	44.6%	42%	56%
BW	6.3 GHz	18.9 GHz	18 GHz	17 GHz

The amplifier has five amplifying stages consuming total 44 mW dc power with the buffer circuit. The simulation results based on the assura extracted view in Cadence are shown in Fig. 2.

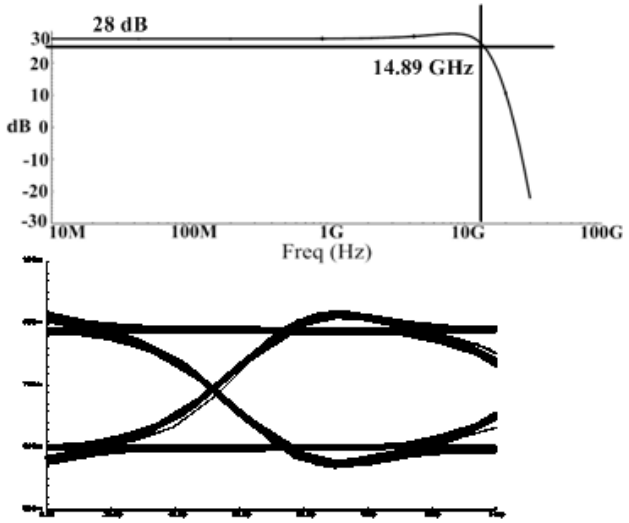

Figure 2: Frequency response and eye diagram for the designed amplifier.

Keywords: THz detection, Parasitic Patch Antenna, Active Feedback, E shaped Patch.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Gutin, A.; Nahar, S.; Hella, M.; Shur, M., "Modeling Terahertz Plasmonic Si FETs With SPICE," *Terahertz Science and Technology, IEEE Transactions on* , in Press. Available on IEEEXplore.

TASK 1836.082, LOW-COST ENERGY-EFFICIENT 60GHZ TRANSCEIVERS WITH BUILT-IN SELF-TEST

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ALI NIKNEJAD, UC BERKELEY

SIGNIFICANCE AND OBJECTIVES

CMOS mm-wave technology has the potential to transform short-range communication. Reducing the cost and power consumption of today's CMOS mm-wave transceivers – especially in chip-to-chip communication applications – is the principal goal of this project.

TECHNICAL APPROACH

To make wireless chip-to-chip links viable, our research focus has been on low energy and low cost, enabled by built-in self test (BIST) and on-chip antennas. Low energy consumption can be achieved by exploring extremely efficient circuit topologies, the primary focus of our research. The second approach is to explore extremely high data rates, which allows one to duty cycle the radios and maintain high throughput, low latency links. The first approach favors a lower carrier frequency (60 GHz) while the second favors a higher one (240 GHz). On-chip antennas are a key piece of technology for BIST and for eliminating expensive packaging.

SUMMARY OF RESULTS

Our project has explored the design space of short range communication links in the mm-wave band using two carrier frequencies. In the first approach, a fundamental mode transceiver is designed to operate at 60 GHz, and circuit and system optimization is used to reduce the power consumption of the radio to a great extent. The system is designed in concert with an on-chip slot loop antenna, which achieves a high efficiency of 30% (on a standard silicon substrate of 100um thickness). A 2x2 array is utilized and used for both transmission and reception. A novel switching scheme described in [1] utilized gated oscillators to achieve ultra low power operation and phase array transmission capability. By utilizing different antenna feedpoints, the Rx and Tx share the same array, which also allows reception in broadside or end-fire direction. Quarter wave feedlines minimize loading and allow signals to be routed and muxed into the LNA. The LO path of the receiver is carefully designed to minimize power consumption; the I/Q hybrid utilizes both distributed and lumped components to minimize size and loss, and the distributed portions serve as LO routing. A tripler with a push-push output and a large lock range (14%) is used to generate the carrier from a 10 GHz reference.

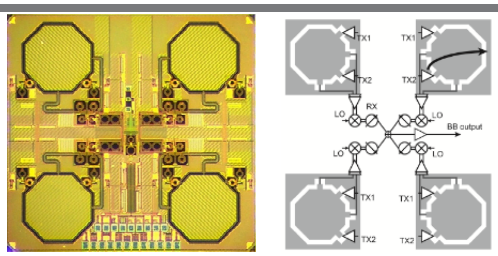

Figure 1: Fully integrated 60GHz phased array prototype in 65nm CMOS.

A prototype in 65nm technology measures 2.2 mm by 2.2 mm. The four element TX consumes only 50mW, while the RX consumes 65mW. To verify the integrated antenna array, the TX/RX radiation patterns were characterized using an external horn antenna. Full end-fire coverage is verified, with a peak output power of a single TX of -5dBm. The receiver's measured conversion gain is 20dB. Link measurements were performed for multiple ranges and directions. At 10.4Gb/s, the transceiver operates error-free over 10^7 symbols at 60cm range broadside, and with 12.5mW/16.25mW (TX/RX) per element, this represents the most energy-efficient 10+Gb/s phased-array to date [2].

The second focus of our project was to realize energy efficient high data rate links at a higher carrier frequency. In our first 65nm prototype the output of a 60 GHz transmitter was quadrupled to generate the carrier and efficient and high gain broadband traveling wave antennas were realized on-chip [3]. While the feasibility of a 240GHz link in CMOS was demonstrated, the power consumption and resulting energy consumption was rather high (1W and perhaps as low as 100pJ/bit). A second prototype has been designed from the ground up utilizing QPSK modulation, a coherent receiver, and a new slot based on-chip antenna. If fully operational, this prototype should demonstrate 20 Gbps with 20pJ/bit efficiency at 1.6 cm range. With a silicon lens, the range can be extended to 1.5 m.

MAJOR PAPERS/PATENTS

[1] L. Kong, et al., "A 21.5mW 10+Gb/s mm-Wave Phased-Array Transmitter in 65nm CMOS", *VLSI* 2012.

[2] L. Kong, et al., "A 50mW-TX 65mW-RX 60GHz 4-element phased-array transceiver with integrated antennas in 65nm CMOS," *ISSCC 2013.*

[3] J.-D. Park, et al., "A 260 GHz Fully Integrated CMOS Transceiver for Wireless Chip-to-Chip Communication," *VLSI* 2012.

TASK 1836.083, BUILT-IN TEST FOR POWER-EFFICIENT MILLIMETER-WAVE ARRAYS

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SIGNIFICANCE AND OBJECTIVES

This program will develop orthogonal code-based built-in-test techniques for millimeter-wave arrays, allowing for simultaneous testing of all elements in the array at either circuit or package level, reducing the time and cost of test. Also, circuit and system architectures to increase the power efficiency of a 60GHz phased array will be explored, and a transmitter with BIST will be demonstrated.

TECHNICAL APPROACH

A low-power 60GHz phased-array transmitter prototype with BIST will be developed in 0.12µm SiGe BiCMOS technology and scalable code-multiplexed test techniques will be developed for this demonstration platform. CDMA test techniques will be compared to both external test and traditional BIST techniques. Power-efficient PA and phase-shifters will be developed and incorporated into a multi-element 60-GHz phased-array prototype with BIST.

SUMMARY OF RESULTS

Code-Multiplexed Test Research: Behavioral simulations have been completed, validating the approach of applying CDMA coding to the phase shifter to allow measurement of all elements in the array simultaneously. Power detectors have been built into our PAs within a prototype array and software-based test algorithms will be run on the hardware in 4Q2013.

Power Amplifier (PA) Research: Our objectives for PA design were to explore techniques to enable >10% efficiency at 6dB back-off power levels to dramatically reduce the overall power consumption in a phased array. Multiple PA architectures have been explored, including class-AB, class-J, class-C, and Doherty structures. Three generations of PAs have been implemented and two have been measured. Our Gen-1 class-AB PA (8/2011 tapeout) achieved a measured 9dBm output 1dB compression point (oP_{1dB}), 15.6% peak power-added efficiency (PAE), and 3% PAE at 6dB output backoff (OBO) [1]. To improve performance, we explored harmonic termination techniques and developed a new multi-harmonic load-pull simulation technique. Using this approach, a 2nd generation class-AB PA (7/2012 tapeout) was designed and measurements show oP_{1dB} of 12dBm, with *record-breaking peak PAE* for a 60GHz PA. In May 2013, we taped out a class-J PA and a Doherty PA [2], both achieving *record efficiencies* and meeting program-level efficiency targets. Measurements will be made in 4Q2013.

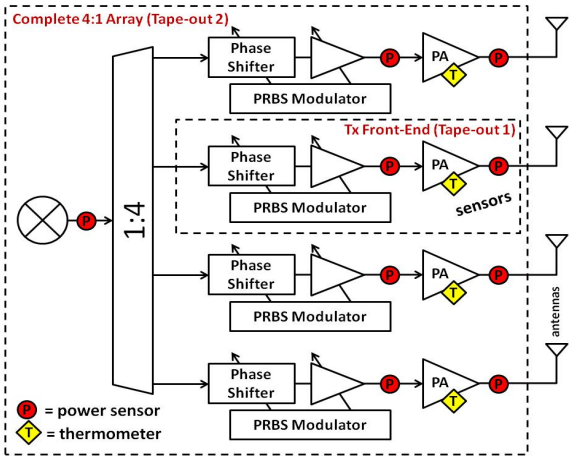

Figure 1: Block diagram of 60-GHz phased-array prototype.

Phase Shifter Research: Our objectives for phase shifter design were to explore compact architectures which do not degrade overall array efficiency. Three generations of phase shifters have been developed and one measured. Our 1st generation design (8/2011 tapeout) was a reflective-type topology targeting 360° phase shift in a single stage; however limited varactor Q led to poor performance. Our 2nd generation design was a vector interpolator, achieving a simulated 6dB gain at 31mW and 2°/0.3dB RMS accuracy. In May 2013, we taped out a novel dual-vector rotator which can provide two quadrature phase-shifted outputs suitable for efficiently driving a Doherty amplifier, to be measured in 4Q2013.

60GHz Phase Array Research: In May 2013, a dual-vector Doherty (DVD) 3-element array was taped out which includes our dual-vector rotators, Doherty amplifier, and class-J PAs with BIST. This first-of-a-kind architecture promises to significantly improve the array efficiency. Detailed simulated results are posted to the SRC website and measurements will be made in 4Q2013.

Keywords: millimeter-wave, phased-arrays, built-in test, 60GHz, CDMA, power amplifiers

INDUSTRY INTERACTIONS

Freescale

MAJOR PAPERS/PATENTS

[1] A. Sarkar and B. Floyd, "A 60 GHz Doherty PA with 14% PAE at 6-dB back off," *Proc. SRC Techcon Conf.*, Sept. 2013.

[2] A. Sarkar and B. Floyd, "Power efficient PAs for 60GHz phased arrays" *Proc. SRC Techcon Conf.*, Sept. 2012.

TASK 1836.084 SINGLE SET-UP DETAILED TESTING OF WIRELESS TRANSCEIVERS FRONT-ENDS USING DIGITAL PROCESSING

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SIGNIFICANCE AND OBJECTIVES

RF transceiver front-ends are typically tested in two steps, with RX and TX being tested separately, using RF instrumentation. Moreover, multiple set-ups are used to measure significant parameters, which increases the test cost. This project aims at eliminating the need for multiple test-ups and RF instrumentation.

TECHNICAL APPROACH

First a full-path model of the TX-RX loop-back is derived using the behavioral equivalent of each building block and the non-idealities that are expected in the path. This model is used to determine the optimum test signals that will separate the effect of desired parameters on observable output signals. Next, the derived relations are used to analytically compute the desired parameters in the loop-back mode, with the same set-up.

SUMMARY OF RESULTS

The above-described technique is applied to a zero-IF transceiver, which is hardest to test in the loop-back mode since all he information is compounded around the

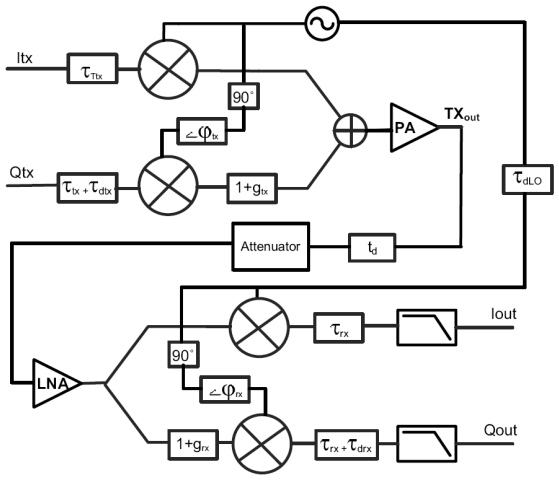

Figure 1: Full-path model of a zero-IF transceiver RF front-end

DC frequency. Hence, separating out TX and RX contributions are most challenging. The full path model (Figure 1) includes all path non-idealities, such as delays and delay skews, as well as expected non-idealities of the individual building blocks.

Upon derivation of this model, it is clear that a simple signal is needed to decouple effects of RX and TX as well as multiple parameters that need to be observed. A time domain decoupling technique is used to first separate out the effect of I and Q signals from one another. This helps in imposing a subset of terms on each observable output signal. Next, it is clear that a single measurement will not yield the ability to decouple all the desired parameters. Hence, a two-step measurement (with the same test set-up) is used to generate more independent equations. Once these equations are derived, they can be analytically solved to obtain the desired set of parameters. Table I shows the results of the hardware measurements using this approach.

Table I: Hardware measurement results using a custom designed board. The board is intentionally degraded to show that the technique works over a wide range of possible scenarios.

Parameter	Traditional	Proposed
g_{tx} (%)	-68	-69
g_{rx} (%)	-65	-68
ϕ_{tx} (˚)	31.2	35.9
ϕ_{rx} (˚)	64	66.8
IIP3 (dBm)	12.23	12.57
IIP3 (dBm)	13.28	13.16

Keywords: RF Built-in test, TX-RX loop-back, Single set-up measurement, EVM computation.

INDUSTRY INTERACTIONS

Intel Corporation, IBM

MAJOR PAPERS/PATENTS

[1] Nassery, Afsaneh; Ozev, Sule; Slamani, Mustapha; “Analytical modeling for EVM in OFDM transmitters including the effects of IIP3, I/Q imbalance, noise, AM/AM and AM/PM distortion”, (ETS), 2013.

TASK 1836.091, INTERCONNECTS ON FLEXIBLE PLASTIC SUBSTRATES

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SIGNIFICANCE AND OBJECTIVES

Interconnects which operate in the sub-THz range can perform over very large bandwidths and are well suited for high data-rate communication systems. The goal of this task is to investigate plastic waveguides with tunable dielectric constants that support low loss, low distortion, low crosstalk, and strong radiation confinement.

TECHNICAL APPROACH

The current task focuses on the fabrication and measurement of plastic composites with tuned dielectric constant as waveguides for THz interconnects. The classic mechanism for guiding in dielectrics is total internal reflection where radiation is confined in a region of high-refractive index cladded by a low-index region. Simulation indicates that high-index contrast in a ribbon waveguide design is the most efficient for strong radiation confinement. Mechanical measurements provide insight regarding the plastic flexibility at higher loading. It is our hope that with sufficiently high-dielectric constant ribbon, simple index guiding will provide acceptable confinement while retaining the low-loss benefits of polypropylene.

SUMMARY OF RESULTS

In the first year of the task, our efforts were devoted to a comprehensive simulation study of several dielectric waveguide designs including ribbon guides, and 1D & 2D Bragg reflector structures. In the current (2nd) year of the effort, the task has been focused on experimental studies of the simulated guides. The ribbon waveguides were identified as the simplest structure to fabricate and might be suitable for low-loss confined guiding if the dielectric constant of the ribbon was sufficiently high enough. To increase the dielectric constant, inorganic nanoparticles were employed and loaded into the host to make a composite plastic as illustrated in Figure 1.

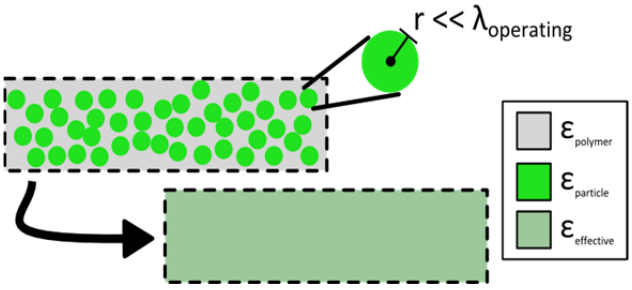

Figure 1: Illustration of the composite material featuring the plastic/polymeric host and the nanoparticle loading. The overall dielectric constant depends on the polymer and the volume loading of the nanoparticles (TiO_2)

A materials synthesis process based on micro-compounding was developed and composite plastic sheets using polypropylene as the host material (owing to its low-loss properties) were fabricated. Figure 2 shows an image of a fabricated polypropylene sheet.

Figure 2: Example of a fabricated polypropylene plastic.

TiO_2 nanoparticles were employed to increase the dielectric constant of the polypropylene plastic. We found that the dielectric constant of the composite sheet correlated with the loading fraction as expected (Figure 3). However, the flexibility of the composite sheet degraded at higher loadings which have not been well-studied in the literature. Further experimental studies are planned for the final (3rd) year of the task to obtain the dielectric loss tangent by spectroscopy and measure the propagation loss (dB/m) of the ribbon waveguides with various volume loading percentages, which is a matter of central importance for the future of flexible THz interconnects based on index guiding.

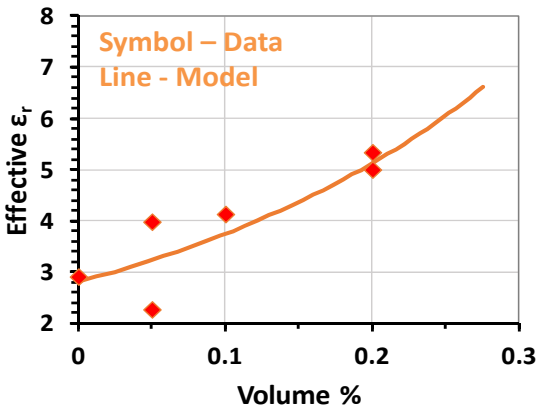

Figure 3: Experimental quasi-static measurements of the dependence of the dielectric constant of the composite plastics on the volume loading by the TiO_2 nanoparticle.

Keywords: dielectric waveguides, Thz, flexible ribbons

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Ian Williamson et al., "DIELECTRIC INTERCONNECTS FOR THZ CHIP-TO-CHIP COMMUNICATIONS", SRC Techcon September 2012.

TASK 1836.092, A MODEL-VIEW-CONTROLLER (MVC) PLATFORM FOR ADAPTIVE TEST

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SIGNIFICANCE AND OBJECTIVES

Adaptive test is an emerging approach to dynamically modify the test plan for RF devices with high specificity: per wafer or per device. This project will develop a model view controller (MVC) framework and statistical learning theory/machine learning methods necessary to support industrial adaptive test.

TECHNICAL APPROACH

We are architecting an adaptive test MVC framework with: (i) Models, which will serve as abstractions of existing industry production databases, (ii) Views, which will provide test engineers feedback on adaptive test algorithms, and (iii) Controllers, which will contain modular adaptive test components to be employed at each stage of testing. We anticipate treating these adaptive test components as "applications", which consist of algorithms for each stage of data collection and processing (inline/kerf, wafer final test, module final test, field returns, etc.). By standardizing the controller platform we can encourage the emergence of an adaptive test "application ecosystem", simplifying deployment.

SUMMARY OF RESULTS

There is growing industrial interest in deploying so-called “adaptive test”, or dynamically modifying the test plan. Adaptive test is particularly challenging for analog and RF testing, where testing is already a complicated and expensive endeavor. In this project, we posit that achieving meaningful results for adaptive test in the analog and RF test domain will require statistical models that are at parity of sophistication with the complexity of the test problem. To address this, we develop a model-view-controller architecture that responds to the challenges of adaptive test for analog and RF devices with an elegant and modular solution, enabling rapid deployment of novel statistical methods as they become available, while keeping test engineers informed about the inner workings of the deployed adaptive test system.

Within this MVC framework, in the last year of this project we developed a novel approach which handles discontinuous effects in spatial correlation modeling of wafer level analog/RF tests [1]. Effectiveness of the proposed approach is evaluated on industrial probe test data from more than 3,400 wafers, revealing significant error reduction over existing approaches.

We then investigated the potential of combining both intra-die and inter-die statistical modeling approaches for reducing test cost in analog/RF ICs, anticipating that the performance prediction accuracy of the joint correlation model will surpass the accuracy of its constituents [2]. Experimental results on industrial semiconductor manufacturing data validate this conjecture and corroborate the utility of the combined performance prediction models.

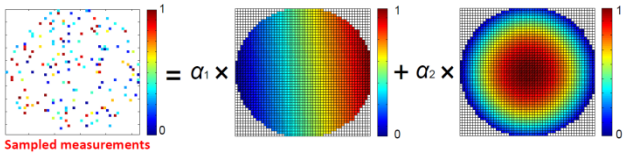

Figure 1: Wafer-level spatial decomposition approach

Finally, in an effort to monitor the semiconductor manufacturing process and understand the various sources of variation and their repercussions, we introduced a spatial decomposition method for breaking down the variation of a wafer to its spatial constituents, based on a small number of measurements sampled across the wafer, as shown in Figure 1. We demonstrated that by leveraging domain-specific knowledge and by using as constituents dynamically learned, interpretable basis functions, the ability of the proposed method to accurately identify the sources of variation is drastically improved, as compared to existing approaches. Results are reported on industrial data from high-volume manufacturing, confirming the ability of the proposed method to provide great insight regarding the sources of process variation in semiconductor manufacturing [3].

Keywords: analog/RF, adaptive test, test metric estimation, machine learning, spatial modeling

INDUSTRY INTERACTIONS

Texas Instruments, IBM

MAJOR PAPERS/PATENTS

[1] K. Huang, N. Kupp, J. Carulli, and Y. Makris, “Handling discontinuous effects in modeling spatial correlation of wafer-level analog/RF tests,” DATE, 2013

[2] K. Huang, N. Kupp, J. Carulli, and Y. Makris, “On combining alternate test with spatial correlation modeling in analog/RF ICs,” ETS 2013

[3] K. Huang, N. Kupp, J. Carulli, and Y. Makris, “Process monitoring through wafer-level spatial variation decomposition,” ITC 2013

TASK 1836.094, ACCURATE FSM APPROXIMATIONS OF ANALOG/RF SYSTEMS FOR DEBUGGING MIXED-SIGNAL DESIGNS

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ROBERT BRAYTON, UC BERKELEY

SIGNIFICANCE AND OBJECTIVES

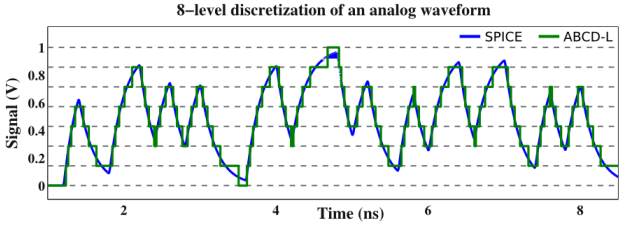
This project aims to develop tools, techniques, and algorithms to automatically generate purely Boolean models (e.g., FSMs, BDDs, AIGs, etc.) that accurately capture the SPICE-level continuous I/O behavior of analog/mixed-signal (AMS) systems. Such models will enable efficient formal analysis, verification, high-speed simulation, validation, and debugging of AMS designs, by leveraging existing Boolean analysis tools (e.g., ABC) and hybrid systems frameworks.

TECHNICAL APPROACH

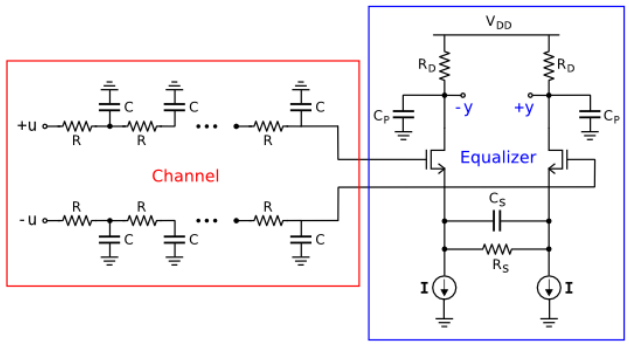
We have developed a suite of techniques for accurately Booleanizing AMS systems, by, (1) discretizing the signals in the system into multi-level sequences of bits, and (2) approximating the analog dynamics of the given system using purely Boolean operations carried out on those bits. One such technique, dubbed DAE2FSM, is based on Angluin's algorithm from computational learning theory, which we have adapted to automatically generate Mealy machine models of SPICE-level AMS designs. Another technique, called ABCD-D, was designed to accurately and efficiently Booleanize the transistor-level analog dynamics exhibited by cutting-edge digital designs. Yet another technique, ABCD-L, was designed to Booleanize continuous linear systems to capture analog effects, including inter-symbol interference (ISI), crosstalk, ringing, etc., to near-SPICE accuracy. We are actively exploring the Booleanization of large non-linear AMS systems, and the integration of such Boolean models into leading edge tools like ABC for accurate and scalable AMS verification/debugging.

SUMMARY OF RESULTS

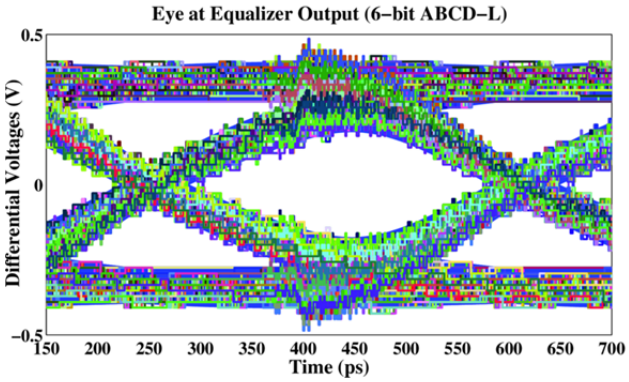
We have applied DAE2FSM, ABCD-D, and ABCD-L to a number of systems that are of interest to AMS designers. For example, the figure below was obtained by applying ABCD-L to a high-speed I/O link, where it accurately captures analog phenomena such as ISI, crosstalk, etc.



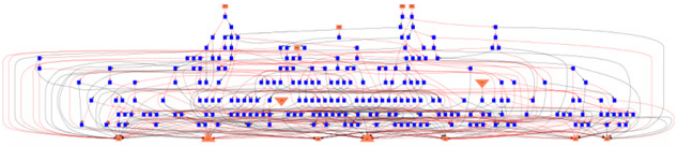
We have also applied ABCD-L to a (linearized) "channel followed by an equalizer" system, as shown below.



For the above system, the purely Boolean model produced by ABCD-L is able to accurately reproduce a key AMS-design relevant metric, i.e., the eye diagram at the output of the equalizer.



In addition, our efforts to integrate ABCD with cutting edge Boolean analysis tools (e.g., ABC) have produced promising initial results.



For example, the figure above depicts an AIG representation of an ABCD-L model, as produced by ABC.

Keywords: AMS verification, debugging, ABCD, FSM, AIG

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] Aadithya and Roychowdhury, DAE2FSM, DAC 2012.

[2] Aadithya and Roychowdhury, ABCD-D, TAU 2013.

[3] Aadithya and Roychowdhury, ABCD-L, DAC 2013.

TASK 1836.101, SPARSE 2D MIMO RADAR TRANSCEIVER DESIGN AND PROTOTYPING FOR 3D MILLIMETER-WAVE IMAGING

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SIGNIFICANCE AND OBJECTIVES

Millimeter wave (mm-wave) radar technology is a highly potential candidate for many safety and commercial applications. In an effort to achieving a better precision and affordability of such systems, sparse multiple-input-multiple-output (MIMO) radar technologies are explored within the mm-wave framework in this project.

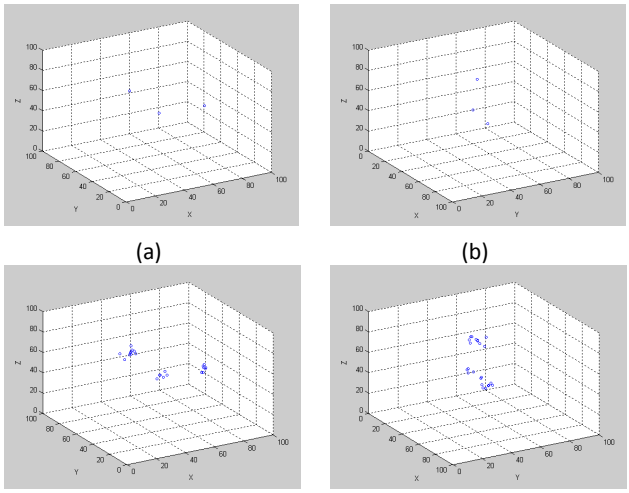
TECHNICAL APPROACH

The transceiver design for the MIMO radar mm-wave imaging system involves waveform design, antenna array design, and image processing techniques. In this project, three dimensional mm-wave imagers are designed in order to obtain images of objects placed behind obstacles or inside closed boxes. A two-dimensional arrangement of imaging transceiver arrays are placed in order to attain spatial diversity, which is exploited by interpolating the range and angle bin information from different imagers. In addition, a two-dimensional sparse MIMO transceiver array will be designed to help reduce the number of elements as well as the system cost.

SUMMARY OF RESULTS

In PI's previous work [2], the performance of a MIMO radar imaging system was compared with the traditional one, and it was demonstrated that the deployment of space-time block–codes in the transmit waveforms had the capability to yield further improvements. In this work, we make use of multiple such MIMO radar imaging systems to obtain three dimensional images. Four imagers placed at the corners of a rectangular plane capture the target images in different angle and range bins depending on their positions relative to the target.

Initially, we exploit the angular bin information received from the sensors in constructing images, similar to the scheme in [1]. However, it was not sufficient in estimating the presence and precise locations of multiple targets. Therefore, we enhance our scheme by utilizing the range bins obtained at the four sensors as well. In Figure 1(a) and (b), three point targets are shown from two different angles. For each point in the region under surveillance, the respective range and angle bins for the point for each of the four sensors are computed. Then the reflectivity coefficients are combined to estimate the likelihood of the presence of a target in that point. The resultant estimations are shown in Figure 1(c) and (d). The point targets are clearly identified, although they are somewhat blurred due to the spreading of the target pixels. Our ongoing and future tasks include the quantification of the detection probabilities and false alarm rates of such point targets.



(a) (b) (c) (d)

Figure 1: (a) and (b) Three point targets shown from two different angles of view; (c) and (d) the estimated images.

This scheme has also proven effective with simple (e.g. L-shaped) objects. But with more complex structures, the scheme cannot produce a clear image, which remains as our future task. In addition, we are exploring the use of image recovery by compressed sensing (CS) methods, and working towards building a prototype.

Keywords: MIMO Radar; millimeter wave; 3D imaging; reflectivity coefficient; transmit diversity.

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] T. Ali et al., "MIMO Radar for Target Detection and Localization in Sensor Networks," IEEE Systems Journal: Special Issue on Sensor Networks for Advanced Localization Systems, (accepted, December 2012).

[2] A. Sadeque et al., "Waveform Transmission Scheme for MIMO Radar Imaging based on Space-Time Block Codes," IEEE Transactions on Aerospace and Electronic Systems (accepted, April 2013).

[3] J. Sung et al., "Effects of ADC Quantization Noise on MIMO Radar Imaging," IEEE Transactions on Signal Processing (submitted, Nov. 2011).

TASK 1836.102, SUPERRESOLUTION TECHNIQUES FOR 3D MILLIMETER WAVE RADARS

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SIGNIFICANCE AND OBJECTIVES

Implementation of high-resolution 3D-millimeter wave imaging system will invariably use multiple antenna system such as beamformer whose performance is constrained by phase-errors in beamforming weights. Our objective is to derive analytical expression for minimum number of antenna elements required to ensure imaging system is immune to the given phase errors.

TECHNICAL APPROACH

To derive the expression for minimum antenna elements required, stochastic analysis of the phase errors in the beamforming weights is performed. We assumed phase errors are Gaussian distributed and found its effect on the directional capabilities of beamformer in terms of sidelobe suppression level. Using the central limit theorem we found out the PDFs of the mainlobe and the sidelobe in the presence of phase errors. We have also derived closed form expression for the expected beamformer power for any given direction, number of antenna element and known phase error variance.

SUMMARY OF RESULTS

The resolution of the beamforming imaging system greatly relies on beamformer's ability to unambiguously extract the wave data from the particular direction. Thus, we use the ratio of power in sidelobe to the power in mainlobe as a measure of resolution of the imaging system. This ratio is also called as sidelobe suppression level (SSL). For fixed antenna array geometry, SSL is sensitive to phase errors in beamforming weights. We assume i.i.d. Gaussian phase error with zero mean and finite variance σ^2. For example, consider a millimeter wave system operating at 60 GHz. A timing error of $\Delta_t = 1ps$ corresponds to phase error with $\sigma = 2\pi f \Delta_t = 0.12\pi$. SSL remains constant when phase error variance is low and it increases linearly after certain threshold. This threshold is termed as sidelobe suppression breakpoint σ_{SB}. As SSL increases linearly after σ_{SB}, imaging system resolution is sensitive to phase noise. Due to linear increase in SSL with the σ, the sidelobes start competing with the mainlobe. As further increase in σ will result into tilt in the positions of the mainlobe and sidelobes, it is difficult to determine their power accurately. Hence, the presented analysis is only valid for low phase noise variance. Our aim is to derive an analytical expression for σ_{SB} in terms of number of antenna elements (N). Figure 1 indicates logarithmic relation between σ_{SB} and number of antenna elements. As $\sigma_{SB} = 0.69 \log_{10} N - 0.25$, as number of antenna elements take higher value the growth in the σ_{SB} is not proportional.

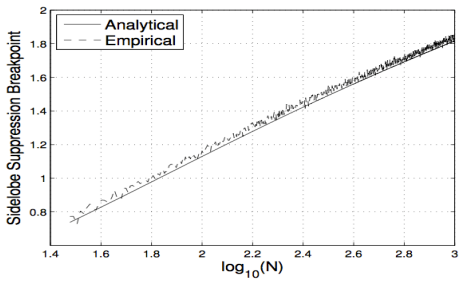

Figure 1: Relation between sidelobe suppression breakpoint against the antenna array size

To validate our analytical result, consider an active beamforming imaging system with transmit and receive beamforming. In an ideal system there exists no error in the beamforming weights, thus transmit and receive beams are steered in exactly same direction providing maximum normalized gain. Left hand side of figure 2 shows that beamformer remains directional below σ_{SB}, however loses its directionality above σ_{SB}.

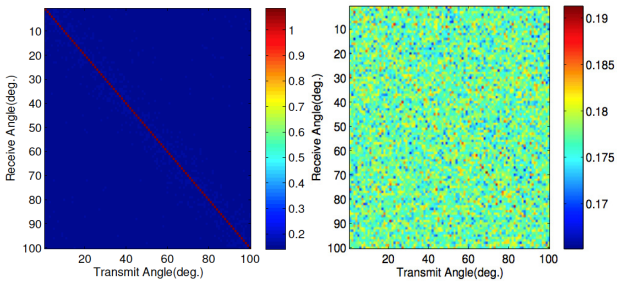

Figure 2: Normalized gain of the transmit receive beamformer 2 dB below (left) and above (right) sidelobe suppression breakpoint

Keywords: phase error, coherent imaging, antenna array, sensitivity analysis, and envelope probability distribution function

INDUSTRY INTERACTIONS

Texas Instruments, IBM

MAJOR PAPERS/PATENTS

[1] S. Patole and M. Torlak, "Sensitivity Analysis of Beamforming Applied to Coherent Imaging Systems," submitted, IEEE GlobalSIP Conf, Dec. 2013, Austin TX.

TASK 1836.119, DEMONSTRATION OF 180-300 GHZ TRANSMITTER FOR ROTATIONAL SPECTROSCOPY

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SIGNIFICANCE AND OBJECTIVES

As part of the effort to help open up high millimeter and sub-millimeter wave frequency range for moderate volume and cost applications, this task is seeking to demonstrate a 180-300 GHz transmitter in CMOS for a rotational spectrometer that detects harmful molecules and analyzes breath.

TECHNICAL APPROACH

The transmitted power should be ~10-100 μW. The main challenge is increasing the output frequency range, power, and frequency for phase locked signals. To realize a fast scan rate with a 10-kHz step, use of a fractional-N synthesizer is being investigated. The synthesizer will also incorporate a frequency modulation function. The output signal is generated using a combination of an N-push technique and a frequency multiplication technique. This task will also help generating the receiver LO signal.

SUMMARY OF RESULTS

To examine the feasibility of phase locking 300-GHz signal, a 195-GHz frequency-divide-four circuit driven by a 195-GHz oscillator with a 390-GHz push-push output is fabricated in TI 45-nm CMOS (Figs. 1 & 2). The divider successfully locked to 192.2-195.5 GHz indicating that it is possible to phase lock 390 GHz signal in CMOS. The measured radiated output power was also increased to 2 μW at 385GHz.

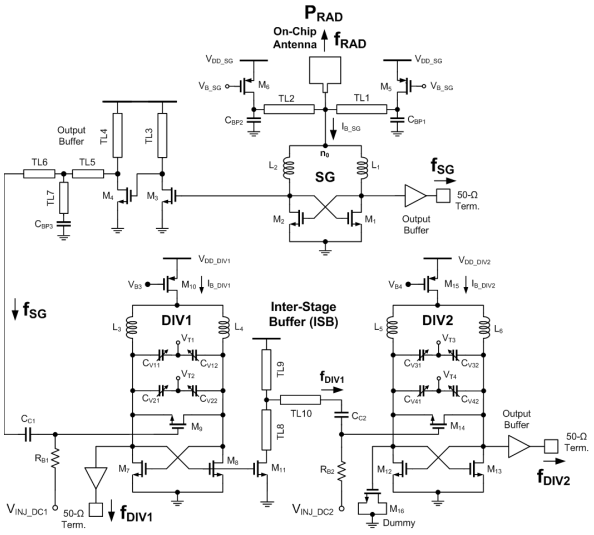

Figure 1: Circuit schematic of component chain for 390-GHz phase locked loop (PLL).

The output power and locking range of 390-GHz oscillator is still too low for the spectroscopy applications.

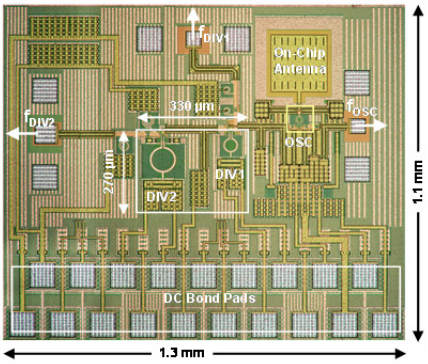

Figure 2: Die photograph of component chain for 390-GHz PLL.

To generate signals at 180-300 GHz, a transmitter architecture in which signals at 90-150 GHz is generated by a single oscillator followed by an amplifier and a frequency multiplier proposed. A wide-tuning LC-VCOs coupled with a passive quadrature coupling and phase combining network was fabricated in a 65-nm 6LM CMOS process. The circuit generated signals between 87 and 134.8 GHz. The frequency tuning range is ~7X higher than other CMOS oscillators operating over 90 GHz. The circuit consumes 30~45 mW from a 1.5 V supply.

Keywords: rotational spectrometer, transmitter, CMOS, millimeter-wave.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] E. Seok et al., "Paths to Terahertz CMOS Integrated Circuits," IEEE J. of Solid State Circuits, vol. 45, no. 8, pp. 1554-1564, August 2010.

[2] D. Shim et al., "553-GHz Signal Generation in CMOS Using a Quadruple-Push Oscillator," 2011 IEEE VLSI Symp. on Circuits, pp 154-155, June 2011, Kyoto, Japan.

[3] D. Shim et al., "Components for Generation and Phase Locking 390-GHz Signal in 45-nm CMOS," IEEE VLSI Symp. on Circuits, pp. 10-11, June 2012, Honolulu, HI.

TASK 1836.120, EVALUATION OF FREQUENCY AND NOISE PERFORMANCE OF CMOS 180 – 300 GHZ SPECTROMETER TRANSMITTER AND RECEIVER COMPONENTS

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SIGNIFICANCE AND OBJECTIVES

A gas phase absorption spectrometer in the 300 GHz range would be extremely valuable to rapidly and precisely assay a wide range of chemical vapors. This project's objective is to quantitatively evaluate materials and devices for suitability as millimeter-wave CMOS components to be integrated into such a spectrometer system.

TECHNICAL APPROACH

The first six months of this project undertook two tasks: (1) assembling capability to measure accurately low levels of transmitter power through free space, and (2) using Fourier transform spectroscopy (FTS) to evaluate dielectric characteristics of passive material components through the relevant frequency range. In (1), a photo-acoustic absolute power meter was built that covers 30 GHz to 3 THz with NEP of ≤ 5 μW/Hz$^{1/2}$. In (2), broadband reflection and transmission FTS was used to measure the dielectric function magnitude and loss tangent of FR4, a candidate substrate for millimeter-wave antennas and circuits, from 150 GHz to 70 THz.

SUMMARY OF RESULTS

An vital piece of this project in the next two years will be to quantitatively determine the free-space power characteristics of advanced CMOS sources transmitting across the 180 to 300 GHz range. For this purpose, a photoacoustic absolute power meter was built. This power meter is capable of measuring < 10 μW of coherent continuous-wave power at any frequency between 30 GHz and 3 THz. The absolute accuracy of this power meter is better than 10%, and it includes an internal self-calibration capability.

The power meter absorbs incident modulated light power to generate (via periodic heating) standing sound waves at twice the modulation frequency in a layer of trapped air. A pressure transducer senses the amplitude and frequency of the sound waves, and lock-in detection is used to record the amplitude, which is proportional to the light power absorbed. Calibration is provided by using a known resistive heater to generate sound waves in the air layer. The window of this power meter can be oriented at the Brewster angle to a properly polarized incoming light wave. This guarantees 100% absorption and hence no reflected power adjustment to the measured power, greatly enhancing accuracy.

Dr. Rashaunda Henderson's group is interested in the potential applicability of FR40x glass-epoxy laminates as substrates for transmitter/receiver antennas and waveguides for this project. Thus, it is necessary to know the materials' dielectric values and loss properties, but these are not reported in the literature above 30 GHz. FTS methods were thus used to measure these critical characteristics for FR406 and FR408 in the frequency range of 150 GHz up to 70 THz. By measuring both reflection and transmission across this broad range of frequencies, the full complex dielectric function was obtained. A graph of the real dielectric constant and loss tangent of FR406 as a function of frequency is shown in Fig. 1. From this data, it is evident that the loss tangent remains approximately constant at 0.02 up to ~500 GHz, but soars above that. As a consequence, this material is marginally useful for antenna or waveguide applications at 300 GHz, but is clearly unsuitable above 500 GHz.

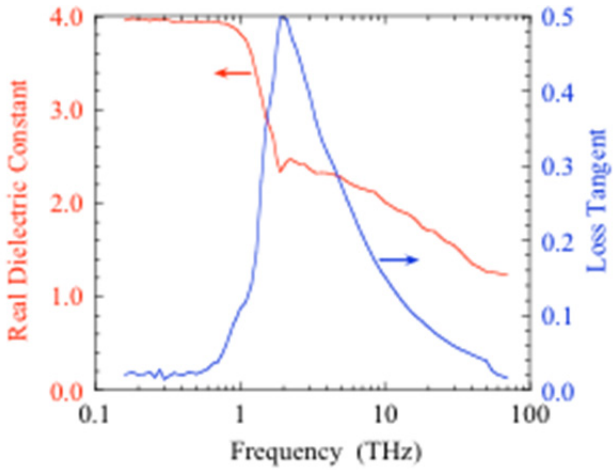

Figure 1: Graph of the measured real dielectric constant (red) and loss tangent (blue) of FR406 (from Isola) as a function of frequency. Measurements were made via Fourier transform spectroscopy.

Keywords: Millimeter-wave, Terahertz, Spectrometer, Dielectric loss, Power meter

INDUSTRY INTERACTIONS

MAJOR PAPERS/PATENTS

[1] S. Aroor, R. Henderson, B. L. Brown, M. Lee, "Evaluation of FR4 laminates for millimeter-wave and terahertz circuit applications," (in preparation, 2013)

TASK 1836.121: DEMONSTRATION OF 180 – 300 GHZ RECEIVER FOR ROTATIONAL SPECTROSCOPY

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SIGNIFICANCE AND OBJECTIVES

This work focuses on developing CMOS integrated receiver for spectrometer covering 180GHz-300GHz frequency band. CMOS integrated receiver with on-chip antenna will be demonstrated for 180 – 300 GHz rotational spectroscopy for gas sensor application in collaboration. Active and passive mixers, filters, and low noise IF amplifiers will be developed and integrated to develop a direct conversion receiver with an overall noise figure < 20 dB.

TECHNICAL APPROACH

In order to optimize the overall system performance, multiple architectures are analyzed and explored. The overall system Noise Figure achieved is < 18dB for an input RF power of -50dBm for direct down conversion receiver. Figure 1 shows the overall receiver system architecture. The key building block for the receiver is the front-end mixer. With current CMOS technology it is not possible to design active mixers using transistors at these frequencies. However, the high cut-off frequencies of Schottky Barrier Diodes (SBDs) in standard CMOS technology, allows us to design anti-parallel-diode-pair (APDP) based subharmonic passive mixers covering the 180-300 GHz bands. Fig. 2 shows the schematic and simulation result of the improved passive mixer. Fig. 3 shows the schematic and simulated performance of the transistor based active mixer at 180 GHz.

SUMMARY OF RESULTS

Active and Passive (APDP) mixers, for 180-300 GHz bands, have been designed and submitted for fabrication in UMC 90nm CMOS Technology. The passive mixer has a maximum voltage gain of -3 dB, and the active mixer has a maximum gain of -5 dB.

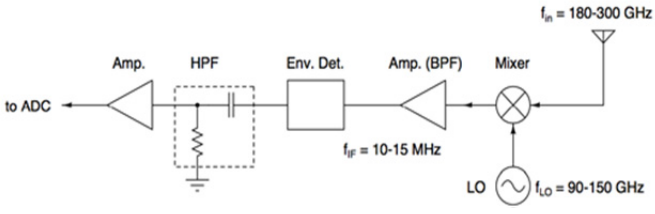


Figure 1: The overall receiver architecture.

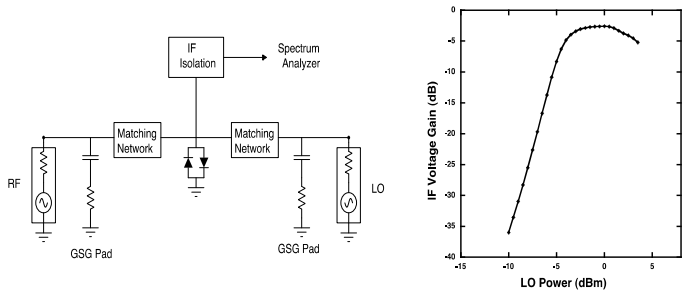
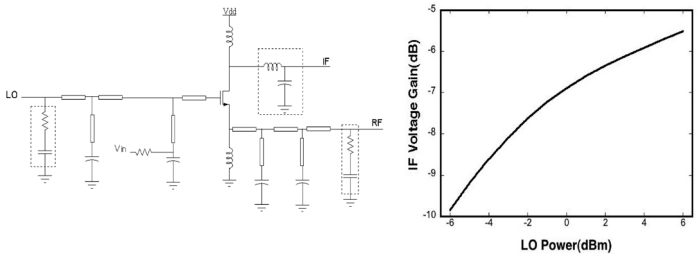


Figure 2. Schematic and conversion gain for an improved APDP mixer at 200 GHz.



In the next six months, the project will focus on measuring the improved mixer and finalizing the receiver architecture.

Figure 3. Schematic and conversion gain for an active CMOS mixer at 200 GHz.

Keywords: THz CMOS, spectroscopy, APDP Mixer.

Keywords:

INDUSTRY INTERACTIONS

Texas Instruments, Intel, IBM Research

MAJOR PAPERS/PATENTS

[1] M. F. Hanif, et. al., "Development of CMOS Sub-THz Receivers for Spectrometer", SRC Techcon 2011, 2012.

[2] M. F. Hanif, et. al., "200 GHz CMOS APDP Mixer," under review IEEE MWCL.

TASK 1836.122, ON-CHIP INTEGRATION TECHNIQUES FOR 180-300 GHZ SPECTROMETERS

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ANDREW BLANCHARD, UT DALLAS,

SIGNIFICANCE AND OBJECTIVES

The objectives include design and fabrication techniques to integrate a CMOS-based gas spectrometer with on-chip broadband planar aperture antennas.

TECHNICAL APPROACH

The approach uses coplanar waveguide (CPW) interconnects fabricated in a post-IC technology and a planar aperture bowtie antenna that uses electromagnetic band gap (EBG) structures to improve radiation performance. The fabrication techniques to achieve dielectric polymer heights up to 200 micrometers will be explored. The design of interconnects and vertical transitions will be carried out using ANSYS HFSS. If successful, this technology can lead to the design of affordable gas spectrometers that can be used for safety and security applications.

SUMMARY OF RESULTS

Many researchers have explored CMOS circuit design at sub-millimeter wave frequencies in the last 10 years. Techniques to integrate the ICs with planar radiators has also been demonstrated where the antennas are fabricated in the back end of line (BEOL) using interlayer dielectric (ILD) and metal stacks that are up to 9 micrometers away from the lossy silicon substrate. Resulting bandwidth and gain is low for planar microstrip patch and dipole antennas.

This research involves combining broadband antenna design with post-IC processing techniques to realize planar antennas fabricated on-chip in the presence of the silicon substrate. The antennas are separated from the lossy silicon substrate by using thick layers of polymer dielectrics like benzocyclobutene (BCB) and SU-8. The planar aperture bowtie antenna has been demonstrated at 6 and 60 GHz on laminate substrates and shows up to 50% bandwidth when printed on a single layer and radiating in both hemispheres.

When the antenna is positioned in the vicinity of a CMOS substrate, a ground plane reflector is used to prevent energy from radiating into the silicon. The distance between reflector and antenna is $\lambda/4$. Polymers are being used to support the aperture antenna and create the thicknesses on-chip. These thicknesses can be as high as 200 micrometers at 200 GHz and also lead to unwanted surface waves. An EBG material does not support propagating modes and can combat the surface wave issue. A mushroom EBG as shown in Figure 1 (for 60-90 GHz antenna operation) has been incorporated with the reflector ground to improve the planar aperture radiation performance. Table 1 shows the simulated 10 dB return loss bandwidth is the same for an antenna with and without an EBG ring. A gain of 8 dB can be achieved.

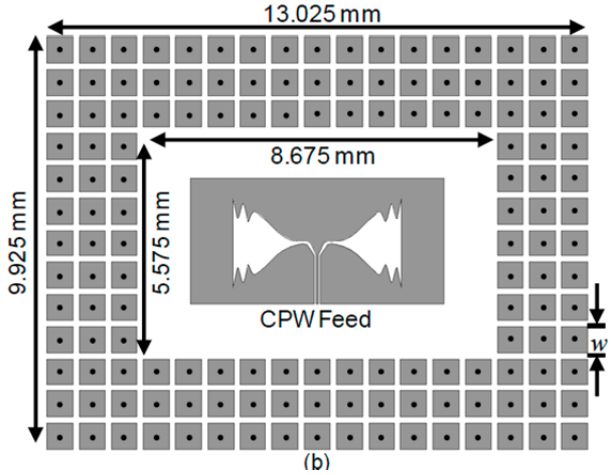


Figure 1: Top view of CPW fed aperture antenna with EBG.

The bandwidth of the simulated antenna gain is improved from 8 to 17 GHz by incorporating the EBG and reflector. SU-8 has been demonstrated in MEMS technology and provides polymer thicknesses up to 200 GHz. The BCB has been shown to provide low loss.

Table 1: Transition losses (dB) at frequency (GHz)

Design	*10 dB Return Loss BW*	*Gain*	*Gain BW (GHz)*
No EBG ring	32%	8	55 – 72
With EBG ring	32%	8	62 - 70

The multilayer via process required for this integration has been studied along with the fabrication of the EBG structure.

Keywords: aperture antennas, BCB, CMOS, CPW, post-IC

INDUSTRY INTERACTIONS

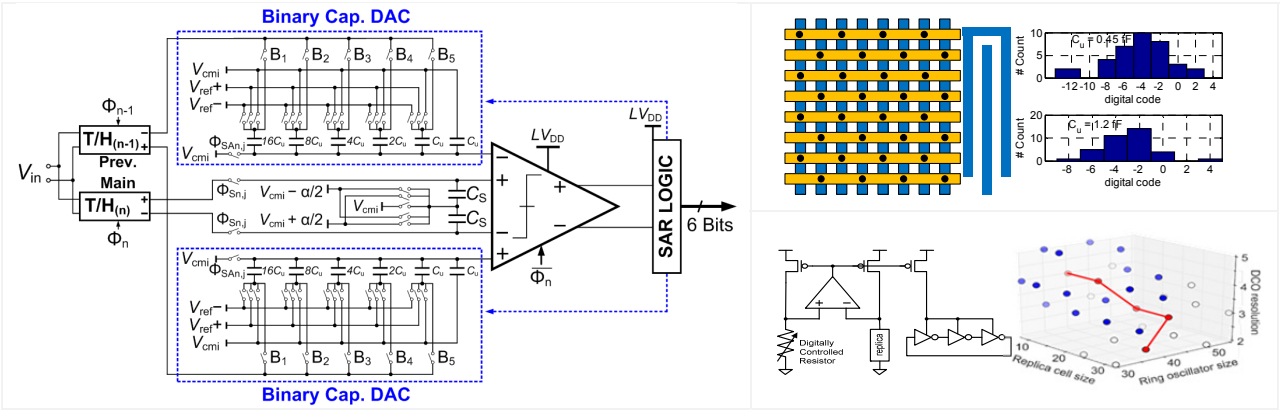
Texas Instruments (Django Trombley, Baher Haroun)

MAJOR PAPERS/PATENTS

[1] R. Islam & R. M. Henderson, “Minimizing attenuation of coplanar waveguide on lossy silicon substrates up to 300 GHz,” 2013 IMS, June 2013, Seattle, WA.

[2] R. Pierce, et al., “Broadband millimeter wave aperture bowtie antenna-in-package,” 2013 WMCS, April 2013, Waco, TX.

Fundamental Analog Thrust



Summary of Accomplishments

Category	Accomplishment
Fundamental Analog	ADC-based high-speed serial links aim to improve interconnect bandwidth density in an energy-efficient manner. Embedding the normally required channel equalization within the ADC has the potential for significant power savings. The first 10Gs/s ADC with embedded FFE/DFE that achieves a BER of 10^{9} at 10Gb/s over a 10" channel is demonstrated. The 6bit ADC has an FOM (0.48pj/c-s) that is as competitive as the FOM of plain vanilla ADCs that operate at that speed. (1836.111, PI: S. Palermo, Texas A&M University) Publication: E. Zhian Tabasy, A. Shafik, K. Lee, S. Hoyos, S. Palermo "A 6b 10GS/s TI-SAR ADC with Embedded 2-TAP FFE/1-Tap DFE in 65nm CMOS," IEEE VLSI Sym., June 2013. (Winner best in session at Techcon 2013)
Fundamental Analog	Successive approximation register (SAR) ADCs, are extremely flexible (6-12 bits), have the potential to consume the lowest power and can be made to operate that reasonably high speeds by using time interleaving (~10Gsps). However, this requires extremely small capacitor values. This project investigated the matching limit of small metal fringe capacitors. Measured results from a 65nm CMOS process show excellent matching (1 sigma) of 1.2% can be achieved for 0.45fF capacitors with a Pelgrom coeff of ~0.85% at 1fF. This opens up the field for extremely low power high-speed ADCs using SARs. (1836.078, PI: B. Murmann, Stanford University) Publication: V. Tripathi and B. Murmann, "Mismatch Characterization of Small Metal Fringe Capacitors," IEEE Custom Integrated Circuits Conference 2013, San Jose, CA
Fundamental Analog	This task explores the use of discrete optimization techniques for variability-aware analog circuit synthesis. Discretization of the analog design space exploiting the inherent variability in the IC process can lead to a fast, deterministic optimizer that can perform quick, incremental 'what-if' analyses. This research has been able to justify the exploration of discrete spaces even for analog designs allowing a new era of analog CAD tools that can utilize efficient algorithms and approaches that have up until now been relegated to digital CAD tools. (1836.085, PI: J. Kim, Seoul National University) Publications: J. Kim, et al., "Discretization and Discrimination Methods for Design, Verification, and Testing of Analog/Mixed-Signal Circuits," IEEE Custom Integrated Circuits Conference (CICC) 2013.

TASK 1836.057, HIGH ACCURACY ALL-CMOS TEMPERATURE SENSOR WITH LOW-VOLTAGE LOW-POWER SUBTHRESHOLD MOSFETS FRONT-END AND PERFORMANCE-ENHANCEMENT TECHNIQUES

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SIGNIFICANCE AND OBJECTIVES

This project investigates scattered temperature sensor based on subthreshold-MOSFETs and Schottky barrier diodes for on-chip thermal management, aiming to achieve low supply voltage, small chip size and high accuracy with no or minimal calibration/trimming.

TECHNICAL APPROACH

For low supply voltage, subthreshold MOSFETs, Schottky barrier diodes, and bulk-driven technique are used. Dynamic element matching (DEM), dynamic offset cancellation (DOC) and gain boosting are applied to the sensor to minimize device mismatch induced errors. One-point low-cost digital trimming is optional to further improve the accuracy of the sensor. Low-voltage low power inverter-based sigma-delta modulator is investigated for temperature reading. Furthermore, scattered thermal monitors with small sensing diodes distributed across the chip featuring high accuracy relative temperature measurement are reported.

SUMMARY OF RESULTS

A 5×5 subthreshold MOSFETs-based scattered relative temperature sensor front-end was implemented in 0.5 µm CMOS process, as shown in Fig. 1 (a). DEM and DOC are used to minimize the errors induced by device mismatches. A gate-bulk-driven error correction amplifier is proposed to minimize the offset error and maintain low voltage operation. The minimum supply voltage was 1 V over -40-100 ^{0}C, with a typical N-/P-threshold voltage of 0.8 V and 0.9 V at room temperature, respectively. Fig. 1 (b) shows the measured 3σ relative inaccuracy, which is less than ±2.5 ^{0}C without any calibration or trimming. To our knowledge, this is the first time that non-calibrated on-chip relative temperature monitoring accuracy is reported. The multi-location thermal monitoring function has been experimentally demonstrated and a 2 ^{0}C/mm on-chip temperature gradient was detected. Fig. 1 (c) shows the measured on-chip thermal map when a corner hot spot was turned on.

A 3×3 low-voltage temperature sensor with a regulated current mirror structure and 46×23 µm^2 sensor node size was also developed for superior line sensitivity. Measurement shows a 0.45 V supply voltage over -55-105 ^{0}C in a 90 nm process, and a ±3.5 ^{0}C 3σ relative inaccuracy without any calibration/trimming. The sensor can monitor a 2.2 ^{0}C/mm on-chip temperature gradient.

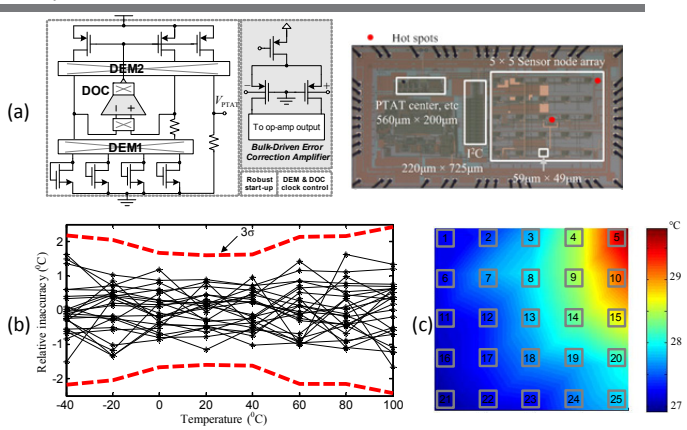

Figure 1: (a) PTAT generator and the chip photo. (b) Measured temperature inaccuracy without any calibration or trimming. (c) Chip thermal map when the corner hot spot is turned on.

For digital temperature reading, a fully-differential inverter-based switched-capacitor sigma-delta modulator was investigated. To reduce the supply voltage, power consumption and chip area, a simple inverter is used as the integrator. A prototype fabricated in 0.5 µm CMOS has a measured 1.5 V supply voltage and 55.39 dB SNDR. Simulation also shows that the modulator can work under 0.7 V with 59.38 dB SNDR in IBM 180 nm CMOS.

Keywords: subthreshold MOSFETs, Schottky barrier diode, scattered temperature sensor, low voltage, multi-location thermal monitoring

INDUSTRY INTERACTIONS

Intel, IBM, Freescale, Globalfoundries.

MAJOR PAPERS/PATENTS

[1] L. Lu, et al., "A subthreshold-MOSFETs-based scattered relative temperature sensor front-end with a non-calibrated ±2.5 ^{0}C 3σ relative inaccuracy from -40 ^{0}C to 100 ^{0}C," IEEE TCAS-I, vol. 60, no. 5, May 2013.

[2] L. Lu, et al., "A 0.45 V MOSFETs-based temperature sensor front-end in 90nm CMOS with a non-calibrated ±3.5 ^{0}C 3σ relative inaccuracy from -55 ^{0}C to 105 ^{0}C," IEEE TCAS-II, minor revision, 2013.

[3] L. Lu, C. Li, "Offset error reduction using a gate-bulk-driven error correction amplifier for a low-voltage subbandgap reference," IET Electronics Letters, vol. 49, no. 11, May 2013.

[4] Y. Yang, et al., "An inverter-based second-order sigma-delta modulator for smart sensors," IET Electronics Letters, vol. 49, no. 7, March 2013.

TASK 1836.058, HIERARCHICAL MODEL CHECKING FOR PRACTICAL ANALOG/MIXED-SIGNAL DESIGN VERIFICATION

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SIGNIFICANCE AND OBJECTIVES

Analog/mixed-signal (AMS) verification has grown in importance as the AMS design complexity increases and verification becomes a significant bottleneck in design. This project aims to address the grand challenges in AMS verification by developing a variety of techniques including hierarchical analog behavioral model equivalence checking, formal and semi-formal methods and machine-learning guided verification.

TECHNICAL APPROACH

Many formal verification methods are not scalable due to the inherent computational complexity associated with the verification of analog and mixed-signal circuits. Recently, we have been primarily working on two types of techniques to address the above challenge: machine learning and circuit-specific modeling. The use of these two techniques has allowed us to significantly speed up the challenging transient verification of several AMS designs such as PLLs.

SUMMARY OF RESULTS

We have developed a novel active-learning guided machine learning approach to building circuit performance classifiers for design property checking as shown in Figure 1. When employed under the context of support vector machines (SVMs), the proposed probabilistically weighted active learning approach is able to dramatically reduce the size of the training data, leading to about 10X reduction of overall training cost.

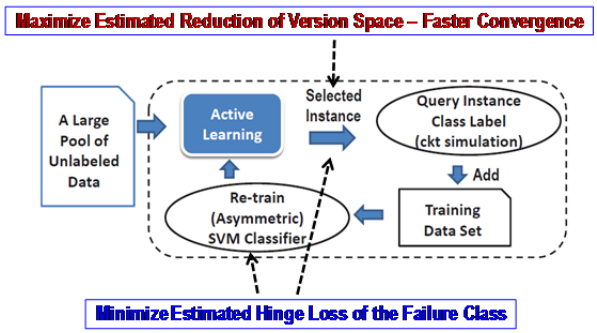

Figure 1: Active-learning guided training of SVM classifiers.

The proposed active learning approach is extended to the training of asymmetric support vector machine classifiers, which is further sped up by a global acceleration scheme. We have demonstrated the excellent performance of the proposed techniques for several applications including charge-pump PLL lock-time verification and SRAM yield analysis.

In a related direction, we have looked that the verification challenges brought by the emergence of digitally-intensive analog circuits due to their increased digital design content and non-ideal digital effects such as finite resolution effects. We propose a machine learning approach to convert digital blocks to conservative analog approximations via the use of kernel ridge regression. These learned models are then adopted in a hybrid formal reachability analysis framework where the support function based manipulations are developed to efficiently handle the large linear portion of the design and the more general satisfiability modulo theories technique is applied to the remaining nonlinear portion. This approach has sped up the lock time verification of a digital PLL against uncertain initial conditions by more than 70X (Figure 2). Without the proposed techniques, the verification would have been impossible.

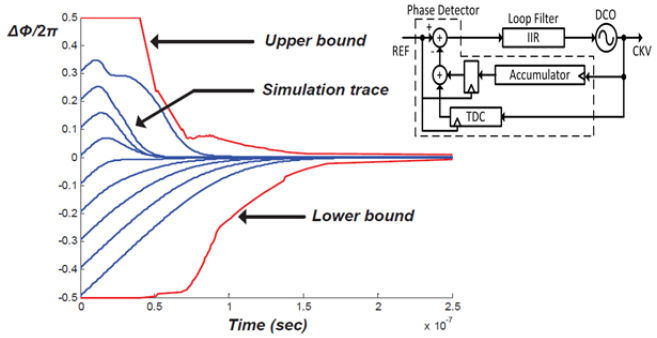

Figure 2: Reachability analysis for a digital PLL for lock time verification: phase error as a function of time.

Our future work will focus on extending the learning guided verification and developing parallel techniques.

Keywords: verification, analog and mixed-signal, reachability analysis, machine learning, formal methods

INDUSTRY INTERACTIONS

Intel, Freescale, Texas Instruments

MAJOR PAPERS/PATENTS

[1] H. Lin, P. Li and C. Myers, "Verification of digitally-Intensive analog circuits via kernel ridge regression and hybrid reachability analysis," IEEE/ACM DAC, 2013.

[2] H. Lin and P. Li, "Classifying circuit Performance using active-learning guided support vector machines," IEEE/ACM ICCAD, Nov. 2012.

TASK 1836.059, POWER-EFFICIENT 10-20GS/S ADCS FOR HIGH-SPEED COMMUNICATIONS

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SIGNIFICANCE AND OBJECTIVES

Next generation high-speed communication systems demand wide-bandwidth ADCs with sampling rates beyond 10GS/s. This research will focus on investigating new design techniques to significantly lower the power consumption of high-speed ADCs, while achieving sufficient effective resolution across the Nyquist frequency band.

TECHNICAL APPROACH

This research will investigate using time-interleaved flash converters to achieve 10-20GS/s sampling rates. As flash ADCs generally offer much higher speed than other architectures, a smaller interleaving factor can be used to achieve the desired speed. With a smaller interleaving factor, degradations of the ENOB at high frequencies and the FOM in the complete ADC will be improved. The accuracy of a flash ADC in CMOS is dominated by random offsets of comparators due to device mismatches. Using offset calibration, smaller devices can be used to achieve the desired accuracy leading to better FOM. New digitally controlled trimming offset calibration techniques to minimize the loading of the calibration devices on the critical signal path will be investigated.

SUMMARY OF RESULTS

In high-speed wire-line communication systems, ADC based receivers can allow more sophisticated equalization and complex timing recovery approaches in the following digital signal processors to enhance the spectral efficiency of transmission media. The key design challenge for these ADCs is to ensure sufficient effective resolution across the input signal bandwidth such that critical information of the received signal is preserved, while maintaining low power consumption. This calls for ADCs with high power-efficiency. To achieve larger than 10GS/s sampling rate in current CMOS technologies, the ADCs need to adopt time-interleaving architectures and require multi-phase clocks for the time-interleaved channels. Timing skew among the multi-phase clocks can degrades ADC effective resolution at high input frequencies, leading to degraded power efficiency. The state of the art >10GS/s ADC designs in CMOS have employed pipeline, SAR and flash sub-ADC architectures. This research proposes a new sub-ADC architecture, partially active flash (PA flash), is presented to achieve a better power efficiency. Also presented are a new source-follower based boot-strap track-and-hold (T&H) circuit to reduce the input kickback and interference among the interleaved channels and a multi-phase clock generation scheme with accurate timing skew calibration based on duty-cycle calibration. Compared with the state of the art ADCs with larger than 10GS/s sampling rate, this design achieved a better power efficiency with a FOM of 197fJ/conv-step in the same technology, while achieving better resolution.

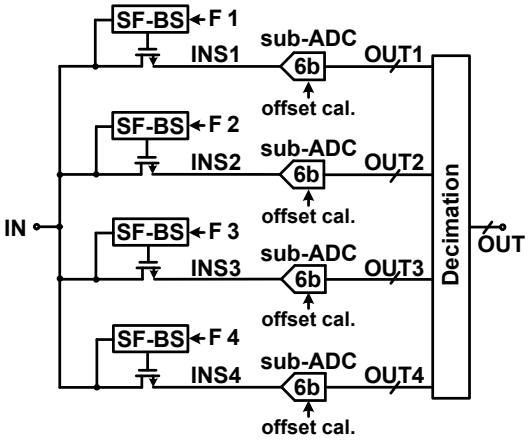

Figure 1: Block diagram of the 10GS/s four-way time-interleaved ADC.

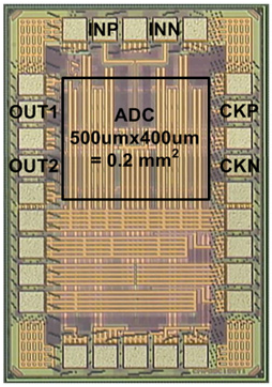

Figure 2: Chip micrograph.

Keywords: ADCs, partially-active flash

INDUSTRY INTERACTIONS

Texas Instruments, Intel, Freescale, IBM

MAJOR PAPERS/PATENTS

[1] X. Yang et al., "A 10GS/s 6b Time-Interleaved ADC with Partially Active Flash sub-ADCs," in *proc. IEEE CICC*, 2013.

TASK 1836.075: DESIGN OF 3D INTEGRATED HETEROGENEOUS SYSTEM

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SUNG-KYU LIM, GEORGIA INSTITUTE OF TECHNOLOGY

SIGNIFICANCE AND OBJECTIVES

The objective of this research is to address the challenges to 3D integration of highly different circuits/systems with varying technology, power profiles, operating voltage, and clock domains through the 3D technology using Through-Silicon-Via (TSV).

TECHNICAL APPROACH

The performance, power, and reliability of a 3D-Integrated Heterogeneous System (3D-IHS) depend on the functionality, power profile, and frequency of individual dies; the non-uniformity in their physical environments; die-to-die coupling; and die-to-package coupling. This research will develop design methods for the 3D-IHS and transform them into design tools and silicon prototype. The technical approach integrates modeling, circuit techniques, and physical design to deliver design tools and silicon prototype.

SUMMARY OF RESULTS

- Variation Analysis for 3D ICs [1, 2]: We have studied the effect of variations on logic path as well as in the clock distribution network. As different tiers in a 3D IC come from different wafers, there exist larger tier-to-tier variations. When a logic path is partitioned between two tiers (3D paths), depending on the location of the TSVs, the overall delay variation can be reduced compared to the 2D path. Therefore, 2D paths suffer more than 3D paths under uncorrelated tier-to-tier variations. The analysis on the clock skew variability shows that, the uncorrelated tier-to-tier variations significantly degrade the 3D skew i.e. the skew between two clock leaves in two tiers, and the 2D clock skew is less impacted.
- Post-silicon Tuning of 3D ICs [1, 2]: We have developed methods for post-silicon tuning of the 3D ICs. First, we have developed ring-oscillator based circuits to characterize the process induced shifts in delay as well as individual variations in PMOS and NMOS devices. Second, we have proposed tier-adaptive-voltage-scaling (TAVS) as a post-silicon tuning methodology where optimal supply voltages are applied to different tiers using on-chip process detection and voltage regulation circuits to minimize the delay variations. Finally, we have studied tier-adaptive-body-biasing (TABB) to minimize variation in clock skew. In TABB, the optimal body biases are applied to both PMOS and NMOSs in each die to minimize variations in clock skew and slew. The effect of TABB on logic delay variation is analyzed.
- TSV-to-TSV coupling extraction and mitigation [3]: TSV-to-TSV coupling is a new parasitic element in 3D ICs and can become a significant source of signal integrity problem. Existing studies on its extraction, however, becomes highly inaccurate when handling more than two TSVs on full-chip scale. We investigated the multiple TSV-to-TSV coupling issues and proposed an accurate model that can be efficiently used for full-chip extraction. Unlike the common belief that only the closest neighboring TSVs affect the victim, our study shows that non-neighboring aggressors also cause non-negligible impact. Based on this observation, we propose an effective method of reducing the overall coupling level in multiple TSV cases.

Sub-threshold 3D micro-controller [4]: We studied a 3D IC micro-controller implemented with sub-threshold supply for ultra-low power (ULP) applications. Our study is based on GDSII layouts of a sub-threshold 8052 micro-controller that consumes 3.6uW power running at 20 KHz clock frequency and 0.4V logic supply. Our 3D sub-threshold design reduces the footprint area by 78% and wirelength by 33% compared with the 2D counterpart. Our studies also show that thermal and IR drop issues are negligible in this sub-threshold 3D implementation due to its extreme low power operation. Lastly, we demonstrate the low power and high memory bandwidth advantages of many-core 3D sub-threshold circuits.

Keywords: 3D IC, Post-silicon tuning, Signal Integrity, Variation, Ultra low power (ULP)

INDUSTRY INTERACTIONS

Globalfoundries, IBM, and Intel Corporation

MAJOR PAPERS/PATENTS

[1] K. Chae et. al, “Tier-Adaptive-Voltage-Scaling (TAVS): A Methodology for Post-Silicon Tuning of 3D ICs,” ASP-DAC 2012.

[2] K. Chae, et. al, “Tier-Adaptive-Body-Biasing: A Post-Silicon Tuning Method to Minimize Clock Skew Variations in 3D ICs,” IEEE TCPMT (accepted).

[3] T. Song, et al, “Full-Chip Multiple TSV-to-TSV Coupling Extraction and Optimization in 3D ICs,” DAC 2013.

[4] S. Samal, et al, "Design and Analysis of Ultra Low Power Processors Using Sub/Near-Threshold 3D Stacked ICs", ISLPED 2013.

TASK 1836.077, STATISTICAL CHARACTERIZATION OF CIRCUIT AGING

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SIGNIFICANCE AND OBJECTIVES

The impact of RTN on ring oscillator (ROSC) frequency was measured for the first time on 65nm technology using an on-chip beat frequency detection system [1]. The proposed differential sensing scheme effectively detects RTN induced frequency shift by enabling a high frequency measurement resolution (>0.01%) at a short sampling time (>1μs).

TECHNICAL APPROACH

In prior works, actual RTN impact on logic circuit has seldom being characterized due to the difficulty of taking high precision measurements in a short measurement time [2]. The basic concept of the beat frequency detection odometer technique [3] is to measure the frequency difference between two ROSCs. This differential structure is insensitive to the common mode noises such as temperature and voltage drifts. Therefore, a high precision measurement on RTN induced frequency shift can be readily achieved down to a microsecond, making it ideally suited for characterizing RTN effects in logic paths.

SUMMARY OF RESULTS

Detail of the beat frequency detection odometer technique is illustrated in Fig. 1. The odometer samples the output of one oscillator using a D flip-flop at intervals set by the output of the other. The faster signal A catches up and then overtakes the slower signal B, and as this process repeats, the time between the overlapping points is the period of the beat frequency. This time is measured by counting the number of reference ROSC periods during a single beat period. This information is then read out through a scan based interface.

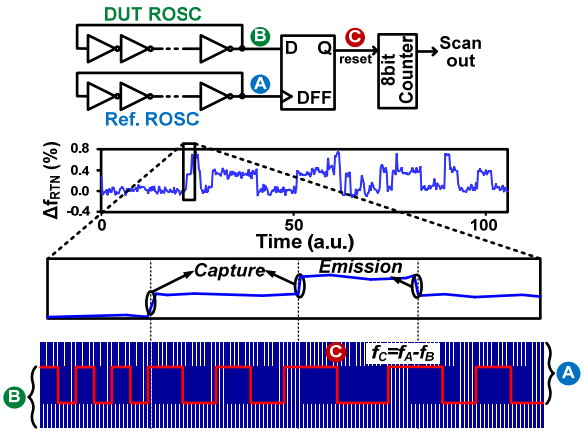

Figure 1: Beat frequency technique proposed for RTN measurements. A high frequency shift resolution (>0.01%) and a short (>1μs) measurement time can be achieved.

The frequency shift waveforms in Fig. 2 are from three different ROSCs in the test array. RTN's signature trapping/de-trapping behavior can be clearly observed. Independent of the time constant values, the frequency shift caused by a single RTN trap was approximately 0.4% for the 11 stage ROSC operating at 0.8V and 25°C. Determined by number of traps, frequency shift transient waveforms with two levels are due to single trap whereas three-level frequency shift is cause by two traps (Fig.1). The emission and capture time constants (i.e. τ_e and τ_c) ranges from ~ms to ~100ms depending on the supply voltage and ROSC instance.

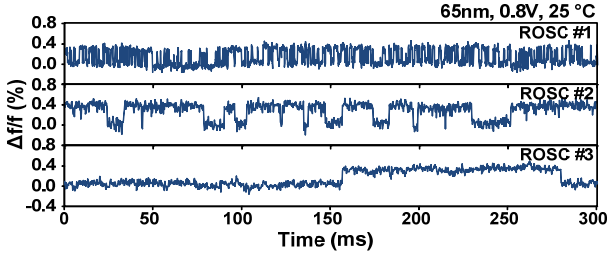

Figure 2: RTN waveforms measured from 65nm test chip.

RTN parameters are shown to have a strong voltage dependence which was experimentally verified from the test chip. As the supply voltage increases, percentage frequency shift due to RTN decreases and τ_e increases in PMOS while decreases in NMOS. Furthermore, τ_c and τ_e extracted from the distributions display opposite dependencies on supply voltage. In our experiment, the majority of ROSCs did not show any signs of RTN while no ROSC had more than 2 traps. The relatively low number of traps in each ROSC can be attributed to the mature process technology used for the test chip fabrication.

Keywords: RTN, ring oscillator, CMOS, logic circuit, frequency shift

INDUSTRY INTERACTIONS

Texas Instruments, Intel, IBM, Freescale

MAJOR PAPERS/PATENTS

[1] Q. Tang, et al., "RTN Induced Frequency Shift Measurements Using a Ring Oscillator Based Circuit", VLSI Symposium, June 2013

[2] K. Ito et al., "The Impact of RTN on Performance Fluctuation in CMOS Logic Circuits," IRPS 2011, April, 2011.

[3] T. Kim et al., "Silicon Odometer: An On-Chip Reliability Monitor for Measuring Frequency Degradation of Digital Circuits," IEEE J. of Solid State Circuits, April, 2008.

TASK 1836.078, HIGH-RESOLUTION, CHARGE-BASED A/D CONVERTERS FOR NANO-CMOS TECHNOLOGIES

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SIGNIFICANCE AND OBJECTIVES

The successive approximation register (SAR) ADC architecture is attractive for integration in aggressively scaled CMOS, primarily since it does not rely on linear amplification blocks. This project aims to push the performance of SAR ADCs, targeting both high resolution (~12bits) and high speed (>150MHz) in 65nm CMOS technology. These specifications are required e.g. in wireless base station receivers.

TECHNICAL APPROACH

Aggressive scaling of unit capacitances in a SAR ADC allows the designer to set the input capacitance according to the thermal noise limit, resulting in lower switching energy and faster conversion speed. As a first step, we investigated the matching limit of small metal fringe capacitors and fabricated a test structure to measure their mismatch characteristics. Next, in order to identify performance bottlenecks and thereby improve the conversion speed, we designed an 8 bit SAR ADC employing top plate sampling, loop delay optimization and asynchronous timing. Finally, SAR ADC pipelining together with learnings from the above two test chips was used to design a 12 bit, 200 MS/s A/D converter (to be taped out shortly).

SUMMARY OF RESULTS

Fig. 1 shows the measured mismatch characteristics of small metal fringe caps across 8 chips. For each chip, 72 test structures were measured (36 each for 0.45 fF and 1.2 fF unit capacitance) and the calculated average sample coefficient of variation (σ/μ) is 1.2% for 0.45 fF, and 0.8% for 1.2 fF unit capacitors, which is in accordance with Pelgrom's variance scaling law (σ^2~ 1/Area).

Fig. 2 summarizes the measurement results of the 8 bit SAR ADC obtained at f_s = 450 MHz. The DNL and INL are within ±1 LSB, which indicates good matching of the small unit capacitors (0.75 fF in this design). The measured SNDR is nearly flat with input frequency and the ADC achieves SNDR = 47.3 dB at Nyquist.

In the final design, we pipeline 2 SAR ADC's with an open-loop inter-stage amplifier. The measurement results from the first test chip helped us choose a small unit cap (sufficient for linearity) for the backend ADC, thereby reducing the residue amplifier load, and resulting in higher speed and lower power dissipation. The second test chip provided us with a methodology to design high speed, medium resolution (8 bits) SAR A/D converters, which can be pipelined together to realize a 12 bit ADC.

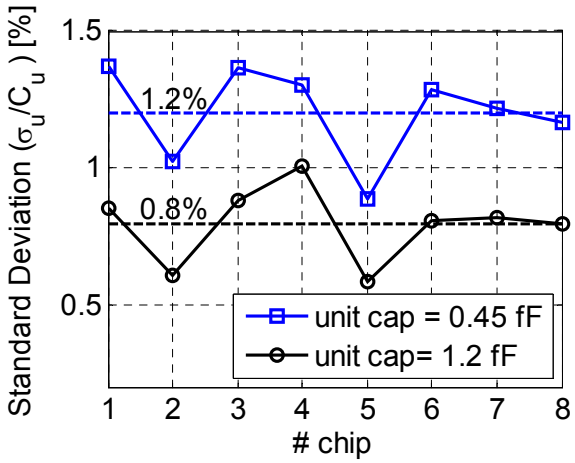

Fig.1: Capacitor mismatch measured across 8 dies.

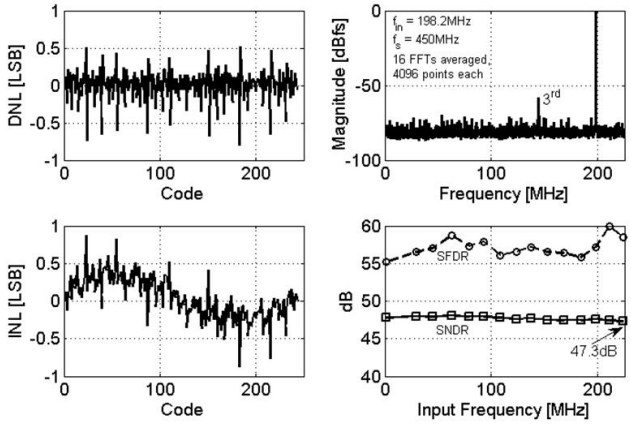

Fig.2: 8-bit SAR ADC measurement results.

Keywords: Capacitor matching, CMOS, Successive approximation, ADC

INDUSTRY INTERACTIONS

Texas Instruments, Intel, Freescale

MAJOR PAPERS/PATENTS

[1] V. Tripathi and B. Murmann, "An 8-bit 450-MS/s Single-Bit/Cycle SAR ADC in 65-nm CMOS," to appear at ESSCIRC 2013, Bucharest, Romania.

[2] V.Tripathi and B. Murmann, "Mismatch Characterization of Small Metal Fringe Capacitors," to appear at CICC 2013, San Jose, CA.

TASK 1836.080, VARIATION-TOLERANT NOISE-SHAPING ADCS WITH EMBEDDED DIGITAL BIAS AND V_{DD} SCALABLE FROM 0.5V TO 1.2V FOR NANOSCALE CMOS

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SIGNIFICANCE AND OBJECTIVES

We have demonstrated different design techniques and architectures for analog circuits down to 0.5V in earlier work. However, for some applications high performance interfaces with flexible supplies in deep-submicron CMOS are required. We are investigating such supply scalable analog interfaces with embedded digital biasing technique in this project.

TECHNICAL APPROACH

A sigma-delta modulator with pulse-controlled common-mode feedback biasing has been designed and fabricated to accomplish flexible, supply scalable operation in nano-scale CMOS. The sigma-delta modulator uses a continuous-time implementation to relax the sampling network requirement and to avoid signal path switches which cannot be operated at low supply voltage. A cascaded 2-1 structure sigma-delta architecture is used to simplify stability issues which are aggravated by the scalable supply voltage. A pulse-controlled common-mode feedback biasing is proposed to operate at flexible supplies and avoid the use of large-area passive components.

SUMMARY OF RESULTS

The architecture of the cascaded 2-1 continuous-time (CT) sigma-delta modulator (SDM) operating with a supply voltage from 0.6V to 1.2V is shown as Figure 1.

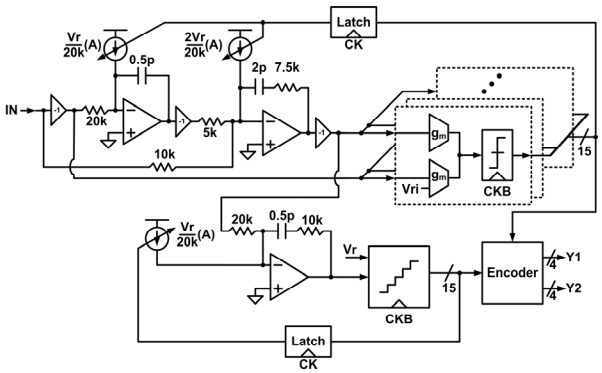

Figure 1: Architecture of the cascaded 2-1 CT SDM.

The novel proposed pulse-controlled common-mode feedback (CMFB) circuit shown in Fig. 2 results in a smaller area for the passive components without gain reduction of a main amplifier.

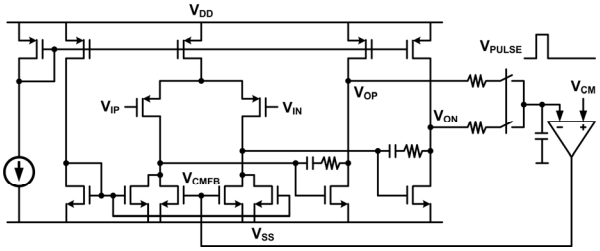

Figure 2: An amplifier with the pulse-controlled CMFB circuit

The CT SDM was fabricated in low-leakage/low power CMOS 65nm process with the active area is 0.14mm^2. The die photo is shown in Figure 3.

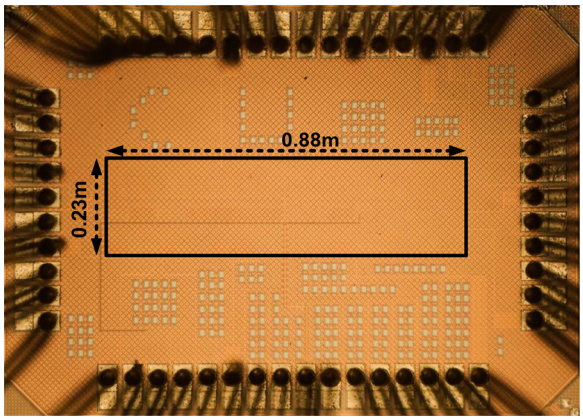

Figure 3: Die Photo of the CT SDM

The chip is currently being experimentally evaluated.

Keywords: Supply scalable amplifier, Continuous-time sigma delta modulator, Digital biasing

INDUSTRY INTERACTIONS

Texas Instruments, Freescale, Intel

MAJOR PAPERS/PATENTS

TASK 1836.085, CMOS SWITCHED-CAPACITOR POWER AMPLIFIER TECHNIQUES

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SIGNIFICANCE AND OBJECTIVES

A digitally-controlled switched-capacitor RF power amplifier (SCPA) uses a dual-supply, class-G architecture and is implemented in 65nm CMOS. It implements signal envelope digital-to-analog conversion using switching functions controlled by digital logic to achieve superior efficiency and high linearity at output power back-off to eliminate the need for digital pre-distortion.

TECHNICAL APPROACH

A class-G SCPA improves the average efficiency for signals with large peak-to-average power ratios. It operates from either of two power supply voltages depending on the amplitude of the signal. Operation close to saturation for more than just the near-peak signal levels is achieved by digitally selecting the optimal supply voltage based on a digital code word representation of the envelope $A(t)$. For small (large) $A(t)$ values, selected capacitors are switched between V_{DD} and V_{gnd} (V_{DD2} ($2\times V_{DD}$) and V_{gnd}). An optimal switching arrangement is used in the design to maximize efficiency.

SUMMARY OF RESULTS

A class-G SCPA is shown in Fig. 1 (the fabricated circuit is fully differential). It utilizes a digital EER technique to achieve high linearity from a high-efficiency switching configuration. First, the non-CE modulated baseband signal is transformed from a Cartesian representation to an equivalent polar form. The resulting time-varying amplitude signal, $A(t)$, is input as a digital code word, $B_{IN}(A)$, to combinatorial decoding logic that enables switching of the bottom plates of selected capacitors between V_{DD} and V_{gnd} or V_{DD2} and V_{gnd}. After up-conversion to the RF carrier frequency, the time-varying phase signal, $\phi(t)$, serves as the clock input to the combinatorial logic that drives the capacitor array.

The un-switched top plates are connected to a band-pass matching network that provides low impedance to the array at the desired frequency, enables high power output, and filters harmonics associated with switching.

For the conventional switching sequence (Figure 1), the efficiency decreases as the normalized output voltage changes from 1.0 to 0.5 V. This drawback is overcome using a switching sequence that uses both V_{DD} and V_{DD2} (Fig. 1). The SCPA delivers a peak (average) output power of 24.3 (16.8) dBm with a peak (average) PAE of 44% (33%) for an *IEEE 802.11g* signal with an EVM of 2.9 % at 2.4 GHz as shown in Fig. 2.

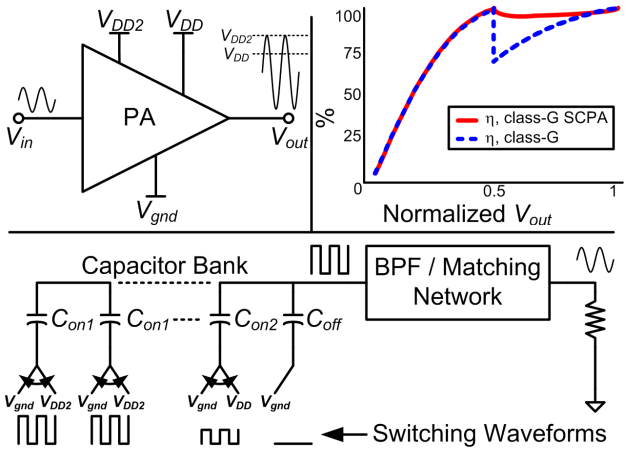

Figure 1: Class-G SCPA with two supply voltages. Clockwise from top left: Conceptual class-G PA, comparison of ideal efficiencies for the conventional and SCPA versions, and an ideal implementation with ideal switches and capacitors.

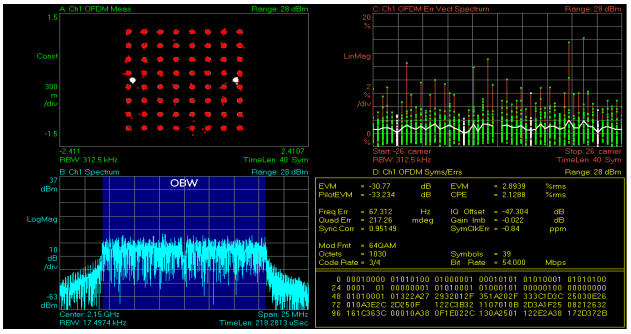

Figure 2: 64 QAM/OFDM; EVM = 2.9% (w/o predistortion)

Keywords: Power Amplifier; switched-capacitor PA; RF PA

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] S. Yoo, et al., "A class-G dual-supply switched-capacitor power amplifier in 65nm CMOS," *IEEE Radio Frequency Integrated Circuits Symp.*, 2012, pp. 233-236.

[2] S. Yoo, et al., "A class-G switched-capacitor power amplifier," *IEEE J. Solid-State Circuits*, vol. 48, pp. 1212-1224, May 2013.

[3] J. Walling, et al., "Switched capacitor PAs: Toward efficient, linear amplification," *IEEE PA Symp.*, Sept. 2013.

TASK 1836.086, VARIATION TOLERANT CALIBRATION CIRCUITS FOR HIGH PERFORMANCE I/O

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SIGNIFICANCE AND OBJECTIVES

Process variation degrades operation of analog subsystems and high performance I/O. While sources of process variation are well understood, methods to combat its effects are ad-hoc with power and area costs. This project explores circuit techniques to improve calibration of high performance I/O blocks at a reduced cost.

TECHNICAL APPROACH

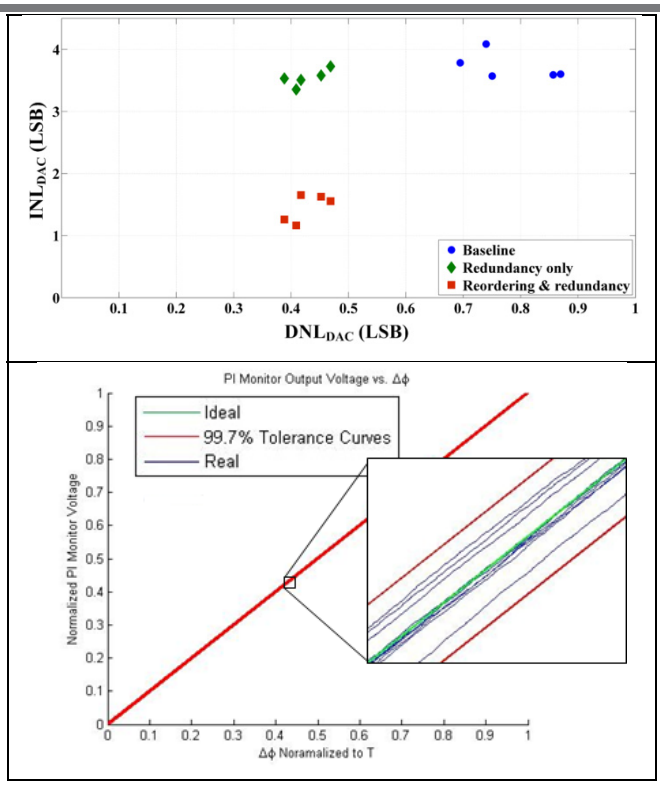
This project focuses on design of current mode calibration DAC's with improved INL and DNL and Phase Interpolator calibration circuits. This former is accomplished through combining methods. Redundant DAC cells are added to enable elimination of "outlier" high variation cells. Cells are also selected in an order such that the variation in the sum (INL) is reduced.

Phase Interpolator calibration is achieved through a circuit that measures delay by counting the number of random events occurring in the measured interval of phase offset. Over time this measurement converges to an accurate count of the phase difference between the two signals.

SUMMARY OF RESULTS

DAC calibration: We have developed new theory to describe the techniques of redundancy and reordering described above based upon ordered statistics. This work, submitted for publication in [1], is important because this new mathematical description allows us to build accurate system level models of the entire I/O block. Without these models, simulation is prohibitively time consuming for the larger I/O system.

An 8 bit current mode calibration DAC with 16 redundant cells has been designed and sent for fabrication. In addition to implementing the redundant cells an encoding/decoding scheme to identify and eliminate high variation cells has been implemented. Figure (Top) shows the initial measured results for 5 of these chips. As can be seen from this small sample, application of redundancy and reordering moves the INL and DNL of the DAC from the blue to the red, with significant improvement in performance. In the coming year, we will test more samples of an improved (smaller) DAC with full on-chip calibration and provide a full model of how this circuit effects the overall receiver I/O chain.



Top: Measured results of calibration DAC for 5 samples. Bottom: Simulation of PI monitor showing 0.5ps with a 99.7% confidence.

PI monitor: Simulation of our recently taped out PI monitor design shows accuracy to 0.5ps with 99.7% confidence. Design of the correct oscillator characteristics is essential to prevent aliasing and error. Even with oscillator variation, it is possible to keep this curve within certain range from the ideal curve, thus set a minimum bound for the accuracy. A maximum of 0.28% of the time, the accuracy was worse than 0.5ps.

Keywords: process variation, calibration, INL, DNL, PI

INDUSTRY INTERACTIONS

Intel, IBM

MAJOR PAPERS/PATENTS

[1] I. Mukhopadhyay, et al., "Modeling of statistical techniques to improve static linearity of thermometer DAC," Submitted IEEE Transactions on Circuits and Systems II.

TASK 1836.087, A HIGH-SPEED LOW-POWER REFERENCE-LESS CLOCK DATA RECOVERY (CDR)

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SIGNIFICANCE AND OBJECTIVES

We propose a high-speed, low-power reference-less CDR targeting at a data rate of 28 Gb/s and above. The automatic frequency detection achieves unlimited frequency acquisition range and has no harmonic locking issue. A novel low-power phase detection circuitry will be explored to reduce the overall CDR power consumption.

TECHNICAL APPROACH

A novel frequency acquisition method and a new phase detection (PD) circuit are explored to enable a low-power reference-less CDR with unlimited frequency acquisition range. The proposed CDR is able to perform automatic frequency acquisition from the incoming data and clock/data recovery without the need of a reference clock. The automatic frequency detection achieves unlimited frequency acquisition range and has no harmonic locking issue as presented in conventional frequency acquisition methods. The proposed full-rate Bang-Bang PD (BBPD) reduces the number of high-speed power hungry latches from seven in a conventional PD down to four and implements the data delay by using passive transmission line, thereby reducing the power consumption of a conventional PD by up to ~40%.

SUMMARY OF RESULTS

Exiting CDRs either require a reference clock or suffer from the problem of harmonic locking when performing automatic frequency acquisition. The goal of this project is to design a low-power reference-less CDR architecture that can automatically detect the frequency of the incoming data without using a reference clock and with no harmonic locking problem. The major research outputs include a new architecture and IC demonstration of a low-power reference-less CDR. The design is targeted at data rate of 28 Gb/s and above, a chip area of less than 1 x 1 mm^2, and a power consumption of the core CDR of less than 2 mW/Gbps.

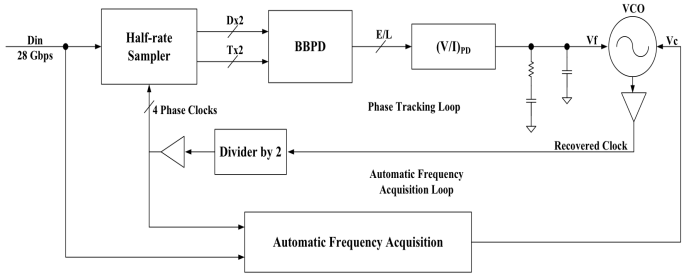

Figure 1: The architecture of the proposed reference-less CDR that is able to perform automatic frequency acquisition without harmonic locking issues and with unlimited frequency range.

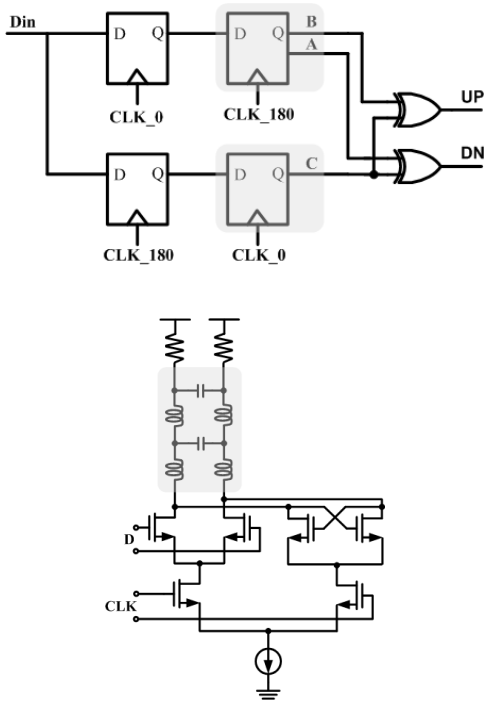

Figure 2: [Top] The proposed full-rate BBPD consisting of only 4 latches for data sampling. [Bottom] The proposed topology of a latch with delay element implemented using passive artificial transmission line, thereby reducing the power consumption of a conventional PD by up to ~40%.

Keywords: Clock Data Recovery (CDR), Automatic Frequency Acquisition, Reference-less, Phase Detector

INDUSTRY INTERACTIONS

Texas Instruments, Intel

TASK 1836.088, EFFICIENT SWITCHING MODE DIGITAL-INTENSIVE WIRELESS TRANSMITTERS UTILIZING SWITCHING MODE PAS

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SIGNIFICANCE AND OBJECTIVES

The efficiency of radio transmitters and power amplifiers continues to pose a significant challenge in the design of battery-operated wireless communication systems as well as in base station applications. The goal of this work is to investigate the use of switching power amplifiers and suitable modulation schemes for enhancing efficiency.

TECHNICAL APPROACH

Two-level modulation schemes such as PWM are well suited for use with efficient switching power amplifiers. These schemes are inherently digital friendly and therefore can be implemented in low-cost CMOS technologies. A PWM-based approach that relaxes the requirement for high quality reference signal generation will be employed as part of this work. High-speed Class-D switching PAs in CMOS will be utilized for enhancing efficiency. Minimization of in-band spurs is a key design goal. A passive external band-pass filter will be employed to reduce out-of-band spurs. The use of power mixers to upconvert low-frequency PWM will be investigated.

SUMMARY OF RESULTS

A classical PWM system generates its output by comparing the input to a ramp signal. This approach becomes progressively challenging as the bandwidth increases, since the ramp rate needs to be orders of magnitude higher than the signal bandwidth in order to ensure linearity. To avoid this requirement, a modified phase-locked loop based PWM generator is utilized to achieve adequate bandwidth (Fig. 1). The PWM generator has been verified in an IC implementation. The design consists of a single modulator path shown in Fig. 1, without the upconversion mixer. A peak output power of 1.2 W is achieved in a 6.8 Ohm load, with a 4.8 V supply. The design has a THD of -65 dB with a switching frequency up to 20 MHz. The peak efficiency is measured at 83% for an output power larger than 1W, with a switching frequency of 10 MHz.

The design of the wireless transmitter [1] consists of two PLL-PWM generators, one each for the I and Q quadrature paths. The outputs of the baseband generator are frequency translated using quadrature LOs to the transmit band, combined and bandlimited in an external bandpass filter.

An analysis of the above architecture has been performed and several critical challenges and potential solutions have been identified [1]. A major design challenge arises from the non-linearity of the frequency-to-control-voltage (K_{VCO}) characteristic. If the VCOs used in the I and Q paths have non-linear and mismatched K_{VCO} characteristics, the operating (quiescent) values of K_{VCO} in the two loops will be different, leading to mismatched closed-loop responses. This will lead to distortion in the output. The impact of this distortion can be suppressed by the gain of the low-pass filter that precedes the VCO.

Another major design challenge in the system arises from the potential for in-band spurs caused by aliasing of the PWM output by the harmonics of the upconversion LO. In order to mitigate this, the choice of PLL reference for a 900 MHz output has been optimized. This can be similarly optimized for other carrier frequencies. A consequence of this choice of frequencies is that the output of the mixer can consist of narrow pulses, which can lead to non-linear slewing. The use of a practical low-inductance package has been found to be adequate for pulses that are up to 60 ps wide. An off-chip non-isolating combiner will be implemented for this design.

In addition the above work, we have designed a transmitter based on the use of an output mixer stage that avoids the requirement for a large PA stage.

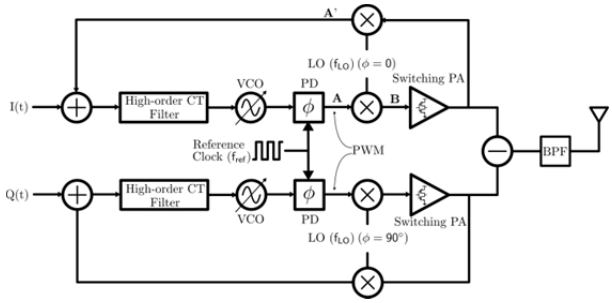

Figure 1: PLL-PWM Based Transmitter Architecture

Keywords: PWM, digital modulation, wireless transmitters, switching mode PAs.

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] J. Lu et al., "Phase-Locked Loop Based PWM Wireless Transmitter," 2013 IEEE Int. Symp. Ckts and Sys., Beijing

TASK 1836.089, ENERGY EFFICIENT COMPARATOR ELEMENTS FOR A/D CONVERTERS AND HIGH-SPEED I/OS

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VLADIMIR M. STOJANOVIC, UC BERKELEY

SIGNIFICANCE AND OBJECTIVES

This work addresses the problem of excess power dissipation in ADCs. We focus on the comparator as one of the key elements that needs to be optimized in order to achieve energy-efficient A/D conversion. Several factors influence power consumption of a comparator, such as supply voltage, input common-mode, input overdrive, and transistor sizing.

TECHNICAL APPROACH

After preparing the characterization and tuning tools, we are looking into developing new sense amplifier structures. It is of special interest to analyze the Impulse Sensitivity Function (ISF) of the sense amplifier, as it allows predicting what is the Effective Number of Bits (ENOB) it can achieve. An energy budget can then be established if the desired resolution is given. It is desired to analyze the newest approaches that have allowed a significant reduction in supply voltage with its subsequent power saving.

SUMMARY OF RESULTS

A new topology for a clocked comparator is presented in this report. It is based in two stage architectures previously reported by Schinkel and Elzakker. A significant difference is that it relies in only one clock phase, thus freeing the constraint of accuracy timing as in the designs based in a two phase clock.

Its operation can be described as follows. In pre-charge state, when the clock signal CLK is low, transistors M8, M5 and M15 are turned off and transistors M6, M7, M7 and M17 are turned on. This causes nodes n2, n12, n3 and n13 to charge up to VDD, which in turn causes to keep transistors M4 and M14 turned off and turn on transistors M2 and M12, discharging the output nodes outp and outn down to VSS.

As the clock signal changes to high the evaluation state starts, turning off transistors M6, M7, M16 and M17. At the same time transistors M5, M8 and M15 turn on. Transistors M1 and M11 start discharging nodes n2 and n12, respectively, at a rate proportional to their gate voltage (Vin and Vin_ref). Transistors M5 connect node n3 with node outn, and transistor M15 connects node n13 with outp, starting a regeneration of the voltage imbalance caused by transistors M2 and M12 as nodes n2 and n12 discharge.

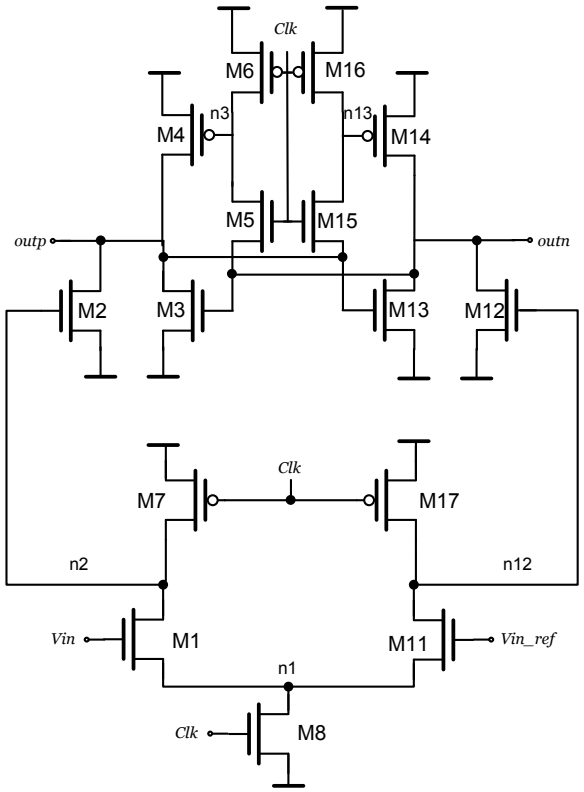

Figure 1: Circuit schematic of the proposed sense amplifier

In order to verify the ISF profile of the new comparator, a chip has been fabricated in IBM 45nm SOI technology. The output signals of the sense amplifier are then followed by an SR latch, and the output of the SR latch is captured by a D flip-flop to be processed in the digital backend. The performance of the new sense amplifier will be compared against similar topologies such as Strong Arm, Schinkel, and Elzakker. It is intended to give the possibility to obtain the ISF with the method portrayed by Metha Jeeradit in 2008.

Keywords: ADC, low power design, sense amplifier

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

TASK 1836.093, VARIABILITY-AWARE, DISCRETE OPTIMIZATION FOR ANALOG CIRCUITS

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SIGNIFICANCE AND OBJECTIVES

While analog circuit optimizers, that can automatically size transistors in a circuit according to a prescribed performance metric, can be an effective productivity tool for analog, yet the reality is that their adoption into the mainstream flows has been rather slow. Exploiting the inherent uncertainty in IC process, this task aims to explore the use of discrete optimization techniques for realizing a fast, deterministic optimizer that can perform quick, incremental 'what-if' analysis.

TECHNICAL APPROACH

While analog design parameters are typically of continuous values, we assert that such a continuous design space can be effectively covered with a set of finite, coarsely-spaced, discrete points by exploiting the inherent variability in the IC technology. Our expectation is that a discrete optimizer can solve many of the problems faced with the existing, continuous optimizers for analog circuits.

However, since one weakness of a discrete optimization approach is its poor scaling with the problem dimensionality, various approaches have been investigated, including a predictive global search algorithm and a hierarchical optimization approach based on Pareto-front extraction.

SUMMARY OF RESULTS

Last year, three novel algorithms were proposed that leverage the discrete optimization technique yet mitigate its limitation in dimensionality scaling [1]: 1) an isotropic discretization scheme (Figure 1) in which all the nearest-neighbors on the grid have the same distance and their number grows only quadratically with the dimension, 2) a stochastic hill-climbing algorithm of which required number of evaluation during a local search grows mildly with the space dimension, and 3) an incremental Monte Carlo simulation algorithm that determines which design is better in statistical sense with minimal number of Monte Carlo samples. These algorithms help find the optimal design of analog circuits efficiently.

This year, an efficient method to extract a yield-aware Pareto front between two competing metrics of an analog circuit block is investigated [2]. By using these component-level Parent-fronts as meta-models, one can perform scalable system-level optimization in a hierarchical manner. The proposed method consists of three steps: 1) finding a set of Pareto-optimal design points by tracing them on a discrete grid; 2) estimating the yield distribution of each optimal design point using a control-variate method, and 3) constructing a yield-aware Pareto front by interpolation (Figure 2). Within a 2% margin of error, the algorithm can estimate the Pareto front of a circuit block with 99% yield while requiring only 600~1,200 Monte Carlo simulation samples.

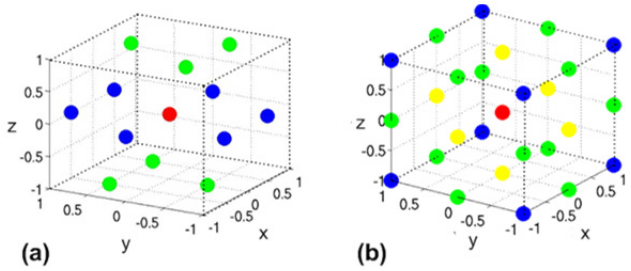

Figure 1: (a) The proposed isotropic grid named "Polka-Dot" in comparison with (b) the classical Cartesian grid.

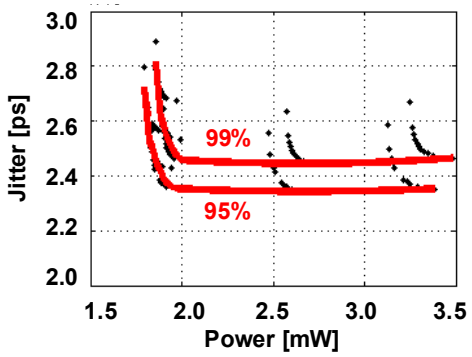

Figure 2: The estimated 95% and 99%-yield Pareto fronts of a phase mixer circuit.

Keywords: analog circuit synthesis, circuit optimization, discrete optimization, yield-aware optimization, statistical comparison.

INDUSTRY INTERACTIONS

Texas Instruments, Inc. and Intel Corp.

MAJOR PAPERS/PATENTS

[1] S. Jung, J. Lee, and J. Kim, "Variability-Aware, Discrete Optimization for Analog Circuits," in preparation for Trans. on Computer-Aided Design, 2013.

[2] S. Jung, J. Lee, and J. Kim, "Yield-Aware Pareto-Front Extraction for Discrete, Hierarchical Optimization of Analog Circuits," in preparation for Trans. on Computer-Aided Design, 2013.

TASK 1836.95, TEST GENERATION FOR MIXED-SIGNAL DESIGN VERIFICTION AND POST-SILICON DEBUGGING

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SIGNIFICANCE AND OBJECTIVES

Mixed-signal design, verification, and debugging critically depend on running circuit simulation. Current research efforts have resulted in progress exclusively on advanced simulation algorithms. This project aims at the development of theory, techniques, and tools for *generating test benches and vectors used to drive circuit simulation for mixed-signal design verification and post-silicon debugging.*

TECHNICAL APPROACH

The research is directed to solve the following two problems (1) generation of the *minimal-length verification tests* that can sensitize the worst-case errors in analog blocks embedded in complex mixed-signal integrated circuits, and (2) Generation of the shortest *debugging simulation test benches and stimulus sequences* that can isolate the errors that cause mixed-signal chip failures for post-silicon design debugging. The technical approach is to represent a complex mixed-signal integrated circuit by a system-level signal path diagram based on behavioral models, and to generate the candidate test benches and vectors based on signal types and signal path diagrams.

SUMMARY OF RESULTS

In the initial period of this project, we focus on the development of a real mixed-signal test case that can illustrate the problem complexity and highlight the research requirement. The test case we developed is a high sensitivity plastic optical fiber receiver in a 65nm UMC CMOS process. This initial work for design case tape out has been sponsored by matching grants from the State of Washington and Boeing.

The avionics communication backplanes provide all fly-by-wire controls and sensor data exchange across the airplane. Traditionally, copper wire based communications have been used for their good reliability and low attenuation of the transmitted signal. However, drawbacks of added weight to the aircraft and non-negligible material costs increase to airplane construction have put a limit in their usage. Plastic optical fiber (POF) is a very low cost and light weight solution for backplane communications that has been adopted by commercial consumer Local Area Network (LAN) replacing the more expensive bulky copper based wire cabling Optical receiver in CMOS standard process will enable mass production at low cost optical systems for enabling plastic fiber based communications in aerospace products.

In this work, a novel optical receiver is designed and implemented to meet the needed sensitivities for aerospace applications when utilizing Plastic Optical Fiber channels. The basic concept is to oversample the incoming optical receiver data and use digital signal processing to reduce the effective noise floor while providing significant gain of the data signal using digital correlation techniques. These techniques are enabled by the extremely fast 1GHz+ processing speeds of modern CMOS microelectronics technology and the relatively slow data rates used in aerospace applications(<10M-bits/sec). The implementation of the optical receiver in a standard 65nm CMOS process also allows for a mass produced and low cost downstream production.

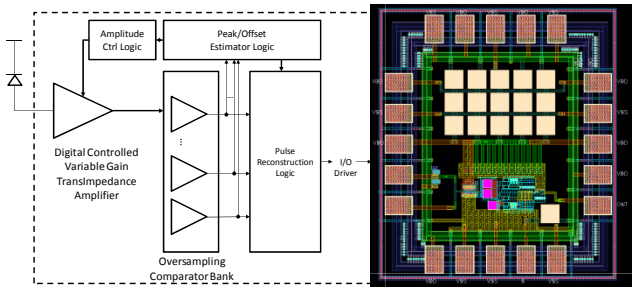

Figure 1: Architecture and die-graph of a POF receiver.

Our work in the coming years will focus on the algorithmic development of test generation method for mixed-signal design verification and post-silicon debugging using the designed POF receiver as a driver. The specific tasks consist of the development of behavioral models for mixed-signal circuit blocks, the development of test generation algorithms, and the demonstration of the developed tool on real test cases

Keywords: test generation, simulation, mixed-signal verification, post-silicon debugging, behavioral modeling

INDUSTRY INTERACTIONS

Texas Instruments, Intel

PUBLICATION

[1] J. P. Uehlin, et al, “A novel high sensitivity receiver for avionics controls and sensor communications using plastic optic fiber (POF)”, Symp. JCATI, June 2013.

TASK 1836.096, MIXED-SIGNAL DESIGN CENTERING IN DEEPLY-SCALED TECHNOLOGIES

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SIGNIFICANCE AND OBJECTIVES

A design methodology for robust design of high-performance analog circuit blocks in highly-scaled technologies is being investigated, that will enable rapid yield ramp-up in scaled technologies.

TECHNICAL APPROACH

We are developing a methodology that enables centering with respect to technology variability of high-performance mixed-signal signal designs in as few as one design iteration. It is based on the components, which are developed simultaneously:

- Instrumenting critical design components to accurately monitor impact of process variability on their performance.
- Creating a dedicated set of representative circuit primitives for their full variability characterization.
- Extracting a variability model from the test structures; building simplified Spice models to predict the distribution spread of critical components.

These components enable centering of critical analog blocks, such as clock and data recovery loops and high-performance data converters.

SUMMARY OF RESULTS

We are developing a design methodology that address variability at all levels. This is being accomplished by developing yield-aware optimization tools targeting critical analog circuit designs and by relying on extraction and modeling of manufacturability requirements specific to the target design.

The methodology is based on variability characterization by using representative test structures and building blocks to hierarchically capture variability and propagate distributions from devices, via components to systems. The approach involves selection of representative critical analog components, the design of transistor and component arrays in a characterization run, and backward propagation of performance data and its variability across the levels of hierarchy.

The approach is illustrated in on a yield optimization of a high-performance clock-and-data-recovery (CDR) loop, Fig. 1.a, to achieve high data rates. Comparator is a key component in the loop, which we are characterizing using impulse-sensitivity function (ISF), Fig. 1.b.

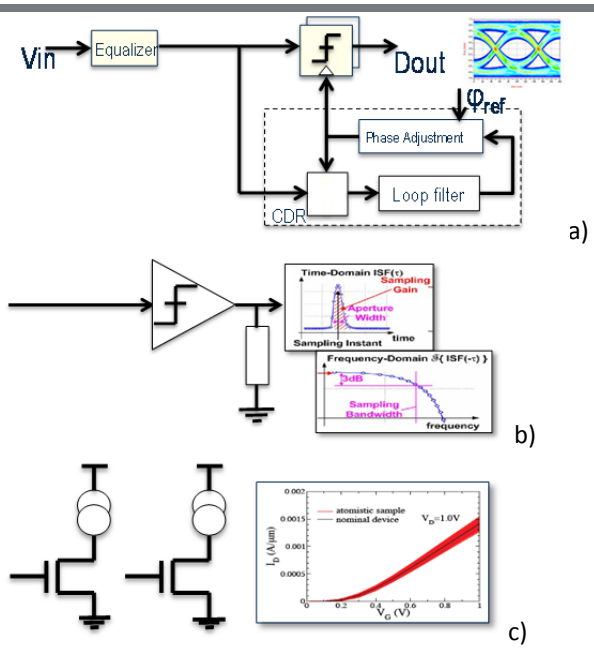

Figure 1: Illustration of the characterization approach a) Block diagram of a CDR; b) Impulse-sensitivity function of a comparator; c) device-level I-V characteristics.

Measured variability in ISF is being related to the variability measured by I-V sweeps of individual devices, Fig. 1.c, via backward variability propagation.

A set of transistor variability characterization structures with gate lengths of 20nm in fully-depleted SOI technology has been received from fabrication. Test boards have been sent out for fabrication.

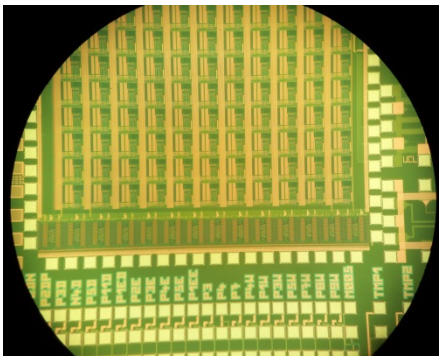

Figure 2: Test chip viewed though a microscope.

Keywords: CMOS, variability, yield, design optimization, clock and data recovery.

INDUSTRY INTERACTIONS

Intel

TASK 1836.097, DUAL-DOMAIN SAR ADCS INCORPORATING BOTH VOLTAGE AND TIME INFORMATION

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SIGNIFICANCE AND OBJECTIVES

Traditional SAR ADCs operate with one or more binary quantizers in the voltage domain to dictate DAC switching operations. The purpose of this research is to improve the efficiency and resolution achievable with a single comparator by utilizing statistical information in both the voltage and time domains.

TECHNICAL APPROACH

The TSAR structure is based on traditional SAR techniques, coupled with analyzing the propagation delay of a latched comparator to create an optimized switching algorithm, half bit redundancy, and speed enhancements. Time and voltage information are examined to provide polarity and magnitude information of the input. The concept of PDF residue shaping is examined to provide extra resolution for a given number of cycles. The described techniques are implemented in a prototype Ternary SAR (TSAR) IC.

SUMMARY OF RESULTS

The TSAR is implemented by placing a time comparator after the traditional voltage comparator [1][3]. The comparator propagation delay is compared against a pre-set maximum time period, generating a third output code in addition to the standard SAR codes. This new third level is utilized to optimize DAC switching operations by eliminating worst case delays associated with small input voltages through implementing a no switching region. An added benefit is redundancy and residue shaping without the added cost of extra stages or sub-radix arrays [2].

The Feedback Initialized TSAR (FITSAR) improves upon TSAR energy savings by driving the DAC with both a coarse binary SAR and a fine TSAR. This segmentation allows the early stages to use a quantizer designed for energy efficiency, and the mid to late stages to use a quantizer with added accuracy. Due to the described changes, the energy used per code conversion and number of capacitors switched per conversion is reduced by 61% and 34% respectively over the TSAR structure and is lower for every code. Additionally the use of a coarse SAR nested in the TSAR loop and use of embedded EMCS coarse stage reduces overall comparator energy by 45%. The fabricated prototype in 0.13µm CMOS achieves a FOM of 15.4 fJ/CS at 8MHz and 9b accuracy [4].

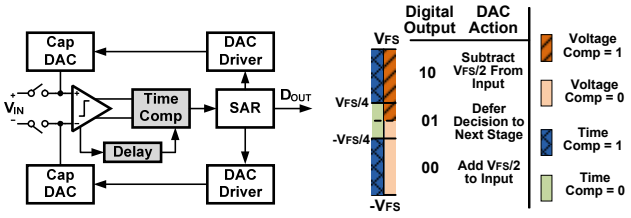

Figure 1: The Ternary SAR (TSAR) structure and stage output

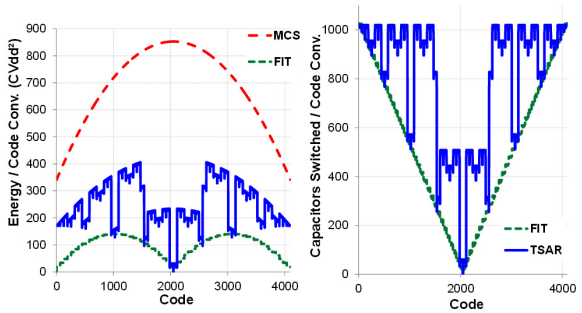

Figure 2: FITSAR Energy and DAC savings compared to TSAR and MCS

Table 1: Performance Summary

	VDD	ENOB	BW	Power	Area
FITSAR	0.8 V	8.89 b	8 MHz	58 µW	0.06mm^2

Keywords: Ternary SAR, residue shaping, time comparator, SAR energy, SAR ADC

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] J. Guerber, M. Gande, H. Venkatram, A. Waters, and U. Moon, "A 10b ternary SAR ADC with decision time quantization based redundancy," *A-SSCC,* Nov. 2011.

[2] J. Guerber, M. Gande, and U. Moon, "The analysis and application of redundant multistage ADC resolution improvements through PDF residue Shaping," IEEE Trans. Circuits Syst, Aug. 2012.

[3] J. Guerber, H. Venkatram, M. Gande, A. Waters, and U. Moon, "A 10-b ternary SAR ADC with quantization time information utilization" JSSC, Nov. 2012.

[4] J. Guerber, M. Gande, H. Venkatram, and U. Moon, "A feedback initialized ternary SAR ADC," submitted, *A-SSSC* 2013.

TASK 1836.100, TEST TECHNIQUES AND FAULT MODELING FOR HIGH VOLTAGE DEVICES AND BOARDS

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SIGNIFICANCE AND OBJECTIVES

Our project objectives are 1) develop physics-based fault models for LDMOS transistors, 2) develop parasitic device models, 3) modify ATE load boards for high voltage discharge problems, and 4) provide novel low-cost test techniques for high voltage LDMOS devices.

TECHNICAL APPROACH

Lateral DMOS transistors are used in various applications. We have developed equivalent circuit models for LDMOS and structural defect fault models. Test simulations were performed and a fault dictionary was created. We continued to improve HVPro to perform automatic program generation for troubleshooting load boards. We built a test prototype to test the DUT. We performed simulations to reduce avalanche breakdown voltages.

SUMMARY OF RESULTS

We prototyped a new noise reduction scheme to measure nano amp range current. The proposed LDMOS test setup is shown in Figure 1.

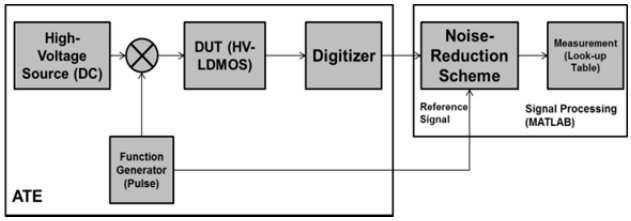

Figure 1: Proposed LDMOS Test Setup

Hardware test measurement apparatus was built. Simulated results were compared with the measured ATE test results as shown in Table 1.

We developed a low-cost test technique to reduce the avalanche breakdown voltage. We performed extensive simulations based on the parasitic devices modeling as shown in Figure 2(A). The model consists of BJT parasitic transistor that could trigger the avalanche breakdown at a high voltage level. The high voltage in the drain terminal provides excessive substrate current that could bias the base of the BJT to trigger the device into the avalanche region. We used closed form mathematical expressions to describe the drain current. These expression were simulated on Matlab and points were gathered to plot as shown in Figure 2(B)

Table 1. Test Measurement Results

Test Condition	DUT Input	Simulated	Measured
Fault-free	1mA	6.89 V	6.92 V
Gate Oxide breakdown	0mA	0.89 V	0.70 V
Thermal Stress	1mA	6.19 V	6.38 V
I_D Leakage Test	1mA	6.83 nA	6.69 nA

We can summarize that a non-conventional test technique using transmission line pulses at the gate terminal provides a much lower avalanche voltage.

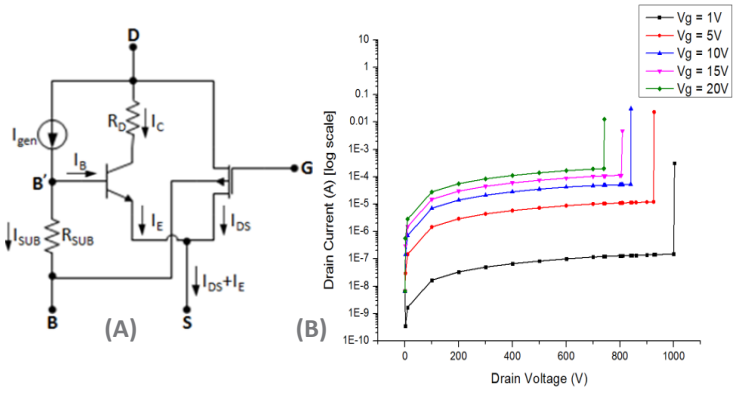

Figure 2. (A) LDMOS Device Parasitic Model and (B) Simulation Results for Avalanche Breakdowns.

Keywords: LDMOS, Structural defects, avalanche voltage, fault model, high voltage

INDUSTRY INTERACTIONS

Texas Instruments, Globalfoundries

MAJOR PAPERS/PATENTS

[1] S. Kannan, B. Kim, F. Taenzler, R. Antley, K. Moushegian, "Development of Novel Test Technique and Fault Modeling for High-Voltage LDMOS," Proceedings of Semiconductor Research Corporation, TECHCON, Austin Texas, September 2012.

[2] S. Kannan, B. Kim, F. Taenzler, R. Antley, K. Moushegian, A. Gupta, "Physics Based Fault Models for Testing High-Voltage LDMOS," IEEE VLSI Design Conference, Pune India, January 2013.

TASK 1836.107, VERIFICATION OF MULTI-STATE VULNERABLE AMS CIRCUITS

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SIGNIFICANCE AND OBJECTIVES

The objective is to develop systematic procedures for detecting presence or absence of Trojan equilibrium states in AMS circuits and to develop a verification process that identifies need for and effectiveness of start-up circuits. The process can eliminate circuit failures due to undetected or ineffective removal of Trojan states.

TECHNICAL APPROACH

Circuit-level homotopy methods that use a standard circuit simulator as the primary computational tool are being developed for determining presence or absence of multiple stable equilibrium points. If a Trojan state is identified with this process, the process can be repeated after a start-up circuit is added to verify the Trojan state has been robustly eliminated over PVT variations. A mapping from a circuit schematic to a circuit graph will be used to identify critical feedback loops used for applying homotopy methods. The resultant verification algorithm will be applied to a group of benchmark circuits to assess its performance.

SUMMARY OF RESULTS

Circuit-level homotopy methods have been developed, compared, and adapted for determining both the presence of Trojan operating states and for verifying the effectiveness and robustness of Trojan State Removal circuits (often termed start-up circuits). An initial procedure for identifying the feedback loops that are an integral part of the circuit-level homotopy analysis has been developed. A set of benchmark circuits comprised of several popular circuits with known start-up issues as well as some other self-stabilized circuits that are vulnerable to the presence of Trojan operating points has been created. The circuit-level homotopy methods have been effective at identifying all Trojan states in the group of benchmark circuits that has been created.

As an example, the standard Inverse Widlar bias generator without start-up circuit is shown in Fig. 1a. The single positive feedback loop is broken for doing a circuit-level homotopy analysis in Fig. 1b. The transfer characteristics, V_{OUT} vs V_{IN}, obtained from the dc sweep is shown in Fig. 2. This homotopy analysis correctly identifies two stable equilibrium points, the desired point and a Trojan operating point. After a start-up circuit is added, robustness over PVT variations can be verified by repeating the same sweep and verifying that there is only one stable equilibrium point.

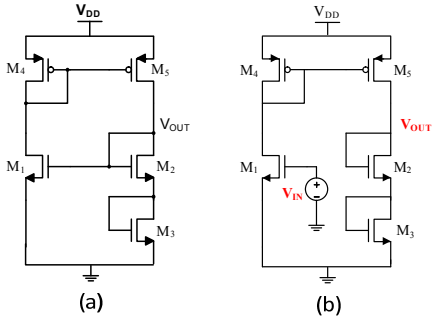

Figure 1: Inverse Widlar Bias Generator (a) basic circuit, (b) feedback loop broken for Homotopy analysis

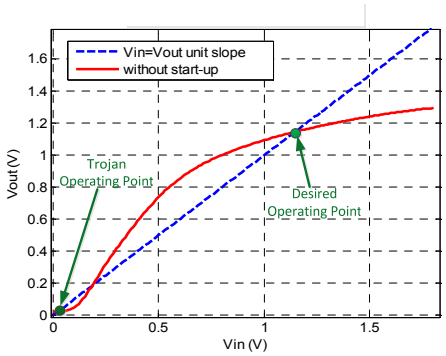

Figure 2: Transfer Characteristics of Inverse Widlar Generator with Break-Loop Homotopy Analysis

Keywords: Verification, Homotopy, Start-up, Equilibrium points, Trojan states

INDUSTRY INTERACTIONS

Texas Instruments, Intel, Freescale

MAJOR PAPERS/PATENTS

[1] B. Vasan, et al, (invited) "Low Distortion Sine Wave Generation Using a Novel Harmonic Cancellation Technique, TCAS (to appear).

[2] Y-T. Wang, et al, "Practical Methods for Verifying Removal of Trojan Stable Operating Points", ISCAS, May 2013.

[3] Y-T. Wang, et al, "Performance verification of start-up circuits in reference generators", MWSCAS, Aug. 2012.

[4] C. Zhao, et al, "A CMOS on-Chip Temperature Sensor with -0.21°C/ 0.17 °C Inaccuracy from -20 °C to 100 °C", ISCAS, May 2013.

TASK 1836.109, NEW PARADIGMS FOR HIGH-PERFORMANCE AMPLIFICATION

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SIGNIFICANCE AND OBJECTIVES

Amplifiers are increasingly power hungry and difficult to build in evolving nanoscale CMOS. This has created a serious crisis that affects us all, particularly in the era of SoCs. The techniques presented in this summary offer new paradigms for high-performance amplification in a variety of applications as a scalable solution.

TECHNICAL APPROACH

A ring oscillator that has been internally split into two separate signal paths is used as an amplifier. A voltage offset of equal amplitude but opposite polarity is injected into each path by the reference voltage V_{DZ}. This creates an input-referred dead-zone – a small range of input values for which neither output transistor will conduct to stabilize the oscillation process. The ring amplifier has been expanded on by the introduction of a fine ring amplifier. An ADC was designed, built, and tested using a composite coarse and fine ring amplifier block.

SUMMARY OF RESULTS

Previously, two prototype ADCs employing a coarse ring amplifier were implemented. The first prototype ADC demonstrated the basic principles of a ring amplifier in 10.5b pipelined ADC. The second prototype ADC employs the technique of Split-CLS to perform efficient, accurate amplification aided by ring amplifiers.

To expand the applications of ring amplifiers, a fine ring amplifier was designed. This ring amplifier takes advantage of a 'weak-zone' where the output still slightly conducts. The system is only limited by the overall finite gain of structure. The high accuracy ring-amplifier in the bottom left of Fig 1. has a tunable resistor to set the size of the stability zone to match the weak-zone.

The high precision ring amplifier has two key drawbacks. The drawbacks are reduced slew rate (compared to a coarse ring amplifier), and a single ended output. By designing a composite ring amplifier block as seen in Fig 2, these disadvantages can be removed.

A 15b pipelined ADC was implemented using this structure in .18µm CMOS technology [1]. With a 1.2V supply it achieved 75.9dB SNDR, 76.1dB SNR, and 91.4 dB SFDR at 20 MSPS. It consumed 2.96 mW with a FOM of 29 fJ/conversion-step. Table 1 summarizes the performance of this ring amplifier ADC.

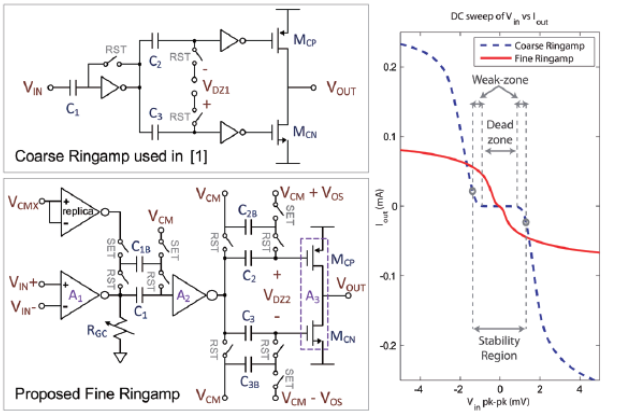

Figure 1: Coarse and Fine Ringamps

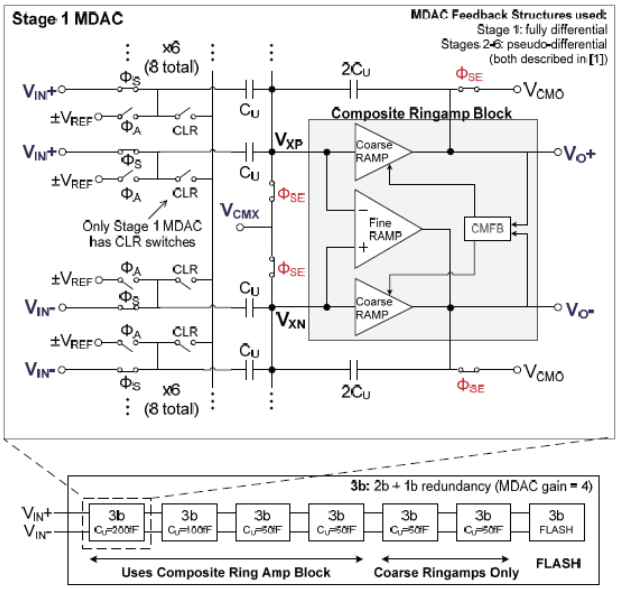

Figure 2: 15b Composite Ringamp ADC (Chip)

Table 1: Performance Summary

VDD	ENOB	BW	Power	FOM
1.2V	12.3b	10MHz	2.96mW	29fJ/c-step

Keywords: Ring amplifier, stabilized ring oscillator, scalability, ADC, fine ring amplifier.

INDUSTRY INTERACTIONS

Texas Instruments, Freescale, Intel.

MAJOR PAPERS/PATENTS

[1] B. Hershberg *et al.*, "A 75.9dB-SNDR 2.96mW 29fJ/conv-step ringamp-only pipelined ADC" *VLSI Circuits Symp.,* Jun. 2013.

TASK 1836.111, ADVANCED ADC-BASED SERIAL LINK RECEIVER ARCHITECTURES

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SIGNIFICANCE AND OBJECTIVES

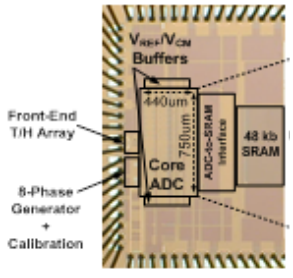
While CMOS technology scaling allows for the efficient implementation of powerful on-chip DSP algorithms for equalization and symbol detection, ADC-based receivers are generally more complex and consume higher power. The proposed ADC-based serial link techniques aim to significantly improve interconnect bandwidth density in an energy-efficient manner.

TECHNICAL APPROACH

In order to investigate design trade-offs, a novel statistical-modeling framework for advanced ADC-based serial links will be developed. This tool will be used to guide the design of a new hybrid ADC-based receiver architecture which combines in a power optimum manner equalization embedded in the ADC and dynamically power-gated digital equalization based on threshold detection, with an ultimate target data rate in excess of 25Gb/s. The statistical modeling framework and receiver prototypes will be leveraged to investigate the performance of the hybrid ADC architecture with multi-level modulation schemes (duobinary, PAM4, PAM8, etc.) and error correction coding.

SUMMARY OF RESULTS

In order to relax ADC-based receiver power and complexity trade-offs, partial equalization can be embedded inside the ADC and not be limited by the ADC resolution. Two CMOS ADC prototype chips were implemented to explore this. The first, a 6-bit 1.6GS/s SAR ADC with an embedded 1-tap DFE was implemented in an LP 90nm CMOS process and achieved 4.75b ENOB at 0.46pJ/conv [1]. The second (Figure 1), a 6b 10GS/s SAR ADC with embedded 2-tap FFE and 1-tap DFE was implemented in a GP 65nm CMOS process and achieved 4.56b ENOB at 0.48pJ/conv. [2].



(a)

TABLE I: PERFORMANCE SUMMARY

Specification	[El-Chammas 2011]	[Chen 2012]	This Work
Technology	65nm	65nm	65nm
Power Supply	1.1V	1.1V	1.1V/0.9V
ADC Structure	TI-Flash	TI-Flash	TI-SAR
Equalization	No	HPF + FFE	Embedded FFE + DFE
Sampling Rate	12 GS/s	10 GS/s	10 GS/s
Resolution	5 bits	4 bits	6 bits
ENOB @ ERBW	3.88 bits	N/A	4.03 bits
Input Range	590 mV_{pp}	600 mV_{pp}	500 mV_{pp}
FOM ($P/2^{ENOB} \cdot f_s$)	0.46 pJ/c.-s.	N/A	0.48 pJ/c.-s.
Area	0.44 mm^2	0.29 mm^2	0.52 mm^2
Power	81 mW	93 mW*	79.1 mW

* This value includes the clock and analog front-end power consumption.

(b)

Figure 1: 6b 10Gb/s time-interleaved SAR ADC with embedded 2-tap FFE and 1-tap DFE: (a) GP 65nm CMOS prototype, (b) performance summary.

While embedded DFE and 2-tap FFE provides improved BER performance, additional equalization is generally required to support channels with loss greater than 30dB. A new hybrid ADC-based receiver architecture which combines in a power optimum manner equalization embedded in the ADC and dynamically power-gated digital equalization based on threshold detection is proposed. In this scheme, the ADC output is considered as a reliable decision if the value exceeds a certain differential threshold, which can also serve as an indication that further equalization is necessary on a sample-by-sample basis. In the proposed hybrid ADC receiver architecture (Figure 2), any samples below the threshold level are passed through the digital equalizer, while samples which exceed the threshold are treated as reliable decisions. The percentage of digital equalization power saving is set by the probability that the ADC output exceeds the threshold value that corresponds to BER=10^{-12}. With embedded FFE equalization, savings of more than 50% of digital equalization power is possible for up to 37dB of attenuation at Nyquist frequency. A 10Gb/s receiver prototype with a 6-b ADC and the digital equalizer is currently being implemented in a GP 65nm CMOS process.

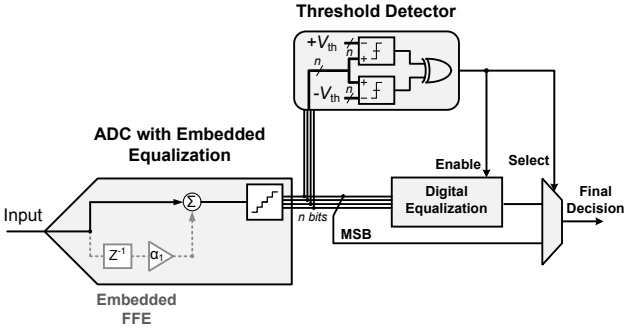


Figure 2: Proposed hybrid ADC RX architecture.

Keywords: Analog-to-digital converter, embedded equalization, energy efficient

INDUSTRY INTERACTIONS

Freescale, Intel, Texas Instruments

MAJOR PAPERS/PATENTS

[1] E. Zhian Tabasy et al., "A 6-b 1.6-GS/s ADC with Redundant Cycle One-Tap Embedded DFE in 90-nm CMOS," IEEE JSSC, Aug. 2013.

[2] E. Zhian Tabasy et al., "A 6b 10GS/s TI-SAR ADC with Embedded 2-TAP FFE/1-Tap DFE in 65nm CMOS," IEEE VLSI Sym., June 2013.

TASK 1836.113, SYNTHESIZED CELL-BASED ADPLL IMPLEMENTATION FOR ACCELERATED DESIGN

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SIGNIFICANCE AND OBJECTIVES

This 3-year program focuses on developing "cell-based" all-digital PLLs that can be synthesized from a cell library, implemented using existing automatic place and route (APR) tools, and then digitally calibrated. The end result will be a set of PLL architectures described in HDL which can be adopted to a wide range of performance requirements.

TECHNICAL APPROACH

ADPLLs are preferred over analog PLLs because they take advantage of process scaling, offer area savings and reconfigurability, and are mostly portable across processes. However, ADPLL performance inherently suffers due to TDC and DCO quantization errors, leading to the use of DACs, ΔΣ modulators, and carefully matched layout to improve performance. Our approach is to improve the performance of ADPLLs through novel architectural and implementation improvements, targeting the aggressive specs of LO generation for connectivity radios. The goal is to produce a design synthesizable using standard CAD tools. These new designs will be prototyped in a series of test chips in advanced CMOS processes.

SUMMARY OF RESULTS

We have recently demonstrated a sub-sampling, integer-N ADPLL that was completely designed and APR-ed using digital design flows. Additionally, this ADPLL demonstrated a technique of pulse-width-modulating (PWM) the DCO control signals to enhance DCO resolution, replacing the traditional DAC and ΔΣ modulator. The PWM technique has the advantage of introducing no spurs, and allows DCO tuning with 59kHz steps. An adaptive digital loop filter (DLF) is implemented to allow a large lock-in range as well as have low bandwidth to suppress TDC noise. The ADPLL FoM is -218dB at 403MHz, and covers the entire MedRadio range (401 to 457MHz) [1].

Fig. 1 shows the ADPLL architecture with PWM-based resolution enhancement technique. It consists of a ten stage ring DCO, embedded TDC, adaptive DLF and DCO controller. The DCO controller sends a 20b coarse, 20b fine and 7b ultrafine frequency control word to the DCO. The entire ADPLL is cell-based and the layout APR-ed, including the DCO and TDC, which introduces systematic mismatch in wiring capacitance. The most critical is the stage-to-stage mismatch that causes a bounded differential non-linearity in the TDC. The TDC output is processed in the DLF in order to mitigate the effect of these mismatches.

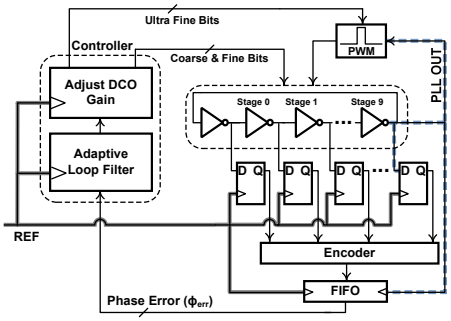

Figure 1: Architecture of the synthesizable ADPLL with embedded TDC, adaptive filter, and PWM control of the DCO.

This ADPLL performs integer-N synthesis without a divider by subsampling the TDC output. The division ratio (N) is programmable by the controller. The ADPLL performance was compared with and without PWM control enabled. This results in 14dB and 11dB improvements in in-band phase noise for 403MHz and 40.3MHz reference frequencies, respectively. The ADPLL is implemented in a 65nm CMOS process, and occupies an active area of 0.1 mm^2. Table 1 compares more specific performance metrics of this work to some recently published state-of-the-art ADPLLs

Table 1: ADPLL Performance Comparison

	This Work		ISSCC'10	JSSC'11	ISSCC'12
F_{REF} (MHz)	403	40.3	26	544	108/72/36
F_{OUT}(MHz)	403	403	800	0.7 - 3.5	3100
RMS Jitter	7.9 ps	13.3 ps	21.5 ps	1.6 ps	1.01 ps
PN (dBc/Hz)	-98 @ 1MHz	-87 @ 1MHz	-98 @ 1MHz	-116 @ 1MHz	-
Area	0.1 mm^2	0.1 mm^2	0.05 mm^2	0.36 mm^2	0.32 mm^2
Power	3.3 mA	2.1 mA	2.66 mA	1.6 mA	27.5/26.8/ 25.8 mA
VDD	1	1	1.1-1.3	1	1.2
Architecture	ADPLL	ADPLL	ADPLL	Highly Digital	ADPLL
DAC & ΔΣ	No	No	DAC & ∑Δ	Multiple DACs	DAC
Technology	65 nm	65 nm	65 nm	90 nm	65 nm

Keywords: VLSA (Very Large Scale Analog), ADPLL, CMOS, frequency synthesizer

INDUSTRY INTERACTIONS

Intel, Freescale

MAJOR PAPERS/PATENTS

[1] M. Faisal, D. D. Wentzloff, "An Automatically Placed-and-Routed ADPLL for the MedRadio Band Using PWM to Enhance DCO Resolution," RFIC 2013.

TASK 1836.114, FREQUENCY SHAPEABLE MULTICHANNEL ADCS

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SIGNIFICANCE AND OBJECTIVES

During this period we focused on understanding the fundamental sampling limits of multichannel ADC sampling for cognitive radio applications, we begun investigating a chip implementation of our basic structure, and started exploring common distortions such as nonlinear distortions and ways to overcome them.

TECHNICAL APPROACH

Cognitive radio applications: Our approach was based on developing a multichannel ADC structure that can sample multiband signals at sub-Nyquist rates by exploiting the statistical properties of typical communication channels focusing on cyclo stationarity and stationarity.

Chip implementation: together with our collaborators at Stanford, Prof. Boris Murman and his PhD student, Douglas Adams, we have begun designing a chip that can implement the algorithms achieving minimal sampling rate outlined above.

Nonlinear distortions: We suggested several algorithms for recovery of sparse inputs in the presence of a variety of different nonlinear distortions.

SUMMARY OF RESULTS

Cognitive radio applications: Cognitive Radio (CR) challenges spectrum sensing into dealing with wideband signals in an efficient and reliable way. CR receivers traditionally deal with signals with high Nyquist rates and low Signal to Noise Ratios (SNRs). On the one hand, sub-Nyquist sampling of such signals alleviates the burden both on the analog and the digital side. On the other hand, cyclostationary detection ensures better robustness to noise. We consider cyclostationary detection from sub-Nyquist samples via two separate models that can be appropriate in different applications.

We derive the minimal sampling rate allowing for perfect reconstruction of the signal's cyclic spectrum considering both sparse and non sparse signals as well as blind and non blind detection in the sparse case. We show that frequency shapeable ADCs can be used to achieve robust detection at sub-Nyquist rates. Simulations reported in Fig. 1 show that our detector outperforms energy detection at low SNRs and at a much lower rate than traditional Nyquist-rate sampling [1]. The figure shows the ROC curves using our ADC structure when sampling a wideband signal at 1/10th of the Nyquist rate for different SNRs. The student working on this project is Deborah Cohen. She is assisted in the lab by Idan Shmuel and Alon Eilam.

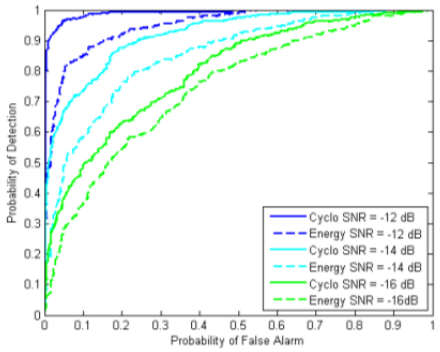

Figure 1: ROC curves of our sub-Nyquist receiver operating at 1/10th of the Nyquist rate at low SNR. We compare energy based detection with cyclo stationary based detection.

Chip design: We have been considering applying the frequency-shapeable ADC to LTE advanced in detection mode. This will allow us to detect signals by sampling at much lower rates than allowed for today. In the chip design we assume detection mode when the carriers are known. The design is based on combining novel circuit tools together with signal processing algorithms to maximize the ability for interference rejection based on single harmonic rejection. Our design uses a 3-level mixing sequence where we adjust the levels that are nominally zero in order to attenuate undesired harmonics. We then enhance the harmonic cancelation using an additional branch with a 180 phase delay. We are now working on algorithms for proper calibration.

Nonlinear distortions: Nonlinearities are prominent in communicatio circuits. In the upcoming year we intend to study these in detail within our framework. As a first step we developed efficient algorithms to recover sparse signals from nonlinear samples [2].

Keywords: Sub-Nyquist sampling, cognitive radio, LTE advanced, nonlinear distortions

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] D. Cohen et al.,"Cyclostationary Detection from Sub-Nyquist Samples for Cognitive Radios: Models Reconciliation", to appear in camsap 2013.

[2] A. Beck and Y. C. Eldar, "Sparsity Constrained Nonlinear Optimization: Optimality Conditions and Algorithms", to appear in SIAM Optimization.

TASK 1836.117, PERFORMANCE AND RELIABILITY ENHANCEMENT OF EMBEDDED ADCS WITH VALUE-ADDED BIST

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SIGNIFICANCE AND OBJECTIVES

The objective is to develop a practical method for on-chip BIST for linearity testing of high performance embedded ADCs with minimal area overhead for the BIST circuitry. A second objective is to provide added value with the BIST capability by enhancing linearity performance through BIST-based calibration.

TECHNICAL APPROACH

Highly nonlinear and unknown but very small on-chip Functionally Related Excitations (FRE) will be generated for linearity testing of the ADC. A Stimulus Error Identification and Removal (SEIR) algorithm, previously validated for ATE-based testing, will be used to correct for errors that would otherwise be introduced with unknown nonlinear excitations. The FRE/SEIR approaches will be combined to provide a BIST capability. Added value will be provided by enhancing the linearity performance of the ADC with a BIST-based calibration algorithm driven by data obtained from the BIST process.

SUMMARY OF RESULTS

A small and simple multi-ramp nonlinear triangle wave generator has been developed that can be used for the on-chip generation of the nonlinear and unknown input signals needed for linearity testing of the ADC. Multiple ramps rather than a single ramp are used to keep the size of the on-chip capacitor needed for the ramp generator small.

The level shift operation will be used to generate the Functionally Related Excitations. When the level shift operation is used to create the FRE excitations, a tradeoff between generating a linear input ramp for generating a constant shift is made. This tradeoff is justifiable only if the constancy of the shift is easier to implement than the linearity of the ramp signal. Several different level shifters have been designed that exploit the offset voltage of an operational for the creation of a level shift. Specifically, a small but programmable offset voltage is incorporated into the design of an operational amplifier to provide a level shift in the output voltage. Whereas it is extremely difficult to generate a ramp signal that is sufficiently linear for BIST of 12-bit and higher resolution ADCs, it can be shown that the simple level shifters that have been designed are sufficiently constant for testing 12-bit and higher resolution ADCs.

A method for modifying an existing 12-bit ADC internal to the MSP 430 to provide two additional bits of resolution with almost no area overhead has been developed. The two additional bits of resolution will be useful for enhancing the performance with the BIST-based calibration algorithm that will be developed.

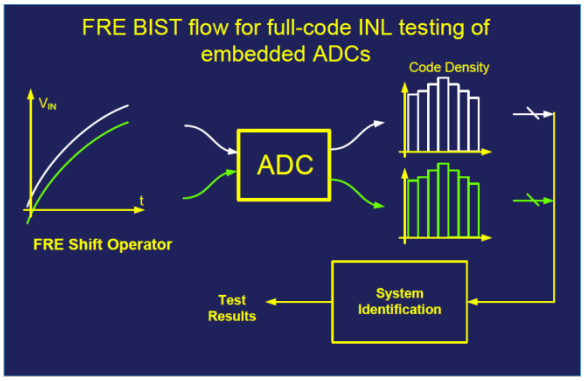

Figure 1: Testing of embedded ADCs with nonlinear Functionally Related Excitations (FRE)

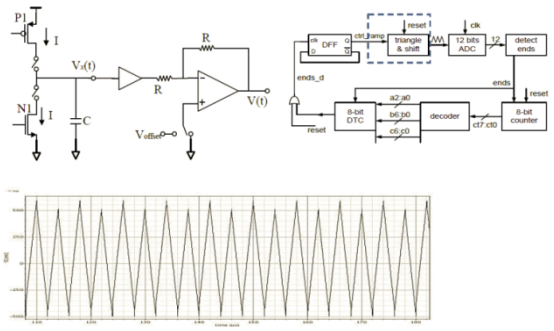

Figure 2: Multi-ramp nonlinear triangle wave generator

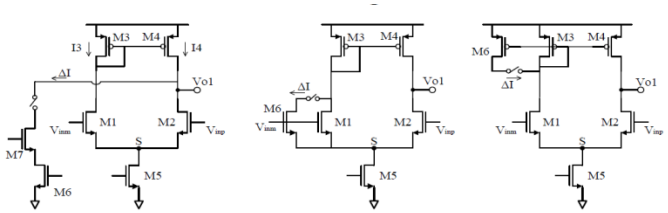

Figure 3: Op Amps for Generating Constant Shift Excitations

INDUSTRY INTERACTIONS

Texas Instruments and Freescale

MAJOR PAPERS/PATENTS

Appendix I Publications of TxACE Researchers

Conference Publications

(1) M. Majzoobi, M. Rostami, F. Koushanfar, D. S. Wallach, and S. Devadas, "Slender PUF Protocol: A lightweight, robust, and secure authentication by substring matching," IEEE Security and Privacy Workshop on Trustworthy Embedded Devices, May 2012.

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(5) S. Aroor, B. Faheem, R. Pierce, A. Blanchard, R. Henderson, “RF Integration Components for a System-in-Package Solution for 60 GHz Applications using FR4 Laminates,” ICUWB 2012.

(6) Dongkyung Park and Hoi Lee, "A 40V 10W 93%-efficiency current-accuracy-enhanced dimmable LED driver with adaptive timing difference compensation for solid-state lighting applications," IEEE Custom Integrated Circuits Conference, Sep. 2013, accepted for publication.

(7) Kristoffer Flores and Hoi Lee, "An auto-reconfigurable load-dependent wireless power receiver for biomedical implants," SRC TECHCON, Sep. 2013, accepted for publication.

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(17) S. Lai, B. Yan and P. Li, “Stability Assurance and Design Optimization of Large PDNs with Multiple On-chip LDOs,” IEEE/ACM ICCAD, 2012 (Best Paper Award).
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