TEXAS ANALOG CENTER

TEXAS ANALOG CENTER OF EXCELLENCE

Annual Report 2017 – 2018

SRC®

TxACE
TEXAS ANALOG
CENTER OF EXCELLENCE

TxACE MISSION

The Texas Analog Center of Excellence seeks to create fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, health care, and public safety and security.

TxACE THRUSTS

- *Safety, Security and Health Care*
- *Energy Efficiency*
- *Fundamental Analog Circuits*

TxACE 2017-2018 ANNUAL REPORT

The Texas Analog Center of Excellence (TxACE), located at the University of Texas at Dallas is the largest analog research center based in an academic institution. Analog and mixed signal integrated circuits engineering is both a major opportunity and challenge. Analog circuitry is a critical component of nearly every product of the $400+ billion per year integrated circuits industry, as a part of sensing, actuation, communication, power management and others. Digital integrated circuits such as microprocessors, logic circuits and memories are now integrating analog functions such as input/output circuits, phase locked loops, temperature sensors and power management circuits. It is also common to find microcontrollers with multiple analog-to-digital and digital-to-analog converters. These circuitries impact almost all aspect of modern life: safety security, health care, transportation, energy, entertainment and others.

Creation of advanced analog and mixed signal circuits and systems depends on the availability of engineering talent for analog research and development. TxACE was established to help translate the opportunity into economic benefits by overcoming the challenge and meeting the need. TxACE was established through a collaboration of the state of Texas, Texas Instruments, the Semiconductor Research Corporation, the University of Texas System, and The University of Texas at Dallas.

The research tasks are organized into three research thrust areas: Safety, Security and Health Care, Energy Efficiency and Fundamental Analog. The scope of investigation extends from circuits operating at dc through terahertz, data converters that sample at a few samples/sec to 10's of Giga-samples/sec, AC-to-DC and DC-to-AC converters working at µW to Watts, energy harvesting circuits, sensors and many more. Significant improvements to existing mixed signal systems and new applications have been made and continued to be anticipated. Students who have been exposed to hands-on innovative research are forming the leading edge of analog talent flow into the industry. Close collaboration with and responsiveness to industry needs provide focus to the educational experience.

DIRECTOR'S MESSAGE

The Texas Analog Center of Excellence (TxACE) is leading analog research and education. As of October 14th of this year, the Center is 10 years young. Over the past 10 years, TxACE has supported research for 121 PI's and Co-PI's at 44 institutions all over the globe. Seven of them were from the State of Texas (SMU, Rice, Texas A&M, Texas Tech, UNT, UT Austin, UT Dallas). Almost 200 Ph.D., 72 M.S. and 38 B.S. degrees were awarded to TxACE supported students. TxACE has published 661 conference papers and 212 journal papers. TxACE faculty members have started three companies (Movellus, Formula Electronics, Insilixa) and TxACE has issued 16 IP license agreements. Our works on IC testing, clock generation, I/O circuits, power management circuits, and millimeter wave circuits and systems have been incorporated into the products and engineering processes of member companies.

This year the Center together with SRC, its member companies and other agencies has been brain storming on the future research directions. Some key research directions under consideration are advanced sensors, analog-digital mixed signal hybrid computing to improve energy efficiency of artificial intelligence, security of mixed signal hardware, and using these technologies to foresee the future to prevent failures or mitigate their impact.

The Center is continuing to excel in research. As always, there are too many accomplishments in the past year to list all here. A selected list includes demonstrations of a 56Gb/s mixed-signal PAM4 quarter-rate receiver employing a single-stage CTLE and a DFE with 1 FIR and 1 IIR-tap to efficiently compensate for more than 20dB channel loss while achieving an energy efficiency of 4.63mW/Gb/sec, a sub-baud rate clock data recovery circuit that improves energy efficiency of I/O's, a technique that reduces the startup time of crystal oscillator by 15X, and techniques that suppress spurs by 15dB and improve the phase noise by a maximum of 25 dB at offset frequencies between 4MHz-200MHz from a 1.4-GHz carrier.

The TxACE laboratory is continuing to help advance integrated circuit research by making its instruments and expertise available to researchers and our industrial partners all over the world.

I would like to thank the students, principal investigators and staff for their efforts, and UT Dallas, the University of Texas System, TI, and SRC, as well as many friends of TxACE all over the world for their generous support. As we start our 2nd decade, I look forward to working with the TxACE team to make our world better through our research, education and innovation.

Kenneth K. O, Director TxACE
Texas Instruments Distinguished
University Chair Professor
The University of Texas at Dallas

BACKGROUND & VISION

The $400+ billion per year integrated circuits industry is evolving into an analog/digital mixed signal industry. Analog circuits are providing or supporting critical functions such as sensing, actuation, communication, power management and others. These circuits impact almost all aspect of modern life including safety, security, health care, transportation, energy, and entertainment. To lead this change, in particular to lead analog and mixed signal technology education, research, commercialization, manufacturing, and job creation, the Texas Analog Center of Excellence was announced by Texas Governor Rick Perry in October 2008 as a collaboration of the Semiconductor Research Corporation, state of Texas through its Texas Emerging Technology Fund, Texas Instruments Inc., University of Texas system and University of Texas at Dallas. The Center seeks to accomplish the objectives by creating fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, healthcare, and public safety and security as well as by improving the research and educational infrastructure.

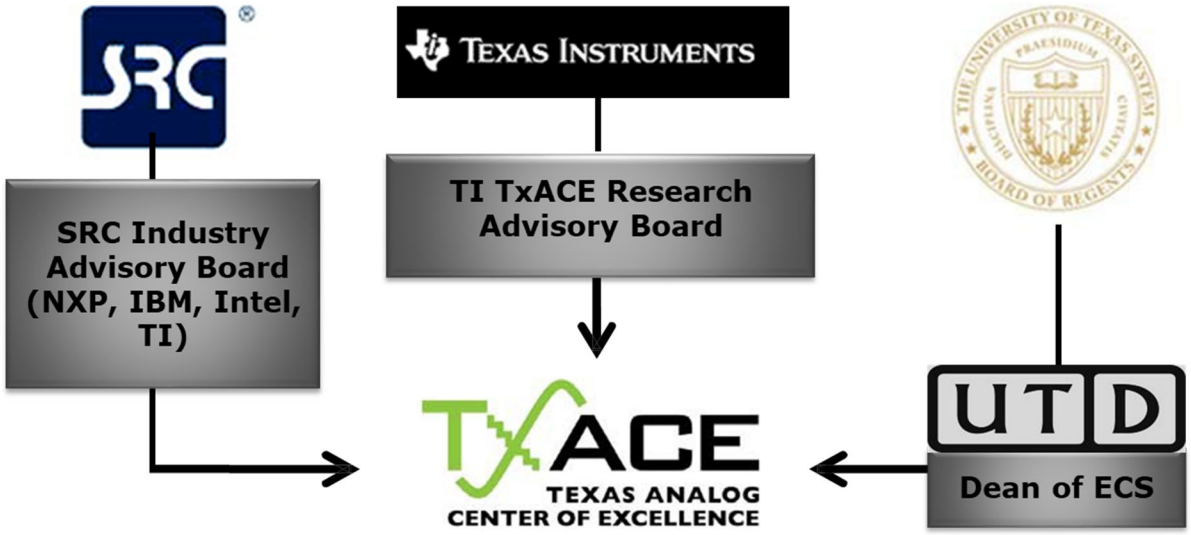


Figure 1. TxACE organization relative to the sponsoring collaboration (2017-2018).

CENTER ORGANIZATION

The Texas Analog Center of Excellence is guided by agreements established with the Center sponsors. Members of the industrial advisory boards identify the research needs and select research tasks in consultation with the Center leadership. Figure 1 diagrams the relationship of TxACE to the members of the sponsoring collaboration.

The internal organization of the Center is structured to flexibly perform the research mission while fully embracing the educational missions of the Universities.

Figure 2 shows the center management structure. The TxACE Director is Professor Kenneth O. The research is arranged into three thrusts that comply with the center mission: Safety, Security and Health Care, Energy Efficiency and Fundamental Analog Research. The third thrust consists of vital research that cuts across the first two research thrusts. The thrust leaders are Prof. Yiorgos Makris of the University of Texas at Dallas for safety, security and health care, and Prof. Ali Niknejad of the University of California, Berkeley for energy efficiency. The leader for fundamental analog is Prof. Pavan Hanumolu of University of Illinois, Urbana-Champaign. The thrust leaders along with Professor Dongsheng Ma of the The University of Texas at Dallas form the executive committee. The committee, along with the director, forms the leadership team that works to improve the research productivity by increasing collaboration, better leveraging the diverse capabilities of principle investigators of the Center, and lowering research barriers. The leadership team also identifies new research opportunities for consideration by the Industrial Advisory Boards.

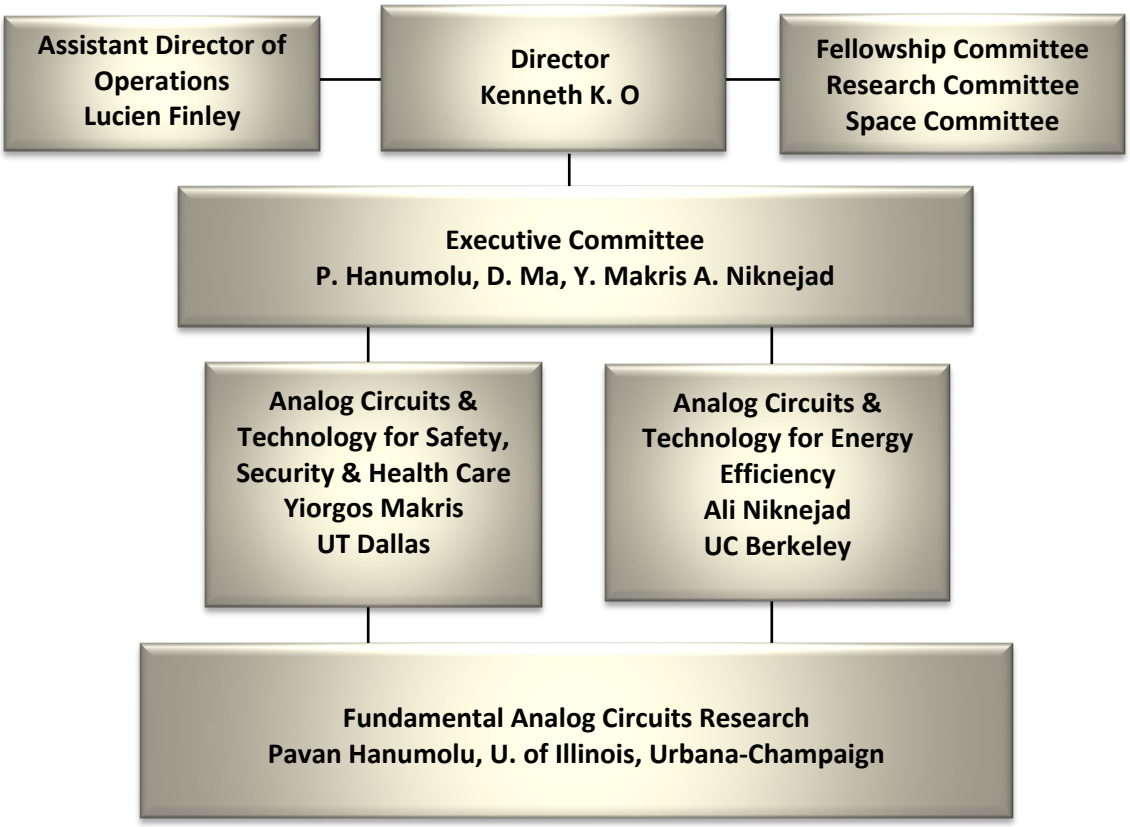


Figure 2. TxACE organization for management of research

SAFETY, SECURITY & HEALTH CARE

(Thrust leader: Yiorgos Makris, University of Texas at Dallas)

TxACE is developing analog technology that enhances public safety and security, and health care. The projects are intended to enable a new generation of devices that can scan for harmful substances by researching 200-300 GHz silicon ICs for use in spectrometers as well as a CO_2 sensor. The ICs and CO_2 sensor can also be used to analyze breaths for medical applications. The thrust is also working to significantly reduce the cost of millimeter wave imaging and on-vehicle radar technology for automotive safety by researching signal processing techniques that reduce system complexity. This thrust is also investigating vibration sensors and sensing techniques to monitor health of motors and mixed signal circuits including power devices. This thrust also includes research tasks on mixed signal hardware security.

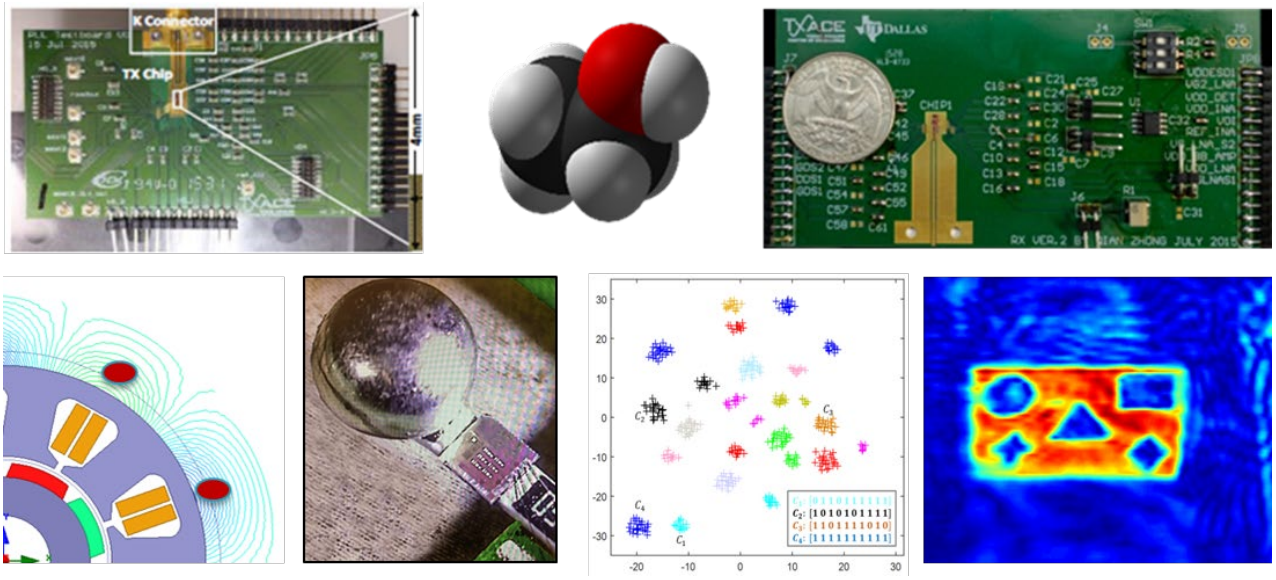


Figure 3. (Top) 200-260 GHz CMOS transmitter and receiver for rotational spectroscopy (K. O, W. Choi, UT-Dallas), (Bottom left) Simulated flux leakage in a motor (B. Akin, UT-Dallas), (Bottom left center) Vibration sensor compatible with conventional silicon IC and packaging technologies (S. Pourkamali, UT Dallas), (Bottom right center) Projected e-test space, where each point represents a wafer. A proper test flow to each process signature of each wafer is assigned to maximize the test cost reduction while maintaining the test escape rate below a target level. (Y. Makris, UT-Dallas), (Bottom right) Automotive radar image (M. Torlak, UT-Dallas).

ENERGY EFFICIENCY

(Thrust leader: Ali Niknejad, UC Berkeley)

TxACE is committed to alleviate the global energy problem by improving the energy efficiency of electronic systems as well as by developing analog technologies that can make energy generation and distribution more efficient. The Center is also working to energize and power long-lasting in-situ microscale devices such as wireless microsensors, biomedical implants, and portable microelectronics.

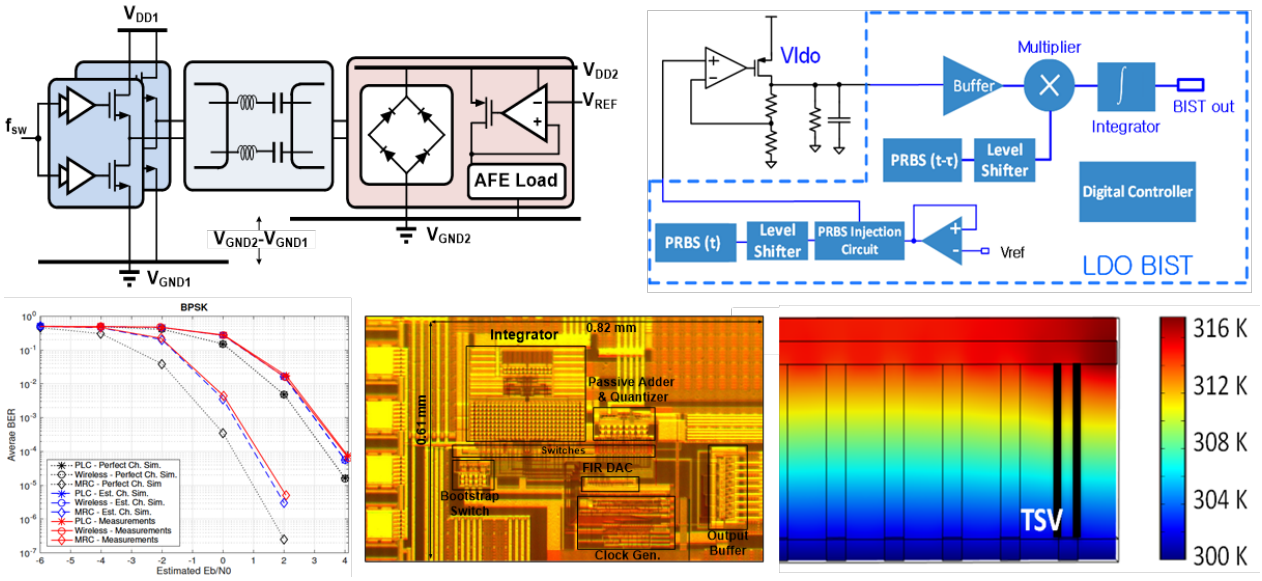


Figure 4. (Top left) Resonant converter for isolated power transfer (B. Ma, UT-Dallas), (Top right) Dynamic BIST for LDO's (S. Ozev, Arizona State U.), (Bottom left) BER versus SNR for PLC/Wireless receiver combining techniques based on maximal-ratio-combining that take into account the impulsive nature of noise on the two links (N. Al-Dhahir, UT-Dallas, B. Evans, UT-Austin), (Bottom center) Micro-power three step incremental ADC (G. Temes, Oregon State U.), (Bottom right) Simulated cross-sectional temperature distribution in a 8-row TSV arrangement (J. Lee, N. Bagherzadeh, UC-Irvine).

FUNDAMENTAL ANALOG CIRCUITS RESEARCH

(Thrust leader: Pavan Hanumolu, U. of Illinois Urbana-Champaign)

Research in this thrust focuses on cross-cutting areas in analog Circuits which impact all of the TxACE application areas (Energy Efficiency, Public Safety and Security, Health Care). The list of research includes design of a wide variety of analog-to-digital converters, communication links, temperature sensors and I/O circuits, development of CAD tools, and testing of integrated circuits.

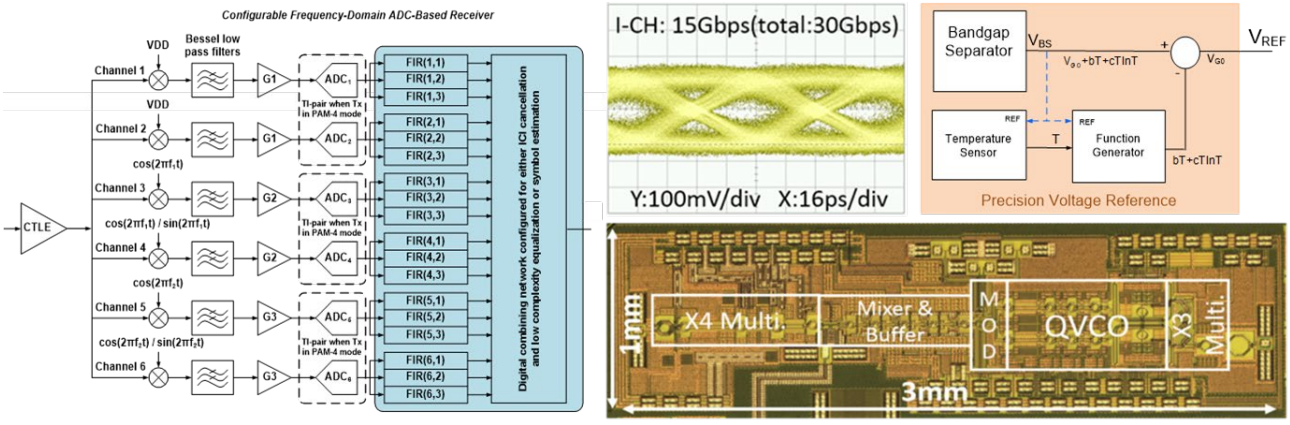


Figure 5. (Left) Configurable frequency-domain ADC-based receiver (S. Palermo, Texas A&M), (Top center and Bottom right), 30-Gbps data from a 300-GHz QPSK transmitter (K. O, UT Dallas), (Top right) Precision Voltage Reference using Bandgap Separator and thermal Function Generator (R. Geiger, Iowa State U.).

TXACE ANALOG RESEARCH FACILITY

The centralized group of laboratories of the Texas Analog Center of Excellence dedicated to analog engineering research and training occupy a ~8000 ft^2 area on the 3rd floor of the Engineering and Computer Science North building (Figure 6). The facility includes RF and THz, Integrated System Design, Embedded Signal Processing, and Analog & Mixed Signal laboratories as well as CAD/Design laboratory structured to promote collaborative research**.** The unique instrumentation capability includes network analyses and linearity measurements up to 325 GHz, spectrum analysis up to 120 THz, and cryo-measurements down to 2^{o}K. The Center also added a pulsed multiple harmonic load and source pull measurement set up (up to 60 GHz for the third harmonic) and a 325-GHz antenna measurement set up. The close proximity of researchers in an open layout enables natural interaction and compels sharing of knowledge and instrumentation among the students and faculty. The TxACE analog research facility is one of the best equipped electronics laboratories. The laboratory is available for use by TxACE researchers and industrial partners all over the world.

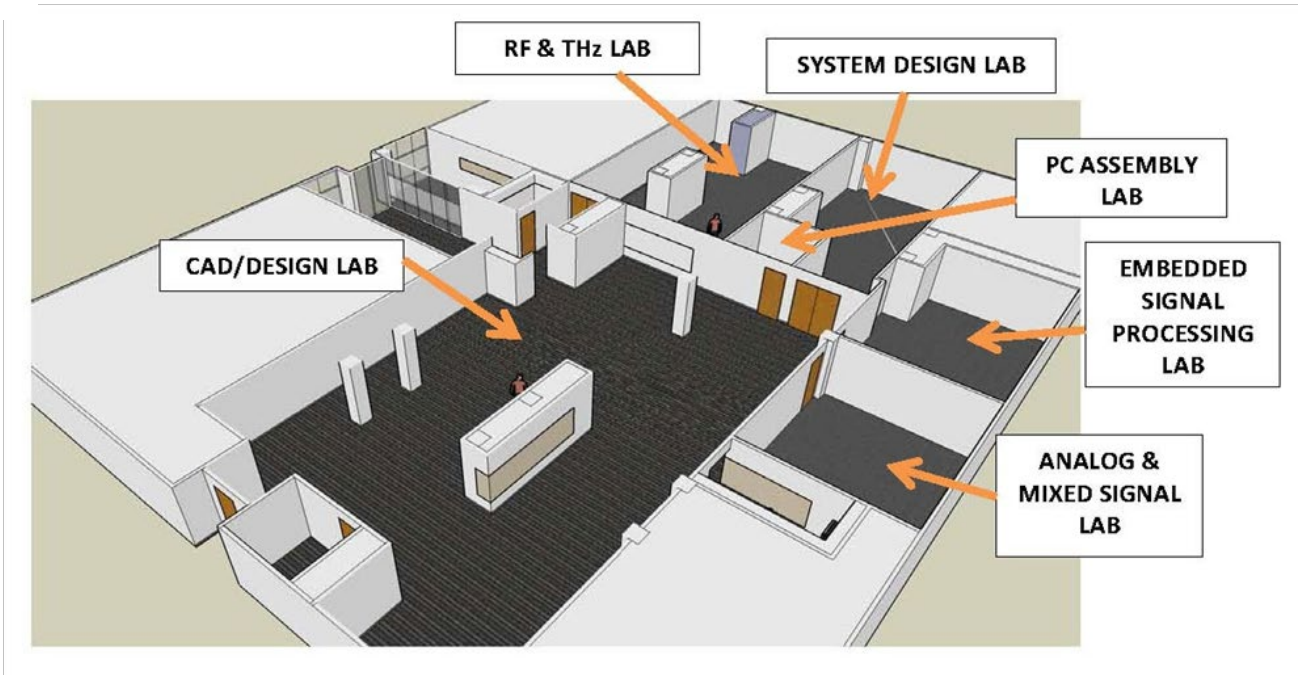


Figure 6. TxACE Analog Research Facility

RESEARCH PROJECTS AND INVESTIGATORS

The Texas Analog Center of Excellence (TxACE) is the largest university analog technology center in the world. Table 1 lists the current principal investigators of the 67 tasks from 25 academic institutions funded by TxACE. Four universities (SMU, Texas A&M, UT Austin, UT Dallas) are from the state of Texas. Eighteen are from outside of Texas. One (Delft University of Technology) (Figure 7) is from outside of the US. Of the 59 investigators, 21 are from Texas. During the past year, the Center supported 136 Ph.D., 19 M.S., and 14 B.S. students. Twenty-one Ph.D. and seven M.S. degrees were awarded to the TxACE students.

Investigator	Institution	Investigator	Institution	Investigator	Institution
B. Akin	UT Dallas	M. Johnston	UT Dallas	S. Pourmakali	UT Dallas
N. Al-Dhahir	UT Dallas	C. Kim	U Minnesota	S. Prasad	UT Dallas
S. Ang	U Arkansas	M. Kim	UT Dallas	A. Raychowdhury	Georgia Tech
N. Bagherzadeh	UC Irvine	P. Kinget	Columbia	E. Rosenbaum	UIUC
S. Bhunia	U Florida	G. Lee	UT Dallas	A. Sanyal	SUNY
D. Blaauw	U Michigan	J. Lee	UC Irvine	V. Sathe	U Washington
C. Busso	UT Dallas	P. Li	Texas A&M	P. Schaumont	Virginia Tech
A. Chatterjee	Georgia Tech	D. Ma	UT Dallas	K. Sengupta	Princeton
D. Chen	Iowa State	D. Macfarlane	SMU	M. Seok	Columbia
Z. Chen	U Arkansas	N. Maghari	U Florida	H. Shichijo	UT Dallas
Y. Chiu	UT Dallas	K. Makinwa	Delft Univ	N. Sun	UT Austin
F. De Lucia	Ohio State	Y. Makris	UT Dallas	M. Swaminathan	Georgia Tech
W. Eisenstadt	U Florida	Y. Menguc	Oregon State	D. Sylvester	U Michigan
B. Evans	UT Austin	U-K Moon	Oregon State	G. Temes	Oregon State
M. Flynn	U Michigan	S. Mukhpadhyay	Georgia Tech	M. Torlak	UT Dallas
R. Geiger	Iowa State	A. Nikejad	UC Berkeley	A. Trivedi	U. of Illinois, Chicago
P. Gui	SMU	B. Nikolic	UC Berkeley	X. Zhang	Wash., St. Louis
P. Hanumolu	UIUC	K.K. O	UT Dallas		
R. Harjani	U Minnesota	S. Ozev	Arizona State		
R. Henderson	UT Dallas	S. Palermo	Texas A&M		
S. Hoyos	Texas A&M	S. Pamarti	UCLA		

Table 1. Principal Investigators (September 2017 through August 2018)

Figure 7. Member Institutions of Texas Analog Center of Excellence

SUMMARY OF RESEARCH PROJECTS

The 67 research projects funded through TxACE during 2017-2018 are listed in Table 2 below by the Semiconductor Research Corporation task identification number.

Table 2: Funded research projects at TxACE by SRC task identification number (FA: Fundamental Analog, EE: Energy Efficiency, SS: Safety, Security and Health Care)

	Task	Thrust	Title	Task Leader	Institution
1	1836.117	SS	Performance and Reliability Enhancement of Embedded ADCS with Value-Added BIST	Geiger, Randall	Iowa State
2	1836.126	SS	Design Spin Reduction via Integrated THz Design: Applications, Physics, and System Engineering	De Lucia, Frank	Ohio State
3	1836.127	FA	Precision Test without Precision Instruments – A Necessity for Future On-Chip Self-Test and Self Healing	Chen, Degang	Iowa State
4	1836.130	EE/SS	Built-In Self-Test Techniques for Test, Calibration, and Trimming of Power	Ozev, Sule	Arizona State
5	1836.133	EE	Energy-Efficient Signal Processing Techniques for Smart Grid Heterogeneous Communications Networks	Al-Dhahir, Naofal	UT dallas
6	1836.134	FA	Hybrid Two-Step PLLs for Digital SoCs in Nanoscale CMOS	Kinget, Peter	Columbia
7	1836.136	FA	Injection-Locked Ring Oscillators for Clock Distribution in Manycore Processors	Nikolić, Borivoje	UC Berkeley
8	1836.137	FA/EE	50GS/s and Beyond Frequency-interleaved Energy-Efficient ADCs	Niknejad, Ali	UC Berkeley
9	1836.139	EE	Enabling Fully-Integrated VHF Clk-Sync Multiphase Switching Regulators on Silicon	Ma, Dongsheng	UT Dallas
10	1836.140	EE	Embedded & Adaptive Voltage Regulators with Proactive Noise Reduction for Digital Loads Under Wide Dynamic Range	Raychowdhury, Arijit	Georgia Tech
11	1836.143	FA/EE	Design Techniques for Modulation-Agile and Energy-Efficient 60+Gb/s Receiver Front-Ends	Palermo, Samuel	Texas A&M
12	1836.146	EE	On-Chip AC-DC Power Conversion with Ground Disturbance Shielding for Environmental Sensing Applications	Ma, Dongsheng	UT Dallas
13	1836.148	FA	50GSPS+ TI Hybrid SAR ADC Array with Comprehensive DDI Calibration	Chiu, Yun	UT Dallas
14	1836.149	SS	Condition Monitoring of PM/IPM Motors through Axial/Radial Leakage Flux	Akin, Bilal	UT Dallas
15	1836.150	SS	Robust High Resolution Techniques for Millimeter Wave Radars in Complex Environments	Torlak, Murat	UT Dallas
16	1836.152	FA	Feasibility of CMOS Transmitter and Receiver for 500-Gbps Communication over Dielectric Waveguide	O, Kenneth K.	UT Dallas
17	1836.153	EE	High-Speed Compact Power Supplies For Ultra-Low-Power Wireless Sensor Applications	Ma, Dongsheng	UT Dallas

	Task	Thrust	Title	Task Leader	Institution
18	1836.154	SS	State of The Health (SOH) for IGBTS: Incipient Fault Characterization and Degradation Monitoring	Akin, Bilal	UT Dallas
19	1836.155	SS	Development of Wideband Vibration Sensors Based On Existing Process Platforms	Pourkamali, Siavash	UT Dallas
20	1836.156	FA	Transition Design for High Data Rate Links at Submillimeter Wave Frequencies	Henderson, Rashaunda	UT Dallas
21	1836.157	FA	CMOS GSPS 12-Bit SAR ADC Array With On-Chip Reference Buffers	Chiu, Yun	UT Dallas
22	1836.158	FA	Development of Dielectric Waveguides for THz Radiation Applications	Macfarlane, Duncan	SMU
23	2712.002	EE/SS	On-line Self-Testing and Self-Tuning of Integrated Voltage Regulators	Mukhopadhyay, Saibal	Georgia Tech
24	2712.003	SS	Multi-Modal BIST Design and Test Metrics Evaluation for Analog/RF Circuits	Ozev, Sule	Arizona State
25	2712.004	FA	Hierarchical Analog and Mixed-Signal Verification Using Hybrid Formal and Machine Learning Techniques	Li, Peng	Texas A&M
26	2712.005	FA	Automated Cross-Level Validation and Debug of Mixed-Signal Systems in Top-Down Design: From Pre-Silicon to Post-Silicon	Chatterjee, Abhijit	Georgia Tech
27	2712.006	EE	Robust, Efficient All-Digital SIMO Converters for Future SOC Domains	Sathe, Visvesh	U. Washington
28	2712.007	FA	High-Resolution Low-Voltage Hybrid ADCs for Sensor Interfaces	Flynn, Michael P.	U. Michigan
29	2712.008	EE	Direct-Battery-to-Silicon Power Transfer in Advanced Nanometer CMOS	Harjani, Ramesh	U. Minnesota
30	2712.009	EE	Low Power Area Efficient Flexible-rate Energy Proportional Serial Link Transceivers	Hanumolu, Pavan Kumar	UIUC
31	2712.010	FA	Ringamp-assisted Circuits/Techniques and Next-generation Ringamps	Moon, Un-Ku	Oregon State U.
32	2712.011	FA	Robust Reliable and Practical High Performance References in Advanced Technologies	Geiger, Randall L.	Iowa State
33	2712.012	EE	EDAC and DC-DC-Converter Co-Design for Addressing Robustness Challenges in Emerging Architectures	Seok, Mingoo	Columbia
34	2712.013	SS	Generalized Reconfigurable MM-Wave Tx Architecture and Antenna Interface with Active Impedance Synthesis	Sengupta, Kaushik	Princeton
35	2712.014	FA	Leveraging CMOS Scaling in High Performance ADCS	Maghari, Nima	U. Florida
36	2712.015	SS	Area-Efficient On-Chip System-Level IEC ESD Protection for High Speed Interface ICs	Chen, Zhong	U. Arkansas
37	2712.016	EE	3D IC Thermal Management Based on TSV Placement Optimization and Novel Materials	Lee, Jaeho	UC Irvine
38	2712.017	SS	Mitigating Reliability Issues in Analog Circuits	Kim, Chris H.	U. Minnesota
39	2712.018	SS/EE	Test Techniques to Approach Several Defect-per-billion for Power ICs	Eisenstadt, William	U. Florida
40	2712.019	SS/EE	Pre-computed Security Protocols for Energy	Schaumont, Patrick	Virginia Tech

	Task	Thrust	Title	Task Leader	Institution
41	2712.020	FA	Low-Power Mostly Digital Time-Domain Delta-Sigma ADCs for IoTs	Sanyal, Arindam	SUNY at Buffalo
42	2712.021	SS	Distributed Silicon Circuits and Sensors in 3D-Printed systems for wearable IoT sensors	Johnston, Matthew	Oregon State
43	2712.022	SS	Intrinsic identifiers for Database-Free Remote Authentication of IoT Edge Devices	Trivedi, Amit R.	U. of Florida
44	2712.023	FA	Ultra-Low-Power Compressive Sensing Techniques for IoT Applications	Sun, Nan	UT Austin
45	2712.024	EE	A System-In-Package Platform for Energy Harvesting and Delivery for IoT Edge Devices	Mukjopadhyay, Saibal	Georgia Tech
46	2712.025	FA	Reduction of Low Frequency Noise Impact in Nano-scale CMOS Circuits	O, Kenneth	UT Dallas
47	2712.026	SS	Fault Characterization and Degradation Monitoring of SiC Devices	Akin, Bilal	UT Dallas
48	2712.027	EE	Gate Driving Techniques and Circuits for Automotive-Use GaN Power Circuits	Ma, Dongsheng	UT Dallas
49	2712.028	EE	High Performance Micro-supercapacitor on a Chip Based on a Hierarchical Network of Nitrogen Doped Carbon Nanotube Sheets Supported MnO2 Nanoparticles	Lee, Gil	UT Dallas
50	2712.029	SS	Novel Super-resolution and MIMO Techniques for Automotive and Emerging Radar Applications	Torlak, Murat	UT Dallas
51	2712.030	SS	Performance of Carbon Dioxide CO_2 Gas Sensors	Prasad, Shalini	UT Dallas
52	2712.031	FA	Adaptive Trimming and Testing of Analog/RF Integrated Circuits (ICs)	Makris, Yiorgos	UT Dallas
53	2810.002	SS/EE	Security-Aware Dynamic Power Management for System-on-Chips	Mukhopadhyay, Saibal	Georgia Tech
54	2810.003	EE	Integrated Voltage Regulator Management for System-on-Chip Architectures	Zhang, Xuan	Washington Univ., St. Louis
55	2810.005	SS	Circuit Design for ESD and Supply Noise Mitigation	Rosebaum, Elyse	UIUC
56	2810.006	EE	Combating Unprecedented Efficiency, Noise and Frequency Challenges in Modern High Current Integrated Power Converters	Ma, Dongsheng	UT Dallas
57	2810.007	FA	Fully Integrated Phase Noise Cancellation Techniques	Niknejad, Ali M.	UC Berkeley
58	2810.008	EE	Circuit Techniques for Fast Start-Up of Crystal Oscillators	Pamarti, Sudhakar	UCLA
59	2810.009	EE/FA	Mixed-Signal Building Blocks for Ultra-Low Power Wireless Sensor Nodes	Blaauw, David T.	U. of Michigan
60	2810.010	EE	GS/s ADC Based Cycle-to-Cycle Closed Loop Adaptive Smart Driver for High-Performance SiC/GaN Power Devices	Gui, Ping	SMU
61	2810.011	FA	Micro-Power Analog-to-Digital Data Converters for Sensor Interfaces	Temes, Gabor	Oregon State
62	2810.012	FA	NPSense-Nano-Power Current Sensing	Makinwa, Kofi	Delft University
63	2810.013	SS	Frequency-Domain ADC-Based Serial Link Receiver Architectures for 100+Gb/s Serial Links	Palermo, Samuel	Texas A&M
64	2810.014	SS	Deep Learning Solutions for ADAS: From Algorithms to Real-World Driving Evaluations	Busso, Carlos	UT Dallas
65	2810.015	FA	Demonstration of 120-Gbps Dielectric Waveguide Communication Using Frequency Division Multiplexing (FDM) and Polarization Division Multiplexing (PDM)	O, Kenneth	UT Dallas

	Task	Thrust	Title	Task Leader	Institution
66	2810.016	SS	Condition Monitoring of Industrial/Automotive Drive Components through Leakage Flux	Akin, Bilal	UT Dallas
67	2810.017	SS	Reliability Study of E-mode GaN HEMT Devices	Kim, Moon	UT Dallas

ACCOMPLISHMENTS

In the past year, TxACE has made significant research progress. Table 3 summarizes the number of publications and inventions resulting from the TxACE research during May 2017 to April 2018, while Table 4 lists the major research accomplishments for the Center during the period. The TxACE researchers have published 47 conference papers, 20 journal papers, and 2 books/chapters. They have also made five invention disclosures, filed three patents, and were granted one patent. The list of publications is included as Appendix I. Following the tabulation, brief summaries of each project are provided.

Table 3. TxACE number of publications (May 2017 through April 2018)

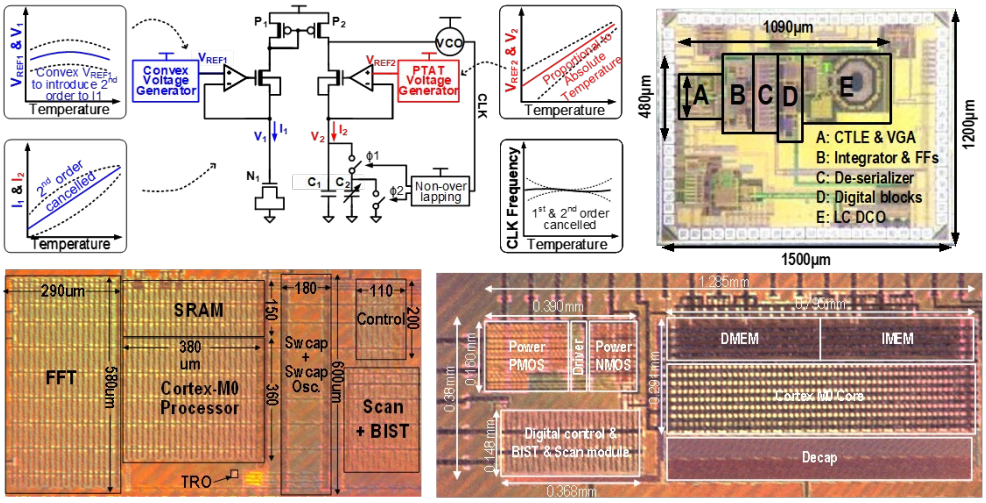
Conference Papers	Journal Papers	Books/Chapters	Invention Disclosures	Patents Filed	Patents Granted
47	20	2	5	3	1

Table 4. Major TxACE Research Accomplishments (May 2017 through April 2018)

Category	Accomplishment
Fundamental Analog (Circuits)	A mixed-signal PAM4 quarter-rate receiver employs a single-stage CTLE and a DFE with 1 FIR and 1 IIR-tap to efficiently compensate for more than 20dB channel loss. An edge-based sampler is used to perform both PLL-based CDR phase detection and adaptation of the DFE tap coefficients in background. Fabricated in GP 65-nm CMOS, the 56Gb/s receiver achieves 4.63mW/Gb/sec when operated with a 2-tap FFE transmitter. (1836.143, PI: Sam Palermo, Texas A&M)
Fundamental Analog (Circuits)	Techniques for spur and phase noise cancellation are developed. A delay-and-interpolate method introduces notches to suppress spurs. A delay-line discriminator extracts phase noise and a feed-forward loop cancels out input phase noise. Fabricated in a 65-nm CMOS process, the spurs are suppressed by more than 15dB and the phase noise at offset frequencies in the range of 4MHz-200MHz from a 1.4-GHz carrier is improved by a maximum of 25dB. (2810.007, PI: Ali Niknejad, UC Berkeley)
Fundamental Analog (Circuits)	A 300-GHz 30-Gbps QPSK transmitter consists of an on-chip multi-mode modulator, an injection locked quadrature oscillator, a 40-GHz bandwidth power amplifier with constant gain and group delay, a 4X frequency multiplier chain to generate a 165-GHz LO signal for a double balanced up-conversion mixer that generates the output at 300 GHz. The transmitter without equalization consumes 180mW with an energy efficiency of 6 pJ/bit. (1836.152, PI: Ken O, UT Dallas)
Safety, Security and Health Care (Systems)	Dynamic power management and security methods are both important for modern SoCs but have typically been developed independently. This task seeks to study the interplay between dynamic power management and security. Recent studies have demonstrated the effect of integrated voltage regulators and adaptive clocking-based voltage dithering on reducing information leakage through power and electromagnetic side channels in cryptographic cores. (2810.002 Mukhopadhyay, Georgia Tech)

Category	Accomplishment
Safety, Security and Health Care (Systems	Modeling aging effects as a function of their workload is imperative for evaluating reliability of analog/mixed-signal ICs. This task is developing dedicated test structures and in-situ monitoring circuits in order to measure BTI/HCI effects, along with simulation frameworks for projecting lifetime reliability and design guidelines for mitigating aging effects in analog/mixed-signal ICs. To date, an in-situ INL/DNL measurement block has been used for SAR-ADC DNL measurement, and the frequency and phase noise degradation of an all-digital PLL have been measured using simple on-chip monitoring circuits. (2712.017, Kim, U. of Minnesota)
Energy Efficiency (Circuits)	A novel gate-leakage-based frequency locking timer has been proposed that achieves 260ppm/^{o}C from -5^{o}C to 95^{o}C while only consuming 224 pW at 90-Hz output frequency and less than 1%/V supply dependence over a wide range of 1.1V-3.3V. The circuit uses 1st and 2nd order cancellation over temperature to realize the performance. (2810.009, D. Sylvester, U. Michigan)
Energy Efficiency (Systems)	IoT devices and sensor nodes must be able to wake up quickly and transmit and receive data in order to maximize energy efficiency. Crystal wakeup time is often the dominant limit due to the high Q of resonator. A technique that reduces the startup time by more than 15X over an extended temperature range is demonstrated. Techniques are being developed to relax the precision requirements of the injection oscillator. (2810.008, S. Pamarti, UCLA)
Energy Efficiency (Circuits)	Energy proportional links have the potential to greatly lower power consumption of practical systems where high power in the high speed links implies high efficiency only during high speed communication. A sub-baud rate clock and data recovery technique is being developed to further lower power consumption. To date a 15 Gb/s 1.9 pJ/b link has been demonstrated with a 15-MHz JTOL bandwidth. (2712.009, P. Hanumolu, UIUC)
Energy Efficiency (Circuits)	Efficient multi-voltage domain digital SoC power management is accomplished through integrated voltage regulation of fine-grained voltage domains using a resonant-clocked SIMO buck converter. Load regulation is solved by an accompanying unified clock-regulator architecture. A prototype in 65-nm CMOS utilizes a 64-bank 2:1 SC with continuous supply scalability. Droop margins and PVT variations on a Cortex M0 + FFT co-processor have been characterized with 94% average recovery of supply margins. A second test-chip demonstrates an all-digital single phase buck architecture with 82% recovery of voltage margins. (2712.006, V. Sathe, U. of Washington)

Energy Efficiency Thrust



Category	Accomplishment
Energy Efficiency (Circuits)	A novel gate-leakage-based frequency locking timer has been proposed that achieves 260ppm/°C from -5°C to 95°C while only consuming 224 pW at 90-Hz output frequency and less than 1%/V supply dependence over a wide range of 1.1V-3.3V. The circuit uses 1st and 2nd order cancellation over temperature to realize the performance. (2810.009, D. Sylvester, U. Michigan)
Energy Efficiency (Systems)	IoT devices and sensor nodes must be able to wake up quickly and transmit and receive data in order to maximize energy efficiency. Crystal wakeup time is often the dominant limit due to the high Q of resonator. A technique that reduces the startup time by more than 15X over an extended temperature range is demonstrated. Techniques are being developed to relax the precision requirements of the injection oscillator. (2810.008, S. Pamarti, UCLA)
Energy Efficiency (Circuits)	Energy proportional links have the potential to greatly lower power consumption of practical systems where high power in the high speed links implies high efficiency only during high speed communication. A sub-baud rate clock and data recovery technique is being developed to further lower power consumption. To date a 15 Gb/s 1.9 pJ/b link has been demonstrated with a 15-MHz JTOL bandwidth. (2712.009, P. Hanumolu, UIUC)
Energy Efficiency (Circuits)	Efficient multi-voltage domain digital SoC power management is accomplished through integrated voltage regulation of fine-grained voltage domains using a resonant-clocked SIMO buck converter. Load regulation is solved by an accompanying unified clock-regulator architecture. A prototype in 65-nm CMOS utilizes a 64-bank 2:1 SC with continuous supply scalability. Droop margins and PVT variations on a Cortex M0 + FFT co-processor have been characterized with 94% average recovery of supply margins. A second test-chip demonstrates an all-digital single phase buck architecture with 82% recovery of voltage margins. (2712.006, V. Sathe, U. of Washington)

TASK 1836.130, BUILT-IN SELF-TEST TECHNIQUES FOR TEST, CALIBRATION, AND TRIMMING OF POWER MANAGEMENT UNITS: PMU-BIST

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SIGNIFICANCE AND OBJECTIVES

This project aims at (a) enabling trimming and calibration of PMU/PMICs through static measurements using small footprint BIST circuitry, (b) enabling dynamic testing through open-loop measurements and mathematical modeling, (c) fault analysis and grading approaches to identify design and layout issues, and (d) correlating trim coefficients with measurements.

TECHNICAL APPROACH

We have divided this problem into two parallel threads. First, our goal was to implement a very small foot-print, low frequency analog to digital converter that works in a particular voltage range (1-1.4V) and provides 10 bits of resolution (INL<1mV). Another goal was to implement a dynamic built-in-self-test system for the converter loop to test phase margin in order to evaluate loop stability.

SUMMARY OF RESULTS

The zoom-in ADC was designed and taped out in 2016. The dynamic BIST system is shown in Figure 1. All of the system components are implemented in 40nm GF technology. The overall area of the BIST circuit is 0.019mm^2 and the evaluation time is 20ms. Figure 2 shows the layout of the LDO with BIST. Figure 3 shows the comparison of the BIST circuit response at various load current values to a more traditional technique for phase margin evaluation.

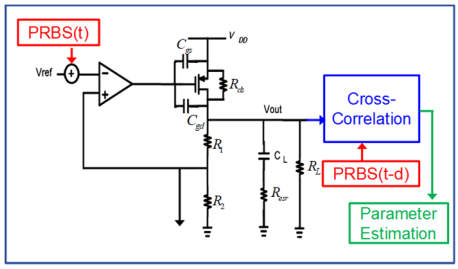

Figure 1. Dynamic BIST for LDOs.

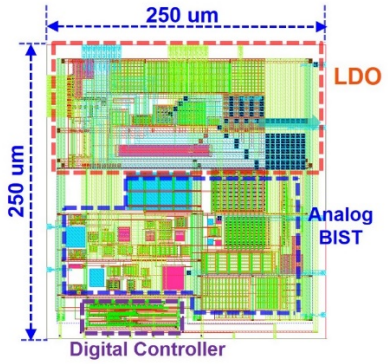

Figure 2. Layout and size for BIST and LDO.

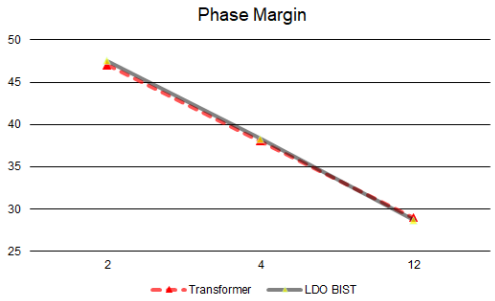

Figure 3. Hardware BIST results compared with loop analysis.

Keywords: BIST, PMU, phase margin, bandgap reference

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

[1] Navankur Beohar, Priyanka Bakliwal, Sidhanto Roy, Debashis Mandal, Bertan Bakkaloglu, Sule Ozev, "Disturbance-free BIST for Loop Characterization of DC-DC Buck Converters", IEEE VLSI Test Symposium, 2015. (Received best paper honorable mention award)

[2] Osman Emir Erol, Sule Ozev, Chandra Suresh, Rubin Parekhji, and Lakshmanan Balasubramanian. "On-chip measurement of bandgap reference voltage using a small form factor VCO based zoom-in ADC." IEEE Design, Automation & Test in Europe Conference, pp. 1559-1562, 2015.

[3] Liu, Tao, Chao Fu, Sule Ozev, and Bertan Bakkaloglu. "A built-in self-test technique for load inductance and lossless current sensing of DC-DC converters." IEEE VLSI Test Symposium (VTS), 2014. (Received Best paper award)

TASK 1836.133, ENERGY-EFFICIENT SIGNAL PROCESSING TECHNIQUES FOR SMART GRID HETEROGENEOUS COMMUNICATIONS NETWORKS

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BRIAN L. EVANS, UNIVERSITY OF TEXAS AUSTIN

SIGNIFICANCE AND OBJECTIVES

We propose a reliable hybrid power line and wireless communication transceiver to enhance the reliability of Smart Grid communications.

TECHNICAL APPROACH

We focus on the last mile communication link between the utility data concentrator and the residential smart meter. The transceiver is implemented over power lines in the narrowband 3-500 kHz frequency band and also over the unlicensed wireless frequency band from 902 MHz to 928 MHz. The interference on both links is impulsive in nature. To mitigate such impulsive noise on both links, we propose a hybrid PLC/wireless communication transceiver where both links carry the same information data. We present efficient receiver diversity combining techniques for the PLC and wireless signals that takes into account the impulsive nature of the interference.

SUMMARY OF RESULTS

We propose PLC/wireless receiver combining techniques based on maximal-ratio-combining (MRC) that take into account the impulsive nature of noise on the two links. In particular, for coherent modulation schemes, we present three PLC/wireless receiver combining techniques with different performance/complexity tradeoffs. For differential modulation, we propose a diversity combining technique based on the received signal power and the noise PSD which outperforms the conventional average SNR and equal gain combining techniques.

In addition, we implemented a flexible real-time testbed to evaluate the proposed diversity combining schemes over physical PLC and wireless channels. The testbed realizes essential parts of the physical layers on which both powerline and wireless communications operate.

The real-time testbed is built using products from National Instruments as shown in Fig. 1. Two chassis on the left and in the middle are for PLC and wireless communications, respectively. The two systems will be located in different places as they need different physical channels. Therefore, the two communication systems reside in different chassis. A PXI chassis has slots that can accommodate an x86 controller and various modules. As Fig. 1 depicts, a PXI-1045 chassis on the left has a PXI-8106 controller, a PXI-5421 signal generator and a PXI-5122 digitizer. This chassis functions as a baseband PLC system. Similarly, a PXIe-1082 chassis contains a PXIe-8133 controller, a PXIe-7965R FPGA module and an NI-5791 RF adapter module. Since the RF adapter module has both transmit and receive ports, a unidirectional single-input single-output link can be established with a single adapter.

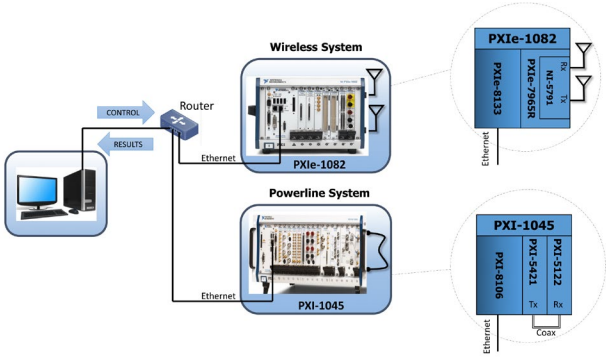

Figure 1. Hardware architecture.

The performance of the proposed combining techniques measured on the testbed is compared with computer simulation results by plotting BER curves for binary phase-shift keying (BPSK) modulation in Fig. 2 for both perfect and estimated channel scenarios.

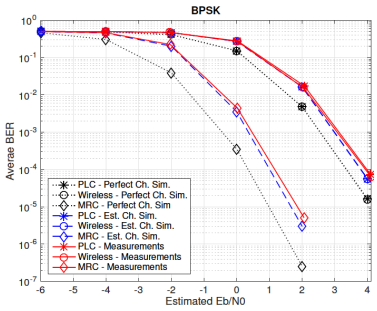

Figure 2. BER performance versus E_b/N_o.

Keywords: Smart Grids, power line and wireless communication, diversity, periodic impulsive noise.

INDUSTRY Interactions

Texas Instruments, NXP

MAJOR PAPERS

[1] Junmo Sung and Brian L. Evans, "Real-Time Testbed for Diversity in Powerline and Wireless Smart Grid Communications" in Proc. IEEE ICC, Work. Integrating Comm., Control, Comp. Tech. for Smart Grid, May 20-24, 2018, Kansas City, MO, USA.

TASK 1836.137, 50GS/S AND BEYOND FREQUENCY-INTERLEAVED ENERGY-EFFICIENT ADCS

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SIGNIFICANCE AND OBJECTIVES

This research explores a novel ADC architecture to realize a frequency-interleaved analog-to-digital conversion (FI-ADC), ultimately to push the performance limits of very high-speed ADCs. Performance of conventional high-speed ADCs is limited by jitter and we aim to determine if and how the FI-ADC can mitigate the jitter sensitivity of high-speed ADCs.

TECHNICAL APPROACH

One of the key focus areas of this work has been the development of a comprehensive model for comparing the FI-ADC to the time-interleaved ADC (TI-ADC). A comprehensive quantitative analysis was performed in addition to system-level simulations that compare the two architectures. The simulations support the theoretical findings and additionally provide further insight into the conditions under which the FI-ADC outperforms the TI-ADC.

SUMMARY OF RESULTS

This has been the final period of review for this project. In the first phase of the project, we designed a frequency interleaved ADC with an innovative distributed amplifier based signal splitter that provides filtering and high bandwidth (see Fig. 1). The prototype is shown in Fig. 2. The second phase of the proejct focused on analytical formulation and numerical simulation. A key results from this work is the detailed analysis of the impact of jitter and phase noise on the FI-ADC. Previous works have hinted at the reduced jitter sensitivity of the FI-ADC due to the reduced bandwidths presented to the sampling network, but have failed to provide an analysis of the impact of phase noise introduced during the downconversion which occurs in each passband channel. Quantitative analysis shows that the phase noise on the LOs used for downconversion plays a critical role in determining if the FI-ADC outperforms the TI-ADC. In general, the FI-ADC has the potential to improve performance for high input frequencies but may sacrifice performance at lower frequencies depending on the implemented architecture. Using our comprehensive model, we can predict maximum achievable SNR. Results have been published in Techcon 2016.

The final phase of the project focused on a redesign of key buildign blocks that limit performance. In particular, the LO chain of the chip must generate LO frequencies from a common low phase noise VCO using frequency dividers and mixers. The first divider is one of the key components as it must operate at high frequency, similar to the prescalar in a PLL. We analyzed the optimal CML divider design for low phase noise and high carrier frequency locking (40 GHz), designed a 28nm frequency divider chain for a new FI-ADC architecture and sent design for fabrication. We published a final report summarizing the project accomplishments to date.

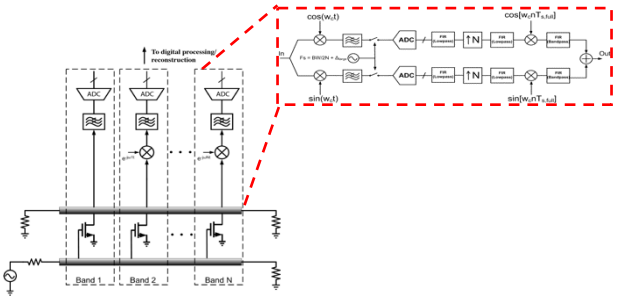

Figure 1. Architecture of FI-ADC.

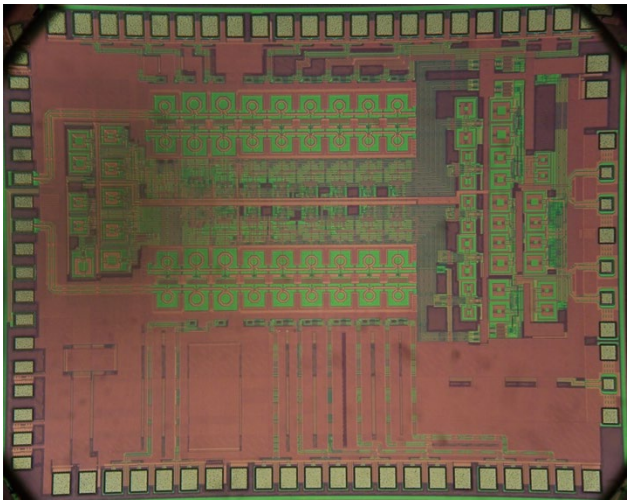

Figure 2. Die photo of prototype FI-ADC in 65nm CMOS.

Keywords: high-speed ADC, frequency-interleaved, channelized front-end, wideband receiver

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] N. Baniasadi and A. M. Niknejad, “Jitter Analysis in Frequency-Interleaved ADCs,” Techcon 2016

TASK 1836.139, ENABLING FULLY-INTEGRATED VHF CLK-SYNC MULTIPHASE SWITCHING REGULATORS ON SILICON

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SIGNIFICANCE AND OBJECTIVES

Voltage regulators in advanced SoC systems are expected to achieve transient speed and power density higher than conventional regulators. In this project, three major issues in the development of VHF (30-300 MHz range) multiphase switching regulators: high-speed feedback control, clock synchronization, and system miniaturization are investigated.

TECHNICAL APPROACH

A current-mode hysteretic control is being investigated. Compared to its voltage-mode counterparts, this current-mode approach is more robust to the noise at output, as the sensed control vector is inductor current.

From the perspective of system operation and circuit topology, an interleaved multiphase topology can effectively improve the system response. By taking advantage of the proposed current-mode hysteretic control, a simple clock synchronization technique is proposed which achieves cycle-by-cycle regulation in each sub-converter.

The regulator is being monolithically implemented, which allows reducing parasitics on power delivery paths, mitigating negative effects on noise, voltage drooping and stability.

SUMMARY OF RESULTS

The challenge in the modern design of switching power converters has been to develop a fully integrated switching converter, that which meets the additional demand for system miniaturization. In order to develop a fully integrated switching converter, it becomes necessary to operate in the VHF regime to reduce the inductive and capacitive components in the power stage and to eliminate other bulky off-chip components.

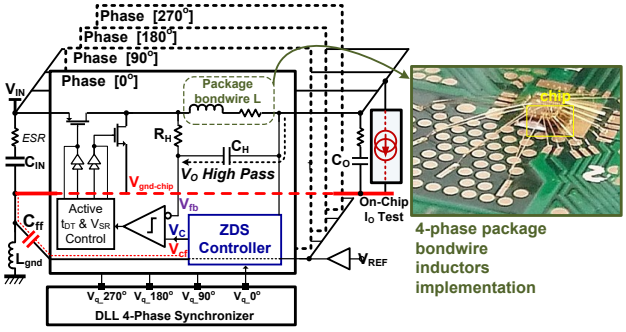

Figure 1. Block diagram of the four-phase buck converter with the photo of the package bondwire inductors.

In this project, a fully on-chip integrated multiphase converter is proposed, and the system block diagram is shown in Fig. 1. The four sub-converters are phase-synchronized by a built-in DLL-based synchronizer. As the proposed dual-loop control is independently conducted in each sub-converter, cycle-by-cycle current balancing is inherently implemented between phases. Moreover, the benefit of a multiphase operation is that it can achieve reduced passive components size and ns-level transient response. Thus, the required inductor size is significantly reduced to the range of the package bond wires, which allows the power inductor be implemented by using package bond wires as shown in Fig. 1. Accordingly, the system form factor, transient response, and power density are significantly improved.

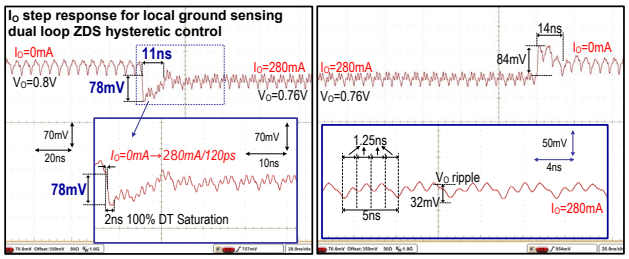

Figure 2. Measured load transient response to a load step from 0 to 280mA within 120ps with on-chip 1.97nF capacitor.

Fig. 2 shows the measured transient response and the output voltage ripple. The proposed converter employs a 1.8nF input capacitor, a 1.97nF output capacitor, and four 6.5nH bond-wire inductors without any other external components. In response to a 280mA/120ps load step-up, the voltage droop is 78mV (9.8% of output voltage) with 11ns response time. For load step-down, the converter exhibits 84mV overshoot within 14ns of 1% settling time. The output voltage ripple is maintained at 32 mV.

Keywords: fully integrated converters, VHF switching converters, multiphase operation, high-speed feedback control

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] M. K. Song et al., "A 200-MHz 4-phase fully integrated voltage regulator with local ground sensing dual loop ZDS hysteretic control using 6.5nH package bondwire inductors on 65nm bulk CMOS," (Invited) in 2016 ASP-DAC, pp. 1422-1425, Jan. 2016.

TASK 1836.140, EMBEDDED & ADAPTIVE VOLTAGE REGULATORS WITH PROACTIVE NOISE REDUCTION FOR DIGITAL LOADS UNDER WIDE DYNAMIC RANGE

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SIGNIFICANCE AND OBJECTIVES

The primary goal of the project is to develop an integrated power flow architecture for fine-grained spatio-temporal voltage distribution and management in microprocessors and SoCs. We investigate through models, simulations, hardware development and experimentation of novel control topologies and circuit techniques for efficient wide-dynamic range linear and switched capacitor voltage regulators (VRs).

TECHNICAL APPROACH

This project investigates power flow architecture in microprocessors and SoCs. There are two primary thrusts here: (1) development of novel control topologies for all digital linear regulators for Point of Load (PoL) regulation and (2) use of switched capacitor on-die regulators to provide power on demand for distributed IP blocks.

SUMMARY OF RESULTS

All digital LDOs are designed with synchronous digital control that enables sampling of the output voltage followed by comparison and thermometer based output power PMOS actuation. The strength of the design lies in its simplicity and process and voltage scalability. We have demonstrated 0.5V dropout at near threshold voltage (NTV) with less than 1μs droop recovery time. However, the biggest challenge with this design is the low small signal gain and existence of output ripple. We have developed models of the limit cycle ripples as well as ways to mitigate them. However, the all-digital designs are limited by the small signal gain and hence suffer from low PSR [1]-[4].

To meet the challenges of all-digital LDOs, a hybrid (digital and analog) low dropout regulator (LDO) utilizing switched mode control is designed in 130 nm CMOS for fine grain power management, fast droop recovery and robust small signal regulation of multi-VCC digital loads. The design provides an optimal trade-off of performance and accuracy by switching between a digital and an analog control loop. The hybrid topology achieves robust small signal regulation and fast recovery from large signal transients or power state transitions. Measurements from a 130nm test-chip show Near-Threshold Voltage (NTV) operation, fast transient response of 18 ns for a load step of 10.3mA and a peak current efficiency of 98.64%. However, the existence of the analog loop limits voltage and process scalability.

To address the challenges of voltage regulation and clocking, we propose Unified Voltage Frequency Regulator (UVFR) as an alternate to standalone LDO designs. Conventional systems are limited by the fact that voltage and frequency are generated by separate control loops. Motivated by the observation that the main objective of supply voltage regulation in digital systems is meeting timing, UVFR sets the supply voltage based on system timing properties and minimizes supply noise margins by temporarily modulating the clock frequency. Synthesized from all-digital cells, which generates and co-regulates a local clock and the local supply voltage simultaneously, UVFR powers a digital load circuit block embedded in a multi-domain SoC. Here a frequency-only reference is provided (FREF) from a shared PLL. The regulated supply (VREG) is locally generated at one point in the loop and a local VCO clock (can be divided by N) which is locked to the reference (FLOC=NFREF) is generated at another point of the same loop, providing a tightly coupled FLOC-VREG pair and the DVFS state is only defined uniquely by the performance (FREF which is equal to FLOC).

Keywords: integrated voltage regulator, discrete control, continuous time control, LDO, switched mode control

INDUSTRY INTERACTIONS

Intel, IBM

SELECTED PAPERS/PATENTS

[1] S. Gangopadhyay et al., CICC, 2017.
[2] Saad Nasir, et al. ISSCC, 2015.
[3] Saad Nasir et al., Transactions on Power Electronics.
[4] Saad B. Nasir, et al. ISCAS, 2016.
[5] Saad Nasir, et al. Applied Power Electronics Conference and Exposition (APEC), 2015.
[6] S. Gangopadhyay et al., JSSC, 2014.
[7] Saad B. Nasir, et al. ESSCIRC, 2016.
[8] S. Gangopadhyay et al., ESSCIRC, 2016.
[9] S. Gangopadhyay et al., DAC, 2015.

TASK 1836.143, DESIGN TECHNIQUES FOR MODULATION-AGILE AND ENERGY-EFFICIENT 60+GB/S RECEIVER FRONT-ENDS

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SIGNIFICANCE AND OBJECTIVES

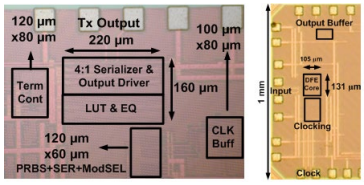
While high-performance I/O circuitry can leverage CMOS technology improvements, unfortunately the bandwidth of the electrical communication channels has not scaled in the same manner. The high-speed serial link receiver design and modeling techniques proposed here aim to significantly improve interconnect bandwidth density in an energy-efficient manner.

TECHNICAL APPROACH

In order to investigate design trade-offs, a statistical-modeling framework will be utilized to investigate power-optimum equalization partitioning and modulation format for 60+Gb/s signaling environments. This tool will be used to guide the design of a new modulation-agile receiver front-end which includes a multi-level decision-feedback equalizer (DFE) with multiple FIR/IIR feedback taps for efficient long-tail ISI cancellation. Adaptive techniques will also be developed to tune key equalization parameters, such as DFE tap time constants/weights and CTLE settings.

SUMMARY OF RESULTS

While dedicated PAM4 transceivers have been developed, the majority of serial I/O standards use simple binary NRZ modulation. In order to address this, a dual-mode NRZ/PAM4 SerDes which seamlessly supports both modulations with a 1-FIR- and 2-IIR-tap DFE receiver and a 4/2-tap FFE transmitter in NRZ/PAM4 modes were developed [1],[2]. A source-series-terminated (SST) transmitter employs lookup-table (LUT) control of a 31-segment output DAC to implement FFE equalization in NRZ and PAM4 modes with an 1.2Vpp output swing and utilizes low-overhead analog impedance control. Optimization of the quarter-rate transmitter serializer is achieved with a tri-state inverter-based mux with dynamic pre-driver gates. The quarter-rate DFE receiver achieves equalization with 1-FIR tap for the large first post-cursor ISI and 2-IIR taps for long-tail ISI cancellation. Fabricated in GP 65-nm CMOS (Fig. 1), the transceiver occupies 0.074 mm^2 and achieves power efficiencies of 10.9 and 5.5 mW/Gbps with 16Gb/s NRZ and 32Gb/s PAM4 data.



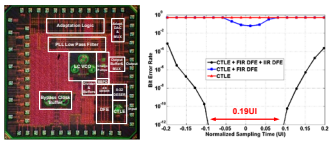
(a) (b)

TRANSCEIVER PERFORMANCE SUMMARY

References	This Work		[5]	[6]	[35]	[13]	[34]
Data Rate	32 Gb/s	16 Gb/s	20 Gb/s	56 Gb/s	56 Gb/s	28 Gb/s	16 Gb/s
Equalization	2-tap TX FFE + 1-tap FIR, 2-tap IIR RX DFE	4-tap TX FFE + 1-tap FIR, 2-tap IIR RX DFE	3-tap TX FFE	3-tap TX FFE + 1-tap RX DFE	3-tap TX FFE + RX CTLE + ADC based RX 24-tap FEE, 1-tap DFE	5-tap TX FFE + RX CTLE + 14-tap RX DFE	3-tap TX FFE + RX CTLE + 14-tap RX DFE
Modulation	PAM4	NRZ	PAM4	PAM4	PAM4	NRZ	NRZ
Total Loss @ Nyquist	13.5 dB	27.6 dB	5 dB	2 dB	25dB	40 dB for 25.78 Gb/s	34 dB
Eye Width BER	6% 10^{-12}	18% 10^{-12}	- 10^{-12}	- 10^{-12}	- 10^{-8}	23% 10^{-12}	- 10^{-15}
Supply (V)	1.2 TX, 1 RX		1.8	1.2	0.9 digital, 1.2 analog, 1.8 auxiliary	1 TX & RX, 1.25 TX driver	1/1.5 TX, 0.9 RX
Power (mW) (mW/Gbps)	176.3 5.5	173.7 10.9	408 20.4	475 8.5	550* 9.8	295* 10.5	235* 14.7
Area (mm^2)	0.074		0.43	2.74	1.4	0.62	2.15
Technology	65-nm		90-nm	65-nm TX, 40-nm RX	16-nm FinFET	28-nm	40-nm

(c)

Figure 1. 16/32Gb/s dual-mode NRZ/PAM4 SerDes in 65nm CMOS: (a) transmitter, (b) receiver, (c) performance summary.



(a) (b)

Figure 2. 56Gb/s PAM4 receiver: (a) 65nm CMOS die photo and (b) timing bathtub curves with a 20.8dB loss channel.

For higher data rate operation over higher-loss channels, a PAM4 quarter-rate receiver was developed that employs a single-stage CTLE and a DFE with 1 FIR and 1 IIR-taps to efficiently compensate for the channel loss [3]. In addition to the per-slice main 3 data samplers, an error sampler is utilized for background threshold control. An edge-based sampler performs both PLL-based CDR phase detection and generates information for background DFE tap adaptation. Fabricated in GP 65nm CMOS, the 56Gb/s receiver achieves 4.63mW/Gb/s and compensates for up to 20.8dB loss when operated with a 2-tap FFE transmitter.

Keywords: decision feedback equalizer, infinite impulse response (IIR) DFE, receiver, serial link

INDUSTRY INTERACTIONS

IBM, Texas Instruments

MAJOR PAPERS/PATENTS

[1] A. Roshan-Zamir et al., "A 16/32 Gb/s Dual-Mode NRZ/PAM4 SerDes in 65nm CMOS," IEEE CSICS, 2016.

[2] A. Roshan-Zamir et al., "A Low-Overhead Reconfigurable 16/32 Gb/s Dual-Mode NRZ/PAM4 SerDes in 65nm CMOS," IEEE JSSC, Sept. 2017.

[3] A. Roshan-Zamir et al., "A 56 Gb/s PAM4 Receiver with Low-Overhead Threshold and Edge-Based DFE FIR and IIR-Tap Adaptation in 65nm CMOS," IEEE CICC, 2018.

TASK 1836.146, ON-CHIP AC-DC POWER CONVERSION WITH GROUND DISTURBANCE SHIELDING FOR ENVIRONMENTAL SENSING APPLICATIONS

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SIGNIFICANCE AND OBJECTIVES

This project is exploring the optimal circuit architecture and operation scheme in achieving on-silicon AC-DC power conversion for environmental sensor applications. The power converter under development should be resilient to ground voltage disturbance, and have high power efficiency and a small physical form factor.

TECHNICAL APPROACH

Capacitive power transfer enables the implementation of fully integrated power converters. It is resilient to ground voltage surge and noise. A high-voltage on-chip capacitor provides a smaller form factor than a traditional discrete transformer. Thanks to a novel operation scheme, the topology can achieve power transfer efficiency over 50% when it is operating in a low power (<100mW) region.

SUMMARY OF RESULTS

Capacitive isolation replaces the bulky magetic components with on-chip barrier, enabling low-cost monolithic implementation. However, the low density on-chip capacitor and large parasitics limit the output power level and efficiency of the power transfer system.

In order to address the issues of capacitive isolation system, a resonant-based circuit architecture, which is shown in Fig. 1, for isolation power transmission is proposed. Differentiated from the traditional capacitive coupling power system, two inductors are placed on the power path, and form the resonant tank with isolation capacitor and the bottom-plate capacitors. The inductors not only can reduce the impedance due to the capacitors on the power path, but also limit the peak currents that charge and discharge the bottom-plate capacitors.

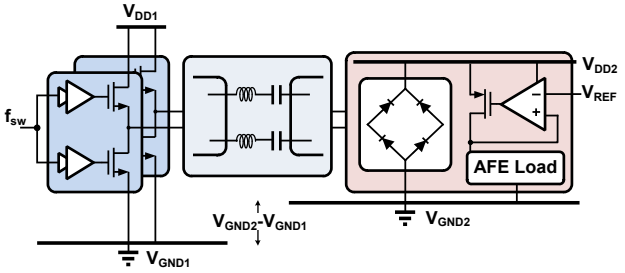

Figure 1. The resonant converter for isolation power transfer.

DC voltage VDD1 is converted by a H-bridge circuit into a square wave with a frequency of f_{sw}. When f_{sw} is equal to the resonant frequency, the fundamental component can pass through the resonant tank. The selected AC power is rectified at the output node as DC power supply for loading circuitries.

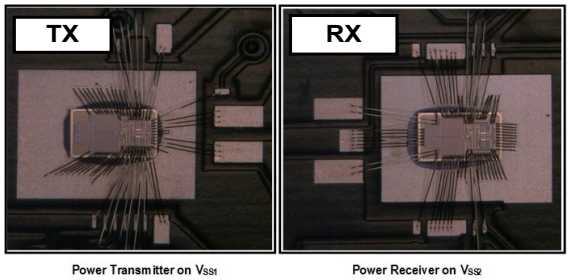

Figure 2. Photograph of fully-integrated capacitive isolation power transfer chips (transmitter and receiver).

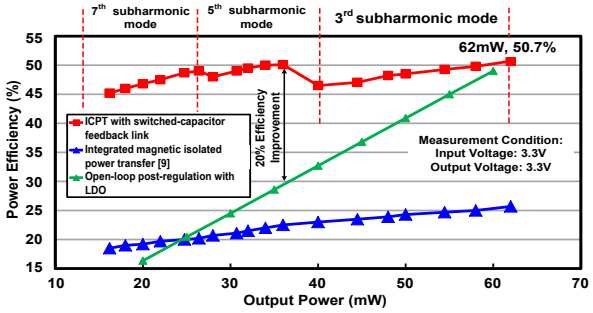

Figure 3. Measured ICPT efficiency over output power range.

The capacitive power transfer system is fabricated with HV BCD process. The chip and PCB implementation is shown in Fig. 2. To achieve isolation, two high-voltage capacitors are integrated on-chip for each phase. inducotrs is implemented with off-chip air-core inductor. Thanks to the resonant operation, the peak power efficiency is 50.7% and maximum output power is 62mW as shown in Fig. 3. This design achieves 4× efficiency improvement and 3× power delivery than prior art.

Keywords: power isolation, low-power sensor interface, capacitive power transfer, resonant power transfer

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] L. Chen et al., “A 50.7% Peak Efficiency Subharmonic Resonant Isolated Capacitive Power Transfer System with 62mW Output Power for Low-Power Industrial Sensor Interfaces” 2017 ISSCC, Feb., 2017, San Francisco, USA.

TASK 1836.153, HIGH-SPEED COMPACT POWER SUPPLIES FOR ULTRA-LOW-POWER WIRELESS SENSOR APPLICATIONS

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SIGNIFICANCE AND OBJECTIVES

Efficient and compact switched-capacitor (SC) voltage regulators are highly desirable for ultra-low-power sensor applications to improve energy efficiency and reduce system form factor. This project seeks to deliver a wide-input, fully-integrated SC voltage regulator with high efficiency and fast dynamic responses for sensor systems.

TECHNICAL APPROACH

A buck/boost unit SC cell is proposed to attain multiple conversion ratios (CRs), handle a wide input range and reduce system complexity. The symmetrical unit cell consists of one flying capacitors and five power switches, realizing 2:1 step-down conversion and 1:2 step-up conversion. By using three unit SC cells, the proposed SC voltage regulator can support 21 CRs and the input range from 0.5V to 5V. To improve efficiency, all power switches are implemented by thin-oxide NMOS transistors and the bootstrapped gate drivers have been designed to turn on/off power switches.

SUMMARY OF RESULTS

In the last year, the first test prototype was implemented by 65nm CMOS process to verify the CR reconfiguration and the interleaving scheme for variable input range and load conditions. The entire system implementation with multiple CRs and a low-power controller will be vadidated in the second prototype, which is designed with high-voltage BCD process to accommodate to high input voltage. An unit SC cell is proposed in this project to achieve both step-down and step-up conversion with one flying capacitor and five power switches. Shown in Fig. 1, three unit cells are implemented to attain 21 CRs. Meanwhile, interleaved 2-cell operation eliminates the need of two intermediate decoupling capacitors, reducing complexity. Power switches are designed identically with the back-to-back 1.8V NMOS transistors to avoid high-voltage breakdown and forward-biasing leakage. All NMOS implementation improves system efficiency due to the better device figure of merit. However, to efficiently turn on/off NMOS power switches, a bootstrapped gate driver is essential, which is illustrated in Fig. 2. Fixed-on pulse with a 20ns pulse width is generated to charge the bootstrapped capacitor, C_{BST}, when the nominal power switch, S_P, turns off. High-speed level shifter ensures the voltage domain transition of the clock signal.

The system architecture of the proposed SC voltage regulator is shown in Fig. 3. The power stage is constructed by using three unit cells. The flying capacitor is implemented by integrated MOS capacitors. The output regulation is achieved by single-bound hysteretic control for low quiescent power. This design is fabricated by 180nm BCD process and will be tested in future.

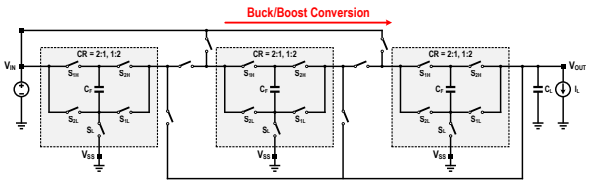

Figure 1. Circuit diagrams of proposed reconfigurable buck/boost swtiched-capacitor topology.

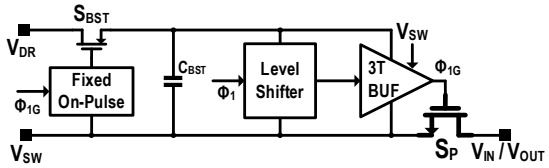

Figure 2. Bootstrapped gate driver for NMOS power switch.

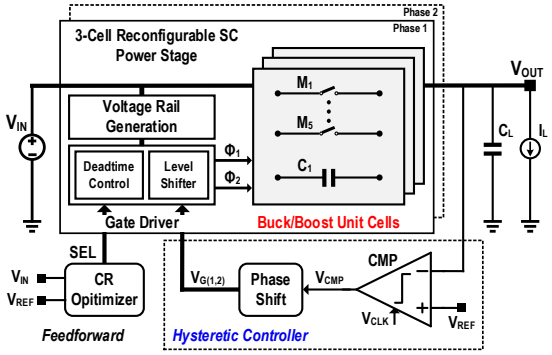

Figure 3. System architecture of the second proposed switched-capacitor voltage regulator.

Keywords: wireless sensor, wide input, switched-capacitor, reconfiguration, bootstrapped gate driver

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

[1] Kang Wei and D. Brian Ma, "A 0.2V-to-5V Fully-Integrated Reconfigurable Buck/Boost Switched-Capacitor Voltage Regulator for Self-Powered Wireless Sensors," *2017 32nd Conference on Design of Circuits and Integrated Systems (DCIS)*, Barcelona, 2017, pp. 1-6.

TASK 2712.002, ON-LINE SELF-TESTING AND SELF-TUNING OF INTEGRATED VOLTAGE REGULATORS

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SIGNIFICANCE AND OBJECTIVES

The proposed research will develop low-complexity algorithms and low-overhead all-digital self-testing and self-tuning architecture for high-frequency integrated voltage regulators (IVRs). The work will focus on digitally controlled fully integrated inductive VR (FIVR), digital low-dropout regulators (DLDO), and power delivery system with FIVR and multiple distributed DLDOs.

TECHNICAL APPROACH

The challenge for testing/tuning of IVRs is the presence of high frequency closed-loop control. The proposed approach is based on the principle that in a system with IVR and digital core(s), the testing/tuning should focus on system's performance rather than the IVR in isolation. We propose to characterize the output voltage variation that ultimately determines the performance of the digital load. We consider large signal perturbations (load and reference steps) to excite the transient noise in the IVR's output, and tune the IVR's loop to minimize the noise. Finally, we explore co-tuning of IVR and processor.

SUMMARY OF RESULTS

Self-tuning of Digital Low-dropout Regulator: We have demonstrated all-digital tuning and dynamic control of feedback compensator in digital low drop out regulators (DLDO) to enhance transient performance under process and passive variations, aging, and load changes. The measured results from a 130nm CMOS test-chip shows 2.1× improvement in transient performance under process variations and 30% improvement for aging-induced degradations. We demonstrate 55ns setting time for a 5mA to 45mA load step in 100ps, with 97.8% peak current efficiency.

Performance-based Tuning of Inductive IVR: We have presented an auto-tuning method for fully integrated voltage regulators (IVRs) driving digital cores against variations in passive as well as process/temperature of the core. The key contribution is to perform auto-tuning of the coefficients of the feedback loop of the IVR based on the performance of the digital cores. The proposed performance driven auto-tuning demonstrates potential for up to 12% increase in system performance under inductance and threshold variation. A test-chip has been designed in 130nm CMOS to demonstrate the performance-based tuning. The test-chip is currently being measured.

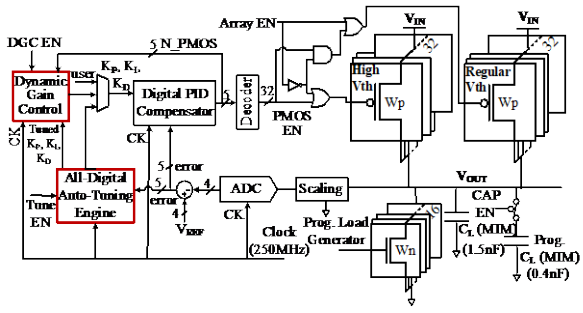

Figure 1. Architecture and test-chip of self-tuning Digital Low-dropout Regulator.

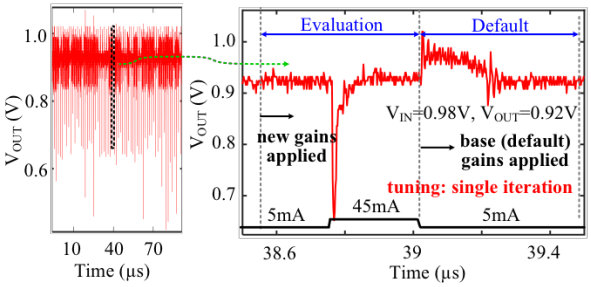

Figure 2. Measurement results showing DLDO tuning.

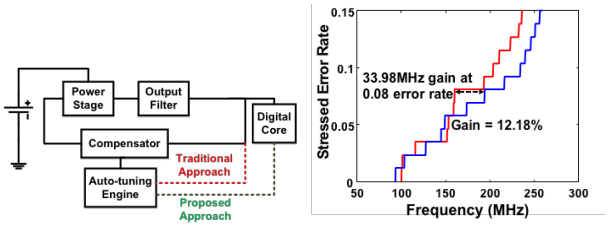

Figure 3. Concept and simulation of performance-based tuning of inductive IVR.

Keywords: integrated voltage regulator, self-testing, and self-tuning.

INDUSTRY INTERACTIONS

Intel, NXP

MAJOR PAPERS/PATENTS

[1] V. Chekuri, M. Kar, A. Singh, and S. Mukhopadhyay, "Performance Based Tuning of an Inductive Integrated Voltage Regulator Driving a Digital Core against Process and Passive Variations," Design, Automation, and Test in Europe (DATE), 2018.

[2] A. Singh, M. Kar, V. Chekuri, and S. Mukhopadhyay, "A Digital Low-Dropout Regulator with Auto-Tuned PID Compensator and Dynamic Gain Control for Improved Transient Performance Under Process Variations and Aging", SRC TECHCON'18.

TASK 2712.006, ROBUST, EFFICIENT ALL-DIGITAL SIMO CONVERTERS FOR FUTURE SOC DOMAINS

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SIGNIFICANCE AND OBJECTIVES

The scalability of buck-converter based Integrated Voltage Regulated (IVR) systems is a key challenge in SoC design. Single-Inductor Multiple Output (SIMO) converters are scalable, but face several challenges. This effort investigates an all-digital SIMO architecture for digital SoCs, employing a Unified Clock and Power (UnCaP) architecture for robust regulation.

TECHNICAL APPROACH

SIMO converters exhibit poor transient response due to the reliance on a time-shared inductor. In such situations, ensuring robust regulation by relying on elastic clock generation, that matches the system critical path and "stretches" the clock during a droop or large ripple event, provides timing relief and robust regulation without excessive decoupling capacitance. However, phase lock to a reference must be maintained. We have thus far proceeded on two fronts (1) The translation of our proposed Unified Clock and Power (UniCaP) architecture into a test-chip demonstration and (2) Exploration into all-digital computational control for rapid, scalable regulation of a load.

SUMMARY OF RESULTS

We recently demonstrated an architecture for unified clock and power using an integrated buck converter with an ARM microprocessor to demonstrate the effectiveness of the approach in terms of voltage margin reduction [1]. This is the first-ever architectural solution for unifying power and clock sub-systems applicable to buck, switched-capacitor [2] and LDO topologies that drastically reduces margins due to imperfect regulator performance. We have also built upon our recent efforts in computational control to develop a simplified version of model-predictive control for LDOs which serves as a test-bed for eventual SIMO control. We hope to successfully prove out computational control and then transition toward detailed simulations of the proposed SIMO architecture by March 2018.

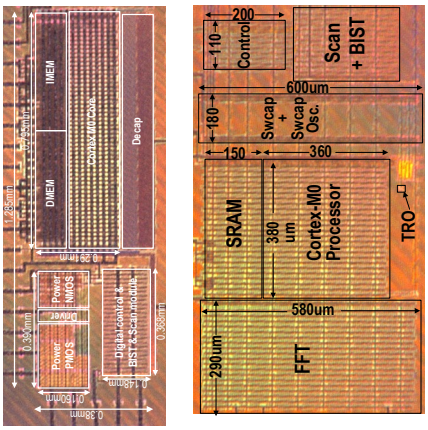

Figure 1. Demonstration of UniCaP test chips using an integrated buck converter and switched capacitor converters in 65nm CMOS. Both designs employed a Cortex M0 microprocessor to demonstrate the effectiveness of the approach.

Specifically, the buck test chip, which serves as an important milestone for the eventual SIMO architecture demonstrated a voltage margin recovery of 84% due it its ability to not only regulate performance in the presence of severe droop (or voltage ripple anticipated in the SIMO system) but also to recover any cycles lost due to clock stretching in the process.

Keywords: SIMO, unified clock and power, voltage regulation, clock stretching

INDUSTRY INTERACTIONS

Intel, ARM

MAJOR PAPERS/PATENTS

[1] X. Sun et al. "A Combined All-Digital PLL-Buck Slack Regulation System with Autonomous CCM/DCM Transition Control and 82% Average Voltage Margin Reduction in a 0.6-1.0V Cortex-M0 Processor", ISSCC 2018

[2] F. Rahman et al. " An All-Digital Unified Clock Frequency and Switched-Capacitor Voltage Regulator for Variation Tolerance in a Sub-Threshold ARM Cortex M0 Processor " to appear in Symposium on VLSI circuits 2018

TASK 2712.008, DIRECT-BATTERY-TO-SILICON POWER TRANSFER IN ADVANCED NANOMETER CMOS

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SIGNIFICANCE AND OBJECTIVES

The aim of the task is to facilitate direct-battery-to-silicon high-tension-power delivery in advanced CMOS processes to bring down delivery losses and area footprint. The key objective is to develop circuit techniques to handle breakdown voltages and implement fine-grain feedforward control for SOCs while making these solutions portable across technology and types of SOCs.

TECHNICAL APPROACH

Deep-submicron technologies have ~1V as the core MOS rated voltages and at max, 2.5V for thick-oxide I/O MOS devices. In order to handle 4+V battery voltage careful stacking/design of devices is required. During the course of the project, we will work on both capacitive and inductive converters. In this part of project, we focused on low voltage LDOs to regulate switching converter's output and a new multimode hybrid DC-DC converter to do direct battery to silicon voltage conversion.

SUMMARY OF RESULTS

Low voltage LDO: In order to remove ripples from the switching converters, we designed a fully integrated analog LDO for sub-0.5V supply voltages. To realize the gate drive, we introduce a negative charge pump based adaptive offset between the pass FET and error amplifier (Fig. 1) which provides a gate-source headroom at input operation voltages normally reserved for digital LDOs. As shown in Fig.2 (left), the LDO can operate from 0.3V-to-1.0V input voltage, and can sustain a load variation of 10mA to 100mA at 1.0V and 5mA to 25mA at 0.3V input. It achieves a peak 99.1% current efficiency.

High voltage DC-DC converter: We implemented a direct battery to silicon multimode hybrid switching regualtor system in 65nm CMOS. The lithium ion battery discharges from 4.2V to 2.8V. Also, in a SOC system, the voltage requirements could vary from 1.5V (for RF PA's) to 0.5V (for sleep mode digital). So, we would need a programmable conversion ratio (K) to support this combination of input and output voltage ranges as illustrated in Fig. 3 (left). The proposed DC-DC converter has three modes of operations, namely - 4 level buck (for K=5-13), resonant (K=1 & 2) and soft switching (for K=3 & 4). The system achieves peak efficiency 91%.

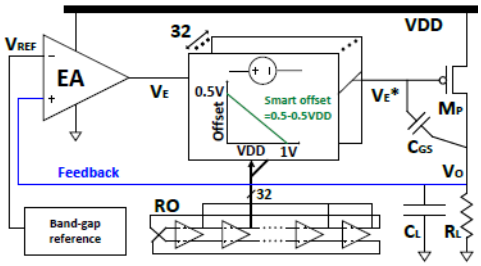

Figure 1. Proposed LDO with charge pump based smart offset.

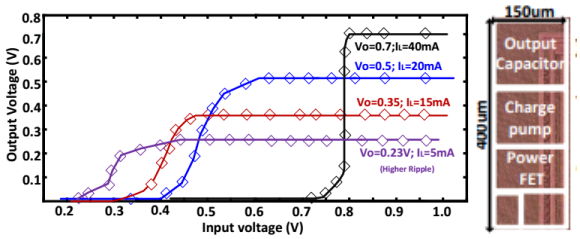

Figure 2. (Left) Output voltage Vs input voltage of Low voltage analog LDO, (Right) Chip micrograph of in 65nm CMOS.

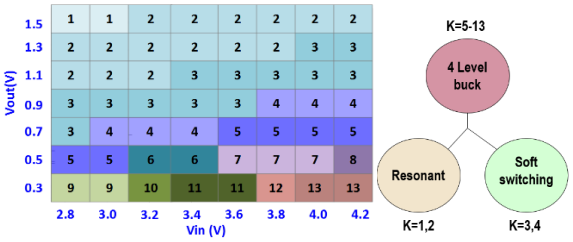

Figure 3. (Left) Different conversion ratios for output Vs input voltages (Right) Three modes of hybrid DC-DC.

Keywords: analog LDO, smart offset, multimode DC-DC

INDUSTRY INTERACTIONS

Texas Instruments, Intel, IBM

MAJOR PAPERS/PATENTS

[1] Chaubey, S. & Harjani, R., "Fully Tunable Software Defined DC-DC Converter with 3000X Output Current & 4X Output Voltage Range 2010", IEEE CICC 2017, Austin

[2] Chaubey, S & Harjani, R., " A Smart-Offset Analog LDO with 0.3V Minimum Input Voltage and 99.1% Current Efficiency", IEEE A-SSCC, Seoul, South Korea, Nov 2017

[3] Harjani, et al., "Ultra High Density Integrated Composite Capacitor", US patent # 9,812,457, Issued Nov 7, 2017 **[Patent]**

TASK 2712.009, LOW POWER AREA EFFICIENT FLEXIBLE-RATE ENERGY PROPORTIONAL SERIAL LINK TRANSCEIVERS

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SIGNIFICANCE AND OBJECTIVES

We present a sub-baud-rate clock and data recovery technique that eliminates one clock edge for every data bit requirement present in all conventional CDRs. Using a combination of data samplers and current integrators, the prototype CDR recovers 15.2Gb/s data while using a single 3.8GHz clock generated by an LC oscillator.

TECHNICAL APPROACH

Figure 1 shows a simplified block diagram of the sub-baud-rate CDR [1]. Two data samplers (S1 and S2) sample VGA output, d(t), on positive and negative edges of the quarter-rate clock (CK) and recover odd numbered bits (d[4k+1], d[4k+3]). Two time-interleaved current integrators integrate d(t) between the positive and negative edges of CK in a ping-pong manner. Three samplers slice each integrator's output at 3 different threshold voltages and receover even bit (d[4k+2]/d[4k+4]). Hence, 4 data bits are recovered in each CK cycle. A digital loop filter (DLF) drives the digitally-controlled oscillator toward phase lock.

SUMMARY OF RESULTS

The prototype CDR was fabricated in a 65nm CMOS process and characterized using chip-on-board assembly. The bit error rate (BER) performance of the CDR was characterized with different 15.2Gb/s PRBS sequences provided by an external BER Tester. The channel used for characterizing the CDR contains an 1-m coaxial SMA cable and an 1-inch on-board PCB trace. The CDR achieves error-free operation (BER < 10^{-12}) while recovering PRBS31 data.

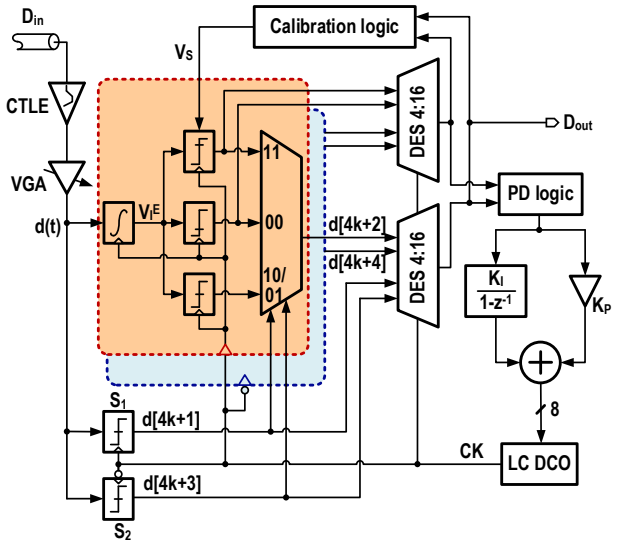

Figure 1. Simplified block diagram of sub-baud-rate CDR.

The measured bathtub indicate that worst case timing margin is larger than 0.35UI for a BER < 10^{-11}. The measured JTOL curve shows that a large JTOL corner frequency of about 20MHz is achieved with BER < 10^{-11}. The phase noise plot of the recovered 3.8GHz clock shows that integrated jitter (10kHz – 100Mz) when operating with PRBS7 data is 537fs_{rms} and it increases to 955fs_{rms} with PRBS31 data. The total power consumption of the CDR is 29.3mW (1.9pJ/bit) of which the analog front-end (CTLE + VGA + samplers + integrators) consumes 13.3mW and the LC oscillator, clock distribution, CDR logic and de-serializer together consume 16.0mW.

Keywords: CDR, baud-rate, PLL.

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] D. Kim et al., "A 15Gb/s 1.9pJ/bit sub-baud-rate digital CDR", IEEE Custom Integrated Circuits Conference, 2018.

TASK 2712.012, EDAC AND DCDC-CONVERTER CO-DESIGN FOR ADDRESSING ROBUSTNESS CHALLENGES IN EMERGING ARCHITECTURE

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SIGNIFICANCE AND OBJECTIVES

The goal of this project is to investigate techniques on EDAC (Error Detection and Correction) and DCDC converter co-design for the post-Moore's law era where aggressive architectures and circuits will be explored to continue performance and energy-efficiency scaling while ensuring robustness and reliability.

TECHNICAL APPROACH

We will devise the following techniques: (i) direct error regulation to make DVS energy-efficient and fully-digital while miniaturizing capacitor sizes in the integrated switched-capacitor converter; (ii) EDAC+Converter for non von-Neumann and parallel architecture, such as error correction scheme for super-Vt circuits performing no instruction replay, and techniques for in and around embedded memory; (iii) EDAC+DVS for clock domain crossing with focus to simplify clock distribution and generation.

SUMMARY OF RESULTS

During May/2017-Apr/2018, we have worked on mainly two projects. In the first project, we demonstrated a sub-µW neural spike processor (NSP) integrated with a power management unit (PMU) for on-implant processing in motor intention decoding. The NSP-PMU system demonstrates: (i) among the highest level of functional integration including spike detection, feature extraction, sorting, the first half of decoding, which reduces wireless data rate by more than 4 orders of magnitude; (ii) on-chip nanowatt PMU integration enabling resilient and energy-efficient operation; (iii) the lowest power dissipation of 0.78 µW for 96 channels, 21× lower than the prior art at a comparable/better spike-signal decoding accuracy. Figure 1 shows the chip photo, that is prototyped in a 0.18 µm CMOS. This work is accepted for the publication in 2018 IEEE ESSCIRC [1]

In the second project, we have worked on a new methodology in co-designing an integrated switched-capacitor converter and a digital load. Conventionally, a load has been specified to the minimum supply voltage and the maximum power dissipation, each found at the own worst-case process, workload, and environment condition. Furthermore, in designing an SC converter toward this worst-case load specification, designers often have added another separate pessimistic assumption on power-switch resistance and flying-capacitor density of an SC converter. Such worst-case design methodology can lead to a significantly over-sized flying capacitor and thereby limit on-chip integration of a converter.

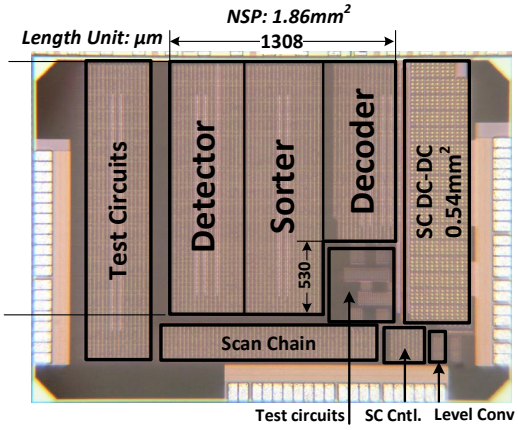

Figure 1. The lowest-power NSP-PMU SoC.

Our proposed methodology instead adopts the better than worst-case (BTWC) perspective to avoid over-design and thus optimizes the area of an SC converter. Specifically, we propose BTWC load modeling where we specify non-pessimistic sets of supply voltage requirement and load power dissipation across variations. In addition, by considering coupled variations between the SC converter and the load integrated in the same die, our methodology can further reduce the pessimism in power-switch resistance and capacitor density. The proposed co-design methodology is verified with a 2:1 SC converter and a digital load in 65 nm CMOS, achieving more than one order of magnitude reduction in flying capacitor area, over the conventional worst-case approach. We also verified our methodology with a wide range of load characteristics in terms of their supply voltages and current draw and confirmed the similar benefits. This work is accepted in 2018 ACM/IEEE ISLPED [2].

Keywords: near/sub-Vt digital circuits, power converter, direct error regulation

INDUSTRY INTERACTIONS

Intel, Texas Instruments

MAJOR PAPERS/PATENTS

[1] J. Li, et al., "A 0.78-µW 96-Ch. Deep Sub-Vt Neural Spike Processor Integrated with a Nanowatt Power Management Unit," IEEE ESSCIRC, 2018

[2] D. Kim, et al., "Better-Than-Worst-Case Design Methodology for a Compact Integrated Switched-Capacitor DC-DC Converter," ACM/IEEE ISLPED, 2018

TASK 2712.016, 3D IC THERMAL MANAGEMENT BASED ON TSV PLACEMENT OPTIMIZATION AND NOVEL MATERIALS

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NADER BAGHERZADEH, UNIVERSITY OF CALIFORNIA, IRVINE

SIGNIFICANCE AND OBJECTIVES

3D ICs can offer advantages in power and performance management, but the stacked geometry makes heat dissipation substantially more challenging. The project objective is to enable efficient thermal management by including thermal TSVs early in the system design process, fully addressing the electrical workload, and exploring various TSV design parameters.

TECHNICAL APPROACH

Based on a cross-disciplinary approach, we have built floorplans of 2D and 3D Nehalem like x86 processors and developed a detailed thermal model incorporating the effects of TSVs, interfaces, TSVs, BEOL, and Die-to-Die layers. We first use the gem5 simulator to adopt benchmarks and generate system component activities. We then use McPAT to estimate the power consumption of all the system components and generate the power traces that are fed into HotSpot for temperature simulations. Using these simulations, the impact of TSVs on thermal management is evaluated and power consumptions of 3D ICs is optimized utilizing machine learning heuristics.

SUMMARY OF RESULTS

We have adopted x86 Instruction Set Architecture (ISA) out of order Nehalem like processor. The 2D Nehalem is composed of 8 cores with private L1 and L2 caches. The threads share data by using a shared L3 cache. In the 3D case, the stack is composed of two core layers, and each layer contains four cores. The next layer contains eight L2 caches for each core and connects to the core layers by signal TSVs, which are used for signal processing. The last layer has the L3 cache and connects to L2 by signal TSVs.

The thermal model of 3D Nehalem includes a heat sink, a heat spreader, silicon chips, metal layers, Die-to-Die layers, interface resistances, and the effects of TSVs. The TSVs are modeled within the silicon chip layers and assumed to use micro-bump (µbump) connections.

We have adopted a full system level simulation using the gem5 that uses specifications including cores, caches, memory, controllers and interconnect component. We simulate Splash-2 benchmarks, which are cross-compiled for the appropriate ISA such as x86. The components activities output along with the system configuration are fed into McPAT, which is an integrated power, area and timing modeling framework for multithreaded and many core architectures. All system activities generated by gem5 are fed into to the McPAT as input parameters to generate the power traces. HotSpot then receives the power estimation of all components generated by McPAT, along with a floorplan that is compatible with specifications made in gem5 to generate temperature distributions of 2D and 3D Nehalem floorplans.

While the 3D design provides a short distance for signal processing and reduces the wire latency, the heat generation and temperature rise issues limit the performance in 3D Nehalem. As shown in Figure 1, the peak temperature of 3D Nehalem is much higher than that of 2D Nehalem and there are five benchmarks that exceed the threshold temperature, which is the maximum temperature to ensure reliable operations.

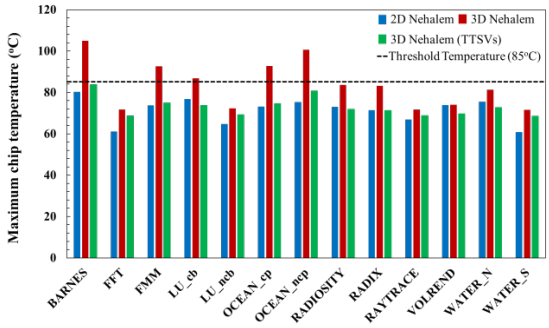

Figure 1. Maximum chip temperature data of various benchmarks for 2D Nehalem, 3D Nehalem and 3D Nehalem with Thermal TSVs (TTSVs), indicating the impact of TTSVs.

By placing Thermal TSVs (TTSVs), which are not used for signal processing, close to hot spot regions that are identified in temperature simulations, the maximum chip temperature has been significantly reduced. The use of TTSVs can effectively reduce the hot spot temperature of 3D Nehalem below the threshold temperature and even close to those of 2D Nehalem case. The total area of TTSVs used in these simulations is 10 mm^2, which corresponds to a 6% area overhead and the resulting peak temperature reduction ranges from 5% to 25% for the Splash-2 benchmarks investigated in this project.

Keywords: 3D ICs, thermal TSV, thermal management

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

TASK 2712.018, TEST TECHNIQUES TO APPROACH SEVERAL DEFECT-PER-BILLION FOR POWER IC'S

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SIGNIFICANCE AND OBJECTIVES

Existing power IC test techniques examine and model chip performance through external terminals. This work will simulate, design and test power IC subcircuits using additional bare-die test points to reduce part failure rates. The goal is test yield enhancement by culling power ICs with outlier subcircuit performance.

TECHNICAL APPROACH

Task researchers will demonstrate the use of internal IC test points to determine subcircuit performance inside of generic LDOs and Buck Converters. The test points are placed either in the wafer scribe lanes or at internal IC test pads. Bare-die power IC probing will allow the measurement of DC, small-signal response and precise control of low and high temperature wafer measurements. Analyses, simulations and measurements of custom-designed LDO and Buck Converters will be performed in order to prove these new test concepts. A 65nm CMOS LDO test IC has been sent for fabrication.

SUMMARY OF RESULTS

Existing test and modeling methodologies for LDO ICs characterize three external nodes (V_{in}, V_{load} and GND). In this work, the researchers have developed generic LDO designs with PFET (p-type FET) or NFET (n-type FET) pass transistors. Researchers performed simulations of these generic LDO designs with internal probe points. This work demonstrated ways of injecting signals and overcoming the high control loop gain in the LDO in order to do individual subcircuit characterization. Investigations showed that operating a PFET LDO at V_{Input} voltages near but below LDO dropout the gain of the feedback loop is significantly weakened and this can place the PFET pass transistor into triode mode while keeping the Error Amplifier working. The simulated probe points could be used to find, 1) differential circuit imbalances in the LDO error amplifier, 2) PFET and NFET pass transistor weaknesses, 3) integrated resistor and capacitor values at the edge of process tolerances, 4) charge-pump circuit's output voltage and 5) Bandgap Reference voltage.

The researchers have designed a generic LDO for characterization and fault modeling in a 65 nm CMOS process. In the IC, there is an error amplifier (which compares the reference voltage and scaled down output voltage), a Bandgap reference (BGR), pass transistor (output driver), feedback resistances and compensation capacitances as shown in Figure 1. In the 65nm CMOS LDO, a buffer and a transmission gate are added at the output of the Error Amplifier and Bandgap Reference in order to read, more accurately, those voltages out of the chip during testing. The functionality of the LDO system as a whole and its individual subcircuits were simulated. There was a dropout voltage of 140mV at load current of 200mA with a 1.6V output voltage. Simulations of dropout characteristics and the multi-fingered PMOS pass transistor performance at high temperatures show the greatest variations. Simulations in 65nm CMOS were performed using a multi-fingered PFET LDO modeled in dropout. Reduced numbers of fingers modeled a weak PFET with inactive or partially active fingers or high V_{th} fingers.

Providing tests for LDO subcircuit response opens several ways to improve yield. There is potential to cull LDOs prone to failure by finding outlier performance inside the subcircuits. In addition, a statistical database for LDO subcircuit response could be measured to form a basis to determine weak subcircuits and acceptable subcircuits. Pre-determined weak LDO subcircuits could be tested after accelerated aging and harsh usage conditions to demonstrate the critical failure and yield issues.

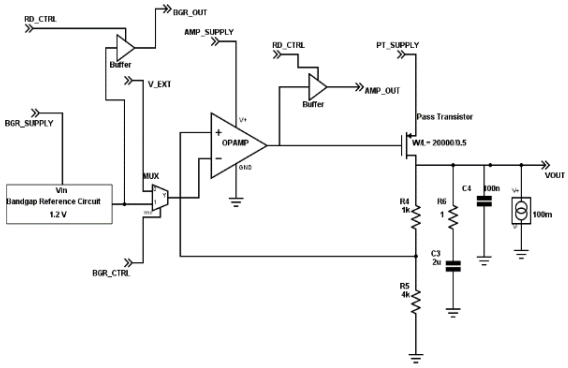

Figure 1. Block diagram of the 65nm CMOS LDO Design.

Keywords: test, analog, power, LDO, buck converter

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] A. Tulsiram et al., "Development of LDO Testing and Fault Detection for Ultra Low Defects," 2018 NATW'18, May 2018, Essex, VT.

TASK 2712.019, PRE-COMPUTED SECURITY PROTOCOLS FOR ENERGY HARVESTED IOT

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SIGNIFICANCE AND OBJECTIVES

We optimize the latency and energy-efficiency of Internet security protocols in energy-harvesting IoT. An energy-harvesting IoT device has limited and leaky energy-storage capacity. The energy must be used as soon as possible. With pre-computing techniques, cryptographic applications can instantly use the harvested energy. We demonstrate precomputed random-number generation and cryptographic key-exchange.

TECHNICAL APPROACH

The feasibility and efficiency of the proposed techniques will be evaluated through an end-to-end demonstrator with an energy-efficient micro-controller and with a wireless communications front-end. We develop techniques to spread out computations over time by reformulating cryptographic algorithms as capable of generating coupons, which are precomputed portions of the algorithm. We propose techniques for coupon generation and their secure storage in non-volatile, possibly off-chip memories. We also consider and optimize the impact of precomputed security protocols on the communication cost and the storage cost. We validate the proposed approach by constructing a prototype implementation on an energy-harvesting oriented microcontroller-based platform.

SUMMARY OF RESULTS

We studied two canonical cryptographic applications: true random number generation and bulk-encryption. Our solutions avoid energy waste during the offline phase, and they offer gains in energy efficiency during the online phase of up to 28 times for bulk-encryption and over 100 times for random number generation [1]. The transformation of energy to coupons for future use allows us to exploit the improved data storage capacity of modern energy harvesting systems and improve the runtime performance of our cryptographic operations. Figure 1 highlights the potential to improve the performance of an energy harvested device in completed operations per second.

We analyze the precomputed implementations on an MSP430 with ferroelectric RAM and an ARM Cortex M4 with nonvolatile flash memory. For bulk encryption, we studied the application of AES in counter mode (AES-CTR). In AES-CTR mode, the actual block cipher operation is independent of the input message, making it a good candidate for parallelizing the encryption/decryption process.

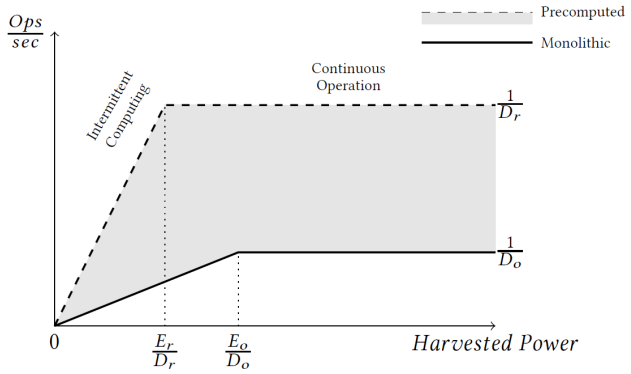

Figure 1. Operations per second as a function of Energy influx into the system. When coupons are available the device is able to execute more operations within a given time period.

Table 1. Improvements in AES-CTR with precomputation

Device	Test case	$\frac{C_o}{C_r}$	$\frac{E_o}{E_r}$	$\frac{D_o}{D_r}$	$\frac{EDP_o}{EDP_r}$
MSP432	SW T-box	5.4	5.4	5.5	29.8
	SW S-box	27.5	27.8	28.4	791.3
	HW	3.2	3.2	3.3	10.5
MSP430	SW S-box	22.3	28.1	26.3	737.7
	HW	1.9	2.1	2.0	4.0

Table 1 compares the operation of AES-CTR in monolithic mode (Figure 1, dashed line) and in precomputed mode (Figure 1, solid line). We use different implementations of AES-CTR, both with and without hardware acceleration. In all cases, there is a large improvement in runtime latency, energy requirement and security in AES-CTR mode when OTPs are precomputed.

Our current research efforts focus on secure storage of tokens in non-voltaile memory.

Keywords: pre-computation, cryptography, energy-harvesting, MSP430, NVM applications

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] C. Suslowicz, A. S. Krishnan, P. Schaumont, "Optimizing Cryptography in Energy Harvesting Applications," ASHES@CCS 2017: 17-26.

TASK 2712.024, A SYSTEM-IN-PACKAGE PLATFORM FOR ENERGY HARVESTING AND DELIVERY FOR IOT EDGE DEVICES

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MADHAVAN SWAMINATHAN, GEORGIA INSTITUTE OF TECHNOLOGY

SIGNIFICANCE AND OBJECTIVES

The proposed research aims to design a System-In-Package (SIP) based energy delivery system for powering wireless sensor nodes and IoT edge devices. We propose to develop a multi-chip SIP, with multiple energy transducers, on-package passives (magnetic core inductor and high-density capacitor), a power management unit (PMU) with a boost/buck voltage regulator (VR), and the load device.

TECHNICAL APPROACH

We will develop the architecture of the proposed system-in-package based energy harvesting and delivery system. We will design and fabricate an on-package inductor for the proposed energy delivery system. We will design, fabricate and test the power management unit of the proposed SiP. The power management unit will consist of a boost/buck regulator to harvest from multiple sources and powering multiple output domains. Finally, we will design, fabricate, and characterize the multi-chip SiP to demonstrate the proposed energy-harvesting system. The SiP will integrate the PMU and passives designed in this program with the off-the shelf energy harvester and an in-house designed load device.

SUMMARY OF RESULTS

A System-in-Package (SiP) with an Integrated Voltage Regulator (IVR) and on-package passives provides a compact energy harvesting system. We have demonstrated that in a SiP based energy harvesting system, co-design of the regulator circuit and the passives depending on the input characteristics of the transducers, the material properties of the passives, and voltage/power demands of the output loads can maximize the efficiency for various applications, and extend lifetime of battery-powered and autonomous IoT devices. We have developed a system design tool that uses a loss model for pulse-frequency modulation (PFM) boost regulators, design of different embedded inductors, and performs co-analysis to estimate optimal efficiency. The simulation result shows potential of 6% improvement in efficiency by co-designing IVR and inductor, compared to optimizing IVR only for a given inductor.

We have extended system level design to integrate the characteristics of the harvesting source. thermoelectric generators and photovoltaic harvesters are chosen for analysis purposes. The results are demonstrated to support the concept of System-Focused Maximum Power Point Tracking (SF-MPPT), where the converter is bundled with a transducer and treated as a whole to determine the point of maximum available system output power transfer. A time-based output power estimation method for SF-MPPT with a low overhead is proposed and simulated to demonstrate the effectiveness of implementing SF-MPPT.

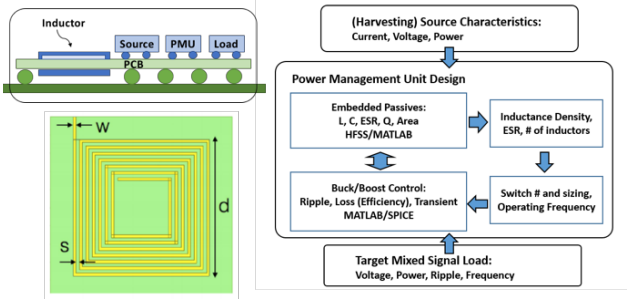

Figure 1. The system architecture, fabricated embedded inductor, and the co-design flow.

Inducor Design[2]	3	5	7
Inductance	114 nH	364 nH	452 nH
DC Resistance	0.171 Ω	0.339 Ω	0.506 Ω
Operating Freq.	5.7 MHz	1.6 MHz	1.4 MHz
Conduction Loss	236 μW	270 μW	306 μW
Switching Loss	414 µW	129 µW	103 µW
Peak Eff.(2mA)	81%	87%	86%

Figure 2. Simulation results of our co-design flow.

Keywords: integrated voltage regulator, self-testing and self-tuning

INDUSTRY INTERACTIONS

Intel

MAJOR PAPERS/PATENTS

[1] E. Lee, et. al, "A System-In-Package based Energy Harvesting for IoT Devices with Integrated Voltage Regulators and Embedded Inductors," Electronic Component and Technology Conference (ECTC), 2018. Design, Automation, and Test in Europe (DATE), 2018.

TASK 2712.027, GATE DRIVING TECHNIQUES AND CIRCUITS FOR AUTOMOTIVE-USE GAN POWER CIRCUITS

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SIGNIFICANCE AND OBJECTIVES

This project explores the gate driving technique for GaN FETs. The high voltage level shifter in GaN drivers should achieve a low propagation delay to support high switching frequency with high efficiency. The bootstrap circuit in GaN drivers should control the bootstrap (BST) rail voltage to improve the reliability of GaN FET and driving circuits.

TECHNICAL APPROACH

The up and down level shifters in GaN driver are used to realize non-overlapping driving signals of high side and low side power switches. Reducing the deadtime by minimizing the propagation delay of level shifter is an effective way to improve power conversion efficiency at high frequencies. To improve the reliability of GaN FET and driving circuits, the bootstrap circuit should be actively controlled to achieve constant and safe voltage on the bootstrap rail.

SUMMARY OF RESULTS

As shown in Fig. 1, the proposed GaN driver contains two high speed level shifters and an active BST balancing controller. The level shifters in the driving signal transmission line are used to make V_{GH} and V_{GL} non-overlapping. The long delay of level shifter results in high power loss during deadtime which deteriorates power efficiency. So low propagation delays in high speed level shifters enable an increase of switching frequency and improvement of efficiency.

GaN FETs do not have a parasitic diode which is different from conventional silicon FETs. The conventional BST circuit for silicon FETs does not fit for GaN FETs. During deadtime the reverse voltage drop of GaN FET will be much lower than that of a silicon FET, and the voltage on bootstrap capacitor C_{BST} will be much higher which may damage GaN FET and driving circuits. In order to address the issues, an active BST balancing circuit is proposed to regulate the BST rail voltage and prevent C_{BST} being overcharged.

The operation of active BST balancing is as follows. When the high side GaN FET M_H turns on, the bootstrap switch is kept off. When M_H turns off, switching node voltage V_{SW} falls because of continuous positive inductor current. V_{SW} may even fall to -3V depending on inductor current before M_L turns on. During this period, M_{BST} keeps off to block the charging path for C_{BST}. When M_L is turned on, V_{SW} starts to rise from negative. V_{SW} is sensed and once it is higher than the predefined reference voltage, M_{BST} will be turned on by V_{pgate}. V_{DRV} starts to charge C_{BST} through M_{BST} and high voltage diode D_{HV}. When V_{GL} turns off M_L, M_{BST} is turned off by V_{pgate} and the C_{BST} charging process is terminated. Thanks to the active bootstrap balancing control, the charging path is blocked during deadtime. Overcharging of C_{BST} is avoided and the BST rail voltage can be controlled precisely. The reliabilities of GaN and driving circuits are improved. The idea has been successfully verified in a preliminary simulation in Fig. 2. The BST rail voltage is controlled below 5V with the ripple of 52mV. C_{BST} charging time t_{charge} is kept constant.

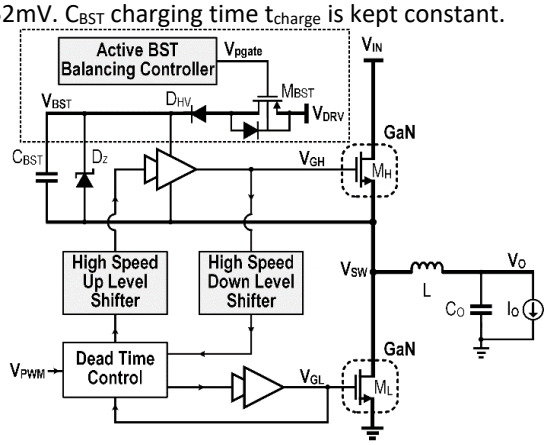

Figure 1. The GaN driver with high-speed level shifters and active BST balancing control.

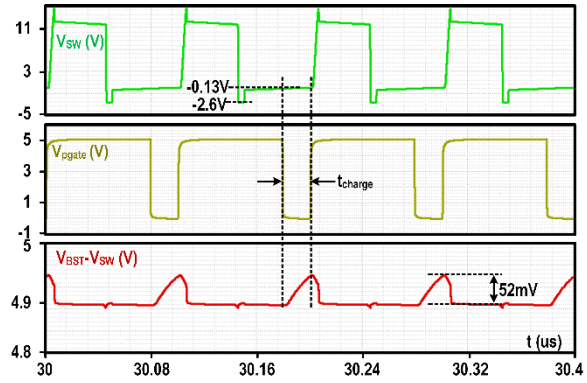

Figure 2. Simulation results of active BST balancing control.

Keywords: GaN driver, high speed level shifter, active bootstrapped balancing, high switching frequency, high efficiency.

INDUSTRY INTERACTIONS

Texas Instruments, IBM

MAJOR PAPERS/PATENTS

TASK 2712.028, HIGH PERFORMANCE MICRO-SUPERCAPACITOR ON A CHIP BASED ON A HIERARCHICAL NETWORK OF NITROGEN DOPED CARBON NANOTUBE SHEETS SUPPORTED MNO_2 NANOPARTICLES

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SIGNIFICANCE AND OBJECTIVES

This study aims to fabricate and characterize a high performance microsupercapacitor based on carbon nanotube (CNT) sheet array and to improve its performance.

TECHNICAL APPROACH

The biggest challenge involved in fabrication of a device using CNT sheets arises from their delicate structure. Two approaches to overcome this problem are being investigated. One is to use plasma etching using a shadow mask to avoid using a photoresist. The other approach is based on a common photolithography process.

SUMMARY OF RESULTS

Carbon nanotube sheet electrodes were first characterized (Figure 1). The CNT sheets exhibit excellent life cycle and capacitance loss is less than 10 % after 10,000 CV cycles.

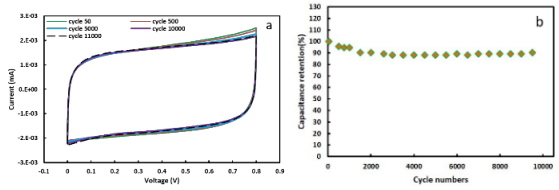

Figure 1. a) Cyclic voltammetry of the CNT sheet electrode up to 11,000 cycles and b) capacitance retention (%).

A plasma process for patterning of an interdigitated microsupercapacitor based on a carbon nanotube sheet with high critical dimension was successfully developed and characterized (Figure 2.).

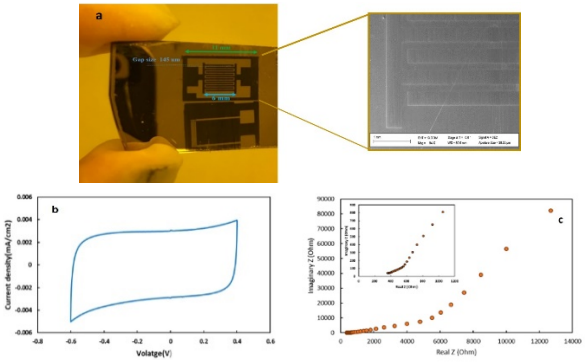

Figure 2. Cyclic voltammetry at scanning rate of 50 mv/s and Impedance spectroscopy measurements of CNT sheet based microsupercapacitor.

To improve the capacitive behavior, CNT arrays were doped with nitrogen (Figures 3 & 4). There is a very small voltage drop in the discharge curve. The n-doped device shows negligible loss (12 %) after 2,000 cycles but lower chemical stability compared to pristine CNT.

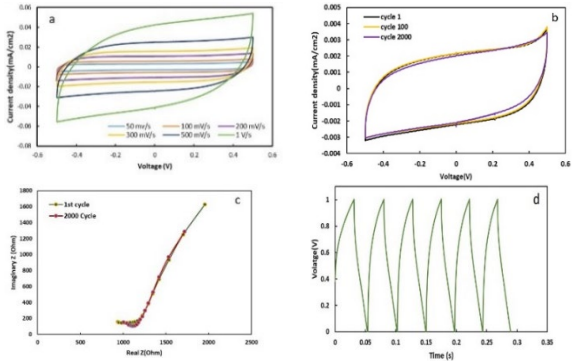

Figure 3. a) CV curves at different scanning rate from 50 mVs^{-1} to 1 Vs^{-1}, b) life cycling test, c) EIS measurements before and after cycling, d) galvanostatic charge-discharge experiment at 50 µA current shows a promising power density.

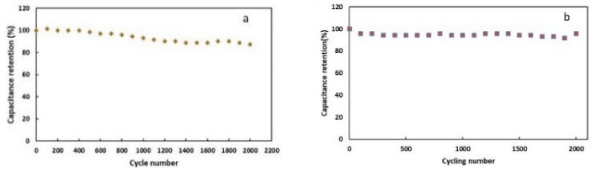

Figure 4. Capacitance retention of microsupercapacitor based on a) n-doped carbon nanotube which shows 12 % drop in capacitance over 2,000 cycles and b) pristine CNT with less than 4% loss in capacitance

Preliminary results indicate the capability of array of CNT sheet and nitrogen doped CNT sheets for supercapacitor applications but further studies are needed.

Keywords: Carbon nanotube sheet, Nitrogen doped, microsupercapacitor, metal oxide, micro-device

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

TASK 2810.002, SECURITY-AWARE DYNAMIC POWER MANAGEMENT FOR SYSTEM-ON-CHIPS

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SIGNIFICANCE AND OBJECTIVES

The proposed research investigates the energy-security trade-offs associated with Dynamic Power Management (DPM). The proposed effort will develop methodology to characterize security implications of DPM in SoCs and design circuit/system techniques to co-optimize security and energy-efficiency of DPM.

TECHNICAL APPROACH

This effort will purse a cross-layer approach to understand the energy-security trade-offs in Dynamic Voltage Frequency Scaling (DVFS). First, we will design power domains that are secure against power-/EM- side-channel analysis by leveraging the distributed integrated voltage regulators. Next we will investigate energy-security trade-off at the chip level by focusing on the DVFS controller and algorithm. Finally we will explore an integrated approach considering secure power domains and secure DVFS controllers.

SUMMARY OF RESULTS

Dynamic power management (DPM) is an integral part of modern SoC which utilizes combined hardware and software approach for energy efficiency. Techniques like dynamic frequency and voltage scaling (DVFS) play crucial role in balancing power and performance of battery powered smartphone devices. In the past, information leakage from side-channels on processors have been exploited to profile instructions, learn program control flow or recover programs, and more recently to identify anomalies and malicious code. But, leveraging information using these techniques requires physical access to devices, expensive acquisition setups, additional pre-processing steps. In this work, we have depicted that fine-grained DVFS control generates a vulnerability wherein, aggressive frequency scaling patterns give indication about core activity, which is a potential information leak, thereby compromising security. The advantage of this attack lies in its simplicity and low cost. The attacker only injects shellcode and poll DVFS states. This dependency has been exploited in our work to identify apps running on a mobile processor. We have explored several supervised learning techniques to classify ARMv8 processor benchmarking application on an Android device (Snapdragon 820 Quad core processor). We used both techniques, DVFS states and EM side channel emanations to develop features. In our key findings, we demonstrate the simplicity of attack, measure the distinctness through classification accuracy, and compare the effectiveness of two techniques

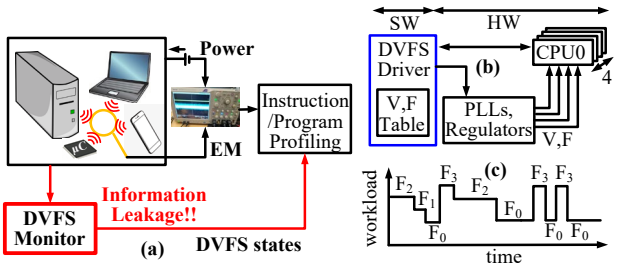

Figure 1. (a) Dynamic voltage frequency scaling algorithms can be a critical side channel for analyzing program behavior, (b) hardware/software approach for power management in modern SoCs, and (c) dynamic management of frequency (and voltage) under varying workloads for a quad-core system

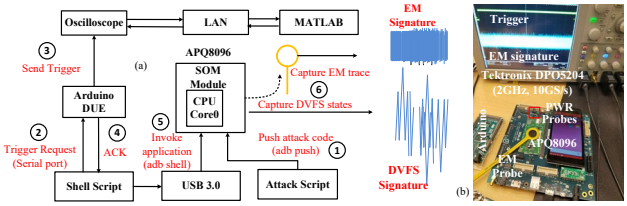

Figure 2. (a) Measurement Setup details to capture DVFS and EM-signature (b) Open-Q APQ8096 System-on-Module development platform for characterization.

Keywords: secure, side-channel, dynamic power management, integrated voltage regulator, dynamic voltage frequency scaling

INDUSTRY INTERACTIONS

Intel, IBM

MAJOR PAPERS/PATENTS

TASK 2810.003, INTEGRATED VOLTAGE REGULATOR MANAGEMENT FOR SYSTEM-ON-CHIP ARCHITECTURES

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SIGNIFICANCE AND OBJECTIVES

We propose to investigate the implication of integrated voltage regulators (IVRs) from a holistic system-level power optimization perspective that is able to account for higher-level temporal workload and spatial chip-wide execution characteristics in order to achieve the maximum efficiency in future heterogeneous systems.

TECHNICAL APPROACH

At the circuit level, we plan to develop a flexible framework for IVR design space exploration that supports different IVR topologies and power delivery network configurations. At the architecture level, we focus on power and supply noise characterization and worst-case analysis in order to understand deeply the interaction between workload behaviors and their dynamic supply noise impacts. At the run-time, we explore feedback-directed prediction-enhanced optimization and develop scheduling algorithms and techniques at the firmware and operating system layer to make efficient use of IVRs.

SUMMARY OF RESULTS

We propose three specific research tasks as well as a comprehensive evaluation platform. Promising preliminary results have been obtained following the project kick-off in June 2018.

First, we have made significant prior contributions to the development of a fast and accurate circuit-level IVR model to conduct design space explorations. The previous IVR research focused on either circuit-level implementation or limited system-level investigations dictated by a single special IVR realization. Instead, our method aims to build a parameterized IVR analytical model that can accurately capture the key performance metrics and dynamic behaviors of an IVR.

Our initial results reveal that although the specific implementation of IVRs vary greatly, they abide by the same fundamental design trade-offs, formulations, and principles that could be extracted and modeled. We have started developing an early-stage design exploreation tool for IVR called Ivory [1], which covers a spectrum of IVR topologies including low drop out (LDO) regulators, buck converters, and switched-capacitor converters. Ivory is able to derive the conversion efficiency, conversion delays, and area overhead from high level inputs such as the supply voltage ranges and load current conditions, with more than 1000x speed-up compared to SPICE level simulation. We plan to extend Ivory in the future to handle multi-level hierarchical power delivery networks and IVRs.

Next, our workload characterization effors are currently underway and will capture the complex interactions among diverse IP blocks (cores and accelerators) at the micro-architecture level and reveal their inherent trade-offs between performance and reliability due to shared resources such as memory, interconnect, and power grid. We have developed a formal approach to rigorously generate the worst-case scenarios of supply for manycore architectures with distributed workloads. This method will be generalized to heterogeneous SoC architectures.

Finally, we plan to investigate the potential application of software-implemented distributed demand-response management strategy in the context of IVR-enabled SoC. Our current work leverages the control theory to dynamically manage the load activities in manycore architectures and prior works have studied the impact of co-scheduling on homogeneous processors. In a similar vein, we believe that with distributed IVRs, there is another interesting degree of scheduling freedom available that involves the spatial disbribution and allocation of power to the different IP blocks in a heterogeneous SoC. These insights will guide our next-step for investigation in the system-level run-time optimization.

Concurrent with all these efforts is our plan to develop a novel hardware evaluation platform for rapid design space exploration and prototyping of IVR-enabled on-chip power delivery.

Keywords: voltage regulation, power delivery, energy efficiency, power optimization, heterogeneous SoC

INDUSTRY INTERACTIONS

Intel

MAJOR PAPERS/PATENTS

[1] A. Zou et. al., “Ivory: Early-Stage Design Space Exploration Tool for Integrated Voltage Regulators”, DAC, 2017.

TASK 2810.006, COMBATING UNPRECEDENTED EFFICIENCY, NOISE AND FREQUENCY CHALLENGES IN MODERN HIGH CURRENT INTEGRATED POWER CONVERTERS

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SIGNIFICANCE AND OBJECTIVES

To optimize the design trade-off between EMI noise and power efficiency in GaN power converters, gate switching with low di/dt and high dv/dt is in demand. Miller Plateau (MP) identification is critical to achieve independent control of low di/dt and high dv/dt. For this, an adaptive MP sensing is proposed here.

TECHNICAL APPROACH

Ideally, Miller Plateau voltage (V_{MP}) of GaN switches can be emulated by V_{FW} dynamically at the switching node during the current freewheeling period. The same I-V characteristic of both high side and low side GaN switches eliminates the dependency of V_{MP} on the electrical parameters without adding any extra mirroring power device. After identifying V_{MP} precisely, it is used as a dynamic regulation reference to detect the MP starting point. By this way, the proposed adaptive MP sensing (AMPS) eliminates the issues of the large delay time and low accuracy in the conventional sensing methods.

SUMMARY OF RESULTS

The basic principle of the proposed emulated MP tracking (EMPT) for AMPS is illustrated in Figure 1. At the MP starting point, the high side GaN switch (M_H) works in saturation and conducts the inductor current I_L with $V_{GSH}=V_{MP}$, where V_{GSH} is the gate-to-source voltage of M_H. If $I_{DSH}=f(V_{GSH})$, where I_{DSH} is the drain current of M_H and $f(\bullet)$ denotes the functionality of I_{DSH} versus V_{GSH}, then $V_{GSH}=f^{-1}(I_{DSH})$. Thus, $V_{MP}=f^{-1}(I_L)$. Now let's investigate the conduction of the low side GaN switch (M_L) during the current freewheeling period (t_{CF}). During t_{CF}, the gate of M_L is pulled down to the ground and M_H is not turned on yet. Then it means that after M_L is turned off, either M_H or M_L stays off and does not conduct any current. As I_L cannot change instantaneously, it acts as a current source to discharge the switching node (V_{SW}) continuously. In the conventional power circuits where the power devices are silicon MOSFETs, V_{SW} would be clamped by the body diode of M_L to a negative p-n junction forward voltage. However, GaN FETs do not have such a p-n junction body diode. The result is that V_{SW} is discharged to a much more negative voltage level ($-V_{FW}$), such that the gate-drain voltage (V_{GDL}) of M_L is sufficient to conduct I_L in the reverse conduction mode. Because of this, the GaN power stage can be in a current freewheeling mode. Accordingly, if the GaN FET is drain-source symmetric and the channel length modulation effect is ignored, then V_{FW} can be calculated as $V_{FW}=f^{-1}(I_L)$ and $V_{MP}=V_{FW}$.

It suggests that the Miller Plateau voltage (V_{MP}) can be tracked by sensing V_{FW}. It is well known that it is hard to detect V_{MP} directly due to the extremely fast switching transient. On the other hand, t_{CF} is easily predicted by appropriate timing control. Therefore, it is much easier to detect V_{FW} by sensing V_{SW} during t_{CF}. Thus, the sensed V_{FW} can be used as a reference voltage to identify the MP starting point during the high side switching. Besides, V_{FW} varies along with I_O naturally. Therefore, I_O does not needed to be sensed for dynamic MP prediction. Overall, the accuracy issue existing in the conventional Miller Plateau detections is eliminated by V_{MP} emulation through sensing V_{FW}.

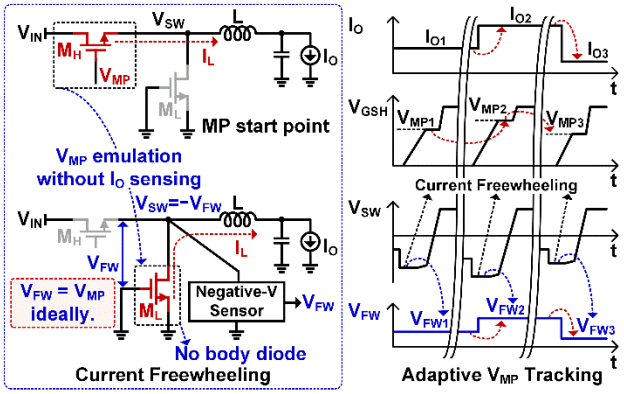

Figure 1. Basic principle of emulated Miller Plateau tracking.

In the following year, based on the above pricinple, the circuit incorporating AMPS will be implemented. This will then be applied to adjust the gate driving strength to achieve the expected balance performance of EMI noise and power efficiency.

Keywords: Miller plateau, di/dt and dv/dt control, EMI regulation, adaptive MP sensing, GaN FET

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

TASK 2810.008, CIRCUIT TECHNIQUES FOR FAST START-UP OF CRYTAL OSCILLATORS

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SIGNIFICANCE AND OBJECTIVES

High-Q crystal oscillators are notorious for being extremely slow at start-up. Their long start-up time increases the average power consumption in duty-cycled systems such as Internet-of-Things. The objective of this work is to reduce the start-up time with minimal energy consumption.

TECHNICAL APPROACH

Previously, we demonstrated an oscillator start-up technique that pre-energizes a high-Q resonator close to its final steady-state energy using a low-Q "injection" oscillator for a precisely-calculated, short duration (~100cycles). The technique achieved 15x faster startup than all prior art. The short injection duration, which amounts to wideband signal injection, and a PTAT injection signal drive, together, make the technique tolerant to +/-6500ppm injection frequency errors from temperature and resonator/circuit process variability. This project will change the injection duration in a temperature-dependent manner to further reduce the temperature sensitivity. It will also extend it to other high-Q oscillator topologies.

SUMMARY OF RESULTS

The block diagram of the precisely-timed energy injection technique is shown in Figure 1. The crystal oscillator is implemented in a Pierce configuration with an amplitude regulator loop. A PTAT voltage regulator is used to set the injection amplitude during start-up. This will make the injection amplitude linearly track the oscillation amplitude, which results in a constant, PVT-invariant injection duration [1]. Since the technique relaxes the matching requirement between the injection and resonance frequencies, a simple temperature-compensated ring oscillator provides the injection signal.

A prototype IC was fabricated in a TSMC 65nm CMOS process prior to the start of this project. Figure 1 shows the measured start-up time as function of intentionally introduced errors in the injection duration and frequency: no degradation was observed in the start-up time for up to ±10% and ±6500ppm variations in the injection duration and frequency, respectively. As seen from the Figure, our technique demonstrated 20x lower start-up time with dramatically lower sensitivity to the injection frequency. To the best of our knowledge, our technique achieved the lowest start-up energy of reported prior art (~12nJ). The low start-up energy is a result of having a small injection duration.

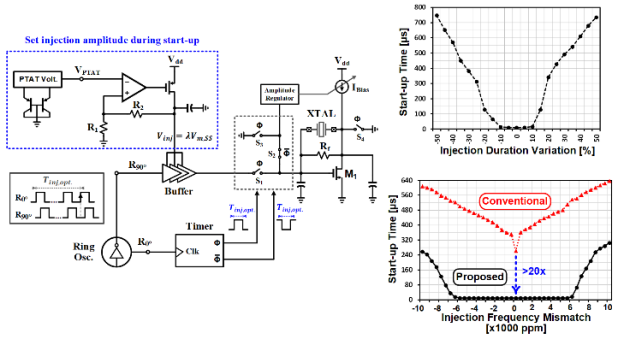

Figure 1. Block diagram of the proposed technique with measured start-up sensitivity of the 10 MHz XO to the variations in Injection duration and frequency.

While our implementation provides a robust, quick start-up, it requires a precise injection oscillator to kick-start very stable oscillators, e.g., TCXOs/OCXOs. Theoretical analyses and simulation results suggest that an adaptive (instead of fixed) injection duration can enable quick startup in TCXO/OCXO with <1ppm stability. Figure 2 shows how the frequency insensitivity range is broadened by properly varying the injection duration.

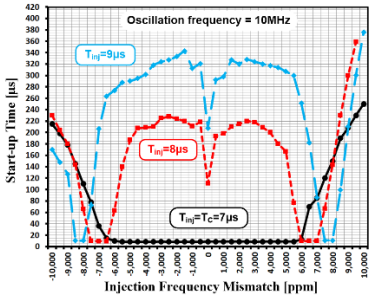

Figure 2. Circuit simulations for multiple injection durations.

Keywords: start-up time, crystal oscillators, low power, energy injection, Internet of Things

INDUSTRY INTERACTIONS

Intel, AMD

MAJOR PAPERS/PATENTS

[1] H. Esmaeelzadeh and S. Pamarti, "A Quick Startup Technique for High- Q Oscillators Using Precisely Timed Energy Injection," *JSSC* 2018.

[2] H. Esmaeelzadeh and S. Pamarti, "A precisely-timed energy injection technique achieving 58/10/2µs start-up in 1.84/10/50MHz crystal oscillators," *CICC* 2017.

TASK 2810.009, MIXED-SIGNAL BUILDING BLOCKS FOR ULTRA-LOW POWER WIRELESS SENSOR NODES

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DAVID BLAAUW, UNIVERSITY OF MICHIGAN

SIGNIFICANCE AND OBJECTIVES

This project develops novel and state-of-art performing ultra-low power mixed-signal circuits, suitable for IoT systems. This includes timekeeping circuits, amplifiers, and CMOS-based sensors.

TECHNICAL APPROACH

The most challenging ultra-low power circuit components are mixed-signal circuits such as timers, clock sources, sensing and interface circuits (e.g., temperature sensors and low-noise amplifiers). Some of these cannot be duty cycled (e.g., timers), while others require both low noise and low power (e.g., amplifiers), which are traditionally mutually exclusive. This work proposes new ULP designs for: 1) crystal oscillator based real time clocks (RTCs), 2) temperature-compensated wakeup timers, 3) temperature sensors, and 4) front-end low-noise amplifiers.

SUMMARY OF RESULTS

A challenge in the design of on-chip wake-up timers for compact wireless sensor nodes is to achieve high timing accuracy over temperature and supply voltage variation within an ultra-low power budget. We propose a gate-leakage-based frequency locking timer with first- and second-order cancellation achieving 260 ppm/°C from −5 to 95°C. The timer consumes 224 pW at 90 Hz output frequency with 0.93%/V supply voltage dependence in the 1.1-3.3 V range. Figure 1 shows the overall circuit topology, including voltage reference generators that serve to compensate for temperature dependency.

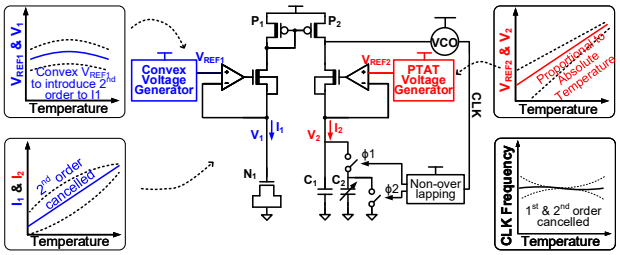

Figure 1. Overall structure of the proposed timer.

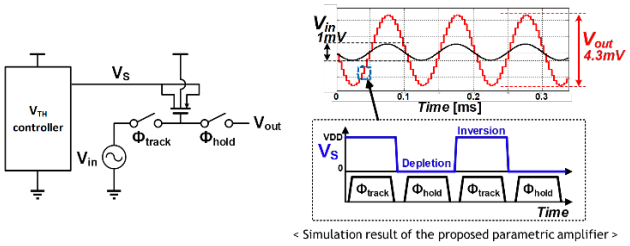

Figure 2. The architecture of the parametric amplifier.

This project also developed a 2.2 noise efficiency factor (NEF) instrumentation amplifier for neural recording applications. A parametric amplifier based on the MOS C-V characteristic is designed as a pre-amplifier stage, lowering the input referred noise of the following stages by 3.4X. Sampling noise is minimized by oversampling the input signal and switching power is reduced by adopting an 8-phase soft-charging technique. Figure 2 shows the architecture of the parametric amplifier.

Keywords: CMOS, low-noise amplifiers, mixed-signal

INDUSTRY INTERACTIONS

Intel

MAJOR PAPERS/PATENTS

[1] J. Lim, T. Jang, M. Saligane, M. Yasuda, S. Miyoshi, M. Kawaminami, D. Blaauw, and D. Sylvester, “A 224pW 260ppm/°C gate-leakage based timer for ultra-low power sensor nodes with second-order temperature dependency calibration,” *IEEE Symposium on VLSI Circuits*, 2018.

[2] T. Jang, K. Choo, J. Lim, S. Nason, J. Lee, S. Oh, S. Jeong, C. Chestek, D. Sylvester, and D. Blaauw, “A 2.2 NEF neural-recording amplifier using discrete-time parametric amplification,” *IEEE Symposium on VLSI Circuits*, 2018.

TASK 2810.010, GS/S ADC BASED CYCLE-TO-CYCLE CLOSED-LOOP ADAPTIVE SMART DRIVER FOR HIGH-PERFORMANCE SIC/GAN POWER DEVICES

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SIGNIFICANCE AND OBJECTIVES

Silicon-Carbide and Gallium-Nitride power devices can be driven at high frequency but the gate drivers for these devices suffer from a tradeoff between electromagnetic interferences and power efficiency. The objective of this research is to demonstrate a SiC/GaN driver that can maximize the power efficiency while meeting EMI requirements.

TECHNICAL APPROACH

We propose a smart gate driver capable of evaluating the EMI on a cycle-to-cycle base thus minimizing the power consumption under different EMI requirements. During the switching-on transition, a high-speed GS/s ADC is used to detect the ringing levels reflecting the EMI levels. The gate driving strength of GaN device will then be regulated to meet the EMI upper limits. While meeting the EMI requirements, the driving strength of the GaN device will be set to the maximum level to shorten the miller plateau thus maximizing the power efficiency. The EMI regulation and Miller plateau regulation operate cycle-by-cycle.

SUMMARY OF RESULTS

Figure 1 depicted a schematic of a typical half-bridge buck converter with the proposed smart gate driver. C_{sample} is connected to the switching node to sample the ringing of V_{sw} for the high-speed ADC. The ringing at different magnitudes which reflect the levels of the EMI are sampled by GS/s ADC. Compared to a conventional peak detector circuit which can only detect the maximum points of the signal, the sampled data by ADC are stored and processed in the digital domain to obtain the more complete picture of the ringing waveform to avoid interference from the glitches which are not induced from EMI.

The ringing information sampled by ADC is compared to a preset EMI code which sets the regulated EMI level. When the ringing magnitude is higher, the driving strength of the GaN device will be decreased to reduce to suppress the EMI level cycle-by-cycle. Likewise, when the ringing magnitude is lower than the EMI code, the driving strength will be increased to shorten the switching time to improve the power efficiency.

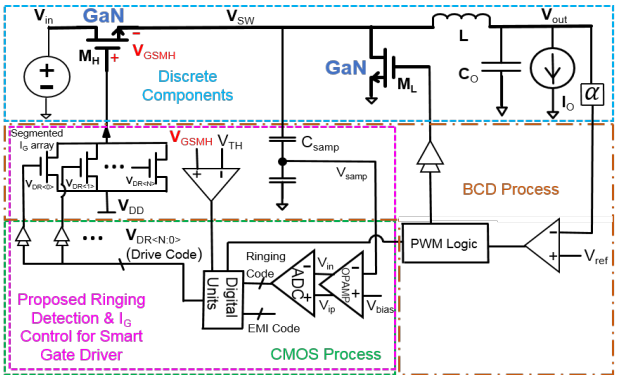


Figure 1. The architecture of a half-bridge buck converter with the smart gate driver.

We choose the SAR topology for the ADC to achieve both high speed sampling as well as low power consumption. Our recent work on a 1GS/s 8-bit SAR ADC has demonstrated that it can operate at 1GS/s with 8-bits with a power consumption of around only 3mW [1]. The SAR ADC employs a single external clock of 1GHz. The SAR logics operates asynchronously in order to maximize the ADC conversion speed. The differential voltage of V_{SW} will be sampled onto a capacitive DAC and then quantized by the SAR logic to get the V_{SW} code during the ringing period. The digitized V_{SW} values are further processed to get the ringing profile which reflects the level of the EMI at the time. Compared to the EMI code, the decoder will generate the drive code to further control the gate current on the M_H.

Keywords: GaN driver, Miller plateau regulation, high-speed ADC, smart driver, EMI regulation

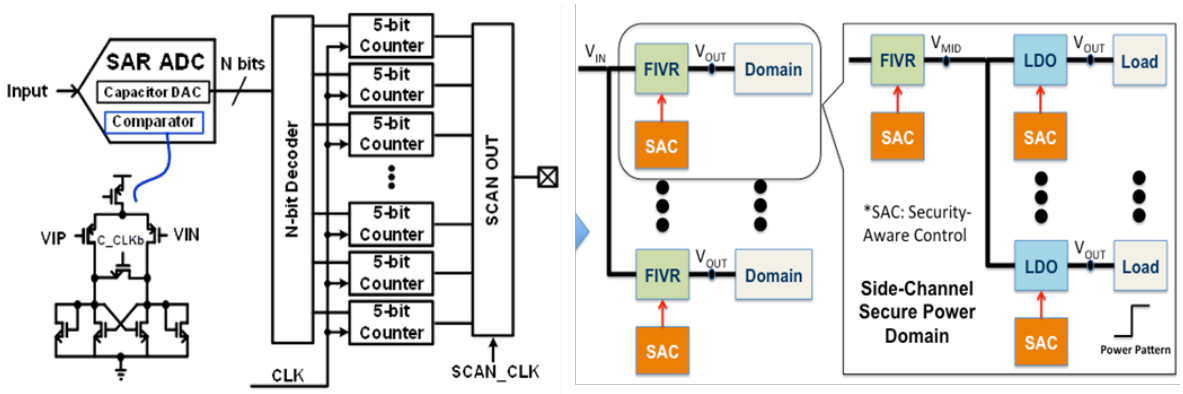
INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] G. Wang et al., "A 43.6-dB SNDR 1-GS/s Single-Channel SAR ADC using Coarse and Fine Comparators with Background Comparator Offset Calibration," 2017 ESSCIRC, Sep. 2017, Leuven, Belgium.

Safety, Security and Health Care Thrust



Category	Accomplishment
Safety, Security and Health Care (Systems)	Online fault diagnosis/failure prognosis methods are paramount for identifying incipient faults of power semiconductor devices and determining IGBT state of health based on monitoring electrical failure precursors. Studies have been conducted to identify the most reliable aging precursors, based on which a start/stop diagnostic circuit has been designed for gate drivers and a method for estimating the remaining useful lifetime based on Gaussian process modeling has been developed and experimentally demonstrated. (1836.154 Akin, UT Dallas)
Safety, Security and Health Care (Systems)	Dynamic power management and security methods are both important for modern SoCs but have typically been developed independently. This task seeks to study the interplay between dynamic power management and security. Recent studies have demonstrated the effect of integrated voltage regulators and adaptive clocking-based voltage dithering on reducing information leakage through power and electromagnetic side channels in cryptographic cores. (2810.002 Mukhopadhyay, Georgia Tech)
Safety, Security and Health Care (Systems	Modeling aging effects as a function of their workload is imperative for evaluating reliability of analog/mixed-signal ICs. This task is developing dedicated test structures and in-situ monitoring circuits in order to measure BTI/HCI effects, along with simulation frameworks for projecting lifetime reliability and design guidelines for mitigating aging effects in analog/mixed-signal ICs. To date, an in-situ INL/DNL measurement block has been used for SAR-ADC DNL measurement, and the frequency and phase noise degradation of an all-digital PLL have been measured using simple on-chip monitoring circuits. (2712.017, Kim, U. of Minnesota)

TASK 1836.117, PERFORMANCE AND RELIABILITY ENHANCEMENT OF EMBEDDED ADCS WITH VALUE-ADDED BIST

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DEGANG CHEN, IOWA STATE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

The objectives are to develop procedures for implementing parametric BIST of ADCs with minimal area overhead, to use on-chip test results to enhance performance by digitally calibrating the ADC, and to experimentally demonstrate the BIST and BIST-based calibration on an ADC internal to a microcontroller.

TECHNICAL APPROACH

A Functionally Related Excitation (FRE) approach to testing using a Stimulus Error Identification and Removal (SEIR) algorithm will be adapted to a BIST solution. The FRE/SEIR approach was developed in conjunction with TI on a previous SRC project. On-chip FRE signal generators using the shift operator will be developed for test signal generation and existing on-chip computation resources will be utilized to minimize the area overhead required to implement the SEIR algorithm. Target area overhead is at most 10% of the area of the existing uncalibrated ADC that is currently in high-volume production.

SUMMARY OF RESULTS

A block diagram showing the BIST capability and the BIST-based calibration is shown in Fig. 1 with a target 12-bit ADC. Two additional bits of resolution have been added to the SAR ADC to allow for a 2-bit improvement in linearity with the BIST-based calibration. The final output is then decimated back to 12 bits after calibration.

The signal generator will be a current ramp based integrator comprised of the output from a simple regulated cascode current source charging a nonlinear capacitor. With the FRE/SEIR approach, linearity of the ramp is of little concern. To manage the size of the integration capacitor, a series of faster-rising ramps will be used instead of a single ramp. A second-generation level-spreading ramp generator using a dithered integration starting voltage was developed to maintain approximately uniform density of the input signal throughout the input range of the ADC.

A critical component is the shift generator which must have a constant shift. The second-generation shift generator of Fig. 2 that provides rail-to-rail output using correlated level shifting (CLS) and that provides the constancy needed for testing 14-bit ADCs has been designed. The BIST circuitry has been added to an existing ADC that is in volume production and a test circuit comprising the BIST-enabled ADC has been fabricated. A testbench for the fabricated ADC is under development.

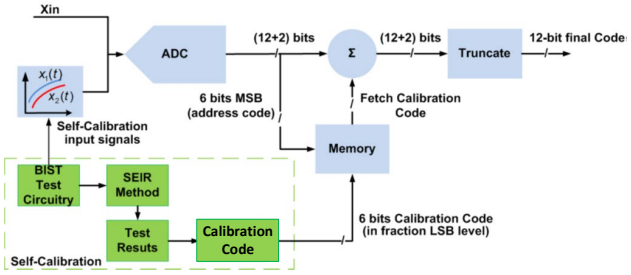

Figure 1. Block Diagram of ADC with BIST-Based Calibration and Value-Added BIST.

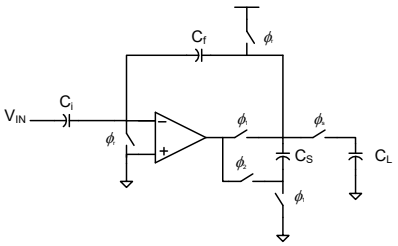

Figure 2. FRE shift generator using correlated level shifting for rail-to-rail outputs.

Keywords: ADC BIST, self-calibration, analog testing, FRE signal generators, SEIR testing

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] H. Meng, R. Geiger, and D. Chen, "A High Constancy Rail-to-rail Level Shift Generator for SEIR-based BIST Circuit for ADCs", 2018 IEEE Int. Symp.on Circuits and Systems (ISCAS), pp. 1-5, May, 2018.

TASK 1836.126, DESIGN SPIN REDUCTION VIA INTEGRATED THZ DESIGN: APPLICATIONS, PHYSICS, AND SYSTEM ENGINEERING

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CHRISTOPHER F. NEESE, OHIO STATE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

The objective of this project was to develop a THz System Engineering Tool that allows for analysis of systems based on the characteristics of their building blocks and to validate it by applications to systems of interest.

TECHNICAL APPROACH

This effort included: (1) Diagnostics and process control in semiconductor plasma reactors, and (2) in parallel the development of CMOS systems for this application, as well as more generally for gas sensors. We are also developing a computational System Evaluation Tool to aid in the design of these CMOS circuits.

SUMMARY OF RESULTS

Our effort was to demonstrate and explore applications of CMOS terahertz technology and to support development of appropriate technology. This effort had a number of mutually supporting pieces. Organizationally, we will discuss results in the context of our effort to develop a terahertz tool for the study, characterization, and process control of plasma equipment for semiconductor chip manufacturing.

Physics makes this application favorable. The working pressures of these reactors, 5 – 50 mTorr, are optimal for spectroscopy in the THz and many molecules of interest have strong spectra in the THz. Moreover, these plasmas are transparent and noise free. Finally, it is an absorption techniques which can provide concentration and temperatures from first principles, without system calibration.

Fig. 1 shows an example of a large number of species in a variety of gas mixtures that we have studied. Molecules can have spectra whose sensitivity for trace constituents of the plasma can vary widely.

In another example, shown in Fig. 2, discharges in O_2 are often run between processing steps to clean the system and return it to a steady state. Here we show the results of using absolute measurements of the reaction product CO as an end point measurement. Modeling shows how the minimum detectable concentration varies as a function of THz system parameters.

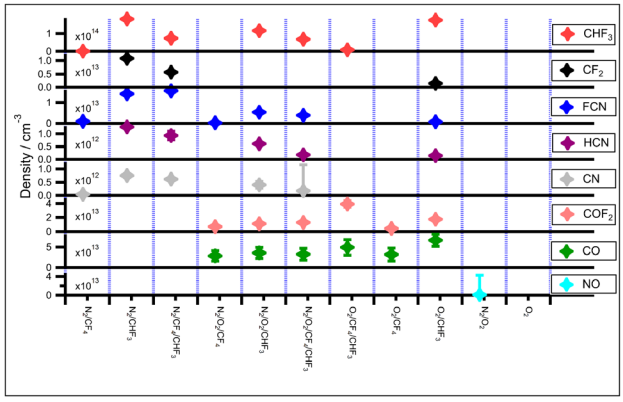

Figure 1. Measurement of absolute densities of CHF_3, CF_2, FCN, HCN, CN, COF_2, CO, and NO in a survey of plasmas produced from combinations of CF_4, CHF_3, N_2, and O_2.

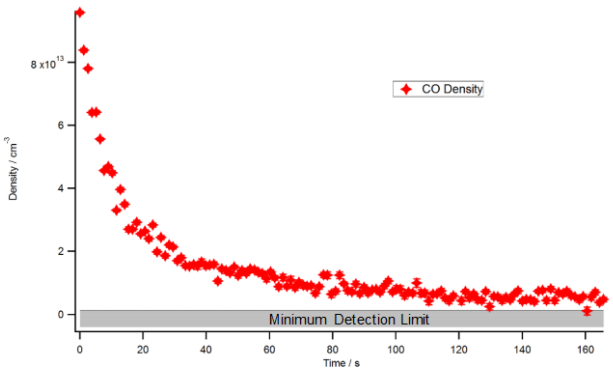

Figure 2. Measured concentration of CO in a cleaning experiment as a function of time. Also shown is the minimum detectable concentration.

Keywords: terahertz, spectroscopy, plasmas

INDUSTRY INTERACTIONS

Texas Instruments, IBM, Applied Materials

MAJOR PAPERS/PATENTS

TASK 1836.130, BUILT-IN SELF-TEST TECHNIQUES FOR TEST, CALIBRATION, AND TRIMMING OF POWER MANAGEMENT UNITS: PMU-BIST

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SIGNIFICANCE AND OBJECTIVES

This project aims at (a) enabling trimming and calibration of PMU/PMICs through static measurements using small footprint BIST circuitry, (b) enabling dynamic testing through open-loop measurements and mathematical modeling, (c) fault analysis and grading approaches to identify design and layout issues, and (d) correlating trim coefficients with measurements.

TECHNICAL APPROACH

We have divided this problem into two parallel threads. First, our goal was to implement a very small foot-print, low frequency analog to digital converter that works in a particular voltage range (1-1.4V) and provides 10 bits of resolution (INL<1mV). Another goal was to implement a dynamic built-in-self-test system for the converter loop to test phase margin in order to evaluate loop stability.

SUMMARY OF RESULTS

The zoom-in ADC was designed and taped out in 2016. The dynamic BIST system is shown in Figure 1. All of the system components are implemented in 40nm GF technology. The overall area of the BIST circuit is 0.019mm^2 and the evaluation time is 20ms. Figure 2 shows the layout of the LDO with BIST. Figure 3 shows the comparison of the BIST circuit response at various load current values to a more traditional technique for phase margin evaluation.

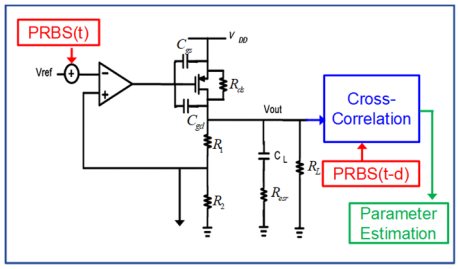

Figure 1. Dynamic BIST for LDOs.

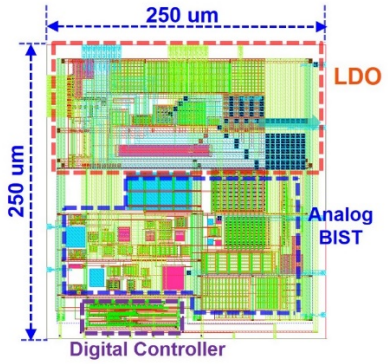

Figure 2. Layout and size for BIST and LDO.

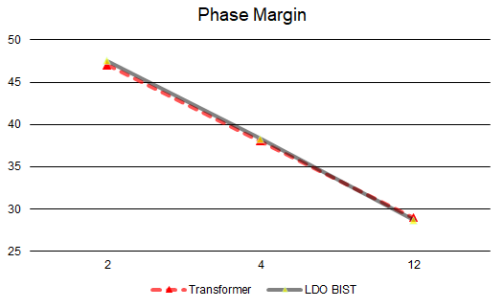

Figure 3. Hardware BIST results compared with loop analysis.

Keywords: BIST, PMU, phase margin, bandgap reference

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

[1] Navankur Beohar, Priyanka Bakliwal, Sidhanto Roy, Debashis Mandal, Bertan Bakkaloglu, Sule Ozev, "Disturbance-free BIST for Loop Characterization of DC-DC Buck Converters", IEEE VLSI Test Symposium, 2015. (Received best paper honorable mention award)

[2] Osman Emir Erol, Sule Ozev, Chandra Suresh, Rubin Parekhji, and Lakshmanan Balasubramanian. "On-chip measurement of bandgap reference voltage using a small form factor VCO based zoom-in ADC." IEEE Design, Automation & Test in Europe Conference, pp. 1559-1562, 2015.

[3] Liu, Tao, Chao Fu, Sule Ozev, and Bertan Bakkaloglu. "A built-in self-test technique for load inductance and lossless current sensing of DC-DC converters." IEEE VLSI Test Symposium (VTS), 2014. (Received Best paper award)

TASK 1836.149, CONDITION MONITORING OF PM/IPM MOTORS THROUGH AXIAL/RADIAL LEAKAGE FLUX

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SIGNIFICANCE AND OBJECTIVES

The fault signature characteristics may cause misleading results depending on motor topology, winding configuration, and controller parameters. However, leakage flux leads superior diagnostic results in time and frequency domain. Simulation and experimental results show that the deployment of a direction-sensitive fluxgate sensor yields promising results.

TECHNICAL APPROACH

The magnetic field distribution plays a fundamental role in motor performance. In particular, the air-gap magnetic field determines the back-emf, torque, stator flux and leakage flux. In order to analyze the circulating flux in and out of the machine, an approximate magnetic equivalent circuit including major reluctances is introduced in PMSMs. Among the flux components, the leakage flux has a relatively low amplitude when compared to air-gap flux (ϕ_g). However, leakage components provide valuable information regarding the motor condition and can be used to detect magnet defect faults in PM motors.

SUMMARY OF RESULTS

Fig. 2. shows the radial flux component behind tooth, and tangential flux component behind slot at 200Hz supply frequency, respectively. When there is a magnet defect fault, the leakage flux contents change across the defected magnet in experimental results. Fig. 3 shows the spectrum of radial and tangential (behind tooth and behind slot) leakage flux components. The signatures rise remarkably and the change in dominant components such as 0.25th and 0.5th harmonics is negligible when the load increases. These tests show that the magnetic field created by the rotor magnets dominates and results in load independent magnet defect analysis. To show the speed effects on the fault signatures when stator is excited, the motor is run at two different speeds under full load both in simulation and experimental tests at 600 rpm

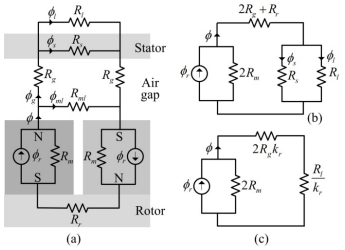

Figure 1. Conceptual fluxgate sensor permeability.

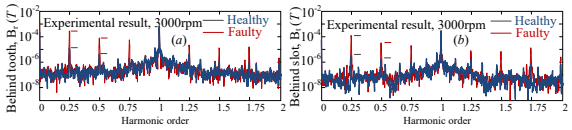

Figure 2. Exp., results, terminals disconnected (back-emf).

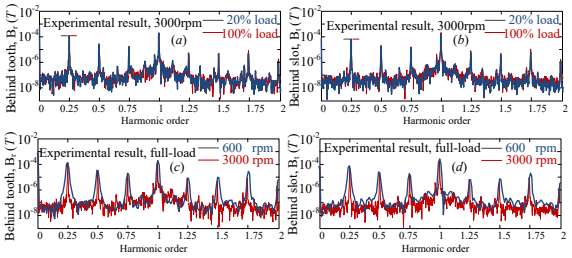

Figure 3. Experimental results, motor operation for different torque/speed profiles.

and 3000 rpm. As shown in Fig. 3(c) and Fig. 3(d), the fault related harmonics are almost speed independent as in the case of open terminal test. Table 1 shows the amplitude of some characteristics fault signatures i.e. 0.25th and 0.5th with different controller parameters in the leakage flux spectrum. In brief, these test results show that the flux based monitoring analysis is more immune to controller parameter changes than current based monitoring.

Table 1. The controller effects on the fault signatures.

Controller parameters	*0.25th (μT)*	*0.5th (μT)*	*0.25th (mA)*	*0.5^{t} mA)*
k_{p_spd}=1; k_{i_spd}=0.005; k_{p_id}=1; k_{i_id}=0.0025; k_{p_iq}=1; k_{i_iq}=0.0025;	*218.5*	*59.9*	*9.19*	*24.4*
k_{p_spd}=1; k_{i_spd}=0.005; k_{p_id}=1; k_{i_id}=0.0125; k_{p_iq}=1; k_{i_iq}=0.0125;	*217.8*	*63.7*	*7.38*	*19.4*
k_{p_spd}=3; k_{i_spd}=0.005; k_{p_id}=1; k_{i_id}=0.0025; k_{p_iq}=1; k_{i_iq}=0.0025;	*211.6*	*64.4*	*7.94*	*18.6*

Keywords: fault diagnosis, condition monitoring, fluxgate sensors, leakage flux spectrum analysis

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] "Comprehensive Analysis of Magnet Defect Fault Monitoring Through Leakage Flux," IEEE Transactions on Magnetics, vol. 53, no. 4, pp. 1-10, April 2017.

[2]"An Investigation of Motor Topology Impacts on Magnet Defect Fault Signatures," IEEE Transactions on Industrial Electronics, vol. 64, no. 1, pp. 32-42, Jan. 2017.

TASK 1836.150, ROBUST HIGH RESOLUTION TECHNIQUES FOR MILLIMETER WAVE RADARS IN COMPLEX ENVIRONMENTS

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SIGNIFICANCE AND OBJECTIVES

This project is developing robust high resolution techniques for millimeter wave radars operating in complex environments. Detailed mathematical framework is developed. Experimental verification of the proposed algorithms using a 24GHz band radar testbeds is carried out in complex enviroments.

TECHNICAL APPROACH

Novel algorithms are designed to localize targets jointly across multiple dimensions using superresolution techniques. For the real time implementation of these algorithms, the emphasis is given on the computational cost reduction. We know that computational cost of joint superresolution algorithms lies mainly in the eigenvalue decomposition of large covariance matrices. To reduce the computational complexity, the size of the covariance matrix should be reduced. Low complexity imaging algorithms are developed using a two stage process. The first stage implements low resolution FFT based digital beamforming. The second stage applies super-resolution techniques to the areas where a higher resolution is desired.

SUMMARY OF RESULTS

Digital beamforming (DBF) based fast Fourier transform implementation (FFT) can efficiently determine the incident angles, range, and Doppler in mm-Wave radars/imagers. Super-resolution techniques use different mechanisms to improve the resolution limit determined by the antenna/sample size. These techniques are data dependent. The 3D information such as (range, angular direction, and Doppler shifts) about targets is embedded in a rank deficient matrix formed from noise-free data. With noisy data, the appropriate subspace is estimated, usually with the eigenvalue decomposition (EVD), and the 3D parameters are extracted from the estimated subspaces. The FFT based DBF techniques have a low complexity of implementation; however, they have a limited resolution resolution limited by the system parameters. Thus, there exists a tradeoff between resolution and complexity. To reduce the computational complexity of superresolution imaging algorithms and still have a high resolution capability, we design two stage detection techniques. The first stage is implemented using 3D FFTs. This stage is known as beamspace processing. Then, the super resolution techniques are applied at the second stage to the areas where a higher resolution is desired.

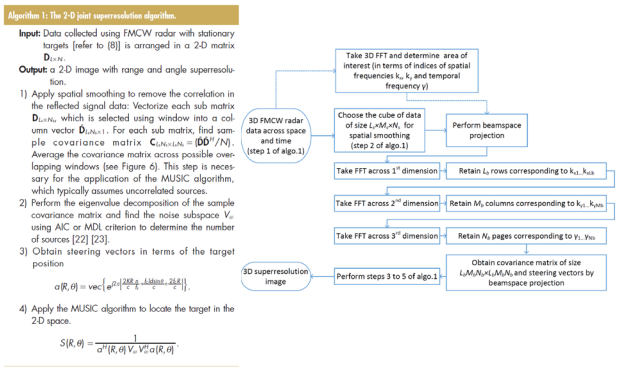

Figure 1. Algorithm 1 lists the details of 2-D version of the joint superresolution algorithm. The flowchart shows how the data are processed by the proposed algorithm.

While modeling the radar systems, the targets and channels under consideration are assumed to be ideal. The targets are modeled as objects with perfect reflectivity and the signals are assumed to propagate through unobstructed paths. To verify the viability of the proposed radar algorithms in the real world, we prototypied a 24 GHz radar testbed at UT Dallas. Sample results are shown in Fig. 2.

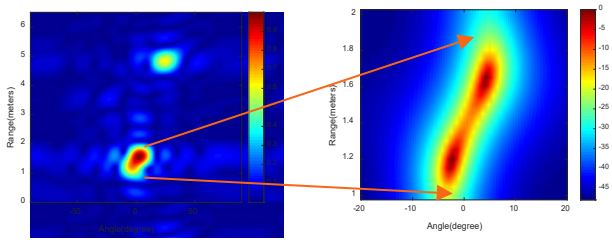

Figure 2. The experimental images at 24 GHz radar with 8 receive antennas. FMCW waveforms. B=250MHz. Three targets are in the view. Two targets are closely spaced by 0.4 meters. FFT based image (left). 2D superresolution based image (right).

Keywords: mm-Wave imaging, space time adaptive signal processing, MIMO radar, clutter reduction

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] S. Patole et al., “Automotive Radars: A Review of Signal Processing Techniques,” IEEE Signal Processing Magazine, March, 2017, vol. 34, no. 2, pp. 22-35.

TASK 1836.154, STATE OF THE HEALTH (SOH) FOR IGBTS: INCIPIENT FAULT CHARACTERIZATION AND DEGRADATION MONITORING

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SIGNIFICANCE AND OBJECTIVES

This project aims to investigate incipient faults of IGBT devices and create online fault diagnosis / failure prognosis tools to establish early warning system for future power electronics (PE) systems. Continuously monitoring these systems is essential to prevent unexpected shutdowns and catastrophic failures that may result in fatal accidents or significant operation loss.

TECHNICAL APPROACH

Prognostics and failure prediction require accurate characterization of IGBT with respect to aging. The proposed apporach determines the state of health for IGBT based on actual in-field data. So, firstly, variations in all current-voltage characteristics and parasitic elements of IGBTs at different thermal stress levels using a custom-built testbed have to be analyzed. Using these aging tests data, failure precursor (electrical measurements) have to be identified and then in-situ measurement circuit(s) need to be developed. Further, based on these in-situ measurements state of the IGBT's health and lifetime have been determined.

SUMMARY OF RESULTS

Remaining useful lifetime (RUL) estimation is the process of determining the remaining time to failure of a specific device based on an aging precursor measured from the device. In simplistic terms, RUL is the data extrapolation of the system for predicting system health condition in future. Generally, extrapolation is done by fitting a model to available data points by minimizing the interpolation error and hoping that this model is valid for future points. Thus, extrapolation is associated with an inherent error.

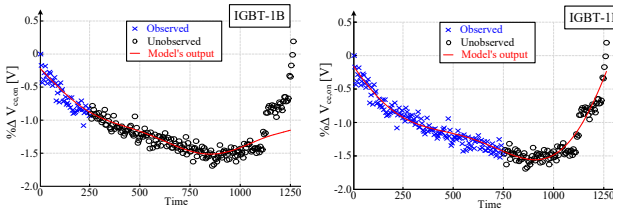

Figure 1. Lifetime estimation results by observing; (a) 250 points and (b) 750 points.

To overcome this difficulty, another information source needs to be included. The later information can be obtained by doing experiments on the devices with the same type. Devices from the same type are expected to fail for the same reasons and having similar aging precursors. Accordingly, an RUL estimator can be developed. Moreover, this estimator can also be biased with the knowledge obtained from prior experiments. With Bayesian inference, the estimator can be biased systematically. Figure 1 shows the effect of applying the prior knowledge in fitting a curve to the health indicator using MAP with different number of observed points. Clearly, the MAP is can accurately predict the End-of-Life (EOL).

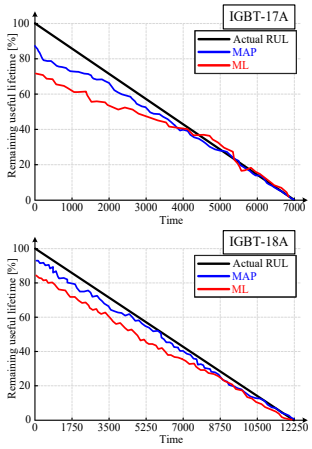

Figure 2. RUL estimation for three different devices using GPR with prior knowledge (MAP estimator) and without prior knowledge (ML) for (a) IGBT-17A and (b) IGBT-18A.

In the last step, accurate RUL estimation can be made by determing the intersection of fitted GPR and EoL threshold fixed based on prior experimental results. Figure 2 shows the results of RUL estimation for three devices and MAP produces accurate estimation results compared to that of ML (conventional method).

Keywords: failure prognosis, on-state voltage drop, aging, Gaussian process regression, remaining useful lifetime estimation

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] S. H. Ali et al., “Lifetime Estimation of Discrete IGBT Devices Based on Gaussian Process,” in IEEE Transactions on Industry Applications, vol. 54, no. 1, pp. 395-403, Jan 2018.

[2] S. Dusmez, S. H. Ali, et al, "Aging Precursor Identification and Lifetime Estimation for Thermally Aged Discrete Package Silicon Power Switches," in IEEE Transactions on Industry Applications, vol. 53, no. 1, pp. 251-260, Jan.-Feb. 2017

TASK 1836.155, DEVELOPMENT OF WIDEBAND VIBRATION SENSORS

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SIGNIFICANCE AND OBJECTIVES

The objective of this research is to design, implement, characterize and optimize a very low power consuming chip-scale vibration sensor that can operate over a wide range of frequency from DC to 10kHz with a resolution of 1mg or better.

TECHNICAL APPROACH

The aim of this research is to be realized without adding any extensive modifications to an existing CMOS process platform. The plan is to utilize the CMOS processed, thinned-down electronic chip as the mechanical component itself which would respond to vibrations in the form of bending that would influence the tensile and compressive stresses on different locations of the chip. These stresses can be then detected by placing a highly piezoresistive coefficient material at the maximum stress locations. The proposed vibration sensor is comprised of an array of several piezoresistive cantilevers each covering a narrow frequency range (~15-100Hz) in the close vicinity of its resonance frequency (Figure 1).

RESULTS

To measure the effect of vibrations on the CMOS chips, a speaker/sub-woofer was used to create sinusoidal vibrations at different frequencies using a network analyzer. The frequency spectrum for the vibration spectrometer was swept and the vibration response for the cantilever array was recorded. A maximum sensitivity of ~5.3mV/V.g was achieved for the longest cantilever with its resonance frequency at ~7.2kHz as shown in Figure 2. Table 1 summarizes the results for an array of 5 cantilevers tested with this approach.

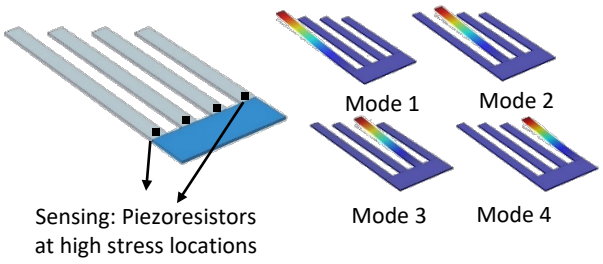

Figure 1. Eigenfrequency and mode shapes for 4 integrated cantilevers, each covering a small portion of the targeted frequency spectrum.

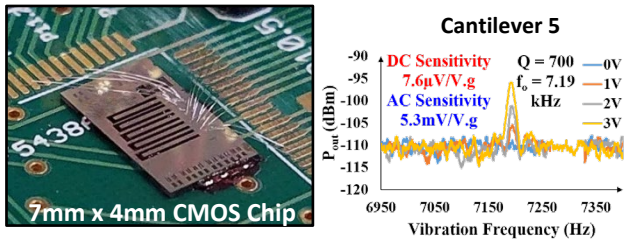

Figure 2. Image of the post processed and wire-bonded CMOS cantilevers along with the response to vibrations at different frequencies for the longest cantilever (Cantilever 5).

Table 1. Summary of the measured parameters for the cantilever array

Cantilever	5	4	3	2	1
Resonance Frequency (kHz)	7.19	8.4	9.5	10.8	12.2
Sensitivity at DC (μV/V.g)	7.6	6.5	5.5	4.74	4
Sensitivity at AC (mV/V.g)	5.3	4.5	5.0	3.32	2.8
Q	700	700	900	700	700
Bandwidth (Hz)	10.2	10.6	10.6	15.5	17.4

The measured DC and AC sensitivities for the different cantilevers, make it possible to sense very low amplitudes of vibrations over a large bandwidth by using a larger number of cantilevers. Further concrete tests on the noise performance of these devices can provide an insight into the absolute resolution and the sensitivity/bandwidth limitation of such sensors.

Keywords: high sensitivity, vibration sensor, low power, CMOS MEMS, large bandwidth.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Kumar V. et.al, “A Low power CMOS-MEMS Vibration Spectrum Nalyzer”, IFCS 2018.
[2] Abbasalipour A. et al., “Thermal Piezoresistive Resonant Mass Balance Implemented in a Standard CMOS Process,” IFCS 2018.

TASK 2712.002, ON-LINE SELF-TESTING AND SELF-TUNING OF INTEGRATED VOLTAGE REGULATORS

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SIGNIFICANCE AND OBJECTIVES

The proposed research will develop low-complexity algorithms and low-overhead all-digital self-testing and self-tuning architecture for high-frequency integrated voltage regulators (IVRs). The work will focus on digitally controlled fully integrated inductive VR (FIVR), digital low-dropout regulators (DLDO), and power delivery system with FIVR and multiple distributed DLDOs.

TECHNICAL APPROACH

The challenge for testing/tuning of IVRs is the presence of high frequency closed-loop control. The proposed approach is based on the principle that in a system with IVR and digital core(s), the testing/tuning should focus on system's performance rather than the IVR in isolation. We propose to characterize the output voltage variation that ultimately determines the performance of the digital load. We consider large signal perturbations (load and reference steps) to excite the transient noise in the IVR's output, and tune the IVR's loop to minimize the noise. Finally, we explore co-tuning of IVR and processor.

SUMMARY OF RESULTS

Self-tuning of Digital Low-dropout Regulator: We have demonstrated all-digital tuning and dynamic control of feedback compensator in digital low drop out regulators (DLDO) to enhance transient performance under process and passive variations, aging, and load changes. The measured results from a 130nm CMOS test-chip shows 2.1× improvement in transient performance under process variations and 30% improvement for aging-induced degradations. We demonstrate 55ns setting time for a 5mA to 45mA load step in 100ps, with 97.8% peak current efficiency.

Performance-based Tuning of Inductive IVR: We have presented an auto-tuning method for fully integrated voltage regulators (IVRs) driving digital cores against variations in passive as well as process/temperature of the core. The key contribution is to perform auto-tuning of the coefficients of the feedback loop of the IVR based on the performance of the digital cores. The proposed performance driven auto-tuning demonstrates potential for up to 12% increase in system performance under inductance and threshold variation. A test-chip has been designed in 130nm CMOS to demonstrate the performance-based tuning. The test-chip is currently being measured.

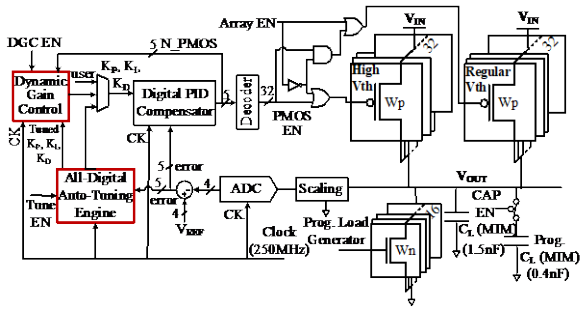

Figure 1. Architecture and test-chip of self-tuning Digital Low-dropout Regulator.

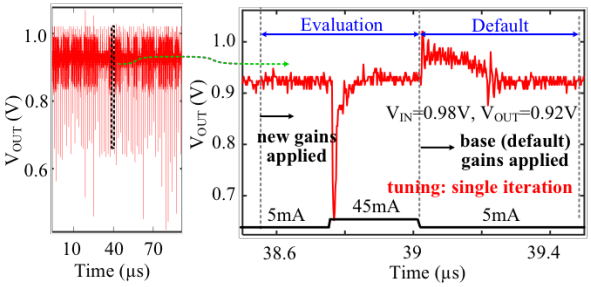

Figure 2. Measurement results showing DLDO tuning.

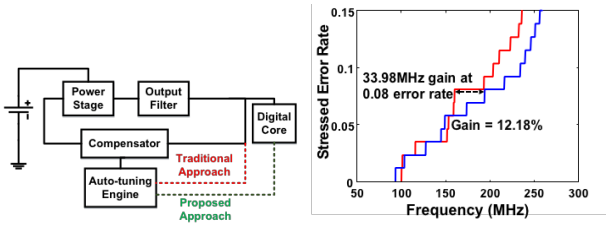

Figure 3. Concept and simulation of performance-based tuning of inductive IVR.

Keywords: integrated voltage regulator, self-testing, and self-tuning.

INDUSTRY INTERACTIONS

Intel, NXP

MAJOR PAPERS/PATENTS

[1] V. Chekuri, M. Kar, A. Singh, and S. Mukhopadhyay, "Performance Based Tuning of an Inductive Integrated Voltage Regulator Driving a Digital Core against Process and Passive Variations," Design, Automation, and Test in Europe (DATE), 2018.

[2] A. Singh, M. Kar, V. Chekuri, and S. Mukhopadhyay, "A Digital Low-Dropout Regulator with Auto-Tuned PID Compensator and Dynamic Gain Control for Improved Transient Performance Under Process Variations and Aging", SRC TECHCON'18.

TASK 2712.003, MULTI-MODAL BIST DESIGN AND TEST METRICS EVALUATION FOR ANALOG/RF CIRCUITS

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SIGNIFICANCE AND OBJECTIVES

This project aims at (a) designing a library of BIST blocks that can be re-designed with minimal effort, (b) developing measurement techniques that do not rely on detailed knowledge of internal BIST parameters, and (c) developing a BIST advisor toolflow for system-level BIST insertion and evaluation.

TECHNICAL APPROACH

We have divided this problem into two parallel threads. First, we have developed a library of BIST components, including a gain measurement unit, a phase mismatch measurement unit, a PRBS injection unit, a cross correlator, and a programmable OPAMP-less ADC. Second, the BIST advisor toolflow takes into account multiple BIST options and evaluates them in terms of fault coverage and hardware cost to provide viable options for the designers.

SUMMARY OF RESULTS

Two ADC architectures have been designed for the library, both based on passive sigma-delta loop, with a coarse front-end to perform the zooming function. The first ADC uses a SAR for the zooming function, while the second uses an interpolating 5b flash ADC. The second ADC, which is designed to also meet the requirements of wireless application, is shown in Figure 1. Due to the lack of OPAMPs in this design, this design is easily reconfigurable and can be scaled to a different technology node. Figure 2 shows the performance of the designed ADC (130nm node). Its performance is sufficient for several communications standards and its figure of merit matches or exceeds the performance of published works.

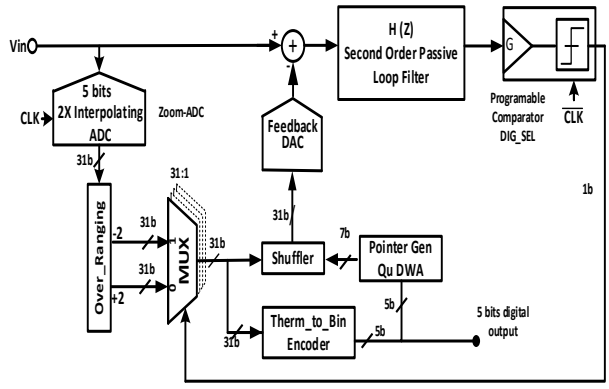

Figure 1. Hardware BIST results compared with loop analysis.

Standard	BW	fin	fs	ENOB
Edge	100kHz	10kHz	26MHz	13.4
3G	2MHz	100kHz	248MHz	12.5
LTE	5MHz	400kHz	480MHz	12
LTE	10MHz	500kHz	640MHz	10.4

Figure 2. BIST/Functional ADC performance.

The ADC can be used for test, with a higher resolution at lower frequencies.

The multi-bit feedback DAC updates every clock cycle, which relaxes the requirements on the oversampling ratio, and reduces quantization noise. Comparators are designed to provide high gain to recover the small signal swing, alleviating the low gain of the passive loop filter. Data weighted averaging is used to suppress within die variations. The zooming is enabled over an extended range to make sure that the input signal remains within the zoom range over the DNL errors of the front-end ADC.

Along with the ADC, we have developed a design flow that can be used by test engineers to scale this design with respect to different technology nodes. The motivation behind this design flow is that test engineers with little to no ADC design experience can easily retool the existing design with respect to their needs and adjust area/performance/speed trade-offs.

Keywords: analog BIST, fault simulation, analog design for test

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

[1] Ince, Mehmet, Ender Yilmaz, Jae Woong Jeong, LeRoy Winemberg, and Sule Ozev. "Evaluation of loop transfer function based dynamic testing of LDOs." In Test Conference in Asia (ITC-Asia), 2017 International, pp. 14-19. IEEE, 2017.

TASK 2712.013, RECONFIGURABLE MM-WAVE TX ARCHITECTURE AND ANTENNA INTERFACE WITH ACTIVE IMPEDANCE SYNTHESIS IN MULTI-PORT NODE-CONJUGATED COMBINER

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SIGNIFICANCE AND OBJECTIVES

The task is aimed at enabling universal transmitter architecture in silicon at mm-Wave frequencies for 5G bands (30-70 GHz) that is simultaneously back-off efficient across the frequency range and has the capability to overcome antenna impedance mismatches, and process variations.

TECHNICAL APPROACH

The method is based on a generalized model of multiple asymmetrical unit Tx-cells (mm-Wave DACs/power-mixers) interacting in a non-isolated complex network. This interaction among them results in the impedance that each cell sees is a function of the driving amplitude and phase of the other cells which can be digitally configured (through DAC architecture). This active control leads to reconfigurable on-chip complex mm-Wave impedance synthesis on the fly without any variable passives. This efficient wideband operation and high efficiencies at deep back-off across the spectrum, while being capable of countering process variations and antenna impedance mismatches

SUMMARY OF RESULTS

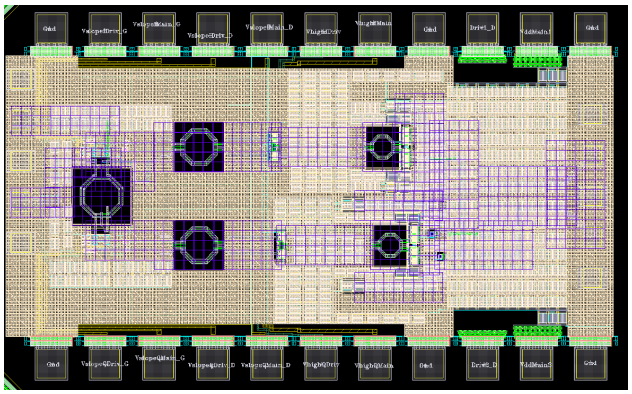

Figure 1. Layout of the multi-band VSWR tolerant and back-off efficient PA chip

The work leverages on the method proposed by the PI and his group on active impedance synthesis which demonstrated programmable load impedances resulting in reconfigurable operation across the mm-Wave range without any lossy variable passives (30-70 GHz) with record output power level and efficiency across the frequency range using a node-conjugated combiner architecture. The architecture was generalized to enable simultaneously broadband and back-of efficient operation, where the amplitude modulaton is enebaled by digital DACs. In this work, we focused in an RF-in-to RF out architecture where the architecture is an analog version of the proposed architecture and it avoids the complex polar operation (amplitude and phase separation), bandwidth expansion and synchronization issues. The PA cells are modulated through an integrated envelope detector that allows operation similar to the proposed digitial DAC-based approach. The PA operates at both bands at 28/39 GHz and has the ability to overcome load impedance mismatches upto VSWR 4:1.

Keywords: mmWave, PA, back-off efficient, wideband, load mismatch, 5G

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] RFIC workshop 5G mm-Wave Power Amplifiers, Transmitters, Beamformign Technqiues and Massive MIMO.

[2] ISSCC 2018 Forum, Circuit and System Techniques for mm-wave Multi-Antenna Systems

TASK 2712.015, AREA-EFFICIENT ON-CHIP SYSTEM-LEVEL IEC ESD PROTECTION FOR HIGH SPEED INTERFACE IC'S

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SIMON ANG, UNIVERSITY OF ARKANSAS

SIGNIFICANCE AND OBJECTIVES

Area-efficient, low-capacitance, on-chip system-level IEC ESD protection solutions for high-speed interface ICs will be designed, fabricated and characterized. Device physics for the substrate parasitic PNP structure in p^+/n-well diodes will be modeled. Novel designs of IEC ESD structures will be provided for cost-effective system-level ESD protections on high-speed interface ICs.

TECHNICAL APPROACH

To reduce the total ESD device areas and reduce the parasitic capacitance, our approach is to utilize the inherent parasitic PNP structure in the high-side ESD diode as a parallel path to shunt the ESD discharge current. The key for this approach is to understand and adjust the characteristics of substrate PNP structures, such that the triggering and ESD clamping voltage of parasitic PNP structure is within the specific ESD protection window. Meanwhile, the clamping voltage of the primary ESD protection path needs to be higher than the triggering voltage of the parasitic PNP device.

SUMMARY OF RESULTS

The ESD characteristics of the bipolar devices has been studied to understand the relationship between device geometry and triggering/holding voltage. For parasitic PNP inside the p^+/n-well diode, the triggering voltage of the parasitic PNP is mainly decided by the avalanche breakdown between collector and base, which is due to the impact ionization process. The doping concentration of the collector and base region will strongly affect the triggering of the PNP. The holding voltage of parasitic PNP are decided by the current gain of the device and the avalanche multiplication factor.

For the proposed p^+/n-well ESD protection solutions based on Figure 1, device TCAD simulations have been performed.

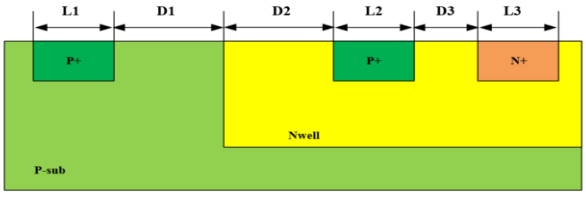

Figure 1. TCAD simulations based on the p+/n-well ESD diode.

Figure 2 shows one simlution result in which parameter D2 (Fig. 1) has a significant impact on the triggering voltage of parasitic PNP. Detailed simlutions based on different D2 parameters are shown in Figure 2. The TCAD simulation results show that triggering voltage changes more rapidly with D2 than D1, L1, L2. Besides the basic structure of Figure 1, other design structures are proposed and simulated, for example, adding n^+ floating region to the right side of p^+ diffusion in the p-substrate or n^+ bridging between p-substrate and n-well.

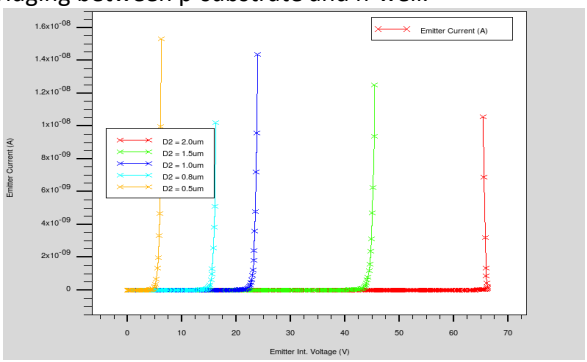

Figure 2. The effect of D2 on the triggering of the parasitic PNP.

The tapeout of proposed ESD test structures using UMC 65nm process has been submited, and the modules are designed with different parameters as shown in Table 1 ("others" represents structures with floating n^+ or p^+ region). Total 42 device structures are designed.

Table 1. Modules of the tapeout.

Modules	1	2	3	4	5
Parameters	D1	D2	L1,L2	Width of diffusion	Others

One Ph.D. student (Hui Wang) was hired by at Texas Instrument as an intern this summer. Hui will conduct TLP characterizations, TCAD simulations and design optimizations on various componoents and ESD protection cells at room and elevated temperatures.

Keywords: ESD, PNP, parasitic, IEC, TCAD

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Z. Chen, F. Farbiz, Area-efficient IEC ESD protection for high speed integrated circuits, patent pending.
[2] Z. Chen, R. Sankaralingam and G. Boselli, Study of Voltage Overshooting of Gate-Coupled Silicon Controlled Rectifier on HBM Protection, 40th Annual EOS/ESD Symposium, Reno NV, Sept. 2018, Accepted.

TASK 2712.017, MITIGATING RELIABILITY ISSUES IN ANALOG CIRCUITS

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SIGNIFICANCE AND OBJECTIVES

There have been growing interest towards building aging simulation frameworks for circuits where the stress condition itself varies as the circuit ages [1,2]. We propose an iterative simulation method that can estimate the power law exponent more accurately.

TECHNICAL APPROACH

An array-based test structure (Fig. 1), representative specifically in context of biasing circuits was implemented with the aim of understanding the impact of feedback on aging dynamics. The aim is to (1) characterize the impact of feedback on aging rate and compare it to the no-feedback case & (2) evaluate the efficacy of iterative simulations / compact modeling approaches for lifetime projection and compare it with method based on Universality of Hot-Carrier degradation [3].

SUMMARY OF RESULTS

Fig. 2 illustrates the impact of feedback on aging rate by comparing the experimentally obtained values of Vth degradation for different values of applied stress bias for the no-feedback case (const. voltage) and for the case when the DUT is in feedback (const. current). As can be seen clearly, in feedback the DUT experiences a faster initial aging rate which saturates overtime in accordance with the Bond Dispersion model.

Using an iterative methodology for lifetime prediction for feedback in conjunction with a constant power law model as shown in Fig. 3 leads to gross overestimations at longer times and at higher degradation levels.

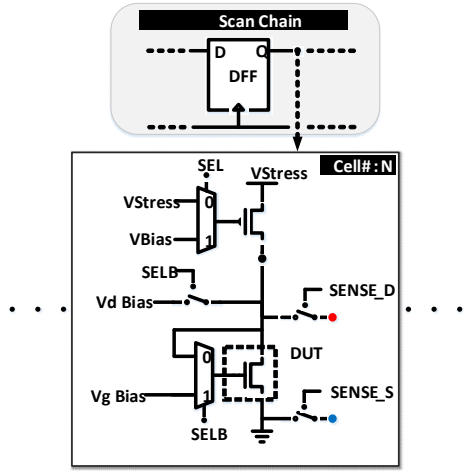

Figure 1. Overview of proposed array based test structure.

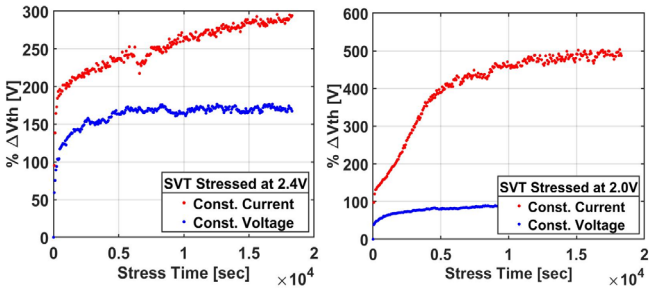

Figure 2. Measured Vth voltage degradation vs. time.

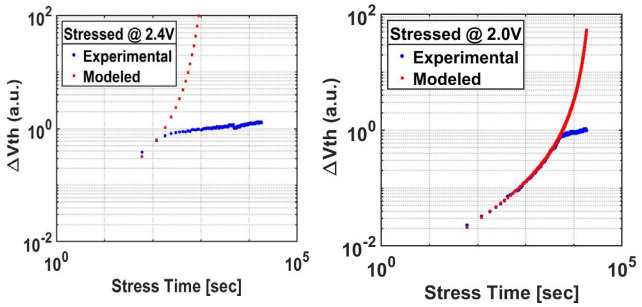

Figure 3. Estimated degradation in Vth using an iterative simulation based approach.

However, the method of lifetime prediction using universality of hot carrier injection provides useful insight in scenarios like this, since now only a few short term measurements are needed to extrapolate the degradation at nominal / sub-nominal voltages (Fig. 4).

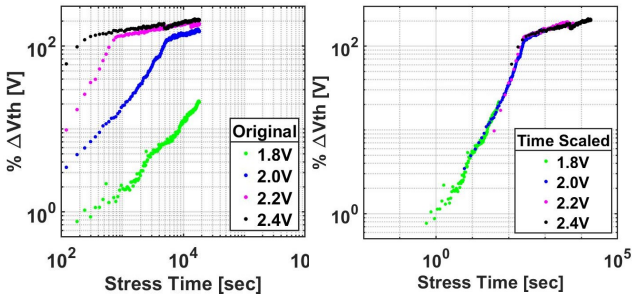

Figure 4. Shape of the Universal curve extrapolated from a few short term measurements for the DUT in feedback.

Keywords: analog circuit reliability, bond-dispersion model, hot carrier injection, universality of degradation

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

TASK 2712.018, TEST TECHNIQUES TO APPROACH SEVERAL DEFECT-PER-BILLION FOR POWER IC'S

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SIGNIFICANCE AND OBJECTIVES

Existing power IC test techniques examine and model chip performance through external terminals. This work will simulate, design and test power IC subcircuits using additional bare-die test points to reduce part failure rates. The goal is test yield enhancement by culling power ICs with outlier subcircuit performance.

TECHNICAL APPROACH

Task researchers will demonstrate the use of internal IC test points to determine subcircuit performance inside of generic LDOs and Buck Converters. The test points are placed either in the wafer scribe lanes or at internal IC test pads. Bare-die power IC probing will allow the measurement of DC, small-signal response and precise control of low and high temperature wafer measurements. Analyses, simulations and measurements of custom-designed LDO and Buck Converters will be performed in order to prove these new test concepts. A 65nm CMOS LDO test IC has been sent for fabrication.

SUMMARY OF RESULTS

Existing test and modeling methodologies for LDO ICs characterize three external nodes (V_{in}, V_{load} and GND). In this work, the researchers have developed generic LDO designs with PFET (p-type FET) or NFET (n-type FET) pass transistors. Researchers performed simulations of these generic LDO designs with internal probe points. This work demonstrated ways of injecting signals and overcoming the high control loop gain in the LDO in order to do individual subcircuit characterization. Investigations showed that operating a PFET LDO at V_{Input} voltages near but below LDO dropout the gain of the feedback loop is significantly weakened and this can place the PFET pass transistor into triode mode while keeping the Error Amplifier working. The simulated probe points could be used to find, 1) differential circuit imbalances in the LDO error amplifier, 2) PFET and NFET pass transistor weaknesses, 3) integrated resistor and capacitor values at the edge of process tolerances, 4) charge-pump circuit's output voltage and 5) Bandgap Reference voltage.

The researchers have designed a generic LDO for characterization and fault modeling in a 65 nm CMOS process. In the IC, there is an error amplifier (which compares the reference voltage and scaled down output voltage), a Bandgap reference (BGR), pass transistor (output driver), feedback resistances and compensation capacitances as shown in Figure 1. In the 65nm CMOS LDO, a buffer and a transmission gate are added at the output of the Error Amplifier and Bandgap Reference in order to read, more accurately, those voltages out of the chip during testing. The functionality of the LDO system as a whole and its individual subcircuits were simulated. There was a dropout voltage of 140mV at load current of 200mA with a 1.6V output voltage. Simulations of dropout characteristics and the multi-fingered PMOS pass transistor performance at high temperatures show the greatest variations. Simulations in 65nm CMOS were performed using a multi-fingered PFET LDO modeled in dropout. Reduced numbers of fingers modeled a weak PFET with inactive or partially active fingers or high V_{th} fingers.

Providing tests for LDO subcircuit response opens several ways to improve yield. There is potential to cull LDOs prone to failure by finding outlier performance inside the subcircuits. In addition, a statistical database for LDO subcircuit response could be measured to form a basis to determine weak subcircuits and acceptable subcircuits. Pre-determined weak LDO subcircuits could be tested after accelerated aging and harsh usage conditions to demonstrate the critical failure and yield issues.

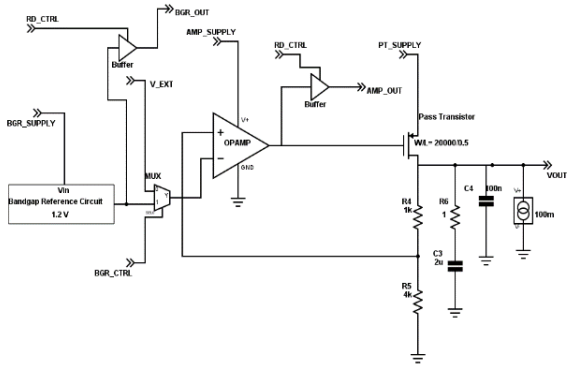

Figure 1. Block diagram of the 65nm CMOS LDO Design.

Keywords: test, analog, power, LDO, buck converter

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] A. Tulsiram et al., "Development of LDO Testing and Fault Detection for Ultra Low Defects," 2018 NATW'18, May 2018, Essex, VT.

TASK 2712.019, PRE-COMPUTED SECURITY PROTOCOLS FOR ENERGY HARVESTED IOT

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SIGNIFICANCE AND OBJECTIVES

We optimize the latency and energy-efficiency of Internet security protocols in energy-harvesting IoT. An energy-harvesting IoT device has limited and leaky energy-storage capacity. The energy must be used as soon as possible. With pre-computing techniques, cryptographic applications can instantly use the harvested energy. We demonstrate precomputed random-number generation and cryptographic key-exchange.

TECHNICAL APPROACH

The feasibility and efficiency of the proposed techniques will be evaluated through an end-to-end demonstrator with an energy-efficient micro-controller and with a wireless communications front-end. We develop techniques to spread out computations over time by reformulating cryptographic algorithms as capable of generating coupons, which are precomputed portions of the algorithm. We propose techniques for coupon generation and their secure storage in non-volatile, possibly off-chip memories. We also consider and optimize the impact of precomputed security protocols on the communication cost and the storage cost. We validate the proposed approach by constructing a prototype implementation on an energy-harvesting oriented microcontroller-based platform.

SUMMARY OF RESULTS

We studied two canonical cryptographic applications: true random number generation and bulk-encryption. Our solutions avoid energy waste during the offline phase, and they offer gains in energy efficiency during the online phase of up to 28 times for bulk-encryption and over 100 times for random number generation [1]. The transformation of energy to coupons for future use allows us to exploit the improved data storage capacity of modern energy harvesting systems and improve the runtime performance of our cryptographic operations. Figure 1 highlights the potential to improve the performance of an energy harvested device in completed operations per second.

We analyze the precomputed implementations on an MSP430 with ferroelectric RAM and an ARM Cortex M4 with nonvolatile flash memory. For bulk encryption, we studied the application of AES in counter mode (AES-CTR). In AES-CTR mode, the actual block cipher operation is independent of the input message, making it a good candidate for parallelizing the encryption/decryption process.

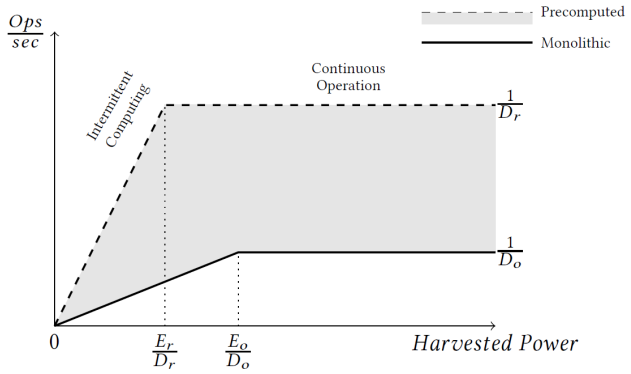

Figure 1. Operations per second as a function of Energy influx into the system. When coupons are available the device is able to execute more operations within a given time period.

Table 1. Improvements in AES-CTR with precomputation

Device	Test case	$\frac{C_o}{C_r}$	$\frac{E_o}{E_r}$	$\frac{D_o}{D_r}$	$\frac{EDP_o}{EDP_r}$
MSP432	SW T-box	5.4	5.4	5.5	29.8
	SW S-box	27.5	27.8	28.4	791.3
	HW	3.2	3.2	3.3	10.5
MSP430	SW S-box	22.3	28.1	26.3	737.7
	HW	1.9	2.1	2.0	4.0

Table 1 compares the operation of AES-CTR in monolithic mode (Figure 1, dashed line) and in precomputed mode (Figure 1, solid line). We use different implementations of AES-CTR, both with and without hardware acceleration. In all cases, there is a large improvement in runtime latency, energy requirement and security in AES-CTR mode when OTPs are precomputed.

Our current research efforts focus on secure storage of tokens in non-voltaile memory.

Keywords: pre-computation, cryptography, energy-harvesting, MSP430, NVM applications

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] C. Suslowicz, A. S. Krishnan, P. Schaumont, "Optimizing Cryptography in Energy Harvesting Applications," ASHES@CCS 2017: 17-26.

TASK 2712.021, DISTRIBUTED SILICON CIRCUITS AND SENSORS IN 3D-PRINTED SYSTEMS FOR WEARABLE IOT SENSORS

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SIGNIFICANCE AND OBJECTIVES

There is an emerging set of applications that require stretchable and compliant electronics – including wearable devices, instrumented fabrics, and soft robots with distributed sensors and computation. In this project, we are working to demonstrate a fundamentally new method for the fabrication of stretchable 3D-printed objects containing distributed sensors and silicon ICs.

TECHNICAL APPROACH

Developing stretchable electronics faces two primary challenges: integration of active semiconductor devices in elastic substrates, and providing stretchable and conductive interconnects. In this project, we combine 3D printing of liquid metal materials and silicone rubber with PCB fabrication techniques to build solid 3D objects with electronic components distributed throughout. Silicon integrated circuits, used for computation, sensing, and actuation, will be connected through liquid metal conductors confined to 3D microfluidic channels. Through additive, layer-by-layer construction, electronic devices can be inserted and connected throughout the 3D structure. We will also develop compact models for the interconnects, which will be used to design adaptable front-end circuits for stretchable interconnect interfaces.

SUMMARY OF RESULTS

In the previous project year (Year 1), we have demonstrated progress in materials, fabrication, and system-level aspects of the proposed approach. In November 2017, we reported results of ongoing investigations of liquid metal paste formulations, and we demonstrated the use of modified liquid metal materials with gel-like properties to enable 3D printing of self-supporting liquid metal structures, interconnects, and electrical vias. Specific outcomes included:

- Optimized process for formulating liquid metal paste with rheological modification and nickel particle filling for 3D printing
- Demonstrated 3D printing of self-supporting mm-scale structures using liquid metal paste
- Characterized printed liquid metal conductors for resistance change under strain and repeated dynamic stretch

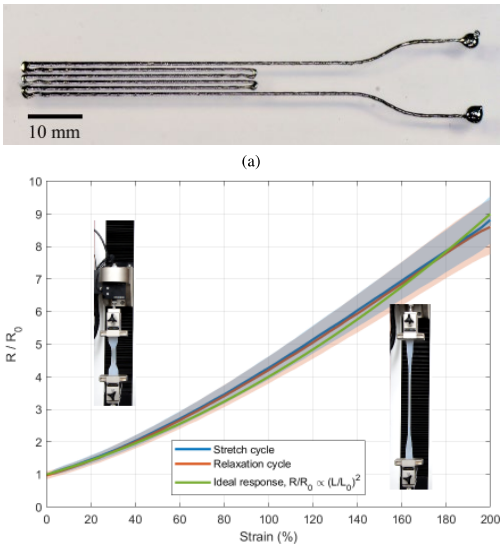

Figure 1. Printed liquid metal paste encapsulated in silicone elastomer demonstrating conductivity from 0-200% strain.

More recently, in May 2018, we have reported results on prototype fabrication using 3D-printed liquid metal paste to form interconnects among active and passive discrete electronic components. An example printed conductor is shown in Fig. 1, along with measured resistance vs. strain data for a stretchable strain sensor.

In addition, a multi-component stretchable relaxation oscillator was demonstrated, as was a 3D-printed strain sensor with in-device computation and digital interface. These prototypes demonstrate interconnection of multiple ICs, along with passive components, in which both power, analog signal, and digital signal lines are implemented using stretchable liquid metal links embedded in a elastomer substrate.

In the next project period, we will focus on further printing and circuit fabrication improvements, in parallel with development of static and dynamic models of stretchable liquid metal interconnects.

Keywords: stretchable electronics, 3D printing, wearable devices, packaging, sensor interfaces

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

TASK 2712.022, INTRINSIC IDENTIFIERS FOR DATABASE-FREE REMOTE AUTHENTICATION OF IOT EDGE DEVICES

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AMIT RANJAN TRIVEDI, UNIVERSITY OF ILLINOIS, CHICAGO

SIGNIFICANCE AND OBJECTIVES

Counterfiet ICs are critical in biomedical, defense applications. PUF based techniques require dedicated resources for authentication of ICs. FEOL (front end of line) components based intrinsic authentication overcomes the short-comings of the PUF based techniques, by exploiting the discrepancies in hardware blocks invariably present in ICs. BEOL (back end of line) componenets based authentication is also being explored.

TECHNICAL APPROACH

Process variations in BEOL componenets such as capacitors can be exploited for authentication purposes. MOM capacitors exhibit a high degree of correlation between process variation and process parameters, thus, can be utilized for watermarking purpose. Capacitors form intergral componenets in ADC architectures (SAR, Delta-Sigma, Pipeline) and MOM capacitors are the preferred architecture due to resource effective reasons. SAR ADC architecture is most widely employed in Medium-High resolution, moderate speed and low power applications. A capacitive DAC is the most important block of SAR ADC and CDAC consists of large number of unit capacitor elements. Therefore, SAR ADC can be used for authentication purposes with few modifications.

SUMMARY OF RESULTS

In the proposed scheme, intrinsic authentication is performed by characterizing process variation BEOL capacitors. BEOL capacitors are less affected by temperature and aging induced variations, thus, improving the reliability of the authentication process. Further, conventional SAR ADC architecture has been modified to facilitate authentication signature extraction using unit elements in CDAC, alleviating the resource overhead. Moreover, proposed scheme does not require large database for storing authentication information.

Figure 1 shows the modified SAR ADC architecture operating in the authentication mode. From the figure, it can be observed that the MSB capacitance in the CDAC array has been modified to incorporate provision to access each unit element. In addition to the above, capacitance ΔC_U will be used during the authentication process.

While in the normal mode of operation, unit capacitances of the MSB block are connected to form a single capacitance and hence, allow for normal conversion process. In the authentication phase, ΔC_U is connected to either positive or negative terminal of the comparator using the switch arrangements. Value of ΔC_U can be programmed based on the requirement.

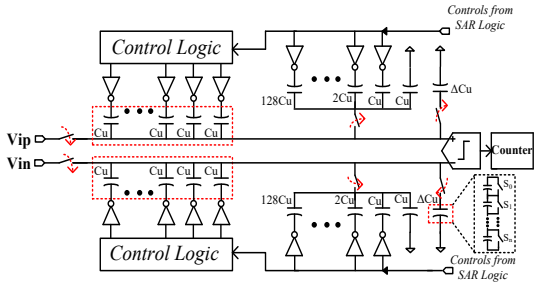

Figure 1. Modified SAR ADC architecture for extraction of authentication signature.

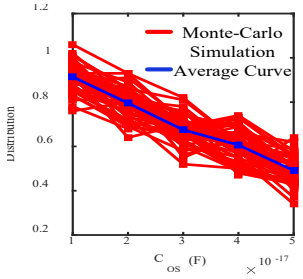

Figure 2. Distribution obtained while operating in the authentication mode.

Now, one unit capacitance connected to each of the comparator inputs is considered and their bottom plates are connected to V_{DD} along with the bottom plate of ΔC_U. With this, there will voltage developed at comparator inputs. Counter output is increased if $V_+ > V_-$ (when ΔC_U is connected to negative input) and vice versa. After completing this process for all the unit capacitances in the MSB array, the procedure is repeated to obtain the distribution in Fig. 2 that can be used for authentication.

Keywords: SAR ADC, MOM capacitor, database-free, intrinsic authentication

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] Ahish Shylendra et al., "Intrinsic and Database-free Watermarking in ICs by Exploiting Process and Design Dependent Variability in Metal-Oxide-Metal Capacitances," accepted to ISLPED, 2018.

TASK 2712.026, FAULT CHARACTERIZATION AND DEGRADATION MONITORING OF SIC DEVICES

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SIGNIFICANCE AND OBJECTIVES

Silicon carbide (SiC) power MOSFETs are becoming more popular in high-voltage, high-frequency, and high-temperature applications. However, limited field data are available regarding the long-term reliability of discrete SiC MOSFETs. In this study, an accelerated DC power cycling test setup is designed to age the devices, and the variation of the electrical parameters throughout the degradation is studied to find suitable aging precursors for the state-of-art discrete SiC power MOSFETs.

TECHNICAL APPROACH

An aging setup is developed first to degrade the SiC devices through power cycling tests. The diagram of the test setup is illustrated in Fig. 1. The device under test (DUT) is heated up through the current source of the power supply and then cooled down when the power supply is turned off. The temperature swing is actively controlled during the aging process.

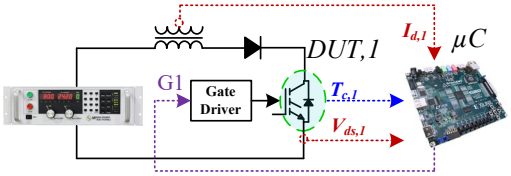

Fig. 1. Accelerated aging setup for SiC devices.

The aging process is interrupted after 200 power cycles, and a curve tracer is used to analyze the static parameter shifts of the devices. Meanwhile, at the room temperature, a double-pulse test setup together with the detection circuit is implemented to evaluate the switching transient variation of the device throughout the degradation process. Utilizing the high-resolution capture module of an MCU, the detection circuit is able to monitor the device's turn-on time during the switching transient with an accuracy of 300 ps.

SUMMARY OF RESULTS

The static parameter variation of the Gen-II SiC devices from Wolfspeed is monitored under a temperature swing from 30 °C to 200 °C. As shown in Fig. 2(a), the threshold voltage is increased for all the DUTs. This variation is mainly because of the gate oxide degradation during the aging process. Meanwhile, an increase of on-resistance is observed as illustrated in Fig. 2(b). The threshold voltage shift is the main cause of this $R_{ds,on}$ increase.

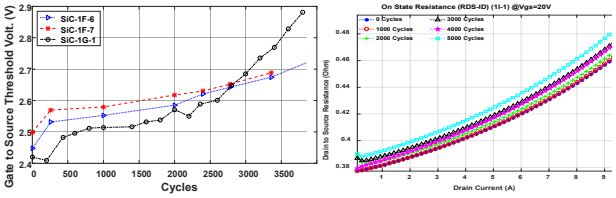

Fig. 2. (a) Threshold voltage variation over aging cycles (b) On-resistance ($V_{gs} = 20$ V) variation over aging cycles.

Besides the static parameter variation, the device's switching transient is also changed over the degradation process. In this study, the turn-on time of the SiC devices at room temperature is compared at different aging intervals. Fig. 3(a) shows the experimental turn-on voltage waveforms at different aging cycles. As can be seen, the turn-on time of all DUTs is changed as the devices are aged. Specifically, the turn-on time goes up because of the threshold voltage increase as summarized in Fig. 3(b).

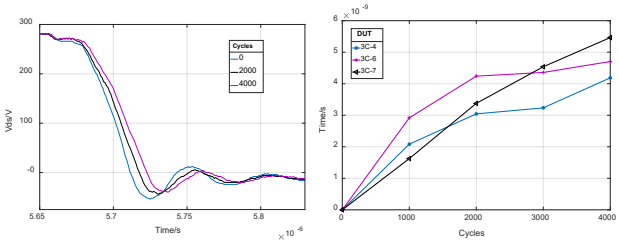

Fig. 3. Switching transient variation over aging for SiC devices. (a) Turn-on voltage waveform (b) Turn-on time variation

Based on the previous fault characterization, the threshold voltage, on-resistance and turn-on time can be used for SiC device aging precursors.

Keywords: power cycling, SiC device, aging precursor

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] E. Ugur and B. Akin, "Aging assessment of SiC FETs under high temperature cycling tests," IEEE ECCE, 2017.
[2] S. Pu, E. Ugur, B. Akin and H. Akca, "Investigation of EM radiation changes in SiC based converters throughout device aging," IEEE WiPDA, NM, pp. 190-194, 2017.
[3] S. Pu, E. Ugur and B. Akin, "Real-time degradation monitoring of SiC-MOSFETs through readily available system microcontroller," IEEE WiPDA, NM, pp. 378-382, 2017.

TASK 2712.029, NOVEL SUPER-RESOLUTION AND MIMO TECHNIQUES FOR AUTOMOTIVE AND EMERGING RADAR APPLICATIONS

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SIGNIFICANCE AND OBJECTIVES

Millimeter-wave (mmWave) imaging technology is one of the fastest growing technologies of this decade with a wide range of applications including medical, automotive radars, and security screening. In the past year, a X-Y imaging system utilizing commercially available 77 GHz radar sensors and high-speed mechanical scanner has been developed and tested.

TECHNICAL APPROACH

Millimeter-wave imaging techniques involve collecting the reflected wave data from targets in distinct dimensions. We develop novel image reconstruction algorithms, inspired by the synthetic aperture radar (SAR) signal processing techniques used in remote sensing/surface mapping. In particular, we show 2D mmWave imaging using wideband (FMCW) mmWave sources. Our prototype system is described along with various imaging results.

SUMMARY OF RESULTS

Imaging of a two dimensional object requires reflected wave data to be collected across two distinct dimensions. In this project, we propose a reconstruction method that uses FMCW waveforms along with two dimensional scanning. The image reconstruction technique uses inverse Fourier transform along with amplitude and phase correction factors. In addition, this reconstruction technique does not require interpolation of the data in either wavenumber or spatial domain.

The reflected wave data are collected by putting only one transmitting and one receiving antenna in action at a given time. Assume that transmitting and receiving antennas are located very close to each other, then they can be represented by the mid-point between them. A target image is characterized by a reflectivity function $f(x,y,z_0)$. Then, the total received reflected wave data from the target located at z_0 distance away from the radar is given by,

$$r(x',y') = \iint f(x,y,z_0) e^{-j2k\sqrt{(x-x')^2+(y-y')^2+z_0^2}}\, dxdy$$

where $k = 2\pi f/c$ is the wavenumber. We can obtain $f(x,y,z_0)$ by a matched filter. However, the computational complexity will be high. Thus, we decompose the spherical wave into a superposition of plane-wave components:

$$\frac{e^{-j2kR}}{R} = \frac{1}{2\pi}\iint \frac{e^{jk_x'(x'-x)+jk_y'(y'-y)+jk_z z_0}}{k_z} dk_{x'} dk_{y'}$$

Then, using 2D DFTs, we can establish the computationally efficient image reconstruction as

$$f(x,y) = \mathrm{IFFT}_{2\mathrm{D}}\{A(\zeta)\mathrm{FFT}_{2\mathrm{D}}\{r(x,y)\}\}$$

where $A(\zeta) = \Pi(\zeta)\sqrt{\zeta}e^{-jz_0\sqrt{\zeta}}$ combines the amplitude and phase correction factors. Figures 1 shows the X-Y imaging system utilizing commercially available 77 GHz radar sensors and a high-speed mechanical scanner along with the measured point spread function. Figure 2 shows an example of reconstructed image for a given M-shape target.

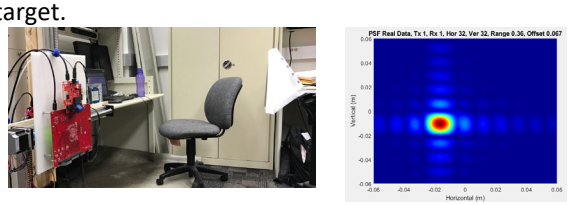

Figure 1. Left: The corner reflector is placed 30cm away from the SAR scanner. Right: The image of the corner reflector which can be viewed as an emprical point spread function of the imaging system.

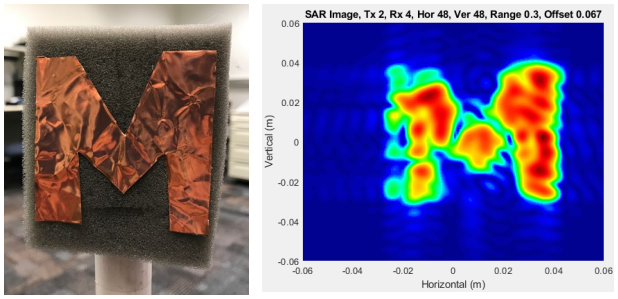

Figure 2. Left: M-shape target image is made out of copper tape. Right: Reconstructed image.

Keywords: mm-Wave radar, FMCW, SAR imaging, image reconstruction, X-Y scanner

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] M. E. Yanik and M. Torlak, "mm-Wave Imaging with Two-Dimensional SAR Data", Accepted to SRC Techcon, Sept. 2018, Austin, TX.

TASK 2712.030, PERFORMANCE OF CARBON DIOXIDE (CO_2) GAS SENSORS

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SIGNIFICANCE AND OBJECTIVES

Electrochemical impedance spectroscopy (EIS) is utilized to characterize the impedance changes occurring at the electrode-RTIL (Room Temperature Ionic Liquid) interface on exposure to CO_2 under varying humidity and temperature conditions. The objectives achieved are (1) Investigate the impact of electrochemical window (ECW) voltages, and (2) Investigate the adsorption and desorption dynamics of CO_2.

TECHNICAL APPROACH

A custom closed environmental test system consisting of a gas mixer was developed wherein the RTILs were exposed to varying CO_2 concentrations, humidity, and temperatures. Using electrochemical impedance spectroscopy, the impedance is measured utilizing a small 100mV-AC perturbation applied to a DC offset. For the adsorption and desorption studies, the test chamber was initially incubated with N_2 at the required humidity and temperature conditions (Fig. 1). The RTILs were subjected to elevated temperatures in the absence of humidity and the EIS responses to varying CO_2 concentrations were recorded to understand the behavior of the sensor.

SUMMARY OF RESULTS

It is important to understand the effects of voltage bias on the performance of RTILs for CO_2 sensing to achieve maximum signal response. As RTILs have wide ECW, operating at higher voltage bias would allow the RTIL moieties to stretch further allowing more CO_2 molecules to dock in the interstices. The key takeaways are: (1) operating at the edge of the ECW yields higher CO_2 response, (2) among the 3 RTILs EMIM[TF_2N] performs the best with no trend reversals when operated at the edge of the ECW followed by MMIM[$MeSO_4$], and (3) EMIM[FAP] showed a negative sensitivity slope for CO_2 as opposed to the other two RTILs which showed a positive sensitivity.

The capability of the RTILs to desorb the absorbed CO_2 naturally without the application of external stimulus is of interest to understand the rate of dynamic adsorption and physidesoprtion. Fig 2. shows the dynamic impedance adsorption and desorption response of 1000ppm CO_2 at 25%RH/25°C in MMIM[$MeSO_4$] and EMIM[TF_2N] over 3 cycles. A time period of Δ= 4mintues is applied between N_2 and CO_2 cycles to allow for the stabilization of the sensor response. The key findings of this study are: (1) switching voltage bias from ON and OFF is required to relax EDL and assist in physidesorption, (2) dynamic desorption is slow, and (3) acceleration of desorption through an external mechanism is needed.

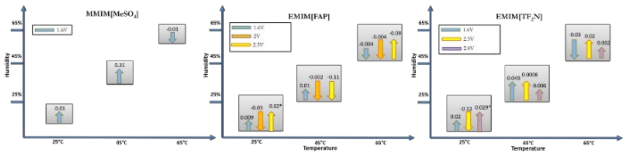

Figure 1. Humidity and temperature sensitivity of MMIM[MeSO4], EMIM[FAP] and EMIM[TF2N] for varying temperature and humidity conditions across ECW .

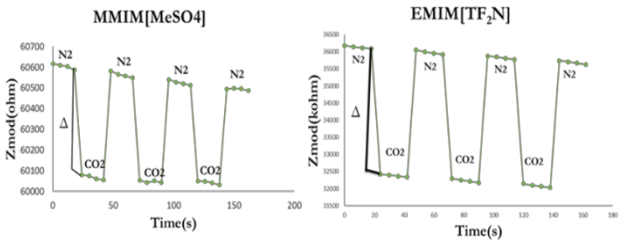

Figure 2. Dynamic impedance adsorption and desorption response of 1000ppm CO2 at 25%RH/25°C in MMIM[MeSO4] and EMIM[TF2N].

Keywords: Electrochemical Impedance spectroscopy, Chronoamperometry, CO_2 sensing, humidity, temperature

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] E. Graef, B. Jagannath, R. Munje, S. Prasad. "Fluorinated Anionic Room Temperature Ionic Liquid based CO_2 Electrochemical Sensing," IEEE Sensors Journal. PP. 1-1. 10.1109/JSEN.2018.2816901, 2018.

[2] A. Bhide, B. Jagannath, E. Graef, S. Prasad, "A Robust Electrochemical Humidity Sensor for the Detection of Relative Humidity Using Room Temperature Ionic Liquid (RTIL) for Integration in Semiconductor IC's," ECS Journal of Solid State Science and Technology. 7. Q3043-Q3048. 10.1149/2.0091807, 2018

TASK 2810.002, SECURITY-AWARE DYNAMIC POWER MANAGEMENT FOR SYSTEM-ON-CHIPS

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SIGNIFICANCE AND OBJECTIVES

The proposed research investigates the energy-security trade-offs associated with Dynamic Power Management (DPM). The proposed effort will develop methodology to characterize security implications of DPM in SoCs and design circuit/system techniques to co-optimize security and energy-efficiency of DPM.

TECHNICAL APPROACH

This effort will purse a cross-layer approach to understand the energy-security trade-offs in Dynamic Voltage Frequency Scaling (DVFS). First, we will design power domains that are secure against power-/EM- side-channel analysis by leveraging the distributed integrated voltage regulators. Next we will investigate energy-security trade-off at the chip level by focusing on the DVFS controller and algorithm. Finally we will explore an integrated approach considering secure power domains and secure DVFS controllers.

SUMMARY OF RESULTS

Dynamic power management (DPM) is an integral part of modern SoC which utilizes combined hardware and software approach for energy efficiency. Techniques like dynamic frequency and voltage scaling (DVFS) play crucial role in balancing power and performance of battery powered smartphone devices. In the past, information leakage from side-channels on processors have been exploited to profile instructions, learn program control flow or recover programs, and more recently to identify anomalies and malicious code. But, leveraging information using these techniques requires physical access to devices, expensive acquisition setups, additional pre-processing steps. In this work, we have depicted that fine-grained DVFS control generates a vulnerability wherein, aggressive frequency scaling patterns give indication about core activity, which is a potential information leak, thereby compromising security. The advantage of this attack lies in its simplicity and low cost. The attacker only injects shellcode and poll DVFS states. This dependency has been exploited in our work to identify apps running on a mobile processor. We have explored several supervised learning techniques to classify ARMv8 processor benchmarking application on an Android device (Snapdragon 820 Quad core processor). We used both techniques, DVFS states and EM side channel emanations to develop features. In our key findings, we demonstrate the simplicity of attack, measure the distinctness through classification accuracy, and compare the effectiveness of two techniques

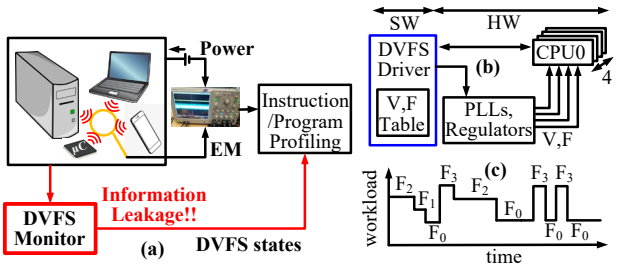

Figure 1. (a) Dynamic voltage frequency scaling algorithms can be a critical side channel for analyzing program behavior, (b) hardware/software approach for power management in modern SoCs, and (c) dynamic management of frequency (and voltage) under varying workloads for a quad-core system

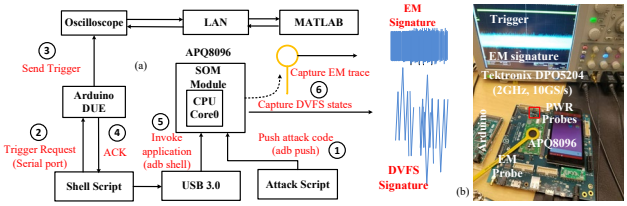

Figure 2. (a) Measurement Setup details to capture DVFS and EM-signature (b) Open-Q APQ8096 System-on-Module development platform for characterization.

Keywords: secure, side-channel, dynamic power management, integrated voltage regulator, dynamic voltage frequency scaling

INDUSTRY INTERACTIONS

Intel, IBM

MAJOR PAPERS/PATENTS

TASK 2810.005, CIRCUIT DESIGN FOR ESD AND SUPPLY NOISE MITIGATION

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SIGNIFICANCE AND OBJECTIVES

This project seeks to develop (1) IC-level power distribution networks that promote power integrity even in the presence of power-on ESD, and (2) biasing strategies for IO circuits that boost ESD resilience, thereby enabling high-speed IO circuits to meet both performance requirements and ESD target levels.

TECHNICAL APPROACH

The PI's research group will leverage its past work on modeling and simulation of IC response to ESD (Figure 1) to identify reliability hazards and evaluate solutions. The investigations will focus on integrated voltage regulators, rail clamp circuits, and high-speed IO. Promising solutions will be implemented in silicon. Additionally, the group will continue to develop on-chip noise sensors that are most sensitive to ESD-induced noise. Experiments will be performed to establish whether ESD noise can be distinguished from other disturbances (e.g., supply brown out, simultaneous switching noise) or a bonafide reset signal. Such sensors would aid in mitigation of ESD-induced soft failures.

SUMMARY OF RESULTS

This is a recently started project and there are no substantive results to report.

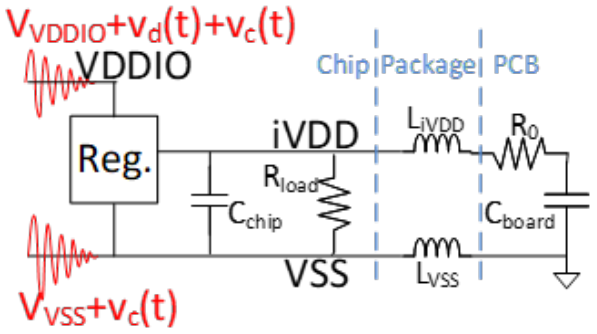

Figure 1. ESD current injected at an IO pin will return to the board via the supply and ground nets. Supply noise results, with its amplitude and frequency content being a function of the package inductance and the chararacteristics of the on-chip rail clamp circuit. The figure illustrates the noise analysis for an IC with an externally-generated HV supply (VDDIO) and internally-generated LV supply (iVDD). R_0 is the ESR of the board-level decap. L_0 represents the sum of the package-level inductance on iVDD and the ESL of the board-level decap. The regulator rejects the differential-mode noise v_d. The common-mode noise v_c is problematic unless $Z_{off\text{-}chip}$ is very large; this is achieved by not connecting iVDD to any package pins, which is suitable only if the LDO is stable without an off-chip decap.

Keywords: ESD, latch-up, integrated voltage regulator, simultaneous switching noise, rail clamp

INDUSTRY INTERACTIONS

Texas Instruments, Intel, NXP

MAJOR PAPERS/PATENTS

TASK 2810.013, FREQUENCY-DOMAIN ADC-BASED SERIAL LINK RECEIVER ARCHITECTURES FOR 100+GB/S SERIAL LINKS

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SEBASTIAN HOYOS, TEXAS A&M UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

Clock jitter places fundamental performance limitations on common time-interleaved ADC architectures, necessitating clock generation and distribution circuitry that achieve rms jitter of a few hundred femtoseconds. The ADC-based high-speed serial link design techniques in this proposal aim to improve jitter robustness and reduce ADC resolution and digital equalization complexity.

TECHNICAL APPROACH

A new configurable frequency-domain ADC-based receiver serial link architecture is in development that is capable of providing jitter robustness for baseband and coherent multi-tone modulation applications. The receiver utilizes ADCs with novel techniques to improve the configurable SAR sub-ADC speed and efficiency, including a design that utilizes reference pre-emphasis to enhance DAC settling and low-overhead reconfiguration logic to enable per-channel operation with a scalable resolution. Efficient digital reconstruction, equalization, and inter-channel interference filters for symbol detection are also in development.

SUMMARY OF RESULTS

Figure 1 shows the proposed frequency-domain ADC-based receiver. The input CTLE drives the front-end channels that have a mixer for down-conversion, a Bessel low-pass filter, and an ADC for sampling and digitization. These digitized samples are then processed by the FIR filters in the DSP and their outputs are combined to either perform symbol estimation in PAM-4 baseband mode or to perform both inter-channel interference (ICI) and ISI cancellation in multi-tone mode. This architecture

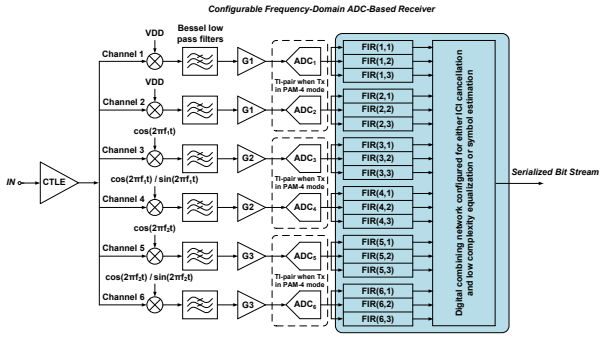

Figure 1. Configurable frequency-domain ADC-based receiver.

provides several benefits. First, the mixers perform self-equalization and provide some channel loss compensation, allowing for a reduction in digital equalization complexity. Second, high-frequency noise introduced by the mixers and CTLE is attenuated by the channel filters. Finally, the inclusion of digital receive-side ICI cancellation filters in the proposed 128Gb/s system allows for a 50% improvement in relative channel spacing when compared to a previous 10Gb/s implementation.

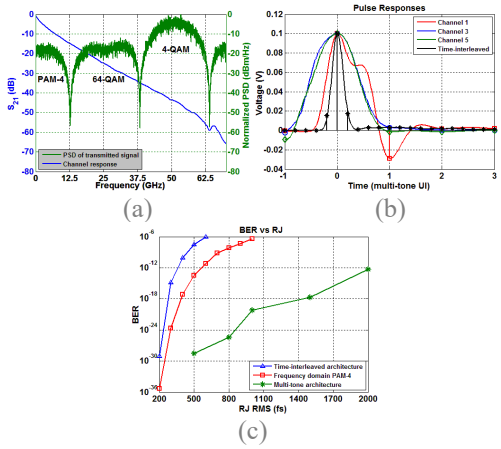

Figure 2. (a) 128Gb/s partitioning in 5-channel multi-tone mode. (b) 128Gb/s system pulse responses. (c) BER vs RJ.

Figure 2 shows a potential 128Gb/s multi-tone implementation implemented with 5 12.8GS/s channels consisting of baseband PAM4, QAM64 centered at 25.6GHz, and QAM4 centered at 51.2GHz. An intuitive visualization of the relative jitter robustness of the proposed architecture is shown in the pulse responses from a conventional time-interleaved system and the proposed frequency-domain architecture operating in multi-tone mode over a channel with over 30dB loss at 32GHz. Assuming an equal amount of RJ on both the ADC samplers and the mixer LO clocks, the multi-tone architecture is able to achieve a BER=10^{-12} with an RJ near $2ps_{rms}$. This is over 5X the jitter required by the time-interleaved system. In a more conventional PAM4 mode, the frequency-domain receiver still provides a 60% improvement in jitter tolerance.

Keywords: analog-to-digital converter, frequency-interleaving, jitter, receiver, serial link

INDUSTRY INTERACTIONS

Intel, Texas Instruments

MAJOR PAPERS/PATENTS

TASK 2810.014, DEEP LEARNING SOLUTIONS FOR ADAS: FROM ALGORITHMS TO REAL-WORLD DRIVING EVALUATIONS

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NAOFAL AL-DHAHIR, THE UNIVERSITY OF TEXAS AT DALLAS

SIGNIFICANCE AND OBJECTIVES

Investigate deep-learning-based algorithms and evaluate their performance using fusion of sensing technologies (regular cameras, infrared lenses, RADAR) to estimate the driver's visual attention in real-world driving conditions. The project explores novel probabilistic models of visual attention, creating shared representation across multiple sensing technologies.

TECHNICAL APPROACH

We analyze alternative sensing technologies suitable for head pose estimation for in-vehicle applications, creating novel visual attention models (gaze). We perform real-world driving tests to evaluate alternative sensors that are appropriate for head pose estimation, benchmarking the results with the Fi-Cap device. We develop novel probabilistic models of the visual attention of the drivers describing confidence regions of the gaze given the position and orientations of the driver's head using deep learning. We propose multimodal deep learning frameworks to fuse sensors using shared layer representation between modalities, creating robust and accurate solutions regardless of the environment.

SUMMARY OF RESULTS

We created Fi-Cap, a helmet with fiducial markers designed for head pose estimation (Fig. 1). This helmet is an important part of the data collection, since it will allow us to estimate reliable ground truth labels for head pose estimation in diverse environments. The size of each square is big and, therefore, the fiducial markers can be accurately detected. The design considers markers in the horizontal and vertical directions, increasing the precision for pitch, yaw and roll rotations. The design of the Fi-Cap system allows multiple fiducial markers to be seen regardless of the head rotation of the target subject. As long as few of the tags are visible, the system is able to provide reliable frame-by-frame estimations which can be used as ground truth for training and evaluating head pose estimation algorithms.

We conduct experiments, where we ask subjects to wear the Fi-Cap system. The subjects also wear a laser mounted on glasses, projecting a trackable mark on a white screen signaling their head pose. The evaluation suggests that with a few seconds of calibration, the system provides reliable head pose estimation with less than 5° of error. We also conducted a preliminary recording of a driver wearing the Fi-Cap system. At least one tag is observed in 99.8% of the frames. Furthermore, we are able to detect four or more tags in 99.2% of the frames, increasing the reliability.

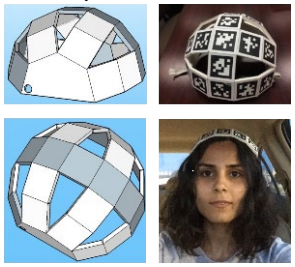

Figure 1. Design of Fi-Cap, which is worn on the back, avoiding occlusions with primary sensors.

1-) Data collection: The project includes the collection of driving recordings using multimodal sensors. The students are being trained to operate the RADAR and camera sensors by our industrial collaborators. We are designing the protocol for the data collection, including the placement and synchronization of the sensors.

2) Visual attention models with deep learning: we aim to establish a probabilistic relationship using a deep learning framework. This approach is more generic than parametric probabilistic models without making assumptions. It learns the relationship between gaze and head pose from the data. In our formulation, the continuous gaze angles are converted into intervals and the grid of the quantized angles is treated as an image for dense prediction. We rely on convolutional neural networks (CNNs) with upsampling to map the six degrees of freedom of the orientation and position of the head into gaze angles. The proposed architecture offers an appealing and general solution to convert regression problems into dense classification problems.

Keywords: ADAS, head pose estimation, deep learning, visual attention, multimodal sensing

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] S. Jha and C. Busso, "Fi-Cap: Robust framework to benchmark head pose estimation in challenging environments," in IEEE International Conference on Multimedia and Expo (ICME), San Diego, CA, July 2018.

TASK 2810.016, CONDITION MONITORING OF INDUSTRIAL/AUTOMOTIVE DRIVE COMPONENTS THROUGH LEAKAGE FLUX

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SIGNIFICANCE AND OBJECTIVES

The fault diagnostics of electrical motors typically use electrical parameters such as current, back emf, voltage etc. The magnetic field in motor also undergos changes due to fault which is reflected in leakage flux measurable on the housing of the machine. It can be used as a good diagnostic tool in frequency domain and sometimes in time domain as well. The initial results for diagnostics of bearing fault are presented here.

TECHNICAL APPROACH

As the conversion of electric energy into mechanical energy takes place via magnetic energy, faulty scenarios are likely to generate some signatures in motor parameters including the air gap magnetic field. However measuring air gap magnetic field is not a feasible approach but the leakage flux around the motor housing can be measured and it is a promisable diagnostic tool.

SUMMARY OF RESULTS

Among the various faults which can occur in an electric motor, the likelihood of occurrence of bearing fault is high. The fault in the bearing is artificially created by drilling a hole in the outer race of bearing (Fig. 1).

Figure 1. Outer race fault in bearing of test motor.

The bearing fault diagnostics based on the motor current signature is most common which has fault signatures in predictable frequencies based on the geometry of bearing and location. Fig. 2 shows the frequency spectrum of phase-A current of faulty motor. The fault signatures are introduction of frequency components at 157.5 Hz and 242.5 Hz. The leakage flux in is monitored in both healthy and faulty motors. The leakage flux spectra of healthy and faulty motors are shown in Fig.3. It can be seen that the mechanical frequency component of flux is introduced due to a fault.

The motor has 8 poles which makes mechanical frequency component as 0.25th component in normalized frequency spectrum in Fig 3. Fig. 4 shows the variation of flux spectrum for various load and speed.

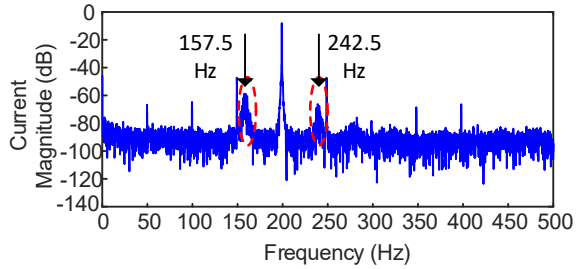

Figure 2. Current spectrum of test motor with faulty bearing.

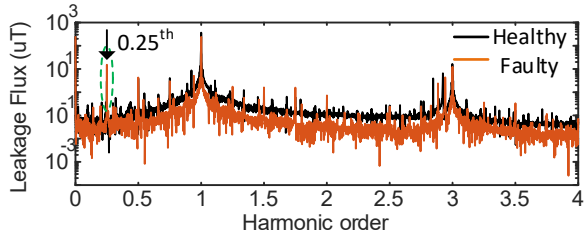

Figure 3. Leakage flux spectrum of test motor with healthy and faulty bearing.

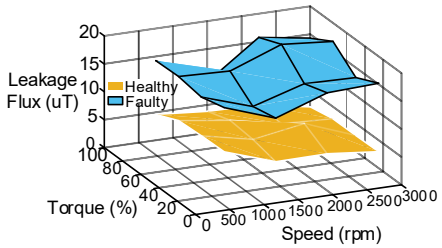

Figure 4. Leakage flux spectrum of test motor with healthy and faulty bearing under various loading condition.

These results show that the leakage flux spectrum can be used as a diagnostic tool for bearing fault detection and the fault signature is not the same as in motor current.

Keywords: fault diagnostics, outer race bearing fault, leakge flux spectrum

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] M. Zafarani, E. Bostanci, Y. Qi, T. Goktas and B. Akin, "Inter-turn Short Circuit Faults in Permanent Magnet Synchronous Machines: An Extended Review and Comprehensive Analysis," in IEEE Journal of Emerging and Selected Topics in Power Electronics.

TASK 2810.017, RELIABILITY STUDY OF E-MODE GAN HEMT DEVICES

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HISHASHI SHICHIJO, THE UNIVERSITY OF TEXAS AT DALLAS

SIGNIFICANCE AND OBJECTIVES

AlGaN/GaN High Electron Mobility Transistors (HEMTs) have emerged as the most promising candidates for high-voltage power switching applications. This project is to investigate the gate TDDB of commercial p-GaN gate E-mode HEMTs by High Resolution TEM/STEM and *in-situ* TEM coupled with the electrical characterization over bias voltage and temperature.

TECHNICAL APPROACH

The recently observed time dependent dielectric breakdown (TDDB) of forward biased gate will be studied on commercially available E-mode GaN HEMT devices. The location and nature of the breakdown percolation path will be determined by high resolution transmission electron microscopy/scanning transmission electron microscopy (HR TEM/STEM) and will be correlated with the electrical TDDB data. In addition, in-situ TEM/STEM will be conducted to understand the electrical break down mechanism in detail.

SUMMARY OF RESULTS

A commercial EPC eGaN HEMT device was preliminarily DC characterized. Figure 1 shows the measured gate current vs. gate voltage and drain and gate current vs gate voltage characteristics of an EPC2007 device. The gate breakdown occurs around the gate voltage of 9V. EPC2016 device was also measured with similar characteristics and breakdown voltage. More in-depth studies of device behaviors as stressed with various gate voltage are in progress.

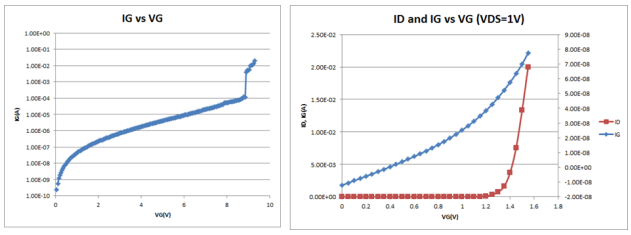


Figure 1. Gate current vs. gate voltage (left) and drain and gate current vs. gate voltage characteristics (right) on EPC2007 eGaN HEMT device.

The device structure prior to electrical gate breakdown was characterized by cross-sectional scanning electron microscopy (SEM), as shown in Figure 2. More detailed microstructural analysis by high resolution TEM/STEM is in progress. Failure analysis is also in progress.

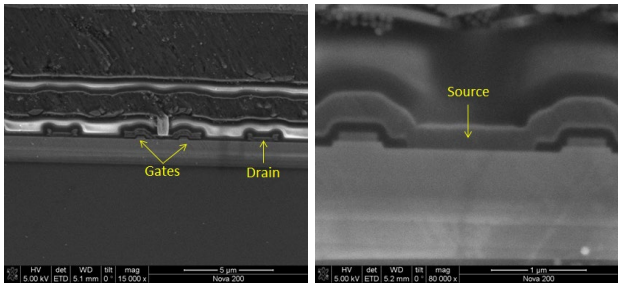


Figure 2. Cross-sectional SEM images of as-received eGaN HEMT device, showing the intended source/gate/drain device structure.

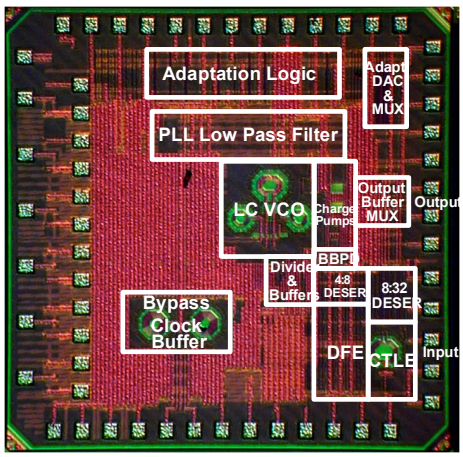
Keywords: E-mode GaN HEMT device, reliability, failure mechanism

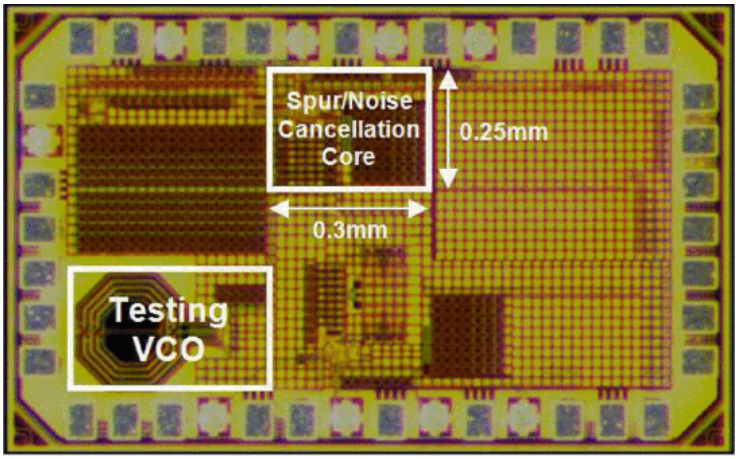
INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

Fundamental Analog Thrust





Category	Accomplishment
Fundamental Analog (Circuits)	A mixed-signal PAM4 quarter-rate receiver employs a single-stage CTLE and a DFE with 1 FIR and 1 IIR-tap to efficiently compensate for more than 20dB channel loss. An edge-based sampler is used to perform both PLL-based CDR phase detection and adaptation of the DFE tap coefficients in background. Fabricated in GP 65-nm CMOS, the 56Gb/s receiver achieves 4.63mW/Gb/sec when operated with a 2-tap FFE transmitter. (1836.143, PI: Sam Palermo, Texas A&M)
Fundamental Analog (Circuits)	Techniques for spur and phase noise cancellation are developed. A delay-and-interpolate method introduces notches to suppress spurs. A delay-line discriminator extracts phase noise and a feed-forward loop cancels out input phase noise. Fabricated in a 65-nm CMOS process, the spurs are suppressed by more than 15dB and the phase noise at offset frequencies in the range of 4MHz-200MHz from a 1.4-GHz carrier is improved by a maximum of 25dB. (2810.007, PI: Ali Niknejad, UC Berkeley)
Fundamental Analog (Circuits)	A 300-GHz 30-Gbps QPSK transmitter consists of an on-chip multi-mode modulator, an injection locked quadrature oscillator, a 40-GHz bandwidth power amplifier with constant gain and group delay, a 4X frequency multiplier chain to generate a 165-GHz LO signal for a double balanced up-conversion mixer that generates the output at 300 GHz. The transmitter without equalization consumes 180mW with an energy efficiency of 6 pJ/bit. (1836.152, PI: Ken O, UT Dallas)

TASK 1836.127, PRECISION TEST WITHOUT PRECISION INSTRUMENTS – A NECESSITY FOR FUTURE ON-CHIP SELF-TEST AND SELF-HEALING

DEGANG CHEN, IOWA STATE UNIVERSITY, DJCHEN@IASTATE.EDU
RANDY GEIGER, IOWA STATE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

IEEE standards on accurate spectral testing require accurate instruments and accurate test control, resulting in expensive equipment, complex test setup, demanding maintenance, TTM delays, and high test cost. This project develops new algorithms to relax conventional requirements, deliver accurate full-spectrum testing, greatly reduce equipment cost, TTM delays, and test time.

TECHNICAL APPROACH

Spectral testing is re-casted as an identification problem of weakly nonlinear systems. Statistical signal processing techniques are incorporated to develop algorithms for accurately separating and extracting all distortion, jitter, and noise information out of a greatly reduced data set. An innovative iterative time-frequency domain processing technique achieves optimal accuracy and efficiency trade-offs. All spectral spurs (input, distortions, periodic jitter, etc.) are identified in frequency domain while residue error construction and noise/jitter characterization are done in time domain. This dual-domain approach enables high time efficiency and high dynamic range detection, allowing accurate spectral estimation in the simultaneous presence of various error sources.

SUMMARY OF RESULTS

The final goal of the project is the elimination of all the stringent requirements in the ideal IEEE standard spectral testing. These requirements include: coherent sampling, accurate amplitude control, high purity sinusoidal signal sources, and jitter-free sampling clock signal. During the project, we published 9 journal papers and 19 conference papers. These papers introduced: 1) the FIRE method for removing non-coherency, 2) the FERARI method for both non-coherency and amplitude clipping, 3) a jitter and noise separation method for accurate SNR testing, 4) a comparative study of state of the art methods for dealing with non-coherent sampling, 5) an algorithm for both nonlinear signal source and non-coherent sampling, 6) an algorithms for simultaneous AC and DC test with dramatic test time reduction, 7) an algorithm for accurate SNR test in the presence of clock jitter, 8) a method for clock jitter separation and characterization, 9) a method for ultra-pure sine wave generation, 10) a method for dealing with simultaneous amplitude and frequency drifts, 11) a method for accurate and fast decomposition of jitter in high speed links, and 12) a low-cost comparator based method for jitter decomposition.

During the half year May 2017 – December 2017, we published 6 journal papers and 11 conference papers. SRC is also applying for two patents on our behalf. We developed an algorithm for accurate spectral testing with non-coherent sampling and large distortion to noise ratios. We also presented a new test solution for accurate spectral testing of ADCs despite both amplitude and frequency drifts using proper segmentation and and averaging techniques. With a simple ISI model, we developed a method for accurate RJ and DJ decomposition and estimation for high-speed data links. Building upon this, we presented a low-cost method for multi-site ADC testing with clock jitter, aperture jitter and noise separation. Many of the proposed test algorithms have been validated at SRC member companies.

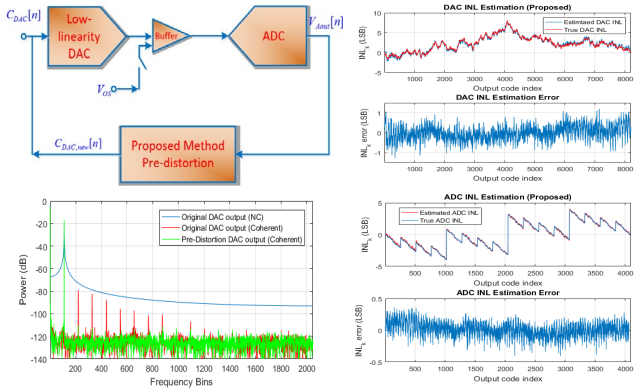


Figure 1. Low cost simultaneous co-testing and calibration of both ADC and DAC with a shift mechanism in between. Right upper shows accurate DAC testing. Right lower shows accurate ADC testing. Left lower shows 30 dB improvement in DAC output linearity.

Keywords: AC test, spectral test, nonlinear source, non-coherent sampling, jitter

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

[1] Zhuang, book'18; [2]Zhuang, ITC Asia'18; [3] Zhuang, ITC Asia'18; [4] Chaganti, ISCAS'18; [5] Liu, ISCAS'18; [6] Zhuang, I2MTC'18; [7] Chaganti,I2MTC'18; [8] Liu, TCAS-I'18; [9] Zhuang, TIM'18; [10] Duan, TEMC'18; [11] Duan, TEMC'18; [12] Chen, TCAS-I'18; [13] Zhuang, TCAS-II'17; [14] Zhuang, TIM'17; [15-6] Zhuang, patents pending.

TASK 1836.134, HYBRID TWO-STEP PLLS FOR DIGITAL SOCS IN NANOSCALE CMOS

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SIGNIFICANCE AND OBJECTIVES

PLLs are a critical part of today's communication systems. Their performance optimization is essential for modern SOCs. The objective of this project is to replace the bulky on-chip inductors used in low-jitter PLLs with compact ring oscillators, while still preserving the performance. This calls for development of a hybrid two-step PLL.

TECHNICAL APPROACH

The overall frequency conversion is divided into two cascaded stages (Fig.1). The first stage, employing a novel Type-I sub-sampling phase detector (SSPD) loop generates a high quality, high frequency reference for the second stage. The second stage, a fractional-N PLL, provides the required fine resolution. Due to the low-ratio multiplication, it has much reduced noise impact.

SUMMARY OF RESULTS

The usage of large bandwidth (>1MHz) in the two-step PLLs architecture (Fig. 1) reduces the noise impact of the VCOs. This enables the usage of compact ring oscillators in spite of there poorer performance in comparison to large-size LC oscillators. The large BW also helps in shrinking the loop filter area, further reducing the area of the PLL. The research is currently focused on the first-stage ring-oscillator PLL architecture and circuit design.

A ring-oscillator (RO) based PLL is presented combining a type-I architecture and a sub-sampling phase detector (SSPD). It achieves low jitter thanks to the wide-bandwidth type-I loop and low reference spurs thanks to the SSPD with its sample-and-hold function and high gain. The integrating filter capacitor is avoided, resulting in a very low area.

The PLL prototype was taped out in 65nm CMOS (Fig. 2) in May 2017. The PLL occupies 0.008mm^2, has a loop bandwidth of 15MHz and tunes from 2 to 3.2GHz. It consumes 6.1mW at 2.4GHz with a phase noise of -122.6dBc/Hz at 1MHz offset (Fig. 3). The measured reference spurs, RMSjitter and FoMjitter are -64.2dBc, 422fs and -239.7dB.

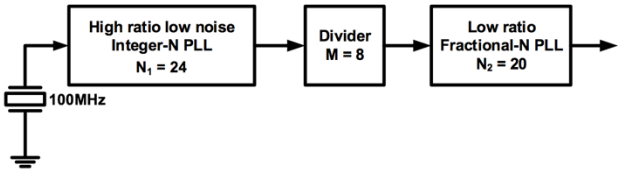

Figure 1. The block diagram of the proposed two step PLL.

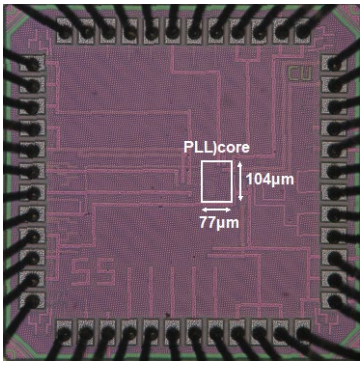

Figure 2. Die photo of the Type-I SSPD ring-oscillator PLL prototype.

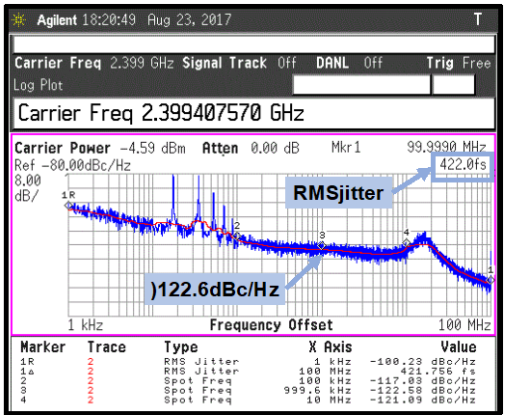

Figure 3. Measured phase noise of the Type-I SSPD PLL with loop BW of 15MHz.

Keywords: two-step PLLs, sub-sampling phase detectors, ring oscillators, wide bandwidth Type-I PLL.

INDUSTRY INTERACTIONS

Intel, Texas Instruments, Globalfoundries

MAJOR PAPERS/PATENTS

[1] Shravan Nagam and P. R. Kinget, " A 0.008mm^2 2.4GHz Type-I Sub-Sampling Ring-Oscillator-based Phase-Locked Loop with a -239.7dB FoM and -64dBc Reference Spurs," 2018 IEEE Custom Integrated Circuits Conference.

[2] Shravan Nagam and P. R. Kinget, "A Low-Jitter Ring-Oscillator Phase-Locked Loop Using Feedforward Noise Cancellation With a Sub-Sampling Phase Detector," IEEE Journal of Solid State Circuits, Volume: 53, Issue: 3, March 2018.

TASK 1836.136, INJECTION-LOCKED RING OSCILLATORS FOR CLOCK DISTRIBUTION IN MANYCORE PROCESSORS

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SIGNIFICANCE AND OBJECTIVES

Technology scaling has enabled integration of many independent processing elements on a single die or in the same module. Energy-efficient circuit design for synchronization of manycore processors, based on both traditional PLLs and DLLs and on injection-locked ring oscillators is the objective of this work.

TECHNICAL APPROACH

We have developed a low-overhead global clock distribution scheme for manycore processors and heterogeneous SoCs. We have studied distribution based on DLLs and injection-locked MDLLs and implemented prototypes on several test chips.

SUMMARY OF RESULTS

We have developed three designs for clock generation in manycore processors, based on a central bang-bang PLL, Fig. 1, followed by a per-core delay-locked loop (DLL) or a multiplying DLL (MDLL), and implemented them in four test chips, Fig 2. In the first approach [1-2], a ~2GHz reference clock is distributed to DLLs, which generate 16 uniformly-distributed clock phases. Phase-picking clock generator picks the appropriate phase for each clock cycle, based on an information from the timing replica path.

The design, implemented in a 28nm ultra-thin body and BOX fully-depleted silicon-on-insulator (UTBB FDSOI) technology is fully functional and occupies 32µm x 30µm, Fig. 3. Generated clock frequency is in the range 550-2260MHz at 1V and 100-625MHz at 0.5V.

The second clock generation scheme is self-timed [2]. Figure 2 shows the schematic of the adaptive clock generator. The delay units are composed of four tunable delay banks, each of which uses a different cell for its delay element and can be tuned independently. Instead of using the delay line outputs for selecting DLL phases, in this approach we simply asynchronously toggle a standard flip-flop through its set/reset inputs. This design was also implemented in the 28nm UTBB FDSOI process and achieved similar performance with much lower complexity.

The third local clock generation scheme is based on coupled to an injection-locked MDLL that multiplies the reference clock frequency by four.

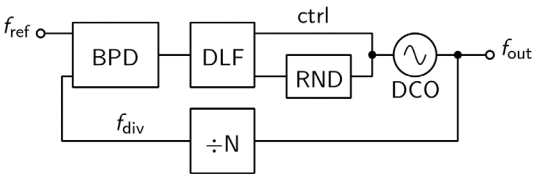

Figure 1. Bang-bang PLL.

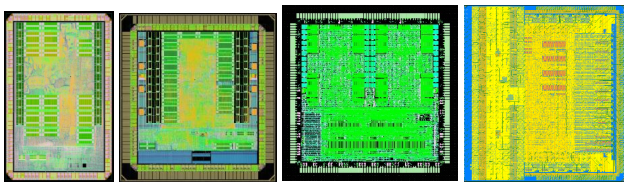

Figure 2. Four test chips.

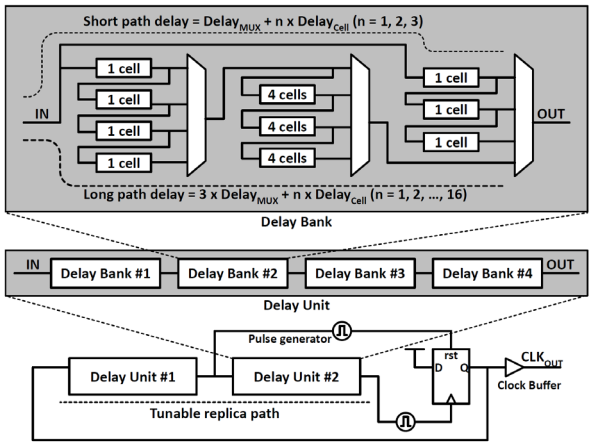

Figure 3. Self-timed clock generation.

Keywords: CMOS, clock, manycore, DLL, PLL

INDUSTRY INTERACTIONS

Intel

MAJOR PAPERS/PATENTS

[1] B. Zimmer, *et al*, "A RISC-V vector processor with simultaneous-switching switched-capacitor DC-DC converters in 28nm FDSOI," *IEEE J. Solid-State Circuits*, 2016, vol. 51, no. 4, pp. 930-942, Apr. 2016.

[2] J. Kwak, B. Nikolić, "A self-adjustable clock generator with wide dynamic range in 28nm FDSOI," *IEEE J. Solid-State Circuits*, vol. 51, no. 10, pp. 2368-2379, Oct. 2016.

[3] B. Keller, et al, "A RISC-V processor SoC with integrated power management at sub-microsecond timescales in 28nm FD-SOI," to appear in *IEEE J. Solid-State Circuits*, vol. 52, no.7, Jul. 2017.

TASK 1836.137, 50GS/S AND BEYOND FREQUENCY-INTERLEAVED ENERGY-EFFICIENT ADCS

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SIGNIFICANCE AND OBJECTIVES

This research explores a novel ADC architecture to realize a frequency-interleaved analog-to-digital conversion (FI-ADC), ultimately to push the performance limits of very high-speed ADCs. Performance of conventional high-speed ADCs is limited by jitter and we aim to determine if and how the FI-ADC can mitigate the jitter sensitivity of high-speed ADCs.

TECHNICAL APPROACH

One of the key focus areas of this work has been the development of a comprehensive model for comparing the FI-ADC to the time-interleaved ADC (TI-ADC). A comprehensive quantitative analysis was performed in addition to system-level simulations that compare the two architectures. The simulations support the theoretical findings and additionally provide further insight into the conditions under which the FI-ADC outperforms the TI-ADC.

SUMMARY OF RESULTS

This has been the final period of review for this project. In the first phase of the project, we designed a frequency interleaved ADC with an innovative distributed amplifier based signal splitter that provides filtering and high bandwidth (see Fig. 1). The prototype is shown in Fig. 2. The second phase of the proejct focused on analytical formulation and numerical simulation. A key results from this work is the detailed analysis of the impact of jitter and phase noise on the FI-ADC. Previous works have hinted at the reduced jitter sensitivity of the FI-ADC due to the reduced bandwidths presented to the sampling network, but have failed to provide an analysis of the impact of phase noise introduced during the downconversion which occurs in each passband channel. Quantitative analysis shows that the phase noise on the LOs used for downconversion plays a critical role in determining if the FI-ADC outperforms the TI-ADC. In general, the FI-ADC has the potential to improve performance for high input frequencies but may sacrifice performance at lower frequencies depending on the implemented architecture. Using our comprehensive model, we can predict maximum achievable SNR. Results have been published in Techcon 2016.

The final phase of the project focused on a redesign of key buildign blocks that limit performance. In particular, the LO chain of the chip must generate LO frequencies from a common low phase noise VCO using frequency dividers and mixers. The first divider is one of the key components as it must operate at high frequency, similar to the prescalar in a PLL. We analyzed the optimal CML divider design for low phase noise and high carrier frequency locking (40 GHz), designed a 28nm frequency divider chain for a new FI-ADC architecture and sent design for fabrication. We published a final report summarizing the project accomplishments to date.

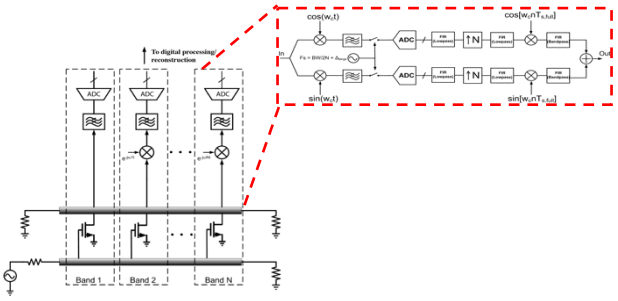

Figure 1. Architecture of FI-ADC.

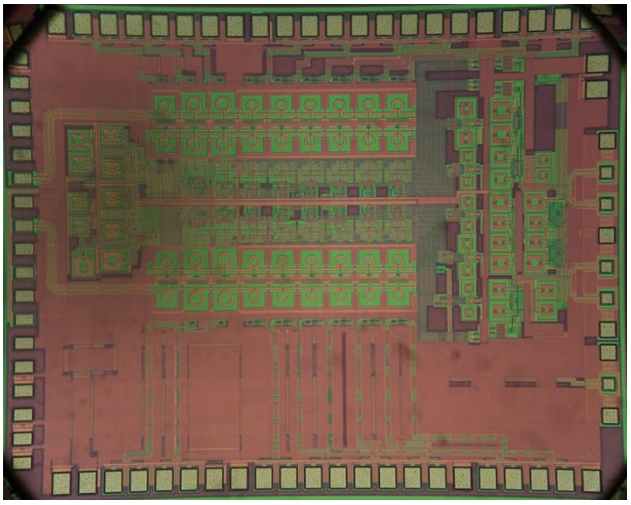

Figure 2. Die photo of prototype FI-ADC in 65nm CMOS.

Keywords: high-speed ADC, frequency-interleaved, channelized front-end, wideband receiver

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] N. Baniasadi and A. M. Niknejad, “Jitter Analysis in Frequency-Interleaved ADCs,” Techcon 2016

TASK 1836.143, DESIGN TECHNIQUES FOR MODULATION-AGILE AND ENERGY-EFFICIENT 60+GB/S RECEIVER FRONT-ENDS

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SIGNIFICANCE AND OBJECTIVES

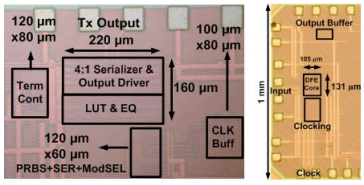
While high-performance I/O circuitry can leverage CMOS technology improvements, unfortunately the bandwidth of the electrical communication channels has not scaled in the same manner. The high-speed serial link receiver design and modeling techniques proposed here aim to significantly improve interconnect bandwidth density in an energy-efficient manner.

TECHNICAL APPROACH

In order to investigate design trade-offs, a statistical-modeling framework will be utilized to investigate power-optimum equalization partitioning and modulation format for 60+Gb/s signaling environments. This tool will be used to guide the design of a new modulation-agile receiver front-end which includes a multi-level decision-feedback equalizer (DFE) with multiple FIR/IIR feedback taps for efficient long-tail ISI cancellation. Adaptive techniques will also be developed to tune key equalization parameters, such as DFE tap time constants/weights and CTLE settings.

SUMMARY OF RESULTS

While dedicated PAM4 transceivers have been developed, the majority of serial I/O standards use simple binary NRZ modulation. In order to address this, a dual-mode NRZ/PAM4 SerDes which seamlessly supports both modulations with a 1-FIR- and 2-IIR-tap DFE receiver and a 4/2-tap FFE transmitter in NRZ/PAM4 modes were developed [1],[2]. A source-series-terminated (SST) transmitter employs lookup-table (LUT) control of a 31-segment output DAC to implement FFE equalization in NRZ and PAM4 modes with an 1.2Vpp output swing and utilizes low-overhead analog impedance control. Optimization of the quarter-rate transmitter serializer is achieved with a tri-state inverter-based mux with dynamic pre-driver gates. The quarter-rate DFE receiver achieves equalization with 1-FIR tap for the large first post-cursor ISI and 2-IIR taps for long-tail ISI cancellation. Fabricated in GP 65-nm CMOS (Fig. 1), the transceiver occupies 0.074 mm^2 and achieves power efficiencies of 10.9 and 5.5 mW/Gbps with 16Gb/s NRZ and 32Gb/s PAM4 data.



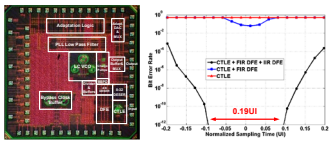
(a) (b)

TRANSCEIVER PERFORMANCE SUMMARY

References	This Work		[5]	[6]	[35]	[13]	[34]
Data Rate	32 Gb/s	16 Gb/s	20 Gb/s	56 Gb/s	56 Gb/s	28 Gb/s	16 Gb/s
Equalization	2-tap TX FFE + 1-tap FIR, 2-tap IIR RX DFE	4-tap TX FFE + 1-tap FIR, 2-tap IIR RX DFE	3-tap TX FFE	3-tap TX FFE + 1-tap RX DFE	3-tap TX FFE + RX CTLE + ADC based RX 24-tap FEE, 1-tap DFE	5-tap TX FFE + RX CTLE + 14-tap RX DFE	3-tap TX FFE + RX CTLE + 14-tap RX DFE
Modulation	PAM4	NRZ	PAM4	PAM4	PAM4	NRZ	NRZ
Total Loss @ Nyquist	13.5 dB	27.6 dB	5 dB	2 dB	25dB	40 dB for 25.78 Gb/s	34 dB
Eye Width BER	6% 10^{-12}	18% 10^{-12}	- 10^{-12}	- 10^{-12}	- 10^{-8}	23% 10^{-12}	- 10^{-15}
Supply (V)	1.2 TX, 1 RX		1.8	1.2	0.9 digital, 1.2 analog, 1.8 auxiliary	1 TX & RX, 1.25 TX driver	1/1.5 TX, 0.9 RX
Power (mW) (mW/Gbps)	176.3 5.5	173.7 10.9	408 20.4	475 8.5	550* 9.8	295* 10.5	235* 14.7
Area (mm^2)	0.074		0.43	2.74	1.4	0.62	2.15
Technology	65-nm		90-nm	65-nm TX, 40-nm RX	16-nm FinFET	28-nm	40-nm

(c)

Figure 1. 16/32Gb/s dual-mode NRZ/PAM4 SerDes in 65nm CMOS: (a) transmitter, (b) receiver, (c) performance summary.



(a) (b)

Figure 2. 56Gb/s PAM4 receiver: (a) 65nm CMOS die photo and (b) timing bathtub curves with a 20.8dB loss channel.

For higher data rate operation over higher-loss channels, a PAM4 quarter-rate receiver was developed that employs a single-stage CTLE and a DFE with 1 FIR and 1 IIR-taps to efficiently compensate for the channel loss [3]. In addition to the per-slice main 3 data samplers, an error sampler is utilized for background threshold control. An edge-based sampler performs both PLL-based CDR phase detection and generates information for background DFE tap adaptation. Fabricated in GP 65nm CMOS, the 56Gb/s receiver achieves 4.63mW/Gb/s and compensates for up to 20.8dB loss when operated with a 2-tap FFE transmitter.

Keywords: decision feedback equalizer, infinite impulse response (IIR) DFE, receiver, serial link

INDUSTRY INTERACTIONS

IBM, Texas Instruments

MAJOR PAPERS/PATENTS

[1] A. Roshan-Zamir et al., "A 16/32 Gb/s Dual-Mode NRZ/PAM4 SerDes in 65nm CMOS," IEEE CSICS, 2016.

[2] A. Roshan-Zamir et al., "A Low-Overhead Reconfigurable 16/32 Gb/s Dual-Mode NRZ/PAM4 SerDes in 65nm CMOS," IEEE JSSC, Sept. 2017.

[3] A. Roshan-Zamir et al., "A 56 Gb/s PAM4 Receiver with Low-Overhead Threshold and Edge-Based DFE FIR and IIR-Tap Adaptation in 65nm CMOS," IEEE CICC, 2018.

TASK 1836.148, 50GSPS+ TI HYBRID SAR ADC ARRAY WITH COMPREHENSIVE DDI CALIBRATION

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SIGNIFICANCE AND OBJECTIVES

Time interleaving is an effective way to increase analog-to-digital conversion (ADC) speed. Low-power, high-speed sub-ADC is needed to reduce the interleaving complexity and power consumption. This work introduces a V-T hybrid two-step SAR ADC to meet both the speed and the efficiency target. Also, a reference dither based skew calibration is introduced to calibrate the timing mismatch of the interleaving array.

TECHNICAL APPROACH

A comparator's resolving time is roughly inversely proportional to its input voltage magnitude. In this work the comparator resolving time of the residue voltage on the summing node of a SAR ADC is quantized by the second-stage time-to-digital converter (TDC), resulting in an efficient two-step quantization structure. A slow-but-accurate reference ADC with precise timing is introduced and used as a timing reference of the array. The ref. ADC clock is modulated by a 1b pseudo-random signal and the skew information is extracted by correlating the PN signal with the output difference between the ref. ADC and sub-ADCs.

SUMMARY OF RESULTS

In the previous phases of this project, we designed and tested a 24GS/s TI-ADC. Important lessons are learned from that design and pave our way to the 50GS/s TI-ADC. Instead of doubling the interleaving factor to achieve twice the sampling frequency, some crucial modifications are necessary. Our plan is to keep the interleaving factor=16 and increase the single channel speed to 3.125GS/s with a multibit/stage approach. This allows us to keep a simple floor plan and to minimize the calibration overhead. Also hierarchical sampling will be adopted to alleviate the burden of front-end sampling and skew calibration.

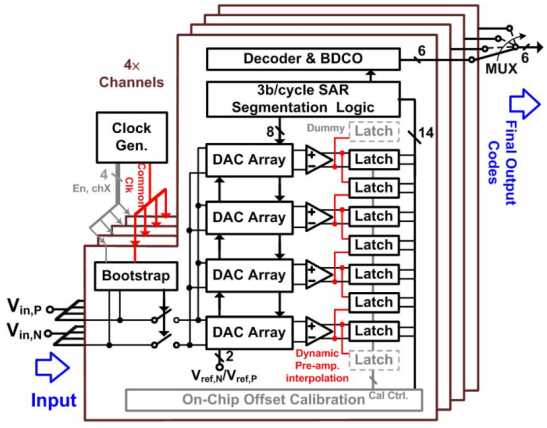

Figure 1. 3b/cycle SAR [Chan, ISSCC 2015].

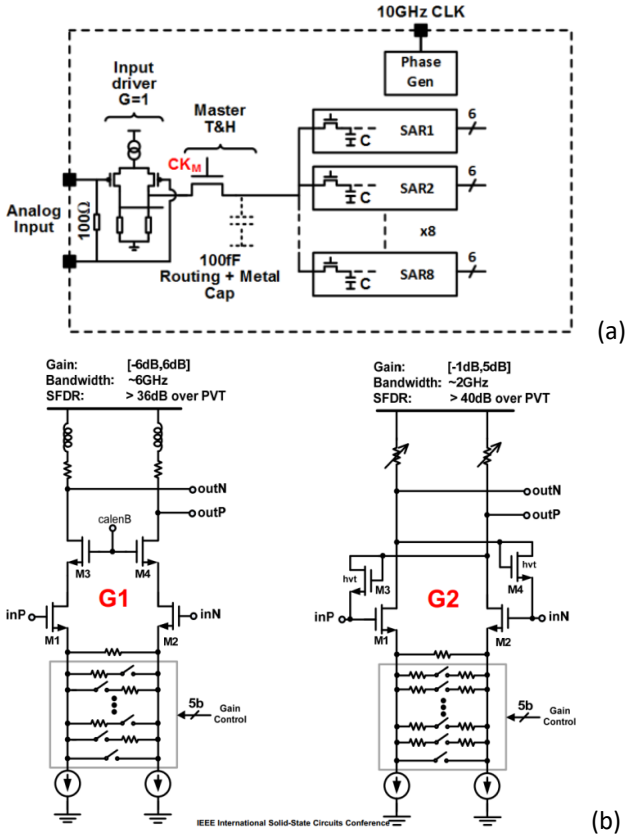

Figure 2. (a) common source input buffer [Le Tual, ISSCC 2014] (b) common source with inductive peaking buffer [Varzaghani, JSSC 2013].

Keywords: TI-ADC, calibration, hybrid SAR, reference-ADC equalization, direct derivative information

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] "System and method for dynamic path-mismatch equalization in time-interleaved ADC," U.S. Patent No. 9,287,889.

[2] "Pipelined SAR ADC using comparator as a voltage-to-time converter with multi-bit second stage," U.S. Patent application # 15/620,821.

TASK 1836.152, FEASIBILITY OF CMOS TRANSMITTER AND RECEIVER FOR 500-GBPS COMMUNICATION OVER DIELECTRIC WAVEGUIDE

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SIGNIFICANCE AND OBJECTIVES

The increasing bandwidth of silicon integrated circuits is enabling a waveguide interconnection system using millimeter waves that may be be able to support communication at 500-Gbps. If proven feasible, this technology will provide a bandwidth approaching that of optical systems, while bypassing the photonic component integration and coupling/packaging challenges of optical systems.

TECHNICAL APPROACH

This project in conjunction with the efforts on developing transitions and dielectric waveguides is investigating the feasibility of 500 Gbits/sec electronic communication over a 1-m dielectric waveguide using circuits fabricated in 65-nm CMOS. Use of a combination of frequency division multiple access (Five frequency channels), polarization division multiple access and a higher order signal modulation scheme will be investigated. Based on the results, implementation plans for a 120-Gbps communication system incorporating two frequency bands and two polarization modes will be formulated.

SUMMARY OF RESULTS

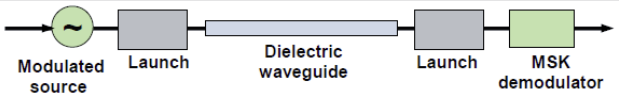

Figure 1. Conceptual diagram of the dielectric waveguide communication system.

Fig. 1 shows a conceptual diagram of the dielectric waveguide system. It consists of a transmitter, a launch from the transmitter to a waveguide, a waveguide, a launch from a waveguide to a receiver, and a receiver. The system uses five 45-GHz frequency bands spanning 157.5 to 382.5 GHz and supporting two polarization channels for a total of 10 channels.

Fig. 2 is a block diagram of transmitter, while Fig. 3 is that of receiver for the 315-GHz band. The receiver down converts, amplifies, demodulates and performs clock and data recovery to generate a digital output stream. Presently, the receiver in simulation can demodulate up to 10Gbps, which is limited by the delay through the loop. Approaches to increase the data rate to 30Gbps are being investigated. The receiver and transmitter designs in 65-nm CMOS have been fabricated. The transmitter was used to generate a 300-GHz 30-Gbps QPSK modulated signal that meets the output power target of -6dBm [5] while consuming 180mW.

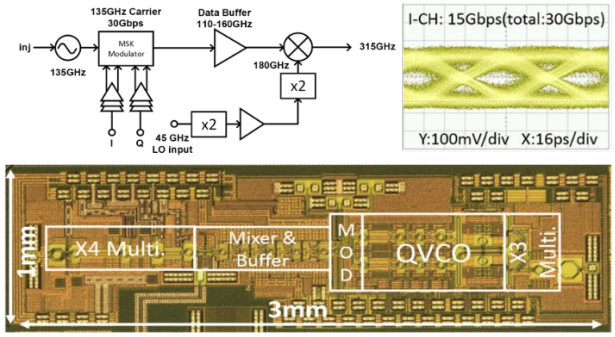

Figure 2. Block diagram of transmitter for the 315-GHz band. Measured eye diagram at 30-Gbps and die photo.

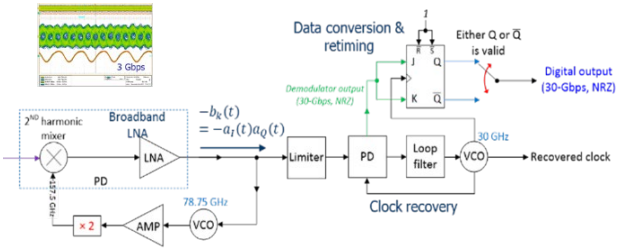

Figure 3. Block diagram of receiver for the 315-GHz band.

The 300-GHz receiver operation was confirmed using a 3-Gbps FSK input. The MSK receiver can demodulate a continuous phase FSK signal (Fig. 3). The power consumption not including that for a CDR is 220mW. The eyes are not good due the quality of signals that can be generated with an arbitrary waveform generator.

Keywords: dielectric, waveguide, communication, sub-millimeter, waves

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] Z. Ahmad et al., "Devices and Circuits in CMOS for THz Applications," (Invited), *IEDM*, Paper 29.8, pp. 734-737, Dec. 2016, San Francisco, CA.
[2] Q. Zhong et al., "CMOS Terahertz Receivers," (Invited) *IEEE CICC*, April, 2018, San Diego, CA.
[3] Q. Zhong et al., "300-GHz CMOS QPSK Transmitter for 30-Gbps Dielectric Waveguide Communication," *IEEE CICC*, April 2018, San Diego, CA.

TASK 1836.156, TRANSITION DESIGN FOR HIGH DATA RATE LINKS AT SUBMILLIMETER WAVE FREQUENCIES

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SIGNIFICANCE AND OBJECTIVES

This project focuses on transition designs interfacing a CMOS IC to a dielectric waveguide for high data rate wireline communication links. This all-electronics effort is designed at millimeter wave frequencies to offer a larger bandwidth while utilizing standard IC and packaging processes for low-cost system implementation.

TECHNICAL APPROACH

The technical approach involves using a manifold diplexer design to combine 180 and 315 GHz coupled line filters. These filters are used on the transmit and receive sides of the links and are then integrated with a dual-band antenna to excite those 180 and 315 GHz signals through a square waveguide. The signals are then transferred to a dielectric waveguide which can support the entire bandwidth for the transceiver circuits (Fig. 1). The PWB transition will improve efficiency of the transitions.

SUMMARY OF RESULTS

We completed a second tapeout with Ken O's team that included the diplexer with two receiver designs at 180 and 315 GHz. In order to provide a demonstration IC we also included a dual-band dipole antenna in a cross configuration to excite the dielectric waveguide. This compact antenna design is created by adding a spur to the 180 GHz design which allows the 315 GHz signal to radiate.

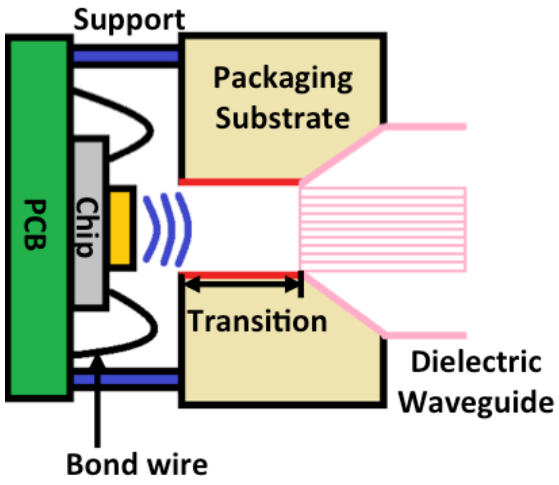

Figure 1. Concept of radiating antenna on a transceiver die and a quad ridge waveguide transition located above the die to couple to the dielectric waveguide. The waveguide transition is realized using packaging substrate material.

These two antennas should have the bandwidth to support the RF signal and also radiate to a quadruple ridge waveguide. The quad ridge waveguide will be manufactured with PWB techniques and at the appropriate size to support 122 to 337 GHz signals.

Fig. 2 shows the PWB transition above the chip with antennas. The waveguide opening is 0.711 mm x 0.711 mm, the ridge is 0.168 mm and the gap (directly above the antennas) is 0.375 mm x 0.375 mm. The plated through hole vias are 0.130 mm and the center-to-center pitch is 0.113 mm. 16 layers of 0.10mm thick dielectric will be used to implement the electrical transition. Also in the figure is crossed dipole antenna with ground plane keep out of 0.4 mm x 0.68 mm. The 180 GHz antenna is 0.370 mm x 0.20 mm but folded down to 0.275 mm. The 315 GHz dipole is 0.241 mm x 0.12 mm.

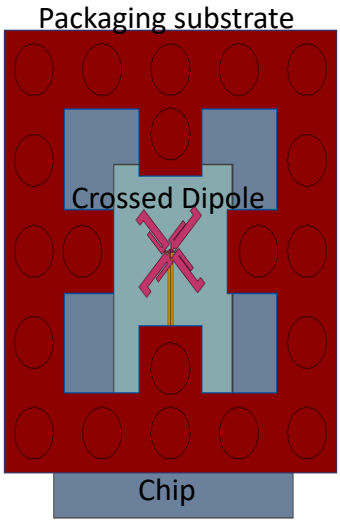

Figure 2. Top view of quad ridge waveguide transition with crossed dipole below.

Keywords: diplexer, dual-band dipole antenna, quad ridge waveguide, printed wiring board (PWB)

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] N. Mahendarkar Vijayakumar, M. Gomez, K. K. O, R. Henderson, "Submillimeter Wave Manifold Diplexer Designed in 65 nm CMOS," *2018 SiRF Conference*, Anaheim, CA, Jan. 2018.

TASK 1836.157, CMOS GSPS 12-BIT SAR ADC ARRAY WITH ON-CHIP REFERENCE BUFFERS

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SIGNIFICANCE AND OBJECTIVES

ADCs that can deliver GS/s, 12-14 bit performance are of critical demand for applications such as wireless base stations, instrumentations, and software-defined radios, and usually consume more than 500 mW. The target of this work is to time-interleave 4 pipelined two-step SAR ADCs to achieve GSPS throughputs at a 12-bit resolution with a power consumption of less than 50 mW.

TECHNICAL APPROACH

The sub ADC used in the time-interleave array is based on the pipelined two-step SAR architecture which can deliver a desirable throughput while maintaining high power efficiency. To further enhance the conversion speed, 2b/cycle conversion scheme is exploited by the first stage. The offsets of first-stage comparators are calibrated in a foreground way to remove the impact on the overall conversion accuracy. Meanwhile, a dynamic amplifier is employed as the inter-stage residue amplifier. Benefiting from the dynamic amplifier, a very power efficient residue amplification that also consumes less time relative to the conventional amplifier is obtained.

SUMMARY OF RESULTS

A 4-way time-interleaved SAR ADC array in 65nm CMOS has been taped out. It consists of 4 single channel pipelined SAR ADCs operating at a 250MS/s conversion rate. An algorithm is implemented to calibrate the inter-channel gain, offset and skew mismatches.

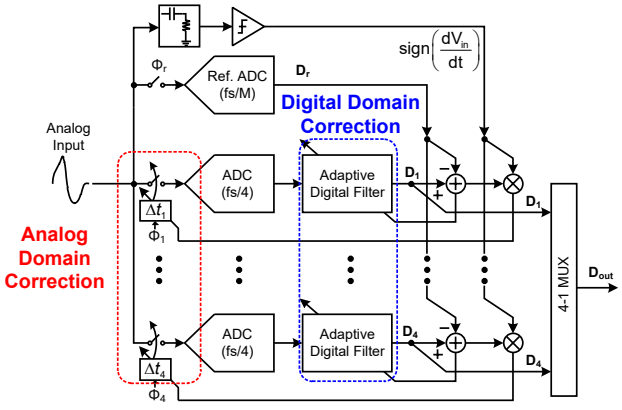

Figure 1. Block diagram of the prototype 12b, 1GS/s time-interleaved ADC array.

Fig. 1 illustrates the block diagram of the prototype TI-ADC. The sub-ADCs utilize an asynchronous SAR timing scheme, with integrated on-chip reference buffers. The SAR raw outputs are background calibrated in the digital domain. Four digitally controlled delay lines (DCDL) are also employed to fine-tune the sampling clock phases of the sub-ADCs to minimize any skew mismatch errors.

Fig. 2 shows a layout screenshot of the 12bit 1GS/s ADC array implemented in the GlobalFoundries 65nm CMOS process. The reference ADC and the high-pass filter are all implemented on-chip. Table 1 summarizes the post-layout simulation results.

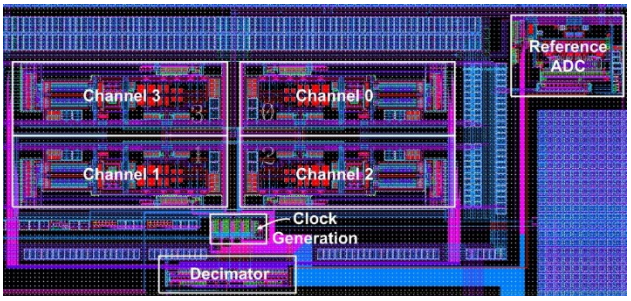

Figure 2. Layout screenshot of the prototype.

Table 1. Summary of the post-layout simulation results

Process	65nm CMOS	
Sampling speed	1 GS/s	
Input swing	2.4 V	
SNDR	71.5 dB	
Power dissipation	Single channel	5.5mW
	Total	30.0mW

Keywords: time-interleaved ADC, split-ADC, pipelined two-step SAR, dynamic amplifier

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] H. Huang, H. Xu, B. Elies, and Y. Chiu, "A Non-Interleaved 12 b 330 MS/s Pipelined-SAR ADC with PVT-Stabilized Dynamic Amplifier Achieving Sub-1 dB SNDR Variation," IEEE Journal of Solid-State Circuits, Dec. 2017.

TASK 1836.158, DEVELOPMENT OF DIELECTRIC WAVEGUIDES FOR THZ RADIATION APPLICATIONS

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SIGNIFICANCE AND OBJECTIVES

The task comprises the design, fabrication, characterization and application of square dielectric waveguides for the propagation of THz and near-THz radiation using a "holey" fiber structure to engineer the refractive index profile and thereby supporting high-speed data transmission to provide interconnection between electronic chips and boards.

TECHNICAL APPROACH

A holey core/cladding structure is presented for low loss transmission. A holey cladding forces the beam to travel in the core using an appropriate boundary condition while creating low loss propagation with a holey core. The first generation of the structure is assembled using commercially available borosilicate capillaries. The transmission loss is measured using a vector network analyzer. A horn antenna is used to maximize coupling efficiency out of the waveguide.

SUMMARY OF RESULTS

Figs. 1 (a) and (b) show the selected design. Four square capillary tubes with 0.5 mm inner and 0.6 mm outer dimensions form the cladding. The core capillaries have 0.3 mm and 0.25 mm outer and inner dimensions, respectively. The four cladding corner squares were eliminated to increase the core-confinement.

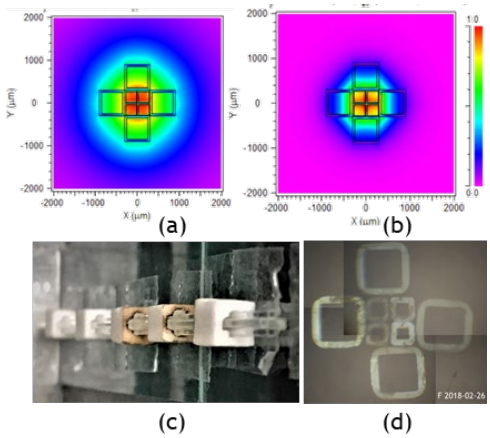

Figure 1. Mode profile of the accepted design at (a) 180 GHz and (b) 360 GHz. (c) The assembled waveguide and (d) the waveguide cross section.

The design supports both vertical and horizontal states of polarization in the frequency range of 180 GHz to 360 GHz. This design shows a 0.15 dB/cm loss reduction compared to a square solid core holey cladding dielectric THz waveguide. Figures 1 (c) and (d) show the assembled waveguide and its cross section.

An assembled waveguide was tested for fiber loss. Fig. 2(a) shows the measurement setup. Fig. 2(b) shows the measured fiber loss. The measured average fiber loss of 5.85 dB/cm is mostly due to the material loss of the borosilicate capillaries. A comparison between a quartz and borosilicate single capillary (0.5 mm inner size and 0.1 mm walls) shows a factor of five material loss reduction (0.88 dB/cm compared to 4.44 dB/cm).

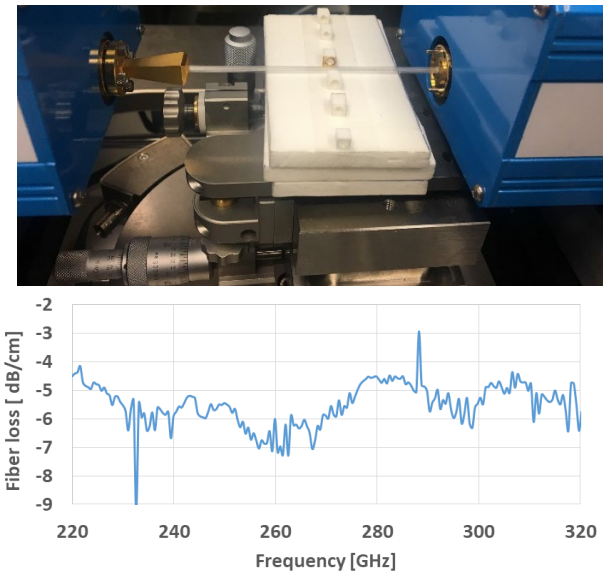

Figure 2. Experimental setup (a) and measured fiber loss (b).

The next step is to demonstrate the low loss design in quartz using commercially available sizes and appropriate wavelength for these dimensions. This will determine whether an investment in scaling these quartz capillaries is justified.

Keywords: dielectric losses, submillimeter waveguides

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] N. Aflakian, T. LaFave Jr, R. M. Henderson, K. K. O, and D. L. MacFarlane, "Low Loss Square Grid Dielectric Waveguide," Manuscript submitted *ECOC,* Roma, Italy (2018).

TASK 2712.004, HIERARCHICAL ANALOG AND MIXED-SIGNAL VERIFICATION USING HYBRID FORMAL AND MACHINE LEARNING TECHNIQUES

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SIGNIFICANCE AND OBJECTIVES

We present a new direction in AMS verification by proposing a hybrid formal/machine-learning verification technique (HFMV) to combine the best of the two worlds. HFMV adds formalism on the top of a probabilistic learning model while providing a sense of coverage for extremely rare failure detection.

TECHNICAL APPROACH

With increasing design complexity and robustness requirement, analog and mixed-signal (AMS) verification manifests itself as a key bottleneck. While formal methods and machine learning have been proposed for AMS verification, these two techniques suffer from their own limitations, with the former being specifically limited by scalability and the latter by the inherent uncertainty in learning based models. In HFMV, the probabilistic model is trained from limited simulation/measurement data and comes with a measure of uncertainty for each prediction of the circuit performance under verification. Given a bounded verification space of design or uncertainty parameters, e.g. process variations or operating conditions, formal verification is applied with respect to a symbolic formula derived from the posterior prediction of the probabilistic learning model to check if the targeted specification is met across the entire verification space with a sufficiently high confidence.

SUMMARY OF RESULTS

A small initial training dataset may not contain any failure, which results in an initial lousy probabilistic model as illustrated in Fig. 1. To address this challenge, we propose to iteratively improve the model accuracy through active learning with the goal of approaching rare failure regions under a limited data budget (Fig. 1). Active learning selects optimal sampling locations on-the-fly and directs re-training of the machine learning model across multiple iterations. We explore two active learning approaches: 1) max variance learning to reduce model uncertainty based on max variance values of model prediction, and 2) a novel formally-guided approach aiming at discovery of rare failure regions. HFMV intelligently and iteratively reduces uncertainty of the learning model by a proposed formally-guided active learning strategy and discovers potential rare failure regions in complex high-dimensional parameter spaces. We compare HFMV with the Monte Carlo (MC) method and Scaled-Sigma Sampling algorithm (SSS), a state-of-the-art smart statistical sampling technique.

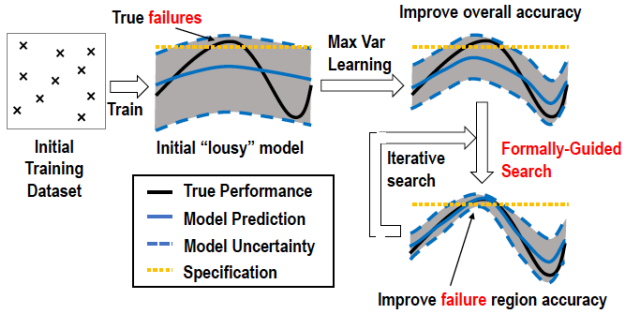

Figure 1. Proposed actively learning.

We consider an amplifier, DC-DC converter, and LDO subjected to 15, 44, and 60 transistor-level process variations, and with a number of specifications, respectively in Table 1. As seen from Table 1, the numbers of simulation samples used by HFMV are significantly lower than SSS. HFMV can hit the first true failure point using 600 to about 900 samples. Yet, SSS cannot find any true failure in the bounded parameter space. The scalability of MC is even worse.

Table 1. Comparison on failure detection. # Samp: # of training (simulation) samples used by each method; # 1st Fail Hit: # of samples used for finding the first true failure by HFMV; # Failure: # of failures found in the bounded parameter space.

Spec.		Target	HFMV			SSS	
			# Samp	# 1st Fail Hit	# Failure	# Samp	# Failure
Amp	GBW	5MHz	1,000	600	396	9,000	0
DCDC	OA	10.0%	1,300	600	312	9,000	0
	OS	1.00%	600	600	85	9,000	0
	RS	0.6mV	600	600	87	9,000	0
	PE	80.00%	1,000	600	275	9,000	0
LDO	QC	20mA	896	600	140	9,000	0
	US	100%	1,897	897	381	9,000	0
	LR	80%	1,618	599	382	9,000	0

Keywords: machine learning, formal verification, hybrid verification, analog and mixed-signal

INDUSTRY INTERACTIONS

Intel, Texas Instruments

MAJOR PAPERS/PATENTS

[1] H. Hu, Q. Zheng, Y. Wang, and P. Li, "HFMV: Hybridizing Formal Methods and Machine Learning for Verification of Analog and Mixed-Signal Circuits," IEEE/ACM DAC, 2018.

TASK 2712.005, AUTOMATED CROSS-LEVEL VALIDATION AND DEBUG OF MIXED-SIGNAL SYSTEMS IN TOP-DOWN DESIGN: FROM PRE-SILICON TO POST-SILICON

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SIGNIFICANCE AND OBJECTIVES

The objective of this work is to evaluate the use of contemporary reinforcement learning tools within a framework for top-down design verification and post-silicon validation. Its significance is in the potential for greater economy of simulation resources during test design and application.

TECHNICAL APPROACH

Our approach is to formulate test creation for verification and validation as a Markov decision process (MDP) and then adapt techniques from the cutting edge of reinforcement learning (RL) research to train an autonomous actor to create high performance tests. Similar to an objective function in an optimization, we define a reward function and the RL algorithms produce an actor which can design tests which maximize reward. The major benefits over explicit optimization are twofold: 1) many RL algorithms converge on global optima, 2) RL actors have memory and can dynamically react to changes in the circuits underlying their environment.

SUMMARY OF RESULTS

Performance throughout training of an RL actor is shown in Figure 1. A more in-depth look at convergence of off-the-shelf differential evolution (DE) algorithm is given in Figure 2 and reveals a pitfall: in several independent trials of the DE algorithm, we observe a high variance and a majority of the attempts converge on a poorer solution than deep Q-network (DQN). This is a result of the lack of global convergence of DE.

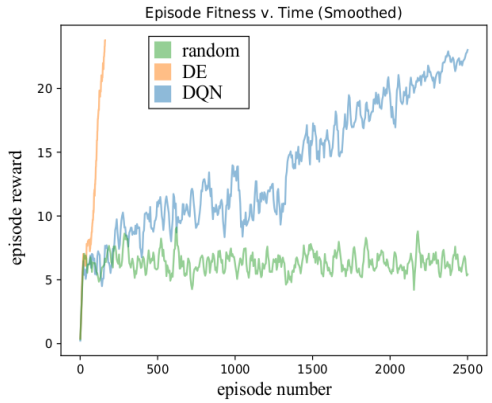

Figure 1. DQN actor performance compared to random stimulus and differential evolution stimulus.

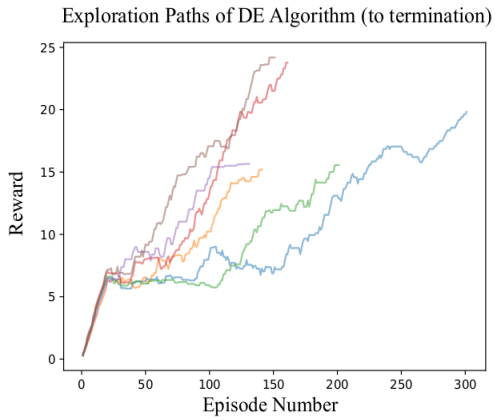

Figure 2. Several independent trials of differential evolution revealing variance in convergent solution.

Our work suggests that deep reinforcement learning provides a very powerful complement to less intensive tools like differential evolution and Monte Carlo stimulus generation. While DQN is able to ultimately outperform the other methods, it comes at the cost of simulation time. The fundamental characteristic of RL and deep RL generally, is their dependence on large volumes of data. There are two ways to generate this data and they are: 1) power up a physical circuit and apply stimuli, or 2) build a simulation model.

We will continue this work into the future, continuing to look at broader classes of circuits and varying degrees of bug magnitude and nature. There are classes of circuits which require continuous input, and for these, DQN is ill-suited. By nature, DQN selects actions from a discrete set of available actions – attempting to discretize circuit inputs to even modest levels will result in an explosion in the number of parameters in the network.

Keywords: design validation, post-silicon validation, ATPG, AMS verification

INDUSTRY INTERACTIONS

Intel, Texas Instruments

MAJOR PAPERS/PATENTS

[1] B.Muldrey and A. Chatterjee, “Mixed-Signal Design Validation Using Reinforcement Learning,” International Test Conference, 2018, submitted.

TASK 2712.007, HIGH-RESOLUTION LOW-VOLTAGE HYBRID ADCS FOR SENSOR INTERFACES

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SIGNIFICANCE AND OBJECTIVES

The goal of this research is to extend the state-of-the-art of high resolution sensor interface ADCs through research and development of a hybrid ADC architectures, that are also easy to drive.

TECHNICAL APPROACH

This new class of converters will facilitate and improve sensing and IoT applications. These needs are currently unmet since state-of-the-art low-power ADCs are difficult to drive (i.e. requiring filter and input buffer), and are limited in either resolution or power consumption. ADCs for sensors are often implemented as SAR or oversampling ADCs. SAR ADCs achieve excellent energy efficiency but are limited to moderate resolution. Calibration adds complexity and may need to be adjusted continually with temperature and supply changes. Sigma-Delta ADCs and incremental converters can achieve higher resolution but are constrained by the requirements of the op-amps and switches.

SUMMARY OF RESULTS

In this research, we are developing and demonstrating new 14-16b, low power ADCs for sensors. The goal is also to make the ADC easy to drive. Power consumption of the driver and references will be considered in addition to the ADC power to achieve the best overall system performance. This research addresses the needs for very energy efficient digital and analog circuits, a rea efficient analog/RF/Clocking/IO design in scaled digital technologies, and low voltage digital and analog circuit design including moderate inversion and weak inversion regions of operation.

Although tremendous progress has been made on the energy efficiency of ADCs, ADCs are still a bottleneck in many systems because they are difficult to drive and suffer from many other practical limitations. SAR ADCs have impressive reported efficiency, however, the large switched capacitive input in a moderate/high resolution SAR necessitates a highly capable ADC driver which itself consumes considerable power. For example, the highly efficient TI OPA835 (-70dB HD2) SAR ADC driver consumes 1mW, which dwarfs the ADC power. Moreover, SAR ADC energy efficiency drops steadily as the ADC ENOB increases above 10b. The anti-alias filter is another huge challenge to the practical implementation of many systems. If a near-minimum sampling speed is selected to minimize ADC power, then the resulting sharp cutoff anti-alias filter can easily be more challenging to design than the ADC itself.

ADCs for sensors are often implemented as SAR or oversampling ADCs. SAR ADCs achieve excellent energy efficiency, but are limited to moderate resolution. Calibration adds complexity, and may need to be adjusted continually with temperature and supply changes. Sigma Delta ADCs and incremental converters can achieve higher resolution, but are constrained by the requirements of the op-amps and switches.

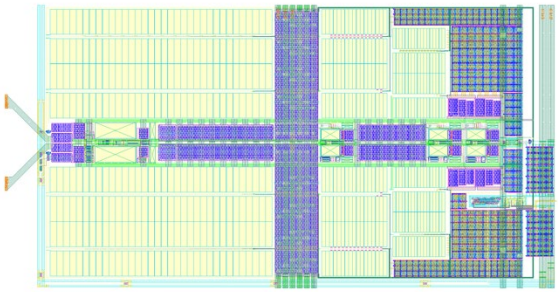

Figure 1. Protoype ADC in 40nm CMOS.

Oversampled discrete time converters have the advantage of relaxing the specifications of the anti-alias filter. Sigma Delta converters are also relatively efficient at high ENOB. Nevertheless, discrete-time Sigma Delta ADC in common with SAR ADCs and all discrete time ADCs, present a switched-capacitor input which is difficult to drive. Besides the switched load, a further challenge is the input side switch, which often limits the linearity.

Keywords: sigma delta, ADC, sensor, IoT

INDUSTRY INTERACTIONS

Texas Instruments, Intel, ARM

MAJOR PAPERS/PATENTS

TASK 2712.010, RINGAMP-ASSISTED CIRCUITS/TECHNIQUES AND NEXT-GENERATION RINGAMPS

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SIGNIFICANCE AND OBJECTIVES

Owing to the degradation of key analog parameters, such as intrinsic gain and supply voltage, many state-of-art systems use digitally-assisted analog circuits. One example is the use of digital low drop out regulators to achieve scalable voltage regulation circuits. However, efficiency improvements can still be realized with improved analog circuits.

TECHNICAL APPROACH

The approach for this work is to improve the scalability and power efficiency of analog low drop out (LDO) regulators by utilizing ring amplifiers. A recent and prominent scalable circuit, the ring amplifier is a three-stage inverter based dynamic amplifier that can drive large capacitive loads with very low quiescent current. Since their inception, ring amplifiers are used mainly in switched capacitor systems to achieve faster settling time and high accuracy. The use of ring amplifiers for LDOs remains unexplored. Ring amplifiers can be used to achieve faster settling time and to improve the driving capability of the error amplifier in an LDO.

SUMMARY OF RESULTS

Fig. 1 shows the basic schematic of a capacitor-less LDO which consists of a pass transistor and a ring amplifier as the error amplifier. The aim of the feedback loop is to regulate the output voltage of the LDO irrespective of the changes in the load current. Faster settling time is required from the error amplifier to accommodate for sudden changes in the load current. In addition, small quiescent current consumption is required from the error amplifier, while still being able to drive a large capacitive load offered by the pass transistor.

By analyzing the transient currents and voltages at each node in the LDO loop in Fig. 1, it can be observed that the transient voltage at the input of the error amplifier is similar to that of the virtual ground node in a switched capacitor amplifier. This can result in the best use of the dynamic operation of the ring amplifier. Thus, the large capacitive load at the gate of the pass transistor can be driven by the ring amplifier with a low quiescent current.

Fig. 2 shows the transient response of the LDO for a current step from 1mA to 100mA and vice versa. The LDO is designed with a 1.1V supply voltage and a drop out voltage of 0.1V in a 0.18um CMOS process. The settling time of the LDO is less than 500ns with a quiescent current of 10uA. As the ring amplifier utilizes a simple inverter based structure, this work demonstrates a scalable analog LDO architecture.

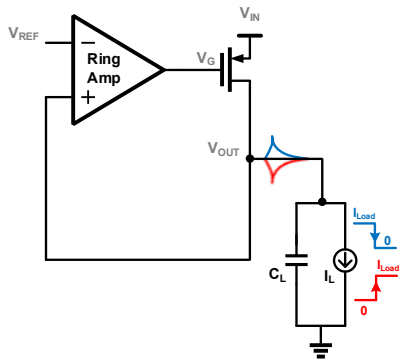

Figure 1. Ring amplifier based LDO.

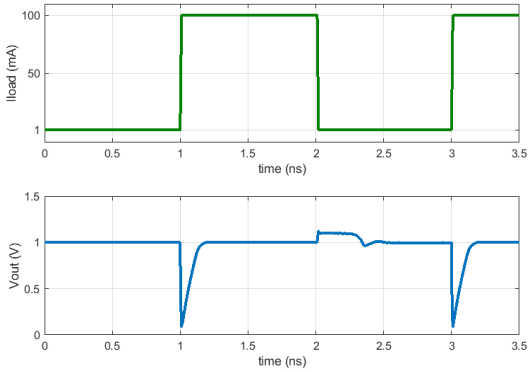

Figure 2. Transient response of the LDO.

Into the future, this ring amplifier based LDO is expected be prototyped in silicon and evaluated. Other work plans include the design of a ring amplifier based integrator to be utilized in a high resolution ADC architecture.

Keywords: ring amplifier, linear-drop-out regulator, scaling

INDUSTRY INTERACTIONS

Texas Instruments, Intel, NXP

MAJOR PAPERS/PATENTS

[1] J. Muhlestein *et al.*, "A 73dB SNDR 20MS/s 1.28mW SAR-TDC using hybrid two-step quantization," CICC May-2017.

[2] S. Leuenberger *et al.*, "A 74.33 dB SNDR 20 MSPS 2.74 mW pipelined ADC…," CICC May-2017.

TASK 2712.011, ROBUST RELIABLE AND PRACTICAL HIGH PERFORMANCE REFERENCES IN ADVANCED TECHNOLOGIES

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DEGANG CHEN, IOWA STATE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

The objectives are to develop circuits that express the bandgap voltage at the output with a single electrical trim at standard test temperature and to adapt the all-electrical trim to an on-demand run-time trim without requiring external test equipment. Significance is in development of references with lower temperature dependence.

TECHNICAL APPROACH

Our approach to the first objective is to revisit the issue of expressing the bandgap voltage at the output of a circuit directly rather than focusing on expressing the bandgap voltage only at an inflection temperature. Our approach to meet the second objective will be to identify what additional information can be obtained from correlated reconfiguration of a circuit in which the bandgap voltage and temperature are tightly intertwined in the device characteristics and design variables. Two test chips will be designed to obtain experimental verification of the performance of the new precision reference circuits.

SUMMARY OF RESULTS

A new method of designing voltage references using a Bandgap Separator and a Thermal Function Generator, depictd in Figure 1, is proposed. In contrast to most existing bandgap reference circuits that focus on forcing the thermal derivative of the output voltage to vanish at an inflection temperature, and thereby obtain an output proportional to the bandgap voltage at the inflection temperature, the proposed approach offers potential for expressing the bandgap voltage of silicon, a physical constant, at the output for all temperatures. Based upon widely-used models for the temperature dependence of the pn-junction, existing bandgap circuits ideally provide a TC of 10 ppm/^{o}C over a 100^{o}C range. With the same device models, the proposed approach offers potential to improve the performance to the 0.1 ppm/^{o}C range.

A preliminary circuit has been designed to extract the bandgap voltage. Using the existing models for the pn junction that are embedded in the SPECTRE model of the BJT, simulation results suggest performance at approximately the 0.25ppm/^{o}C level over the same 100^{o}C range with a single trim is possible [1]. A test circuit has been designed in a 65nm UMC process and will be tested after fabrication is complete.

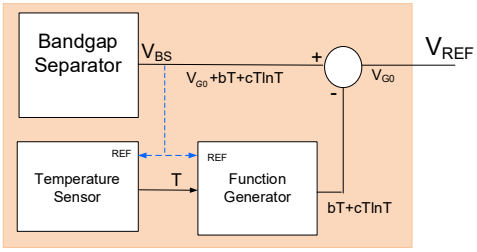

Figure 1. Diagram of Precision Voltage Reference using Bandgap Separator and thermal Function Generator.

Considerable discrepancy exists between simulated results and measured results in several basic bandgap circuits. A comparison of six of the most popular bandgap circuits has been made. Though the reported experimental results differ significantly, it was shown in this comparison that all have an output voltage that is of the form a+bT+cTlnT where a,b, and c are temperature independent and, furthermore, all have identical normalized temperature coefficients if identical device models are used.

In the coming year, emphasis will be placed on understanding the discrepancy between simulated results and measured results reported by numerous authors. This discrepancy is likely due to limitations in models of the pn junction and vertical pnp transistor used in commercial simulators such as Spectre. Test circuits have been designed that can be used to investigate device model limitations and incorporate improved device models into both basic bandgap circuits and the precision reference architecuture depicted in Figure 1.

Keywords: bandgap reference, diode model, curvature-compensation, voltage reference, bandgap separator

INDUSTRY INTERACTIONS

Texas Instruments, Intel, NXP

MAJOR PAPERS/PATENTS

[1] Z. Liu et al., “A Voltage Reference Generator Targeted at Extracting the Silicon Bandgap VGO from VBE ,“ ISCAS, May 2017.
[2] Yin, Y., “Performance Characteristics and Design of Voltage References”, MS Thesis, Iowa State University, Aug. 2017.

TASK 2712.014, LEVERAGING CMOS SCALING IN HIGH PERFORMANCE ADCS

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SIGNIFICANCE AND OBJECTIVES

We have fabricated five prototype ADCs with different features: Self-Excess Loop Delay (ELD) compensation Quantizer [1], Digital Correlated-Level Shifting, Flip-Around Single-Cap time-amplifier, 3-step double-noise shaping quantizer and a new multi-loop modulator. The prototype ICs were fabricated. In this report, we will discuss our latest work; a new multi-loop Delta-Sigma ADC.

TECHNICAL APPROACH

The proposed work introduces a new multi-loop modulator based on Sturdy-MASH (SMASH) called Correlated Double-Loop (CDL) Modulator. This structure simplifies the overall loop filter. The direct quantization error extraction which was an inetivable part of SMASH is removed. Furthermore, the second loop is DAC free, reducing the area and complexity. This ADC is currently under fabrication in 65nm CMOS.

SUMMARY OF RESULTS

The proposed CDL-DSM is shown in Fig. 1. The low distortion structure is used in the first stage, and the output of the first stage loop filter is fed to the next stage without using the quantization error (qe) extraction DAC. Also, the feedback DAC (DAC2) of the second stage is removed. The loop filter transfer function LF1 is set to H1 and LF2 is set to H1+H1H2. Setting H1=H2 makes the two filters correlated and the proposed CDL-DSM and the SMASH can have the same characteristics. Therefore, the proposed CDL-DSM can achieve the same benefit of the SMASH, analog circuit insensitivity, while it simplifies overall design by removing all the DACs of the second loop. The challange of the qe-extraction DAC significantly complicates the timing requirement in a continuous time (CT) implementation. The CT-SMASH needs to make the decision of the first stage, feed the qe to the next stage, make the decision of the second stage, and feed the digital output back to the modulator within one cycle. Therefore, it increases the overall delay from the quantizer to the loop filter. In order to compensate the increased loop delay, a complicated timing circuitry is required.

The proposed CDL-DSM can also be implemented in CT fashion. Since the CT-CDL-DSM does not require qe-extraction DAC, the clock circuitry can be simplified and only complimentary clock (ϕ and $\bar{\phi}$) can be used. The ELD of the CT-CDL-DSM can be compensated by using the traditional methods, an additional DAC around the quantizer, differentiated DAC to the last integrator, and etc. It can be noted that no ELD DAC is required for the second loop as shown in Fig. 2.

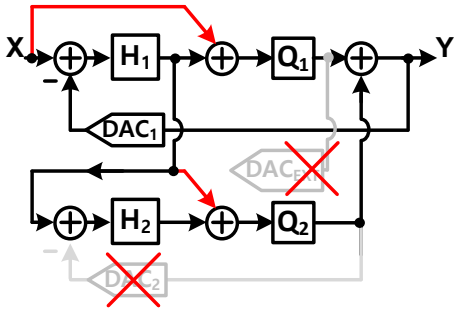

Figure 1. Simplified diagram of the proposed CDL-DSM in comparison with SMASH [2].

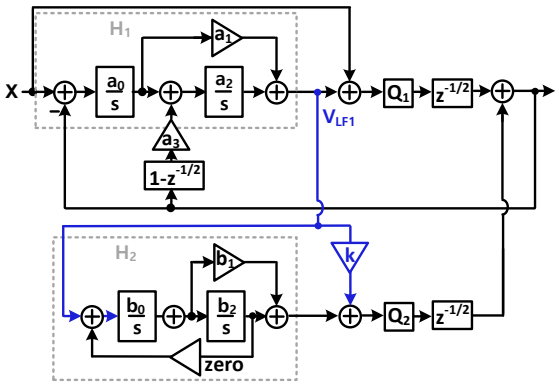

Figure 2. Architecture level of the under fabrication prototype CDL Delta-Sigma ADC.

Order	BW	SNDR	Power
4	20M	78	10 mW

Keywords: delta-sigma, quantization, analog circuits, DAC, analog-to-digital converter

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] C. Han et al, "A CT Delta-Sigma Modulator with Self-ELD Compensated Quantizer," CICC 2018

[2] N. Maghari et al, "Sturdy MASH Δ-Σ Modulator," IEE Electron. Lett., vol. 42, pp. 1269-1270, Oct. 2006.

TASK 2712.020, LOW-POWER MOSTLY DIGITAL TIME-DOMAIN DELTA-SIGMA ADCS FOR IOT

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SIGNIFICANCE AND OBJECTIVES

The aim of this project is to develop low-power, delta-sigma ADCs for IoT. A purely VCO-based highly digital architecture is investigated in this project. The target is to design high-order, digital delta-sigma ADC with power consumption less than 100μW.

TECHNICAL APPROACH

A modified digital phase-locked loop (DPLL) architecture is used for the proposed ADC design. The analog input perturbs the digitally controlled oscillator (DCO) phase and the DPLL changes the DCO control word to cancel out the phase perturbation. Thus, the DCO control word acts as a quantized representation of the analog input. Ring oscillators are used as DCO and DPLL loop filter, resulting in highly digital architecture and high-order quantization noise shaping. The merits of the proposed ADC are a) no nonlinearity calibration b) excess loop delay can be compensated without requiring an auxiliary DAC c) inherent DAC mismatch shaping.

SUMMARY OF RESULTS

A prototype ADC was fabricated in a 65nm CMOS process and characterized. The active core occupies an area of 0.06mm^2. The test chip consumes 1mW power from a supply of 1.2V while running at a sampling frequency of 205MHz. 17-stage differential VCOs were used for this design. The large power consumption was largely because of the static current in the NMOS current steering DAC which is drawn away from the VCO. The power can be reduced substantially by using a PMOS current steering DAC and scaling down the DAC current. Preliminary post-layout simulations for our next chip indicate that we can reduce the power to less than 80μW while maintaining the signal-to-noise ratio.

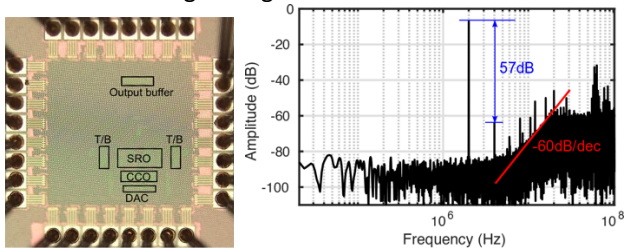

Figure 1. Prototype third-order VCO-ADC in 65nm CMOS and measured spectrum.

The ADC was tested by applying a differential current of 70μA (peak-to-peak) which is -7dBFs. The current was supplied using 2 off-chip resistors. Unfortunately, mismatch in the resistors limited the dynamic range of the ADC and also led to even-order distortion tones seen in the measured spectrum. For the next prototype, we will use precision resistors and DEM to remove the limitations arising out of mismatches of off-chip resistors.

The parasitic capacitances from the printed circuit board and chip packaging created a front-end passive integrator which resulted in third-order noise shaping. The ADC input referred noise is dominated by the thermal noise. Based on simulation results, the input-referred thermal noise of the ADC is 22nA which agrees well with our measurement results. Table 1 summarizes the performance of the first test chip. The schreier FoM is comparable to that of existing CT high-order purely VCO-ADCs.

For the next report period, we will prototype a modified version of the chip to significantly reduce power consumption as well as improve dynamic range. The overall objective of this project is to ultimately develop a higher-order (>3) VCO-ADC with large dynamic range.

Table 1. Performance Summary.

Tech (nm)	Fs (MHz)	BW (MHz)	Power (mW)	SNDR (dB)	FoM_s(dB)
65	205	2.5	1	56	150

Keywords: ADC, VCO, DPLL, delta-sigma, noise-shaping

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] V. Prathap, S. T. Chandrasekaran, and A. Sanyal, "2nd-Order VCO- based CT ΔΣ ADC architecture," MWSCAS, 2017.

TASK 2712.023, ULTRA-LOW-POWER COMPRESSIVE SENSING TECHNIQUES FOR IOT APPLICATIONS

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SIGNIFICANCE AND OBJECTIVES

In order for IoT sensors to be widely deployed as expected, an ultra-low-power circuit platform with nominal performance has to be first achieved. To significantly reduce power consumption, and also hardware cost, the potential of compressive sensing is studied and the theory is applied at the circuit level.

TECHNICAL APPROACH

To lower the ADC conversion rate and thus lowering digital data transmission rate and overall sensor front-end power comsumption, compressive sensing theory is implemented on the circuit level in a fully passive manner. The random demodulator architecture of compressive sensing is combined with a SAR ADC sampling process with a minimal increase of circuit complexity and power consumption. For a multi-channel sensor front-end, a spatial compression is achieved to convert multi-channel signals by one ADC with the sampling rate of one channel.

SUMMARY OF RESULTS

A single-channel compressive sensing SAR ADC is implemented, tested, and published. [1] In CS mode, the ADC is tested with discrete tone signals as well as an 1s-long speech signal as an example of real world signals. With proper selection of a reconstruction algorithm, a bandwidth occupancy of 8.2% is achieved with peak post-reconstruction SNDR of 61dB and the peak FoM of 5.5fJ/conv-step, both being the state-of-the-art performance.

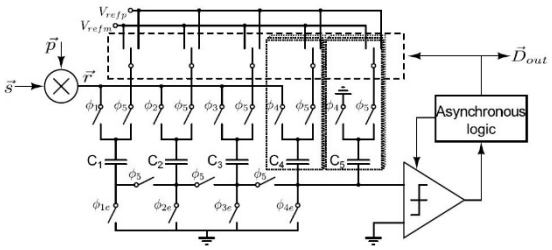

Figure 1. The architecture for single-channel CS SAR ADC.

The single-channel CS SAR achieves a conversion rate reduction and digital data compression by using compressive sensing. And thus achieves power reduction. However, for multi-channel signal acquisition, hardware cost is also a major aspect to be considered. The proposed multi-channel CS SAR ADC takes advantage of compressive sensing and uses a single SAR ADC sampled at the Nyquist rate of one channel to convert multi-channel sparse signal simultaneously. Compared to conventional multi-channel ADCs, the proposed architecture not only saves power and hardware cost, but also avoid such problems as timing skew, offset mismatch, and gain mismatch among channels. The multi-channel CS SAR ADC is implemented in a 130nm CMOS technology. In CS mode, the ADC is able to achieve a max total channel occupancy of 41%. The effectiveness of different reconstruction algorithms is also studied. Convex optimization based algorithm SL0 achieves the best reconstruction robustness and accuracy. Among the greedy method based algorithms, SOMP shows its capability of efficiently reconstructing multi-channel signals when the correlation is high.

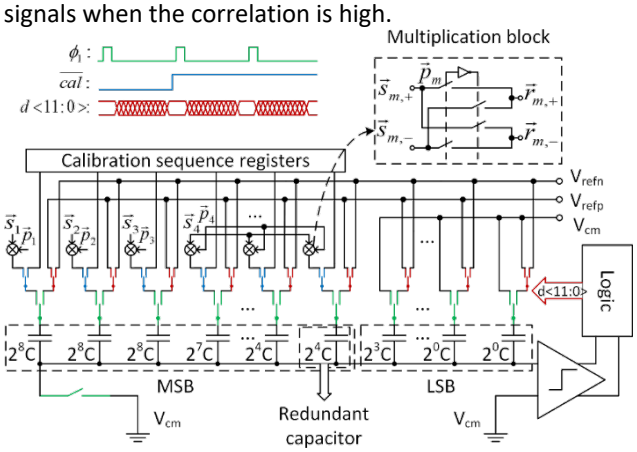

Figure 2. The architecture for multi-channel CS SAR ADC.

For future works, a passive residue voltage boosting technique to relax the requirement on comparator noise is being developed and will be applied on future CS SAR ADCs to increase the compressive ratio or number of channels. A time-stampless non-uniform sampling technique is being studied and its circuit implementation is scheduled.

Keywords: compressive sensing, wireless sensor front-end, IoT applications, ultra-low-power data converter, signal processing

INDUSTRY INTERACTIONS

Texas Instruments, Intel, ARM

MAJOR PAPERS/PATENTS

[1] W. Guo et al., "A Fully Passive Compressive Sensing SAR ADC for Low-Power Wireless Sensors," in IEEE Journal of Solid-State Circuits, vol. 52, no. 8, pp. 2154-2167, Aug. 2017.

TASK 2712.025, REDUCTION OF LOW FREQUENCY NOISE IMPACT IN NANO-SCALE CMOS CIRCUITS

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SIGNIFICANCE AND OBJECTIVES

This project is investigating approaches to incorporate an on-chip measurement capability and post-fabrication configurable minimum size transistor arrays for reducing the low frequency noise impact in RF and analog circuits. This approach may be more effective for reducing low frequency noise impact than increasing the transistor size.

TECHNICAL APPROACH

Using transistors with lower noise through post fabrication selection, and approaches for integrating a highly sensitive noise measurement circuit based on a frequency synthesizer commonly found in RF and millimeter wave transmitter and receiver will be investigated. Intelligent search algorithms will be applied to select the combinations with low frequency noise with the minimum number of measurements. Approaches to increase the operating frequency of VCO will be investigated and the factors that limit the maximum operating frequency will be understood. In addition, approaches to extend this technique to other circuits will be investigated.

SUMMARY OF RESULTS

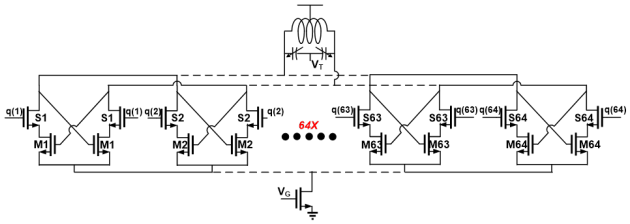

Figure 1. 4.3-GHz voltage controlled oscillator using an array of cross-coupled NMOS transistors.

The number of intended dopants and un-intended defects in a minimum sized device is reduced with technology scaling. One missing dopant or having an additional defect can dramatically increase or decrease the threshold voltage, current and noise. A 4.3-GHz voltage controlled oscillator (VCO) that embraces the variability of nano-scale transistors to reduce its phase noise by taking advantage of reduced low frequency noise of some minimum sized transistors with a fewer defects or traps through post-fabrication selection is reported [1]. The VCO (Fig. 1) uses an addressable array of cross-coupled minimum size NMOS transistor pairs for post fabrication selection and is fabricated in 65-nm CMOS. An algorithm based on Hamming distance using the phase noise measurements of ~1,500 combinations was used to identify the combinations that have record phase noise of -130dBc/Hz at 1-MHz offset from a 4.3-GHz carrier, while consuming 5.2 mW from a 1-V supply. The noise was measured using an external instrument.

To make this technique practical, an affordable and sufficiently rapid on-chip measurement technique for the phase noise that can resolve noise below -130dBc/Hz for a 4.3-GHz carrier is being investigated. Fig. 2 shows a phase locked loop including hooks for measurements of phase noise which has been taped out in a 65-nm CMOS process. This technique will also be applicable to other circuit elements such as a receiver mixer and a baseband amplifier. Applicability of this technique to these circuits as well as at higher operating frequencies will be investigated.

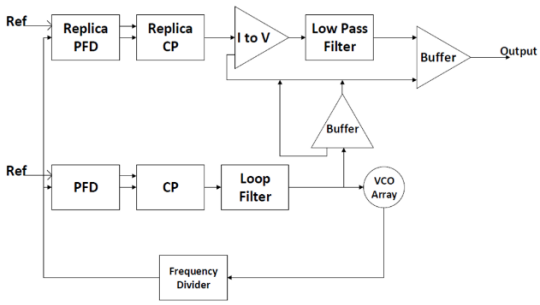

Figure 2. Phase locked loop incorporating a 4.3-GHz voltage controlled oscillator using an array of cross-coupled NMOS transistors and hooks for on-chip phase noise measurements.

Keywords: low frequency noise, on-chip noise measurements, post-fabrication selection

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] A. Jha et al., "-197dBc/Hz FOM 4.3-GHz VCO Using an Addressable Array of Minimum-Sized NMOS Cross-Coupled Transistor Pairs in 65-nm CMOS," *IEEE Symposium on VLSI Circuits*, pp. 214-215, June 2016, Honolulu, Hi.

TASK 2712.031 ADAPTIVE TRIMMING AND TESTING OF ANALOG/RF INTEGRATED CIRCUITS (IC'S)

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SIGNIFICANCE AND OBJECTIVES

The goal of this task is to develop an adaptive methodology that will speed-up the time-consuming V_{min} search without affecting the yield. The V_{min} search is a post-fabrication process that is performed on each device in order to identify its optimal operating voltage. The additional constraint of power consumption has been introduced compared to prior adaptive solutions.

TECHNICAL APPROACH

To achieve the above objective, a machine learning-based system will have to predict the minimum V_{seed} per wafer in order to minimize the total number of search steps needed for all devices on that wafer. A regression model is trained that predicts the optimal V_{seed} for each wafer as a function of the e-test measurements. The training features have been limited to the e-test measurements to simplify the test-floor logistics that would otherwise hinder industrial integration. Furthermore, considerable effort is made in order to bias the prediction error towards lower values, since the search is usually performed in a single direction.

SUMMARY OF RESULTS

An industrial dataset from 178 wafers was provided to us by our industrial collaborators. For each device in the dataset, V_{min} search was performed and the resulting voltages were recorded. First, we had to assess whether there exists a level of variability on the wafer-level V_{seed} to justify development of an adaptive solution.

Figure 1 shows the histogram of the V_{seed} measurements as computed by the provided data. The red and blue vertical lines represent the low and high specification limits for the $V_{min.}$ As shown there is enough variability of V_{seed} with 30 unique values in that range. The extent of the possible savings depends on various test-floor parameters, such as the size of the step by which the voltage is changed during the search and the time it requires for each such iteration. It is also worth noting that the default V_{seed} is very conservatively defined for the provided dataset. This is commonly the case as test engineers set those values to accommodate process shifts that can happen over time, but it leads to higher test times that can only be eliminated by implementing an adaptive methodology.

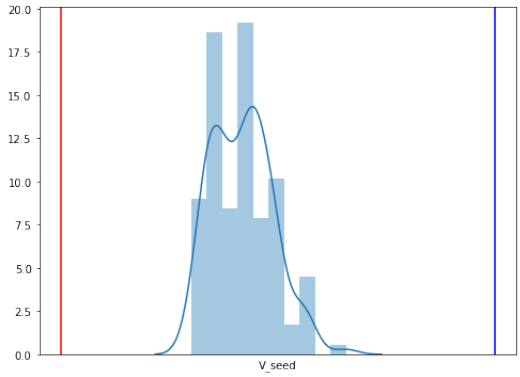

Figure 1. Distribution of V_{seed}.

To determine whether there is any correlation between E-test and the optimal seed for each wafer, we trained a Multivariate Adaptive Regression Splines (MARS) regression model.

The effectiveness of such model was evaluated by performing a leave-one-out experiment for all wafers in the dataset. Figure 2 shows the error distribution expressed as percentage of the specification range. As we can note, the error is normally distributed, and the majority of the wafers was predicted with less than 10 % error from the actual optimal seed.

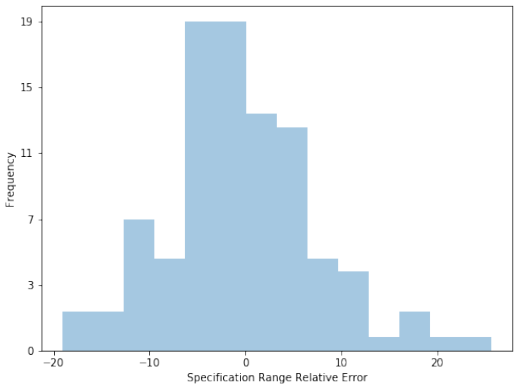

Figure 2. Distribution of error on V_{seed} prediction model.

Keywords: trimming, adaptive test, post-silicon calibration

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

TASK 2810.007, FULLY INTEGRATED PHASE NOISE CANCELLATION TECHNIQUES

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SIGNIFICANCE AND OBJECTIVES

This research will explore techniques to reduce phase noise based on delay line discriminators using on-chip integrated delay components. This will allow higher data rate communication for both wired, traditional wireless, and emerging spatially multiplexed systems.

TECHNICAL APPROACH

We propose to build phase noise cancellation circuitry that can be cascaded after the clock source in a flexible manner to reduce the impact of phase noise and spurs. We will explore the design and implementation of phase noise cancellation circuits that are able to reduce phase noise by >20dB per stage.

SUMMARY OF RESULTS

Two techniques for spur and phase noise cancellation are proposed and tested. First, we proposed a delay-and-interpolate method that generates notches against input clock spurs, as shown in the top portion of Fig. 1. In addition, the phase noise is extacted by the delay-line discriminator, and then a feed-forward loop is used to cancel out input phase noise, which are shown in the bottom portion of Fig. 1.

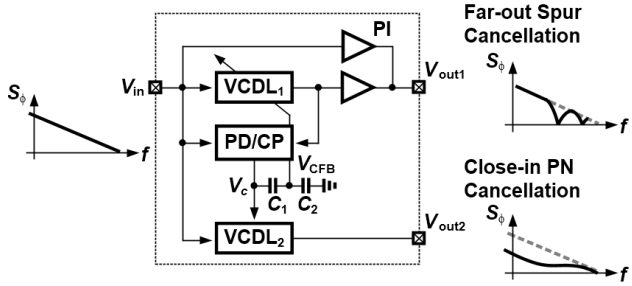

Figure 1. The architecture for both far-out spur and close-in phase noise cancellation.

The architecture above has been fabricated in 65nm CMOS technology, which occupies 0.3×0.25mm^2 core area and consumes a total power of 11mW. To facillite testing, the spurs and white noise waveforms are generated externally and then used to modulate the control line of a 1-GHz test voltage-controlled oscillator (VCO) on-chip to mimic a low power VCO with relaxed performance. The measurement result of phase noise cancellation is demonstrated in Fig. 2(a). The cancellation applies from 4MHz to 200MHz offset frequency and achieves a maximum of 25dB cancellation at 40MHz offset. The RMS jitter can be improved from 74.7ps to 64.6ps, with a 1M~200MHz integration bandwidth. Additionally, the delay-and interpolate method for spur cancellation is also verified. Fig. 2(b) shows the results of spur cancellation. In this design, the delay line is set to be 2ns, which generates notches at 250MHz (1/2T) and 750MHz (3/2T) offset frequency. The spurs at those two offset frequencies can be rejected by 15dB.

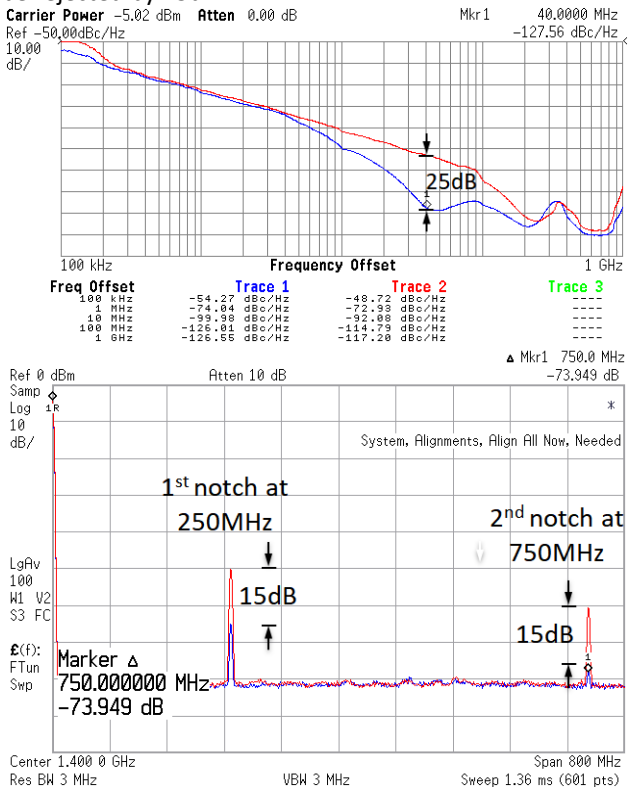

Figure 2. (a) Phase noise is cancelled from 4MHz to 200MHz offset with maximum cancellation of 25dB on a 1-GHz clock. (b) Far-out spurs at 250MHz and 750MHz offset frequencies can be cancelled up to 15dB by the notches.

Keywords: spur, phase noise, cancellation, notches, and delay-line discriminator

INDUSTRY INTERACTIONS

Intel

MAJOR PAPERS/PATENTS

[1] Y. Li et al., "On-chip spur and phase noise cancellation techniques," Digest of Asian Solid-State Circuits Conference, Nov. 2017

TASK 2810.009, MIXED-SIGNAL BUILDING BLOCKS FOR ULTRA-LOW POWER WIRELESS SENSOR NODES

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DAVID BLAAUW, UNIVERSITY OF MICHIGAN

SIGNIFICANCE AND OBJECTIVES

This project develops novel and state-of-art performing ultra-low power mixed-signal circuits, suitable for IoT systems. This includes timekeeping circuits, amplifiers, and CMOS-based sensors.

TECHNICAL APPROACH

The most challenging ultra-low power circuit components are mixed-signal circuits such as timers, clock sources, sensing and interface circuits (e.g., temperature sensors and low-noise amplifiers). Some of these cannot be duty cycled (e.g., timers), while others require both low noise and low power (e.g., amplifiers), which are traditionally mutually exclusive. This work proposes new ULP designs for: 1) crystal oscillator based real time clocks (RTCs), 2) temperature-compensated wakeup timers, 3) temperature sensors, and 4) front-end low-noise amplifiers.

SUMMARY OF RESULTS

A challenge in the design of on-chip wake-up timers for compact wireless sensor nodes is to achieve high timing accuracy over temperature and supply voltage variation within an ultra-low power budget. We propose a gate-leakage-based frequency locking timer with first- and second-order cancellation achieving 260 ppm/°C from −5 to 95°C. The timer consumes 224 pW at 90 Hz output frequency with 0.93%/V supply voltage dependence in the 1.1-3.3 V range. Figure 1 shows the overall circuit topology, including voltage reference generators that serve to compensate for temperature dependency.

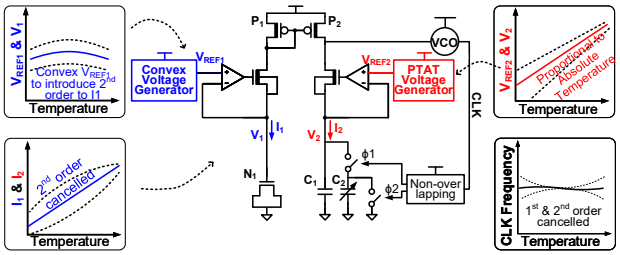

Figure 1. Overall structure of the proposed timer.

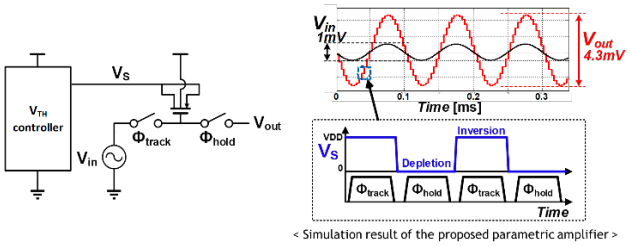

Figure 2. The architecture of the parametric amplifier.

This project also developed a 2.2 noise efficiency factor (NEF) instrumentation amplifier for neural recording applications. A parametric amplifier based on the MOS C-V characteristic is designed as a pre-amplifier stage, lowering the input referred noise of the following stages by 3.4X. Sampling noise is minimized by oversampling the input signal and switching power is reduced by adopting an 8-phase soft-charging technique. Figure 2 shows the architecture of the parametric amplifier.

Keywords: CMOS, low-noise amplifiers, mixed-signal

INDUSTRY INTERACTIONS

Intel

MAJOR PAPERS/PATENTS

[1] J. Lim, T. Jang, M. Saligane, M. Yasuda, S. Miyoshi, M. Kawaminami, D. Blaauw, and D. Sylvester, “A 224pW 260ppm/°C gate-leakage based timer for ultra-low power sensor nodes with second-order temperature dependency calibration,” *IEEE Symposium on VLSI Circuits*, 2018.

[2] T. Jang, K. Choo, J. Lim, S. Nason, J. Lee, S. Oh, S. Jeong, C. Chestek, D. Sylvester, and D. Blaauw, “A 2.2 NEF neural-recording amplifier using discrete-time parametric amplification,” *IEEE Symposium on VLSI Circuits*, 2018.

TASK 2810.011, MICRO-POWER ANALOG-TO-DIGITAL CONVERTERS FOR SENSOR INTERFACES

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SIGNIFICANCE AND OBJECTIVES

Sensors play an important role in medical, IoT, security and other applications. Analog-to-digital converters (ADCs) are crucial components of their interfaces. In many cases, such as battery- or harvested-power sensors, power needs to be minimized. This project develops novel ADCs needing only very small amounts (μW) of power.

TECHNICAL APPROACH

We shall investigate the potential of our existing and future innovations to obtain micro-power data converters that exceed the present state of the art. We plan to utilize our novel schemes (such as parallel-counting IADCs, noise-shaping SAR ADCs) to achieve outstanding performance in terms of resolution, speed and power saving. We also plan to use our new design technique for "pseudo-pseudo differential" circuits (Tao He et al., CICC, 2017) to reduce power dissipation in all ADCs.

SUMMARY OF RESULTS

This project has been active only for two months, and hence only out plans can be discussed at this time. The key projects started include the development of incremental ADCs using micro-power architectures. Specific schemes include successive-approximation-register (SAR) ADCs with higher-order noise shaping, pseudo-pseudo-differential ΔΣ ADCs and parallel-counting incremental data converters. We are also going to investigate circuit-level power reduction schemes, such as charge-assisted and/or dynamically biased operational amplifiers for switched-capacitor integrators.

Some of our recent results in the area of this research, but obtained prior to the start of this project, are illustrated in Figs. 1- 3.

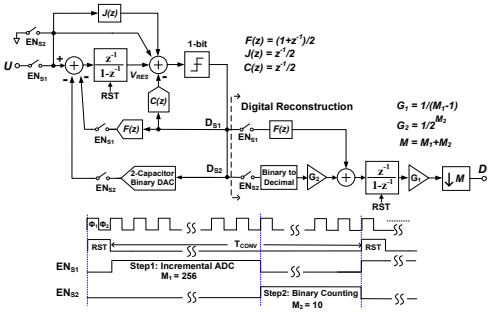

Figure 1. Block diagram of the two-step incremental ADC with binary extended counting.

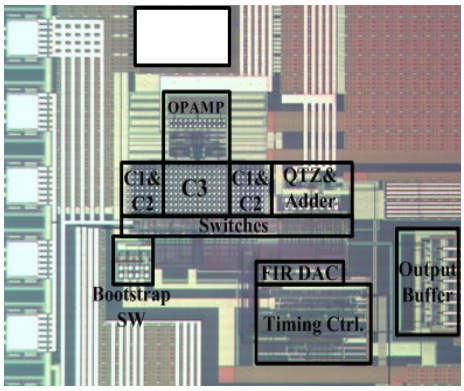

Figure 2. Chip micrograph.

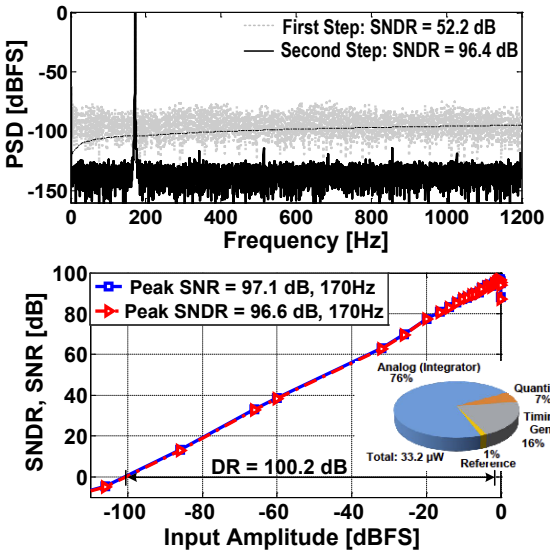

Figure 3. Output spectra and SNDR vs. input curve.

Keywords: sensor interfaces, data converters, micro power circuits, analog-to-digital converters, incremental data converters

INDUSTRY INTERACTIONS

MAJOR PAPERS/PATENTS

[1] He, T. and Temes, G.C. "System-Level Noise Filtering and Linearization," (invited paper) IEEE Custom Integrated Circuits Conf., San Diego, April 2018.

TASK 2810.015, DEMONSTRATION OF 120-GBPS DIELECTRIC WAVEGUIDE COMMUNICATION USING FREQUENCY DIVISION MULTIPLEXING AND POLARIZATION DIVISION MULTIPLEXING

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SIGNIFICANCE AND OBJECTIVES

This project in collaboration with the efforts on transitions and diplexer/combiner, and on low loss dielectric waveguides for operation at 100-400 GHz seeks to demonstrate 120-Gbps Polarization Division Multilexing and Frequency Division Multiplexing (45-GHz bands around 180 and 315 GHz) communication over a 1-m long dielectric waveguide using CMOS circuits.

TECHNICAL APPROACH

The transmitter and receiver architectures will be essentially the same as those demonstrated by Task 1836.152. To excite waves at two different frequency bands with two different polarizations in a dielectric waveguide, transmitters for the 180 and 315-GHz bands will be used to drive a cross dipole. The receivers of two bands will be connected to one of the cross dipoles, while the second dipole will be terminated to reduce reflection. These receivers and transmitters will be used to demonstrate FDM operation. For PDM operation, the receiver will be rotated 90 degrees to pick up signals with the second polarization.

SUMMARY OF RESULTS

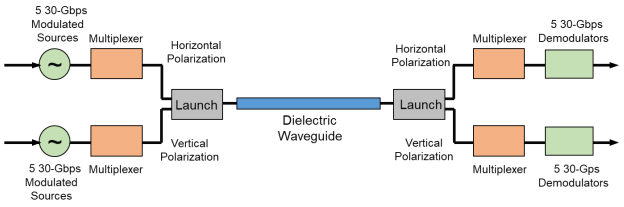

Figure 1. Dielectric waveguide communication system employing both frequency division multiplexing (FDM) and polarization division multiplexing (PDM) proposed to support an aggregated data rate of 300 Gbps [1].

Fig. 1 shows a conceptual diagram of the dielectric waveguide system. It consists of a transmitter, a launch from the transmitter to a waveguide, a waveguide, a launch from a waveguide to a receiver, and a receiver. The system uses five 45-GHz frequency bands spanning 157.5 to 382.5 GHz and supporting two polarization channels for a total of 10 30-Gbps channels for an aggregated data rate of 300 Gbps.

This project in particular seeks to demonstrate 120-Gbps PDM and FDM electronic communication over a 1-m long dielectric waveguide using circuits fabricated in 65-nm CMOS. 45-GHz bands around 180 and 315 GHz will be utilized for FDM. The transmitters and receivers connected through a diplexer or a combiner to a cross-dipole for the demonstration are shown in Fig. 2.

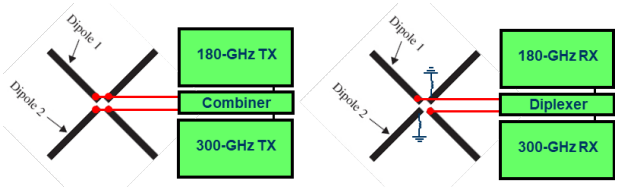

Figure 2. TX and RX chains for PDM and FDM operation with cross-dipoles.

Figure 3. Conceptual diagram of dielectric waveguide demonstration set up.

The transmitters and receivers will be integrated with the transitions to and from a waveguide developed by Prof. Henderson on printed circuit boards. The transitions will in turn be used to excite in and pick up signals from a low loss holey waveguide (8dB/m) that is being presently develop by Prof. MacFarlane and his students for the multiple channel demonstration utilizing PDM and FDM (Fig. 3). A 180-GHz transmitter and a 180 and 315-GHz receiver pair with a diplexer and a cross-dipole have been taped out in 65-nm CMOS.

Keywords: dielectric, waveguide, communication, millimeter waves

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] Q. Zhong et al., "300-GHz CMOS QPSK Transmitter for 30-Gbps Dielectric Waveguide Communication," *IEEE CICC*, April 2018, San Diego, CA.
[2] Q. Zhong et al., "CMOS Terahertz Receivers," (Invited) *IEEE CICC*, April, 2018, San Diego, CA.

APPENDIX I PUBLICATIONS OF TXACE RESEARCHERS

Conference Publications

[1] Xu, L., Zhuang, Y., Thinakaran, R., Butler, K., Chen, D. (2017). Accurate ADC testing with significantly relaxed instrumentation including large cumulative jitter. *IEEE International Test Conference (ITC), Fort Worth, TX*, pp 1-10, IEEE.

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[10] Zafarani, M., Akin, B. (2017). Comparison of real time motor fault signature analysis algorithms for drive embedded systems. *IEEE International Electric Machines and Drives Conference (IEMDC), Miami, FL*, pp. 1-7, IEEE.

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