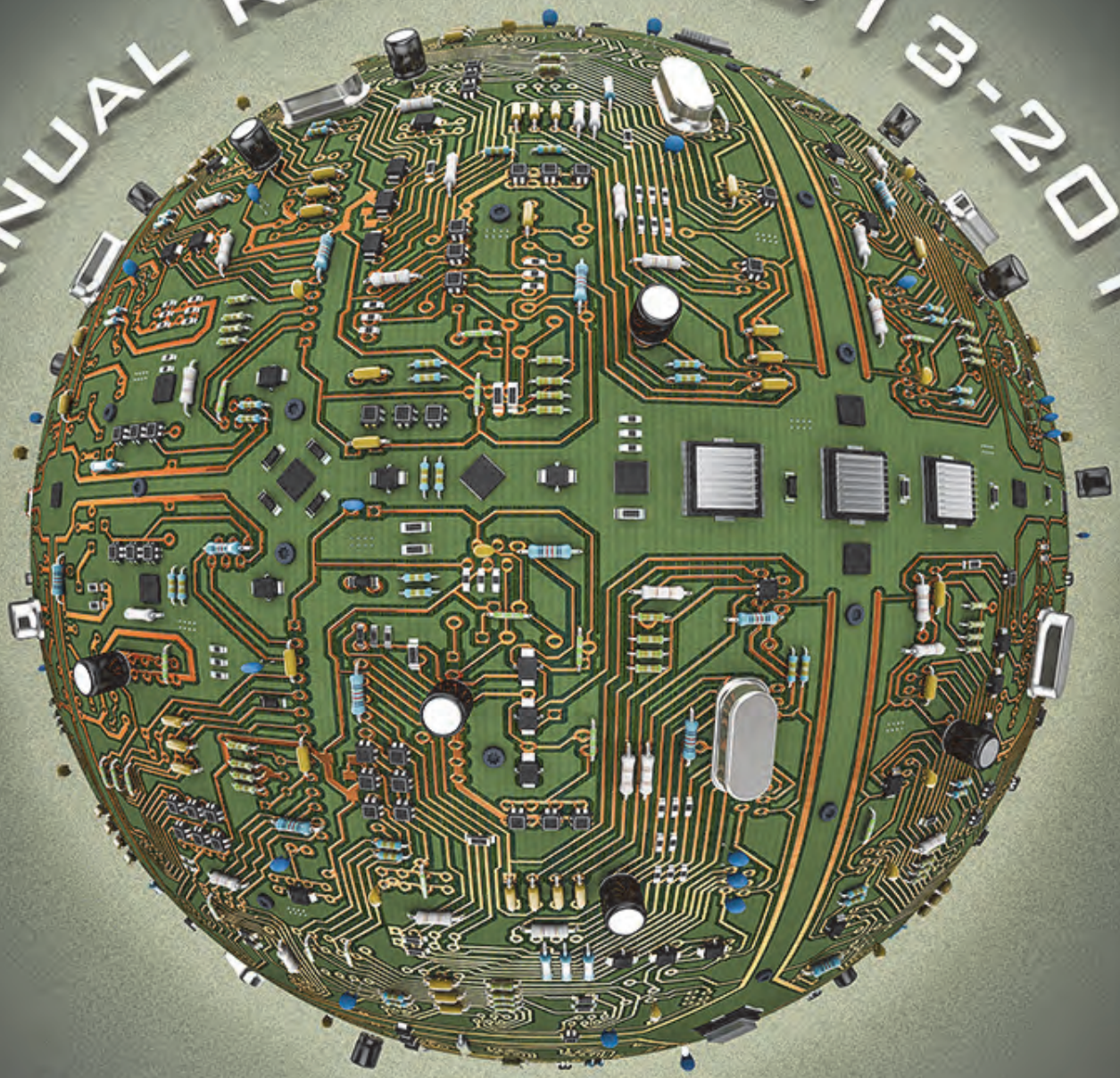
Texas Analog Center of Excellence

Annual Report 2013-2014



TxACE
TEXAS ANALOG
CENTER OF EXCELLENCE

SRC

TxACE MISSION

The Texas Analog Center of Excellence seeks to create fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, health care, and public safety and security.

TxACE THRUSTS

- *Safety & Security*
- *Health Care*
- *Energy Efficiency*
- *Fundamental Analog Circuits*

TxACE 2013-2014 ANNUAL REPORT

The Texas Analog Center of Excellence (TxACE), located at the University of Texas at Dallas is the largest analog research center based in an academic institution. Analog and mixed signal integrated circuits engineering is both a major opportunity and challenge. Analog circuitry is emerging as a critical component of nearly every product of a ~$300 billion per year integrated circuits industry, as a part of sensing, actuation, communication, power management and others. Digital integrated circuits such as microprocessors, logic circuits and memories are now integrating analog functions such as input/output circuits, phase locked loops, temperature sensors and power management circuits. It is also common to find microcontrollers with multiple analog-to-digital and digital-to-analog converters. These circuitries impact almost all aspect of modern life: safety and security, health care, transportation, energy, entertainment and many others.

The increasing importance of analog integrated circuits in electronic systems and the emergence of new applications are providing an exciting opportunity. However, the inherent difficulty of the art makes it challenging. Creation of advanced wireless technology and sophisticated sensing and imaging devices depends on the availability of engineering talent for analog research and development. TxACE was established to help translate these opportunities into economic benefits by overcoming the challenge and meeting the need. Support for TxACE has been provided through a collaboration of the state of Texas, Texas Instruments, the Semiconductor Research Corporation, the University of Texas System, and the University of Texas at Dallas.

The research tasks are organized into four research thrust areas: Health Care, Safety and Security, Energy Efficiency and Fundamental Analog. The scope of investigation extends from circuits operating at dc through terahertz, data converters that sample at a few samples/sec to 10s of Giga-samples/sec, ac-to-dc and dc-to-dc converters working at µW to Watts, energy harvesting circuits, protein and DNA sensors and many more. Significant improvement on existing mixed signal systems and new applications based on this circuit research are anticipated. Students who have been exposed to hands-on innovative research are forming the leading edge of analog talent flow into industry. Close collaboration with and responsiveness to industry needs provide focus to the educational experience.

DIRECTOR'S MESSAGE

The Texas Analog Center of Excellence (TxACE) is leading analog research and education. Last year, TxACE researchers published 42 journal and 100 conference papers. They also made three invention disclosures and filed two patent applications. Two patents have been granted. Twenty-three Ph.D. and six M.S. students of TxACE have graduated.

During the past year, the Center supported 58 principal investigators from 28 academic institutions, including four international universities. Six universities (SMU, Rice, Texas A&M, Texas Tech, UT Austin, UT Dallas) were from the state of Texas. The Center supported 79 research tasks and 117 graduate and undergraduate students.

The TxACE laboratory is continuing to help advancing integrated circuit technology by making its instruments available to all TxACE researchers as well as users outside of TxACE. The number of users outside of UT Dallas is steadily increasing and the infrastructure is being improved to better support all users. Working with the Advanced Research Center of UT Dallas, the Center has recruited a permanent staff member to maintain the laboratory and to support the measurement efforts.

The integrated circuits fabrication program has received a big boost last year. Globalfoundries has decided to support 65-nm and 40-nm MPW runs for the TxACE researchers. I would like to thank Dale Edwards, David Yeh, and Bill Joyner of SRC and Prof. Yun Chiu for their effort. The Center is also continuing to support the UMC 65-nm and 130-nm runs.

The Center had another outstanding year of accomplishments. I would like to thank the students, principal investigators and staff for their contributions, and UT Dallas, the University of Texas System, TI, and SRC, as well as many friends of TxACE all over the world for their generous support. As we enter our 7th year, I look forward to working even closer with the TxACE team to make difference in our world through our research, education and innovation.

Kenneth K. O, Director TxACE
Texas Instruments Distinguished Chair
The University of Texas at Dallas

BACKGROUND & VISION

The $300 billion per year integrated circuits industry is evolving into an analog/digital mixed signal industry. Analog circuits are providing or supporting critical functions such as sensing, actuation, communication, power management and others. These circuits impact almost all aspect of modern life including safety and security, health care, transportation, energy, and entertainment. To lead this change, in particular to lead analog and mixed signal technology education, research, commercialization, manufacturing, and job creation, the Texas Analog Center of Excellence was announced by Texas Governor Rick Perry in October 2008 as a collaboration of the Semiconductor Research Corporation, the state of Texas through its Texas Emerging Technology Fund, Texas Instruments Inc., the University of Texas system and the University of Texas at Dallas. The Center seeks to accomplish these objectives by creating fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, healthcare, and public safety and security as well as by improving the research and educational infrastructure.

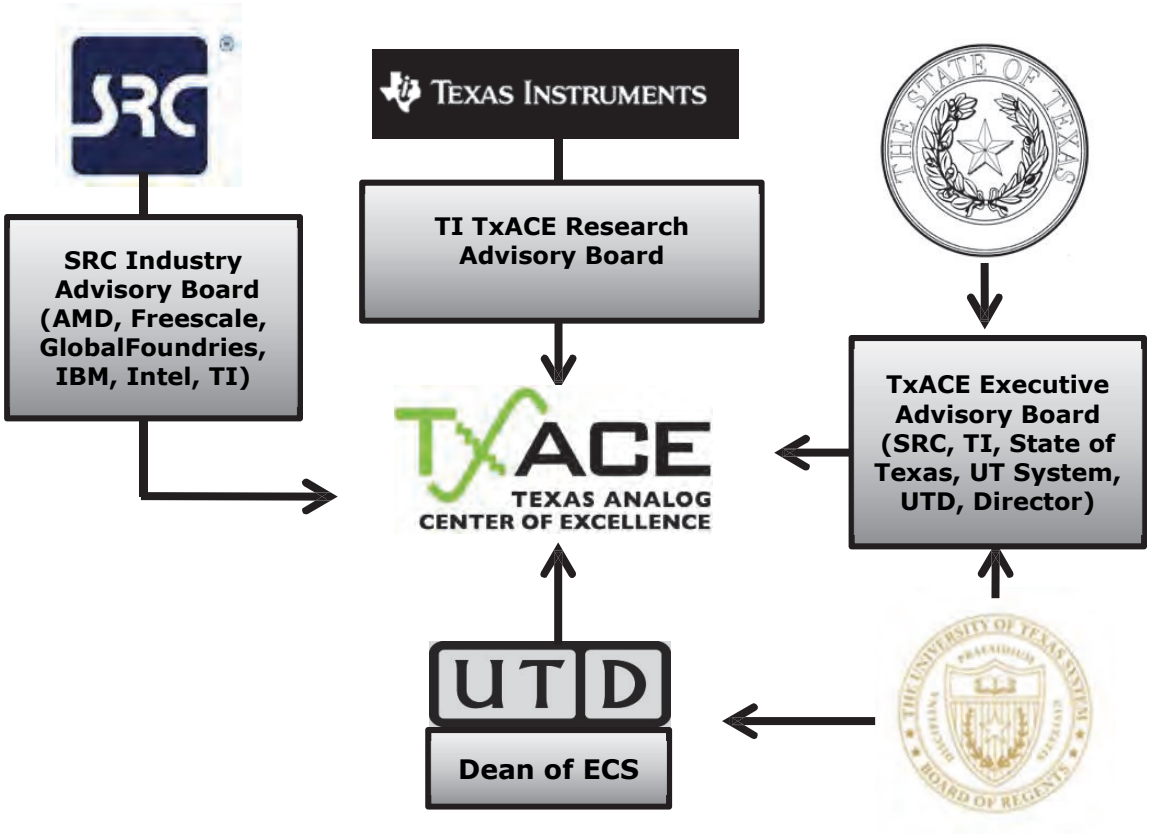


Figure 1: TxACE organization relative to the sponsoring collaboration

CENTER ORGANIZATION

The Texas Analog Center of Excellence is guided by agreements established with the Center sponsors. Members of the industrial advisory boards identify the research needs and select research tasks in consultation with Center leadership. Figure 1 diagrams the relationship of TxACE to the members of the sponsoring collaboration.

The internal organization of the Center is structured to flexibly perform the research mission while not detracting from the educational missions of the University.

Figure 2 shows the elements of the organization. The TxACE Director is Professor Kenneth O. The research is arranged into four thrusts that comply with the mission of the Center: Safety and Security, Health Care, Energy Efficiency and Fundamental Analog Research. The fourth thrust consists of vital research that cuts across more than one of the first three research thrusts. The thrust leaders are Prof. Brian A. Floyd of North Carolina State University for safety and security, Prof. Arjang Hassibi from UT Austin for health care, Prof. D. Ma of the UT Dallas for energy efficiency, and Prof. Ramesh Harjani of the University of Minnesota for fundamental analog research. The thrust leaders and Prof. Yun Chiu of the UT Dallas form the executive committee. The committee, along with the director, forms the leadership team that works to improve the research productivity of center by increasing collaboration, better leveraging the diverse capabilities of principle investigators of the Center, and lowering research barriers. The leadership team also identifies new research opportunities for consideration by the Industrial Advisory Boards.

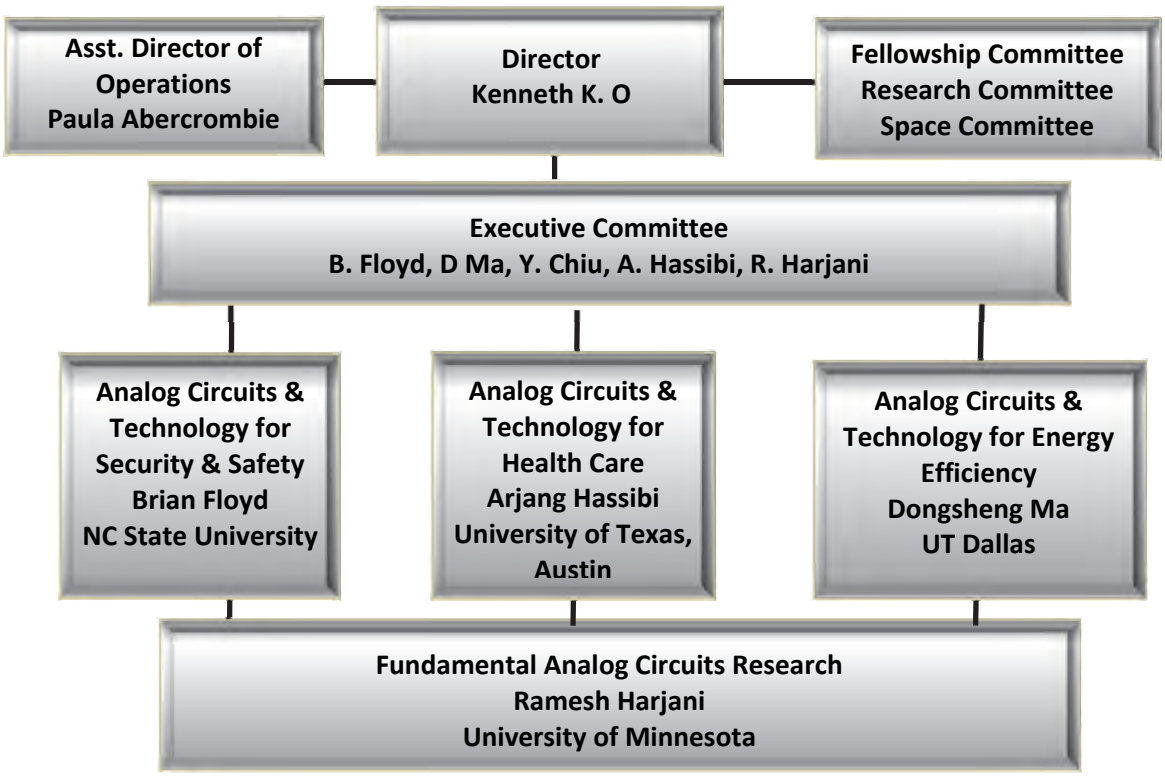


Figure 2: TxACE organization for management of research

PUBLIC SAFETY AND SECURITY

(Thrust leader: Brian Floyd, NC State University)

TxACE is developing analog technology that enhances public safety and security. The projects are intended to 1) enable a new generation of devices that can scan for harmful substances by researching 200-300 GHz silicon ICs for use in spectrometers, and 2) significantly reduce the cost of millimeter wave imaging and on-vehicle radar technology for automotive safety by researching circuit techniques that can improve manufacturing and simplify test and packaging, as well as signal processing techniques that reduce system complexity.

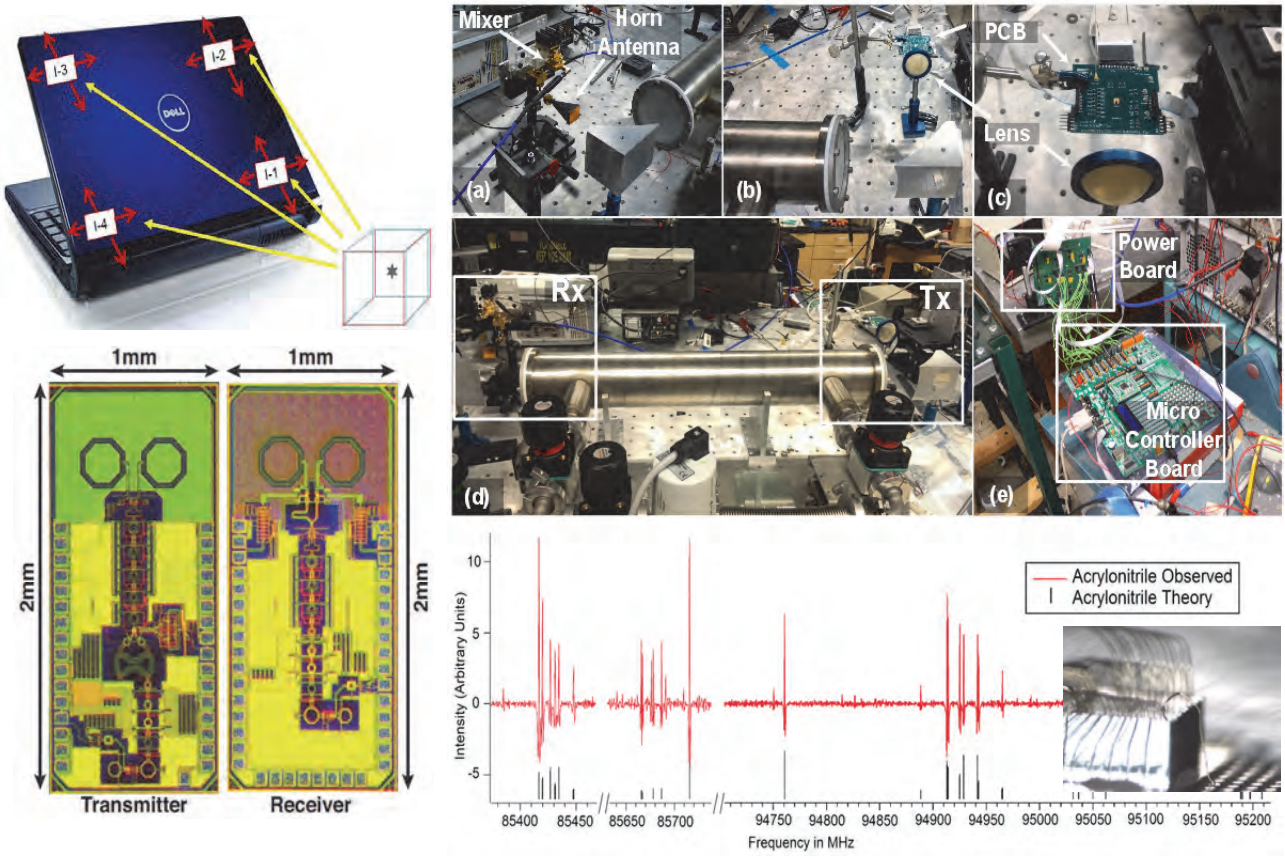


Figure 3: (Top left) 3-D millimeter wave Imaging (Saquib, UT Dallas), (Right) CMOS transmitter prototype for rotational spectroscopy that was used to detect gases. (K. K. O, UT Dallas and D. De Lucia, Ohio State) (Bottom left) 240-GHz QPSK transceiver (Alon, UC Berkeley).

HEALTH CARE

(Thrust leader: Arjang Hassibi, University of Texas, Austin)

Analog and RF integrated circuit technology is the essential interface enabling the power, speed and miniaturization of modern digital microelectronics to be brought to bear on an array of medical issues, including medical imaging, patient monitoring, laboratory analyses, bio-sensing and new therapeutic devices. TxACE is working to identify and support analog circuit research challenges that have the potential to enable important health-related applications. More specifically, TxACE is working to address the contact problem of EEG, to develop an affordable rotational spectrometer that can be used in breath analyses for health monitoring, and energy efficient radios for wearable wireless body area networks.

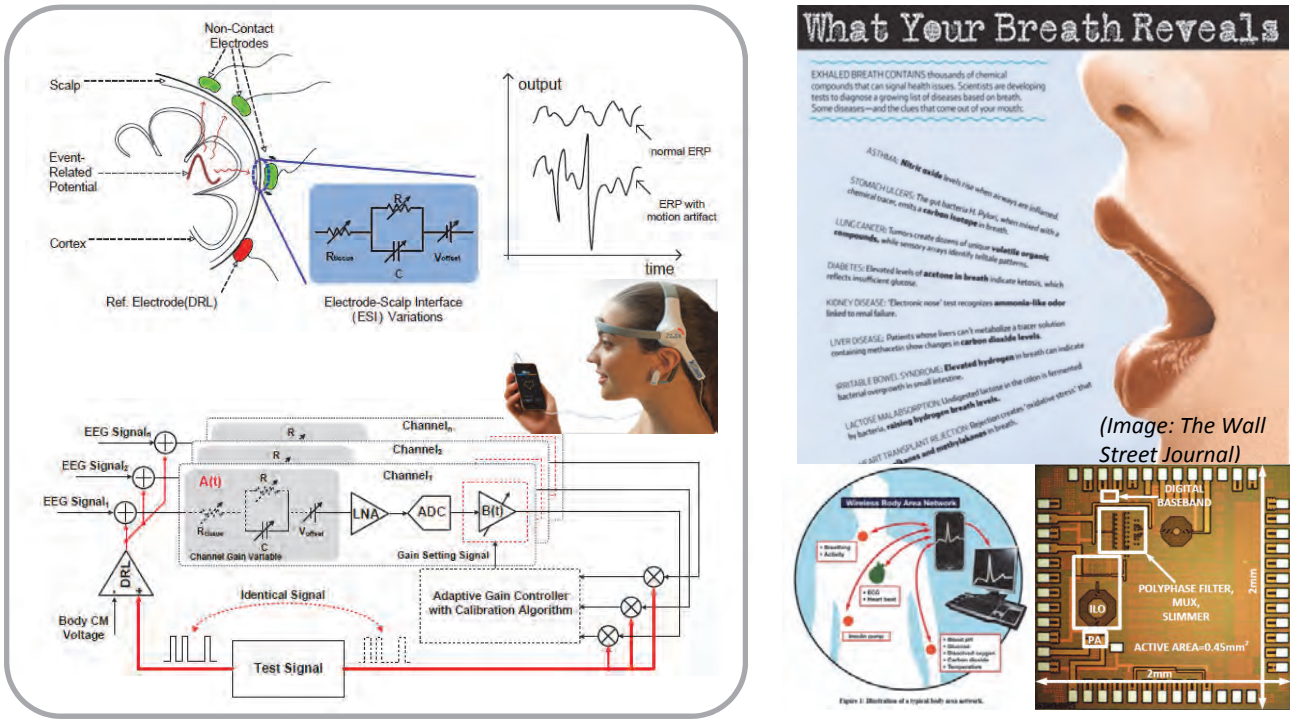


Figure 4: (Left) Adaptive electronics and signal processing for EEG (Y. Chiu and R. Jafari, UT, Dallas), (Top right) Breath analyses using a rotational spectrometer (K. K. O, UT Dallas), (Bottom right) Transmitter for wearable wireless body area networks (R. Harjani, U. of Minnesota).

ENERGY EFFICIENCY

(Thrust leader: Dongsheng Brian Ma, UT Dallas)

TxACE is committed to alleviate the global energy problem by improving the energy efficiency of electronic systems as well as by developing analog technologies that can make energy generation and distribution more efficient. The Center is also working to energize and power long-lasting in-situ microscale devices such as wireless microsensors, biomedical implants, and portable microelectronics.

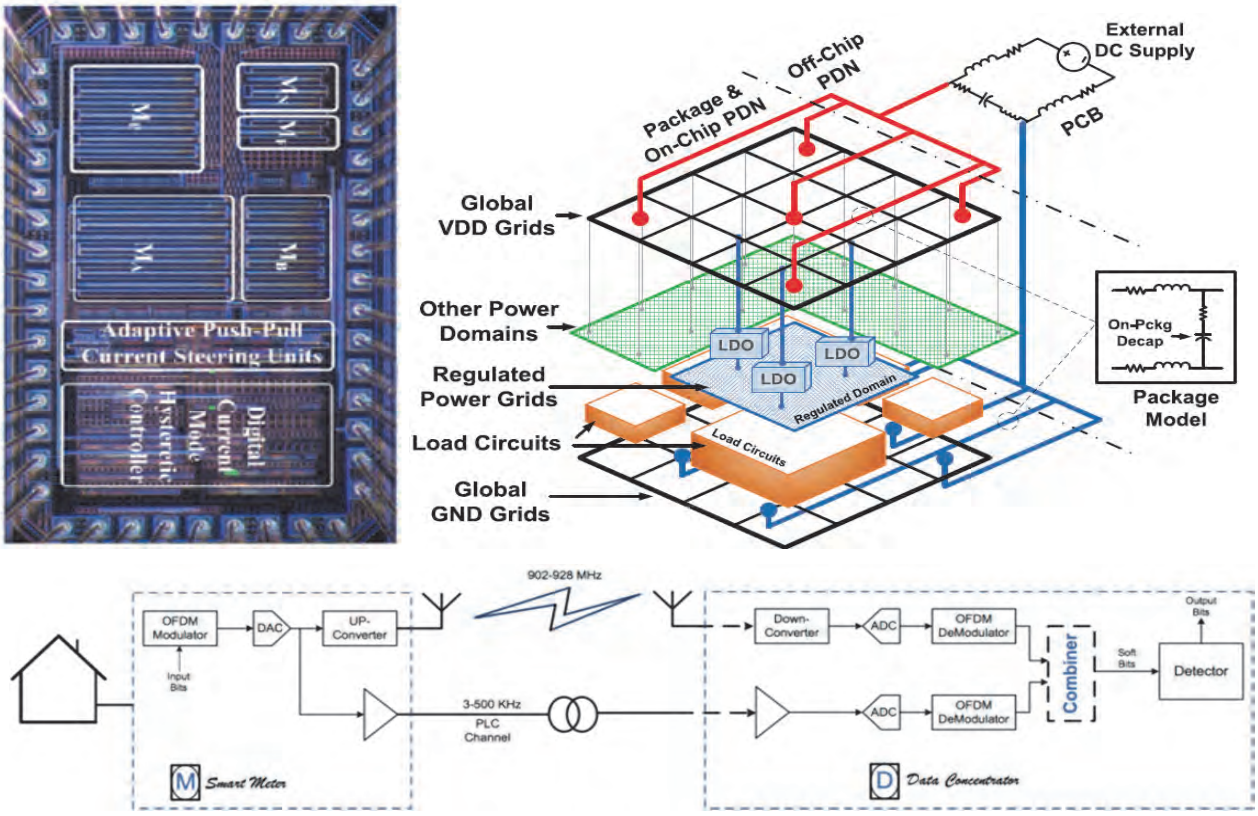


Figure 5: (Top left) Cross-regulation free single inductor multiple output DC-DC converter with nano-second load transient response (D. Ma, UT, Dallas), (Top right) With an increasing number of integrated LDOs, power distribution network instability is of significant concern. Simulation capability, system-oriented design models, and optimization-based design methodologies to enable efficient design space exploration for large PDNs with multiple integrated voltage regulators are being developed (P. Li, TAMU), (Bottom) Power line and wireless communication diversity to improve reliability and throughput (N. Al-Dahir, UT Dallas).

FUNDAMENTAL ANALOG CIRCUITS RESEARCH

(Thrust leader: Ramesh Harjani, University of Minnesota)

Research in this thrust focuses on cross-cutting areas in Analog Circuits which impact all of the TxACE application areas (Energy Efficiency, Health Care, Public Safety and Security). The list of research includes design of a wide variety of analog-to-digital converters, communication links, temperature sensors and I/O circuits, development of CAD tools, and testing of integrated circuits.

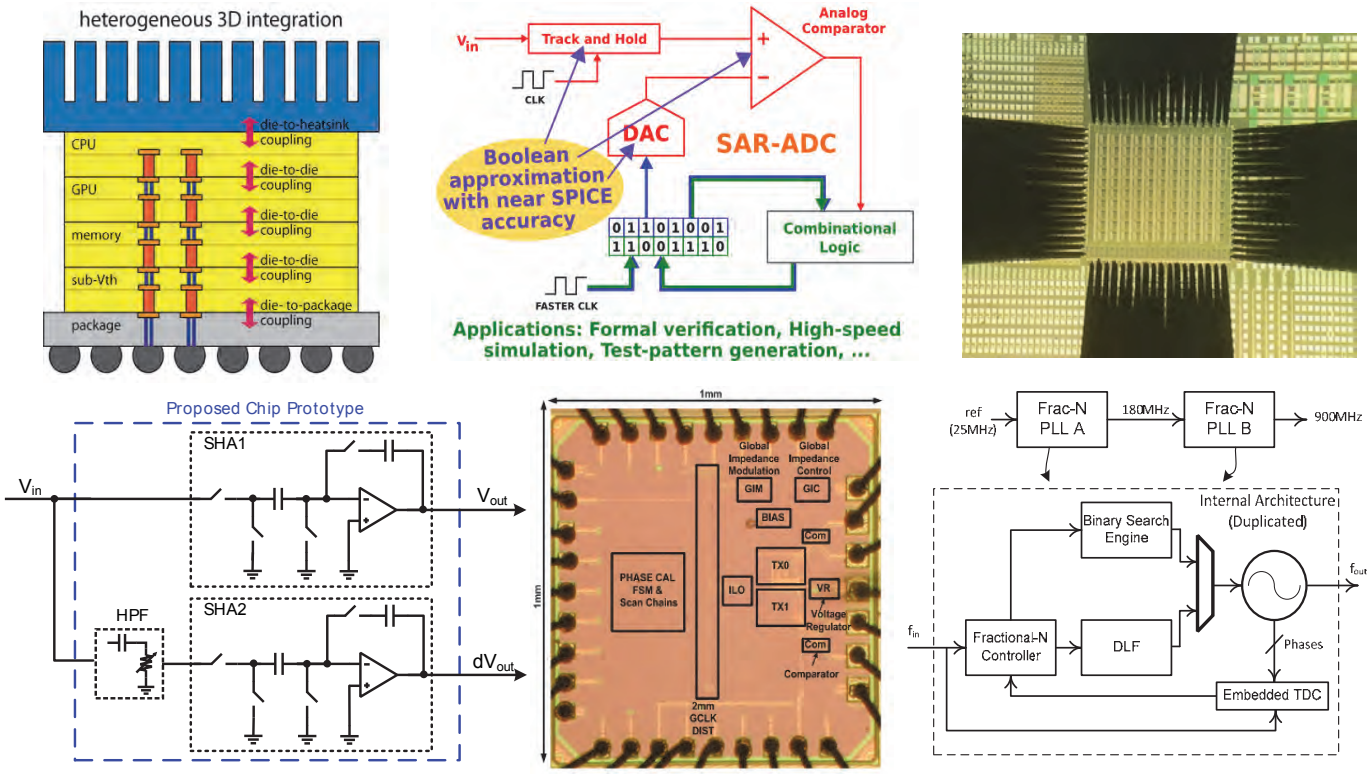


Figure 6: (Top left) 3D integrated heterogeneous system (S. Mukhopadhyay, GaTech), (Top center) Boolean models that accurately capture the SPICE-level continuous I/O behavior of analog/mixed-signal (AMS) systems will enable efficient formal analysis, verification, high-speed simulation (J. Roychowdhury, UC Berkeley), (Top right) A set of transistor variability characterization structures with gate lengths of 22nm in fully-depleted SOI technology (B. Nikolic, UC Berkeley), (Bottom left) Correction of nonlinearity of a switch in a sample and hold circuit (Y. Chiu, UT Dallas), (Bottom center) Sub-1mW/Gbps serial I/O transceiver (S. Palermo, TAMU), (Bottom right), Fully synthesized fractional-N ADPLL (D. Wenzloff, U. of Michigan).

TXACE ANALOG RESEARCH FACILITY

The centralized group of laboratories of the Texas Analog Center of Excellence dedicated to analog engineering research and training occupies a ~8000 ft^2 area on the 3rd floor of the Engineering and Computer Science North building (Figure 7). The facility includes RF and THz, Integrated System Design, Embedded Signal Processing, and Analog & Mixed Signal laboratories as well as CAD/Design laboratory structured to promote collaborative research**.** The unique instrumentation capability includes network analyses and linearity measurements up to 325 GHz, spectrum analysis up to 70 THz, and cryo-measurements down to $2^{o}K$. The Center also added a pulsed multiple harmonic load and source pull measurement set up (up to 60 GHz for the third harmonic) and an antenna measurement set up for measurements up to 325 GHz. The close proximity of researchers in an open layout enables natural interaction and compels sharing of knowledge and instrumentation among the students and faculty. The TxACE analog research facility is one of the best equipped electronics laboratories. The laboratory is available for use by TxACE researchers all over the world.

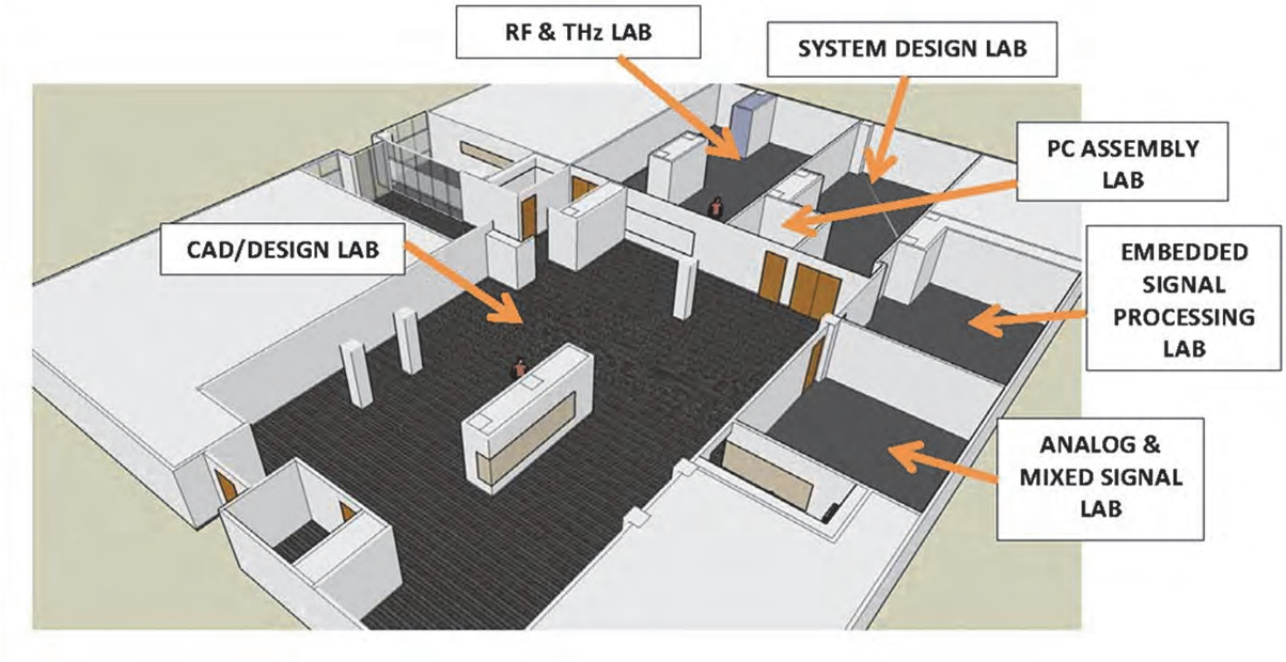


Figure 7: TxACE Analog Research Facility

RESEARCH PROJECTS AND INVESTIGATORS

The Texas Analog Center of Excellence (TxACE) is the largest university analog technology center in the world. Table 1 lists the current principal investigators of the 79 tasks from 28 academic institutions funded by TxACE. Six schools (Rice, SMU, Texas A&M, Texas Tech, UT Austin, UT Dallas) are from the state of Texas. Twenty-two are from outside of Texas. Four (Seoul National University, Korea; University of Cambridge, United Kingdom; National University of Ireland, Maynooth; and Technion – Israel Institute of Technology) (Figure 8) are from outside of the US. Of the 58 investigators, 23 are from Texas. During the past year, the Center supported 104 Ph.D. and 13 M.S. students, and 23 Ph.D. and 6 M.S. degrees were awarded to the TxACE students.

Table 1: Principal Investigators (September 2013 through August 2014)

Investigator	Institution	Investigator	Institution	Investigator	Institution
D. Akinwande	UT Austin	M. Flynn	U Michigan	R. McMahon	Cambridge
N. Al-Dahir	UT Dallas	R. Geiger	Iowa State	U.-K. Moon	Oregon State
E. Alon	UC Berkeley	P. Gui	SMU	S. Mukhopadyay	Georgia Tech
A. Apsel	Cornell	P. Hanumolu	UIUC	B. Murmann	Stanford
A. Babakhani	Rice U	R. Harjani	U Minnesota	A. Niknejad	UC Berkeley
B. Bakkaloglu	Arizona State	M. Hella	RPI	B. Nikolic	UC Berkeley
D. Blaauw	U Michigan	R. Henderson	UT Dallas	K. O	UT Dallas
L. Bleris	UT Dallas	R. Jafari	UT Dallas	S. Ozev	Arizona State
W. Burleson	U Mass	B. Kim	CUNY	S. Palermo	Texas A&M
A. Chatterjee	Georgia Tech	C. Kim	U Minnesota	A. Raychowdhury	Georgia Tech
D. Chen	Iowa State	J. Kim	Seoul Nat.	J. Ringwood	Nui Maynooth
Y. Chiu	UT Dallas	P. Kinget	Columbia	E. Rosenbaum	UIUC
W. Choi	UT Dallas	H. Lee	UT Dallas	J. Roychowdhury	UC Berkeley
F. De Lucia	Ohio State	M. Lee	UT Dallas	M. Saquib	UT Dallas
J. Di	U Arkansas	C. Li	Texas Tech	R. Shi	U Washington
Y. Eldar	Technion	P. Li	Texas A&M	G. Temes	Oregon State
K. Entesari	Texas A&M	D. Lie	Texas Tech	M. Torlak	UT Dallas
B. Evans	UT Austin	D. Ma	UT Dallas	D. Wentzloff	U Michigan
B. Fahimi	UT Dallas	Y. Makris	UT Dallas		
B. Floyd	NC State	H. A. Mantooth	U Arkansas		

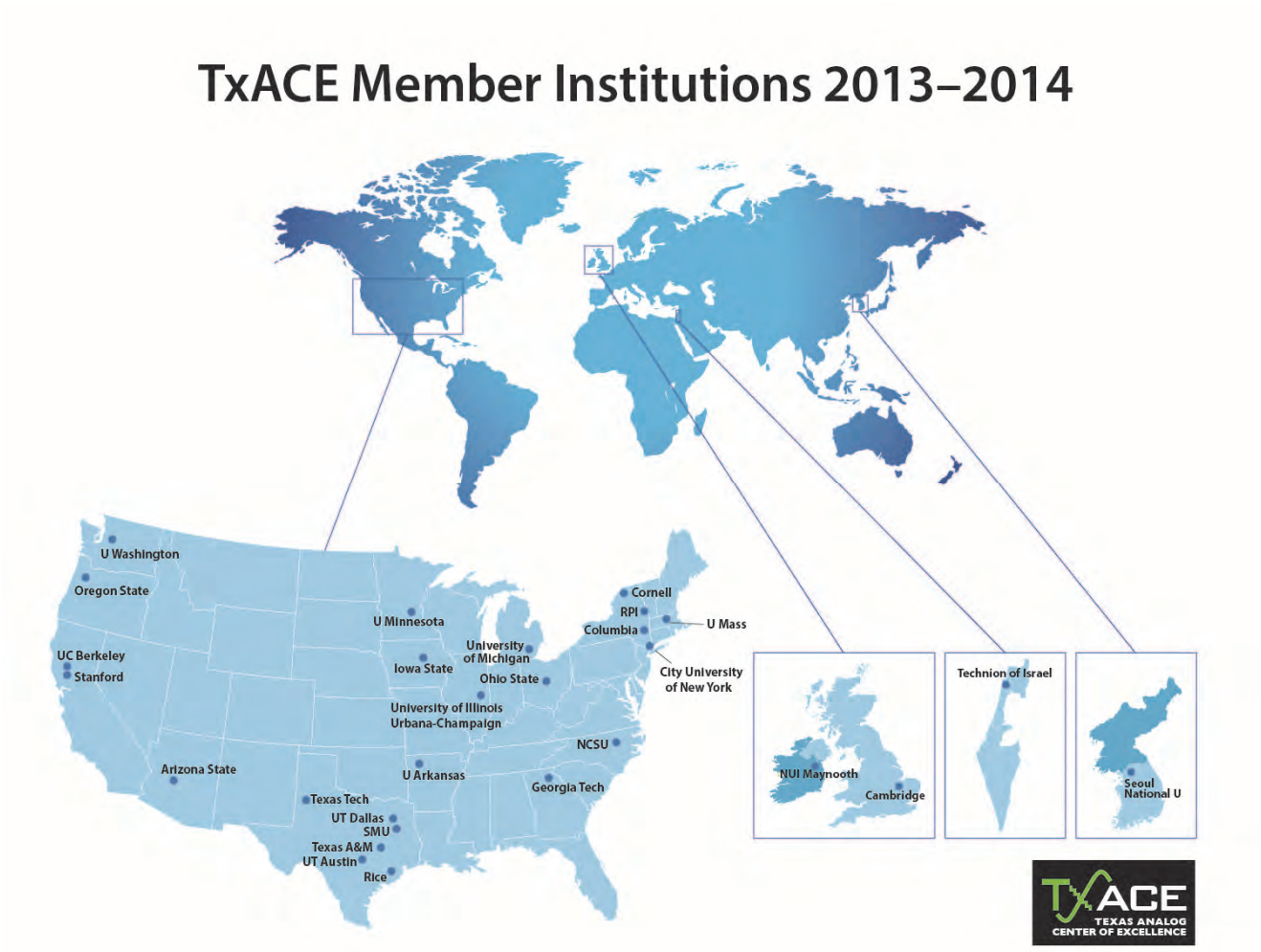


Figure 8: Member institutions of Texas Analog Center of Excellence

SUMMARIES OF RESEARCH PROJECTS

The 79 research projects funded through TxACE during 2013-2014 are listed in Table 2 below by the Semiconductor Research Corporation task identification number.

Table 2: Funded research projects at TxACE by SRC task identification number (FA: Fundamental Analog, EE: Energy Efficiency, HC: Healthcare, S&S: Safety and Security)

	Task	Thrust	Title	Task Leader	Institution
1	1836.057	FA	High Accuracy All-CMOS Temperature Sensor with Low-Voltage Low-Power Subthreshold MOSFETs Front-End and Performance-Enhancement Techniques	Li, Changzhi	Texas Tech
2	1836.058	FA	Hierarchical Model Checking for Practical Analog/Mixed-Signal Design Verification	Li, Peng	Texas A&M
3	1836.060	EE	Design Techniques for Scalable, Sub-1mW/Gbps Serial I/O Transceivers	Palermo, Samuel	Texas A&M
4	1836.061	HC	Analog Computing in Human Cells	Bleris, Leonidas	UT Dallas
5	1836.062	EE	System-Level Models and Design of Power Delivery Networks with On-Chip Voltage Regulators	Li, Peng	Texas A&M
6	1836.063	EE	Powerline Communications for Enabling Smart Grid Applications	Evans, Brian	UT Austin
7	1836.064	HC	Ultra-low-power Analog Front-End IC Design for Implantable Cardioverter Defibrillator (ICD) Devices	Lie, Donald	Texas Tech
8	1836.066	HC	A Fully-Integrated CMOS Platform for Microwave-Based Label-Free DNA Sensing	Entesari, Kamran	Texas A&M
9	1836.067	S&S	Characterization of CMOS Basic Building Blocks for Sub-THz Wideband Transmitters	Hella, Mona	RPI
10	1836.069	EE	Electronic Systems for Small-scale Wind Turbines	McMahon, Richard	Cambridge
11	1836.070	EE	Optimum Control of Power Converters	Ringwood, John	National Univ. of Ireland Maynooth
12	1836.072	S&S	Low Cost Test of High Speed Signals: Data Acquisition and Jitter Analysis	Chatterjee, Abhijit	Georgia Tech
13	1836.074	S&S	Sub-45nm Circuits for True Random Number Generation and Chip Identification	Burleson, Wayne	Univ. of Massachusetts/Amherst
14	1836.075	FA	Design of 3D Integrated Heterogeneous Systems	Mukhopadhyay, Saibal	Georgia Tech
15	1836.076	EE	Ultra-Low Power Delay-Insensitive Asynchronous Circuits	Di, Jia	Univ. of Arkansas/Fayetteville
16	1836.077	FA	Statistical Characterization of Circuit Aging	Kim, Chris	Univ. Of Minnesota

	Task	Thrust	Title	Task Leader	Institution
17	1836.078	FA	High-Resolution, Charge-Based A/D Converters for Nano-CMOS Technologies	Murmann, Boris	Stanford
18	1836.079	S&S	CMOS THz Generation and Detection	Hella, Mona	RPI
19	1836.080	FA	Variation-Tolerant Noise-Shaping ADCs With Embedded Digital Bias and V(DD) Scalable from 0.5V to 1.2V for Nanoscale CMOS	Kinget, Peter	Columbia
20	1836.081	EE	Combined Inductive/Capacitive DC-DC Converter for Efficient Dynamic Voltage Scaling	Harjani, Ramesh	Univ. of Minnesota
21	1836.082	S&S	Low-Cost Energy-Efficient 60GHz Transceivers with Built-In Test (BIST)	Alon, Elad	UC Berkeley
22	1836.083	S&S	Built-In Test for Millimeter-Wave Phased Arrays	Floyd, Brian	NC State
23	1836.084	EE	Single Set-up Detailed Testing of Wireless Transceivers Front-Ends Using Digital Processing	Ozev, Sule	Arizona State
24	1836.086	FA	Variation Tolerant Calibration Circuits for High Performance I/O	Apsel, Alyssa	Cornell
25	1836.087	FA	An Anyrate Reference-less Digital Clock-Data-Recover (CDR) with Decoupled Jitter Transfer and Jitter Tolerance Bandwidths	Gui, Ping	SMU
26	1836.088	EE	Efficient Digital-Intensive Wireless Transmitters Utilizing Switching Mode Pas	Gharpurey, Ranjit	UT Austin
27	1836.091	S&S	Interconnects on Flexible Plastic Substrates	Akinwande, Deji	UT Austin
28	1836.093	FA	Variability-Aware, Discrete Optimization for Analog Circuits	Kim, Jaeha	Seoul National Univ.
29	1836.094	S&S	Accurate FSM Approximations of Analog/RF Subsystems	Roychowdhury, Jaijeet	UC Berkeley
30	1836.095	FA	Test Generation for Mixed-Signal Design Verification and Post-Silicon Debugging	Shi, Richard	Univ. of Washington
31	1836.096	FA	Mixed-Signal Design Centering in Deeply Scaled Technologies	Nikolic, Borivoje	UC Berkeley
32	1836.097	FA	Dual-Domain SAR ADCs Incorporating Both Voltage and Time Information	Moon, Un-Ku	Oregon State
33	1836.098	HC	Sub mW Wireless Transceiver Frontends for Body Area Networks	Harjani, Ramesh	Univ. of Minnesota
34	1836.099	EE	Modeling of Analog and Switching Circuits	Mantooth, Homer Alan	Univ. of Arkansas/ Fayetteville
35	1836.101	S&S	Sparse 2D MIMO Radar Transceiver Design and Prototyping for 3D Millimeter-Wave Imaging	Saquib, Mohammad	UT Dallas
36	1836.102	S&S	Superresolution Techniques for 3D Millimeter Wave Radars	Torlak, Murat	UT Dallas
37	1836.103	HC	Reconfigurable Brain Computer Interface	Jafari, Roozbeh	UT Dallas

	Task	Thrust	Title	Task Leader	Institution
38	1836.104	EE	Fault Tolerant Drive Module for Double Stator Switched Reluctance Motor Drive (DSSRM)	Fahimi, Babak	UT Dallas
39	1836.105	EE	Cross-Regulation-Free Single-Inductor Multiple-Output DC-DC Power Converters with Nano-Second Load Transient Response	Ma, Dongsheng	UT Dallas
40	1836.106	EE	IF-Sampling CMOS ADC Front-End with 100-dB Linearity	Chiu, Yun	UT Dallas
41	1836.107	FA	Verification of Multi-State Vulnerable AMS Circuits	Geiger, Randall	Iowa State
42	1836.109	FA	New Paradigms for High-Performance Amplification	Moon, Un-Ku	Oregon State
43	1836.110	EE	Distributed Power Delivery Architecture for 2D and 3D Integrated Circuits	Mukhopadhyay, Saibal	Georgia Tech
44	1836.111	FA	Advanced ADC-Based Serial Link Receiver Architectures	Palermo, Samuel	Texas A&M
45	1836.112	EE	Shortstop: Fast Power Supply Boosting for Energy-Efficient, High-Performance Processors	Blaauw, David	Univ. of Michigan
46	1836.113	FA	Synthesized Cell-Based ADPLL Implementation for Accelerated Design	Wentzloff, David	Univ. of Michigan
47	1836.114	FA	Frequency Shapeable Multichannel ADCs	Eldar, Yonina	Technion
48	1836.115	EE	Analysis and Characterization of Switched-Mode DC-DC Power Converters	Li, Peng	Texas A&M
49	1836.116	EE	Transmitter Architectures for Powerline Communications	Gharpurey, Ranjit	UT Austin
50	1836.117	FA	Performance and Reliability Enhancement of Embedded ADC with Value-Added BIST	Geiger, Randall	Iowa State
51	1836.118	EE	Low Noise, Low Ripple Fully Integrated Isolated DCDC Converters for Signal Chain Applications	Bakkaloglu, Bertan	Arizona State
52	1836.119	S&S	Demonstration of 180-300 GHz Transmitter for Rotational Spectroscopy	O, Kenneth	UT Dallas
53	1836.120	S&S	Evaluation of Frequency and Noise Performance of CMOS 180 – 300 GHz Spectrometer Transmitter and Receiver Components	Lee, Mark	UT Dallas
54	1836.122	S&S	On-Chip Integration Techniques for 180-300 GHz Spectrometers	Henderson, Rashaunda	UT Dallas
55	1836.123	EE	Test Techniques and Fault Modeling for High Voltage Devices and Boards	Kim, Bruce	CUNY
56	1836.124	EE	Digitally-Enhanced Clocking Strategies to Improve Energy-Efficiency of Serial Links	Hanumolu, Pavan Kumar	UIUC
57	1836.125	FA	10GS/s+ Resolution-Scalable (4-7bits) ADCs	Flynn, Michael	Univ. of Michigan
58	1836.126	S&S	Design Spin Reduction via Integrated THz Design: Applications, Physics, and System Engineering	De Lucia, Frank	Ohio State

	Task	Thrust	Title	Task Leader	Institution
59	1836.127	FA	Precision Test without Precision Instruments - A Necessity for Future On-chip Self-test and Self Healing	Chen, Degang	Iowa State
60	1836.128	FA	Statistical Analog Design Property Checking	Li, Peng	Texas A&M
61	1836.129	FA	Energy-Efficient Digitally-Enhanced Rapid ON/OFF Links in Nanoscale CMOS	Hanumolu, Pavan Kumar	UIUC
62	1836.130	EE	Bulit-In Self-Test Techniques for Test, Calibration and Trimming of Power	Ozev, Sule	Arizona State
63	1836.131	S&S	Process Variation Anatomy: A Statistical Nexus Between Design, Manufacturing and Yield	Makris, Yiorgos	UT Dallas
64	1836.132	FA	Fault Coverage Analysis of Analog/Mixed-Signal Tests Based on Statistical Dissimilarity	Kim, Jaeha	Seoul National Univ.
65	1836.133	EE	Energy-Efficient Signal Processing Techniques for Smart Grid Heterogeneous Communications Networks	Al-Dhahir, Naofal	UT Dallas
66	1836.134	FA	Hybrid Two-Step PLLs for Digital SoCs in Nanoscale CMOS	Kinget, Peter	Columbia
67	1836.135	S&S	Sub-Picosecond Synchronization of Widely Spaced Imaging Arrays	Babakhani, Aydin	Rice Univ.
68	1836.136	FA	Injection-Locked Ring Oscillators for Clock Distribution in Manycore Processors	Nikolic, Borivoje	UC Berkeley
69	1836.137	FA	50GS/s and Beyond Frequency-interleaved Energy-Efficient ADCs	Niknejad, Ali	UC Berkeley
70	1836.138	EE	Micro-Power Analog-to-Digital Data Converters	Temes, Gabor	Oregon State Univ.
71	1836.139	EE	Enabling Fully-Integrated VHF CLK-Sync Multiphase Switching Regulators on Silicon	Ma, Dongsheng	UT Dallas
72	1836.140	EE	Embedded & Adaptive Voltage Regulators with Practive Noise Reduction for Digital Loads Under Wide Dynamic Range	Raychowdhury, Arijit	Georgia Tech
73	1836.141	FA	IC Design for Resilience Against System-Level ESD	Rosenbaum, Elyse	UIUC
74	1836.142	EE	Low Power Applications of FRAM	Blaauw, David	Univ. Michigan
75	1836.143	EE	Design Techniques for Modulation-Agile and Energy-Efficient 60+Gb/s Receiver Front-Ends	Palermo, Samuel	Texas A&M
76	1836.144	EE	High-efficiency High-voltage Power Converters	Lee, Hoi	UT Dallas
77	1836.145	FA	RF and Mixed Signal Quantum CMOS Devices and Circuits	Lee, Mark	UT Dallas
78	1836.146	EE	On-Chip AC-DC Power Conversion with Ground Disturbance Shielding for Environmental Sensing Applications	Ma, Dongsheng	UT Dallas
79	1836.147	S&S	Demonstration of 180 – 300 GHz Receiver for Rotational Spectroscopy	Choi, Wooyeol	UT Dallas

ACCOMPLISHMENTS

TxACE has made significant research progress. Table 3 summarizes the number of publications and inventions resulting from the TxACE research during May 2013 to April 2014, while Table 4 lists the major research accomplishments for the Center during the period. The TxACE researchers have published 100 conference papers and 42 journal papers. They have also made 3 invention disclosures and filed two patent applications. Two patents were granted. The list of publications is included as Appendix I. Following the tabulation, brief summaries of each project are provided.

Table 3: TxACE number of publications (May 2013 through April 2014)

Conference Papers	Journal Papers	Invention Disclosures	Patents Filed	Patents Granted
100	42	3	2	2

Table 4: Major TxACE Research Accomplishments (May 2013 through April 2014)

Category	Accomplishments
Fundamental Analog (Circuits)	The first 10Gs/s ADC with embedded FFE/DFE that achieves a BER of 10^{-9} at 10Gb/s over a 10" channel is demonstrated. The 6bit ADC has an FOM (0.48pJ/c-s) that is as competitive as the FOM of highly optimized ADCs that operate at the same speed. (1836.111, PI: S. Palermo, Texas A&M University)
Fundamental Analog (Circuits)	A Fractional-N dividerless frequency synthesis technique has been developed. The technique has been employed to implement an ADPLL using a digital flow including automatic place-and-route. The ADPLL achieves ~3X lower jitter than the state of the art custom designed fractional-N PLL operating around 900 MHz. (1836.078, PI: D. Wentzloff, University of Michigan)
Energy Efficiency (Circuits)	A novel supply boosting technique, called Shortstop, boosts a 3-nF core in 26ns while maintaining acceptable supply voltage droops. Shortstop is validated in a 28nm CMOS test chip. For a 15-nF core (an Intel Atom-sized core), boost latency is improved by 1.6X in addition to a 6X droop reduction. (1836.112, PI: D. Blaauw, University of Michigan).
Energy Efficiency (Circuits)	By using a highly scalable digital architecture with accurate frequency presetting and instantaneous phase acquisition, a prototype 8X/16X clock multiplier that achieves 10ns (3 reference cycles) power-on time, 2ps long-term absolute jitter, less than 25µW off-state power, 12pJ energy overhead for on/off transition, and 2.2mW on-state power at 2.5GHz output frequency is demonstrated. (1836.090, Pavan Hanumolu, Oregon State University)
Health Care (Circuits)	Demonstrated power efficient transmitter architecture for wireless body area networks. The 2.4-GHz transmitter is 802.15.6 compliant and digitally multiplexes the appropriate phases from an 800 MHz poly-phase filter output to generate π/4 DQPSK signals. Modulation at 1/3rd the RF frequency reduces the transmitter power consumption. (1836.098, PI: D. R. Harjani, University of Minnesota).
Security and Safety (Circuits)	A 240-GHz transceiver chipset was demonstrated using a 65-nm CMOS technology, including a passive mixer-first direct-conversion receiver and a frequency-tripled transmitter employing QPSK modulation. The chipset has been used to demonstrate a 16Gbps link. (1836.082, PI: E. Alon, A. Niknejad, UC Berkeley).
Security and Safety (Circuits)	Low-cost millimeter and sub-millimeter wave spectrometers could provide critical capabilities for breath analysis and detection of harmful molecules. A transmitter for rotational spectroscopy has been demonstrated in CMOS. This transmitter has been used with a bond-wire antenna within a gas spectrometer for detection of acrylonitrile. (1836.119 PI: K.K. O, UT Dallas; and 1836.126, PI: F. DeLucia, Ohio State Univ.)
Security and Safety (Test)	Low complexity high-speed waveform acquisition is an important component for built-in test. Incoherent undersampling has been used for signal acquisition, and has been demonstrated for both high-frequency linearity characterization in RF transmitters as well as jitter characterization in high-speed I/O systems. (1836.072, PI: A. Chatterjee, Georgia Tech)

Health Care Thrust

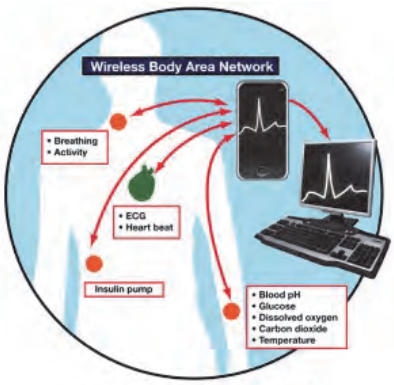
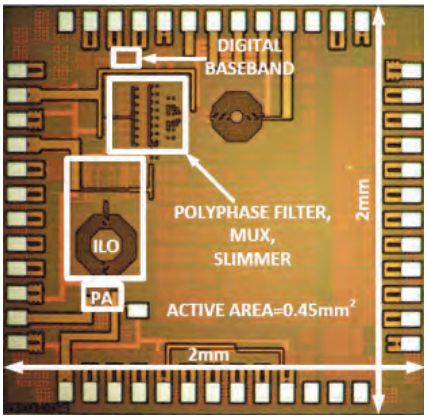


Figure 1: Illustration of a typical body area network.



Category	Accomplishment
Health Care	Demonstrated power efficient transmitter architecture for wireless body area networks. The 2.4-GHz transmitter is 802.15.6 compliant and digitally multiplexes the appropriate phases from an 800 MHz poly-phase filter output to generate π/4 DQPSK signals. Modulation at 1/3rd the RF frequency reduces the transmitter power consumption and enables channel selection using a PLL running at 800 MHz. (1836.098, PI: D. R. Harjani, University of Minnesota). Publication: M. Rahman, M. Elbadry, and R. Harjani, " A 2.5nJ/bit Multiband (MBAN & ISM) Transmitter for IEEE 802.15.6 based on a Hybrid Polyphase-MUX/ILO based Modulator," 2014 RFIC Symposium, Tampa FL, June 2014.

TASK 1836.061: ANALOG COMPUTING IN HUMAN CELLS

LEONIDAS BLERIS, THE UNIVERSITY OF TEXAS AT DALLAS, BLERIS@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

The objective of this project is the implementation of molecular circuits capable of responding to specific cellular disease-related signals and producing accordingly outputs that can be quantified using external devices.

TECHNICAL APPROACH

We developed a general framework for bridging endogenous cellular to extracellular information (Fig. 1), using programmable reagents that are prepared according to the tissue type and disease. Our multi-component RNA- and protein- based biosensor circuits are able to: (a) detect complex conditions related to abnormal expression of a number of molecular signals (microRNA and transcription factor) in human cells, (b) upon detection release biologically active modules in order to transduce the information to external devices.

SUMMARY OF RESULTS

Complex combinations of abnormally expressed microRNAs are an excellent indicator of cell state. A system capable to detect these conditions may be used as a highly selective tool for diagnosis and treatment.

We have implemented direct and inverter microRNA sensors. Both sensors have restriction enzyme sites within the 3'UTR, on both sides of the microRNA targets, to permit rapid replacement of the microRNA under study. We engineered sensors for miR16, miR17, miR21, miR10b, miR29a, miR34a, miR34b, miR34c, miR146a, miR192, miR194, miR210, miR215, miR221.

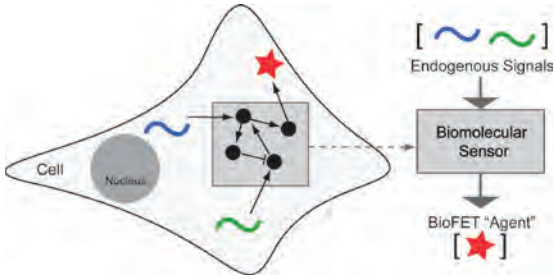


Figure 1: The biomolecular sensor responding to endogenous signals and producing an output for an external device.

We process endogenous information using sophisticated synthetic circuits. As an example, we studied the effect of negative feedback regulation (Fig. 2) on cell-wide (extrinsic) and gene-specific (intrinsic) sources of uncertainty [1]. We also published [2] a synthetic gene network architecture that operates as a biological decoder in human cells, converting 2 inputs to 4 outputs. As a proof-of-principle, we use small molecules to emulate the two inputs and fluorescent reporters as the corresponding four outputs. The experiments are performed in human kidney embryonic cells.

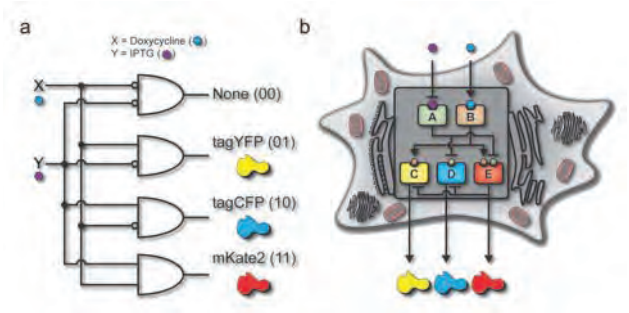


Figure 2: (a) A biological decoder with chemical inputs and fluorescence proteins as the outputs of the genetic circuit. (b) Node and edge schematic of the decoder circuit within a cell.

To connect to an external device, we have been testing proteins that can transduce endogenous information outside of a cell. In particular, we constructed genetic circuits that produce human chorionic gonadotropin (hCG). Illustrated in Fig. 3a, a paper-based colorimetric sensor for the detection of hCG protein activity.

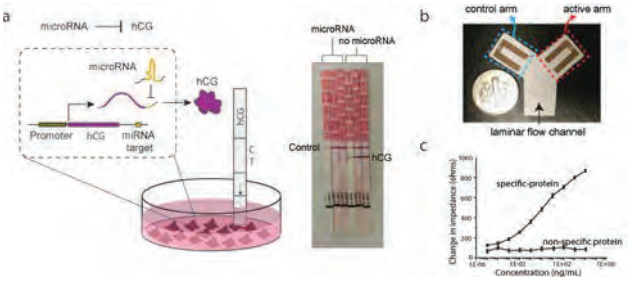


Figure 3: The interface and device. Interface of endogenous cancer information to colorimetric and impedance sensors.

In Fig. 3b, a paper sensor with gold electrodes immobilized with anti-hCG antibodies for the detection of hCG protein marker. The control arm has gold electrodes with no anti-hCG antibodies. Data shows the sample calibration response correlating impedance changes to varying concentration of a studied protein. The protein binding yields an impedance response.

Keywords: Synthetic biology, biosensors, microRNA.

MAJOR PAPERS

[1] Shimoga, V., White, J., Li, Y., E. Sontag, L. G. Bleris. Synthetic mammalian transgene negative autoregulation. Nature/EMBO Molecular Systems Biology, 9:670, 2013.

[2] Guinn, M. and L. G. Bleris. 2-input Decoder Circuit in Human Cells. ACS Synthetic Biology, 2014.

TASK 1836.064: ULTRA-LOW POWER ANALOG FRONT-END IC DESIGN FOR IMPLANTABLE CARDIOVERTER DEFIBRILLATOR (ICD) DEVICES

DONALD Y.C. LIE, TEXAS TECH UNIVERSITY, DONALD.LIE@TTU.EDU

SIGNIFICANCE AND OBJECTIVES

The significance and objectives of the project are to design ultra-low-power analog front-end (AFE) ICs for implantable cardioverter defibrillator (ICD) devices and other biosensors. Since the AFE circuits must always stay on, it is critical to design with both system-level and circuit-level techniques to reduce power dissipation.

TECHNICAL APPROACH

We have performed both SPICE simulation and measurement on the proposed entire AFE channel IC, which includes a couple of designs of the differential instrumentation amplifiers (INAs), differential band-pass filters (BPFs), differential-to-single-end variable gain amplifiers (VGAs), and single-ended successive approximation register (SAR) ADCs. The power consumption is reduced by designing low-power blocks on the circuit level, and by combining two channels on the system level. From the SPICE simulation results, our works are comparable with the state-of-the-art ones. The entire AFE IC only consumes <2 μA and may provide more gain and frequency settings among other works.

SUMMARY OF RESULTS

In this final year effort, progresses have been made on improving the integration of the entire AFE IC channel and setting up of the proper test bench for the AFE IC characterization. Furthermore, two instrumentation amplifiers (INAs), filters, VGAs, SAR ADCs and another whole AFE channels IC have been taped out. As shown in Fig. 1, a typical AFE circuitry for an ICD/bio-sensor can have an INA, a filter, a VGA and an ADC.

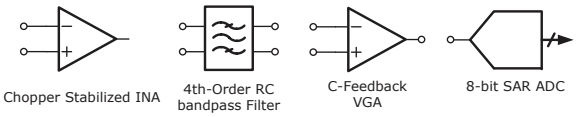


Figure 1: Circuit blocks used in the designed ICD AFE IC.

A chopper-stabilized INA is designed based on the Differential Difference Amplifier (DDA) topology as shown in Fig. 2, which can achieve high common-mode rejection ratio (CMRR) since its CMRR is theoretically only dependent on the mismatches of the input port (i.e., resistors mismatches for the feedback/gain setting should only influence the closed-loop gain). Fig. 2 also shows a selective feedback arrangement controlled using two control signals, making the INA possible for two gain modes (i.e., 20/40 dB). The output chopper modulator is realized using two chopper switches with CMOS devices to relieve the charge injection and clock feed-through issues. A chopper modulation frequency of 5 kHz was used. For simplicity, the block level in Fig. 2 shows the switches as one combined unit.

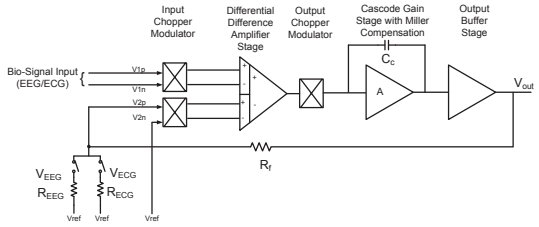


Figure 2: A block diagram of the chopper stabilized INA

The measure current consumption of the AFE IC is 1.4-2 μA and half of it comes from the INA. The SPICE simulated integrated input-referred noise of the AFE in the worst case is 6 μVrms. The integrated bandwidth of INA is 300 Hz and that of filters and VGA is 1 kHz. While calculating the noise of the filter chain referred to the AFE IC, we use an INA gain of 20 dB rather than 40 dB to avoid the possibility of signal saturation/compression. The die size is 3300x1300 μm2 as shown in Fig. 3. The performances of our AFE ICs are comparable vs. the state-of-the-art ones in literature. Eight peer-reviewed papers have come out from this task, including 2 invited and 1 journal papers, together with master theses and 3 internships and 1 direct hire by a member company.

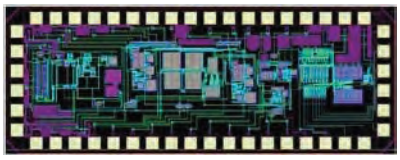


Figure 3: The layout of the proposed entire AFE IC channel.

Keywords: analog front-end (AFE) integrated circuit (IC), implantable cardioverter defibrillator (ICD), SAR (successive approximation register) ADC, sub-threshold CMOS, ultra-low-power sensor

INDUSTRY INTERACTIONS

Texas Instruments, IBM and Freescale

MAJOR PAPERS/PATENTS

[1] W. Hu et al., IEEE Trans. Circuits and Systems – I (TCAS-I), 60, 7, pp. 1726-1739 (2013).

[2] W. Hu et al., Proc. IEEE MWSCAS, pp. 1196-1199, (2012); Invited.

[3] D.Y.C. Lie et al., Open Journal of Applied Biosensor (OJAB), 2, 104-111, Nov. 2013.

TASK 1836.066: A FULLY-INTEGRATED CMOS PLATFORM FOR MICROWAVE-BASED LABEL-FREE DNA SENSING

KAMRAN ENTESARI, TEXAS A & M UNIVERSITY, KENTESAR@ECE.TAMU.EDU
SAMUEL PALERMO, TEXAS A & M UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

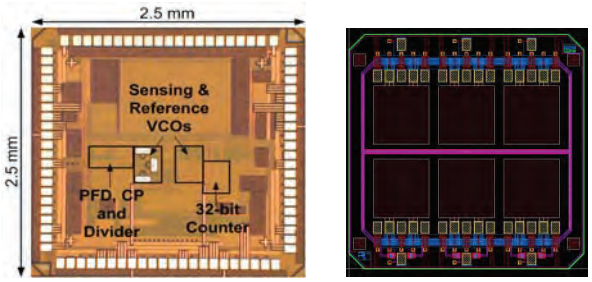
Implementation of cheap and compact sensors/systems to probe biochemicals and their interactions, at the molecular level, in point-of-care settings. Broadband, *bulk/volumetric* measurements of complex permittivity of liquid phase chemicals and small biomolecules can indicate molecular structure/conformation (chip#1). S*urface* charge measurements can indicate affinity-based interaction of probes/targets in DNA assays (chip#2).

TECHNICAL APPROACH

Employing CMOS lumped-circuit, broadband dielectric spectroscopy systems. In chip#1, bulk/volumetric measurements are done with *relatively wide-gap*, planar, interdigitated, fringing-field capacitive sensors. The detected oscillation frequency shift of a MUT-loaded, sensing ring oscillator (*relative* to unloaded, *reference* ring oscillator) varies with *both* load conductance (G) *and* capacitance (C). C and G are mapped to MUT polarization and dielectric loss, respectively. In chip#2, stand-alone, *very narrow-gap* (to detect changing *surface* charge with occurrence of hybridization), interdigitated sensors are built on CMOS, then coated with gold (to graft DNA probes) using post-processing. RF/microwave detection avoids electrode polarization and dielectric loss of water.

SUMMARY OF RESULTS

Both chips were fabrication using 0.18 um CMOS technology, their micrograph and CAD layout are shown in Fig 1. (a) and (b), respectively.



(a) (b)

Figure 1: (a) Micrograph of chip#1, and (b) CAD layout of chip#2

Chip#1 was completely tested directly after fabrication with standard chemicals and the results were published in IEEE CICC conference. A journal paper for IEEE JSSC is under preparation. Chip#2 is under post-processing by Intel (see industry interactions). After fabrication, bio-tests for DNA detection will be performed with the aid of Intel to characterize the bio-sensor. After successful characterization of both chips, the bio-sensors in chip#2 can be merged to the CMOS electronics implemented in chip#1 with proper modifications.

Fig. 1(a) shows the chip micrograph of the broadband dielectric spectroscopy system, fabricated in a 0.18-µm CMOS process. The system occupies 6.25 mm^2, and consumes 69-140 mW from a 1.8V supply. Utilizing a 28.5 MHz reference frequency, the PLL operates between 0.7-6 GHz for material under tests with ε' in the range between 1 and 30 and ε'' in the range between 0 and 30, corresponding to organic chemical values.

For this chip, system performance over mixing ratio is verified by exposing the sensor to several binary mixtures of ethanol and methanol with mixing ratios of methanol q = {0, 20, 50, 80, 100}% and measuring the frequency shifts due to each mixture across 0.7- 6GHz. The mixtures with q = {0, 50, 100}% are utilized for calibration**.** For mixtures with q = {20, 80}, ε' and ε'' are determined by substituting frequency shift measurements in the calibrated equations, with the measured and theoretical values shown in Fig.2.

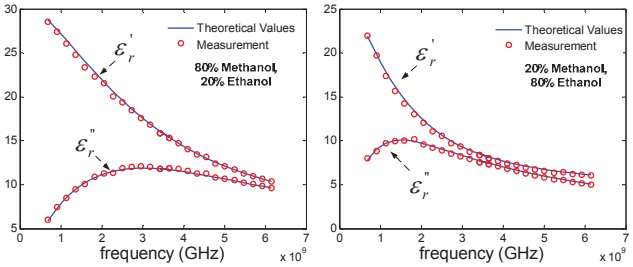


Figure 2: Measured and theoretical ε and ε'' of ethanol-methanol mixtures versus frequency.

Keywords: Biosensor, frequency synthesizer

INDUSTRY INTERACTIONS

Tayebi, Noureddine (Intel). Conference calls were conducted with the liaison regularly over the last year (chip#2). Liaison is providing support for on-die post-processing through Intel;

MAJOR PAPERS/PATENTS

[1] El-Hadidy, O., Shekib, S., Krenek, AK.., Palermo, S., and Entesari, K., "A 0.18-µm CMOS Fully Integrated 0.7-6 GHz PLL-Based Complex Dielectric Spectroscopy System," IEEE 2014 Customs Integrated Circuits Conference, (Accepted for publication).

TASK 1836.098: SUB MW WIRELESS TRANSCEIVER FRONTEND FOR BODY AREA NETWORKS

RAMESH HARJANI, UNIVERSITY OF MINNESOTA, HARJANI@UMN.EDU

SIGNIFICANCE AND OBJECTIVES

The standard for Wireless Body Area Networks (WBAN) is slowly coalescing in the form of IEEE 802.15.6. The project will focus on developing a low power transceiver frontend to meet the 802.15.6 narrowband specifications from 2360 to 2483MHz.

TECHNICAL APPROACH

Our design approach is to use novel simple architecture which consumes less power, sub-threshold operation, explore optimal partitioning of functions between analog and digital sections, applying injection locking, current reuse techniques to minimize power consumption, partial positive feedback, passive voltage multiplication and dynamic current mode techniques.

SUMMARY OF RESULTS

The overall block diagram of the transceiver is shown in Fig. 1. We have taped out and tested the transmitter in IBM 130nm technology. A MUX-based architecture is proposed where modulation occurs at 800MHz (i.e., 1/3rd the RF frequency). A passive polyphase filter centered at 800MHz generates all the 8 phases necessary for π/4 DQPSK modulation at 2.4GHz. The 8 phases generated by the polyphase filter are selected by the phase multiplexer (MUX) based on the digital baseband data. A switch based phase MUX selects the proper phase according to baseband data. A pulse slimmer is used to enhance the 3rd harmonic of the selected phase to which the injection locked oscillator locks. As shown in Fig. 2 the injection locked oscillator is a current reuse PMOS-NMOS oscillator whose output is inductively coupled to a single ended self-biased class AB amplifier with a raised V_{DD} of 1.5V. Modulation at 800MHz i.e. 1/3rd RF frequency using the sub-harmonic IL technique results in a simple and low power design. The design is flexible and can incorporate other harmonics provided the phase mapping is appropriately thought through. The energy efficiency including the estimated power of the PLL is 2.5nJ/bit (1.5 to 6.5X improvement compared to current state of the art). The robust modulation technique gets rid of the calibration needed for PLL based techniques. Further, this design does not require cap bank calibration, can support a large number of channels (118) even at high GHz frequencies and has no nonlinear phase mapping issues unlike existing IL techniques . The measured RMS EVM is 3.21% as shown in Fig. 3 which shows that the modulation scheme is very precise.

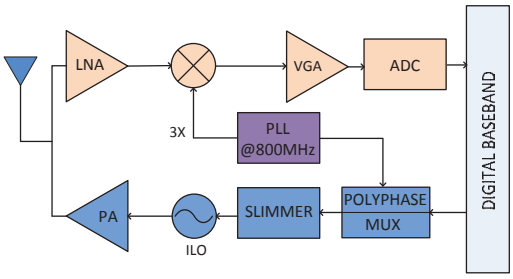


Figure 1: Transceiver architecture

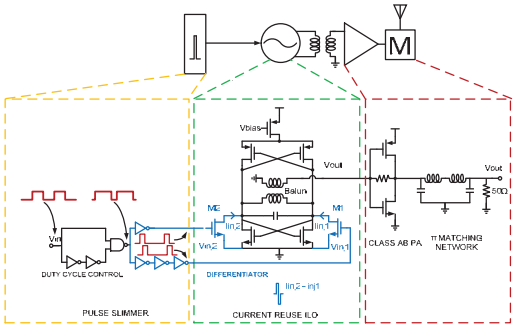


Figure 2: Current reuse ILO inductively coupled to Class AB PA

A low IF receiver has been taped out in 65nm CMOS technology. The receiver has a passive LNA followed by a square law mixer and works with sub 1V supply voltage.

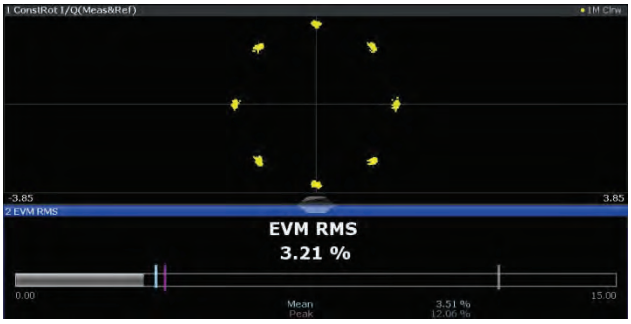


Figure 3: IIP3 of PA shown as 4.8dBm

Keywords: 802.15.6, WBAN, low power RF, sub-threshold RF, injection-locked oscillator.

INDUSTRY INTERACTIONS

Texas Instruments, Intel, Freescale

MAJOR PAPERS/PATENTS

[1] Rahman, M.; Elbadry, M.; Harjani, R., "A 2.5nJ/bit Multiband (MBAN & ISM) Transmitter for IEEE 802.15.6 Based on a Hybrid Polyphase-MUX/ILO-Based Modulator," IEEE RFIC, June 2014.

TASK 1836.103: BRAIN-COMPUTER INTERFACE (MOTION ARTIFACT REJECTION AND STABILIZATION FOR BIO-ELECTRONIC INTERFACE)

YUN CHIU, THE UNIVERSITY OF TEXAS AT DALLAS, CHIU.YUN@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

Accuracy and reliability of clinical diagnosis based on biophysical signals are heavily dependent upon the performance of analog front-end circuit, and variation of patient's electrode-tissue interface (ETI) that adds signal fluctuations (known as motion artifacts) and makes the system vulnerable to environment noise and interference. We present a novel technique to adaptively compensate the ETI variation to achieve maximum attainable biophysical signal and cancel motion artifacts.

TECHNICAL APPROACH

The electrical models of ETI and a commercial dry-contact electrode are utilized to identify different components of motion artifacts in a biophysical acquisition system. It has been shown that the motion artifacts can be categorized as multiplicative and additive motion artifacts (MMA and AMA, respectively) which are directly related to Acquisition-Path Gain (APG). The latter is the well-known baseline wandering phenomenon, for which there are many techniques developed already. It is clear that the MMA can be compensated if an accurate estimate of APG is available. Unfortunately, real-time measurement of APG is a challenging task. Alternately, we have developed a system that removes the multiplicative motion artifacts by desensitizing the biophysical signal to APG variations. Our analysis and simulation demonstrate that adaptive cancellation of effective parasitic capacitance at the front-end amplifier will result in near optimal cancellation of MMA. Estimations of this capacitance can be collected by injecting a pseudo-random signal into the body through driven-right-leg circuit (DRL) and estimating the gain variations from the auto-correlation of received signal.

SUMMARY OF RESULTS

In the proposed motion artifact rejection system, the APG can be formulated as follows,

$$A(t) = \frac{V_{out}(t)}{V_{in}(t)} = \frac{Z_{in} \| (sC_p)^{-1}}{Z_{in} \| (sC_p)^{-1} + Z_{ETI}(t)} \qquad (1)$$

It is evident that A(t) will be independent of $Z_{ETI}(t)$ given $Z_{in}=\infty$ and $C_p=0$. The former can be obtained by using an MOS-input amplifier and proper layout and electrical considerations. C_p is the effective capacitance from electrode and analog circuit parasitic capacitors. This capacitance can be cancelled by injecting a wide-band test signal (pseudo-random sequence) into the body and estimating the overall signal transfer function dynamically. The objective of this adaptive system is to flatten the frequency response in the band of interest which can be achieved by adjusting a negative capacitor (parallel to C_p) corresponding to an error signal calculated from auto-correlation calculations. The continuous injection of test signal and monitoring the transfer function can track patient's movements and remove the multiplicative motion artifacts.

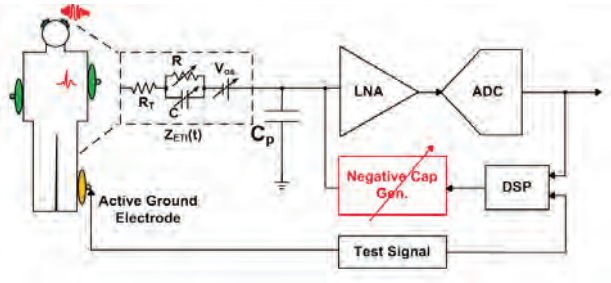


Figure 1: Block diagram of the proposed system prototype

As a proof of concept, a 65-nm CMOS low-noise amplifier and negative capacitance generator circuit and other analog blocks are designed at transistor level and simulated in Spectre. This chip includes all the blocks to acquire stable signals from a ECG/EEG acquisition system and to suppress interference from mains power. The results shown in Fig. 2 illustrate the cancellation of electrode's parasitic capacitance by about 99% which results in an expanded bandwidth.

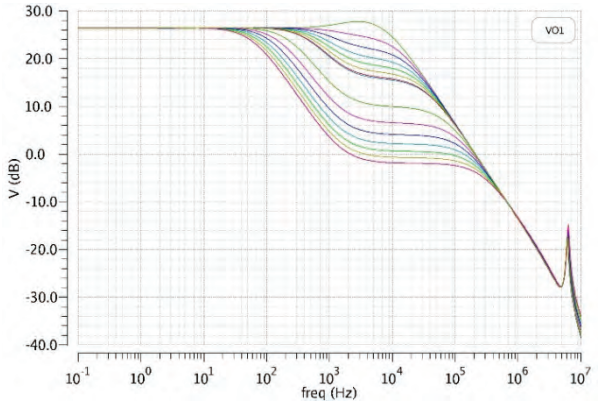


Figure 2: Transistor level simulation of negative capacitance circuit

Keywords: biophysical signals, adaptive compensation, low-noise amplifier, driven-right-leg

INDUSTRY INTERACTIONS

Texas Instruments

TASK 1836.103: RECONFIGURABLE BRAIN COMPUTER INTERFACE

ROOZBEH JAFARI, THE UNIVERSITY OF TEXAS AT DALLAS,
RJAFARI@UTDALLAS.EDU
COLLABORATOR: MIKE CHI, UC SAN DIEGO & COGNIONICS

SIGNIFICANCE AND OBJECTIVES

Dry EEG electrodes enhance the convenience and wearability of brain computer interface (BCI) systems, but the noise induced due to the skin electrode interface reduces the signal quality compared to that of wet electrodes. The aim is to design a wearable dry contact EEG system that estimates and responds to variations in skin contact impedance across different electrodes as well as motion artifacts in real-time in order to improve the signal to noise ratio (SNR)/enhance signal processing accuracy.

TECHNICAL APPROACH

Thorough analyses aimed at electrode-skin noise characterization were performed. Several noise models including half-cell noise, motion artifacts and baseline wandering were considered. Several electrode configurations including an electrode module where each individual finger can be sensed simultaneously and a module where fingers can be activated/deactivated based on their noise characteristics using a MUX were designed, developed and validated. Signal processing algorithms based on ICA that remove noisy channels were developed.

SUMMARY OF RESULTS

We analyzed a popular dry electrode design that incorporates several 'finger' shaped contacts and showed how the noise level can be reduced by estimating the contact quality of each finger and reconfiguring the electrode accordingly. We designed custom electrodes for this analysis and showed the differences in skin interface noise among fingers of the same electrode. Finally, we showed how eliminating the signals from one of more noisy fingers can lead to better correlation with an ideal wet electrode and reduce the amount of noise by 1.6μV on average, which constitutes 11% of the EEG signal.

Several configurations of electrode where designed and developed as shown in Fig. 1. This includes individual finger channel electrode where each finger can be sensed simultaneously. Another configuration where a multiplexer enables real-time reconfiguration of the fingers has been developed. The results of our finger selection algorithm are presented in Table 1. For each of the subjects, at least one of the attempted combinations with fewer fingers showed better performance in terms of average correlation with the wet electrode, serving as a gold standard. These measurements were all statistically significant performance improvements over the 15 trials of each session, with p-values < 0.05 in one-sided paired t-tests with the correlation coefficients of the nearest 'all fingers' trials.

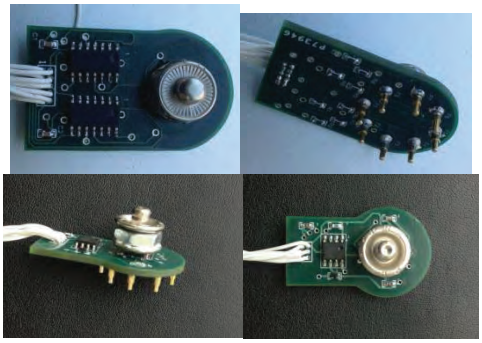


Figure 1: Individual finger channels front and back (top) and MUX electrode front and back (bottom).

Furthermore, a signal quality enhancement method based on the electrode-scalp impedance leveraging ICA was designed and validated.

Table 1: Performance comparison between selected MUX combinations vs the 'all fingers' combination for all three subjects

Subject	Average Correlation Coefficient (custom finger combination)	Average Correlation Coefficient (all 8 fingers selected)	p-value from one-sided paired t-test
Subject 1 Combo 1	0.903 (4 out of 8 fingers)	0.877 (all 8 fingers)	0.0297
Subject 2 Combo 1	0.951 (3 out of 8 fingers)	0.935 (all 8 fingers)	0.0086
Subject 2 Combo 2	0.962 (4 out of 8 fingers)	0.939 (all 8 fingers)	0.0151
Subject 3 Combo 1	0.912 (2 out of 8 fingers)	0.882 (all 8 fingers)	0.0425

Keywords: Dry-contact EEG, BCI, Electrode-skin noise modeling, Electrode reconfiguration, Motion artifact rejection.

INDUSTRY INTERACTIONS

Texas Instruments, Intel

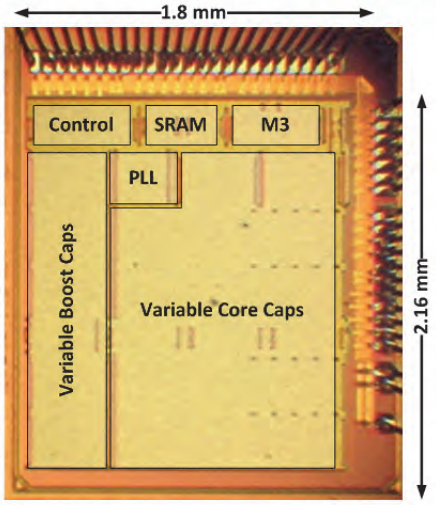
MAJOR PAPERS/PATENTS

[1] Nathan, et al., "Reducing the Noise Level of EEG Signal Acquisition through Reconfiguration of Dry Contact Electrodes", 2014 BioCAS, Lausanne, Switzerland.

[2] Zou et al., "Automatic Removal of EEG Artifacts using Electrode-Scalp Impedance",2014 ICASSP, Florence, Italy.

[3] Jafari, et al., http://bcibench.org/

Energy Efficiency Thrust



Fast On-Chip Power Supply Boosting Implementation on 28nm process (Task 1836.112)

Category	Accomplishment
Energy Efficiency	A novel supply boosting technique, called Shortstop, boosts a 3-nF core in 26ns while maintaining acceptable supply voltage droops. Shortstop adds a second "dirty" supply rail and an on-chip boost capacitor to rapidly boost the core. Shortstop is validated in a 28-nm CMOS test chip. For a 15-nF core (an Intel Atom-sized core), boost latency is improved by 1.6X in addition to a 6X droop reduction. Shortstop maintained a 1.4X latency improvement and 4X droop reduction across the three packages tested. Publication: [1] N. Pinckney et. al., "Shortstop: An On-Chip Fast Supply Boosting Technique," IEEE Symposium on VLSI Circuits, June 2013. (1836.112, PI: D. Blaauw, University of Michigan).
Energy Efficiency	Techniques to realize a highly digital clock multiplier that achieves low jitter, fast locking and near-zero off-state power are being researched. By using a highly scalable digital architecture with accurate frequency presetting and instantaneous phase acquisition, a prototype 8X/16X clock multiplier achieves 10ns (3 reference cycles) power-on time, 2ps long-term absolute jitter, less than 25µW off-state power, 12pJ energy overhead for on/off transition, and 2.2mW on-state power at 2.5GHz output frequency. Publications: [1] T. Anand et al., "A 2.5GHz 2.2mW/25µW On/Off-State Power $2ps_{rms}$ Long-Term-Jitter Digital Clock Multiplier with 3-Reference-Cycles Power-On Time," 2013 ISSCC, February, 2013, San Francisco, USA. (1836.090, Pavan Kumar Hanumolu, Oregon State University)

TASK 1836.060: DESIGN TECHNIQUES FOR SCALABLE SUB-1MW/GBPS SERIAL I/O TRANSCEIVERS

SAMUEL PALERMO, TEXAS A&M UNIVERSITY, SPALERMO@ECE.TAMU.EDU
PATRICK CHIANG, OREGON STATE UNIVERSITY, PCHIANG@EECS.OREGONSTATE.EDU

SIGNIFICANCE AND OBJECTIVES

Interface architectures which allow for high data rates at improved power efficiency levels are required to satisfy the growing I/O bandwidth in power-constrained environments. This project aims to improve the power efficiency of serial I/O transceivers to sub 1mW/Gbps for data rates ranging from 5-20Gbps.

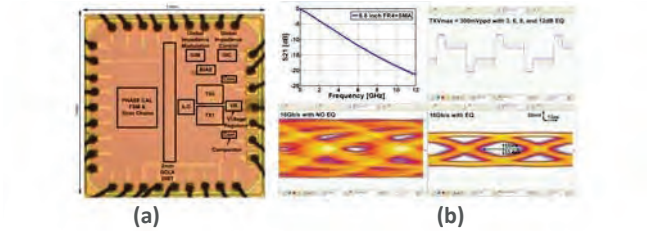
TECHNICAL APPROACH

The project utilizes a source-synchronous architecture with ultra-low-power driver, receiver, and clocking circuits that operate over a wide range of supply voltages. The key design techniques developed in this work include:

- Supply-scalable circuits to enable dynamic power management.
- A voltage-mode transmitter with analog impedance modulation equalization and fast power-state transitioning.
- A low-voltage decision-feedback equalizer based on charge-based latches.
- An injection-locked receiver with input duty-cycle distortion tolerable edge-rotating 5/4X sub-rate CDR.

SUMMARY OF RESULTS

A scalable data-rate voltage-mode transmitter was developed [1]. An impedance-modulated 2-tap equalizer is adopted that employs analog control of the equalizer taps, thereby obviating output driver segmentation. Fast power-state transitioning is achieved using a replica-biased voltage regulator to power the output stages of multiple channels and per-channel injection-locked oscillators (ILO) that can be rapidly disabled. A 65nm CMOS prototype achieved 8-16Gb/s operation at 0.65-1.05pJ/b energy efficiency and sub-3ns power-up/down times (Fig. 1).

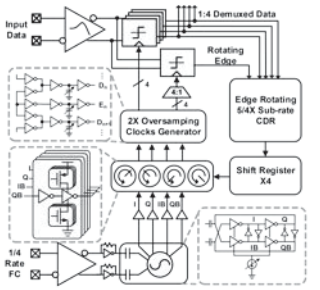


(a) (b)

Figure 1: 8-16Gb/s voltage-mode transmitter with analog impedance modulation equalization (a) GP 65nm CMOS prototype (b) equalization and 16Gb/s performance.

A DFE was developed designed specifically to operate at low-VDD with the following innovations: 1) fast and energy-efficient charge-based latch and sample-and-hold (S/H) topologies; 2) a CMOS-clocked quarter-rate DFE architecture with summer gain and power optimization; 3) an integrating summer with a compact common-mode restoration circuit. The proposed DFE is capable of operating at/below 0.7V, with an energy efficiency of/better than 0.25pJ/bit [2].

A quarter-rate forwarded-clock receiver (Fig. 2) was developed that utilizes an edge- rotating 5/4X sub-rate CDR for improved jitter tolerance with low power overhead [3]. Fabricated in GP 65nm CMOS, the receiver operates up to 16Gb/s with a BER<10^{-12}, achieves a 1MHz phase tracking bandwidth, tolerates ±50%UI_{pp} DCD on input data, and has 14Gb/s energy efficiency of 560fJ/b



(a) (b)

Figure 2: Injection-locked receiver with input DCD tolerable edge-rotating 5/4X sub-rate CDR.

at VDD=0.8V.

Keywords: High-speed I/O, injection-locked oscillator, transmit equalization, voltage-mode driver.

INDUSTRY INTERACTIONS

Freescale, Intel, Texas Instruments

MAJOR PAPERS/PATENTS

[1] Y.-H. Song et al., "An 8-16Gb/s, 0.65-1.05pJ/b, 2-Tap Impedance-Modulated Voltage-Mode Transmitter with Fast Power-State Transitioning in 65nm-CMOS," 2014 IEEE ISSCC.

[2] R. Bai et al., "A 0.25pJ/b, 0.7V, 16Gb/s 3-Tap Decision-Feedback Equalizer in 65nm CMOS," 2014 IEEE ISSCC.

[3] H. Li et al., "A 0.8V, 560fJ/bit, 14Gb/s Injection-Locked Receiver with Input DCD Tolerable Edge-Rotating 5/4X Sub-Rate CDR in 65nm CMOS," 2014 IEEE VLSI Sym.

TASK 1836.062: SYSTEM-LEVEL MODELS AND DESIGN OF POWER DELIVERY NETWORKS WITH ON-CHIP VOLTAGE REGULATORS

PENG LI, TEXAS A&M UNIVERSITY, PLI@TAMU.EDU

SIGNIFICANCE AND OBJECTIVES

The design of power delivery networks (PDNs) is a key avenue and a challenge for achieving power efficiency. We develop simulation tools, models and holistic system design flows to achieve the optimal system performance trade-offs, and facilitate joint design optimization of active voltage regulators, converters, and passive on-die power grids.

TECHNICAL APPROACH

One of the key focuses of this work is to optimize power delivery by identifying, analyzing and leveraging opportunities that involve with joint optimization of active regulator/converter circuits and passive distribution sub-networks. We are building simulation capability, system-oriented design models, and optimization-based design methodologies to enable efficient design space exploration for large PDNs with multiple integrated voltage regulators.

SUMMARY OF RESULTS

Our recent focus in this project has been placed towards addressing the stability design challenge for distributed active on-chip voltage regulation. Placing multiple voltage regulators onto the die is an effective way for distributed on-chip voltage regulation and provides significant benefits in suppressing various types of supply noise. However, the complex interactions between the active voltage regulators and the large passive sub-network may render the complete power delivery network (PDN) unstable. While traditional stability measures such as phase margin are not applicable to PDNs with a huge number of loops, brute-force analysis of network stability can be impractical due to the huge network complexity.

We have proposed a new hybrid stability concept, termed as hybrid stability margin (HSM), and the associated stability checking method for PDNs with integrated linear low-dropout voltage regulators (LDOs). With theoretical rigor, the proposed approach is local in the sense that the stability of the entire network can be efficiently examined through a hybrid stability constraint that is defined locally for individual LDOs. With the introduction of HSM, we have developed a new HSM-based LDO design flow. As shown in Fig. 1, this new design flow resembles the well-familiarized analog design flows that are based on a traditional stability metric such as phase margin. After the passive sub-network of the PDN (on-chip power grids and the package) is characterized, the new design flow is local to analog designers and can be readily incorporated in today's standard analog design environment.

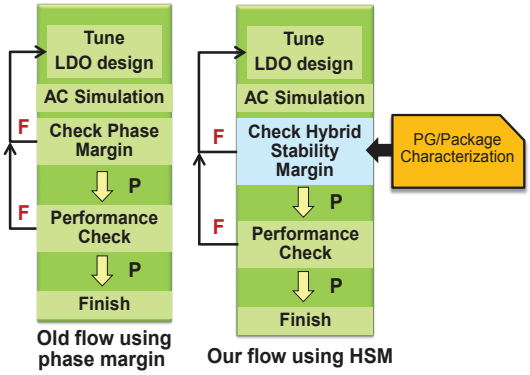


Figure 1: Stability design flow based on a traditional stability metric (e.g. phase margin) vs. the HSM-based design flow.

Utilizing our HSM concept and design flow, we have investigated how HSM can be ensured by introducing minor modifications into standard LDO topologies. As an example, Fig. 2 shows two identified design schemes.

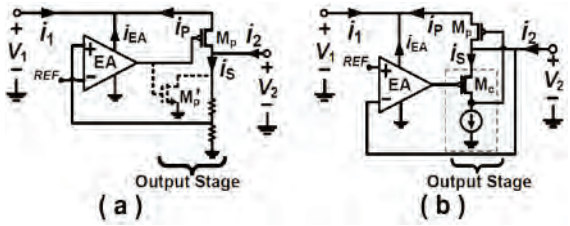


Figure 2: Exemplary HSM-enhancing LDO design schemes: a) simple output stage modification, and b) topological change for the output stage.

Keywords: Power delivery, distributed voltage regulation, LDO, hybrid stability, locality.

INDUSTRY INTERACTIONS

IBM, Texas Instruments, Intel, AMD

MAJOR PAPERS/PATENTS

[1] S. Lai, B. Yan, P. Li, "Localized stability checking and design of IC power delivery with distributed voltage regulators," IEEE TCAD, Sept. 2013.

[2] S. Lai, B. Yan, P. Li, "Stability-ensured design methodology for distributed on-chip linear voltage regulators in modern IC power delivery networks," SRC Techcon, Sept. 2013.

TASK 1836.063: POWERLINE COMMUNICATIONS FOR ENABLING SMART GRID APPLICATIONS

BRIAN L. EVANS, THE UNIVERSITY OF TEXAS AT AUSTIN, BEVANS@ECE.UTEXAS.EDU

SIGNIFICANCE AND OBJECTIVES

Powerline communication (PLC) systems have been deployed to provide two-way communications between local utilities and smart meters for smart grid applications. Communication performance of PLC systems is limited by non-Gaussian noise. In this project, we aim to improve communication efficiency and reliability of PLC systems in non-Gaussian noise.

TECHNICAL APPROACH

We first study the structure of powerline noise by statistically analyzing and modeling the noise properties in both time and frequency domains, based on several field measurements. We then study PLC transmitter and receiver techniques to improve the communication throughput and reliability in the presence of non-Gaussian noise. We develop real-time PLC testbeds to take noise measurements and quantify communication performance vs. complexity tradeoffs of various noise mitigation algorithms.

SUMMARY OF RESULTS

Our field measurements with Aclara and Texas Instruments on outdoor medium-voltage (MV) and low-voltage (LV) power lines have shown that cyclostationary noise is the dominant noise component in the 3-500 kHz band for narrowband PLC (Fig. 1). Based on field measurements, we propose a linear periodically varying system model to characterize the temporal and spectral properties of the noise. The proposed noise model has been accepted to IEEE P1901.2 standard.

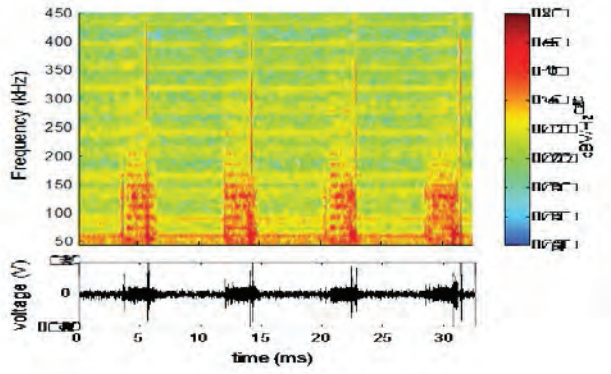


Figure 1: Spectrogram and time-domain trace of powerline noise collected at a LV site near St. Louis, Missouri USA.

To improve the robustness of PLC systems in the presence of cyclostationary noise, we propose noise mitigation algorithms at PLC receivers, which estimate and subtract the noise from received signals. In simulations, our proposed methods have achieved up to 6 dB of SNR gain over conventional PLC systems (Fig. 2).

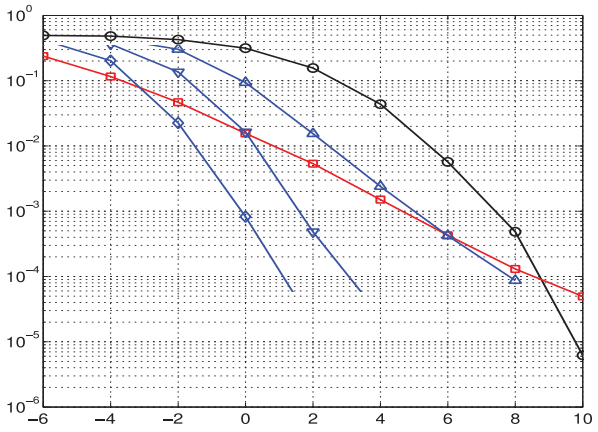


Figure 2: Coded bit error rate (BER) performance of our sparse Bayesian learning (SBL) algorithms vs. conventional PLC systems with time-domain (TDI) or frequency-domain (FDI) interleaving. SBL exploits frequency-domain structure of the orthogonal frequency domain modulation signal, which is based on the fast Fourier transform. DF is decision feedback.

We have developed three real-time testbeds to

(1) Evaluate communication performance vs. complexity tradeoffs of transmitter and receiver algorithms;

(2) Evaluate PLC receiver designs for impulsive noise mitigation using sparse Bayesian learning on FPGAs; and

(3) Measure powerline noise using a G3-PLC testbed.

Keywords: powerline communications, smart grid, cyclostationary noise, noise mitigation, testbed

INDUSTRY INTERACTIONS

Conference call every other week with TI and separately with Freescale. Jing Lin was a summer 2013 intern at TI, and Karl Nieman was a summer 2013 intern at Freescale.

MAJOR PAPERS/PATENTS

[1] J. Lin, M. Nassar and B. L. Evans, "Impulsive Noise Mitigation in Powerline Communications Using Sparse Bayesian Learning", *IEEE J. Sel. Areas Comm.,* Jul. 2013.

[2] M. Nassar, J. Lin, Y. Mortazavi, A. Dabak, I. H. Kim and B. L. Evans, "Local Utility Powerline Communications in the 3-500 kHz Band: Channel Impairments, Noise, and Standards", *IEEE Signal Processing Mag.,* Sep. 2012.

[3] K. Nieman, M. Nassar, J. Lin and B. L. Evans, "FPGA Implementation of a Message-Passing OFDM Receiver for Impulsive Noise Channels", *Asilomar Conf. on Signals, Systems & Comp.* Nov. 2013.

TASK 1836.069: ELECTRONIC SYSTEMS FOR SMALL- SCALE WIND TURBINES

RICHARD MCMAHON, UNIVERSITY OF CAMBRIDGE, RAM1@CAM.AC.UK

SIGNIFICANCE AND OBJECTIVES

This project looks at the electrical system of small-scale wind turbines of power ratings up to 5 kW, with the aim of reducing the cost of this electronics, chiefly by eliminating sensors and replacing them with more advanced control. Advance control will also increase the reliability of the whole system.

TECHNICAL APPROACH

Advanced control has been proposed to achieve maximum extraction of the power generated by generators driven by small-scale wind turbines. The power extraction is done by controlling the speed of a permanent magnet synchronous generator (PMSG). The output from the generator is rectifier with a Voltage Source Inverter (VSI) onto a fixed voltage DC link, potentially offering a lower cost solution with better control possibilities. Sensorless sliding mode control, speed and torque estimators and maximum power point tracking algorithms have been designed and implemented successfully on the test-rig.

SUMMARY OF RESULTS

Four different sensor based advanced controllers: PI, Sliding mode, Fuzzy logic and Port Controlled Hamiltonian were successfully tested on the wind turbine emulator test-rig commissioned in the previous stages of this project.

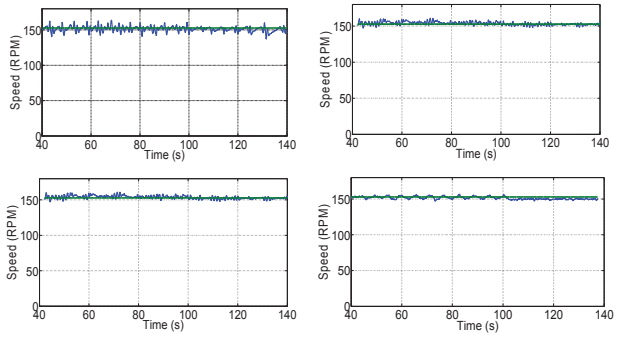


Figure 1: Sensor based advanced controllers. Top left: PI. Top right: Sliding mode. Bottom left: Fuzzy logic. Bottom right: Port Controlled Hamiltonian.

Sliding mode control has shown the best performance with reduced computational requirements. Fuzzy logic has also good performance, but its relatively high computation requirements could limit its applicability, particularly looking at further stages were the estimation and monitoring algorithms would be executed in a single low cost embedded device. As a consequence, sliding mode control was the natural choice for further research. Later on, an Extended Kalman filter was proposed to estimate the generator speed and shaft position (key variables for speed control of electrical machines). Also a wind turbine torque estimator was designed to monitor this variable and use it as input to the sensorless maximum power point tracking algorithm.

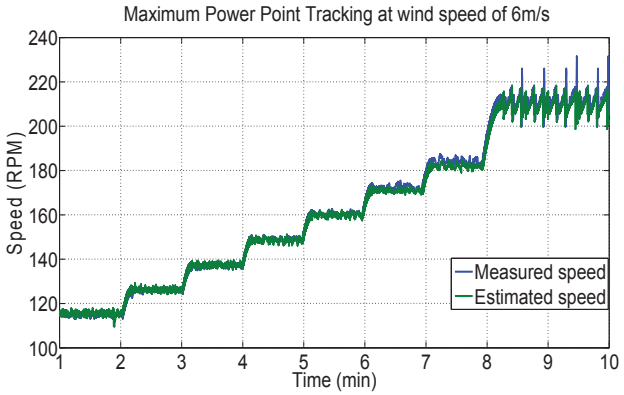


Figure 2: Sensorless speed control and Maximum Power Point Tracking algorithm evaluated on the test-rig

The main challenge of this application is the harsh working environment of the system. Wind conditions cannot be controlled, but wind is the power source, so estimation and control algorithms must be more robust and reliable than the techniques used for motor drives.

Keywords: PMSG, sliding mode control, sensorless control, MPPT, wind turbine

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] D Llano, M Tatlow and R McMahon, “Control Algorithms for Permanent Magnet Generators Evaluated on a Wind Turbine Emulator Test-Rig,” PEMD-14, April, 2014, Manchester, UK.

[2] D Llano and R McMahon, “Maximum Power Point Tracking and Sensorless Control for Permanent Magnet Generators Tested on a Wind Turbine Emulator,” EPE-14, August, 2014, Lappeenranta, Finland.

TASK 1836.070: OPTIMUM CONTROL OF POWER CONVERTERS

JOHN V. RINGWOOD, NATIONAL UNIVERSITY OF IRELAND - MAYNOOTH,
JOHN.RINGWOOD@EENG.NUIM.IE

SIGNIFICANCE AND OBJECTIVES

The project is aimed at designing and implementing digital optimum control for variable-frequency flyback converters. The control solution should provide a high energy conversion efficiency, global stability, high performance and most importantly can be implemented with a low-cost microcontroller.

TECHNICAL APPROACH

Three major steps, consisting of control architecture development, compensator design and implementation, are carried out one after another. The first stage focuses on integrating different control functions, e.g. efficiency optimization, primary-side sensing (PSS), into a unified control architecture while the compensator of the proposed control solution, which is synthesized based on different control theories, is compared in the second stage. Finally, a TI C2000 microcontroller is used as a means to implement the proposed optimum control. Both experimental and simulated results are generated for validation.

SUMMARY OF RESULTS

The architecture of the proposed digital optimum control for a flyback converter is illustrated in Fig. 1, where the output voltage is first estimated by the PSS block and then used as a feedback signal for the compensator and the peak current model control. The role of the efficiency optimizer is to find the switching frequency that maximizes the efficiency of the converter. The operating principle of different blocks in Fig. 1 can be found in [1].

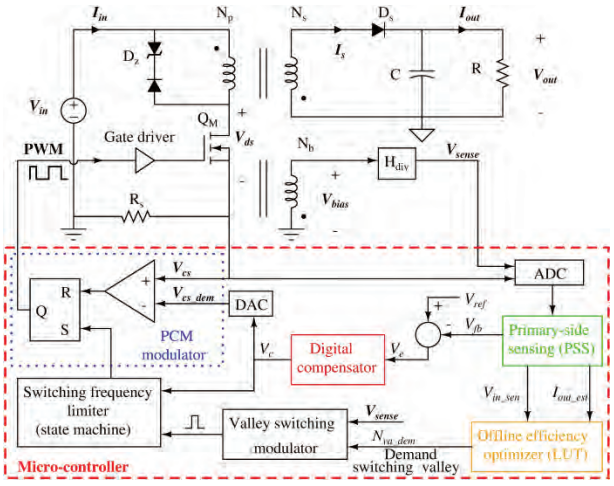
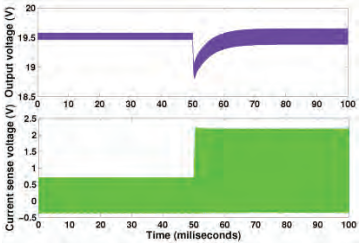


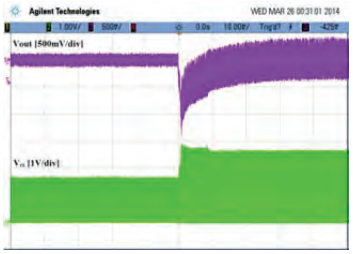
Figure 1: Block diagram of the proposed optimum control for a flyback converter.



(a) Simulation results:

V_{out} = upper curve

V_{cs} = lower curve



(b) Experimental results:

V_{out} = upper curve

V_{cs} = lower curve

Figure 2: Simulation and experimental results of the converter output voltage and inductor current in response to a 0.165A to 3.15A step load with V_{in} = 150V

Two control theories, including robust control and gain-adaptive predictive functional control, have been applied to synthesize the compensator for the proposed solution (Fig. 1). The stability and performance of such controllers are reported in [1] and [2]. Figure 2 plots the converter transient response over different working conditions from both experiment and simulation when the gain-adaptive functional predictive controller in [1] is used. The simulation results (Fig. 2) are obtained based on the control-oriented model developed in [3].

Keywords: Primary side sensing, digital control, flyback converter, efficiency optimization, robust control.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] T. T. Vu, S. O'Driscoll and J.V. Ringwood, "Efficient Fixed Parameter Digital Control of Power Converters," Proc. IEEE ISIE 2014, June 2014

[2] T. T. Vu, S. O'Driscoll and J.V. Ringwood, "A Feasibility study into the Robust Control of a Variable-Frequency Wide Operating Range Flyback Converter," Proc ISSC 2014, June 2014

[3] T. T. Vu, S. O'Driscoll and J.V. Ringwood, "Control-Oriented Modeling and Simulation of a Variable-Frequency Efficiency-Optimized Flyback Converter", IEEE Multi-conference on System and Control 2014, Nice, France, accepted

TASK 1836.076: ULTRA-LOW POWER DELAY-INSENSITIVE ASYNCHRONOUS CIRCUITS

JIA DI, UNIVERSITY OF ARKANSAS, JDI@UARK.EDU
SCOTT SMITH AND H. ALAN MANTOOTH, UNIVERSITY OF ARKANSAS

SIGNIFICANCE AND OBJECTIVES

This project will evaluate the integration of MTCMOS power gating with delay-insensitive asynchronous logic for reducing energy consumption in both active and standby modes, as well as explore the ultra-low voltage asynchronous circuit design opportunity.

TECHNICAL APPROACH

Since the spacer cycle of a dual-rail delay-insensitive asynchronous component is equivalent to gating the power of this component and forcing the output to logic 0, these circuits can enter sleep mode after every data cycle, while the circuit is in operation, and the handshaking signals between registers can be used as sleep control signals to control the power gating transistors. This approach has several merits: 1) limiting leakage in both active and sleep modes; 2) alleviating the effort and complexity of designing the sleep signal generation mechanism; 3) reducing the area overhead; and 4) facilitating the tool flow development.

SUMMARY OF RESULTS

Delay-insensitive asynchronous logic like the NULL Convention Logic (NCL) utilizes dual-rail encoding to achieve delay-insensitivity. A NCL system consists of delay-insensitive combinational logic sandwiched between NCL registers, which use handshaking signals to coordinate circuit behavior. NCL circuits are comprised of 27 threshold gates and MTCMOS power gating structure is implemented inside each threshold gate. In order to maintain delay-insensitivity and maximize leakage saving, a series of innovations including early-completion detection, sleep-enabled register and completion detection unit design, have been applied. Incorporating MTCMOS power gating mechanism in NCL (denoted as MTNCL) has the potential to result in significant savings in energy consumption without large overhead in area.

The second test vehicle, MSP430 core, has been designed in MTNCL. Fig. 1 shows the top-level diagram. Using the synchronous openMSP430 design on Opencores.org (http://opencores.org/project,openmsp430,overview) as reference, the MTNCL version includes all essential circuit components, e.g., ALU, control finite state machine (FSM), register file, and timer. Both the 1KB program memory and the 128B data memory have been designed and laid out using the IBM 8RF 130nm bulk CMOS process. Excluding the timer, the entire design is asynchronous and is controlled through MTNCL handshaking. A synchronous-asynchronous interface is designed and placed in between the asynchronous core and the timer. Internal and external interrupt handling circuits have also been designed. The MTNCL core has been verified using the same comprehensive testbench as the one in the openMSP430 design suite.

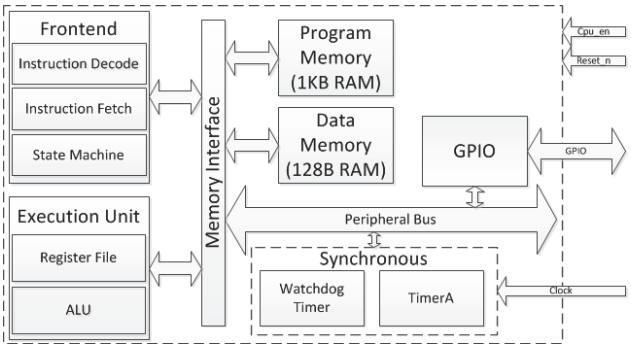


Figure 1: Top-view of the MTNCL MSP430 core.

A preliminary tapeout has been completed in late July. The process used was the GLOBALFOUNDRIES 65nm bulk CMOS process. Both versions of the MSP430 core, i.e., synchronous and MTNCL, were integrated on the test chips. Memory blocks and peripherals were excluded from this tapeout due to the short tapeout deadline. The experience gained will reduce the design time and risk for the final tapeout.

The final tapeout at MOSIS is planned to take place in November 2014 using the IBM 8RF process. Both versions of the MSP430 core will be included. Memory and timers will be integrated into each version for fair comparison. Chip testing will take measurements of active energy, leakage power, performance, and voltage scalability. The results will be analyzed and summarized in the final report.

Keywords: MTCMOS, delay-insensitive, asynchronous, ultra-low power, CAD tool

INDUSTRY INTERACTIONS

Intel, AMD

MAJOR PAPERS/PATENTS

[1] M. Hinds et al., “An Asynchronous Advanced Encryption Standard Core Design for Energy Efficiency,” Journal of Low Power Electronics, Vol. 9, No. 2, pp. 175-188, 2013.

TASK 1836.081: COMBINED INDUCTIVE/CAPACITIVE DC-DC CONVERTER

RAMESH HARJANI, UNIVERSITY OF MINNESOTA, HARJANI@UMN.EDU

SIGNIFICANCE AND OBJECTIVES

This project will develop and experimentally demonstrate innovative on-chip power regulation techniques suitable for application in block level Dynamic Voltage Scaling (DVS). The research will focus on developing optimal power converters based on a unified design framework so that they can cater to a wide range of output powers and being area efficient.

TECHNICAL APPROACH

A hybrid inductive/capacitive converter with inductive supporting higher loads and capacitive the lighter load was taped out and measured in 32nm SOI. To optimize the capacitive part a design framework is developed. The framework models all converter (buck/boot) families providing design insights and tradeoffs among the various topologies. We select the 10 optimal topologies that always perform better than any of the 96 permutations that are possible for series-parallel converters. A logical extension of the framework includes the impact of parasitics and other second order effects including partial charging of bucket capacitors and finite tank capacitor size. In order to demonstrate the utility of this framework we show a design in 65 nm. A high efficiency, low power controller based, 14 phase interleaved converter is designed for wide output range.

SUMMARY OF RESULTS

We demonstrated a combined inductive/capacitive converter taped out in 32 nm SOI [1] (Fig. 1). The peak Efficiency (measured) was 76% working in inductive mode. In the later phase of the project we developed a unified design framework for series-parallel capacitive converters in order to achieve the most optimum conversion solution for a given input/output condition. Fig. 2 depicts the major steps starting from choosing the conversion gain (Fig. 2a) then the suitable topological family (Fig. 2b) followed by modeling of parasitic and second order effects (2c, 2d, 2e). These steps give the optimum open loop implementation. Fig. 2f shows the final step of optimal regulation of the open loop.

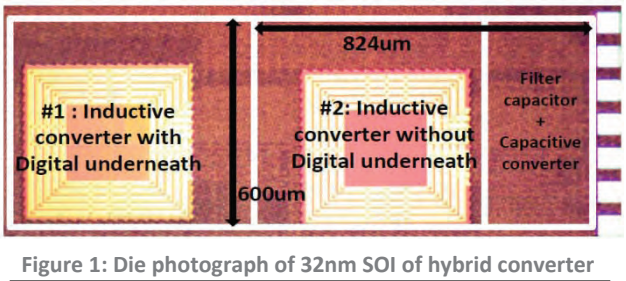


Figure 1: Die photograph of 32nm SOI of hybrid converter

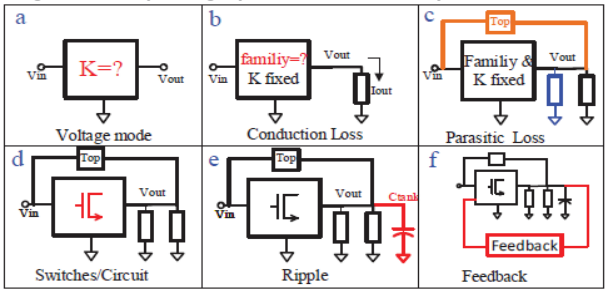


Figure 2: Design steps based on the unified framework

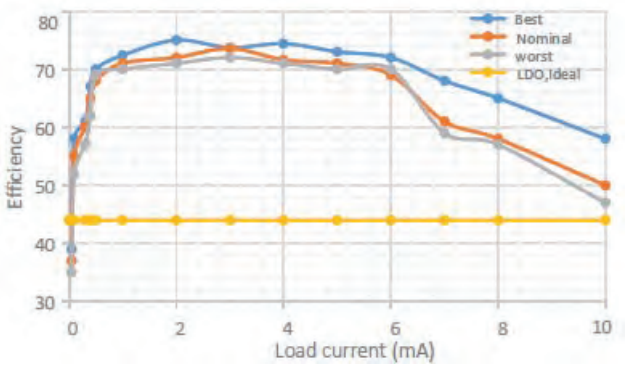


Figure 3: Simulated efficiency of the wide output converter based on unified framework

To evaluate the above framework a wide output, low ripple 2:1 step down capacitive converter is being taped out in TSMC 65 nm. The input is 1V and the regulated output voltage in 460mV. The design maintains an average power efficiency above 60 % for a load range of 50uA to 7mA (Fig. 3). The maximum simulated efficiency of 77% is achieved at load of 2 mA. The worst case ripple for this design is 7%.

Keywords: combined converter, unified design framework, wide output power.

INDUSTRY INTERACTIONS

Intel, IBM , Texas Instruments and Freescale

MAJOR PAPERS/PATENTS

[1] S. S. Kudva, S. Chaubey and R. Harjani, “High Power-Density, Hybrid Inductive/Capacitive Converter with Area Reuse for Multi-Domain DVS” IEEE Custom Integrated Circuits Conference, September 2014.

[2]R. Harjani and S. Chaubey, “A Unified Framework for Capacitive Series-Parallel DC-DC Converter Design,” (Invited) IEEE Custom Integrated Circuits Conference, September 2014.

TASK 1836.084: SINGLE SET-UP DETAILED TESTING OF WIRELESS TRANSCEIVERS FRONT-ENDS USING DIGITAL PROCESSING

SULE OZEV, ARIZONA STATE UNIVERSITY, SULE.OZEV@ASU.EDU

SIGNIFICANCE AND OBJECTIVES

Testing and calibration of RF transceivers take too much effort in terms of cost and time. Built-in-self test can alleviate these problems but it is too costly if conducted in a traditional way. This project aims at developing self-test techniques using the resources already available on the chip and adding minimal overhead if existing resources fall short.

TECHNICAL APPROACH

The way of using existing resources is to loop-back the transmitter output to the receiver input and thereby generating a low-frequency path. However, this generally introduces the problem of parameters being coupled. We develop extensive mathematical models and derive the necessary test signal conditions such that the parameters of the transmitter can be decoupled from the parameters of the receiver.

SUMMARY OF RESULTS

During this project, we developed mathematical models for both traditional Cartesian transceivers and polar transceivers. We developed mathematical methods for calculating each parameter of interest, including I/Q mismatch, DC offsets, non-linearity parameters, path gain, and error vector magnitude. We have also demonstrated these techniques in hardware using off-the-shelf components. We designed additional built-in-self test circuits when loop-back alone did not give us adequate information. We have also shown that once these parameters are measured, the system can easily be calibrated to minimize the effect of circuit impairments.

Table I: Parameter measurement accuracy

Parameter	Trad.	This Work
g_{tx} (%)	-68	-69
g_{rx} (%)	-65	-68
ϕ_{tx} (˚)	31.2	35.9
ϕ_{rx} (˚)	64	66.8
IIP3 (dBm)	12.23	12.57
IIP3 (dBm)	13.28	13.16

As an example to our results, Table I shows the accuracy of parameter measurement for a Cartesian transceiver in the loop-back mode. The baseline measurement is the traditional measurement that is conducted with RF instrumentation. Table II shows the results of EVM calculation based on measured parameters and how that compares to EVM measurement.

Table II: EVM calculation accuracy

MM (°)	MM	IIP3 dBm	AM/AM dB	Gain dB	EVM meas	EVM calc
1	0.10	6.2	0.1	-20	5.2	5.17
			0.25	-12	9.3	10.2
			0.36	-10	15.9	15.6
3	-0.20	6.2	0.1	-20	10.4	10.3
			0.25	-12	12.8	13.0
			0.36	-10	18.1	17.9
-2	0.15	6.2	0.1	-20	8.0	8.0
			0.25	-12	10.5	10.7
			0.36	-10	15.6	15.5

Keywords: EVM measurement, RF test, Built-in-self-test, parameter de-embedding

INDUSTRY INTERACTIONS

- Texas Friedrich J. Taenzler (TI)
- Shreyas Sen (Intel)
- Mustapha Slamani (IBM)

MAJOR PAPERS/PATENTS

1. Nassery, A; Ozev, S., "An Analytical Technique for Characterization of Transceiver IQ Imbalances in the Loop-Back Mode," DATE, pp.1084-1089, 2012.
2. Nassery, A; Erol, O.E.; Ozev, S.; Verhelst, M., "Test Signal Development and Analysis for OFDM Systems RF Front-End Parameter Extraction," Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , vol.31, no.6, pp.958-967, June 2012.
3. Nassery, A; Byregowda, S.; Ozev, S.; Verhelst, M.; Slamani, M., "Built-in-Self Test of Transmitter I/Q Mismatch Using Self-Mixing Envelope Detector," VTS, pp.56-61, 2012.
4. Nassery, A; Ozev, S.; Verhelst, M.; Slamani, M., "Extraction of EVM from Transmitter System Parameters," ETS, pp.75-80, 2011.
5. Nassery, A; Ozev, S.; Slamani, M., "Analytical Modeling for EVM in OFDM Transmitters Including the Effects of IIP3, I/Q Imbalance, Noise, AM/AM and AM/PM Distortion," ETS, 2013.
6. Nassery, A; Jae Woong Jeong; Ozev, S., "Zero-Overhead Self-Test and Calibration of RF Transceivers," ITC, 2013.

TASK 1836.088: EFFICIENT SWITCHING MODE DIGITAL-INTENSIVE WIRELESS TRANSMITTERS UTILIZING SWITCHING MODE PAS

RANJIT GHARPUREY, THE UNIVERSITY OF TEXAS AT AUSTIN, RANJITG@MAIL.UTEXAS.EDU

SIGNIFICANCE AND OBJECTIVES

The efficiency of radio transmitters and power amplifiers (PA) continues to pose a significant challenge in the design of battery-operated wireless communication systems as well as in base station applications. The goal of this work is to investigate the use of switching power amplifiers and suitable modulation schemes for enhancing efficiency.

TECHNICAL APPROACH

Two-level modulation schemes such as PWM are well suited for use with efficient switching power amplifiers. These schemes are inherently digital friendly and therefore can be implemented in low-cost CMOS technologies. An RFPWM generator that employs PLL-based PWM generation at baseband is employed in this work. This PWM generator avoids the requirement for an accurate ramp reference and high-speed comparator. Transmitters with I-Q and polar inputs have been designed. The RFPWM output is applied to a class D power amplifier. Predistortion is employed to minimize out-of-band spurs.

SUMMARY OF RESULTS

The phase-locked loop (PLL) based RFPWM transmitter has been designed and implemented in a 65nm CMOS process. Both polar and I-Q based transmitters have been attempted. Fig. 1 shows an overview of the RF PWM transmitter based on an I-Q to polar transformation. In the proposed design, the RF output signal $x(t) = a(t)\cdot\cos[\omega t + \phi(t)]$ is generated without an upconverter. Additionally, pre-distortion of the baseband signal is employed in order to reduce out-of-band spurs.

To generate a PWM signal without a high speed ramp generator, a PWM generator [1] based on a PLL was proposed previously. The PWM signal is derived from the output of the phase detector in the design. An analog input is compared to the local average of the PWM output. In the locked state, the loop ensures that the local average of the PWM signal is a replica of the input signal. RF PWM signals are generated from two PLL-based PWM modules that employ a reference clock signal (f_{ref}). The modules employ six-stage ring VCOs, which ensures wideband operation. Further this is a digital intensive design with a small area requirement compared to an LC VCO. The use of ring oscillators also allows for the system to operate over multiple bands, which is accomplished by changing the reference clock. The output PWM signals are reshaped to prevent shoot-through currents within the level shifter and PA driver. This is critical to avoid efficiency degradation. These signals subsequently drive differential class D PAs that employ a stacked inverter design. The PA stage uses a supply of 2.4 V. The output load impedance is assumed to be 12.5 Ohms. An external impedance transformer will be employed to achieve this impedance.

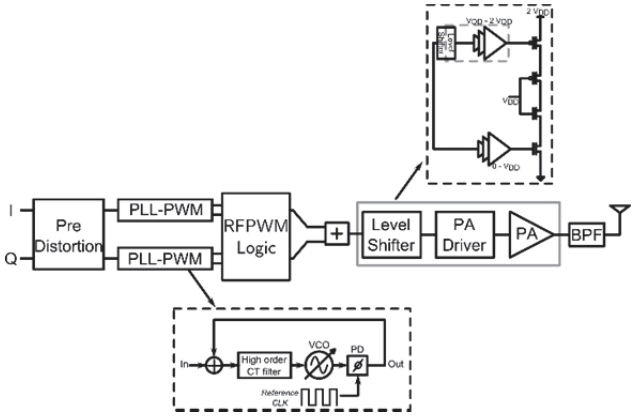


Figure 1: RFPWM architecture

The complete transmitter (Fig. 1) consists of two PLL-based PWM modules, an RF PWM generator, and a PA stage which includes a level shifter, a PA driver, and a class D output stage. The design is intended for standards in the GHz RF frequency band, e.g, 1.85 GHz LTE and 2.4 GHz WLAN, but can be customized for other bands. The simulated maximum power in the 65nm process is 24 dBm. The complete transmitter has an efficiency of 48% at this power, for an unmodulated sinusoidal output.

The IC parts will be housed in 48-pin QFN packages and measured on the board. The design will be tested at different carrier frequencies and modulation bandwidths.

Keywords: PWM, digital modulation, wireless transmitters, switching mode PAs.

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] J. Lu, H. Song, and R. Gharpurey, "A CMOS class-D line Driver Employing a Phase-Locked Loop Based PWM Generator," IEEE Journal of Solid-State Circuits, vol. 49, pp. 729–739, March 2014.

TASK 1836.099: AUTOMATED SWITCHING REGULATOR MODELING

ALAN MANTOOTH, UNIVERSITY OF ARKANSAS, MANTOOTH@UARK.EDU

SIGNIFICANCE AND OBJECTIVES

The goal of this project is to automate the generation of switching regulator behavioral model. At project end the tool should be capable of rapidly generating simulation models for a wide range of switching regulators. This will result in models that are more accurate than hand created models and simulate more quickly.

TECHNICAL APPROACH

The behavioral models are derived from the Vorpérian PWM switch model which replaces the simulation time costly switching element with a time averaged representation. This drastically reduces simulation time with little loss in fidelity.

Automation is accomplished through two means. The first is the simple interface taking raw regulator parameters such as switching frequency, inductor size, duty cycle limits, etc. as inputs. The second key is a curve fitting algorithm which ensures a best fit tradeoff between transient behavior, AC magnitude, and AC phase through simulation.

SUMMARY OF RESULTS

Over the previous year the main accomplishment was to implement the necessary features to successfully generate and simulate a model from datasheet information. Additionally, many software issues have been addressed, paths to integration for all planned features have been identified, and more advanced extensions are being considered for future work.

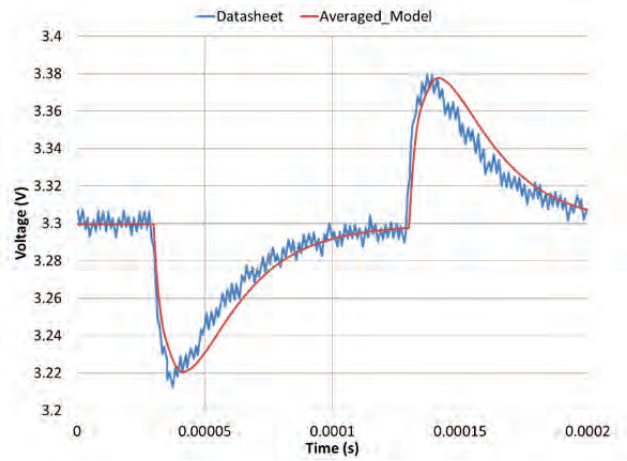


Figure 1: Results from simulation of a semi-automatically generated model of the TPS54320 compared with datasheet data.

The program architecture is a hierarchical approach which makes the model generation process more manageable and easy to develop. The tool is implemented in the Python scripting language with four main modules performing the core capabilities.

In addition to underlying functionality there have also been advances in user interfacing functionality such as user interface planning, error logging and reporting, and improved documentation both in code and in reference information.

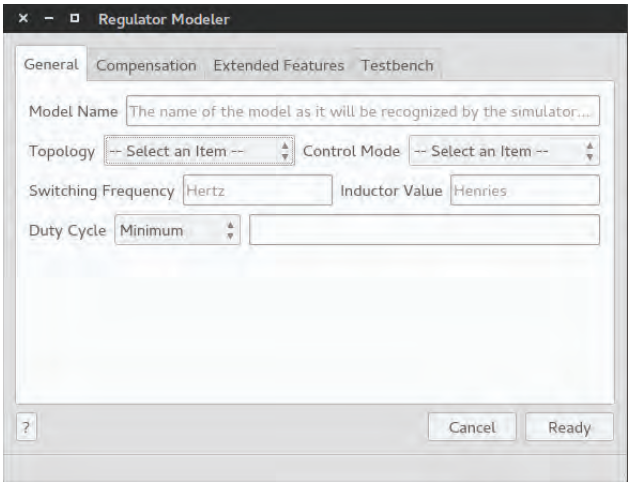


Figure 2: Mockup of simple user interface for creating switching regulator models.

For the remainder of the project the focus will be on closing the final tasks of automating the compensation network generation process and to achieve tie-in with ModLyng.

Future directions may involve the addition of advanced regulator features such as protection schemes, more realistic behavior at operating limits, etc.

There also exists the possibility of implementing event-driven mixed-signal models of the same regulators which would allow for the possibility of simulating in a digital simulator. This would be very useful for system level simulations where the switching regulator dominates the simulation time and causes bottlenecks.

Keywords: switching regulator, modeling, behavioral modeling, automation, software

INDUSTRY INTERACTIONS

Texas Instruments, Freescale

MAJOR PAPERS/PATENTS

None

TASK 1836.104: FAULT TOLERANT INVERTER MODULE FOR DSSRM DRIVE

BABAK FAHIMI, THE UNIVERSITY OF TEXAS AT DALLAS, FAHIMI@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

The motivation behind this task is to engineer a solution for stationary placement of power switches in power converters which can allow for a dynamic circuit topology thereby elevating the size, cost, and complexity issues associated with current technology. The dynamic relocation is attained through piezoelectric (PE) actuation which will generate new opportunities in effective thermal management and reduced part converter topologies for substantial saving in developmental cost and the required footprint.

TECHNICAL APPROACH

A four phase converter is used for a case study, where current in each coil is controlled by one individual asymmetric bridge. Fig.1 shows the proposed model of a PE actuator with the same purpose. The actuator consists of a central fixed copper contact head and four peripheral movable copper contact heads. Each peripheral contact head is bonded to a PE bimorph beam. Upon being actuated, PE bimorphs experience deflection via inverse piezoelectric effect and a physical contact can be created between central and peripheral contact heads to complete the circuit for the corresponding phase. Each beam can be controlled via voltage activation. The model was simulated in ANSYS software using finite element method for simulations.

SUMMARY OF RESULTS

Finite element method of the simplified PE actuator was applied for modal analysis, static analysis, and transient analysis. First, modal analysis was performed to retrieve the natural frequencies and different modes of operation. With an intention to operate in non-resonant mode, natural frequencies were avoided and deflection direction was matched with the fundamental mode of vibration of the beam to maximize the desired deflection.

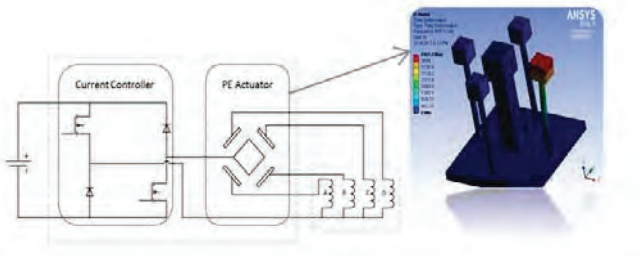


Figure 1: Converter with Piezoelectric Actuator Model.

Moreover, blocked force and tip deflection are two very important parameters determined through static analysis. The blocked force results in deflection upon movement being allowed. The maximum attainable deflection determines the gap that can be maintained between the two copper contact heads, hence, governs the amount blocking voltage that can be safely maintained when the copper heads are not in contact. For the actuating PE beam depicted. In addition, transience time is another parameter of interest for the design of the actuator. Considering non-resonant mode operation, for every actuating pulse signal, the time taken by the actuating PE beam to attain steady state deflection determines the speed of the system (Actuation time). Finally, the design limitations observed from FEA analyses are: power transfer capacity – determined by total deflection and size, and actuation time. Realizing the geometric dependence of these parameters, optimal point of operation was determined by observing the effect of modification of each geometrical dimension. Table 1 displays the optimized measured parameters for the PE actuator model.

Table 1: Parameters of optimized PE actuator model

Deflection (um)	Actuation Time (ms)	Conduction Current (A)	Blocking Voltage (V)
37.085	8.4	6.2	111.26

In conclusion, a new dynamic actuating topology is introduced to eliminate the redundancy from the conventional converter topologies, resulting in increase of size and cost efficiency. Exploiting the piezoelectric properties of the piezoelectric crystals, an electromechanical system is designed to create such dynamic switching effects. Power limitation with decreasing size and speed limitation with increasing size creates a tradeoff between attainable power transfer and frequency of operation. A test bed of the proposed model has been built and tested successfully.

Keywords: Piezoelectric, Power Converters, DSSRM, Actuation Time, Deflection

INDUSTRY INTERACTIONS

Texas Instruments, Intel, AMD

MAJOR PAPERS/PATENTS

[1] L. Maharjan, N. Arbab, B. Fahimi, “Fault Tolerant Drive Module via Electromechanical Alteration of Circuit Topology” proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC 2014), Fort-worth, TX, March 19-23, 2014.

TASK 1836.105: CR-FREE SIMO DC-DC POWER CONVERTERS WITH NANO-SECOND LOAD TRANSIENT RESPONSE

DONGSHENG MA, THE UNIVERSITY OF TEXAS AT DALLAS, EMAIL: D.MA@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

It is desirable to keep the output voltage ripple of modern switching power converters low in high-performance systems. Meanwhile, the load transient response and dynamic voltage scaling (DVS) tracking speed are expected to be fast. A switching converter with both improved steady-state and dynamic performances is highly demanded.

TECHNICAL APPROACH

By using adaptive current compensation (ACC) technique, both the load transient response and DVS tracking speed of switching power converter can be significantly improved without increasing the switching frequency or reducing the filtering inductance. The proposed control method obviates large ESR for filtering capacitor. Therefore, the low output voltage ripple can be achieved simultaneously. The switching frequency is also stabilized to avoid generating randomized switching noise. Moreover, the high power efficiency is maintained since the load current is dominated by the output current of switching converter in steady state.

SUMMARY OF RESULTS

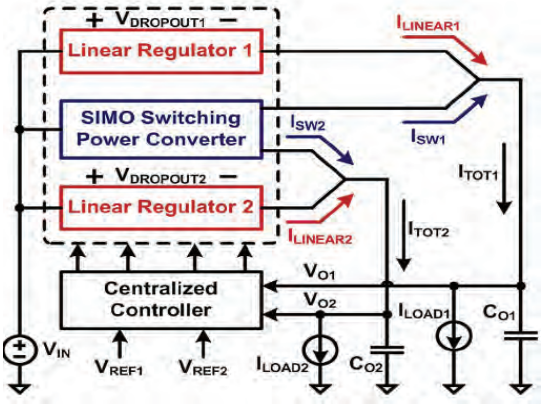


Figure 1: System block diagram of the proposed hybrid SIMO power converter.

Slow load transient response and potential cross-regulation effect are two major performance barriers for single-inductor multiple-output (SIMO) power converters. To overcome these barriers, this project proposes a parallel-structured hybrid SIMO power converter with an adaptive current compensation (ACC) technique, as illustrated in Fig. 1. With the employment of new and compact linear regulators, the proposed ACC technique improves both the step-up/down transient responses significantly without the needs on advanced controls or high switching frequency. The interactive duty ratio changes between sub-converters are also avoided due to the fast recovery during load transition periods. Cross-regulation effect is thus minimized.

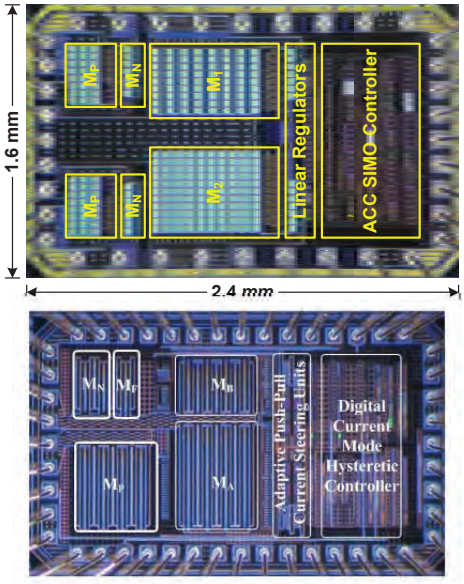


Figure 2: Chip Micrographs (top: analog solution, bottom: digital solution).

The proposed hybrid SIMO converters are designed and implemented using both analog and digital control. They are fabricated with a 0.35-µm CMOS process. The chip micrographs are shown in Fig. 2. Experimental results successfully prove that, with the proposed ACC techniques, the transient response times for both converters are improved by around 2 orders. Meanwhile, cross regulation issues due to dynamic transients are significantly minimized.

Keywords: adaptive current compensation, SIMO converter, cross regulation, fast transient response

INDUSTRY INTERACTIONS

TI, Intel, AMD

MAJOR PAPERS/PATENTS

[1] Y. Zhang, D. Ma, IEEE *JSSC*, pp. 1242-1255, Vol. 49, No. 5, May 2014.
[2] R. Bondade, Y. Zhang, D. Ma, IEEE ECCE, Pittsburg, PA, Sept. 2014, accepted for publication.
[3] Y. Wang, D. Ma, IEEE APEC, pp. 1366-1369, Long Beach, CA, Mar. 2013, (*Outstanding Presentation Award*).
[4] Y. Zhang, D. Ma, IEEE APEC, pp. 1962-1965, Long Beach, CA, Mar. 2013.

TASK 1836.106: IF-SAMPLING CMOS ADC FRONT-END WITH 100-DB LINEARITY

YUN CHIU, THE UNIVERSITY OF TEXAS AT DALLAS, CHIU.YUN@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

IF-sampling demands stringent tracking bandwidth and linearity performance of analog-to-digital converters, requiring high supply voltages and bipolar devices to implement the front-end circuitry. We present a calibration technique to linearize the CMOS sample-and-hold circuits for IF-sampling applications that can potentially achieve a spurious-free dynamic range of over 100 dB.

TECHNICAL APPROACH

A derivative-based error model is developed to address the dynamic nonlinearity in CMOS S/H circuits, which is mainly attributed to the nonlinear on-resistance of the MOS transistors. Our analysis reveals that the nonlinearity of the switch resistance is primarily caused by the drain-source voltage modulation effect. Based on this observation, a compact derivative-based error model is proposed for dynamic nonlinearity calibration. An analog high-pass filter derivative-estimation technique is further proposed to obtain direct derivative information (DDI) of the analog input. The S/H error model is also further simplified due to the availability of DDI with reduced digital computation load.

SUMMARY OF RESULTS

In the proposed derivative-based sample/hold dynamic error model (1), the nonlinearity correction terms (the second and third term) consist of the derivative of the sample/hold output voltage (dVout/dt).

$$V_{in} = V_{out} + \tau_0 \frac{dV_{out}}{dt} + \tau_1 \left|\frac{dV_{out}}{dt}\right| \frac{dV_{out}}{dt} \qquad (1)$$

Instead of using digital interpolation filter, an analog domain high-pass filter is utilized to estimate the derivative of sample/hold output voltage.

Consider a single-ended S/H circuit, in the small signal perspective, it can be seen as a low-pass filter. And the low pass filter output voltage can be written as

$$V_{out} = \frac{V_{in}}{1+sR_{on}C_S} = \frac{V_{in}}{1+s\tau} \qquad (2)$$

The derivative of sample/hold output voltage (dVout/dt) can be derived by multiplying the equation (2) with another **s**,

$$\frac{dV_{out}}{dt} \Rightarrow sV_{out} = \frac{sV_{in}}{1+s\tau} \qquad (3)$$

Notice that the equation (3) is essentially the transfer function of a high-pass filter with the same time-constant. This indicates the derivative of the sample/hold output can be estimated by using a high-pass filter (HPF).

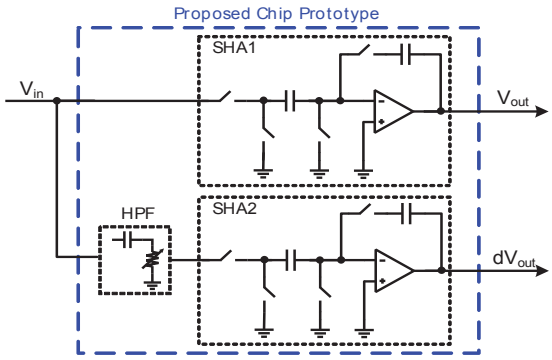


Figure 1: The block diagram of the proposed chip prototype

As shown in Fig. 1, the proposed chip prototype consists of two signal paths, which are the main signal path (SHA1) and the HPF derivative estimation path (SHA2). Both signal paths contain a sample/hold amplifier, which feeds the output voltage to two off-chip buffers respectively.

A 65-nm CMOS S/H circuit with an accompanying analog derivative filter is designed at transistor level and simulated in Spectre. The results (shown in Fig. 2) are post-processed using the proposed calibration model in MATLAB. The SFDR of the S/H is improved from 70 dB to over 100 dB for input frequencies up to 400 MHz.

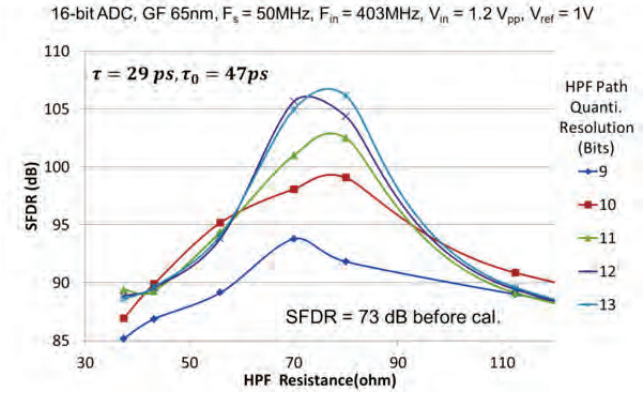


Figure 2: Calibration results of transistor level simulation

Keywords: IF-sampling, digital calibration, sample-and-hold, dynamic nonlinearity, direct derivative information

INDUSTRY INTERACTIONS

Texas Instruments

TASK 1836.110: DISTRIBUTED POWER DELIVERY ARCHITECTURE FOR 2D AND 3D INTEGRATED CIRCUITS

SAIBAL MUKHOPADHYAY, GEORGIA INSTITUTE OF TECHNOLOGY, SAIBAL@ECE.GATECH.EDU

SIGNIFICANCE AND OBJECTIVES

The primary objective is to design a low-loss, fully integrated, and robust distributed Power Delivery Unit for multicore processors targeting low output voltage from relatively high input voltage. The central innovation is a hybrid down conversion architecture composed of a central switched capacitor (SC) converter and multiple distributed inductive buck (IB) converter.

TECHNICAL APPROACH

The hybrid architecture combines the advantages of SC and IB providing following benefits for large down conversion factor: (i) reduced voltage stress across the power FETs compared to a single IB helping integrated DC-DC conversion; (ii) faster response and tighter output regulation compared to a single SC; and (iii) potential for better efficiency compared to a single stage (SC or IB) converter delivering the same output voltage/current as each stage in the hybrid converter operates at reduced conversion ratio and hence, higher efficiency. The circuit innovations are pursued to improve efficiency across wide variation of output voltage and load current.

SUMMARY OF RESULTS

Design of a hybrid converter: A step down converter consisting of a switched capacitor stage followed by an inductive buck stage is designed. The primary down conversion is achieved by an unregulated switched capacitor (SC) converter. The SC converter is designed to produce a 4:1 down conversion from an unregulated 4.8V DC supply. The output of the switched capacitor is then fed to the feedback controlled inductive buck regulator. The buck regulator is designed in synchronous current mode control with load depended variable frequency operation. The load current is sensed and after removal of high frequency components is fed to the oscillator that produces pulses proportional to the DC load current. The buck regulator ensures a tight regulation over the wide variation of input and load demand. The duty cycle can be adjusted to maximize the overall efficiency, by impedance matching between the load, buck converter and the switch capacitor converter. A test-chip is designed and taped-out in 130nm CMOS to study the characteristics of the hybrid converter (Fig. 1). The test-chip includes on-chip decoupling capacitors to minimize the effect of high-frequency noise due to bond-wires. The maximum conversion ratio is designed to be 16 (4.8V input to 0.3V output).

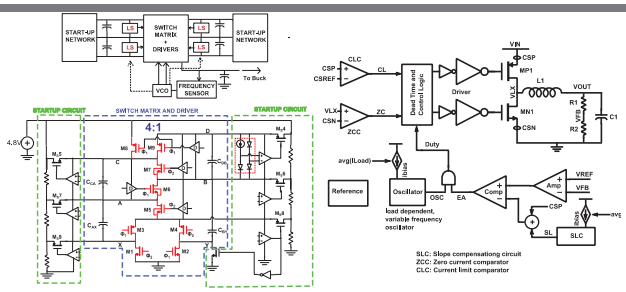


Figure 1: The topologies of the switched capacitor and buck converter.

Modeling/Analysis of Effect of Process Variation: We have analyze the effect of variations in inductor, capacitor, the power transistors, and the delay of the digital control loop, on the performance metrics of integrated voltage regulators (IVR) by performing Monte-Carlo simulations. Inductive IVRs are considered for analysis. The analysis shows that the variation in the output filter passives, specifically the inductor dominates the variability in the power loss, output voltage ripple, and load transient response (overshoot and settling time) of the IVR. The variation in the delay of the controller dominates spread in the voltage transients during transition of power state (i.e. change of output voltage during voltage scaling). We have used the supply voltage dependent delay and power characteristics of a digital circuit to map the effect of variations in IVR on the delay and power. The analysis shows that due to the elimination of the board/package level power delivery network, the variation in the IVR has a much stronger influence on the variations in power/performance of the digital circuits. The effect of IVR variations becomes more prominent on the system outputs at low-voltage/low-power operation of the core.

Keywords: integrated converters, hybrid conversion, efficiency, high conversion ratio, packaging

INDUSTRY INTERACTIONS

Texas Instruments, Intel, IBM, and AMD

MAJOR PAPERS/PATENTS

[1] M. Kar, et.al, “Impact of Process Variation in Inductive Integrated Voltage Regulator on Delay and Power of Digital Circuits,” ISLPED 2014.

[1] S. Carlo et.al, “On the Potential of 3D Integration of Inductive DC-DC Converter for High-Performance Power Delivery,” DAC 2013.

TASK 1836.112: SHORTSTOP: FAST POWER SUPPLY BOOSTING

DAVID BLAAUW, UNIVERSITY OF MICHIGAN, BLAAUW@UMICH.EDU
DENNIS SYLVESTER, UNIVERSITY OF MICHIGAN

SIGNIFICANCE AND OBJECTIVES

Shortstop requires precise timing of header switches for correct and efficient boosts of a processor core's power rail, with timing accuracy on the order of 100ps in a wirebond version [1]. Failure to correctly time switch can lead to excessive ringing, shorting, and droops, which wastes energy and causes failures.

TECHNICAL APPROACH

Shortstop includes two elements for accurately timed switch control, delay generators and maskable XOR trees. The timing system is triggered from a latched boost_*go* signal and includes 16 delay generators that each assert after a chosen amount in time, set by a scannable configuration bits. The maskable XOR trees select a subset of these delayed signals to generate pulsed switch enables, shown in Fig. 1. In the example, three delay generators assert at three points in time: T1, T2, and T3. The XOR combines all three delay generators to assert a pulse from T1 to T2, and reassert at T3.

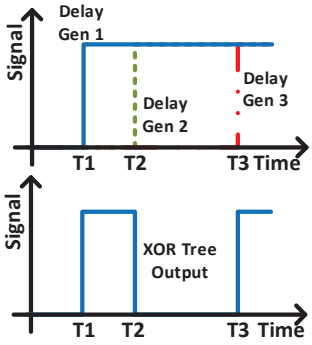


Figure 1: Principle of delay chain + XOR tree operation. Three delay chains select points in time T1, T2, and T3 (top of figure). The XOR tree combine the three points to create a pulsed output (bottom of figure).

SUMMARY OF RESULTS

The first silicon prototype of Shortstop [1] includes 16 delay generators, though in practice Shortstop only requires five delay generators: (1) charge share core to cap; (2) start shorting of dirty supply rails to charge parasitic inductor; (3) connect core to dirty supply rail for inductive boost; (4) connect core to high supply rail; (5) disconnect cap from high supply rail once charged and no energy remains in parasitic inductor. The extra delay generators were included on the first prototype to provide flexibility in testing different boost arrangements, and because each header/footer switch was split into sub-switches of varying sizes to allow gradual actuation. The sub-switches were sized in a binary fashion, so that switch strength could be increased over time by correctly timing additional delay generators to larger switches sizes.

A block diagram of the delay generator is shown in Fig. 2, and each generator includes fine- and course-grained controls. The fine-grain delay is adjusted by multiplexing between taps of a 31-buffer delay chain, while the course delay is adjusted by counting cycles of an asynchronous fast clock. The fast clock is enabled through the *boost_go* trigger signal and, if the coarse adjustment count is zero, this trigger is fed directly into the 31-element delay chain. The fine delay adjustment can be measured by putting the delay generator into a *loopback* mode, which configures the delay chain into a ring oscillator arrangement and observed off-chip.

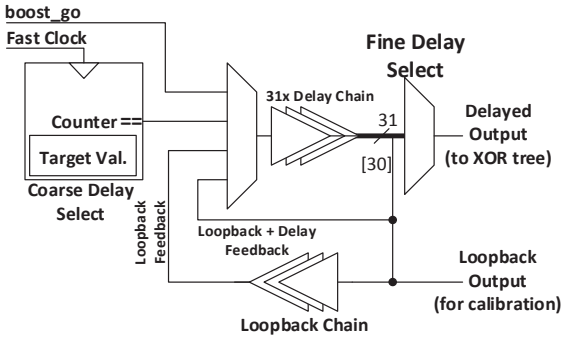


Figure 2: Delay generator element. Shortstop includes 16 of these delay elements.

An automatic tuning finite state machine, optimizing delay generator delays to minimize energy, has been proven in simulation.

Keywords: Power supply boosting, timing generation, near-threshold computing, dark silicon, dim silicon.

INDUSTRY INTERACTIONS

Liaisons: Zeynep Deniz (IBM) and Muhammad Khellah (Intel)

MAJOR PAPERS/PATENTS

[1] N. Pinckney, M. Fojtik, B. Giridhar, D. Sylvester, and D. Blaauw, "Shortstop: An On-Chip Fast Supply Boosting Technique," IEEE Symposium on VLSI Circuits, June 2013.

TASK 1836.115: ANALYSIS AND CHARACTERIZATION OF SWITCHED-MODE DC-DC POWER CONVERTERS

PENG LI, TEXAS A&M UNIVERSITY, PLI@TAMU.EDU

SIGNIFICANCE AND OBJECTIVES

Switched-mode DC-DC power converters are used for critical power processing in many applications ranging from analog/mixed-signal ICs, microprocessors, SoCs and embedded systems. This project aims to develop techniques and methodologies to analyze and design switched-mode DC-DC converts while addressing key design challenges associated with power efficiency and power integrity.

TECHNICAL APPROACH

The design of DC-DC converters involves examining multiple topological choices and trading off between achievable design specifications, design/control complexity, and cost. Such design analysis is critically dependent on accurate analysis of dynamical operations of the converter and various losses. Simulation of DC-DC converters at the full schematic/extracted layout level is confronted by huge cost due to the design complexity.

We will develop methods for efficient simulation and characterization of switched-mode DC-DC converters. Dedicated envelope-following algorithms will be developed for simulation of DC-DC converters without any significant loss of accuracy. Furthermore, we will develop behavioral models to guide the design process.

SUMMARY OF RESULTS

Our recent effort has been geared towards the development of a robust envelope-following (EF) simulation algorithm and its implementation that can be transparently applied to converters that operate in various modulation modes (e.g. PWM and PFM).

The EF simulation of practical DC-DC converters is challenging due to the presence of digital behavior, strong nonlinearity, and complex frequency modulation schemes and feedback loops (Fig. 1). We propose a novel EF method for time-domain analysis of DC-DC converters based upon a numerically robust time-delayed phase condition to track the envelopes of circuit states under a varying switching frequency. We further develop an EF technique that is applicable to both fixed and varying switching frequency operations, thereby providing a unifying solution to converters with pulse-width modulation (PWM) and/or pulse-frequency modulation (PFM). The robustness and efficiency of the proposed method are demonstrated using several DC-DC converter and oscillator circuits modeled using the industrial standard BSIM4 transistor models. A significant runtime speed-up with respect to the conventional transient analysis is achieved for PFM DC-DC converters with strong nonlinear switching characteristics.

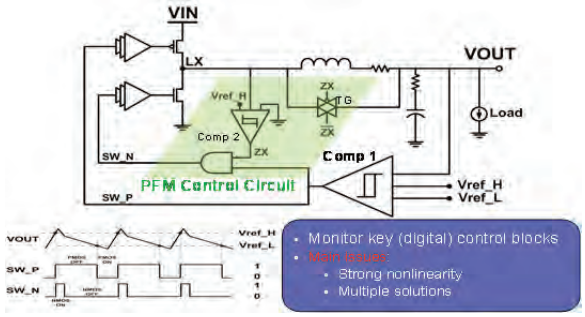


Figure 1: Key envelope-following simulation challenges of PWM/PFM converters.

Fig. 2 shows the application of our EF method to a PFM/hysteretic converter where the proposed method speeds up the simulation by 30X over the standard transient analysis.

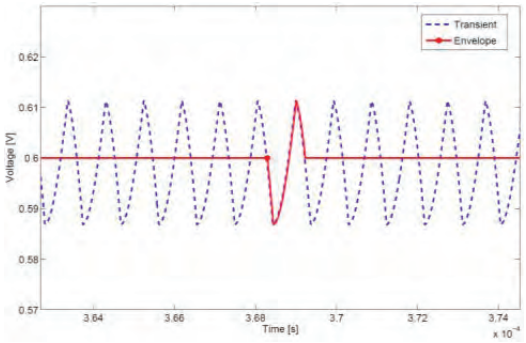


Figure 2: Envelope-following simulation of a PFM/hysteretic converter achieving 30X runtime speedup over the standard transient analysis.

Keywords: switched-mode DC-DC converters, simulation, envelope-following algorithm, behavioral modeling

INDUSTRY INTERACTIONS

Texas Instruments, Freescale

MAJOR PAPERS/PATENTS

[1]Wang, Li and Lai, "A Unifying and Robust Method for Efficient Envelope-Following Simulation of PWM/PFM DC-DC Converters," IEEE/ACM DAC, 2014.

TASK 1836.116: EFFICIENT PA ARCHITECTURES FOR POWERLINE COMMUNICATIONS

RANJIT GHARPUREY, THE UNIVERSITY OF TEXAS AT AUSTIN, RANJITG@MAIL.UTEXAS.EDU

SIGNIFICANCE AND OBJECTIVES

Using power lines for communications is highly attractive for several end applications, since in principle, this communication medium allows for cost-effective reuse of existing infrastructure. This research addresses the design of power efficient transmitters for powerline communication systems that support data rates up to several hundreds of kbps.

TECHNICAL APPROACH

A PWM-based design will be utilized in the transmitter implementation. Transmitter designs in 65nm and 130nm CMOS processes will be investigated. Critical design considerations including efficiency, linearity, and spurious emissions will be addressed. Circuit techniques for ensuring power delivery in the low supply voltage allowed by the CMOS processes will be investigated. Since the switching frequency of the PWM generator can be of the order of several tens of MHz, a PLL-based PWM generator that avoids the requirement for a ramp will be considered for the implementation.

SUMMARY OF RESULTS

The basic architecture of the PLL-based pulse-width modulator is shown in Fig. 1. This architecture has been verified as part of a different project, in an IC implementation [1]. This design provides a peak output power of 1.2 W in a 6.8 Ohm load, with a 4.8 V supply. The design achieves a THD of -65 dB with a switching frequency up to 20 MHz, for input bandwidth up to several tens of kHz. The peak efficiency is measured at 83% for an output power larger than 1W for a switching frequency of 10 MHz.

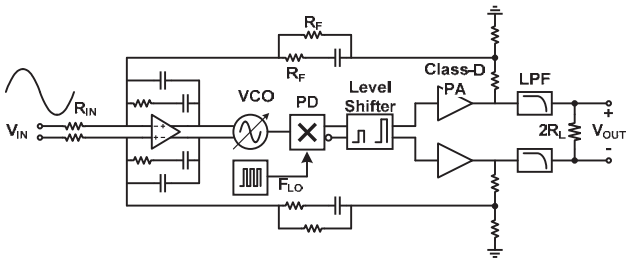


Figure 1: PLL-PWM architecture

We are currently implementing the above design for powerline systems that operate in the range from 40-480 kHz, with signal peak-to-average ratio of 10 dB. The design targets include a 1V-rms signal level into a 2 Ohm load, for a system bandwidth from 40-90 kHz, and 1.6 V-rms signal level into a 10 Ohm load, for a system bandwidth from approximately 150-480 kHz. In both cases, the out-of-band distortion level requirement is less than -60 dBc.

The PLL-PWM approach has been designed in a 130 nm CMOS process for the high-bandwidth system. While the system requires a bandwidth up to 480 kHz, the architecture has been simulated up to 2 MHz.

VCO non-linearity has been determined to be a key contributor to harmonic and intermodulation products in the design. In order to reduce even-order non-linearity, a new VCO topology has been designed. The simulated design operates with a reference frequency of 30 MHz. The output PWM switches at 60 MHz. Spurious content at 60 MHz is attenuated by using an external filter. A simulated spectrum plot for two signal levels, based on transistor level simulations is shown in Fig. 2. As can be observed, the distortion level is less than -60 dBc. The design employs a 2.4 V supply in order to deliver the required power into a 10 Ohm load. A variation of this design based on a step-up transformer, that operates from a 1.2 V supply will also be considered next.

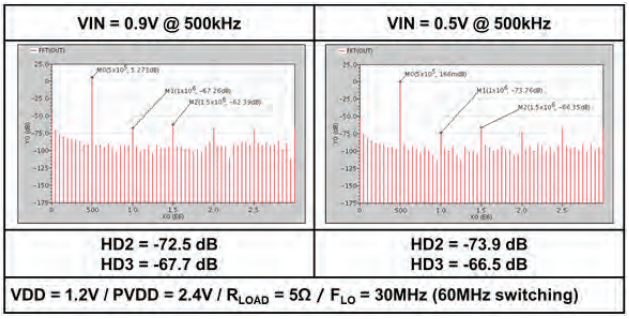


Figure 2: Simulated output spectrum of PWM transmitter

Keywords: PWM, digital powerline transmitters, switching mode PAs. INDUSTRY interactionS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] J. Lu et al., "A CMOS class-D Line Driver Employing a Phase-Locked Loop Based PWM Generator," IEEE Journal of Solid State Circuits, vol. 49, pp. 729–739, March 2014.

TASK 1836.118: LOW NOISE, LOW RIPPLE FULLY INTEGRATED DC-DC CONVERTERS FOR SIGNAL CHAIN APPLICATIONS

BERTAN BAKKALOGLU, ARIZONA STATE UNIVERSITY, BERTAN@ASU.EDU
SAYFE KIAEI, ARIZONA STATE UNIVERSITY, SAYFE@ASU.EDU

SIGNIFICANCE AND OBJECTIVES

Fully integrated isolated DC-DC converters are an essential component in power monitoring, biomedical, and motor control applications where ground isolation is required. Compared to bulky discrete transformers, fully integrated transformer based approaches have advantages over reliability, weight, size and noise performance and are more suitable for high precision mixed signal applications.

TECHNICAL APPROACH

In this project, isolated converters that can be integrated with mixed signal building blocks, such as current monitors, ADCs and telecommunication modules will be developed. This converter utilizes an integrated coreless micro-transformer which is driven resonantly at around 100MHz to achieve efficient energy transfer. A peak power point detection method is developed to ensure the system operates at the optimum frequency while a spread spectrum technique is also utilized to realize EMI noise reduction. Not only the transformer, a full bridge driver, a Schottky diodes rectifier, a voltage regulator and noise sensing cells are also integrated on the same chip. Certain level of isolation is achieved by utilizing a commercially available high voltage silicon process.

SUMMARY OF RESULTS

The fully integrated isolated DC-DC converter architecture is represented in Figure 1. Example input and output voltage are shown with 200V isolation. At the primary side, a transformer is utilized to transfer power source across a ground isolation boundary. At secondary side, in order to make rectifier act fast enough for >100 MHz signal, passive type rectifier should be used. A LDO is also utilized to regulate output to high precision voltage.

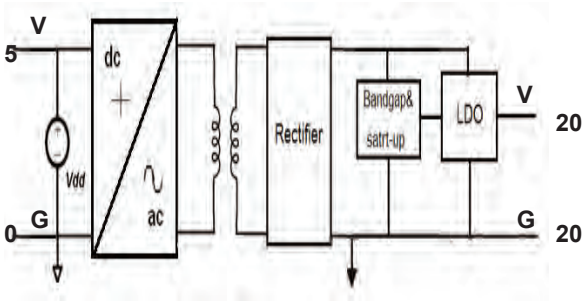


Figure 1a: Power transfer block diagram

Coreless on-chip transformer is key part of our DC-DC converter. It is implemented as planar type spirals as shown in Fig. 1a. It is fabricated in an AMS H18 high voltage process. Isolation between two ground domains is provided by the insulation layers between the primary and secondary coils. SiO_2 naturally acts as an insulation layer between two metal layers and it can provide over 800V/um breakdown strength. Before fabrication, the transformer 3-D model is analyzed in ANSYS HFSS.

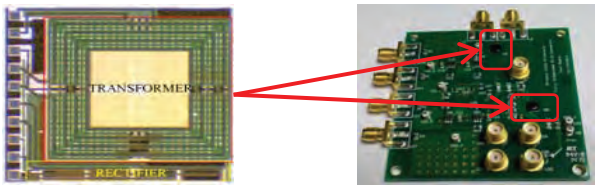


Figure 1b. On-chip transformer die photo and PCB test board

The on-chip transformer is mounted on a PCB board and characterized by a network analyzer. The result shows its inductance is higher than the simulated and the coupling factor is lower than the simulated. These differences are due to the PCB off-chip routings.

This transformer is driven by a full bridge to achieve good voltage swing amplitude. Due to size limitation of the on-chip transformer, two capacitors are added in series with transformer to reduce its resonant frequency to around 100MHz. This structure is different from the previous design which utilizes one capacitor in parallel with a transformer to form a resonant tank. The reason for this change is for better power transfer efficiency. Only current flowing through the transformer primary coil can be transferred to the secondary. A series type resonant tank can force all H-bridge current pass through the inductor, while a parallel type cannot.

In order to make sure the converter works at the optimum frequency, the H-bridge operation frequency will be digitally stepped up by a closed control loop at the start-up of the converter. On the primary side, the envelope power will be measured and logged. At the frequency where the peak power is detected, the H-bridge frequency is locked. After peak power point searching is done, spread spectrum control starts working. By using an off-chip signal to control spread frequency, the EMI noise performance can be optimized.

Keywords: EMI, DC-DC, transformer, isolate

INDUSTRY INTERACTIONS

Texas Instruments

TASK 1836.123: TEST TECHNIQUES AND FAULT MODELING FOR HIGH VOLTAGE DEVICES AND BOARDS

BRUCE KIM, CITY UNIVERSITY OF NEW YORK, BKIM@CCNY.CUNY.EDU

SIGNIFICANCE AND OBJECTIVES

Our project objectives are 1) develop physics-based fault models for LDMOS transistors, 2) develop parasitic device models, 3) modify ATE load boards for high voltage discharge problems, and 4) provide novel low-cost test techniques for high voltage LDMOS devices.

TECHNICAL APPROACH

Lateral DMOS transistors are used in various applications. We have developed equivalent circuit models for LDMOS and structural-defect fault models. Test simulations were performed and a fault dictionary was created. We performed simulations to reduce avalanche breakdown voltages using the fault models. Using pulsed gate terminal stimulus, we evaluated several LDMOS parts. We proved that the simulated results were in good agreement with experimental results with high-voltage apparatus developed in our laboratory. We continued to enhance our HVPro software tool to test DIB automation and reduce high-voltage testing to protect personnel.

SUMMARY OF RESULTS

During the last reporting period, we prototyped a new noise reduction scheme to measure in the nano-amp range. Hardware test measurement apparatus was built to implement the noise reduction scheme [1]. We have developed a low-cost test technique to reduce the avalanche breakdown voltage. We performed extensive simulations based on the parasitic devices using our fault models. We developed a closed form mathematical expression to describe the LDMOS drain current. The expression was simulated on Matlab.

We also developed a new testing scheme to reduce the high-voltage to test LDMOS drivers. The testing scheme involves a pulsed stimulus in the gate terminal to modulate the electric field in the thick oxide layer of LDMOS. This phenomenon provided reduction in high-voltage Avalanche; hence a super high voltage (1,000V) is no longer necessary to test a LDMOS. We have tested several LDMOS parts to prove our concept. Fig. 1 illustrates a LDMOS part which was measured and it shows a reduction in avalanche voltage level. We can summarize that a non-conventional test technique using transmission line pulses at the gate terminal provides a much lower the Avalanche voltage.

After our successful LDMOS measurements, we implemented a BIST circuit to make the entire measurement system on the same LDMOS driver [2].

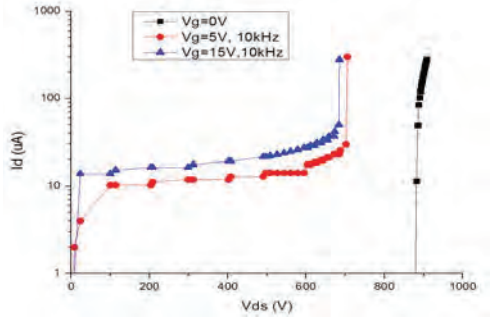


Figure 1: Measurements of LDMOS Drivers with Pulsed Gate Stimulus which Reduced Avalanche Voltage Levels.

This provided us with leakage current measurements due to gate terminal and crystal defects. Fig. 2 illustrates the BIST model.

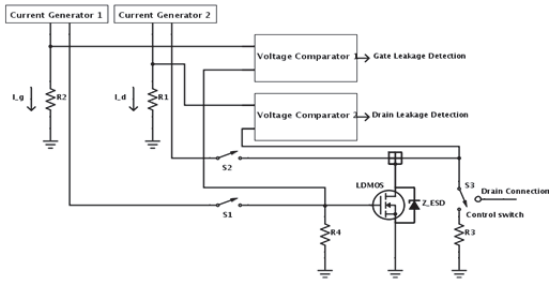


Figure 2: LDMOS Driver BIST Model to Measure Leakage Currents.

Keywords: LDMOS, Structural defects, avalanche voltage, fault model, high voltage

INDUSTRY INTERACTIONS

Texas Instruments Inc., Global Foundries Inc.

MAJOR PAPERS/PATENTS

[1] Patent: US 8,742,777 B2, "Method and System for testing an Electric Circuit," awarded on June 3, 2014.

[2] B. Kim, S. Mondal, F. Taenzler, K. Moushegian, "A Novel BIST Technique for LDMOS Drivers," Invited Paper in BIST Special Session, IEEE 57th Midwest Symposium on Circuits and Systems, College Station, TX, 2014.

[3] S. Kannan, K. Kannan, B. Kim, F. Taenzler, R. Antley, K. Moushegian, K. Butler, D. Mirizzi, "Physics-Based Low-Cost Test Technique for High Voltage LDMOS," Journal of Electronic Testing Theory and Applications, 29:745-762, December 2013.

TASK 1836.124: STUDY AND ANALYSIS OF FAST POWER-ON CLOCK MULTIPLIERS IN THE PRESENCE OF PVT VARIATIONS

PAVAN KUMAR HANUMOLU, UNIVERSITY OF ILLINOIS, HANUMOLU@ILLINOIS.EDU

SIGNIFICANCE AND OBJECTIVES

Inactivity periods in energy proportional wireline or wireless links can be of the order of few milliseconds or higher. Temperature or voltage variations during this idle period could cause frequency drift in an oscillator which cannot not be corrected by the integral path in nanoseconds time frame. Objective is to make oscillators resilient to such errors.

TECHNICAL APPROACH

Proposed research sets out to explore clock multiplying architectures resilient to voltage and temperature variation during off-state. Understanding the effect of temperature and voltage variations in a ring and LC oscillator, and how fast power-on MDLL and PLL architectures react to such variations. Exploring inherent PTAT-NTAT frequency characteristics in a ring oscillator and making it temperature insensitivity. Cancelling temperature sensitivity of a LC oscillator with the help of a temperature sensor and building fast power-on PLL.

SUMMARY OF RESULTS

In a ring oscillator, magnitude and direction of variation depends on the oscillator supply voltage (Fig. 1). At a particular V_{DD} zero-temperature-coefficient of frequency (V_{DD}=850mV in Fig. 1) is achieved. In a LC oscillator, PTAT nature of MOS capacitor and loss component of an inductor results in overall NTAT frequency characteristics. LC has approximate 8x lower temperature sensitivity than ring (Fig. 2). In a MDLL, frequency error causes jitter to accumulate at the end of each reference cycle and results in deterministic jitter at the output. This jitter is a function of frequency error and multiplication factor (Fig 3). PLL is more sensitive to frequency error as compared to MDLL. This is mostly due to PLL's limited bandwidth. Frequency error in a PLL results in a static phase offset at the input of a phase detector. In case of linear PFD, the offset is proportional to the bandwidth and frequency error. Wide up/down correction pulse every reference cycle results in jitter at the PLL output (Fig 4).

Keywords: Fast power-on, multiplying delay locked loop (MDLL),PLL, LC

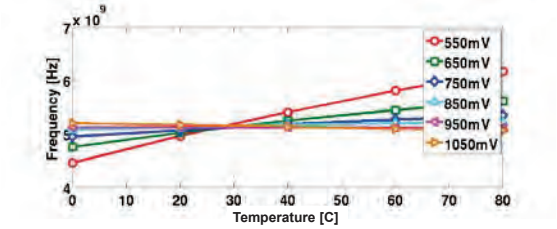


Figure 1: Frequency vs temperature in a ring for various V_{DD}.

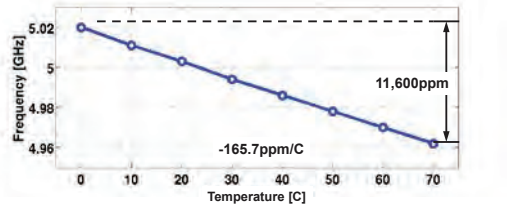


Figure 2: Frequency vs temperature in a LC oscillator.

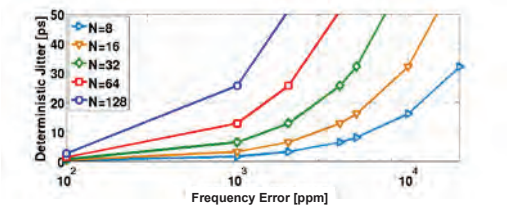


Figure 3: Jitter vs frequency error in a MDLL.

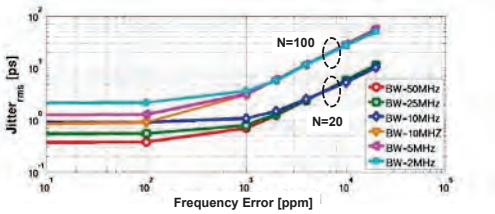


Figure 4: Jitter vs frequency error in a PLL.

INDUSTRY INTERACTIONS

Texas Instruments, Intel, AMD

MAJOR PAPERS/PATENTS

none

TASK 1836.130: BUILT-IN SELF-TEST TECHNIQUES FOR TEST, CALIBRATION, AND TRIMMING OF POWER MANAGEMENT UNITS: PMU-BIST

SULE OZEV, ARIZONA STATE UNIVERSITY, SULE.OZEV@ASU.EDU

SIGNIFICANCE AND OBJECTIVES

State of the art power management units (PMUs) or power management ICs (PMICs) have an increasing number of power domains with multiple embedded bandgap references. Testing, calibration, and trimming of each power management circuit place an undue burden on tester resources. This project aims at developing approaches for built-in self testing, calibration, and trimming of PMU/PMICs.

TECHNICAL APPROACH

Dynamic measurements for PMUs are generally done during characterization but are skipped due to test time and resource constraints where the PMU performance is evaluated as part and calibration of an overall system. Dynamic characterization of PMIC performance is generally required and results in long test times. Detailed characterization and calibration of these dynamic parameters may provide potential performance gains for the overall system, enable faster design, enable the use of less robust designs with smaller slack and margins, and enable easier diagnosis upon systemic parametric fails.

SUMMARY OF RESULTS

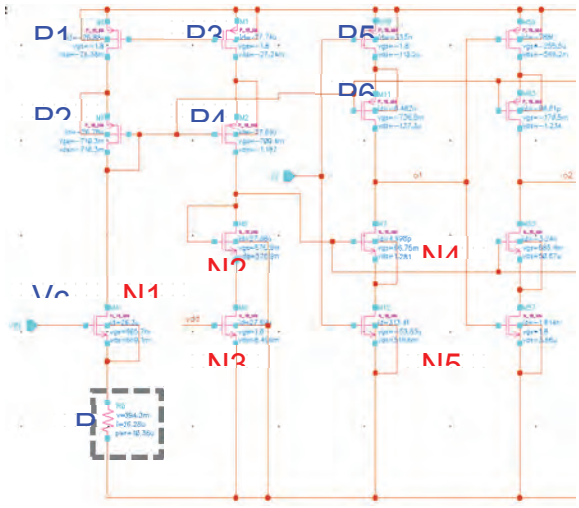


Figure 1: VCO for the BGR voltage measurement

In order to achieve the goals of providing accurate and low-cost testing of PMUs/PMICs, we have developed various approaches. For low-cost on-chip measurement of internal DC voltages, we have developed a VCO-based zoom-in ADC architecture that is comprised of a 7-stage current starved ring oscillator (shown in Fig. 1), and a 15-bit counter. VCOs provide voltage to frequency conversion but are unreliable with respect to process variations and present with drift in their characteristics due to 1/f noise. We have developed an algorithm to use a low-resolution VCO (8-bits) based ADC to be able to measure the bandgap reference voltage with very high resolution (13 bits).

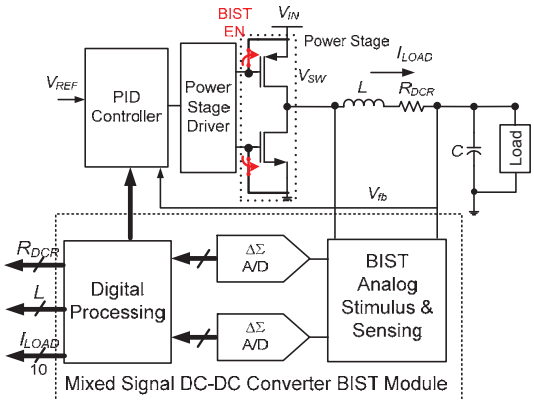


Figure 2: BIST for load current and inductance measurement

We have also designed a built-in-self-test circuitry (Fig. 2) to measure the dynamic load current as well as the inductor characteristics. This circuit provides excellent accuracy in load characterization.

Keywords: PMU/PMIC test, built-in-self-test, load current characterization, VCO-based ADC

INDUSTRY INTERACTIONS

Texas Instruments Inc., Freescale

MAJOR PAPERS/PATENTS

[1] Liu, Tao; Fu, Chao; Ozev, S.; Bakkaloglu, B., "A Built-in Self-Test Technique for Load Inductance and Lossless Current Sensing of DC-DC Converters," VLSI Test Symposium (VTS), pp.1,6, 13-17 April 2014.

TASK 1836.133: ENERGY EFFICIENT SIGNAL PROCESSING TECHNIQUES FOR SMART GRID HETEROGENEOUS COMMUNICATION NETWORKS

NAOFAL AL-DHAHIR, THE UNIVERSITY OF TEXAS AT DALLAS, ALDHAHIR@UTDALLAS.EDU
BRIAN L. EVANS, THE UNIVERSITY OF TEXAS AUSTIN, BEVANS@ECE.UTEXAS.EDU

SIGNIFICANCE AND OBJECTIVES

Within a smart grid (SG), we seek to enable reliable and high-speed communications for better monitoring and control of energy usage. We focus on "last mile" bi-directional communication from a concentrator to smart meters using orthogonal frequency division multiplexing (OFDM) based powerline communications in the 3-500 kHz band and wireless communications in the unlicensed 902-928 MHz band.

TECHNICAL APPROACH

Performance of narrowband PLC is limited by non-Gaussian interference dominated by periodic impulsive noise. We propose a time-frequency modulation diversity scheme at the transmitter and a diversity demodulator at the receiver robust to combat periodic impulsive noise in narrowband PLC, thus enhancing communication reliability without decreasing data rates.

To further enhance SG communications reliability, we propose PLC/wireless receive diversity combining schemes under the impulsive interference variations over the two links. Assuming OFDM transmissions for both links, we analyze the performance gains using simultaneous data transmission and diversity reception over the 3-500 kHz NB-PLC and the unlicensed 902-928 MHz wireless bands.

SUMMARY OF RESULTS

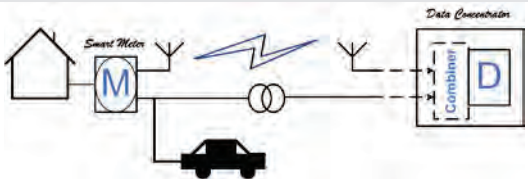


Figure 1.

We investigated the maximal ratio-combining (MRC) scheme for combining the output signals of the NB-PLC and wireless links. The MRC scheme combines the log-likelihood ratios (LLRs) of the received bits over the two links by weighting each link with its SNR. We showed that, due to the impulsive interference on both links, using the instantaneous SNRs of the two links to compute the combining weights provides better bit error rate (BER) than using the average SNRs.

In addition, we proposed a time-frequency modulation diversity technique to improve transmission robustness in periodic impulsive noise without decreasing data rates. The time-frequency modulation diversity transmitter jointly encodes multiple bits to multiple PSK symbols, and allocates them to different subcarriers in various OFDM symbols (Figure 2). It can be embedded into existing narrowband PLC standards.

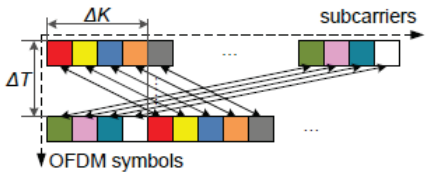


Figure 2: An example of time-frequency modulation diversity. Components of a length-2 modulation diversity code (marked in the same color) are allocated to 2 subcarriers separated in both time and frequency.

On the receiver, we derive a diversity combining demodulator that linearly combines signals received from corresponding sub-channels/OFDM symbols with weights inversely proportional to the sub-channel SNRs. The periodically varying noise power spectrum can be estimated offline based on noise measurements during no-transmission intervals. Alternatively, it can be estimated primarily during data transmission by exploiting its sparsity in frequency domain and applying sparse Bayesian learning algorithms. In simulations, our proposed transceiver methods achieve 100-1000x reduction in coded bit error rates, while maintaining the same data rates, compared to a conventional OFDM narrowband PLC system that uses BPSK, convolutional coding and block interleaving.

Keywords: smart grids, powerline and wireless communication, diversity, periodic impulsive noise.

INDUSTRY INTERACTIONS

Texas Instruments, Freescale Semiconductor

MAJOR PAPERS

[1] M. Sayed and N. Al-Dhahir, "Narrowband-PLC Wireless Diversity for Smart Grid Communications," accepted in IEEE Globecom conference, December, 2014.

[2] J. Lin, T. Pande, I. H. Kim, A. Batra and B. L. Evans, "Time-Frequency Modulation Diversity To Combat Periodic Impulsive Noise In Narrowband Powerline Communications'', submitted to *IEEE Trans. Comm.*

TASK 1836.138: MICRO-POWER ANALOG-TO-DIGITAL CONVERTERS

GABOR C. TEMES, OREGON STATE UNIVERSITY, EMAIL TEMES@IEEE.ORG

SIGNIFICANCE AND OBJECTIVES

In sensor interfaces, medical devices, and RFID systems low power consumption is a critical requirement because power is supplied by a small battery or even obtained by scavenging from the environment. This research focuses on the development of novel analog-to-digital converters (ADCs) for a variety of such applications.

TECHNICAL APPROACH

The incremental data converter (IDC) is a highly efficient micro-power ADC. Its performance may be enhanced by cascading it with one or more additional ADC stages, creating an *extended-counting data converter* (EDC). The focus of our research is on the study, design and implementation of novel micro-power ADCs, particularly IDCs and EDCs, with improved performance. This will result in high efficiency power/performance scalable ADCs, which can be used as high dynamic range analog front ends for sensors, including those used in wearable health monitors.

SUMMARY OF RESULTS

A novel method was developed for extending the order of a conventional IDC from N to ($2N$-1) by using a two-step operation [1]. It only requires the same circuitry as a N^{th}-order IDC. While all following discussions will be specific to N=2, the architecture can easily be generalized to arbitrary values of N. The conversion is performed in two steps: In the first step, the circuit functions as a second-order IDC (IDC2). In the second step, the circuit is reconfigured into a first-order IDC (IDC1). The output bit streams in each step are accumulated and post-processed requiring the same circuitry as an IDC2, and therefore significantly improves the power efficiency.

A two-step IDC (Fig. 1) was fabricated using 2.5V devices in a 65-nm technology (Fig. 2). The measured performance (Fig. 3) showed a 100 dB dynamic range and 91 dB SNDR for a 250 Hz signal bandwidth. The device consumes only 10.7 µW. The ADC achieved a third-order performance by using second-order IDC circuits, and hence it lowers the power consumption significantly. The active area is 0.2 mm^2, which is the smallest among comparable published devices. The results verify that the proposed two-step IDC is a very area- and power-efficient solution for integrated sensor systems. Next year, we shall design a multiplexed system of IDCs, with multi-step operation, to further improve the performance.

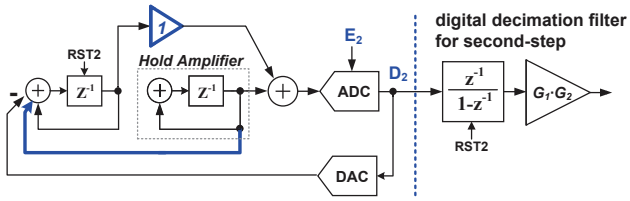


Figure 1: The block diagram of the two-step IADC.

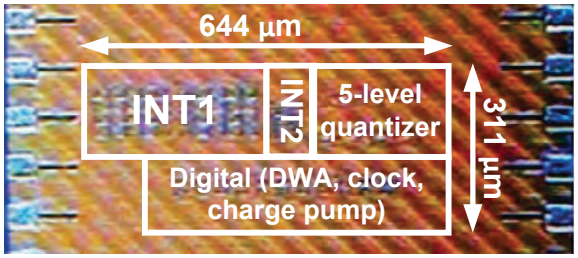


Figure 2: Die photo of the proposed ADC. Active area is 0.2 mm^2.

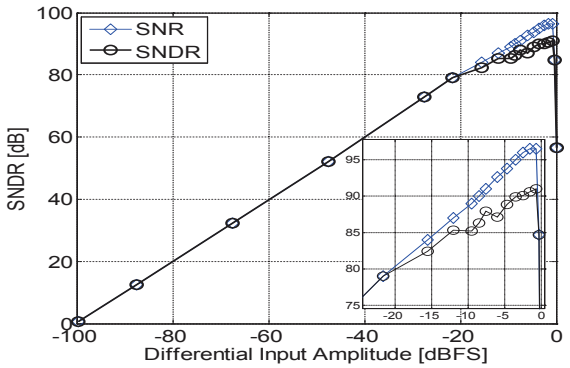


Figure 3: Measured SNDR vs. input signal amplitude.

Keywords: Data converters, ADCs, incremental ADCs, micro-power data converters, multi-step converters, extended-counting ADCs.

INDUSTRY INTERACTIONS

Texas Instruments, Freescale, Intel

MAJOR PAPERS

[1] Chen, C-H, Zhang, Y., He, T., Chiang, P.Y. and Temes, G.C., "A 11µW 250 Hz BW Two-Step Incremental ADC with 100 dB DR and 91 dB SNDR for Integrated Sensor Interfaces," IEEE Custom Integrated Circuits Conf., San Jose, CA, Sept. 15 – 17, 2014.

TASK 1836.139: ENABLING FULLY-INTEGRATED VHF CLK-SYNC MULTIPHASE SWITCHING REGULATORS ON SILICON

DONGSHENG MA, THE UNIVERSITY OF TEXAS AT DALLAS, EMAIL: D.MA@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

With sophisticated architectures, highly advanced task scheduling, and extremely fast and powerful data processing, state-of-art SoCs have imposed stringent requirements on system power delivery and management. As enabling components, voltage regulators in such systems are expected to achieve transient speed and power density two to three orders higher than their siblings in conventional power electronics. In this proposal, the PI plans to investigate three major issues in development of VHF (30-300MHz range) multiphase switching regulators: high speed feedback control, clock synchronization (CLK-Sync) and system miniaturization.

TECHNICAL APPROACH

From the perspective of control scheme, the PI proposes to study a *current-mode zero-delay hysteretic control.* The proposed hysteretic control relies on a single-bound hysteretic reference V_{HYS}, generated by I_L sensing voltage and hysteretic control logic. Compared to its voltage-mode counterparts, this current-mode approach is more robust to the noise at V_{OUT}, as the sensed control vector is I_L, not V_{OUT}. Because it demands no large ESR, noise performance will be highly improved.

From the perspective of system operation and circuit topology, interleaved multiphase topology can be the most effective way to improve both the system response and equivalent I_L slew rate. In this project, by taking advantage of the proposed current-mode zero-delay hysteretic control, a simple CLK-Sync technique is proposed which achieves cycle-by-cycle regulation in each sub-converter.

From the perspective of system implementation, in this project, the PI proposes to achieve monolithic implementation of the regulator, which allows the power flow to follow the desired paths to effectively reduce the parasitics. The PI also plans to explore possible implementation approach of using on-chip magnetic and 3D integration structures.

SUMMARY OF RESULTS

Currently, a commonly used technique for high-speed I_L sensing is to utilize the voltage drop on inductor DCR. As depicted in Fig. 2, by having a matching R_FC_F=L/DCR, the voltage across C_F emulates the V_{DCR}. To achieve sufficient current sense gain (R_I=V_{SENS}/I_L) for system robustness and stability, the DCR value must be large, which adds to conduction loss. Alternatively, an additional amplifier can be implemented, but power dissipation grows as f_{SW} increases.

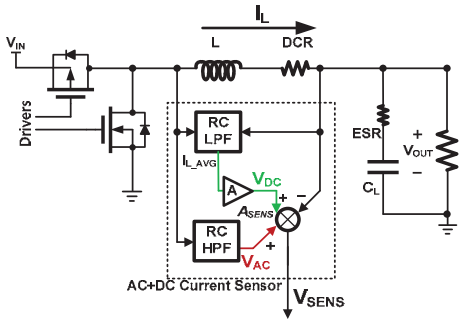


Figure 1: Block diagram of the proposed high-speed AC+DC current sensing circuit.

To overcome the above challenges, the PI proposes an emulated AC+DC current sensing scheme in Fig. 1. The idea is to split I_L into an average (DC) component and AC ripple, amplify each independently, and then recombine the two, as depicted in Fig. 2. The average I_L, I_{L_AVG}, cannot change quickly due to physical I_L slew limit, so the proposed sensor only implements a simple low-power current conveyor circuit to amplify I_{L_AVG}. Meanwhile, the AC ripple, $V_{AC,}$ can be amplified by another passive RC network across L with a smaller time constant to yield an AC gain of A_{SENS_AC}. The idea has been successfully verified in a preliminary simulation in Fig. 2.

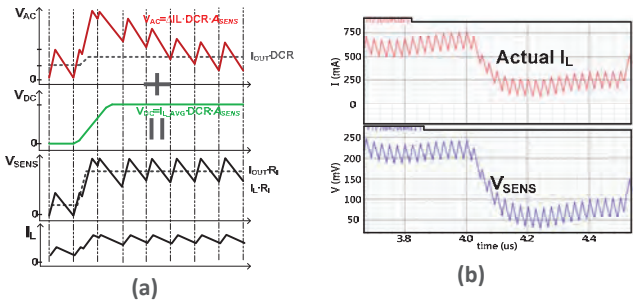


Figure 2: Proposed high-speed AC+DC current sensing circuit: (a) operation scheme, (b) simulation results.

Keywords: VHF switching converters, multi-phase operation, high-speed feedback control

INDUSTRY INTERACTIONS

Texas Instruments Inc.

MAJOR PAPERS/PATENTS

TASK 1836.140: EMBEDDED & ADAPTIVE VOLTAGE REGULATORS WITH PROACTIVE NOISE REDUCTION FOR DIGITAL LOADS UNDER WIDE DYNAMIC RANGE

ARIJIT RAYCHOWDHURY, GEORGIA TECH, ARIJIT.RAYCHOWDHURY@ECE.GATECH.EDU

SIGNIFICANCE AND OBJECTIVES

The primary goal of the project is to develop an integrated power flow architecture for fine-grained spatio-temporal voltage distribution and management in microprocessors and SoCs. We investigate through models, simulations, hardware development and experimentation novel control topologies and circuit techniques for efficient wide-dynamic range linear and switched capacitor voltage regulators (VRs).

TECHNICAL APPROACH

This project investigates power flow architecture in microprocessors and SoCs. This will include development of control models and corresponding circuits for digitally implementable integrated linear regulators for fine-grain power management. These models will be calibrated with Silicon implementation and measurements. In the second part of the project we will develop circuits and models for multiple-output switched capacitor voltage regulators for high efficiency and fine-grained spatial voltage distribution. Further, we will provide models and experimental verification of the interaction of VRs across multiple voltage domains both in terms of stability and cross-domain noise coupling.

SUMMARY OF RESULTS

The key area of the project that has been investigated in the current period has been on the development of models and circuit implementations of integrated linear regulators. We have developed comprehensive control models and circuit implementations for discrete-time digital linear VRs. Linearized models have been developed that illustrate the key design parameters and trade-offs. In particular we have investigated the role of the sampling clock frequency in a digital regulator. While the transient response improves as the sampling frequency is increased, we note an increase in the output ripple of the regulator. This is due to the inherent non-linearity of the loop and the corresponding limit cycle that can exist in the circuit. To comprehend the role of such non-linearity, we have used describing functions to model the steady state behavior of the circuit. We have developed a prototype PCB to understand the steady-state loop dynamics. Further Silicon implementation in IBM 130nm process has been taped out in March 2014, to further validate the models that have been developed. We have further demonstrated the role of adaptive control in providing high power efficiency across a wide operating range.

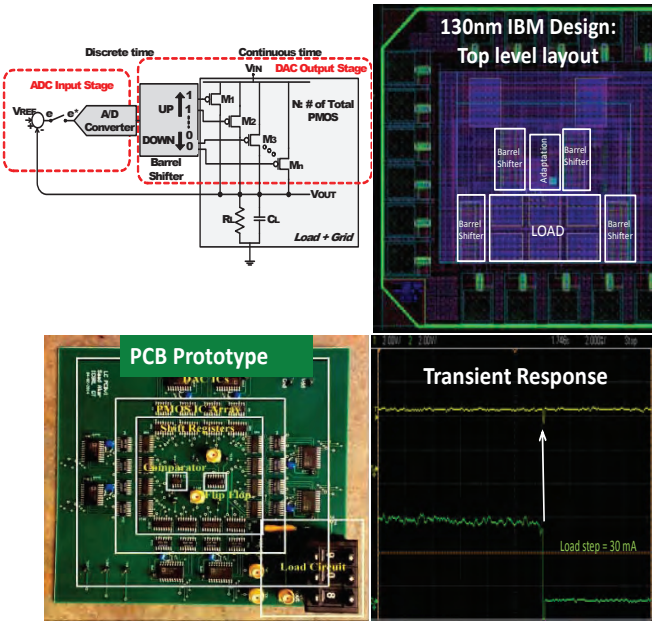


Figure 1: Circuit Implementation of the Discrete Time Linear Regulator along with the layout of a prototype 130nm design and a PCB prototype with measured transient response.

Keywords: Integrated Voltage Regulator, Low-Power Design, Digital Linear Regulators, Discrete Time Control, Continuous Time Control

INDUSTRY INTERACTIONS

M. Khellah, J. Tschanz (Intel),
R. Rao, B. Fleischer (IBM),
M. DiRenzo (TI)

MAJOR PAPERS/PATENTS

[1] Samantak Gangopadhyay, Youngtak Lee, Saad Bin Nasir, Arijit Raychowdhury , "Modeling and Analysis of Digital Linear Dropout Regulators with Adaptive Control for High Efficiency Under Wide Dynamic Range Digital Loads," Design, Automation & Test in Europe (DATE), Dresden Germany, Mar. 2014.

[2] Saad Bin Nasir, YoungTak Lee, Arijit Raychowdhury, "Modeling and Analysis of System Stability in a Distributed Power Delivery Network with Embedded Digital Linear Regulators," International Symposium on Quality Electronic Design (ISQED), San Jose, USA, Mar. 2014.

TASK 1836.142: LOW POWER APPLICATIONS OF FRAM

DAVID BLAAUW, UNIVERSITY OF MICHIGAN, BLAAUW@UMICH.EDU
DENNIS SYLVESTER, UNIVERSITY OF MICHIGAN

SIGNIFICANCE AND OBJECTIVES

Compared to popular non-volatile-memory, flash, FRAM has significantly faster write access time; lower write energy, smaller peak current and orders of magnitude better endurance. On the other hand, Flash has better density than FRAM. To explore FRAM application space, as FRAM is more suitable for write-dominated or balanced read-write applications.

TECHNICAL APPROACH

We evaluate FRAM characteristics against various parameters, and explore FRAM array design-space, specifically targeting low V_{DD}, low power operations. The focus of our research is on ultra-low energy FRAM arrays for millimeter-scale sensor- networks.

Millimeter-scale sensor-networks wake-up for short intervals, store sensor data, and transmit data intermittently, all with a very long battery life, requiring ultra-low energy non-volatile memories. Other applications like implantable medical devices and energy harvesting applications also have similar characteristics.

The objectives are to optimize FRAM for ultra low-power operation by designing peripheral circuits for improved robustness and further optimizing FRAM for sensor node applications.

SUMMARY OF RESULTS

The 1T1C cell in Fig. 1 is used to create an FRAM array model for evaluation. The bit cell has an access transistor in series with a ferroelectric capacitor (FeCap).

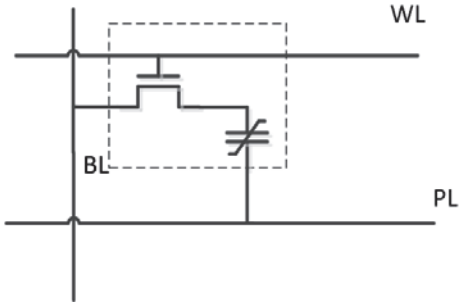


Figure 1: 1T1C FRAM bit cell

To attain ultra low-energy FRAM operation we need to read /write FRAM at low V_{DD} with acceptable margins.

As shown in Fig. 2, by lowering the supply voltage of FRAM the access energy drops significantly. This is because less energy is needed to charge the large parasitic bit line capacitors and ferroelectric capacitors. In Fig.2, the write-back energy is not included in the read.

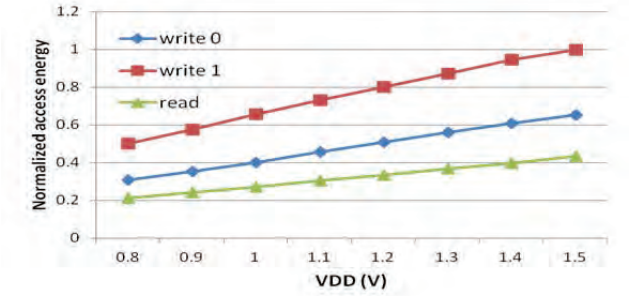


Figure 2: FRAM access energy with different supply voltages

However, low supply voltage will have trade-offs, such as long access time and reduced read margins, as shown in Fig. 3. The margins reduce as the hysteresis loop shrinks with lower voltage across the ferroelectric capacitor.

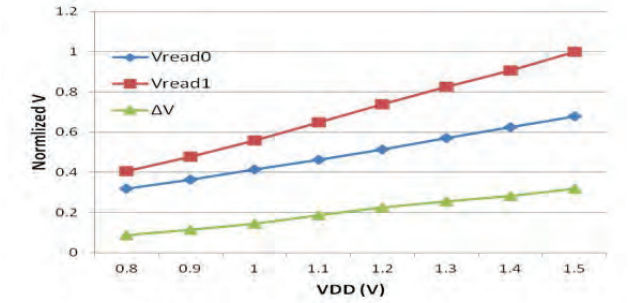


Figure 3: Read Margin 'ΔV' vs supply voltage

Both read speed and low read margin requires better sense amplifier circuit. Overdriving the WL voltage also helps improving the read margin.

Although, FRAM has many advantages compared to other memories, it also has some additional stability issues like thermal depolarization and imprint. There is a polarization reduction for FeCaps at high temperatures.

Variation studies are also performed with different process corners for FeCaps and transistors.

We will further build upon the FRAM array and peripherals for designing specific ultra low-power circuits to work reliably at low voltages.

Keywords: NVM, FRAM, low-power, reliability, sensor-networks

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

TASK 1836.143: DESIGN TECHNIQUES FOR MODULATION-AGILE AND ENERGY-EFFICIENT 60+GB/S RECEIVER FRONT-ENDS

SAMUEL PALERMO, TEXAS A&M UNIVERSITY, SPALERMO@ECE.TAMU.EDU

SIGNIFICANCE AND OBJECTIVES

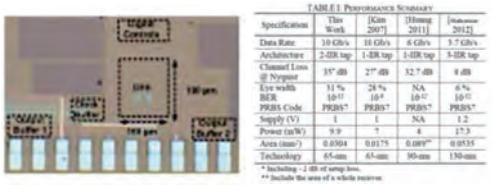
While high-performance I/O circuitry can leverage CMOS technology improvements, unfortunately the bandwidth of the electrical channels used for inter-chip communication has not scaled in the same manner. The high-speed serial link receiver design and modeling techniques proposed here aim to significantly improve interconnect bandwidth density in an energy-efficient manner.

TECHNICAL APPROACH

In order to investigate design trade-offs, a statistical-modeling framework will be utilized to investigate power-optimum equalization partitioning and modulation format for 60+Gb/s signaling environments. This tool will be used to guide the design of a new modulation-agile receiver front-end which includes a multi-level decision-feedback equalizer (DFE) with multiple IIR feedback taps for efficient long-tail ISI cancellation. Adaptive techniques will also be developed to tune key equalization parameters, such as DFE tap time constants/weights and CTLE settings.

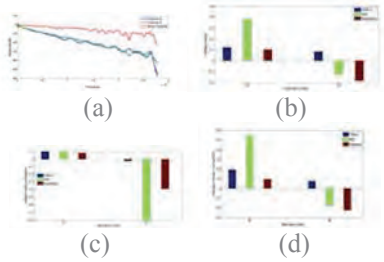
SUMMARY OF RESULTS

While receivers with DFEs are now in wide use, architectures which employ a common FIR feedback filter require an ever-growing number of taps to cancel the long-tail ISI found in typical backplane channels. In order to address this, DFEs with IIR feedback filters have been implemented and shown to improve equalization efficiency for RC-limited and backplane channels. A key challenge associated with these architectures involves optimizing the critical IIR feedback path to allow for ISI cancellation beginning at the first post-cursor. Also, while the use of multiple IIR taps can provide for further ISI cancellation, the IIR tap number should be carefully chosen in order to avoid excessive area and power consumption. This project addressed these issues by implementing a DFE which employs 2 IIR taps to allow for improved long-tail ISI cancellation [1]. Fabricated in GP 65-nm CMOS (Fig. 1), the receiver occupies 0.0304 mm^2 area and consumes 9.9 mW while operating at a BER<10^{-12} for 10 Gb/s data passed over a 40-inch FR4 channel with 35 dB loss at 5 GHz.



(a) (b)

Figure 1: 10Gb/s DFE with 2 IIR taps: (a) GP 65nm CMOS prototype (b) performance summary.



(a) (b) (c) (d)

Figure 2: Statistical modeling of 50 and 64Gb/s systems: (a) Channel models with differing loss profiles. Normalized voltage margin for (b) Channel A, (c) Channel B, and (d) Channel C.

Under this low BER requirements, transient simulations are impractical. In order to investigate this, this project continues to build upon the PI's statistical-modeling framework for high-speed serial links. This tool is utilized to investigate the optimal equalization partitioning and modulation format for 60+Gb/s signaling environments, relevant for applications such as 400Gb Ethernet. As shown in the 50 and 64Gb/s modeling results of Fig. 2, the optimal modulation format is a function of the channel loss profile.

Utilizing more spectrally-efficient modulation that allows for longer unit interval times can relax timing, while also being potentially better suited for a specific channel loss profile, provided that DFE architectures are developed that are agile enough to support multiple modulation formats. To address this, a new high-speed modulation-agile receiver front-end which includes a multi-level decision-feedback equalizer with multiple IIR feedback taps for efficient long-tail ISI cancellation was developed and taped-out in GP 65nm CMOS.

Keywords: decision feedback equalizer, infinite impulse response (IIR) DFE, receiver, serial link

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] O. Elhadidy et al., "A 10 Gb/s 2-IIR-Tap DFE Receiver with 35 dB Loss Compensation in 65-nm CMOS," IEEE VLSI Symposium, June 2013.

TASK 1836.144: HIGH-EFFICIENCY HIGH-VOLTAGE POWER CONVERTERS

HOI LEE, THE UNIVERSITY OF TEXAS AT DALLAS, HOILEE@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

This research aims to investigate novel soft-switching techniques, synchronous gate driving techniques, and control schemes to significantly advance power efficiency and power density of today's high-voltage DC-DC converters. These developed converter technologies help greatly lower the cost and the energy efficiency of renewable energy systems, telecom systems, automotive systems, etc.

TECHNICAL APPROACH

A quasi-square-wave (QSW) zero-voltage-switching (ZVS) non-isolated boost converter using enhancement-mode GaN (eGaN) FETs is reported. The converter topology requires a small number of passive components, minimizes the converter switching loss under high-voltage high-frequency operations, and offers low-voltage stress across power transistors. A transformer-based floating gate driver with 30 ns propagation delay is developed to enable high-speed high-side gate driving of the eGaN power FET and thus high-frequency operation of the proposed ZVS converter. A 130-W output power prototype circuit of the proposed boost converter with 1-MHz switching frequency has been implemented and the peak power efficiency of 95% has been measured.

SUMMARY OF RESULTS

The structure of the proposed PWM ZVS boost converter with synchronous gate driving is illustrated in Fig. 1(a). In contrast to the generic asynchronous boost converter with a single main power switch (M_{low}), a diode (D_{main}) and an inductor (L_{main}), a high-side power switch (M_{high}), a reset capacitor (C_{rst}) and a small inductor (L_{rst}) are added in the proposed converter. Three added components are used to create current to charge or discharge the parasitic capacitance at the switching node V_{sw} for realizing ZVS during switching transitions. When ZVS is

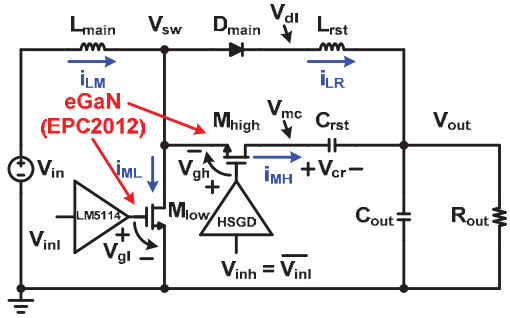


Figure 1: Structure of the proposed quasi-square-wave ZVS boost converter with synchronous gate driving.

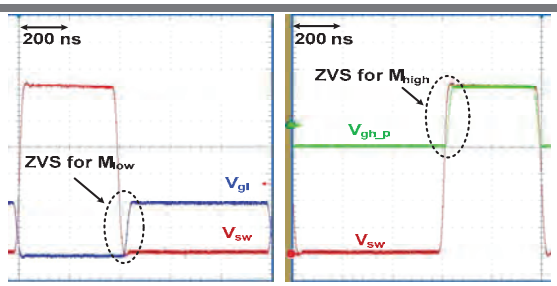


Figure 2: Measured voltage waveforms proving ZVS of (a) M_{low} and (b) M_{high}.

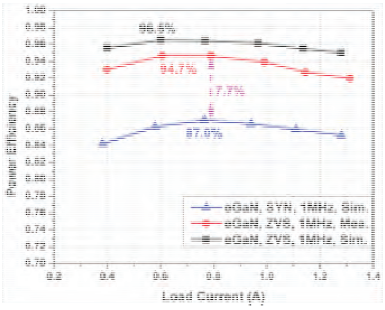


Figure 3: Power efficiency of different boost converters.

achieved for turning on both M_{low} and M_{high}, the converter switching loss at node V_{sw} can be minimized, thus greatly increasing the power efficiency of the converter under high-voltage high-frequency operation.

In Fig. 2, signal V_{gl} becomes high to turn on M_{low} after V_{sw} becomes 0. Also, V_{gh_p} starts to increase to turn on M_{high} after V_{sw} is fully charged to 120V. Hence, ZVS of M_{high} and M_{low} are established at 1MHz.

Fig. 3 shows that the peak power efficiency of the proposed ZVS boost converter is 95%. Compared with the simulated power efficiencies of the synchronous boost converter using the same eGaN switches and gate drivers, the measured power efficiencies of the proposed ZVS boost converter are increased by as much as 7.7% at 80W and 6.8% at 130W output power, saving 6.1W and 8.8W power, respectively.

Keywords: High-voltage DC-DC converters, non-isolated boost converters, zero-voltage switching.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] J. Xue, L. Cong, and H. Lee, "A 130W 95%-Efficiency 1MHz Non-Isolated Boost Converter Using PWM Zero-Voltage Switching and Enhancement-Mode GaN FETs," *IEEE APEC*, Fort Worth, TX, USA, Mar. 2014.

TASK 1836.146: ON-CHIP AC-DC POWER CONVERSION WITH GROUND DISTURBANCE SHIELDING FOR ENVIRONMENTAL SENSING APPLICATIONS

DONGSHENG MA, THE UNIVERSITY OF TEXAS AT DALLAS, EMAIL: D.MA@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

The primary goal of this project is to explore the optimal circuit architecture and operation schemes in achieving highly efficient and robust AC-to-DC power transmission. In addition, three technical performance parameters are of great importance: efficiency, robustness and form factor. High power efficiency is not only the key to operation time and energy saving, but also a dominant factor through temperature/thermal effect on semiconductor devices and circuits. Meanwhile, for sensing applications, form factor is usually critical. Monolithic implementation is thus highly desirable. This, in return, will also benefit the system reliability and power conversion efficiency. Together with the proposed ground disturbance shielding circuit architecture and operation scheme, they could substantially enhance the robustness of the system.

TECHNICAL APPROACH

With ground disturbance shielding based architecture, the AC-DC power transmission and conversion can be accomplished wirelessly. With wireless power, efficiency is the more significant parameter. A large part of the energy sent out by the transmitter must arrive at the receiver or receivers to make the system economical. The difficulty in achieving high efficiency holds valid for both inductive and capacitive coupling. This project employs capacitive coupling approach to achieve the power transmission and conversion. The capacitors are fully integrated on-chip to ensure better performance and a smaller form factor.

In addition to power transmission, the AC-DC conversion circuit should also provide well regulated DC operation voltage as a power supply to load application. The two functions (power transmission and regulation) can be achieved inherently through one single circuit – a switched capacitor power converter. In order to achieve high efficiency in charge pump based power system, the development involves an in-depth and thorough investigation on the various power loss mechanisms in the power stage – charge pump.

Lastly, system miniaturization of switching regulators has been a long-term challenge. In this task, significant effort will be on the optimization of efficiency, switching frequency, power and capacitor size to allow a feasible and efficient monolithic implementation.

SUMMARY OF RESULTS

We propose an N-stage interleaving switched-capacitor power converter as the core of the AC-DC conversion system, as illustrated in Fig. 1.

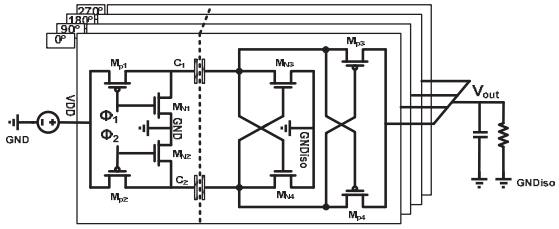


Figure 1: Block diagram of the N-Stage interleaving SC converter.

The proposed N-stage Interleaving topology can reduce the output voltage ripple by N times with the same power transfer capacitance. In this way, we can reduce the output capacitance, enhancing the transient response. In addition, large power transfer capacitance can have a more efficient power transfer but reduce the CMTI (Couple more voltage to the controller side). The interleaving topology can be explored to break this trade-off.

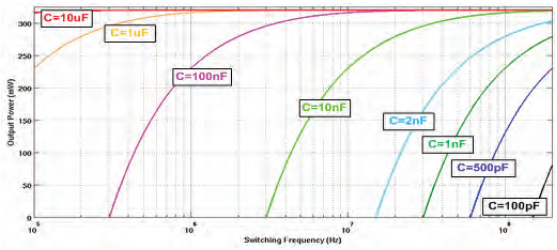


Figure 2: Proposed high-speed AC+DC current sensing circuit: (a) operation scheme, (b) simulation results.

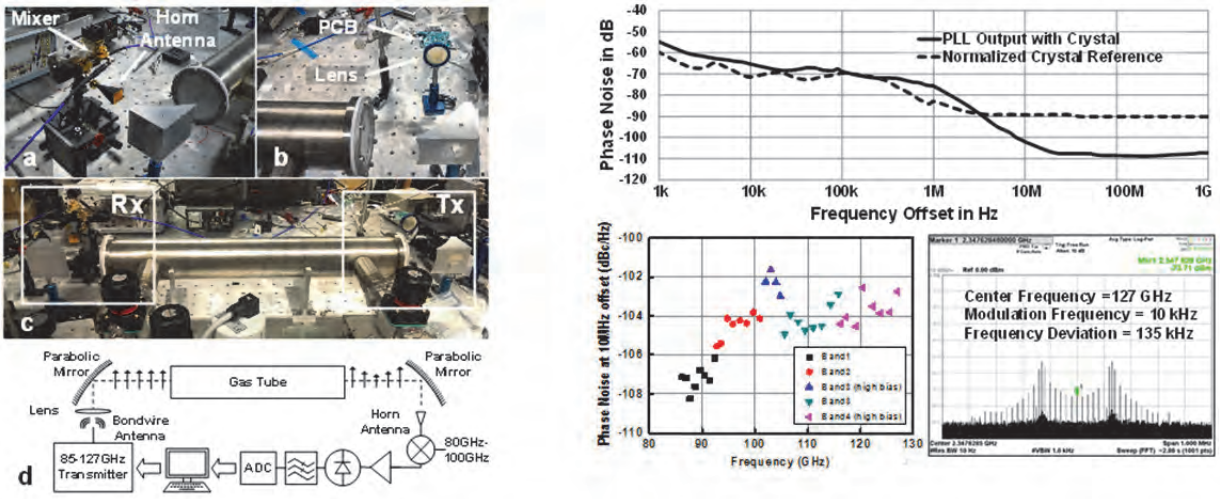
Keywords: Ground noise shielding, AC-DC conversion, Interleaving topology, power transfer efficiency

INDUSTRY INTERACTIONS

Texas Instruments Inc.

MAJOR PAPERS/PATENTS

Safety and Security Thrust



Depiction of 127GHz gas spectrometer realized with CMOS transmitter.

Category	Accomplishment
Security and Safety	A 240-GHz transceiver chipset was demonstrated using a 65-nm CMOS technology, including a passive mixer-first direct-conversion receiver and a frequency-tripled transmitter employing QPSK modulation. The chipset has been used to demonstrate a 16Gbps link and is the first such link demonstrated in CMOS with carrier frequency exceeding 200 GHz. (1836.082, PI: E. Alon, A. Niknejad, UC Berkeley) Publications: S. Kang, et al., "A 240GHz Wideband QPSK Transmitter in 65nm CMOS," RFIC 2014; and S. Thyagarajan, et al., "A 240 GHz Wideband QPSK Receiver in 65 nm CMOS," RFIC 2014.
Security and Safety	Low-cost millimeter and sub-millimeter wave spectrometers could provide critical capabilities for breath analysis and detection of harmful molecules. In this task, a transmitter for rotational spectroscopy has been demonstrated in CMOS. The circuit operates between 85-127 GHz and provides the frequency resolution and settling time necessary for spectrometers. This transmitter has been used together with a bond-wire antenna within a gas spectrometer for detection of acrylonitrile. (1836.119 PI: K.K. O, UT Dallas; and 1836.126, PI: F. DeLucia, Ohio State Univ.) Publication: N. Sharma et. al," 85-to-127 GHz CMOS TX for Rotational Spectroscopy," to appear at 2014 IEEE CICC.
Security and Safety	Low complexity high-speed waveform acquisition is an important component for built-in test. Incoherent undersampling has been used for signal acquisition, and has been demonstrated for both high-frequency linearity characterization in RF transmitters as well as jitter characterization in high-speed I/O systems. (1836.072, PI: A. Chatterjee, Georgia Tech) Publication: D. Bhatta, et. al. "Low Cost Signal Reconstruction Based Testing of RF Components Using Incoherent Undersampling," Journal of Electronic Testing, April 2014, pp 213-228

TASK 1836.067: CHARACTERIZATION OF CMOS BASIC BUILDING BLOCKS FOR SUB-THZ WIDEBAND TRANSMITTERS

MONA HELLA, RENSSELAER POLYTECHNIC INSTITUTE, HELLAM@RPI.EDU
MICHAEL SHUR, SHURM@RPI.EDU

SIGNIFICANCE AND OBJECTIVES

Due to the low f_{max} of 65nm CMOS technology, it is extremely challenging to achieve high output power using fundamental frequency generation or amplification. The primary focus of this work is to generate high power at lower frequency using power amplifiers and use power combiners and frequency multipliers to generate the required power at mm-wave and sub-THz frequencies (180-240GHz).

TECHNICAL APPROACH

The transmitter chip photograph is shown in Fig.1. The transmitter is designed to deliver 5dBm of P_{sat} at 200GHz. A pre-amplifier is realized by adding a four-stage pre-amplifier to the core power amplifier to increase the total gain of the transmitter. The pre-amplifier is designed using a single-ended common-source amplifier topology with shunt-stub microstrip transmission lines for inter-stage matching and delivers 5dBm to the power splitter. A novel power-splitter achieves single-ended to two way differential power division. The power splitter is designed using a coupled line model and achieves 50% smaller area compared to prior art. The core amplifier is designed as a cascaded four stages fully differential common-source amplifier using transformer matching. The core amplifier delivers 16dBm output power at 100GHz to a passive frequency doubler. The frequency doubler, implemented using MOS varactors, has a conversion loss of 10.5dB and delivers 5dBm output power at 200GHz to a 50 Ohms load.

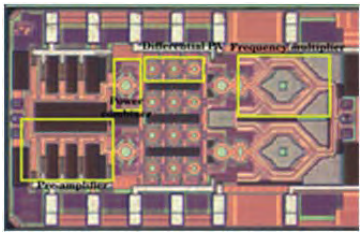


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Figure 1: Schematic of 200GHz transmitter with power budget.

SUMMARY OF RESULTS

The PA and the transmitter are designed in ST 65nm CMOS technology. The differential PA delivers P_{sat} =11.7dBm at 110GHz with a small signal gain of 13dB according to measurement results. This is the highest reported power from a PA without power combining at mm-wave frequencies.

The measurement results of the mm-wave transmitter, are shown in Fig. 2. The TX is centered at 216GHz with a P_{sat} =-4dBm. A 9dB of loss in output power compared to simulations is due to the decoupling circuit of the pre-amplifier. An alternate decoupling circuit has been designed and the transmitter is expected to deliver 5dBm of power with the modified pre-amplification stage.

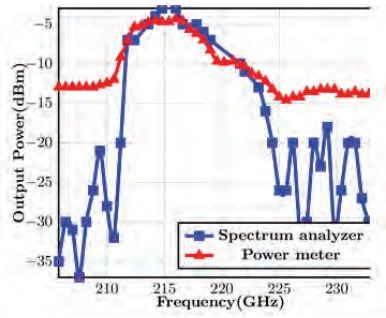


Figure 2: Measured output power of the transmitter.

Table 1: PA Measurement Results

Frequency (GHz)	Bandwidth (%)	Output Power (dBm)	DC Power (W)	Tech.
110	10	11.7	0.16	65nm CMOS

Table 2: TX Measurement Results

Frequency (GHz)	Bandwidth (%)	Output Power (dBm)	DC Power (W)	Tech.
216	2.3	-4(5*)	0.5	65nm CMOS

*Updated results based on the modified decoupling circuit.

Keywords: THz, Power Amplifier, Power Combiner,

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] Sriram Muralidharan, Kefei Wu, Mona Hella., “Compact, Low-loss, Symmetric mm-wave and sub-THz PowerCombiner/Divider,” US Provisional Patent Application No. 61/781,284.

TASK 1836.072: LOW COST TEST OF HIGH SPEED SYSTEMS

ABHIJIT CHATTERJEE, GEORGIA INSTITUTE OF TECHNOLOGY,
ABHIJIT.CHATTERJEE@ECE.GATECH.EDU

SIGNIFICANCE AND OBJECTIVES

The objective of this research is to develop low-complexity high-speed waveform acquisition test hardware and signal processing techniques. The focus application is the test and characterization of communication systems at speeds 10Gbps and higher.

TECHNICAL APPROACH

In this task, the cost of high-speed test instrumentation is reduced by using incoherent undersampling along with complementary back-end signal processing algorithms. Incoherent sampling techniques do not require complicated clock synchronization circuits and hence, lead to reductions in the cost and complexity of high-speed test instrumentation. While direct undersampling based systems are limited in bandwidth by the track-and-hold amplifier bandwidth, techniques such as bandwidth interleaving are used to break the bandwidth bottleneck using broad-band mixers to down convert signal components beyond the track-and-hold bandwidth to a lower frequency band where they can be sampled by the track-and-hold amplifier.

SUMMARY OF RESULTS

Low-cost frequency scalable solutions for high-frequency test signal waveform acquisitionhave been demonstrated that are robust to variations in signal phase and do not require precise phase synchronization at high frequencies. It is possible to reconstruct, with high accuracy, complex periodic signal waveforms ranging from multi-tone signals to pseudo random bit sequences (PRBSs). In Fig 1 the basic idea of the trigger free waveform acquisition setup is shown. Using the proposed techniques, waveform reconstruction is performed using time-domain analysis methods that give O(log(N)) improvement per iteration over Fourier-domain reconstruction (N= no of samples). It was also possible to reconstruct radio-frequency multi-tone signal wave-forms leading to the development of a novel synchronization-free test architecture for linearity testing of high-frequency RF transmitter components with inherent separation of amplitude-amplitude and amplitude-phase non-linearity effects. Also using the proposed techniques, jitter measurement and separation of random, periodic and crosstalk components were demonstrated.

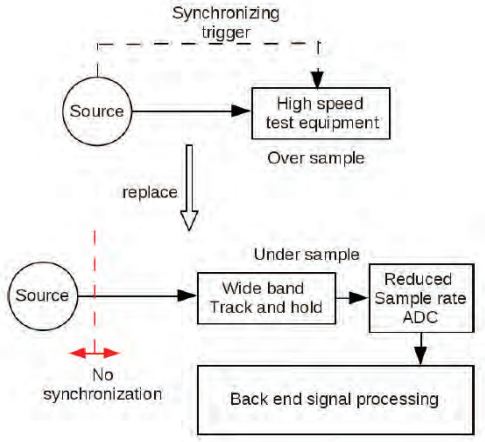


Figure 1: The principle of low-cost trigger-free waveform acquisition. The lack of synchronization between the source and the test equipment provides robustness to phase-delay variations in signal paths.

Keywords: High-speed test, waveform acquisition, under-sampling, bandwidth interleaving, trigger-free waveform acquisition

INDUSTRY INTERACTIONS

Suriyaprakash Natarajan: Intel, Ganesh Srinivasan : Texas Instruments

MAJOR PAPERS/PATENTS

[1] D. Bhatta, et. al. “Low Cost Signal Reconstruction Based Testing of RF Components Using Incoherent Undersampling,” Journal of Electronic Testing April 2014, Volume 30, Issue 2, pp 213-228

[2] D. Bhatta et al., “Time Domain Reconstruction of Incoherently Undersampled Periodic Waveforms Using Bandwidth Interleaving,” Test Symposium (ATS), 2013 22nd Asian, 283-288

TASK 1836.074: SUB-45NM CIRCUIT DESIGN FOR TRUE RANDOM NUMBER GENERATION AND CHIP IDENTIFICATION

WAYNE BURLESON, UNIVERSITY OF MASSACHUSETTS, BURLSESON@ECS.UMASS.EDU
CHRISTOF PAAR, UNIVERSITY OF MASSACHUSETTS / U. BOCHUM, GERMANY

SIGNIFICANCE AND OBJECTIVES

Variations in fabrication process and operating conditions affect the reliability and performance of modern digital circuits. True Random Number Generators (TRNGs) and Physically Unclonable Functions (PUFs) are important cryptographic primitives sensing variability as randomness and secret. This project explores the modeling, analysis and variability aware design of TRNGs and PUFs.

TECHNICAL APPROACH

The project explores the effect of variation in fabrication process and operating conditions on metastability based TRNG and delay based arbiter PUF circuits. The variations in transistor parameters lead to bias in TRNG output. We design and implement novel TRNG circuits based on metastability resolution time that are tolerant to process variation and minimize overhead in performance/power. We also implement on-chip statistical tests to monitor the quality of random bits generated. The arbiter PUF circuits are simulated and taped out in 32nm CMOS with special design to near threshold operations. Simulation methodologies and post-silicon validation platform have been proposed to evaluate PUF metrics. Also, a machine learning attack tolerant design based on non-linear elements has been designed, simulated and fabricated using 32nm IBM SOI.

SUMMARY OF RESULTS

Process variation and sensitivity to noise are the two major challenges in designing TRNG circuits. On the contrary, PUF circuits thrive on large process variations, but are unreliable under variations in voltage and temperature. In this work, we design and implement novel TRNG and PUF circuits that are reliable as well as tolerant to malicious attacks.

Conventional metastability based TRNGs provide excellent performance and energy efficiency. However, increasing intra-die variations affect the reliability of these circuits. We design a novel technique for random bit generation using metastability resolution time, instead of the conventional metastability resolution state (Fig. 1). The circuit is implemented in IBM 32nm SOI CMOS technology and consumes a Si area of 158µm^2. The bit rate at nominal supply voltage of 0.8V is 1.25Gbps at 0.1pJ/bit. Further, a fully re-configurable 1053µm^2 on-chip health check is designed using a reduced set of NIST statistical tests to provide continuous online monitoring of the TRNG output.

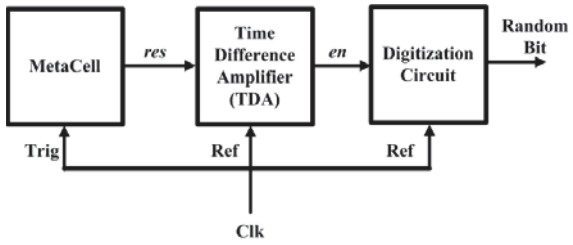


Figure 1: Architecture of PVT-Variation tolerant TRNG based on Metastability Resolution Time

Most of the existing PUF architectures are highly vulnerable to modeling attacks. With as few as 5000 challenge-response pairs, it is possible to construct a computer algorithm that can mimic the PUF. To address this issue, we have developed a non-linear current mirror based PUF, that is analogous to an arbiter PUF in terms of operation. The PUF is based on current shifts that are highly dependent on the input current itself, which makes the parametric modeling extremely difficult. The proposed PUF exhibits a very high modeling attack resistance almost 50x than an arbiter PUF and around 30x when compared to a XOR arbiter PUF. Also, the proposed PUF occupies almost 20% lower area than an equivalent arbiter PUF (64 stage PUF).

Keywords: PUF, TRNG, modeling attacks, process variations, statistical analysis

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] V. Suresh and W. Burleson, "On-chip Lightweight Implementation of Reduced NIST Randomness Test Suite," IEEE HOST 2013.

[2] X. Xu, et.al, "Post-Silicon Validation and Calibration of Hardware Security Primitives," IEEE ISVLSI 201

[3] R. Kumar and W. Burleson, "On Design of a Highly Secure PUF based on Non-linear Current Mirrors," IEEE HOST 2014.

[4] V. Suresh and W. Burleson, "Generate Random Numbers Using Metastability Resolution Time," Application No. US 139,020, Filed 12/2013.

TASK 1836.079: CMOS THZ DETECTION

MONA HELLA, RENSSELAER POLYTECHNIC INSTITUTE, HELLAM@RPI.EDU
MICHAEL SHUR, SHURM@RPI.EDU

SIGNIFICANCE AND OBJECTIVES

This task investigates single FET plasmonic devices as detector/mixer and different antenna, amplifier structures to be used in THz receivers. The main focus is to achieve bandwidth enhanced designs to support very high bit rate data communications with THz carrier frequency.

TECHNICAL APPROACH

We have designed antenna structures with different bandwidth extension techniques such as parasitic half wave, parasitic quarter wave and E shaped patch. The half and quarter wave patch antennas have a parasitic patch in the nearest metal level to the actual one to introduce a second nearby resonant frequency and thus increasing the bandwidth. E shaped patch antenna introduces slots in the conventional patch antenna to introduce multiple resonant points. The considered structures are shown in Fig. 1 along with their die micrographs.

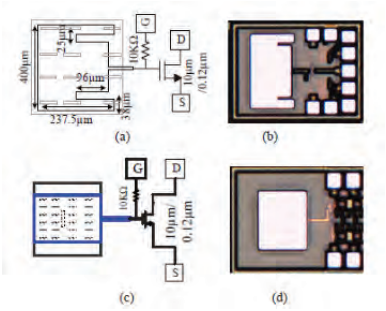


Figure 1: THz detector with E shaped antenna (a) circuit schematic (b) die photograph; THz detector with parasitic half wave patch (c) circuit schematic (d) die photograph.

We have also interfaced the above antennas with a THz detector followed by a wide bandwidth amplifier for communication applications. For the amplifier design, we have followed active feedback topology with inductive peaking to achieve ~15 GHz bandwidth with 28 dB gain (with buffer). The amplifier performance is limited by the input pole of the first stage interfacing with the detector since the detector acts as a very high resistance at the bias point of maximum responsivity.

SUMMARY OF RESULTS

Devices have been fabricated in IBM 130nm CMOS technology. A wide band THz receiver operating from 295 to 312 GHz has been measured in both frequency and time domains. The measured responsivity of 773 V/W and NEP of 66 pW/√Hz at a gate bias of 0.3 V (Fig. 2) for the E-patch antenna coupled device is comparable to recently published results on CMOS THz detectors, while providing 3x higher bandwidth. The receiver has also been characterized for time domain response and can detect THz radiation at 100 ps time resolution. The designed 300GHz receiver has comparable gain and noise performance to published results while having almost ¼ of the area and DC power consumption (Table 1).

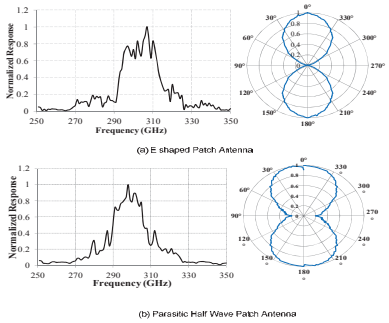


Figure 2: Measured frequency response and polarization of (a) E shaped patch (b) Parasitic 1/2 wave antenna.

Table 1: Comparison with Published Results

Parameter	VLSI'12	RFIC'14	MTT'12	This Work	This Work
Technology	65 nm CMOS	65nm CMOS	130nm SiGe	130 nm CMOS	130 nm CMOS
Frequency (GHz)	260	240	220	300	300
BW(GHz)	NA	7	18	10	5
Gain (dB)	17	16	25	9	23
SNR (dB)	NA	25	NA	30	30
Pdc (mW)	485	260	216	45.5	46
Area (mm^2)	3	2	0.66	0.5	0.5

Keywords: THz detection, Parasitic Patch Antenna, Active Feedback, E shaped Patch.

INDUSTRY INTERACTIONS

Texas Instruments, Intel, IBM

MAJOR PAPERS/PATENTS

[1] Gutin, A.; Nahar, S.; Hella, M.; Shur, M., "Modeling Terahertz Plasmonic Si FETs With SPICE," Terahertz Science and Technology, IEEE Trans. ON , vol. 3, no. 5, pp. 545–549, 2013.

[2] S. Nahar and M. M. Hella, "E-Shaped Patch Antenna Coupled Plasmonic FET for Broadband THz Detection in 130nm CMOS Technology," IRMMW-THz, 2014.

[3] M. Shafee, S. Nahar, and Mona M. Hella, "Stacked Resonator Patch Antenna for Wide Bandwidth THz Detection," ICUWB, 2014.

TASK 1836.082: LOW-COST ENERGY-EFFICIENT 60GHZ TRANSCEIVERS WITH BUILT-IN SELF-TEST

ELAD ALON, UC BERKELEY, ELAD@BERKELEY.EDU
ALI NIKNEJAD, UC BERKELEY

SIGNIFICANCE AND OBJECTIVES

CMOS mm-wave technology has the potential to transform short-range communication. Reducing the cost and power consumption of today's CMOS mm-wave transceivers – especially in chip-to-chip communication applications – is the principal goal of this project.

TECHNICAL APPROACH

To make wireless chip-to-chip links viable, our research focus has been on low energy and low cost, enabled by built-in self test (BIST) and on-chip antennas. Low energy consumption can be achieved by exploring extremely efficient circuit topologies, the primary focus of our research. The second approach is to explore extremely high data rates, which allows one to duty cycle the radios and maintain high throughput, low latency links. The first approach favors a lower carrier frequency (60 GHz) while the second favors a higher one (240 GHz). On-chip antennas are a key piece of technology for BIST and for eliminating expensive packaging.

SUMMARY OF RESULTS

In the first approach, a fundamental mode transceiver is designed to operate at 60 GHz, and circuit and system optimization is used to reduce the power consumption of the radio to a great extent. A 4-element transceiver array prototype in 65nm consumes only 115mW. Link measurements up to 10.4 GB/s are error-free over 10^7 symbols at 60cm range broadside, and with 12.5mW/16.25mW (TX/RX) per element. This represents

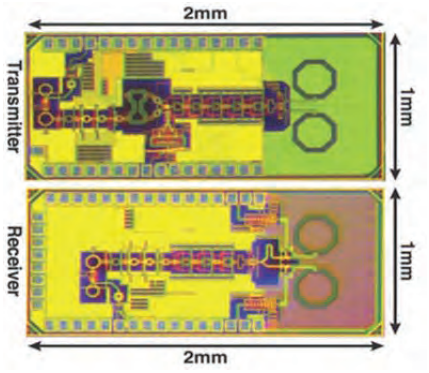


Figure 1: 240 GHz QPSK TX and RX in 65nm CMOS.

the most energy-efficient 10+Gb/s phased-array to date.

The second focus of our project was to realize energy efficient high data rate links at a higher carrier frequency, performed in conjunction with our NSF proposal "A 240GHz QPSK Chip-to-Chip Wireless Link in 65nm CMOS," (NSF ECCS-1201755). In our first 65nm prototype the feasibility of a 240GHz link in CMOS was demonstrated, but the power consumption and resulting energy consumption was rather high (1W and perhaps as low as 100pJ/bit). A second prototype has been designed from the ground up utilizing QPSK modulation, a coherent receiver, and a new slot based on-chip antenna. The transmitter employs an 80GHz local oscillator, a quadrature differential hybrid, and a QPSK modulator. Additionally, an 80GHz class-E switching power amplifier is used to efficiently boost the phase-modulated wideband signal. A frequency tripler then regenerates the modulated signal at 240GHz while preserving the QPSK constellation. By using on-chip slotted loop antennas, the transmitter achieves an EIRP of 1dBm. A maximum data rate of 16Gbps is achieved with a total power consumption of 220mW. A measured eye diagram confirms the stability and QPSK modulation of the transmitter [1]. The receiver uses a direct-conversion mixer-first architecture and is implemented with a 240GHz on-chip antenna. Wideband passive mixers at the frontend employ a 240GHz LO and convert the received signal down to baseband. The baseband signal is then amplified using high gain, wide bandwidth amplifiers. The 240GHz LO chain consists of 27GHz/80GHz injection-locked oscillators, 80GHz amplifiers and a frequency tripler. The overall receiver noise figure is 15dB from measurements. This receiver design achieves a data rate of 16Gbps with a power consumption of 260mW. A full link utilizing both the Tx and Rx demonstrates the functionality of the system. To our knowledge, this is the first demonstration of a fully integrated and operation link implemented in CMOS with a carrier > 200 GHz [2].

Keywords: mm-Wave, BIST, THz, CMOS, wireless

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] S. Kang, et al., "A 240GHz Wideband QPSK Transmitter in 65nm CMOS," RFIC 2014.

[2] S. Thyagarajan, et al., "A 240 GHz Wideband QPSK Receiver in 65 nm CMOS," RFIC 2014.

TASK 1836.083: BUILT-IN TEST FOR POWER-EFFICIENT MILLIMETER-WAVE ARRAYS

BRIAN FLOYD, NORTH CAROLINA STATE UNIVERSITY, BAFLOYD@NCSU.EDU

SIGNIFICANCE AND OBJECTIVES

This program will develop orthogonal code-based built-in-test techniques for millimeter-wave arrays, allowing for simultaneous testing of all elements in the array at either circuit or package level, reducing the time and cost of test. Also, circuit and system architectures to increase the power efficiency of a 60GHz phased array will be explored, and a transmitter with BIST will be demonstrated.

TECHNICAL APPROACH

A low-power 60GHz phased-array transmitter prototype with BIST will be developed in 0.12µm SiGe BiCMOS technology and scalable code-multiplexed test techniques will be developed for this demonstration platform. CDMA test techniques will be compared to both external test and traditional BIST techniques. Power-efficient PA and phase-shifters will be developed and incorporated into a multi-element 60-GHz phased-array prototype with BIST.

SUMMARY OF RESULTS

Code-Multiplexed Test Research: Behavioral simulations have been completed, validating the approach of applying CDMA coding to the phase shifter to allow measurement of all elements in the array simultaneously. A gold-code PRBS generator has been implemented along with a phased array receiver. Power detectors have been built into our 60GHz PAs and software-based test algorithms will be run on the hardware.

Power Amplifier (PA) Research: Our objectives for PA design were to explore ways to enable >10% efficiency at 6dB back-off power levels to reduce the power consumption in a phased array. Multiple PA architectures have been explored, including class-AB, class-J, class-C, and Doherty. Three generations of PAs have been implemented and all have been measured. Our Gen-1 class-AB PA (8/2011) achieved a measured 9dBm output 1dB compression point (OP_{1dB}), 15.6% peak power-added efficiency (PAE), and 3% PAE at 6dB output backoff (OBO) [1]. To improve performance, we explored harmonic termination techniques and developed a multi-harmonic load-pull simulation technique. Using this approach, a 2nd generation class-AB PA (7/2012) was designed and measurements show OP_{1dB} of 12dBm, with 30% peak PAE for a 60GHz PA. Our 3rd generation class-J PA (5/2013) has 25% peak PAE and 9% PAE at 6dB back off. Finally, our Doherty achieves simulated 16.4% PAE at backoff which will be used for the final phased array.

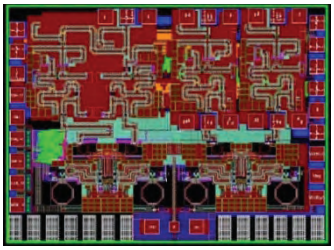


Figure 1: Layout of 60GHz Dual-Vector Doherty Array.

Phase Shifter Research: Our objectives for phase shifter design were to explore compact high-efficiency architectures. Three generations of phase shifters have been developed. Our 1st generation design (8/2011) was a reflective-type topology targeting 360° phase shift in a single stage; however limited varactor Q led to poor performance. Our 2nd generation design was a vector interpolator, achieving a simulated 6dB gain at 31mW and 2°/0.3dB RMS accuracy. Our 3rd generation (5/2013) is a novel dual-vector rotator which can provide two quadrature phase-shifted outputs suitable for efficiently driving a Doherty amplifier. However measurements show functionality but layout parasitics are adversely affecting the performance. A redesign is underway.

60GHz Phase Array Research: In 2013 we taped out a dual-vector Doherty 3-element array which includes our dual-vector rotators, Doherty amplifier, and class-J PAs with BIST. Measurements indicate the individual circuits are working; however, a bug prevents operation of the entire chain. This is currently being redesigned for 9/2014 tape-out and built-in test functions are being expanded.

Keywords: millimeter-wave, phased-arrays, built-in test, 60GHz, CDMA, power amplifiers

INDUSTRY INTERACTIONS

Talks at ARL& IBM (4/14), TxACE Seminar at UTD (5/14)

MAJOR PAPERS/PATENTS

[1] A. Sarkar, K. Greene, and B. Floyd, "A Power-Efficient 4-Element Beamformer in 120-nm SiGe BiCMOS for 28-GHz Cellular Communications," BCTM 2014.

[2] A. Sarkar and B. Floyd, "A 28GHz Class-J Power Amplifier with 18-dBm Output Power and 35% Peak PAE in 120-nm SiGe BiCMOS," SMIC RF Systems 2014.

TASK 1836.091: INTERCONNECTS ON FLEXIBLE PLASTIC SUBSTRATES

DEJI AKINWANDE, THE UNIVERSITY OF TEXAS AT AUSTIN, DEJI@ECE.UTEXAS.EDU

SIGNIFICANCE AND OBJECTIVES

Manufacturing flexible composites for sub-THz interconnects was achieved. A new microcompounding process was developed to prepare bendable PDMS sheets which offers greater flexibility compared to prior polypropylene effort. The refractive index can be tuned by the loading of titania nanoparticles. Advanced techniques were employed to evaluate the flexible PDMS nano-composites.

TECHNICAL APPROACH

Our approach have been focused on fabrication of sub-THz flexible and stretchable waveguide interconnects using polymer nano-composites based on PDMS processable materials. PDMS is a silicon based organic polymer and is well-known for fabrication of MEMS, flexible electronics and for soft lithography. PDMS has several outstanding properties such as flexibility, bio-compatibility, chemical inertness, low attenuation at THz frequencies and high optical transparency. For waveguides, we desire a polymer with high dielectric constant and low attenuation in the frequency band of interest. Here we demonstrate how PDMS nano-composite meets those requirements.

SUMMARY OF RESULTS

PDMS polymer is micro-compounded with TiO_2 nano-particles to obtain polymer nano-composite (Fig. 1). The procedure for synthesis of PDMS nano-composite involves first, mixing Dow Corning's viscous PDMS and curing agent in 10:1 ratio. TiO_2 nano-particles are dispersed into this molten mixture. The molten PDMS nano-composite is slowly injected into waveguide templates with sub-THz (120GHz) rectangular waveguide dimensions. Figs. 2a and 2b are annealed PDMS nano-composite waveguide with 0% and 5% by weight TiO_2 nano-particles. We fabricated waveguides of different composition (5%, 10%, and 20%) by weight percentage. Waveguide permittivity increases with the TiO_2 loading.

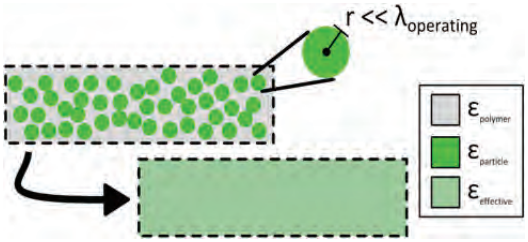


Figure 1: Illustration of the composite material featuring the plastic/polymeric host and the nanoparticle loading. The overall dielectric constant depends on the polymer and the volume loading of the nanoparticles (TiO_2)

Figure 2: Flexible PDMS nano-composite waveguides. a) No TiO_2. b) 5% TiO_2 by weight.

Transmission electron microscopy (TEM) characterization of PDMS composites was performed (Fig. 3), which provides information about nano-particle dispersion in the composite. The TEM image clearly shows the particles are uniformly distributed across the substrate.

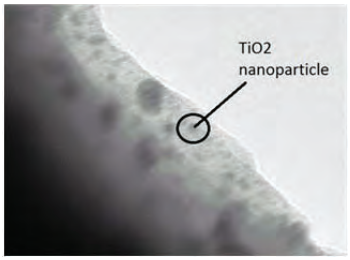


Figure 3: TEM cross section of a PDMS nano-composite.

Fourier Transform Infrared Spectroscopy (FTIR) characterization of the flexible composite was performed to obtain absorption results from the terahertz to infrared frequency band (Fig. 4).

In summary, we have successfully fabricated flexible sheets in which the dielectric constant can be controlled by varying the percent loading of nanoparticles.

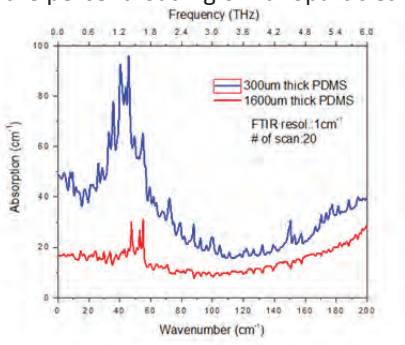


Figure 4: Absorption spectra of PDMS nano-composite.

Keywords: composites, waveguides, interconnects, THz, flexible ribbons

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Emily Walker et al., "Flexible Polymer Nano-Composites for Dielectric Interconnects at Sub-THz Frequencies," SRC Techcon September 2012.

TASK 1836.094: ACCURATE FSM APPROXIMATIONS OF ANALOG/RF SYSTEMS FOR DEBUGGING MIXED-SIGNAL DESIGNS

JAIJEET ROYCHOWDHURY, UC BERKELEY, JR@BERKELEY.EDU
ROBERT BRAYTON, UC BERKELEY

SIGNIFICANCE AND OBJECTIVES

This project aims to develop tools, techniques, and algorithms to automatically generate purely Boolean models (e.g., FSMs, BDDs, AIGs, etc.) that accurately capture the SPICE-level continuous I/O behavior of analog/mixed-signal (AMS) systems. Such models will enable efficient formal analysis, verification, high-speed simulation, validation, and debugging of AMS designs by leveraging existing Boolean analysis tools (e.g., ABC) and hybrid systems frameworks.

TECHNICAL APPROACH

We have developed a suite of techniques for accurately Booleanizing AMS systems, by, (1) discretizing the signals in the system into multi-level sequences of bits, and (2) approximating the analog dynamics of the given system using purely Boolean operations carried out on those bits. One such technique, DAE2FSM, is based on Angluin's algorithm from computational learning theory, which we have adapted to automatically generate Mealy machine models of SPICE-level AMS designs. Another technique, ABCD-D, was designed to Booleanize the analog dynamics underlying cutting-edge digital designs. Yet another technique, ABCD-L, was developed for continuous linear systems, to capture analog effects such as inter-symbol interference (ISI), crosstalk, ringing, etc., to near-SPICE accuracy. Finally, our most powerful general purpose technique, ABCD-NL, extends ABCD-L to Booleanize non-linear AMS systems as well. We have also made progress on formally verifying such Boolean models.

SUMMARY OF RESULTS

We have applied DAE2FSM, ABCD-D, ABCD-L, and ABCD-NL to a number of systems that are of interest to AMS designers. For example, Fig. 1 shows how ABCD can be applied to Booleanize the analog parts of a SAR ADC. This system consists of tightly coupled analog and digital components, so formal analysis/verification of its dynamics is challenging. But with ABCD, each analog component in the system can be modelled very accurately as a purely Boolean unit, and hence one can obtain a system-level description that is all-Boolean, opening the door to formal verification and high-speed simulation using existing Boolean analysis frameworks such as ABC. Fig. 2 illustrates that ABCD can indeed accurately Booleanize AMS designs.

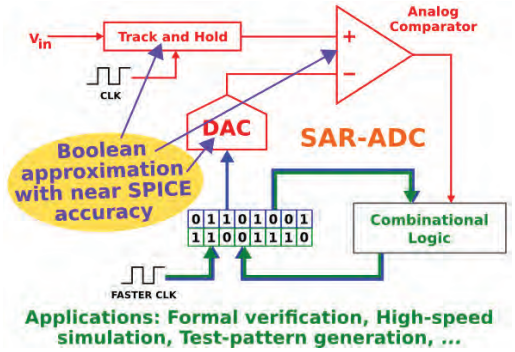


Figure 1.

The blue waveform shows the Booleanized output of the DAC in the above design, as predicted by SPICE, when the ADC input is the red waveform. The green waveform is the output predicted by an ABCD-generated Boolean model for the DAC. As the figure shows, ABCD is clearly able to capture the analog dynamics of the underlying system with very high accuracy. Furthermore, the ABCD-generated Boolean model can be simulated orders of magnitude faster than SPICE, and it can also be formally analyzed/verified.

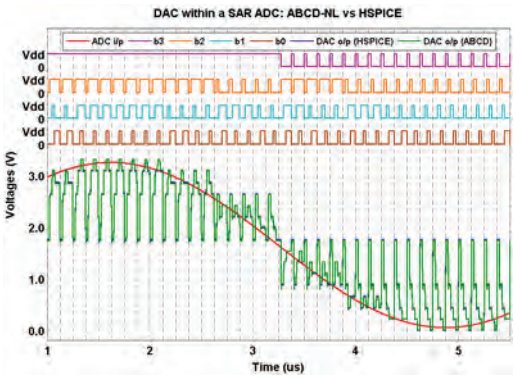


Figure 2.

Keywords: AMS verification, debugging, ABCD, FSM, AIG

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] Aadithya and Roychowdhury, DAE2FSM, DAC 2012

[2] Aadithya and Roychowdhury, ABCD-L, DAC 2013

[3] Aadithya, Roychowdhury, et. al. ABCD-NL, ASPDAC 2014

TASK 1836.101: SPARSE 2D MIMO RADAR TRANSCEIVER DESIGN AND PROTOTYPING FOR 3D MILLIMETER-WAVE IMAGING

MOHAMMAD SAQUIB, THE UNIVERSITY OF TEXAS AT DALLAS, SAQUIB@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

Multiple-input multiple-output (MIMO) radar technologies are explored for millimeter wave (mm-wave) imaging systems in this project. Three-dimensional (3D) mm-wave imagers are designed in order to obtain images of concealed objects. A two-dimensional (2D) sparse MIMO transceiver array is designed to help attain spatial diversity and reduce the number of transceivers.

TECHNICAL APPROACH

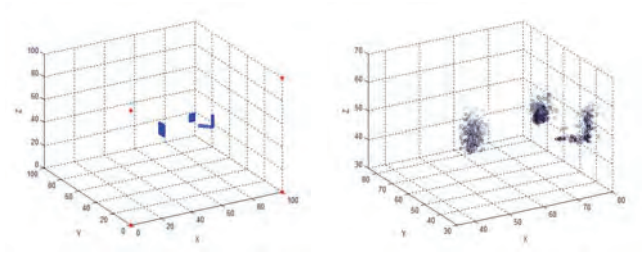
3D mm-wave imagers are designed to obtain images of objects placed behind obstacles or inside closed contours. While the 2D sparse array has a separation in the order of half the wavelength inside an imaging system, several of these "imaging systems" can be placed in the order of several inches apart to obtain localization that leads to 3D images. We showed how a group of imaging sensors located in the close vicinity of a target can provide images respective to their positions, and how this information can be combined to identify a target's presence, location, and shape.

SUMMARY OF RESULTS

We have studied and implemented several schemes to gradually improve the 3D target imaging capability. We first used the angular bin information received from four sensors in constructing the resultant images. Only the presence of point targets can somewhat be estimated based on the angular bins. Therefore, we enhanced our scheme by utilizing the range bins obtained at the four sensors to extract a clearer 3D image. A simple sum-of-pixels was first employed for combining the reflectivity coefficients for each of the pixel values from the four sensors to estimate the likelihood of the presence of a target. More advanced threshold-based interpolation methods were then designed to improve the image.

The effects of the number and location of sensors, and that of objects with different shapes and reflectivity were studied. Changing the orientation of the transceiver arrays has yielded substantial improvement. For example, if the antennas in two sensors are arranged horizontally and that of the other two vertically, the information received from the range and angle bins can complement each other and help reduce the ambiguity.

We have also been working on improving the scene simulation to obtain realistic estimates of the mm-wave radar system environment. A 3D ray tracing simulation is employed, where a large number of discrete rays are generated and each considered individually. The effects of scattering, diffraction and absorption both for the target and neighboring objects are accounted for. The resultant 3D image deteriorates with this improved scene simulation. Images are blurrier due to inclination of the surfaces with respect to the sensors and signal strength variations due to varying transmission distances. The sensor orientations and image recovery algorithms, therefore, are redesigned accordingly.



(a) (b)

Figure 1: Target image (a) and reconstructed image (b) obtained using proposed 3D mm-wave imager.

We have also continued and enhanced the research efforts from our prior project (1836.036). Further improvements were made to the space-time-block-code (STBC) based transmission scheme, and the sensor network localization scheme. We had addressed the use of STBC-based MIMO radar technology to reduce the cost of mm-wave imaging systems by reducing the number of antennas [1]. In [2], we had proposed the use of multiple imaging systems in sensor network target localization for the purpose of surveillance. In addition to our prior studies, we have shown the effects of varying different parameters of the system, such as the regularization parameter, length of the waveform, number of angular bins, etc.

Keywords: MIMO radar; millimeter wave imaging; sparse transceiver array; spatial diversity; pulsed radar.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS

[1] A. Sadeque et al., "Waveform Transmission Scheme for MIMO Radar Imaging Based on Space-Time Block Codes," IEEE Transactions on Aerospace and Electronic Systems, Vol. 50, No. 1, January 2014, pp 12-21.

[2] T. Ali et al., "MIMO Radar for Target Detection and Localization in Sensor Networks", IEEE Systems Journal, Vol. 8, No. 1, March 2014, pp 75-82.

TASK 1836.102: SUPERRESOLUTION TECHNIQUES FOR 3D MILLIMETER WAVE RADARS

MURAT TORLAK, THE UNIVERSITY OF TEXAS AT DALLAS, TORLAK@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

This project aims at developing the 3D superresolution imaging techniques for the millimeter wave applications with appropriate channel model, two dimensional aperture and wideband source. While estimating the various parameters of the interest for the radar, we propose the joint superresolution techniques for better performance.

TECHNICAL APPROACH

We consider the millimeter wave-imaging problem in the automotive radar context. Assuming that wideband FMCW waveforms will be transmitted from a single antenna, reflections from the vehicles as well as other reflective objects will be received by an array of antenna elements, we develop a channel model taking RF aspects and impairments into account. With range, azimuthal & elevation angle and velocity of the target being the parameters of interest we consider the joint estimation techniques to estimate them with superresolution. Conventional direction of arrival algorithms will be modified to obtain angle as well as range and velocity superresolution.

SUMMARY OF RESULTS

At antenna array location varying from *0* to *L-1* and time instances varying from *0* to *N-1* ($N=T*f_s$) received reflected signal from *M* targets across pulses *0* to *P-1* after conjugate mixing and ignoring noise terms is given by:

$$X(l,n,p) = \sum_{1}^{M} e^{-j2\pi(Kt_{dmp}(l)\frac{n}{f_s}+f_c t_{dmp}(l)-0.5Kt_{dmp}^2(l))}$$

Angle, range and velocity superresolution is obtained from multiple antenna elements l, samples over fast time n and slow time p, respectively. For example for range and angle superresolution, the collected data are spatially smoothed in time and space domain. Steering vectors are written in terms of range and angle of particular target and 2D MUSIC algorithm is applied to locate the targets. Thus using the joint superresolution technique, we can separate the objects closely spaced in range as well as angular domain. In Fig.1, three closely spaced cars are shown separated using this algorithm with the detection SNR of 30 dB. The superresolution algorithms are computationally expensive due to two factors. One is large size of covariance matrix and other is grid search over the target space. We need to apply projection-based techniques to reduce the cost of computation. Performance complexity trade off needs to be analyzed while implementing these algorithms.

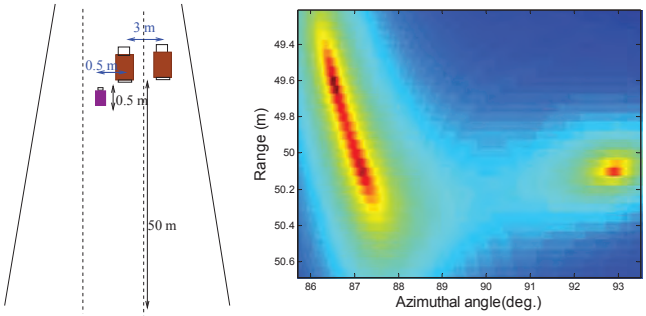


Figure 1: Joint superresolution application in typical traffic scenario

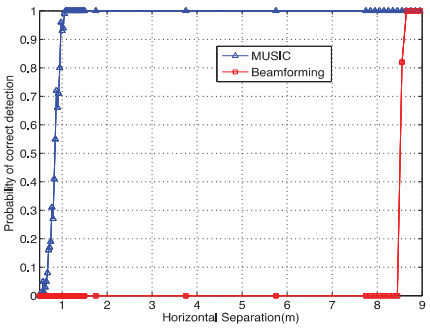


Figure 2: Comparison of algorithms for angular separation

We also analyze the performance of range, angle and velocity estimation in the presence of additive white noise and derive the analytical formulation in terms of probability of false detection. The statistical analysis to compare the performance of the superresolution algorithms with the existing techniques is carried out using Monte-Carlo analysis and cumulative distribution functions. To understand end-to-end operation of the radar system we have developed the imaging toolbox with automotive radar scenario. Typical radar parameters can be estimated with different algorithms. Antenna patterns and other RF parameters can be selected to analyze the performance of these algorithms.

Keywords: Joint Estimation, Superresolution, FMCW, Automotive Radar, RF impairments

INDUSTRY INTERACTIONS

Texas Instruments, IBM

TASK 1836.119: DEMONSTRATION OF 180-300 GHZ TRANSMITTER FOR ROTATIONAL SPECTROSCOPY

KENNETH K. O, THE UNIVERSITY OF TEXAS AT DALLAS, EMAIL K.K.O@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

As part of the effort to help open up the high millimeter and sub-millimeter wave frequency range for moderate volume and cost applications, this task is seeking to demonstrate a 180-300 GHz transmitter in CMOS for a rotational spectrometer that detects harmful molecules and analyzes breath.

TECHNICAL APPROACH

The transmitted power should be ~10-100 μW. The main challenges are increasing the output frequency range, power, and frequency for phase locked signals. To realize a fast scan rate with a 10-kHz step, use of a fractional-N synthesizer is being investigated. The synthesizer will also incorporate a frequency modulation function. The output signal is generated using a combination of an N-push technique and a frequency multiplication technique. This task will also help generating the receiver LO signal.

SUMMARY OF RESULTS

As a step toward the demonstration of 200-300 GHz transmitter for rotational spectroscopy, a transmitter using a fractional-N PLL (FNPLL) that generates frequency shift keyed (FSK) signals at 85 to 127 GHz (39% tuning range) with a fine frequency step of 570 Hz and settling time of ~10 μS is demonstrated. FSK is used to detect small absorption dips out of the baseline variations caused by frequency dependent output power, standing waves in a sample chamber and others. Implemented in 65-nm CMOS, the FNPLL delivers greater than 5 μW of output power, and achieves measured phase noise of less than -70 dBc/Hz in-band and less than -102 dBc/Hz at 10-MHz offset over the output frequency range while consuming 80 mW. The transmitter output is radiated using a bond-wire antenna and successfully utilized in a spectrometer for detection of gas molecules.

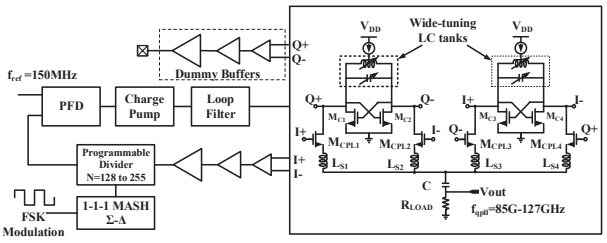


Figure 1: Block diagram including a QVCO with broadband passive coupling and freq. multiplication by 4.

A block diagram of the transmitter is shown in Fig. 1. The signal is generated using a quadrature oscillator operating around 26.5 GHz and a passive broadband frequency multiplication-by-4 circuit. This frequency plan enables use of a switched inductor for a wide tuning QVCO and inductor-less static dividers. The PLL is a 4th order Type-II design with a 3rd order Σ-Δ for sufficient randomization of fractional input. The charge pump current is controlled to maintain the loop bandwidth of 1-2 MHz. To keep the bandwidth sufficiently high for VCO noise rejection, the quantization step for modulator is kept low to one VCO cycle. This lowers the phase step at the PFD input in fractional mode for lower quantization noise, fractional spur level and noise folded in-band due to PFD-CP nonlinearities. Frequency scanning across an octave of operating range is implemented using a programmable divide-by-N circuit with N=128 to 255 that also supports 20-bit fractional resolution. Fig. 2 shows a die photograph of the transmitter and measured spectra for CH_3CN.

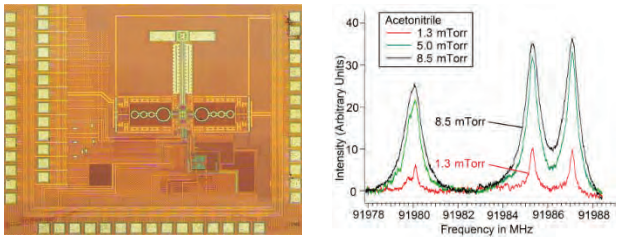


Figure 2: (Left) Die photo of the transmitter, (Right) Measured Spectra for CH3CN with pressure as variable.

Keywords: rotational spectrometer, transmitter, CMOS, millimeter-wave.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] D. Shim et al., "Components for Generation and Phase Locking 390-GHz Signal in 45-nm CMOS," IEEE VLSI Symp. on Circuits, pp. 10-11, June 2012, Honolulu, HI.

[2] N. Sharma et. al," 85-to-127 GHz CMOS TX for Rotational Spectroscopy," Accepted to 2014 IEEE CICC.

[3] J. Zhang et al., "21.5-to-33.4GHz VCO using NMOS Switched Inductors in CMOS," Accepted to IEEE Microwave and Wireless Components Letters.

TASK 1836.120: EVALUATION OF FREQUENCY AND NOISE PERFORMANCE OF CMOS 180 – 300 GHZ SPECTROMETER TRANSMITTER AND RECEIVER COMPONENTS

MARK LEE, THE UNIVERSITY OF TEXAS AT DALLAS, MARKLEE@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

A gas phase absorption spectrometer in the 100 to 1000 GHz frequency range would be extremely valuable to rapidly and precisely assay a wide range of chemical vapors. This project's objective is to quantitatively evaluate materials and devices for suitability as millimeter and sub-millimeter wave components to be integrated into such a spectrometer system.

TECHNICAL APPROACH

The 2nd year of this project undertook two tasks: (1) continued use of Fourier transform spectroscopy (FTS) to evaluate dielectric characteristics of passive material components, and (2) using free-space quasi-optical techniques to quantitatively characterize the frequency and power characteristics of active oscillators. In (1), broadband FTS was used to measure the dielectric function and loss tangent of SU8 and BCB, two candidate substrate materials for sub-millimeter wave antennas and circuits. In (2), FTS and photo-acoustic calorimetry were used to measure the broadcast power and frequency spectrum of a solid-state multiplier oscillator widely used in the TxACE research lab.

SUMMARY OF RESULTS

In a collaboration with Dr. Rashaunda Henderson's group, this project expanded upon the previous year's results characterizing FR4 laminate in the search for low cost, low dispersion, and low loss substrate/backplane dielectric materials to support transmitter/receiver antennas and waveguide connections. Materials' dielectric and loss properties are not typically reported in the literature above 30 GHz. FTS methods were thus used to measure these critical characteristics for the free-standing polymeric resist materials SU8 and BCB from 150 GHz to 70 THz. By measuring both reflection and transmission, the complex dielectric function could be obtained. Results showed that BCB maintains a relative permittivity of 2.7 up to near 1 THz with a low loss tangent of < 0.005. Above 1 THz, the permittivity remains approximately dispersionless but the loss tangent gradually rises. SU8 has a permittivity near 3.8 and a loss tangent of 0.02 that rises gradually with increasing frequency. Near 9 THz SU8 shows a large dielectric resonance where dispersion and loss become very large.

A second capability demonstrated this past year has been the use of a photo-acoustic absolute power meter, built last year, and the FTS system to quantitatively characterize the broadcast power and frequency characteristics of sub-millimeter wave electronic oscillators. Previously, power measurements could only be done in a rectangular waveguide, while for a spectrometer it is the free-space broadcast power that really matters. We found that the actual broadcast power in the forward lobe of a horn antenna on a solid-state multiplier oscillator at 840 GHz was only ~ ½ the nominal power measured in a waveguide. Furthermore, a more precise measurement of the actual output frequency showed the fundamental output to be 837.8 GHz, with a relatively low level of 2nd and 3rd harmonic distortion and an interharmonic at 5/3 of the fundamental whose origin is presently unknown. The broadcast spectrum is shown in Fig. 1. For spectrometer purposes, it is critical to be able to characterize the true frequency output of an oscillator, including harmonic content, with high accuracy to correctly identify absorption lines.

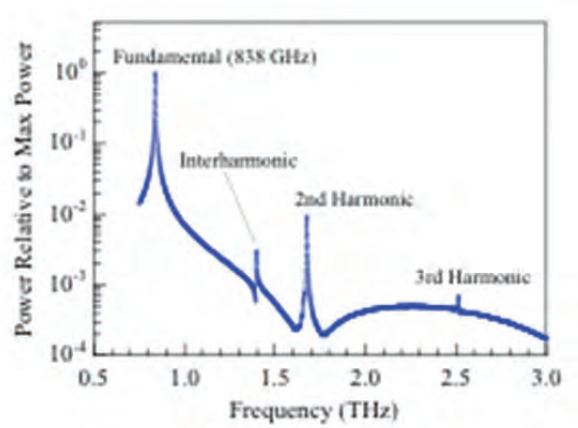


Figure 1: Spectrum of the relative broadcast power output from a solid-state multiplier source nominally set to 840 GHz. Measurements were made via Fourier transform spectroscopy.

Keywords: Millimeter-wave, Terahertz, Spectrometer, Dielectric loss, Power meter

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] S. Aroor, B. L. Brown, M. Lee, R. Henderson, "Evaluation of FR4 laminates for millimeter-wave and terahertz circuit applications," (submitted to Journal of Infrared, Millimeter, and Terahertz Waves, 2014)

TASK 1836.122: ON-CHIP INTEGRATION TECHNIQUES FOR 180-300 GHZ SPECTROMETERS

RASHAUNDA HENDERSON, THE UNIVERISTY OF TEXAS AT DALLAS,
RMH072000@UTDALLAS.EDU
ANDREW BLANCHARD, THE UNIVERSITY OF TEXAS AT DALLAS

SIGNIFICANCE AND OBJECTIVES

The objectives include design and fabrication techniques to integrate a CMOS-based gas spectrometer with on-chip broadband planar aperture antennas.

TECHNICAL APPROACH

The approach uses coplanar waveguide (CPW) interconnects fabricated in a post-IC technology and a planar aperture bowtie antenna that uses electromagnetic band gap (EBG) structures to eliminate surface waves caused by a thick grounded dielectric. The design of the antennas, interconnects and vertical transitions have been carried out using ANSYS HFSS. If successful, this technology can lead to the design of and implementation of affordable gas spectrometers that can be used for safety and security applications.

SUMMARY OF RESULTS

To date we have been able to fabricate a 200 GHz planar bowtie aperture antenna that is integrated onto a 15 ohm-cm silicon substrate using SU-8 photoresist as the dielectric. In the design of this antenna we have characterized the relative permittivity and loss tangent of the SU8 from 140 to 220 GHz using split ring and T-resonators.

SU8 has been used in microelectromechanical systems (MEMS) research to serve as a sacrificial layer when creating mechanical devices and structures. The novelty about using SU-8 is that it can be deposited using a photoresist spinner in thick layers up to 200 micrometers. Once cured or cross-linked, the polymer is therefore a stable flat material similar to a dielectric. The loss tangent of SU-8 is higher than most dielectrics used in millimeter wave circuit design but for the purposes of antenna design, the loss does not adversely affect antenna performance. Vias can be created in SU-8 by using standard photolithography development techniques.

Fig. 1 shows the cross-section of the silicon substrate after additional SU-8 and gold metal layers have been included. When the antenna is positioned in the vicinity of a CMOS substrate, a ground plane reflector is used to prevent energy from radiating into the silicon. The distance between the reflector and antenna is $\lambda/4$. An electromagnetic bandgap (EBG) structure (using vias and square patches) will disrupt propagating modes and can eliminate surface waves caused by the $\lambda/4$ dielectric.

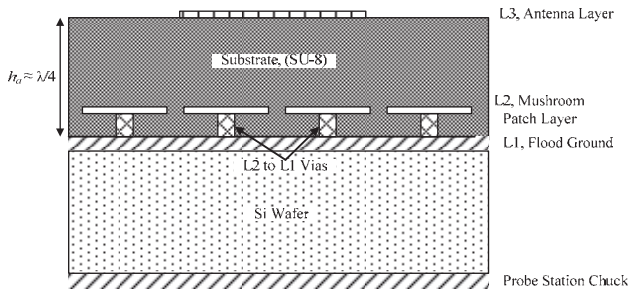


Figure 1: Cross-section of the layers used in processing the 200 GHz antenna using SU-8.

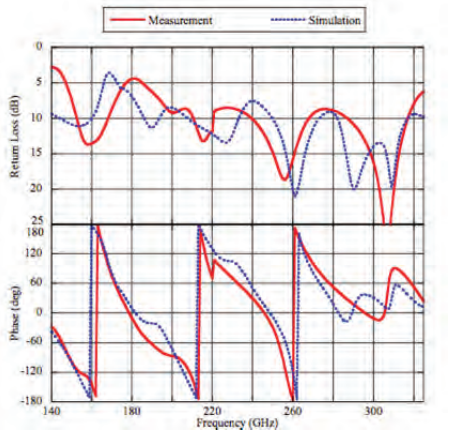


Figure 2.

Fig. 2 shows the measured and simulated return loss and phase of the antenna from 140 to 325 GHz. A 7dB return loss is achieved from 190 to 315 GHz. The antenna has now been demonstrated in isolation and future work will involve measuring the antenna radiation using FTIR with Prof. Mark Lee and incorporating the radiator with an actual active circuit fabricated by a foundry.

Keywords: planar bowtie antennas, SU8, CMOS, post-IC

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] R.G. Pierce, A.J. Blanchard, R. Islam & R. Henderson, "SU-8 2000 Millimeter Wave Material Characterization," IEEE Microwave and Wireless Components Letters, Vol. 24, No. 6, pp. 427-429, June 2014.

[2] R. Islam & R. Henderson, "Millimeter-Wave Coplanar Waveguide Series Stubs on BCB and Low Resistivity Silicon," Microwave and Optical Technology Letters, Vol. 56, No. 2, pp. 375–380, February 2014.

TASK 1836.126: DESIGN SPIN REDUCTION VIA INTEGRATED THZ DESIGN: APPLICATIONS, PHYSICS, AND SYSTEM ENGINEERING

FRANK C. DE LUCIA, OHIO STATE UNIVERSITY, FCD@MPS.OHIO-STATE.EDU
CHRISTOPHER F. NEESE, OHIO STATE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

The objective of this project is to develop a THz System Engineering Tool that allows for analysis of systems based on the characteristics of their building blocks and to validate it by applications to systems of interest. These systems include CMOS gas sensors and systems for process diagnostics and control.

TECHNICAL APPROACH

Our laboratory specializes in the design, development, and application of high-resolution THz systems for the study of gas phase systems. Specific foci of this effort include: (1) In the near to medium term, diagnostics and process control in semiconductor plasma reactors using commercially available III-V systems, and (2) in parallel and the longer term, the development of CMOS systems for this application, as well as more generally for gas sensors. Tying this together is a computationally based THz System Evaluation Tool, which is being designed as a more general tool for use by less system oriented CMOS developers.

SUMMARY OF RESULTS

Fig. 1 shows our diagnostic system in place on an Applied Materials Semiconductor Plasma Processing Reactor and a THz spectral line that arises from the SiO that has been removed from the wafer by the plasma.

Fig. 2 shows high-resolution spectroscopy lines that demonstrate the good spectral purity of the UT-D CMOS synthesizer.

Fig. 3 shows the organization of the THz System Engineering Tool that is used to relate design choices for THz systems to their performance.

Keywords: sub-millimeter, terahertz, spectroscopy, plasmas, semiconductors

INDUSTRY INTERACTIONS

Applied Materials, Texas Instruments, IBM

MAJOR PAPERS/PATENTS

[1] Y. H. Helal et al., "Submillimeter Spectroscopic Diagnostics in Semiconductor Processing Plasmas," 69th Int. Symp. on Mol. Spect, Urbana, IL, 2014

[2] N. Sharma, et al., "85-to-127 GHz CMOS Transmitter for Rotational Spectroscopy," 2014 IEEE Custom Integrated Circuit Conference

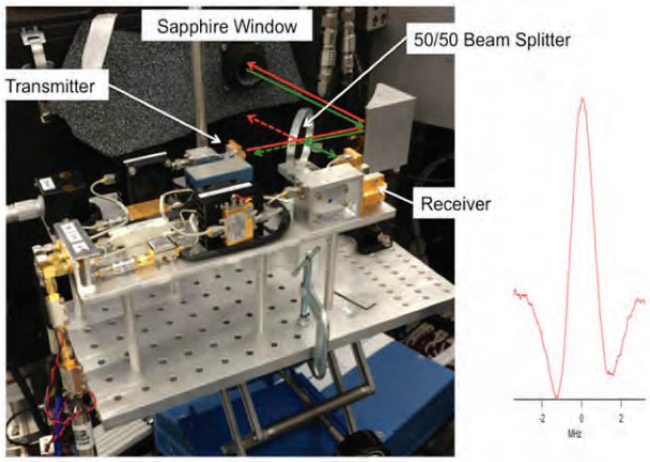


Figure 1: THz diagnostics system in place on Applied Materials semiconductor plasma processing reactor (left). SiO line (right).

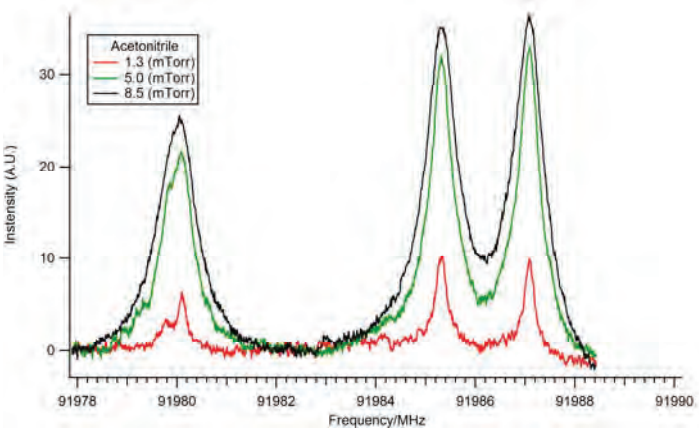


Figure 2: Spectrum of Acetonitrile as a function of pressure.

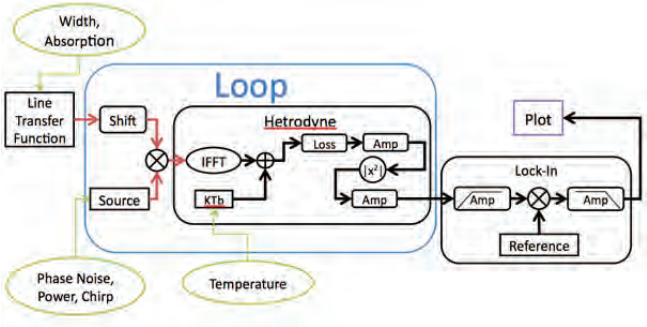


Figure 3: Outline of THz SET.

TASK 1836.131: PROCESS VARIATION ANATOMY: A STATISTICAL NEXUS BETWEEN DESIGN, MANUFACTURING & YIELD

YIORGOS MAKRIS, THE UNIVERSITY OF TEXAS AT DALLAS,
YIORGOS.MAKRIS@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

Monitoring the impact of process variation is crucial for yield enhancement, test time reduction and providing feedback to both process engineers and designers.

TECHNICAL APPROACH

We seek to analyze systematic process variation using dynamic wafer-level spatial decomposition to break down the systematic variation of a wafer to a set of parameterized basis functions based on a small number of measurements across a wafer. The key challenge is to identify an appropriate set of basis functions and the key novelty of the proposed method is that, instead of employing a fixed set of statically defined basis function, it uses domain-specific knowledge and data mining to dynamically learn most appropriate functions. Then, these dynamically learned basis functions serve as an interface for linking yield and design parameters to process variation.

SUMMARY OF RESULTS

The results of our approach for two applications are summarized below. First, we investigate how a process engineer can benefit from spatial correlation modeling in order to reduce IC laser trimming costs. Second, we study estimation of HVM yield from a few early silicon wafers via spatio-temporal process variation correlation models.

1) Laser trimming is used extensively to ensure accurate values of on-chip precision resistors in the presence of process variations. Such laser resistor trimming is slow and expensive, typically performed in a closed-loop, where the laser is iteratively fired and some circuit parameter (i.e. current) is monitored until a target condition is satisfied. Toward reducing this cost, we introduce a novel methodology (Fig. 1) for predicting the laser trim length, thereby eliminating the closed-loop control and speeding up the process. Predictions are obtained from wafer level spatial correlation models, learned from a sparse sample of die on which traditional trimming is performed.

2) Prior to commencing High Volume Manufacturing (HVM), die samples from early wafers are obtained and subjected to thorough characterization. The objective of such characterization is manyfold and includes post-silicon design validation as well as HVM performance and yield estimation. In reality, only a small number of engineering wafers are available for such analysis and only a small number of die are measured from wafers.

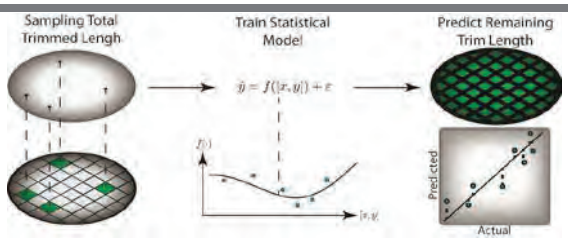


Figure 1: Laser trimming speed-up through wafer-level spatial modeling.

In general, the problem is to infer the probability density function (PDF) of the entire population based on a given sample which is a small set of observations over a few wafers. A simple solution is to use this sample and estimate the PDF by applying histogram-based or kernel-based estimation techniques. However, we can improve the quality of that sample by using correlation model of available observations. For this purpose we combine spatial and temporal information of measurements from available die locations over wafers and build a spatio-temporal model. Then, we use the trained model to predict those parameters of interest for un-sampled die locations. New samples which are a combination of measurements and predictions are then used to estimate the density function. Fig. 2 shows an overview of the proposed approach.

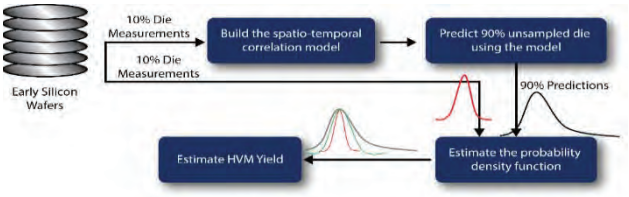


Figure 2: HVM yield estimation approach.

Keywords: process variation, yield estimation, correlation model, laser trimming, cost reduction

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] C. Xanthopoulos et al., "IC Laser Trimming Speed-Up through Wafer-Level Spatial Correlation Modeling," accepted to the IEEE International Test Conference, 2014.

[2] A. Ahmadi et al., "Spatiotemporal Wafer-Level Correlation Modeling with Progressive Sampling: A Pathway to HVM Yield Estimation," accepted to the IEEE International Test Conference, 2014.

TASK 1836.147: DEMONSTRATION OF 180-300 GHZ RECEIVERS FOR ROTATIONAL SPECTROSCOPY

WOOYEOL CHOI, THE UNIVERSITY OF TEXAS AT DALLAS,
WOOYEOL.CHOI@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

A key component of low-cost rotational spectrometer, for detection of harmful gas and breath analyses is a CMOS transceiver. Since only 10 to 100 µW can be transmitted into the gas under test, highly sensitive receivers are required. This task will develop wideband integrated receivers for rotational spectrometers.

TECHNICAL APPROACH

From the previous researches, it is found that nonlinear devices in standard CMOS, such as anti-parallel Schottky barrier diodes and FET switches, can be used to realize passive mixers in 180-300 GHz. Techniques to improve bandwidth and sensitivity will be investigated. To improve sensitivity, local oscillator (LO) amplifiers and intermediate frequency (IF) low noise amplifiers will be integrated with passive mixers. Wideband RF/LO/IF combining and isolation structure will be designed to increase the receiver bandwidth. Integration and co-optimization of wideband radiators will also be investigated. Finally, the performance of the receiver will be evaluated in a spectrometer.

SUMMARY OF RESULTS

Integrated receiver design: Even though the performance of the passive mixer is the most important part of the receiver chain, the overall noise performance is dependent on the noise figure of the intermediate frequency amplifier. To improve sensitivity passive mixers and IF low-noise amplifiers will be integrated, and co-optimized. Also, LO power should be delivered to the mixer core in a stable and efficiency way. To achieve this, a power amplifier for LO amplification will be integrated in the receiver. The signal generator developed in Task #1836.119 will be used as the LO.

Wideband signal combining and isolation structure: Impedance engineering at RF/LO/IF and their harmonic frequencies is required for passive mixer design and optimization. For example, the impedance matching from antenna to nonlinear device, port-to-port isolation and optimum reactive termination for unwanted harmonic components should be obtained at the same time. Typically, these are implemented with tuned circuits which results a narrow bandwidth. To achieve wideband operation, band-switching or a wideband impedance transformation network is required. Band-switching can be employed for LO frequencies and IF which are relatively low. Techniques to achieve a wideband impedance transformation network (180-300 GHz) with a compact form factor to minimize excess loss will be investigated.

Wideband radiator co-design: To demonstrate wideband receivers in a spectrometer, the RF interface should be able to handle wideband signals. In the 180-300 GHz range, non-contact interfaces such as on-chip antenna and/or electromagnetic coupling, can be good alternatives to wire bonding and/or flip-chip bonding which can be lossy, narrowband and costly. Wideband on-chip radiators are key components to enable non-contact interfaces. Thanks to recent advances in packaging techniques, such as wafer thinning and new low-cost mm-wave substrates, bandwidth and efficiency of on-chip radiators can be greatly improved. Feasibility of wideband on-chip radiators are being investigated in collaboration with Task #1836.122.

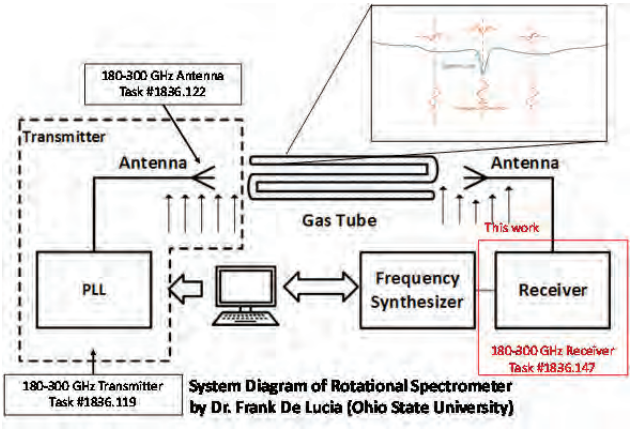


Figure 1: system block diagram of 180-300 GHz rotational spectrometer

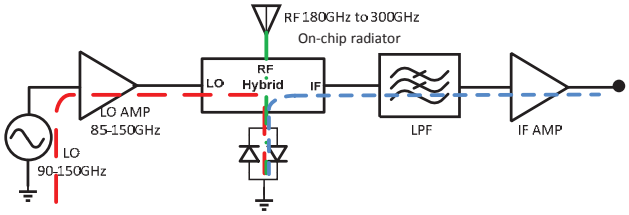


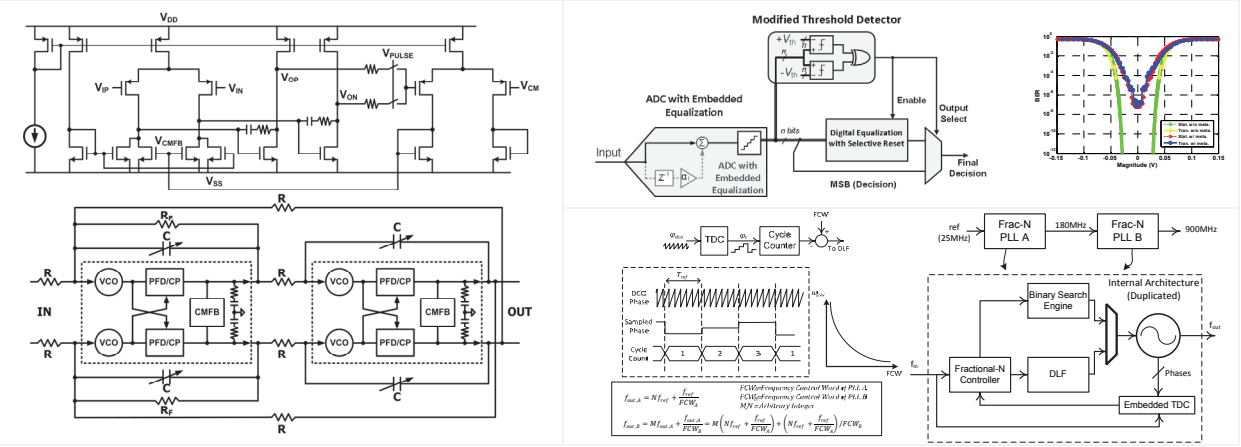
Figure 2: block diagram of integrated receiver

Keywords: integrated receiver, on-chip radiator, passive mixer, rotational spectroscopy, wideband receiver

INDUSTRY INTERACTIONS

Texas Instruments Inc.

Fundamental Analog Thrust



Category	Accomplishment
Fundamental Analog	ADC-based high-speed serial links aim to improve interconnect bandwidth density in an energy-efficient manner. Embedding the normally required channel equalization within the ADC has the potential for significant power savings. The first 10Gs/s ADC with embedded FFE/DFE that achieves a BER of 10^{-9} at 10Gb/s over a 10" channel is demonstrated. The 6bit ADC has an FOM (0.48pJ/c-s) that is as competitive as the FOM of plain vanilla ADCs that operate at that speed. (1836.111, PI: S. Palermo, Texas A&M University) Publication: E. Zhian Tabasy, A. Shafik, K. Lee, S. Hoyos, S. Palermo "A 6b 10GS/s TI-SAR ADC with Embedded 2-TAP FFE/1-Tap DFE in 65nm CMOS," IEEE VLSI Sym., June 2013. (Winner best in session at Techcon 2013)
Fundamental Analog	To design high-performance ADPLLs that utilize digital synthesis and automatic place-and-route flows to simplify the design and to facilitate easier integration with SoCs, a fractional-N dividerless frequency synthesis technique has been proposed and used to implement an ADPLL. The ADPLL achieves ~3X lower jitter than the state of the art custom designed fractional-N PLL operating around 900 MHz. (1836.078, PI: D. Wentzloff, University of Michigan)

TASK 1836.057: HIGH ACCURACY ALL-CMOS TEMPERATURE SENSOR WITH LOW-VOLTAGE LOW-POWER SUBTHRESHOLD MOSFETS FRONT-END AND PERFORMANCE-ENHANCEMENT TECHNIQUES

CHANGZHI LI, TEXAS TECH UNIVERSITY, CHANGZHI.LI@TTU.EDU

SIGNIFICANCE AND OBJECTIVES

This project investigates scattered temperature sensor based on subthreshold-MOSFETs and Schottky barrier diodes (SBD) for on-chip thermal management, aiming to achieve low supply voltage, small chip size and high accuracy with no or minimal calibration/trimming.

TECHNICAL APPROACH

SBD, subthreshold MOSFETs, dynamic threshold MOSFET (DTMOS) diode and bulk-driven technique are used for low supply voltage. Dynamic element matching (DEM), dynamic offset cancellation (DOC) and gain boosting are adopted to minimize device mismatch induced errors. Low-voltage low power inverter-based sigma-delta modulator is investigated for temperature reading. Furthermore, scattered thermal monitors with small sensing diodes distributed across the chip are developed for high accuracy relative temperature measurement.

SUMMARY OF RESULTS

Low-voltage relative temperature sensors were implemented in a 180 nm CMOS process with four types of sensing diodes: SBD, subthreshold MOSFET diode, DTMOS diode, and PNP-BJT diode. 7 × 7 small remote sensor nodes are implemented on the chip with a deployment density of 49/0.81 mm^2 and sharing the same bias current generator, control logic and data converter. The measured minimum supply voltage (analog) of the sensor is 0.7 V over -55 to 125 °C for the three types of low voltage diode-based implementation. The measured relative sensing inaccuracies (3σ) without calibration are less than ±1.5 °C, ±1.2 °C and ±1°C for the designs based on SBD, subthreshold MOSFET and DTMOS, respectively. To our knowledge, this is the first time that non-calibrated relative sensing accuracy is reported for SBD-based and DTMOS-based temperature sensors, and the best reported result for the design based on subthreshold MOSFET. Furthermore, the multi-location thermal monitoring function has been experimentally demonstrated and a 1.8 °C/mm on-chip temperature gradient was detected.

On the top level, several interface structures between sensor nodes and the core, including a tree multiplexer (MUX), a row–column selection MUX and a tree–column selection MUX, are investigated. Tradeoffs among leakage current, area, and headroom for each structure are summarized. A design guide for various performance requirements is provided.

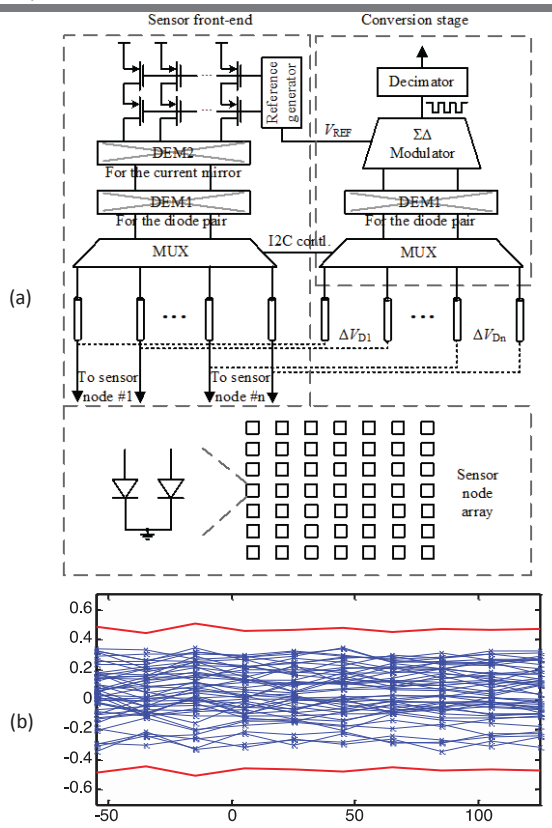


Figure 1: (a) 7×7 relative temperature sensor. (b) Measured temperature inaccuracy.

Keywords: subthreshold MOSFETs, Schottky barrier diode, scattered temperature sensor, low voltage, multi-location thermal monitoring

INDUSTRY INTERACTIONS

Intel, IBM, Freescale, GLOBALFOUNDRIES.

MAJOR PAPERS/PATENTS

[1] B. Vosooghi, et al., "Leakage, area, and headroom tradeoffs for scattered relative temperature sensor front-end architectures," IEEE TCAS-II, vol. 61, no. 2, pp. 80-84, February 2014.

[2] L. Lu, et al., "A 0.45 V MOSFETs-based temperature sensor front-end in 90nm CMOS with a non-calibrated ±3.5 ^{0}C 3σ relative inaccuracy from -55 ^{0}C to 105 ^{0}C," IEEE TCAS-II, vol. 60, no. 11, pp. 771-775, November 2013.

[3] L. Lu, et al., "A subthreshold-MOSFETs-based scattered relative temperature sensor front-end with a non-calibrated ±2.5 ^{0}C 3σ relative inaccuracy from -40 ^{0}C to 100 ^{0}C," IEEE TCAS-I, vol. 60, no. 5, May 2013.

TASK 1836.058: HIERARCHICAL MODEL CHECKING FOR PRACTICAL ANALOG/MIXED-SIGNAL DESIGN VERIFICATION

PENG LI, TEXAS A&M UNIVERSITY, PLI@TAMU.EDU

SIGNIFICANCE AND OBJECTIVES

Analog/mixed-signal (AMS) verification has grown in importance as the AMS design complexity increases and verification becomes a significant bottleneck in design. This project aims to address the grand challenges in AMS verification by developing a variety of techniques including hierarchical analog behavioral model equivalence checking, formal and semi-formal methods and machine-learning guided verification.

TECHNICAL APPROACH

Many formal verification methods are not scalable due to the inherent computational complexity associated with the verification of analog and mixed-signal circuits. Recently, we have been primarily working towards addressing the scalability challenge of analog and mixed-signal circuit verification by developing various device and circuit level modeling techniques and incorporating such techniques into the verification framework. The use of these two techniques has allowed us to significantly speed up the challenging transient verification of several AMS designs such as PLLs.

SUMMARY OF RESULTS

DC operating point analysis is a pivotal step in most circuit simulation/verification tasks. Current tools leverage continuation methods and homotopy to find one DC operating point and cannot guarantee finding all such points. Recent advances in SMT (Satisfiability Modulo Theory) solvers have prompted new work in formal approaches to solve this problem but have been successfully applied only to extremely small circuits. In this project, we couple various abstraction techniques with SMT based search to find all DC equilibrium points for large circuits. While the problem is by no means solved, we reveal several important observations and techniques towards making this problem tractable.

We have explored various device modeling approaches with the aim of incorporating conservative yet accurate device models into the process of formal DC operating point analysis. To this end, we have found that partitioning transistor IV characteristics in a non-uniform manner and leveraging the resulting conservative bounds for the IV characteristics can lead to noticeable runtime speedups in DC verification (Fig. 1). In addition, decomposing a large mixed-signal circuits into multiple strongly connected components (SCC's) can speed up formal SMT-based analysis. This requires certain smart loop breaking techniques (Fig. 2).

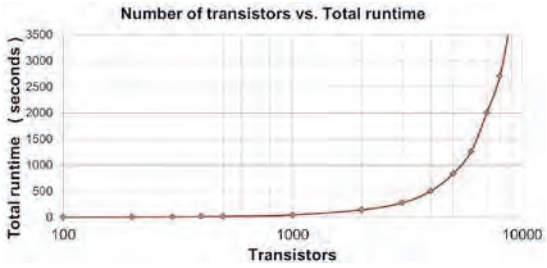


Figure 1: Accelerated DC verification solving time with non-uniform partitioning of device characteristics as a function of size of the circuit.

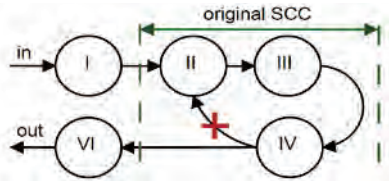


Figure 2: Speeding up DC verification by decomposing into multiple SCCs and breaking feedback loops.

We have also worked on transient verification of digitally-intensive analog circuits. We develop a machine learning approach to convert digital blocks to conservative analog approximations via the use of kernel ridge regression. These learned models are then adopted in a hybrid formal reachability analysis framework where the support function based manipulations are developed to efficiently handle the large linear portion of the design and the more general SMT technique is applied to the remaining nonlinear portion. This approach has sped up the lock time verification of a digital PLL against uncertain initial conditions by more than 70X.

Keywords: verification, analog and mixed-signal, reachability analysis, machine learning, formal methods

INDUSTRY INTERACTIONS

Intel, Freescale, Texas Instruments

MAJOR PAPERS/PATENTS

[1] H. Lin, P. Li and C. Myers, "Verification of digitally-Intensive analog circuits via kernel ridge regression and hybrid reachability analysis," IEEE/ACM DAC, 2013.

[2] P. Mukherjee, C. Amin and P. Li, "A formal approach to DC operating point analysis for large mixed signal circuits: challenges and opportunities," SRC TECHCON, 2013.

TASK 1836.075: DESIGN OF 3D INTEGRATED HETEROGENEOUS SYSTEM

SAIBAL MUKHOPADHYAY, GEORGIA INSTITUTE OF TECHNOLOGY, SAIBAL@ECE.GATECH.EDU
SUNG-KYU LIM, GEORGIA INSTITUTE OF TECHNOLOGY

SIGNIFICANCE AND OBJECTIVES

The objective of this research is to address the challenges to 3D integration of highly different circuits/systems with varying technology, power profiles, operating voltage, and clock domains through the 3D technology using Through-Silicon-Via (TSV).

TECHNICAL APPROACH

The performance, power, and reliability of a 3D-Integrated Heterogeneous System (3D-IHS) depend on the functionality, power profile, and frequency of individual dies; the non-uniformity in their physical environments; die-to-die coupling; and die-to-package coupling. This research will develop design methods for the 3D-IHS and transform them into design tools.

SUMMARY OF RESULTS

1. TSV-to-TSV coupling extraction and mitigation [1]: TSV-to-TSV coupling is a new parasitic element in 3D ICs and can become a significant source of signal integrity problem. Existing studies on its extraction, however, becomes highly inaccurate when handling more than two TSVs on full-chip scale. We investigated the multiple TSV-to-TSV coupling issue and propose an accurate model that can be efficiently used for full-chip extraction. Unlike the common belief that only the closest neighboring TSVs affect the victim, our study shows that non-neighboring aggressors also cause non-negligible impact. Based on this observation, we propose an effective method of reducing the overall coupling level in multiple TSV cases.

2. TSV-to-wire coupling extraction and mitigation [2]: In this work, for the first time, we model and extract the parasitic capacitance between TSVs and their surrounding wires in 3D IC. For a fast and accurate full-chip extraction, we propose a pattern-matching-based algorithm that considers the physical dimensions of TSVs and neighboring wires and captures their field interactions. Our extraction method is accurate within 1.9% average error for a full-chip-level design while requiring negligible runtime and memory compared with a field solver. We also observe that TSV-to-wire capacitance has a significant impact on the noise of TSV-based connections and the longest path delay. To reduce TSV-to-wire coupling, we present two full-chip optimization methods, i.e., increasing KOZ and guard ring protection that are shown to be highly effective in noise reduction with minimal overhead.

3. Asynchronous Interface for Die-to-Die Communication in 3D ICs: An asynchronous FIFO is designed to enable die-to-die communication between multiple dies operating at different VDD and frequency in a heterogeneous 3D IC. The different design options for the FIFO is investigated including (i) 3D FIFO - where the read/write circuits of the FIFO are split between two dies and (ii) 2D FIFO – where the entire communication block is in a single die. The effect of process variations in the individual dies (die-to-die variation) i.e. the logic blocks sending/receiving data as well as the FIFO circuits are considered. The analysis shows the 3D FIFO results in a lower footprint; however, requires more die-to-die vias. Moreover, under process variation, the 3D FIFO has reduced robustness compared to the 2D FIFO. The maximum robustness is observed when the 2D FIFO is placed in the reading core.

4. Effect of CDM-ESD in 3D ICSs [3]: The charged device model electrostatic discharge (CDM-ESD) events in a die stacking process of 3D-ICs is studied. The CDM-ESD protection circuits for individual TSVs to prevent high voltage stress on transistor connected to TSV is investigated. The models for power, area, delay, and signal integrity of TSVs considering ESD protection are developed. The models are used to drive a methodology to design reliable 3D-ICs considering CDM-ESD while minimizing the overheads. The impact of ESD protection on the throughput and power-efficiency of the die-to-die asynchronous interface circuit is studied. It is shown that consideration of the ESD reduces the power-efficiency of 3D ICs. Moreover, as the TSV diameters are reduced with technology scaling, the CDM-ESD can play more significant role in the system performance.

Keywords: 3D IC, Post-silicon tuning, Signal Integrity, Variation, Ultra low power (ULP)

INDUSTRY INTERACTIONS

Texas Instruments, Intel, AMD, IBM

MAJOR PAPERS/PATENTS

[1] T. Song, et al, “Full-Chip Multiple TSV-to-TSV Coupling Extraction and Optimization in 3D ICs,” DAC 2013.

[2] Y. Peng, et al, "Fast and Accurate Full-chip Extraction and Optimization of TSV-to-Wire Coupling", DAC 2014.

[3] D. Kim, et. al., “On the Design of Reliable 3D-ICs Considering Charged Device Model ESD Events During Die Stacking,” DAC 2014.

TASK 1836.077: STATISTICAL CHARACTERIZATION OF CIRCUIT AGING

CHRIS H. KIM, UNIVERSITY OF MINNESOTA, CHRISKIM@UMN.EDU

SIGNIFICANCE AND OBJECTIVES

RTN Monitor: The impact of random telegraph noise on ring oscillator (ROSC) frequency was measured for the first time using an on-chip beat frequency detection system [1]. **PBTI Monitor:** We demonstrated a PBTI/NBTI odometer which supports a realistic recovery bias, sub-µs measurement time, sub-ps resolution, and eliminates the impact of the additional switches on the stress data [2].

TECHNICAL APPROACH

RTN Monitor: A beat frequency detection based RTN monitoring scheme achieves a high frequency measurement resolution (>0.01%) at a short sampling time (>1µs) allowing efficient collection of RTN induced frequency shifts. **PBTI Monitor:** In order to separately stress the NMOS and PMOS transistors and collect high quality PBTI and NBTI data, we utilize two sets of tri-state drivers and switches between the gate and source of PMOS and NMOS in each inverter stage.

SUMMARY OF RESULTS

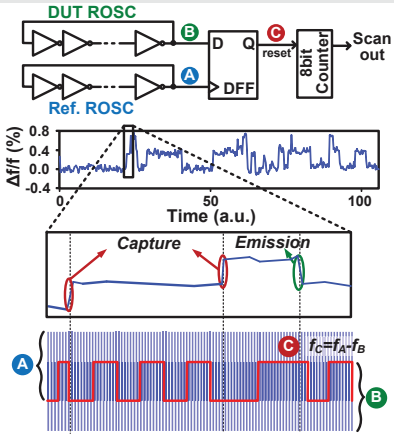


Figure 1: Beat frequency technique proposed for RTN measurements. A high frequency shift resolution (>0.01%) and a short (>1µs) measurement time can be achieved [1].

RTN Monitor: The basic concept of the beat frequency detection odometer technique for measuring the frequency difference between two ROSCs is illustrated in Fig. 1 [1]. The odometer samples the output of one oscillator using a D flip-flop at intervals set by the output of the other. This interval (= beat frequency period) is measured by counting the number of reference ROSC periods during a single beat period. This information is then read out through a scan based interface. The beat frequency approach enables us to measure changes in transistor switching times as small as one part in 10,000 in less than a microsecond, making it ideally suited for characterizing RTN effects. The frequency shift waveforms in Fig. 2 are from three different ROSCs in the test array. RTN's signature trapping/de-trapping behavior can be clearly observed. **PBTI Monitor:** A test chip was implemented in a 32nm high-k metal-gate process (Fig. 3). PBTI and NBTI induced frequency shifts under DC stress closely follow a power law dependency. The stronger recovery under a realistic AC stress can also be seen in the DC to realistic AC stress frequency shift ratio in Fig. 3 (right). The measured ratio for PBTI and NBTI were 3.2X and 18X, respectively.

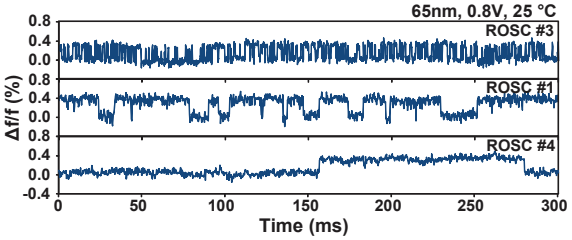


Figure 2: RTN waveforms measured using ROSC array based monitor [1].

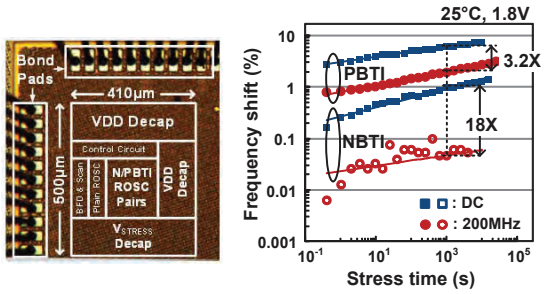


Figure 3: Testchip die photo and chip feature summary. The chip was implemented in a 32nm HKMG process [2].

Keywords: RTN, NBTI, PBTI, odometer circuit, recovery, on-chip reliability monitor, circuit aging

INDUSTRY INTERACTIONS

Monthly teleconference with TI
PI visits and internships: Intel, Global Foundries, TI

MAJOR PAPERS/PATENTS

[1] Q. Tang, et al., "RTN Induced Frequency Shift Measurements Using a Ring Oscillator Based Circuit," VLSI Technology Symposium 2013 (nominated for best student paper award).

[2] X. Wang, et al., "Fast Characterization of PBTI and NBTI Induced Frequency Shifts under a Realistic Recovery Bias Using a Ring Oscillator Based Circuit," IRPS 2014.

[3] W. Choi, et al., "An Array-Based Circuit for Characterizing Latent Plasma-Induced Damage," IRPS 2013.

TASK 1836.078: HIGH-RESOLUTION, CHARGE-BASED A/D CONVERTERS FOR NANO-CMOS TECHNOLOGIES

BORIS MURMANN, STANFORD UNIVERSITY, MURMANN@STANFORD.EDU

SIGNIFICANCE AND OBJECTIVES

The successive approximation register (SAR) ADC architecture is attractive for integration in aggressively scaled CMOS, primarily since it does not rely on linear amplification blocks. This project aims to push the performance of SAR ADCs, targeting both high resolution (~12bits) and high speed (>150MHz) in 65nm CMOS technology together with being suitable for SoC integration.

TECHNICAL APPROACH

Aggressive scaling of unit capacitances in a SAR ADC allows the designer to set the input capacitance according to the thermal noise limit, resulting in lower switching energy and faster conversion speed. As a first step, we investigated the matching limit of small metal fringe capacitors and fabricated a test structure to measure their mismatch characteristics. Next, we designed an 8 bit SAR ADC employing top plate sampling, SAR loop delay optimization and asynchronous timing. Finally, we designed a pipelined-SAR ADC to meet our design target of 12 bit resolution at over 150 MS/s. The ADC employs two capacitive DACs in the frontend to separate high-speed SAR operation from low noise residue generation, which significantly improves the conversion speed while maintaining low energy operation.

SUMMARY OF RESULTS

Fig. 1 shows the measured mismatch characteristics of small metal fringe caps across 8 chips (36 test structures measured, each for 0.45 fF and 1.2 fF unit capacitance per chip) and the calculated average sample coefficient of variation (σ/μ) is 1.2% for 0.45 fF, and 0.8% for 1.2 fF unit capacitors (in accordance with $\sigma^2 \sim 1/\text{Area}$).

Fig. 2 (a) summarizes the measurement results of the 8 bit SAR ADC obtained at f_s = 450 MHz. The measured SNDR is nearly flat with input frequency and the ADC achieves SNDR = 47.3 dB at Nyquist.

Fig. 2(b) presents the measurement results of the pipelined-SAR ADC when operating at 160 MS/s. The SNDR at low input frequency is 68.3 dB and this drops to 66.2 dB at Nyquist. The ADC consumes 11.1 mW including bias generation, references but excluding I/O. A full-scale range of 1.3 $V_{p\text{-}p,diff}$ along with a state-of-the-art FOM_S $(SNDR + 10 \times \log_{10}(P/BW))$ of 164.7 dB (at Nyquist) makes this design suitable for SoC integration.

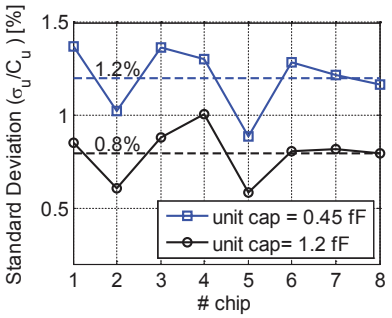


Figure 1: Mismatch characteristics measured across 8 dies.

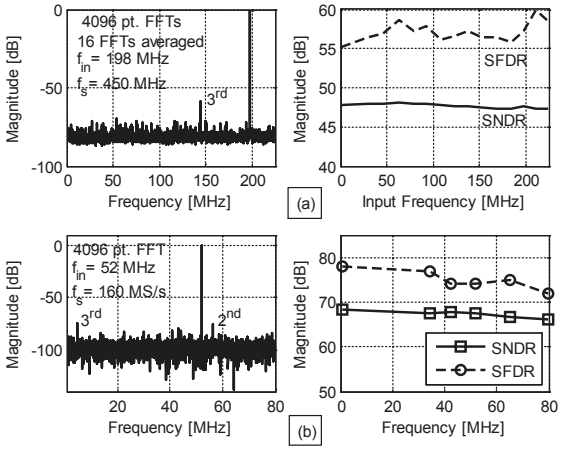


Figure 2: Measurement results of 8 bit SAR ADC (a) and pipelined-SAR ADC (b).

Keywords: Capacitor matching, CMOS, Successive approximation, ADC

INDUSTRY INTERACTIONS

Texas Instruments, Intel, Freescale

MAJOR PAPERS/PATENTS

[1] V. Tripathi and B. Murmann, "An 8-bit 450-MS/s Single-Bit/Cycle SAR ADC in 65-nm CMOS," Proc. ESSCIRC, Bucharest, Romania, Sep. 2013, pp. 117-120.

[2] V. Tripathi and B. Murmann, "Mismatch Characterization of Small Metal Fringe Capacitors," Proc. CICC, San Jose, CA, Sep. 2013.

[3] V. Tripathi and B. Murmann, "Mismatch Characterization of Small Metal Fringe Capacitors," to appear, IEEE Trans. Circuits Syst. I.

[4] V. Tripathi and B. Murmann, "A 160 MS/s, 11.1 mW, Single-Channel Pipelined SAR ADC with 68.3 dB SNDR," to appear at CICC 2014.

TASK 1836.080: VARIATION-TOLERANT NOISE-SHAPING ADCS WITH EMBEDDED DIGITAL BIAS AND VDD SCALABLE FOR NANOSCALE CMOS

PETER KINGET, COLUMBIA UNIVERSITY, KINGET@EE.COLUMIBA.EDU

SIGNIFICANCE AND OBJECTIVES

We focus on analog interfaces with flexible supplies in deep-submicron CMOS processes. We investigate digital circuit techniques in supply-scalable continuous-time sigma-delta modulators to reap the scaling benefits while handling the challenges of nano-scale short-channel devices.

TECHNICAL APPROACHES

A pulse-controlled common-mode feedback (PC CMFB) circuit is proposed to overcome the large area cost associated with a conventional RC common-mode feedback circuit for supply-scalable operations. The amplifier with the pulse-controlled common-mode feedback implemented in a low power/leakage CMOS process operates at a supply voltage from 0.6V to 1.2V.

A VCO-based amplifier with zero compensation is further proposed to replace conventional analog amplifiers. It has a huge DC gain without any significant penalties on its unity-gain bandwidth or area. A 4th-order 40-MHz active-UGB-RC filter implemented with the VCO-based amplifier offers a wide bandwidth, superior linearity and small area.

SUMMARY OF RESULTS

The circuit implementation and die photo of a fully-differential amplifier with PC CMFB are shown as Fig. 1.

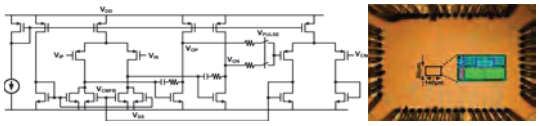


Figure 1: Circuit and die photo of the amplifier

Table 1: Performance summary of the amplifier with PC CMFB

Technology	65nm CMOS		
V_{THN}/V_{THP}	0.36V/-0.44V		
Active Area	0.01mm^2		
Supply Voltage	0.6V	0.9V	1.2V
Common-mode Voltage	0.3V	0.45V	0.6V
Power Consumption	1.21mW	1.94mW	3.07mW
Output Noise PSD (nV/Hz$^{0.5}$)	21.5	26.1	30.3
Maximum Input Signal for 1% THD	-2.3dBm	3.8dBm	6.1dBm

The amplifier performance summarized in Table 1 demonstrates that the PC CMFB has a small area and is suitable for flexible supply operation.

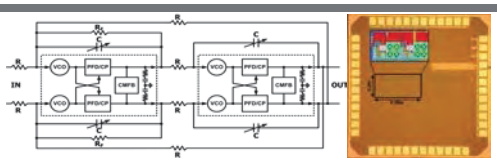


Figure 2: Architecture and die photo of the filter.

The architecture and die photo of the filter using VCO-based amplifiers with zero compensation are shown in Fig. 2. The performance comparison of the filter is summarized in Table 2 demonstrating that the active-UGB-RC filter offers a wide bandwidth and has superior linearity than filters using conventional amplifiers or ring-oscillator integrators. The filter has a small area and a competitive figure of merit particularly when considering the contribution of area.

Table 2: Performance comparison of the filter

	[1]	[2]	[4]	[5]	[6]	This work
Supply Voltage	0.55V	1.2V	1.0V	1.0V	1.5V	1.2V
Topology	Gm-C	Active-UGB-RC	Active-RC	Active-RC	Active-RC	Active-UGB-RC
BW (MHz)	7	11	10	20	19.7	40
Order	4	4	5	5	5	4
Noise (nV/Hz$^{0.5}$)	23.6	11	143	52	30	96
Out-of-band IIP3	-	-	-	8dBm	-	22.5dBm
In-band IIP3	8.7dBm	21dBm	21.3dBm	26dBm	18.3dBm	27.3dBm
Power (mW)	2.9	14.2	4.6	7.5	11.25	7.8
Area (mm^2)	0.29	0.9	0.25	1.53	0.2	0.07
Technology	90nm	130nm	120nm	130nm	130nm	55nm
FoM (fJ×mm^2)	0.15	0.099	0.22	0.23	0.068	0.02

Keywords: VCO-based amplifier, digital circuit technique, supply-scalable amplifier, pulse-controlled common-mode feedback, continuous-time sigma delta modulator

INDUSTRY INTERACTIONS

Texas Instruments and Freescale Semiconductor

MAJOR PAPERS/PATENTS

[1] Chun-Wei Hsu and Peter R. Kinget, "A Supply-Scalable Differential Amplifier with Pulse-Controlled Common-Mode Feedback," IEEE Custom Integrated Circuits Conference (CICC), Sep. 2014

[2] Chun-Wei Hsu and Peter R. Kinget, "A 40MHz 4th-order Active-UGB-RC Filter Using VCO-Based Amplifiers with Zero Compensation," IEEE European Solid-State Circuits Conference (ESSCIRC), Sep. 2014.

TASK 1836.086: VARIATION TOLERANT CALIBRATION CIRCUITS FOR HIGH PERFORMANCE I/O

ALYSSA APSEL, CORNELL UNIVERSITY, ABA25@CORNELL.EDU

SIGNIFICANCE AND OBJECTIVES

Process variation degrades operation of analog subsystems and high performance I/O. While sources of process variation are well understood, methods to combat its effects are ad-hoc with power and area costs. This project explores circuit techniques to improve calibration of high performance I/O blocks at a reduced cost.

TECHNICAL APPROACH

The first focus of this project is I-mode calibration DAC's with improved linearity. Two methods are demonstrated: adding redundant cells to reduce DNL and "ordered" cell selection to reduce INL. Low variation monitor circuits to measure and sort currents and a smaller second generation DAC cell are also developed. Finally, theoretical expressions are derived from ordered statistics to characterize each approach.

The second focus of this project is PI monitors. A novel time to digital converter using a stochastic source is explored. We have applied this technique to the development of a novel integrated jitter detection circuit.

SUMMARY OF RESULTS

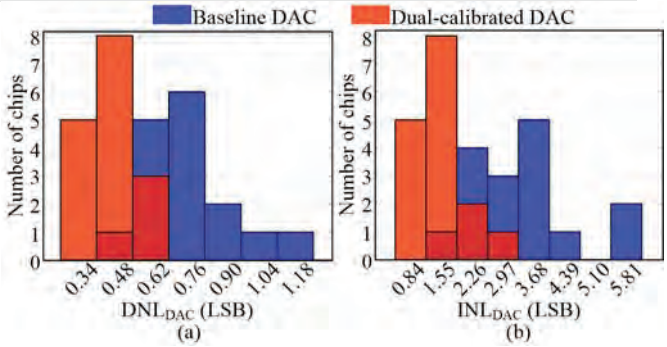


Figure 1a:. Histograms of measured (a) DNLDAC and (b) INLDAC for 8-bit current steering thermometer DAC.

A final 8 bit thermometer DAC was designed and tested to demonstrate the concepts of redundancy and reordering. The DAC cell contains an embedded memory cell to store a configuration bit, indicating if the current source in the cell is an "outlier" to be eliminated. An addressing scheme and decoder allow elimination of 2 cells per row. All measurement of currents in each cell and sorting is done on chip. Measured results for a set of DAC's in a 65nm CMOS process indicate a baseline current variation of 18% and an improvement of 36% in DNL and 50% in INL from measurement of 16 chips over the baseline DAC using the two techniques. Results are shown in Fig. 1a.

The final DAC was redesigned to reduce area overhead and include measurement and sorting circuits. Cell redesign reduces the total area by ~85%. However, there is still a 3X area overhead required to store the configuration bit and enable addressing and sorting. This area could be used for a larger current source with lower variation. Simulation shows that 40% improvement is still achieved considering equal area.

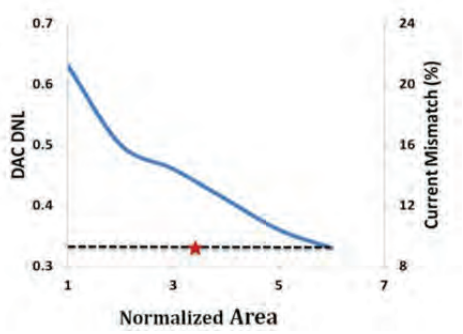


Figure 1b: DAC DNL for various sizes of PMOS I-source. The star indicates area of new DAC with two bits of redundancy per row

New theory has been developed to characterize the effect of redundancy and reordering on INL and DNL. Variances for the redundant DAC are calculated based on a truncated probability distribution and include the effects of row-wise sorting and selection. Reordering is characterized using ordered statistics.

Work also continues on a novel PI monitor circuit based on a stochastic time-to-digital conversion technique. Circuits have been taped out in 65nm CMOS to demonstrate this technique applied to accurate all digital jitter measurement.

Keywords: Variation, DAC, INL, DNL, Phase Interpolator

INDUSTRY INTERACTIONS

Intel, IBM

MAJOR PAPERS/PATENTS

[1] I. Mukhopadhyay, M. Mukadam, R. Narayanan, F. O'Mahony, and A. B. Apsel, "Dual-calibration Technique for Improving Static Linearity of Thermometer DACs," submitted TCAS-I.

TASK 1836.087: A HIGH-SPEED LOW-POWER CLOCK DATA RECOVERY (CDR)

PING GUI, SOUTHERN METHODIST UNIVERSITY, PGUI@SMU.EDU

SIGNIFICANCE AND OBJECTIVES

We propose a low-voltage low-power 28Gb/s serial link receiver in 65nm CMOS technology. Novel circuit techniques are proposed to enable the receiver to operate under 0.6V (nominal supply voltage of 1.1V) for low power consumption with a power efficiency of <2mW/Gb/s.

TECHNICAL APPROACH

Novel circuit techniques are proposed to enable low-voltage and low-power operation of a 28Gb/s serial link receiver. At the center of the receiver is a low-phase-noise VCO employing transformer-feedback technique to achieve large signal swing under Vdd of 0.6V. Capacitive source degeneration is proposed in the secondary coil of the VCO to improve the phase noise. Gate-biasing techniques are utilized in the varactors and capacitor array to ensure wide tuning range of the VCO. Forward-body-biasing technique is proposed in the bang-bang phase detector to achieve a larger signal swing under Vdd=0.6V for low BER.

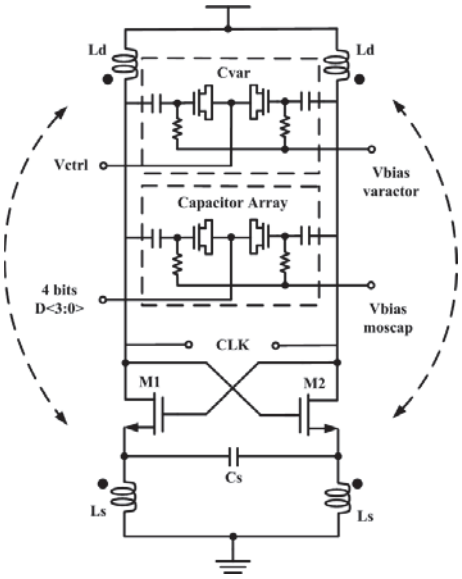


Figure 1: Proposed low-phase-noise Transformer-feedback-based VCO

SUMMARY OF RESULTS

We implemented a 28Gb/s serial link receiver using 65nm CMOS with the proposed circuit techniques so that the entire receiver can be operated at Vdd=0.6 V for low power operation and for compatibility with digital circuitry with decreasing Vdd. The entire receiver including the CTLE equalizer consumes 55mW at 28Gbps, achieving a power efficiency of <2mW/Gb/s.

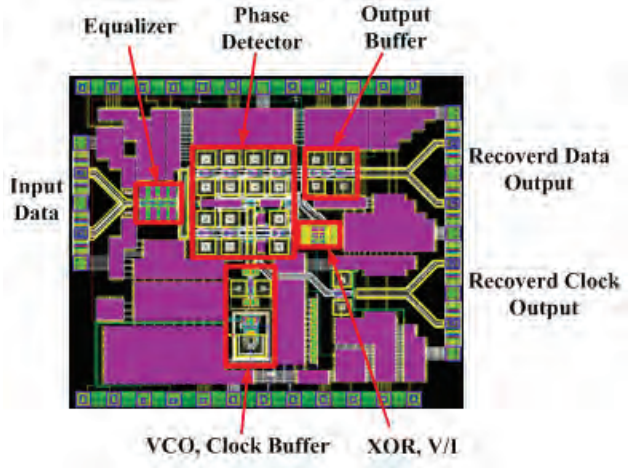


Figure 2: Layout of the 28Gb/s serial link receiver

Table 1: Performance Summary

Data Rate	27.14 Gb/s - 29.42 Gb/s (8.2%)
Supply Voltage Vdd	0.6V (Nominal 1.2V)
Power Consumption	55mW
Recovered Clock Jitter	1.8ps (pp)
Recovered Data Jitter	2.4ps (pp)
Area	0.6 x 0.65 (mm^2)
Technology	65nm CMOS

Keywords: Clock Data Recovery (CDR), Low voltage, low power, serial link receiver

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] G. Wu, et al., "A 1-16 Gb/s All Digital Clock and Data Recovery with a Wideband, High-Linearity Phase Interpolator," SRC TECHON 2014

[2] S. Gui, et al., "A Low-Voltage Low-Power 28 Gb/s Serial-Link Receiver in 65nm CMOS," SRC TECHON 2014.

[3] T. Xi, et al.," Low-Phase-Noise 54GHz Quadrature VCO and 76GHz/90GHz VCOs in 65nm CMOS," IEEE RFIC 2014

TASK 1836.093: VARIABILITY-AWARE, DISCRETE OPTIMIZATION FOR ANALOG CIRCUITS

JAEHA KIM, SEOUL NATIONAL UNIVERSITY, KOREA, JAEHA@SNU.AC.KR

SIGNIFICANCE AND OBJECTIVES

While analog circuit optimizers, that can automatically size transistors in a circuit according to a prescribed performance metric, can be an effective productivity tool for analog, yet the reality is that their adoption into the mainstream flows has been rather slow. Exploiting the inherent uncertainty in IC processes, this task aims to explore the use of discrete optimization techniques for realizing a fast, deterministic optimizer that can perform quick, incremental 'what-if' analysis.

TECHNICAL APPROACH

While analog design parameters are typically of continuous values, we assert that such a continuous design space can be effectively covered with a set of finite, coarsely-spaced, discrete points by exploiting the inherent variability in the IC technology. Our expectation is that a discrete optimizer can solve many of the problems faced with the existing, continuous optimizers for analog circuits.

However, since one weakness of a discrete optimization approach is its poor scaling with the problem dimensionality, various approaches have been investigated, including a predictive global search algorithm and a hierarchical optimization approach based on Pareto-front extraction.

SUMMARY OF RESULTS

Previously, we have proposed three novel algorithms to leverage a discrete optimization technique while mitigating its limitation in dimensionality scaling [2]: an isotropic discretization scheme, a stochastic hill-climbing algorithm, and an incremental Monte Carlo simulation algorithm. We have demonstrated that these algorithms are effective in finding the optimal design [2] as well as exploring the design trade-offs such as yield-aware Pareto fronts [3].

This year, we have investigated the use of a predictive global search algorithm in the discretized design space. [1],[4] The optimizer starts with a set of randomly chosen pilot samples and builds a yield-aware response-surface model to predict the outcome of the unexplored design candidates. Then, it evaluates the most promising candidates to provide the better outcome and updates the response surface model. The process continues until the probability of finding the better outcome drops below a certain threshold. The key advantage of this approach is that 1) the discretized design space provides a notion of coverage, as the number of design candidates within any given area is finite, and 2) the optimizer finds the optimum solution fairly early in the process, rather than reaching it at the very last step, enabling quick interactions with the designers (Fig. 1).

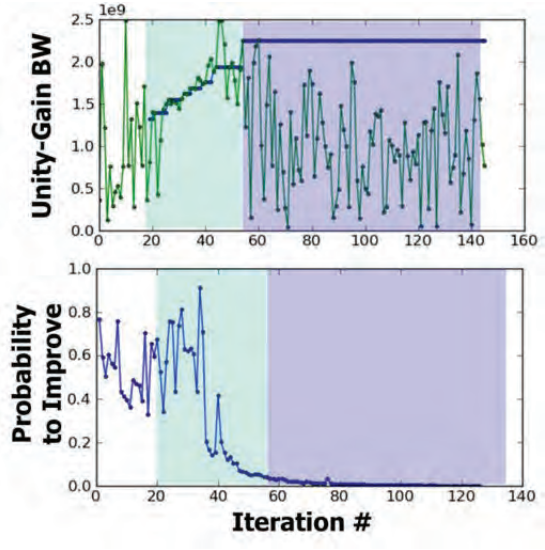


Figure 1: The search process of the predictive global circuit optimizer, demonstrating the early discovery of the optimum point and comprehensive coverage of the design space.

Keywords: analog circuit synthesis, circuit optimization, discrete optimization, predictive global optimization.

INDUSTRY INTERACTIONS

Texas Instruments, Inc. and Intel Corp.

MAJOR PAPERS/PATENTS

[1] J. Lee and J. Kim, "Predictive Global Optimization Method for Analog Circuit with Response Surface Methodology on Discrete Design Space," Frontiers in Analog CAD, 2014.

[2] S. Jung, J. Lee, and J. Kim, "Variability-Aware, Discrete Optimization for Analog Circuits," Trans. on Computer-Aided Design, 2014.

[3] S. Jung, J. Lee, and J. Kim, "Yield-Aware Pareto-Front Extraction for Discrete, Hierarchical Optimization of Analog Circuits," Trans. on Computer-Aided Design, 2014.

[4] J. Kim, et al., "Discretization and Discrimination Methods for Design, Verification, and Testing of Analog/Mixed-Signal Circuits," Custom Integrated Circuits Conf., 2013.

TASK 1836.95: TEST GENERATION FOR MIXED-SIGNAL DESIGN VERIFICATION AND POST-SILICON DEBUGGING

RICHARD SHI, UNIVERSITY OF WAHSINGTON, CJSHI@UW.EDU

SIGNIFICANCE AND OBJECTIVES

Mixed-signal design, verification, and debugging critically depend on running circuit simulation. Current research efforts have resulted in progress exclusively on advanced simulation algorithms. This project aims at developing theory, techniques, and tools for generating test benches and vectors used to drive circuit simulation for mixed-signal design verification and post-silicon debugging.

TECHNICAL APPROACH

The research is directed to solve the following two problems: (1) generation of minimal-length verification tests that can sensitize the worst-case errors in analog blocks embedded in complex mixed-signal integrated circuits, and (2) generation of the shortest debugging simulation test benches and stimulus sequences that can isolate the errors that cause mixed-signal chip failures in post-silicon design debugging. The work is built on systematic behavioral modeling and analog controllability, observability and reachability analysis. Leading-edge design cases are developed to drive the methodology and tool research.

SUMMARY OF RESULTS

We have designed three test cases: (1) an RF-front end (300MHz to 40GHz) using IBM's 9HP process (180nm SiGe/90nm CMOS), taped out on Dec 2013, (2) a mixed-signal SerDes block in IBM's 14nm FinFET, taped out on March 2014, and (3) a 11-bit 50MS/s SAR-ADC in 14nm FinFET, taped out on Oct 2014.

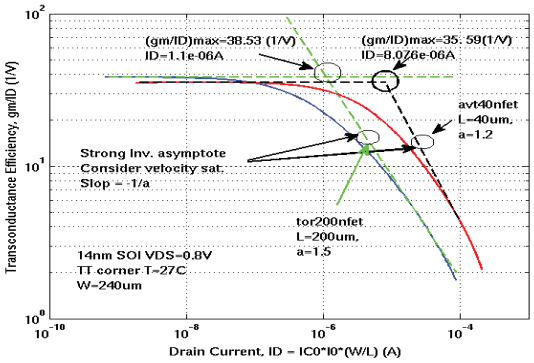


Figure 1: Calculation of technology current I_0 from intersection of $g_{m^\alpha}/I_{Dsat^\alpha}$ with the tangent of slope=$-1/\alpha$ for two FINFET analog devices with FIN length of 40nm and 200nm.

A methodology for characterization of analog performance parameters in terms of inversion coefficient and technology current was developed and demonstated in 14nm FinFET analog building block design [2]. The proposed methodology consists of the following steps:

(1) Characterization of technology current
(2) (Performance Map) Characterization of analog performance parameters, including transconductance efficiency, instrisic gain, gain-bandwidh product, flicker noise, current mismatch in terms of the inversion coefficient, the number of Fins (transistor W), and the Fin length (L)
(3) (Variability Map) Charaterization of variability of analog performance parameters due to process, voltage and temperature variations
(4) (Controlabilty Map): Characterization of controlability of analog performance paramters in terms of controllable deisgn paramters: inversion coefficient, number of Fins (W) and Fin length (L)

Analog reachability analysis bas been employed for mixed-signal functional verification and debugging. We applied the Rapidly Exploring Random Tree (RRT) algorithm in analog test generation[1]. The objective is to find an input stimuli u(t) that guides the system trajectory into a user defined region in the state space. The novelty of our approach lies in effective sample biasing enabled by efficient reachability estimation.

Keywords: Analog Observability, Analog Test Generation, Behavioral Modeling, Verification

INDUSTRY INTERACTIONS

Texas Instruments Inc., Intel and IBM

MAJOR PAPERS/PATENTS

[1] C. Li and C-J Shi, "Towards Test Generation of Mixed-Signal Circuit Using Reachability Analysis," SRC-TechCon, Sept 2014.

[2] A. Wang, V. Dhawan, C-J. Shi, "Analog Building Block Design in 14nm FinFET Using Inversion Coefficient," IEEE SOI/3D-Subreshold United Technology Conference, Oct 2014.

TASK 1836.096: MIXED-SIGNAL DESIGN CENTERING IN DEEPLY-SCALED TECHNOLOGIES

BOROVOJE NIKOLIĆ, UC BERKELEY, BORA@EECS.BERKELEY.EDU

SIGNIFICANCE AND OBJECTIVES

A design methodology for robust design of high-performance analog circuit blocks in highly-scaled technologies is being investigated, that will enable rapid yield ramp-up in scaled technologies.

TECHNICAL APPROACH

We are developing a methodology that enables centering with respect to technology variability of high-performance mixed-signal signal designs in as few as one design iteration. It is based on the components, which are developed simultaneously:

1) Instrumenting critical design components to accurately monitor impact of process variability on their performance.
2) Creating a dedicated set of representative circuit primitives for their full variability characterization.
3) Extracting a variability model from the test structures; building simplified Spice models to predict the distribution spread of critical components.

These components enable centering of critical analog blocks, such as clock and data recovery loops and high-performance data converters.

SUMMARY OF RESULTS

We have developed an algorithm based on backward propagation of variability to improve yield prediction capability of existent models. The algorithm uses the equation below, where e_i is the measurement data and p_j the parameter values, to update the parameter variation values, including parameter correlations in the model.

$$\sigma^2_{\Delta e_k} = \sum_{k=1}^{n} \left(\frac{\partial e_i}{\partial p_k} \right)^2 \sigma^2_{\Delta p_k} + 2 \sum_{(u,v)} \frac{\partial e_i}{\partial p_u} \frac{\partial e_i}{\partial p_v} \mathrm{cov}(\Delta p_u, \Delta p_v)$$

This underdetermined system is solved using a constrained LMS method to limit the solution space. Fig. 1 shows the results of this method (red) compared against MC simulation results (blue).

This algorithm is applied to data extracted from representative test structures and building blocks to hierarchically capture variability and propagate distributions from devices, via components to systems.

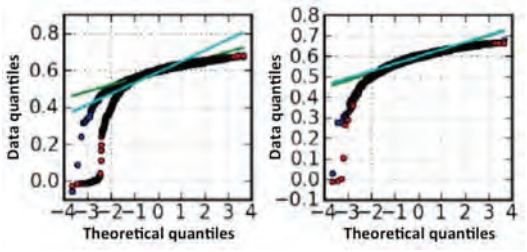


Figure 1: Simulated QQ plots of the V_{TH} distribution using the conventional minimum norm (left) and the constrained LMS solution (right).

The measurement data for the above algorithm are extracted from representative test structures and building blocks to hierarchically capture variability tied to a specific target design. To illustrate this approach we are designing test structures to center comparators, which are key components of mixed-signal systems such as clock-and-data recovery loops. These structures target at characterizing offset and impulse sensitivity functions, which are then related to variability measured by I-V data of individual devices.

A set of transistor variability characterization structures with gate lengths of 22nm in fully-depleted SOI technology has been received from fabrication and is under test (Fig. 2).

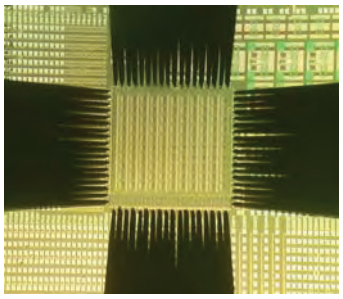


Figure 2: 22nm test chip viewed though a microscope.

A new test chip in 14nm FinFET technology is being designed, containing characterization structures for both I-V curves and comparators.

Keywords: CMOS, variability, yield, design optimization, clock and data recovery.

INDUSTRY INTERACTIONS

Intel.

TASK 1836.097: DUAL-DOMAIN SAR ADCS INCORPORATING BOTH VOLTAGE AND TIME INFORMATION

UN-KU MOON, OREGON STATE UNIVERSITY, MOON@EECS.OREGONSTATE.EDU

SIGNIFICANCE AND OBJECTIVES

Traditional SAR ADCs operate with one or more binary quantizers in the voltage domain to dictate DAC switching operations. The purpose of this research is to improve the efficiency and resolution achievable by utilizing statistical information in both the voltage and time domains.

TECHNICAL APPROACH

The TSAR [1] and FITSAR structures are based on traditional SAR techniques, coupled with analyzing the propagation delay of a latched comparator to create an optimized switching algorithm, half bit redundancy, and speed enhancements. Time and voltage information are examined to provide polarity and magnitude information of the input. The described techniques are implemented in prototype ICs.

A background blind calibration technique [2] was developed to further improve ADC performance. By downsampling the input signal and applying the orthogonality characteristic of sinusoids, unwanted harmonic distortion is extracted to obtain a higher overall signal to noise distortion ratio (SNDR).

SUMMARY OF RESULTS

The Feedback Initialized TSAR (FITSAR) improves upon TSAR [1] energy savings by driving the DAC with both a coarse binary SAR and a fine TSAR. This segmentation allows the early stages to use a quantizer designed for energy efficiency, and the mid to late stages to use a quantizer with improved accuracy. Due to the described changes, the energy used per code conversion and number of capacitors switched per conversion is reduced by 61% and 34% respectively over the TSAR structure and is lower for every code. Additionally the use of a coarse SAR nested in the TSAR loop and use of embedded EMCS coarse stage reduce overall comparator energy by 45%. The fabricated prototype in 0.13um CMOS achieves a FOM of 15.4 fJ/CS at 8 MHz and 9b accuracy.

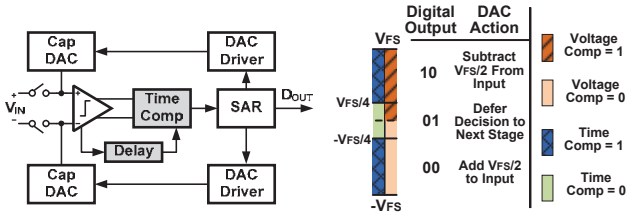


Figure 1: The Ternary SAR (TSAR) structure and stage output

The calibration technique is implemented by combining the properties of downsampling and orthogonality of sinusoid waves. By taking the running average of the product of two digital bit streams D_{out} and downsampled output, a DC component emerges with magnitude proportional to the nonlinearity coefficient. As shown in Figure 2, the calibration algorithm can be made to operate in the background by using two identical ADCs and applying input V_{in} to one ADC and a scaled verison of V_{in} to the other ADC. By doing so, the harmonic distortion components can be extracted since the input is scaled by a linear factor whereas the nonlinear distortion is scaled by a different factor.

As a proof of concept, a highly nonlinear VCO based ADC was fabricated in 0.13um CMOS with power consumption of 1.65mW. Through calibration, the SNDR is improved from 26dB to 65dB.

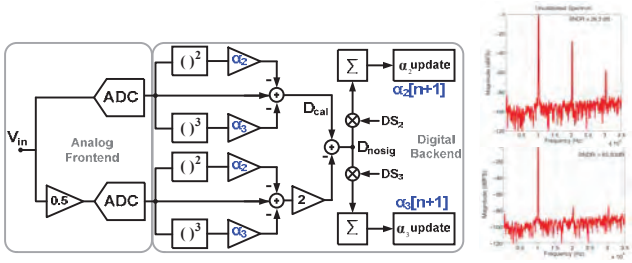


Figure 2: Blind Calibration structure and output spectrums before and after calibration

Table 1: Performance Summary

	VDD	ENOB	BW	Power	Area
FITSAR	0.8 V	8.89 b	8 MHz	58 uW	0.06mm^2

Keywords: Ternary SAR, time comparator, SAR energy, SAR ADC, Blind Calibration

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] J. Guerber, H. Venkatram, M. Gande, A. Waters, and U. Moon, “A 10b Ternary SAR ADC with Quantization Time Information Utilization,” IEEE J. Solid-State Circuits, vol. 47, no. 11, pp. 1900-1910, Nov. 2012.

[2] M. Gande, H. Venkatram, H. Lee, J. Guerber, and U. Moon, "Blind Calibration Algorithm for Nonlinearity Correction Based on Selective Sampling," IEEE J. Solid-State Circuits, vol. 49, no. 8, pp. 1715-1724, Aug. 2014.

TASK 1836.107: VERIFICATION OF MULTI-STATE VULNERABLE AMS CIRCUITS

RANDY GEIGER, IOWA STATE UNIVERSITY, RLGEIGER@IASTATE.EDU
DEGANG CHEN, IOWA STATE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

The objective is to develop a systematic procedure that detects presence or absence of multiple equilibrium points in basic AMS circuits that can be used to verify that a circuit is void of Trojan operating states. This will prevent fabrication of circuits that fail when they enter a Trojan state.

TECHNICAL APPROACH

A mapping of a netlist description of the resistive representation of an AMS circuit to a graphical representation that preserves feedback loops will be developed, Existing graphical analysis methods will be used to identify positive feedback loops to determine if the circuit is vulnerable to the existence of multiple stable equilibrium points. A loop-breaking algorithm will be developed to identify break points for a circuit-level homotopy analysis that can be used to determine the presence or absence of Trojan Operating States, computationally efficient algorithms will be developed for doing the homotopy analysis.

SUMMARY OF RESULTS

A mapping of the netlist description of a basic AMS circuit to a graphical representation of the resistive representation of the circuit that uses Directed Dependency Graphs (DDG) has been developed. From the DDG, the Strongly Connected Components (SCC) are identified using standard graphical analysis techniques. From the SCCs, the positive feedback loops are identified. Again using standard graphical analysis methods, a set of minimal break points is identified that will guarantee that all positive feedback loops (PFLs) are broken. After break points are identified, an inverse mapping from the SCC back to a circuit that includes the sources needed for doing a homotopy analysis is made. Circuit-level homotopy methods are then adapted to determine the presence or absence of undesired (Trojan) operating points. Computationally efficient algorithms have been developed using a “branch-and-bound” approach for conducting the homotopy analysis, which are essential for circuits that have two or more tightly coupled positive feedback loops.

The process of mapping a circuit schematic to a graphical representation that can be used to identify break points in the positive feedback loops is described in the flow-chart shown in Fig. 1. The use of circuit-level homotopy methods to determine the presence or absence of multiple stable equilibrium points is shown in Fig. 2.

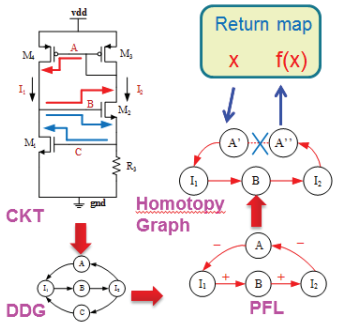


Figure 1: Flow Chart Showing Identification and Breaking of Positive Feedback Loops in AMS Circuit.

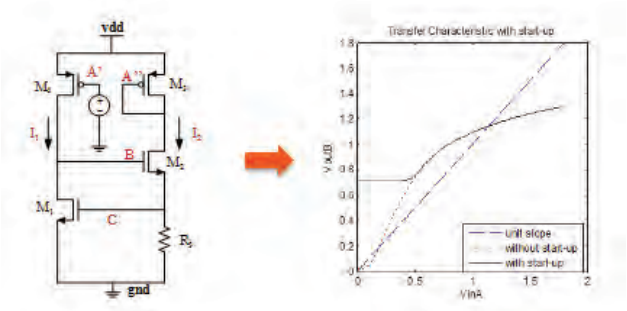


Figure 2: Use of Circuit-Level Homotopy Methods to Determine Stable Operating Points from Return Map with Basic Circuit Simulator

This approach has been applied to several well-known AMS circuits that have a single PFL and some circuits with two PFLs.

Keywords: Start-up Circuits, Equilibrium points, Trojan States, Verification

INDUSTRY INTERACTIONS

Texas Instruments, Intel, AMD

MAJOR PAPERS/PATENTS

[1] Y-T Wang, et al., "Practical Methods for Verifying Removal of Trojan Stable Operating Points,” ISCAS, May 2013, Beijing.

[2] Z. Liu, et al., “Auto-Identification of Positive Feedback Loops in Multi-state Vulnerable Circuits,” VTS, April 2014.

[3] Z. Liu, et al.,”Identification and Breaking of Positive Feedback Loops in Trojan States Vulnerable Circuits, ISCAS, May 2014.

TASK 1836.109: NEW PARADIGMS FOR HIGH-PERFORMANCE AMPLIFICATION

UN-KU MOON, OREGON STATE UNIVERSITY, MOON@EECS.OREGONSTATE.EDU

SIGNIFICANCE AND OBJECTIVES

Amplifiers are becoming more difficult to design in the context of nanoscale CMOS. This has created a drive to achieve new levels of performance in SoCs. The objective is to achieve new levels of performance using architectures that are immune to performance degradation due to scaling.

TECHNICAL APPROACH

The previous realizations of ring amplifiers were composed of two separate fine and coarse paths. Shown in Fig. 1. By combining the first stage of the two paths and creating a fully differential ring amplifier, both power and area are saved. To further reduce power consumption, a new method of generating voltage dead zones is proposed. Shown in Fig. 2, a dead zone voltage is created using a resistor instead of capacitors [Y. Lim and M. P. Flynn, "A 100MSPS, 10.5-bit, 2.46mW Comparator-less Pipeline ADC Using Self-Biased Ring Amplifiers," IEEE ISSCC, Feb. 2014.]. This allows the fine path to be self-biased and no longer requires fine-tuning of the dead zone.

SUMMARY OF RESULTS

The new architecture of the ring amplifier is shown in Fig. 1. By sharing a first stage, the ring amplifier becomes fully differential and saves both area and power.

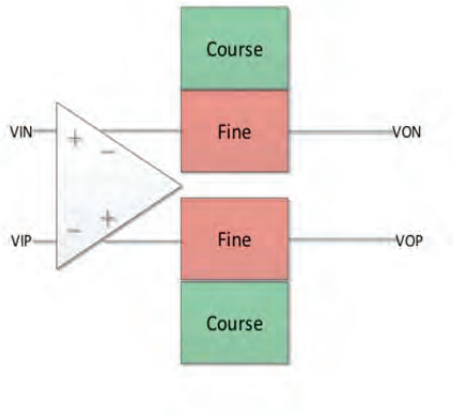


Figure 1: The architecture for reducing both power and area while increasing slew capability.

The new fine path, shown in Fig. 2, uses R_B to create to an embedded dead zone on the output transistor for improved dynamic biasing, allowing for the fine path to be more efficient and faster.

A similar/modified technique can be used in the coarse path for maximal slewing and minimal power consumption. With the combination of efficient slewing and area saving, the new design is expected to be faster while achieving better FoM.

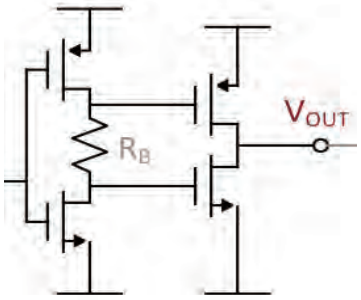


Figure 2: The fine path is shown above with a self-biasing resistor from [Yim and Flynn].

Table 1: Sample of a table caption

	Accuracy	Fs	Power	FoM
Previous Design [1]	75.9 dB	20 MSPS	2.96 mW	29fJ/Conv.
New Design	76 dB	33 MSPS	4 mW	25fJ/Conv.

Shown in the table above, the new design will run at 33 MSPS while consuming roughly one more mW. There will be no compromise in accuracy, resulting in a reduction of FoM from 29fJ/Conv. to estimated 25fJ/Conv.

Keywords: Ring Amplifier, RAMP, dead zone, coarse, fine

INDUSTRY INTERACTIONS

Texas Instruments, Freescale, Intel

MAJOR PAPERS/PATENTS

[1] B. Hershberg and U. Moon, "A 75.9dB-SNDR 2.96mW 29fJ/Conv-Step Ringamp-Only Pipelined ADC," IEEE VLSI Circ. Symp. Dig. Tech. Papers, Jun. 2013.

TASK 1836.111: ADVANCED ADC-BASED SERIAL LINK RECEIVER ARCHITECTURES

SAMUEL PALERMO, TEXAS A&M UNIVERSITY, SPALERMO@ECE.TAMU.EDU
SEBASTIAN HOYOS, TEXAS A&M UNIVERSITY, HOYOS@ECE.TAMU.EDU

SIGNIFICANCE AND OBJECTIVES

While CMOS technology scaling allows for the efficient implementation of powerful on-chip DSP algorithms for equalization and symbol detection, ADC-based receivers are generally more complex and consume higher power. The proposed ADC-based serial link techniques aim to significantly improve interconnect bandwidth density in an energy-efficient manner.

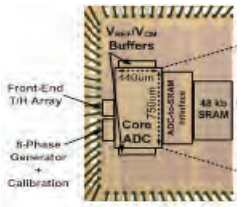
TECHNICAL APPROACH

In order to investigate design trade-offs, a novel statistical-modeling framework for advanced ADC-based serial links will be developed. This tool will be used to guide the design of a new hybrid ADC-based receiver architecture which combines in a power optimum manner equalization embedded in the ADC and dynamically power-gated digital equalization based on threshold detection, with an ultimate target data rate in excess of 25Gb/s. The statistical modeling framework and receiver prototypes will be leveraged to investigate the performance of the hybrid ADC architecture with multi-level modulation schemes (duobinary, PAM4, PAM8, etc.) and error correction coding.

SUMMARY OF RESULTS

In order to relax ADC-based receiver power and complexity trade-offs, partial equalization can be embedded inside the ADC and not be limited by the ADC resolution. To explore this, a 6b 10GS/s SAR ADC with embedded 2-tap FFE and 1-tap DFE (Fig. 1) was implemented in a GP 65nm CMOS process and achieved 4.56b ENOB at 0.48pJ/conv. [1].

While embedded equalization provides improved BER performance, additional equalization is generally required to support channels with loss >30dB. A new hybrid ADC-based receiver architecture which combines embedded ADC equalization and dynamically power-gated digital equalization based on threshold detection is proposed. In this scheme, the ADC output is considered as a reliable decision if the value exceeds a threshold, which can also serve as an indication that further equalization is necessary on a sample-by-sample basis. In the proposed receiver, any samples below the threshold are passed through the digital equalizer, while samples which exceed the threshold are treated as reliable decisions. The percentage of digital equalization power saving is set by the probability that the ADC output exceeds the threshold that corresponds to BER=10^{-12}. A 10Gb/s receiver prototype with a 6-b ADC and the digital equalizer is currently being implemented in a GP 65nm CMOS process.



(a)

TABLE I: PERFORMANCE SUMMARY

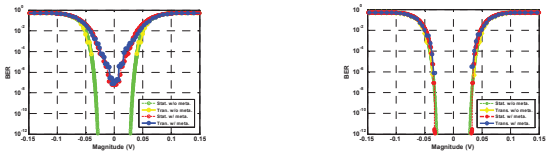
Specification	[El-Chammas 2011]	[Chen 2012]	This Work
Technology	65nm	65nm	65nm
Power Supply	1.1V	1.1V	1.1V/0.9V
ADC Structure	TI-Flash	TI-Flash	TI-SAR
Equalization	No	HPF + FFE	Embedded FFE + DFE
Sampling Rate	12 GS/s	10 GS/s	10 GS/s
Resolution	5 bits	4 bits	6 bits
ENOB @ ERBW	3.88 bits	N/A	4.03 bits
Input Range	590 mV$_{pp}$	600 mV$_{pp}$	500 mV$_{pp}$
FOM (P/2^{ENOB}.f$_s$)	0.46 pJ/c.-s.	N/A	0.48 pJ/c.-s.
Area	0.44 mm^2	0.29 mm^2	0.52 mm^2
Power	81 mW	93 mW*	79.1 mW

* This value includes the clock and analog front-end power consumption.

(b)

Figure 1: 6b 10Gb/s time-interleaved SAR ADC with embedded 2-tap FFE and 1-tap DFE: (a) GP 65nm CMOS prototype, (b) performance summary.

An ADC-based statistical modeling methodology to analyze the BER impact of ADC metastability errors was developed [2]. In order to model metastability error propagation through a digital feed-forward equalizer (FFE), a partial-bit mapping approach is proposed that generates the error probability density function (PDF) at the FFE output. BER degradation due to metastability is evaluated with the proposed statistical model for 10Gb/s NRZ signaling over a 32" backplane channel (Fig. 2) and receivers that consists of a 6-bit ADC followed by a 3-tap digital FFE.



(a) (b)

Figure 2: Transient and statistical simulation BER bathtub curves with comparator τ=16.3ps for (a) flash, (b) aSAR.

Keywords: Analog-to-digital converter, ADC-based receiver, embedded equalization, energy efficient

INDUSTRY INTERACTIONS

Freescale, Intel, Texas Instruments

MAJOR PAPERS/PATENTS

[1] E. Zhian Tabasy et al., "A 6-bit 10-GS/s TI-SAR ADC with Low-Overhead Embedded FFE/DFE Equalization for Wireline Receiver Applications," submitted to IEEE JSSC.
[2] S. Cai et al., "Statistical Modeling of Metastability in ADC-Based Serial I/O Receivers," submitted to IEEE EPEPS Conference.

TASK 1836.113: SYNTHESIZED CELL-BASED ADPLL IMPLEMENTATION FOR ACCELERATED DESIGN

DAVID WENTZLOFF, UNIVERSITY OF MICHIGAN, WENTZLOF@UMICH.EDU

SIGNIFICANCE AND OBJECTIVES

This 3-year program focuses on developing "cell-based" all-digital PLLs that can be synthesized from a cell library, implemented using existing automatic place and route (APR) tools, and then digitally calibrated. The end result will be a set of PLL architectures described in HDL which can be adapted to a wide range of performance requirements.

TECHNICAL APPROACH

All-Digital Phase-locked loops (ADPLLs) are widely used as clock generators in advanced digital systems, eliminating several of the downsides of traditional PLLs. Previous work has demonstrated that integer-N ADPLLs can be implemented using digital synthesis and automatic place-and-route (APR) tools, resulting in a simplified and easily customizable design flow. Our next goal is the development of fractional-N frequency synthesizers which leverage novel architectural and implementation improvements. These new designs will be synthesizable using standard CAD tools, and will be prototyped in a series of test chips in advanced CMOS processes.

SUMMARY OF RESULTS

We have demonstrated a dividerless, fractional-N ADPLL with its physical design synthesized using a cell-based approach by leveraging automatic place and route (APR) tools and digital design flows. The block diagram of the proposed clock generator is shown in Fig. 1. Two cascaded PLLs allow for smaller frequency multiplications, ensuring that locking can occur without the use of a divider or frequency locked loop, and providing finer granularity in fractional frequency selection.

The first PLL (PLL A) uses a 25MHz reference to produce an output at 160-210MHz. The second PLL (PLL B) takes the output of the first as its reference, producing the 900MHz output tone. Each PLL uses an identical controller, differing only in the bit width of the DCO control signals. Because there is no need for a divider or any other block to operate at the frequency of the output oscillator, no custom design is required to account for frequencies which may be outside the range of some standard cell libraries.

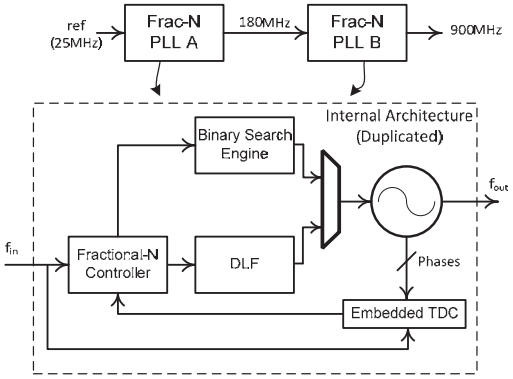


Figure 1: Block Diagram of the proposed clock generator, showing the dividerless architecture and binary search engine.

The ADPLL is fabricated in a 28nm FDSOI CMOS process and occupies 0.09mm^2. It consumes 3.0mW, with an RMS jitter of 7.1ps. The figure of merit (FOM) is -218.2 dB at a 924MHz output frequency. Performance characteristics are summarized in Table 1 and compared with other synthesized PLLs. The performance of this clock generator compares favorably with previous synthesized PLLs; however, this is the first time a fractional-N PLL has been fully synthesized without using a divider.

Table 1: Performance Comparison

	This Work	RFIC '13	ISSCC '13	ISSCC '14
F_{REF} (MHz)	25	40.3	25	40-350
F_{OUT}	908-940MHz	403MHz	4-825MHz	0.39-1.41GHz
RMS Jitter	7.1ps	7.9ps	30ps	2.8ps
Area (mm^2)	0.09	0.1	0.032	0.0066
Power	3.0mW	2.1 mW	3.1mW	0.78mW
FoM	-218.2 dB	-218.8 dB *	-205.5 dB *	-236.5 dB
VDD	1.1V	1.0V	1.0V	0.8V
Architecture	Frac-N	Int-N	Frac-N	Int-N
Divider	No	No	Yes	Yes
Technology	28 nm	65 nm	28 nm	65 nm

Keywords: VLSA (Very Large Scale Analog), ADPLL, CMOS, frequency synthesizer, fractional-N

INDUSTRY INTERACTIONS

Texas Instruments, Intel, Freescale

MAJOR PAPERS/PATENTS

TASK 1836.114: FREQUENCY SHAPEABLE MULTICHANNEL ADCS

YONINA ELDAR, TECHNION, ISRAEL, YONINA@EE.TECHNION.AC.IL

SIGNIFICANCE AND OBJECTIVES

During this period we focused on understanding the fundamental sampling limits of multichannel ADC sampling for cognitive radio (CR) applications in low SNR regimes and in collaborative environments, we continued investigating a chip implementation of our basic structure, and started exploring other areas where our ADCs can reduce rate such as radar and ultrasound.

TECHNICAL APPROACH

Cognitive radio applications: The recovery of wideband input signal support from sub-Nyquist samples in low SNR environments is tackled using two main approaches. Our first objective is to exploit characteristics of communication signals in order to improve detection performance and obtain a detector robust to noise. By exploiting the inherent spectral correlation in communication signals, cyclostationary detectors are highly robust to noise and outperform energy based detectors. The detection of spectrum holes must be impervious to channel fading and shadowing as well. To overcome those issues as well as low SNRs, we develop a collaborative algorithm for cooperative spectrum sensing between several CRs from sub-Nyquist samples.

Chip implementation: together with our collaborators at Stanford we are continuing to investigate various aspects of a chip design that can implement the evolving algorithms achieving minimal sampling rate.

Sub-Nyquist radar: We developed a board for a sub-Nyquist radar based on our new ADC architectures.

SUMMARY OF RESULTS

CR challenges spectrum sensing into dealing with wideband signals in an efficient and reliable way. CR receivers traditionally deal with signals with high Nyquist rates and low Signal to Noise Ratios (SNRs). On the one hand, sub-Nyquist sampling of such signals alleviates the burden both on the analog and the digital side. On the other hand, cyclostationary detection ensures better robustness to noise. We developed a relation between the cyclic spectrum we wish to recover and the correlation between the sub-Nyquist samples, leading to a cyclic spectrum reconstruction algorithm from sub-Nyquist samples. Simulations, performed on typical communication signals, show that our detector outperforms energy detection at low SNRs.

In the context of cooperative CR, we propose a centralized collaborative spectrum sensing from samples acquired at a sub-Nyquist rate at each CR. We use the Modulated Wideband Converter (MWC) for the sampling stage. The CRs sample the wideband sparse signal suffering from different effects of fading and shadowing, and share their low-rate samples with a fusion center, which recover the underlying joint support. The overhead in delay and energy caused by cooperative sensing, is mitigated by processing sub-Nyquist samples. Our approach is shown to outperform one that considers the union of the recovered supports by each CR. We now wish to adapt our centralized approach to a distributed network without a fusion center. The CRs share information with their neighbors and converge together to a common signal support.

The last essential aspect of this task is to bridge between theory and practice, and illustrate our theoretical results in practical conditions. If the theoretical aspects of the research are its very core, the practical ones are part of its motivation and its outcome. To that end, we have designed an analog sampling board with the SAMPL lab. Using the board, we sample an analog wideband signal (with bandwidth 3GHz) at a sub-Nyquist rate of 360MHz, namely 6% of the Nyquist rate. Digital processing and detection are then performed on the samples. The ADC is fed with typical communication signals such as BPSK or OFDM that simulate real CR situations. The next demo is to implement our cyclostationary detection algorithm in order to recover the wideband signal support from the low rate samples from the hardware board. Then, we wish to set up an environment for collaborative spectrum sensing from a network of several CRs, that simulates channel fading and shadowing conditions. We will implement our collaborative spectrum sensing algorithm, first in a centralized and then in a distributed fashion.

Keywords: cognitive radio, spectrum sensing, ADCs, cyclostationarity, collaborative sensing

INDUSTRY INTERACTIONS

Texas Instruments, Intel, AMD

MAJOR PAPERS/PATENTS

[1] D. Cohen and Y. C. Eldar, ”Cyclic Spectrum Reconstruction from Sub-Nyquist Samples,” to appear in Globecom 2014.

[2] D. Cohen and Y. C. Eldar, "Sub-Nyquist Sampling for Power Spectrum Sensing in Cognitive Radios: A Unified Approach," IEEE Trans. on Signal Processing, Aug. 2014.

TASK 1836.117
PERFORMANCE AND RELIABILITY ENHANCEMENT OF EMBEDDED ADCS WITH VALUE-ADDED BIST

RANDY GEIGER, IOWA STATE UNIVERSITY, RLGEIGER@IASTATE.EDU
DEGANG CHEN, IOWA STATE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

The objective of this work is to develop a procedure for implementing parametric BIST of ADCs with a minimal area overhead and with test performance that is at least as good as what is achievable with existing production mixed-signal testers. A second objective is to add value by developing a method of BIST-based calibration to achieve performance enhancement of the ADC. Target linearity improvement is 2 bits. A third objective is to experimentally demonstrate the BIST and BIST-based calibration on a commercial ADC. The test device will be the ADC12, a module in the TI MSP 430 microcontroller. The significance in this work is in providing a BIST solution that can reduce production testing costs and in providing an in-field test and calibration capability that can verify performance in the field and recalibrate on demand if performance degrades due to aging or other factors.

TECHNICAL APPROACH

Working with engineers at TI, the Functionally Related Excitation (FRE) approach to testing using a Stimulus Error Identification and Removal (SEIR) algorithm will be adapted to a BIST solution. The FRE/SEIR approach was developed in conjunction with TI on a previous SRC project. On-chip FRE signal generators using the shift operator will be developed for test signal generation and existing on-chip computation resources will be utilized to minimize the area overhead required to implement the SEIR algorithm. Target area overhead is at most 10% of the area of the existing uncalibrated ADC that is currently in high-volume production.

SUMMARY OF RESULTS

A block diagram showing the BIST capability and the BIST-based calibration is shown in Fig. 1 with a target 12-bit ADC. Two additional bits of resolution have been added to the SAR ADC to allow for a 2-bit improvement in linearity with the BIST-based calibration. The final output is then decimated back to 12 bits after calibration.

The signal generator will be a current ramp integrator comprised of the output from a simple current mirror charging a nonlinear capacitor. With the FRE/SEIR approach, linearity of the ramp is of little concern. But to manage the size of the integration capacitor, a series of faster-rising ramps will be used instead of a single ramp. A delay generator has been developed for initiating the ramps to maintain approximately uniform density of the input signal throughout the input range of the ADC. A critical component is the shift generator which must have a constant shift. The shift generator that has been designed is shown in Fig. 2. The shift is achieved by switching a judiciously placed systematic offset voltage internal to an operational amplifier that is configured as a buffer amplifier. The Boolean control of this shift is shown in the red circle in the figure. The offset voltage of the op amp provides the constancy of the shift needed for the signal generator when targeting true 12-bit performance.

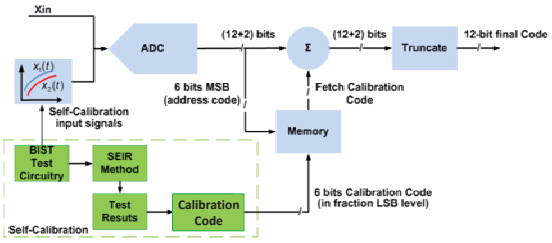


Figure 1: Block Diagram of ADC with BIST-Based Calibration and Value-Added BIST

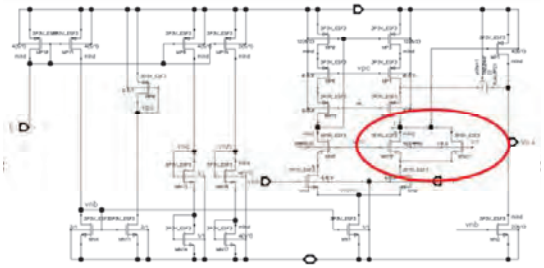


Figure 2: FRE shift generator using switchable systematic Op Amp offset for linear shift operation

Keywords: ADC BIST, self-calibration, analog testing, FRE signal generators, SEIR testing, shift-generators

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

TASK 1836.125: 10GS/S+ RESOLUTION-SCALABLE (4-7BITS) ADCS

MICHAEL FLYNN, UNIVERSITY OF MICHIGAN, MPFLYNN@UMICH.EDU

SIGNIFICANCE AND OBJECTIVES

This research will develop and demonstrate a new approach to high speed ADC design. The new techniques will enable energy efficient, very-high-speed (>10GS/s) moderate resolution analog to digital conversions (4-7b) in nano-scale CMOS technologies. High sampling rate will be achieved without using time-interleaving, thus no calibration is needed and making the system design easier.

TECHNICAL APPROACH

This research to extend the speed and improve the energy efficiency of very fast moderate resolution converters is organized into two key topics:

- New techniques to improve the efficiency of flash-based ADCs
- Sub-ranging and pipelining for efficient 7 bit operation

These techniques will also facilitate adaptability of resolution.

SUMMARY OF RESULTS

This energy efficient ADC with very fast operation speed will facilitate and improve communication applications including:

- High speed serial links
- High bandwidth wireless
- Optical communication

This research addresses SRC research need 1.2 “Architectures for enabling exponential increase in communication bandwidth including embedded memory and NOC approaches.” We will also explore techniques to allow flexible resolution so that the ADC can support both NRZ and multilevel communication.

We are exploring a new fast ADC architecture. The first design iteration of the ADC is operating at 10GS/s sampling speed with 4bit resolution. A prototype 4bit 10GS/s ADC was taped out in the first year of the project. Testing will begin in September 2014.

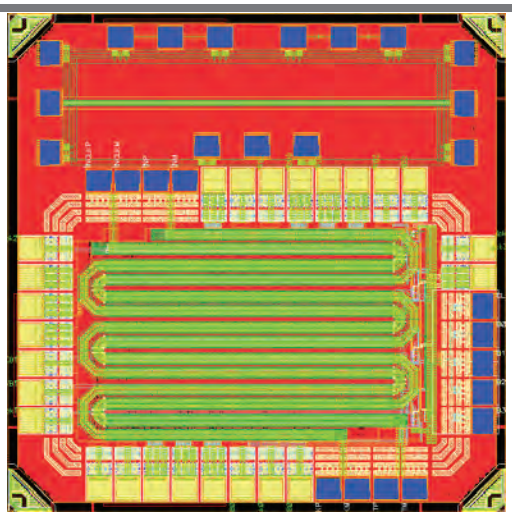


Figure 1: Die plot of 65nm CMOS prototype ADC taped out in first year of project

The new ADC architecture simultaneously achieves high sampling rate and high energy efficiency. The scheme combines the efficiency of the SAR technique with the throughput of flash. The ADC achieves very high-speed operation with low power consumption and occupies a small die area.

Keywords: ADC, flash, two-step, CMOS

INDUSTRY INTERACTIONS

Texas Instruments, IBM

TASK 1836.127: PRECISION TEST WITHOUT PRECISION INSTRUMENTS

DEGANG CHEN, IOWA STATE UNIVERSITY, DJCHEN@IASTATE.EDU
RANDY GEIGER, IOWA STATE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

Accurate spectral analysis is widely used in IC characterization and final test. Ideal IEEE standard test requires accurate instruments and accurate test control, resulting in expensive equipment, complex test setup, demanding maintenance, RTM delays, and high test cost. The objective of this research is to develop new spectral test algorithms to remove IEEE standard requirements, deliver accurate full spectrum test results, and greatly reduce test equipment cost, RTM delays, and test time.

TECHNICAL APPROACH

The task of accurate spectral testing is re-examined as a weakly nonlinear signal and system identification problem. Techniques from statistical signal processing are carefully incorporated to ensure that the new algorithm effectively extracts all useful information available in the collected data and that the achieved test accuracy level is near the theoretical limit. An innovative iterative time-frequency domain processing technique is utilized to achieve the best accuracy and time efficiency trade-off, in which accurate sine wave identification is done in the frequency domain but identified component removal is done in the time domain. This ID and correction technique also enables us to directly work with the small signal components coming from various sources of distortion under test.

SUMMARY OF RESULTS

The final goal of the project is to be able to eliminate all the stringent requirements in the ideal IEEE standard spectral testing. These requirements include: strictly coherent sampling, accurate amplitude control, high purity sine wave stimulus, and jitter-free sampling clock signal. During the first year, we have published two full length journal articles in the IEEE Transactions on Instrumentation and measurements, one full length paper in the IEEE International Test Conference, and one paper in the IEEE VLSI Test Symposium. In the first IEEE TIM paper, we introduced FIRE, the fundamental identification and replacement method, for accurately test an ADC's full spectrum performance, allowing arbitrary amount of sampling clock non-coherency. In the second IEEE TIM and IEEE ITC papers, we introduced a new method for accurate spectral testing allowing simultaneous non-coherent sampling and amplitude clipping. The method is later called FERARI standing for fundamental estimation, removal, and residue interpolation. It runs very fast, is both time and memory efficient, and validated by industry to be accurate beyond the 20 bit level. In the IEEE VTS paper, we introduced a very efficient method for separating the effects due to clock jitter from those due to noise, so that accurate ADC spectral performance can be obtained even in the presence of significant random clock jitter.

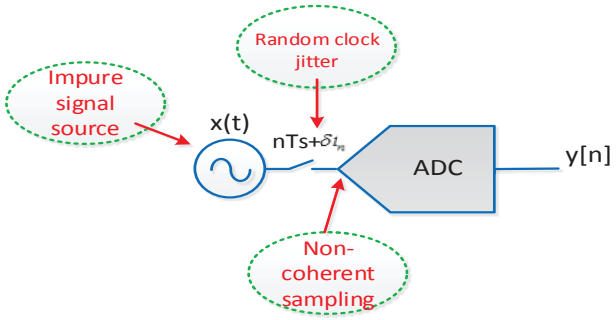


Figure 1: Desired spectral test setup allowing non-pure source, amplitude clipping, non-coherent sampling and random/periodic clock jitter.

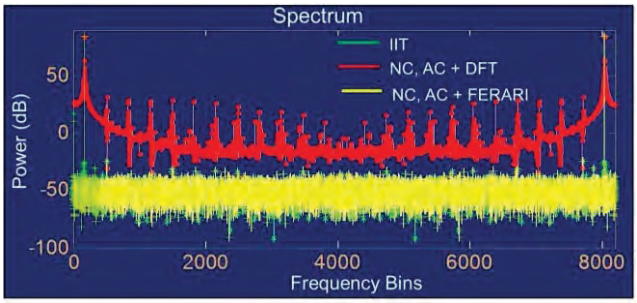


Figure 2: When there is both non-coherency and amplitude clipping, DFT produces gross errors, but FERARI produces a spectrum nearly identical to that obtained under ideal IEEE testing.

Keywords: AC test, spectral test, non-coherent sampling, amplitude clipping

INDUSTRY INTERACTIONS

Texas Instruments, Freescale

MAJOR PAPERS/PATENTS

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TASK 1836.128: STATISTICAL ANALOG DESIGN PROPERTY CHECKING

PENG LI, TEXAS A&M UNIVERSITY, PLI@TAMU.EDU

SIGNIFICANCE AND OBJECTIVES

Analog/mixed-signal (AMS) verification has grown in importance as the AMS design complexity increases and verification becomes a significant bottleneck in design. This project aims to address the grand challenges in AMS verification by developing computationally-scalable statistical property checking methods and/or techniques for reasoning design errors.

TECHNICAL APPROACH

Many formal verification methods are not scalable due to the inherent computational complexity. In this work, our main objective and approach are to address this scalability challenge by developing simulation-data driven techniques that combine various machine-learning techniques to provide feasible verification of large analog/mixed-signal circuits.

SUMMARY OF RESULTS

Growing circuit complexity and design uncertainty has made it difficult to predict whether large circuits meet target property specifications. To address this, we conservatively approximate the failure probability estimate by defining an interval that bounds this probability. Doing so using an arbitrary sampling distribution requires a learner. Given that the learner's knowledge is imperfect, the interval must first capture its uncertainty. An ensemble of such learners can then be used to compensate for the bias. Lastly, we develop an adaptive sampling scheme to tighten the obtained interval with increased simulation resources, thus controlling the accuracy vs. turn-around-time trade-off.

We have explored the above approach by incorporating an adaptive sampling technique in the verification loop. We consider a PLL with 40 uncertain parameters such as transistor length variations and 8 design properties such as settling time and output jitter. Fig. 1 illustrates the application of our approach to the verification of this PLL. As can be observed, our technique provides accurate estimates along with tight bounds for the failure probability with a small amount of simulation data.

In a different direction, we have developed a hierarchical parallel SMT-based formal technique for verifying the dynamic design properties. Internal to this technique, circuit simulation data are exploited to reduce the complexity of formal verification. To further speed up, we propose a parallel hierarchical technique based on circuit decomposition. An AMS circuit is systematically decomposed into subsystems with less complex transient behaviors which can be solved in parallel. Then a simulation-assisted SMT-based reachability analysis approach is adopted to conservatively approximate the reachable spaces in each subsystem with support function representations. We formally develop a general decomposition algorithm without over-approximation in system reconstruction. The efficiency of this general methodology is further optimized with an efficient parallel implementation strategy.

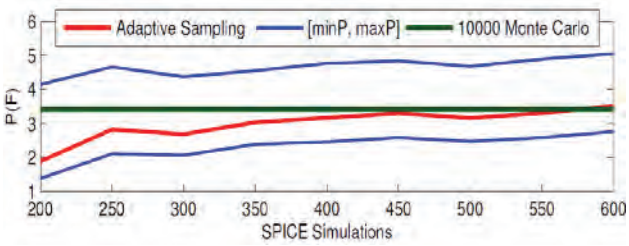

Figure 1: Estimated failure probability of 8 design properties for a PLL: estimated probability and bounds as functions of number of simulation runs.

This approach has been applied to several circuits including a digital PLL, whose lock time verification is sped up by 248X using 20 parallel threads (Fig. 2).

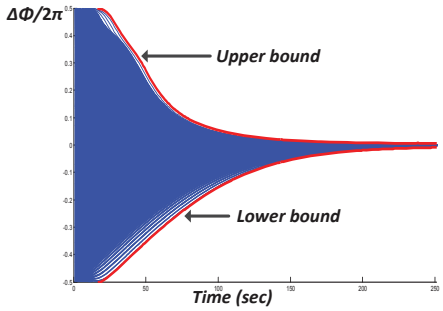

Figure 2: Phase error bounds of a digital PLL with initial condition uncertainty computed by the hierarchical parallel SMT technique with 248X speedup using 20 threads.

Keywords: verification, property checking, analog and mixed-signal, reachability analysis, machine learning.

INDUSTRY INTERACTIONS

Intel, Freescale, Texas Instruments

MAJOR PAPERS/PATENTS

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TASK 1836.129: DESIGN TECHNIQUES FOR FAST TURN ON/OFF VOLTAGE- AND CURRENT-MODE DRIVERS

PAVAN KUMAR HANUMOLU, UNIVERSITY OF ILLINOIS,
HANUMOLU@ILLINOIS.EDU

SIGNIFICANCE AND OBJECTIVES

Proposed research sets out to explore I/O link architectures with "energy-proportional" behavior that results in low power operation at system level across I/O link utilization levels. Use of highly digital architectures that ensure resilience of I/O links to issues such as process variability and low supply voltage is also emphasized.

TECHNICAL APPROACH

To achieve low power I/O link operation, the inactivity periods of the I/O link are exploited in the technical approach. A key requirement to fully exploit idle time of the link is fast turn on/off circuits such as voltage regulators and bias generation circuits. Highly digital circuit architectures that can save the state of the circuit at little power expense are used to achieve fast turn on operation for voltage regulator and bias circuits.

SUMMARY OF RESULTS

For voltage mode output drivers, the turn on time is mainly limited by the slow settling of the voltage regulators that control output swing and termination impedance. To overcome this problem, a highly digital voltage regulator is used that provides a means to turn on/off rapidly while consuming no static power in the off-state (Fig. 1). During the off-state, regulator states are saved in their respective accumulators. When turning on, the nyquist rate DACs rapidly restore node voltages using the accumulators' state. A 5Gb/s output driver is implemented in 90nm CMOS process that achieves 2ns turn-on time (Fig. 2).

While current mode output drivers do not require supply voltage regulators, their turn on time is limited by the tail current source bias circuit. A highly digital calibration-based bias circuit that stores the state of the bias node and helps in its fast settling during turn on is proposed. It utilizes an auxiliary fast charging path to reduce the turn on time. An 8Gb/s current mode output driver is implemented in 90nm CMOS process that achieves 4ns turn on time (Fig. 3).

Keywords: Fast turn-on, Digital voltage regulator, Rapid on-off biasing

INDUSTRY INTERACTIONS

Texas Instruments, Intel, AMD

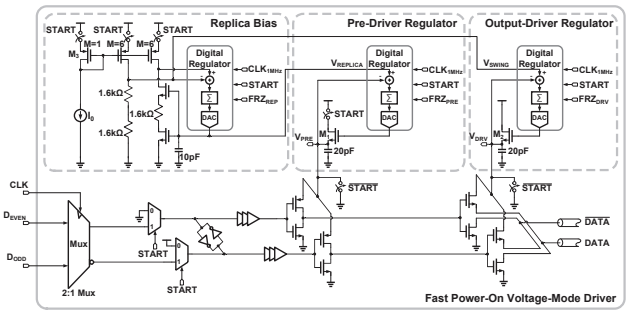

Figure 1: Schematic of voltage-mode fast turn on/off driver.

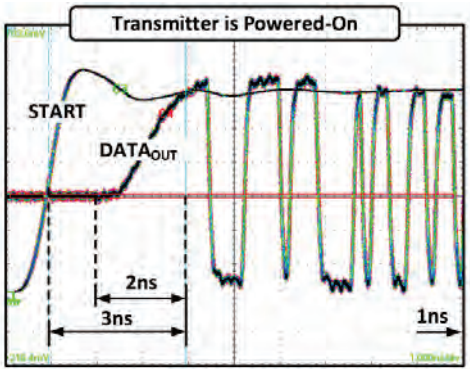

Figure 2: Voltage-mode driver turn on transient waveforms.

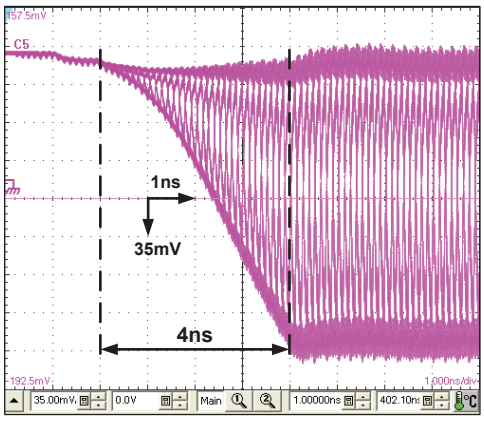

Figure 3: Turn on transient waveform for current-mode driver.

MAJOR PAPERS/PATENTS

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TASK 1836.132: FAULT-COVERAGE ANALYSIS OF ANALOG/MIXED-SIGNAL TESTS BASED ON STATISTICAL DISSIMILIARITY

JAEHA KIM, SEOUL NATIONAL UNIVERSITY, KOREA, JAEHA@SNU.AC.KR

SIGNIFICANCE AND OBJECTIVES

The number of mixed-signal ICs escaping production screening is sharply rising due to the increasing use of digital circuits within analog systems. This task aims to develop a systematic way to quantitatively measure the fault coverage of a given analog/mixed-signal circuit test. This is a key pre-requisite to the automatic generation of efficient analog/mixed-signal test suites or patterns that can achieve high defect coverage and short testing time.

TECHNICAL APPROACH

This task will explore ways of quantitatively measuring the fault coverage of an analog/mixed-signal test suite leveraging various statistical discrimination methods.

For instance, a test is said to cover a fault when the fault causes large enough difference in the test's response that can be distinguished from the normal statistical variations of the circuit due to global process, voltage, and temperature (PVT) variations and local transistor-to-transistor mismatches.

In addition, the correlations among the test responses can be utilized in various ways, for instance, to enhance the effective coverage of a given test suite and to estimate the statistical distributions with a small number of Monte-Carlo samples.

SUMMARY OF RESULTS

An initial study has been conducted that quantifies the test coverage of some representative analog/mixed-signal circuits over basic catastrophic stuck-short/open faults. Despite the simplistic assumptions made, the results demonstrate that the fault coverage analysis based on statistical discrimination can be an effective way to measure the fault coverage of a given test suite and guide the composition of an efficient test suite. For instance, the analysis shows that all the stuck-open/short faults in an 8-bit digitally-controlled phase interpolator can be covered with only 5 different delay measurement tests. The analysis can also identify redundant components in the circuit.

Interestingly, the correlations among the test responses that arise naturally due to the inherent variability in the design can be utilized to improve the effectiveness of this approach. For instance, using correlations, the number of tests required to test a 8-bit phase interpolator can be reduced from 8 to 5.

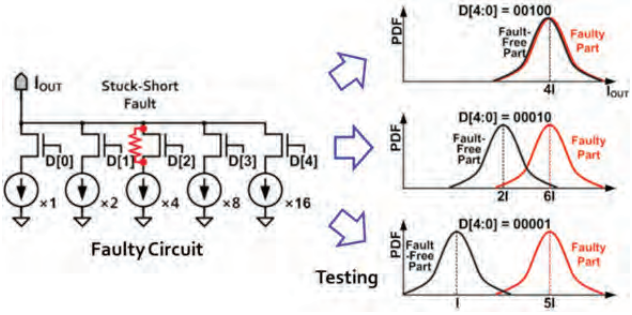

Figure 1: Determining fault coverage based on variability distribution.

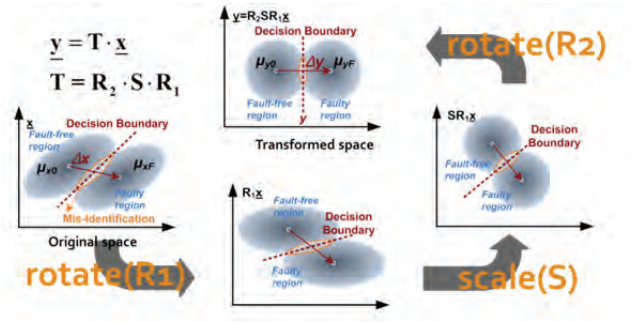

Figure 2: Fault coverage analysis in case when multiple test responses have cross-correlations.

Keywords: analog/mixed-signal circuits, production tests, fault coverage analysis, test compaction, automatic test pattern generation.

INDUSTRY INTERACTIONS

Texas Instruments, Intel, and Global Foundries.

MAJOR PAPERS/PATENTS

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TASK 1836.134: HYBRID TWO-STEP PLLS FOR DIGITAL SOCS IN NANOSCALE CMOS

PETER KINGET, COLUMBIA UNIVERSITY, KINGET@EE.COLUMIBA.EDU

SIGNIFICANCE AND OBJECTIVES

Demonstration of a high frequency PLL in nanoscale CMOS with fine tuning resolution and low jitter while being very area compact through the use of ring oscillators. Innovations at the component level (hybrid phase frequency detectors) and the architecture level (wideband two-step PLLs and fractional-N noise cancellation with auxiliary sub-sampling phase detectors).

TECHNICAL APPROACH

Our target is to design a compact hybrid two-step fractional-N PLL: a first ultra-low noise reference multiplying PLL has low in-band phase noise by exploiting novel hybrid high gain phase detectors while maintaining supply robustness; the second PLL has low frequency gain but provides fractional frequency resolution and has a much reduced noise impact. A novel fractional-N quantization noise suppression mechanism is further proposed using an auxiliary sub-sampling phase detector. We propose to investigate two-step PLLs because they offer better intrinsic performance and, as such, will enable the use of ring oscillators to replace large area LC oscillators while maintaining overall performance.

SUMMARY OF RESULTS

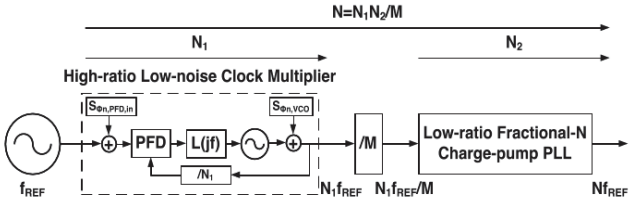

Figure 1: Block Diagram of Two-Step PLL

Fig.2 below shows the comparison of the performance of the two-step PLL with a traditional PFD and the proposed hybrid PFD. The in-band noise of the PLL improves by 8dB and the output jitter improves to 1.18ps RMS and 0.97ps RMS after applying a 3MHz high-pass filter at the PLL output, which meets the target of less than 1ps RMS.

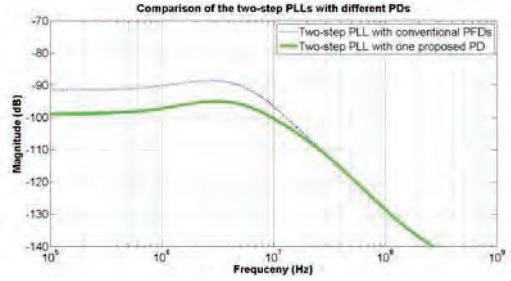

Figure 2: Comparison of the new PFD with conventional PFD

Table 1: Performance comparison of the PLL

	Grollitsch-10'	Sai-12'	Min-13'	Kao -13'	*This Work*
Output Frequency (GHz)	3	3.1	5	2	*4*
Reference Frequency (MHz)	25	36	10	26	*50*
Supply voltage (V)	1.3/1.1	1.2	1.2	1.2	*1.2*
Power (mW)	11.59	25.8	29.6	25	*12*
Active Area (mm2)	0.038	0.95	0.12	0.055	*0.062*
Technology (CMOS)	65nm	65nm	90nm	40nm	*55nm*
Integrated Jitter (psrms)	1.4	2.23	3.8	3.4	*0.79*
Figure of Merit (dB)	-226.4	-218.9	-213.7	-215.4	*-231.3*

Keywords: PLL, fractional-N noise cancellation, novel Phase Frequency Detector, ring oscillator, two-step PLL

INDUSTRY INTERACTIONS

Intel, Texas Instruments, Global Foundries are liasons

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TASK 1836.136: INJECTION-LOCKED RING OSCILLATORS FOR CLOCK DISTRIBUTION IN MANYCORE PROCESSORS

BOROVOJE NIKOLIĆ, UC BERKELEY, BORA@EECS.BERKELEY.EDU

SIGNIFICANCE AND OBJECTIVES

Technology scaling has enabled integration of many independent processing elements on a single die or in a same module. Energy-efficient circuit design for synchronization of manycore processors, based on both traditional techniques and injection-locked ring oscillators is the objective of this work, and will be demonstrated in a scaled CMOS process.

TECHNICAL APPROACH

We are developing a low-overhead global clock distribution scheme for manycore processors and heterogeneous SoCs based on injection-locked ring oscillators (ILROs). Within each core, we will utilize a fast-locking, power and area efficient ILRO, which will be 'hard' injection-locked by a globally distributed low-frequency reference. An ILRO behaves as a first-order PLL, but with unconditional stability and higher bandwidth than PLLs. The high tracking bandwidth of an ILRO helps to reject internal noise. A hard-coupled ILRO can multiply its output frequency, reducing the power overhead of the global clock distribution network. In other words, by routing a low frequency global clock and then multiplying up to obtain the core clock, we can minimize overall power consumption.

SUMMARY OF RESULTS

We have developed a baseline design for clock generation in manycore processors, based a delay-locked loop (DLL) and a phase-picking clock generator. A ~2GHz reference clock is distributed to DLLs, which generate 16 uniformly-distributed clock phases. Phase-picking clock generator picks the appropriate phase for each clock cycle, based on information from the timing replica path.

The design, implemented in 28nm ultra-thin body and BOX fully-depleted silicon-on-insulator (UTBB FDSOI) technologies is fully functional and occupies 32µm x 30µm. Generated clock frequency is in the range of 450-1890MHz at 1V and 155-840MHz at 0.6V.

While this design's size and power are appropriate for a medium-sized core, the overhead of distributing a high-frequency clock to a very small core, or for a system with many cores may be high. Our on-going research targets ILRO-based clock generation, as shown in Fig. 2.

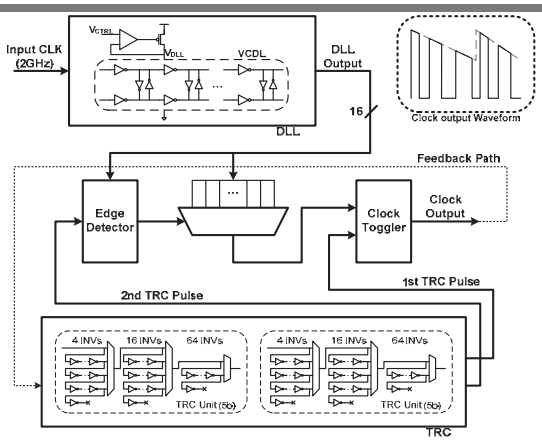

Figure 1: DLL-based clock generation.

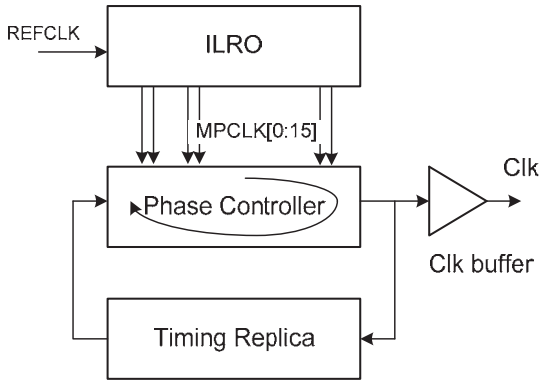

Figure 2: Injection-locked ring-oscillator clock generator.

To generate local clocks within processing cores integer-N clock multiplication scheme will be used, followed by rotating phase picking/interpolation. The concept of local clock generation is based on a local controller that is picking the right phase for the core, based on timing replica circuits, illustrated in Fig. 2. In the example design, the controller can choose to pick any of the 16 clock phases, thus adjusting the clock in a wide range. If a finer resolution of the clock is needed, interpolation between the phases can be used.

Keywords: CMOS, clock, manycore, DLL, PLL.

INDUSTRY INTERACTIONS

Intel, Freescale.

TASK 1836.137: 50 GS/S AND BEYOND FREQUENCY-INTERLEAVED ENERGY-EFFICIENT ADCS

ALI NIKNEJAD, UC BERKELEY, NIKNEJAD@BERKELEY.EDU

SIGNIFICANCE AND OBJECTIVES

Gigabit per second ultra high-speed analog-to-digital converters (ADCs) are needed in a variety of applications, including instrumentation, high speed links, and mm-wave receivers. Fundamentally, analog to digital conversion resolution at these speeds is limited by the clock aperture jitter. Moreover, signal splitting and routing incurs significant power penalties due to the high bandwidth requirements, explaining the poor energy efficiency of published ADCs beyond 10 GS/s.

TECHNICAL APPROACH

In modern CMOS technology, the most effective technique to improve the ADC speed is by time interleaving, whereby slower accurate ADCs can work in concert to effectively increase the data rate. But due to fundamental clock jitter, the resolution of time-interleaved ADCs is limited. By also employing *frequency interleaving*, we propose to introduce a new factor by which we increase the speed of the ADC. The wideband signal is channelized using complex baseband I/Q channels to reduce the clock jitter requirements, preserving the speed and resolution.

SUMMARY OF RESULTS

During the first year of this project, we have made significant progress in the design of our first prototype. First we analyzed the system level requirements for the ADC by performing system level simulations using Agilent SystemVue. Each channel is modeled as a direct sampling system with clock jitter. The phase noise of the LO source is also included to model the extra noise penalty of frequency down-conversion. This system simulation framework first and foremost validates our assumption that with the same jitter specifications, we can increase the signal SNR with a frequency- interleaved architecture by 10-15 dB (assuming 200-400fs jitter and an input frequency of 20 GHz). The framework also allows us to include non-idealities such as harmonic mixing, distortion in the front-end, and finite filter response and therefore channel cross-talk.

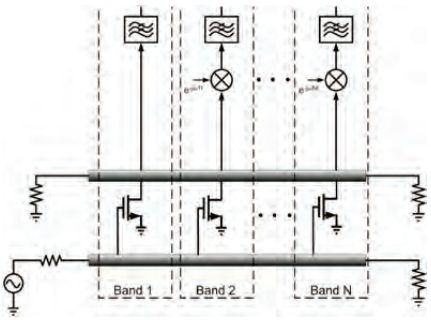

Figure 1: Proposed Frequency Interleaved ADC.

Using the system simulation framework, the architecture shown in Fig. 1 has been proposed and analyzed. The ADC includes a distributed amplifier at the front-end that obviates the need to split the signal. Various stages are tapped by complex I/Q harmonic reject down-converters that bring the signal to baseband. Analog filtering is then following by an oversampled ADC and digital signal processing to reconstruct the signal.

One challenging aspect of the ADC architecture is the need to synthesize dozens of RF LO signals from a few reference tones. RF clock distribution and routing become a major challenge and a bottleneck in determining the optimal number of channels in the ADC. The mixer also needs to have good harmonic rejection because harmonics of the low channels can easily fall into the upper channels, introducing cross-talk. Ultimately this may limit the resolution of the overall system because frequency mixing cross-talk can be equated to SNR loss for a given band. A new architecture for a harmonic rejection mixer is proposed, analyzed, and designed.

Based on our findings, we have designed and manufactured a test chip containing all the key analog elements in the ADC. The first prototype has 8 I/Q outputs that cover from DC to 25 GHz and a LO generation scheme to generate 8 I/Q LO tones from two input tones using SSB mixers and frequency dividers. Each analog output will feed external ADCs and an external FPGA for final signal reconstruction and testing. The prototype has been fabricated in a TSMC 65nm process and is currently undergoing testing. Preliminary findings have confirmed the operation of the distributed amplifier and the IF path (filters), but RF testing has been hampered by frequency locking issues under investigation.

Keywords: mm-Wave, RF ADC, ADC, High Speed Links

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

None.

TASK 1836.141: IC DESIGN FOR RESILIENCE AGAINST SYSTEM-LEVEL ESD

ELYSE ROSENBAUM, UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN, ELYSE@ILLINOIS.EDU

SIGNIFICANCE AND OBJECTIVES

System-level ESD reliability is uncorrelated with component-level ESD reliability yet IC designers are asked to build-in system-level ESD resilience. This project's objective is to develop integrated circuit designs that are resilient to power-on ESD and a behavioral model of the IC's that can be used for system ESD design.

TECHNICAL APPROACH

ESD testing of a prototype system containing a custom test chip is used to ascertain the causes of ESD-induced soft failures. The effect of package and reverse body bias on latchup susceptibility during system-level ESD is studied using measurements and circuit-level simulation. Latchup rules for the body bias nets will be developed. AC analysis of power distribution networks with triggered-on ESD circuits is performed to ascertain the relation between design variables and PDN stability. A methodology to construct a behavioral model of the pin-level response to system-level ESD using measurement data without the proprietary information about the circuit design is being developed.

SUMMARY OF RESULTS

A test-chip for monitoring soft failures was subjected to IEC 61000-4-2 and transmission line pulse ESD stresses. The test chip was placed on a custom test board, shown in Fig. 1, which could be powered by a battery pack or by a table-top power supply. On-chip soft failure diagnostics include logic circuit upset detection, substrate potential latchup monitors, input glitch detectors, system I_{DDQ} monitors, and USB transmitters. Power-on TLP testing and IEC61000-4-2 ESD were observed to produce different failures. Also, different failures are reported for mobile systems and those powered through grounded supplies. In particular, the mobile system is far more susceptible to noise-induced soft failures while the grounded system has a lower threshold for hard failure.

Some of the observed logic errors were attributed to supply noise while others were triggered by a parasitic NPN which couples the I/O region to an N^+ diffusion in the core circuitry. The latter upset mechanism is observed only for ESD stresses of duration greater than 50ns, due to the limited bandwidth of the parasitic NPN. Transistor sizing determines the susceptibility of a given circuit to upset.

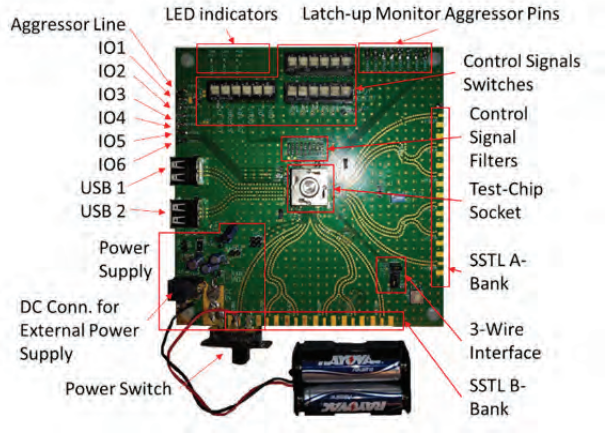

Figure 1: Photograph of test board.

A small-signal model of active rail clamp circuits was developed and used to explore how the trigger circuit design impacts the power integrity during ESD events. Analysis and simulation showed that low gain, high bandwidth trigger circuits promote stability, indicating a tradeoff between clamp on-resistance, stability, and area.

In simulation and measurement, it was observed that ground bounce resulting from parasitic inductance in the system or package can cause the ESD current to return to the board ground via unexpected paths through the IC. The ground bounce may be large enough to briefly power down power domains, causing logic errors and posing a global latchup risk.

Upcoming activities will focus on behavioral modeling and ESD noise mitigation strategies.

Keywords: Electrostatic discharge, IEC 61000-4-2, power integrity, latch-up

INDUSTRY INTERACTIONS

Texas Instruments, Freescale

MAJOR PAPERS/PATENTS

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TASK 1836.145: RF AND MIXED SIGNAL QUANTUM CMOS DEVICES AND CIRCUITS

MARK LEE, THE UNIVERSITY OF TEXAS AT DALLAS, MARKLEE@UTDALLAS.EDU
YUN CHIU, THE UNIVERSITY OF TEXAS AT DALLAS

SIGNIFICANCE AND OBJECTIVES

This project pioneers a path towards explicit quantum mechanical operation in industrial CMOS by demonstrating a new class of quantum MOS devices and circuits. This work will develop understanding of quantum MOS device physics and incorporation of such devices into RF and mixed-signal circuits operating at or near room temperature.

TECHNICAL APPROACH

This research introduces quantum well (QW) MOS transistors that show explicit quantum transport characteristics. A main focus will be to understand how to make QWMOS devices useful in circuits designed to exploit the explicit quantum characteristics. An important goal is to develop a QWMOS device model adaptable into SPICE circuit modeling. Research work started on QWMOS transistors, fabricated by Texas Instruments using its 45-nm CMOS, that show signatures of quantum transport as negative differential transconductances (NDTCs) at temperatures up to at least 230 ^{o}K. Such NDTCs will be exploited to demonstrate feasibility of oscillator and ADC circuits incorporating QWCMOS.

SUMMARY OF RESULTS

The first half year of this project has focused on detailed measurements of QWCMOS devices fabricated using the TI 45-nm CMOS process and the subsequent development of a useful understanding of the particular quantum device physics governing these new devices.

We investigated the design, fabrication, and basic operating characteristics of a new class of explicitly quantum Si transistors. Unlike virtually all existing quantum semiconductor devices, in this case the potential profile that defines an electron quantum well (QW) in a 2-dimensional MOSFET interface is built by lateral ion implantation doping using an industrially standard process. The potential depth of such a QW in the interface channel between source (S) and drain (D) contacts can then be modulated by an applied gate voltage V_G.

In particular, we found evidence that a lateral QW can be successfully constructed in this manner by the observation of explicit quantum transport signatures in the form of one or more negative differential transconductances (NDTC), where $g_m = \partial I_{DS}/\partial V_G < 0$, at temperatures up to 230 ^{o}K. Data showing a series of three NDTCs is shown in Fig. 1, which also shows that a conventional (no QW) NMOS transistor on the same chip does not show any NDTCs.

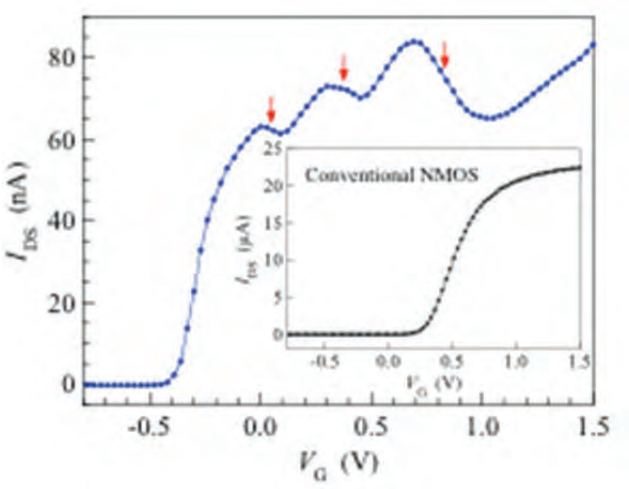

Figure 1: Drain-source current vs. gate voltage for a 35 nm gate length QW NMOS transistor at 10 ^{o}K temperature. Red arrows indicate regions of NDTC. Inset: Same type of measurement for a conventional 35 nm NMOS with no QW. The conventional NMOS devices never show NDTC.

The fact that these QW Si transistors were fabricated by Texas Instruments (TI) using a standard process means that these devices are fully compatible with standard industrial manufacturing and are scalable to smaller generations of processing nodes.

A preliminary device physics model was developed that explains the main features of the QW NMOS operating characteristics in terms of a hybrid MOSFET/bipolar device where the bipolar current gain oscillates as quantum states are introduced in the QW via the applied gate bias.

Keywords: Quantum devices, quantum circuits, negative differential conductance, quantum well, quantum CMOS

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

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