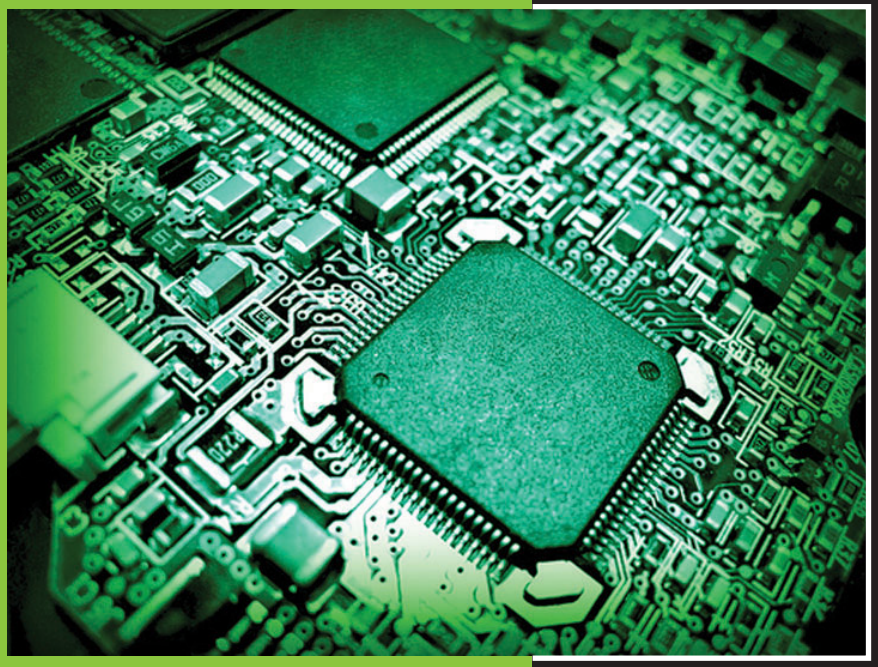
TEXAS ANALOG CENTER OF EXCELLENCE

ANNUAL REPORT 2010-2011



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TxACE
TEXAS ANALOG
CENTER OF EXCELLENCE

TxACE 2010-2011 ANNUAL REPORT

Over the past year, the Texas Analog Center of Excellence (TxACE) has made much progress. TxACE located at the University of Texas is the largest analog research center based in an academic institution. It is also the first to be a global center. Analog and Mixed Signal integrated circuits engineering is both a major opportunity and a major challenge. It is an opportunity because of the increasing importance of analog integrated circuits in electronic systems and the emergence of new applications. It is a challenge because of the inherent difficulty of the art, which also makes it an opportunity. The creation of advanced wireless technology and sophisticated sensing and imaging devices depends on the availability of engineering talent for analog research and development. TxACE was established to help translate these opportunities into economic benefits by overcoming the challenge and meeting the need. Support for TxACE has been provided through a collaboration of the state of Texas, Texas Instruments, the Semiconductor Research Corporation, the University of Texas System, and the University of Texas at Dallas. Figure 1 shows the location of member institutions including three international members.

The research program is beginning to yield results and the center is starting to establish itself as a focal point of academic analog research in the world. The research tasks are organized into four research thrust areas: Healthcare, Safety and Security, Energy Efficiency and Fundamental Analog. The scope of investigation extends from circuits operating at dc through terahertz, data converters that sample at 10's of mega-samples/sec to 10's of giga-samples/sec, ac-to-dc and dc-to-dc converters working at μW to Watts, energy harvesting circuits, protein and DNA sensors and many more. Significant improvement on existing mixed signal systems and exciting new applications based on this circuit research are anticipated. Graduate students who have been exposed to "hands on" innovative research are forming the leading edge of a flow of analog talent into industry. Close collaboration with and responsiveness to industry needs provide focus to the educational experience.

OUR MISSION

The Texas Analog Center of Excellence seeks to create fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, health care, and public safety and security.

OUR RESEARCH THRUSTS

- Safety & Security
- Health Care
- Energy Efficiency
- Fundamental Analog Circuits Research

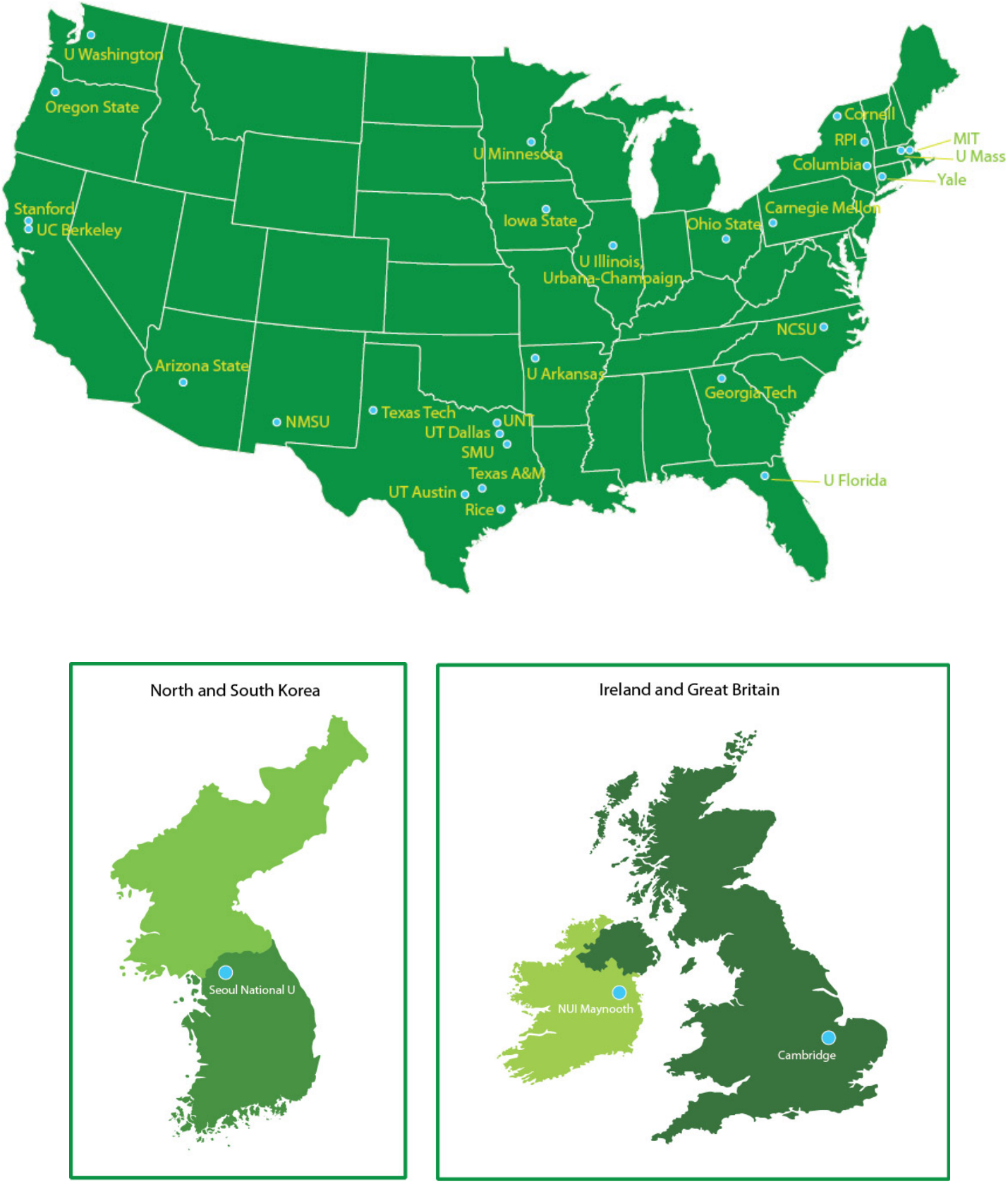


Figure 1: Member institutions of Texas Analog Center of Excellence

DIRECTOR'S MESSAGE

As we end the third year, the infrastructure and research accomplishments of The Texas Analog Center of Excellence (TxACE) have become consistent with our objective to lead analog research and education that can create new economic opportunities by improving analog and mixed signal technology, education, research and manufacturing.

TxACE is the largest center based in an academic institution for analog research in the world on the basis of funding and the number of principal investigators (67 principle investigators from 31 academic institutions). A majority of the leading analog researchers in the United States are participating in the center. Seven universities (Rice, SMU, Texas A&M, Texas Tech, UNT, UT- Austin, UT-Dallas) are from the state of Texas. Of the twenty four from outside of Texas, three are international.

Over the last year, the center supported 94 graduate students (60 from Texas universities and 34 from outside of Texas), and 14 PhD and 7 MS degrees were awarded to TxACE students.

TxACE laboratories and design facilities are fully functional, and nearly fully equipped. They form probably the best laboratory for electronics circuits research. The TxACE high frequency circuit characterization tools are helping to lower a critical barrier for advancing millimeter and sub-millimeter integrated circuit technology. These capabilities are a global asset.

Last year, the TxACE researchers have published 24 journal papers and 68 conference papers. They have also made 5 invention disclosures and filed 2 patents.

TxACE has more importantly started to demonstrate its quality of research and to make impact. An invention of TxACE researchers has been licensed. At the 2011 VLSI Symposium on Circuits, 20-25% of all analog papers were authored by TxACE affliated researchers. Numerous papers authored by TxACE researchers have made into the IEEE list of most down loaded.

There are still much to improve. In particular, the efforts to improve fabrication access have not yet yielded significant results. In the upcoming year, the center with the support of SRC will initiate a program for chip aggregation to lower cost.

All these are due to the hard work of TxACE principal investigators and students as well as the generous support of the state of Texas, the University of Texas, Dallas, the University of Texas System, Texas Instruments Inc., and Semiconductor Research Corporation. I thank the TxACE team, and I am looking forward to a new year with greater research accomplishments and impact.

Kenneth K. O, Director, TxACE, Texas Instruments Distinguished Chair, UT Dallas

BACKGROUND & VISION

For the past 20 years semiconductor electronics was driven by digital logic. This led to the digital revolution that we are all familiar with; impacting things from computational power to high definition digital television. For the next 20 years, analog and mixed signal semiconductor technology is expected to drive progress as electronics continues to bridge the gap between the analog real world and the digital information infrastructure. High performance analog technology is a unique segment of the semiconductor electronics business. It requires special skills in both design and process that reside predominantly in the United States.

To lead this change, in particular to lead analog technology education, research, commercialization, manufacturing, and job creation, the Texas Analog Center of Excellence was formally announced by Texas Governor Rick Perry in October 2008 as a $16M collaboration of the Semiconductor Research Corporation, the state of Texas through its Texas Emerging Technology Fund, Texas Instruments, Inc., the University of Texas system and the University of Texas at Dallas (see Figure 2). The center seeks to accomplish these objectives by creating fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, healthcare, and public safety and security.

CENTER ORGANIZATION

The Texas Analog Center of Excellence is guided by agreements established with the Center sponsors. The Industrial Advisory Boards identifies the research needs and select research tasks in consultation with the center leadership. Figure 2 diagrams the relationship of TxACE to the members of the sponsoring collaboration.

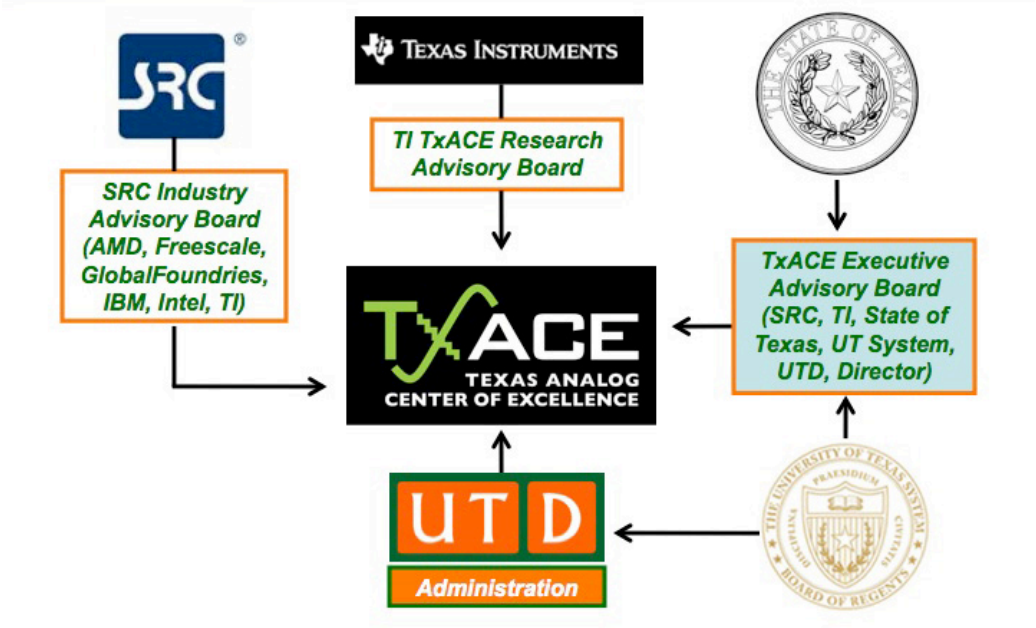


Figure 2: TxACE organization relative to the sponsoring collaboration

The internal organization of the Center is structured to flexibly perform the research mission while not detracting from the educational missions of the University. Figure 3 identifies the elements of the organization. The TxACE Director is Professor Kenneth K. O. The center research is arranged into four thrusts that comply with the mission of the Center: Safety and Security, Health Care, Energy Efficiency and Fundamental Analog Research. The last thrust consists of vital research that cuts across more than one of the first three research thrusts. The thrust leaders are Prof. Brian A. Floyd of North Carolina State University for the safety and security thrust, Prof. R. Harjani of the University of Minnesota for the health care, Prof. D. Ma of the University of Texas, Dallas for the energy efficiency thrust, and Prof. D. Allstot of the University of Washington for fundamental analog research. The thrust leaders and Prof. Y. Chiu of the University of Texas, Dallas form the executive committee. The committee along with the director form the leadership team which works to improve the research productivity of center by increasing collaboration, better leveraging the diverse capabilities of principle investigators of the center, and lowering research barriers. The leadership team also identifies new research opportunities for consideration by the Industrial Advisory Boards.

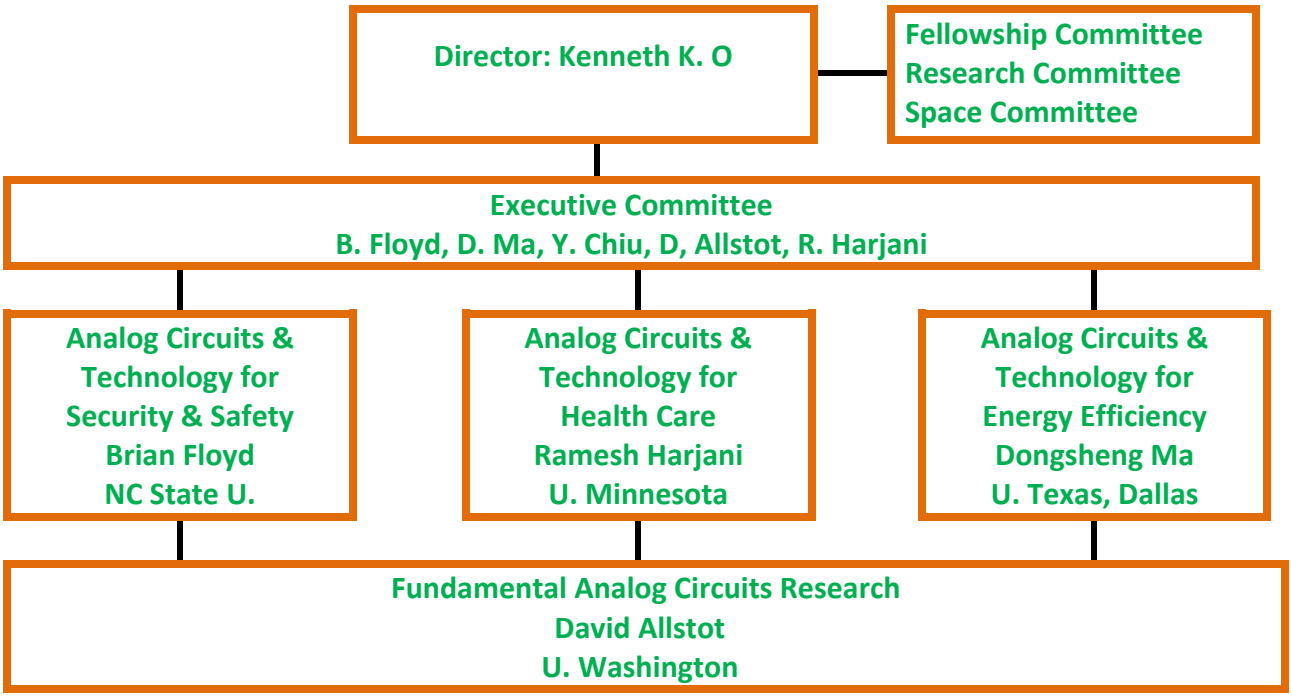
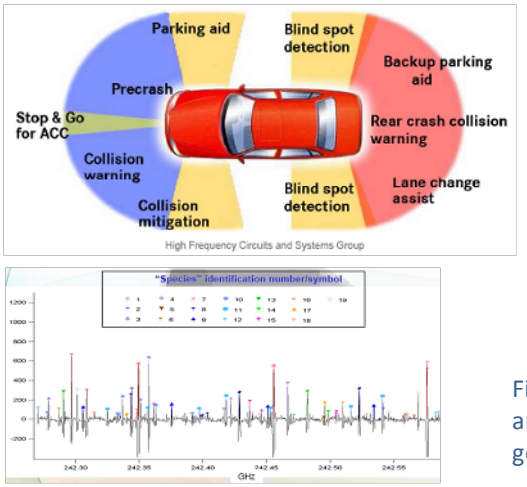


Figure 3: TxACE organization for management of research

PUBLIC SAFETY AND SECURITY

(Thrust leader: Brian Floyd, NC State University)

TxACE has awarded nearly $3 million to researchers to develop analog technology that enhances public safety and security. The projects are intended to: 1) Enable a new generation of devices that can scan for harmful substances by researching 200-300-GHz silicon ICs for use in spectrometers and 2) Significantly reduce the cost of on-vehicle radar technology to improve automotive safety by researching circuit techniques that can improve manufacturing and lower test and packaging costs.



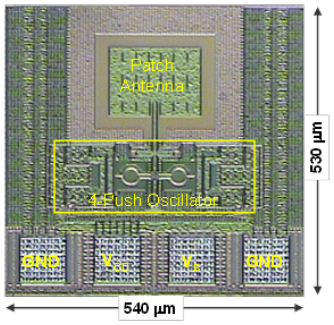


Figure 4: Millimeter wave radar to improve automobile safety and rotational spectrum around 300 GHz. 560-GHz signal generation circuit in 45-nm CMOS (O, UT, Dallas).

HEALTH CARE

(Thrust leader: Ramesh Harjani, University of Minnesota)

Analog and RF integrated circuit technology is the essential interface enabling the power, speed and miniaturization of modern digital microelectronics to be brought to bear on an array of medical issues, including medical imaging, patient monitoring, laboratory analyses, bio-sensing and new therapeutic devices. TxACE is working to identify and support analog circuit research challenges that have the potential to enable important health-related applications.

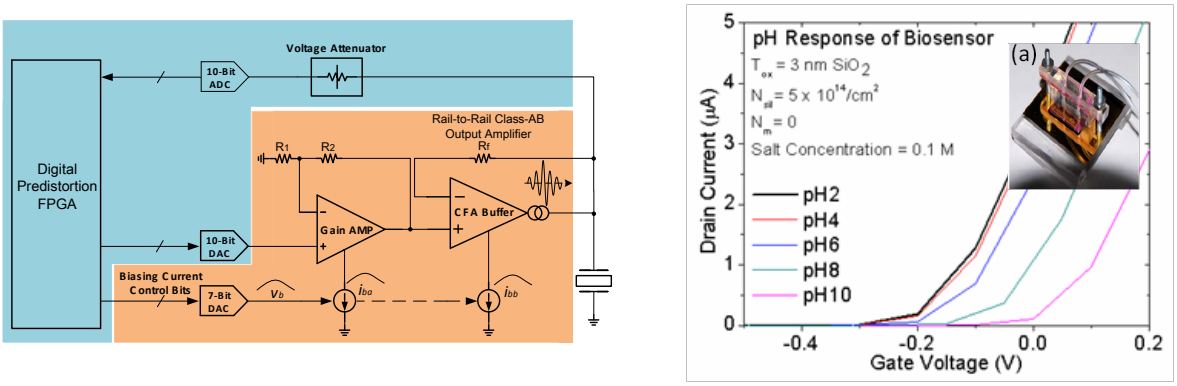


Figure 5: Digital pre-distortion technique is used to reduce the harmonic distortions by 20dB in a single-ended linear amplifier for ultrasound imaging (Gui, SMU)). (Left), SPICE simulated response of silicon nano-wire micro-fluidic biosensor to variation in pH (Vogel, Ga Tech) (Right).

ENERGY EFFICIENCY

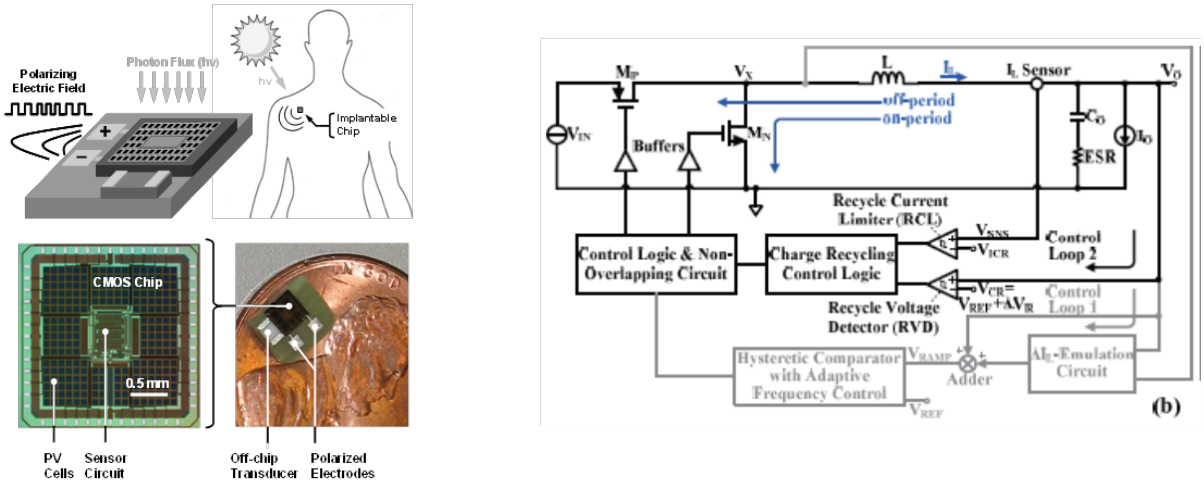


Figure 6: Photo voltaic for powering implanted devices, which is compatible to MRI unlike coil based devices (Hassibi, UT, Austin) (Left), Fast transient switching DC-DC converter for dynamic voltage scaling. 400 mA load transient, recovery times of 8 and 14 mS are achieved with 35 and 52 mV undershoot and overshoot voltages (Ma, UT, Dallas) (Right).

(Thrust leader: Dongsheng Brian Ma, UT Dallas)

TxACE is committed to alleviate the global energy problem by improving the energy efficiency of electronic systems as well as by developing analog technologies that can make energy generation more efficient. The Center is also working to energize and power long-lasting in-situ microscale devices such as wireless microsensors, biomedical implants, and portable microelectronics.

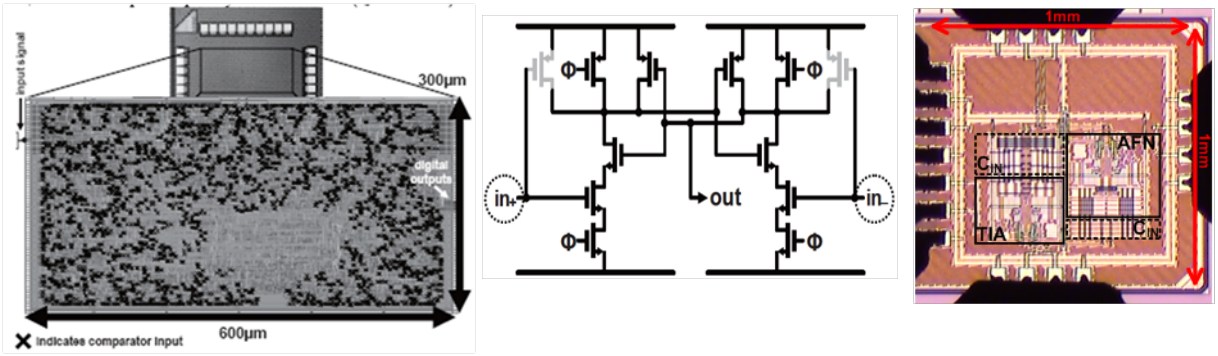


Figure 7: 5.5 ENOB Flash analog-to-digital converter (ADC) synthesized using a 90-nm standard digital library (Moon, Oregon SU) (Left), 3-input nand gate used to implement comparators in the ADC (Center), 10-MHz blocker robust transimpedance amplifier. Tolerant to ±10mA single tones at ≥50MHz, and to ±9mA tones at ≥40MHz for P1dB in-band (10uA, 6MHz) signal (Silva-Martinez, TAMU) (Right).

FUNDAMENTAL ANALOG CIRCUITS RESEARCH

(Thrust leader: David Allstot, University of Washington)

Research in this thrust focuses on cross-cutting areas in Analog Circuits which impact all of the TxACE application areas (Energy Efficiency, Health Care, Public Safety and Security).

Fundamental analog circuits' research is crucial for the design of analog-to-digital converters and communication links, the development of CAD tools, and testing of high speed circuits.

TXACE ANALOG RESEARCH FACILITY

The University of Texas at Dallas (UTD) has renovated a ~7500 ft^2 area on the 3rd floor of the Engineering and Computer Science North building to form an enhanced centralized group of laboratories dedicated to analog engineering research and research training. (Appendix I) The facility includes RF and THz, Integrated System Design, Embedded Signal Processing, and Analog & Mixed Signal laboratories as well as CAD/Design laboratory structured to promote collaborative research**.** The unique instrumentation capability includes network analysis and linearity measurements up to 325 GHz, spectrum analysis up to 20 THz, and cryo-measurements down to 2^{o}K. The close proximity of researchers in an open layout enables natural interaction and compels sharing of knowledge and instrumentation among the students and faculty. The TxACE analog research facility is one of the best equipped university based electronics laboratories in the state, and the RF and THz laboratory is one of the best in the world. The laboratory is available for use by TxACE researchers all over the world.

RESEARCH PROJECTS AND INVESTIGATORS

The Texas Analog Center is the largest university analog technology center in the world on the basis of funding and the number of principal investigators. Table 1 lists the names of the 67 principal investigators from 31 academic institutions with directed research tasks funded by TxACE. Seven schools (Rice, SMU, Texas A&M, Texas Tech, UNT, UT- Austin, UT-Dallas) are from the state of Texas. Nineteen are from outside of Texas. Three (Seoul National University, Korea, Cambridge University, Great Britain, Nui Maynooth, Ireland) are from outside of the US. Of the 67 investigators, 30 are from Texas. During the past year the center supported 80 PhD and 10 MS students, and 14 PhD and 7 MS degrees were awarded to TxACE students.

Investigator	Institution	Investigator	Institution	Investigator	Institution
David Allstot	U Washington	Arjang Hassibi	UT-Austin	Un-Ku Moon	Oregon State U
E. Alon	U Cal, Berkeley	Mona Hella	RPI	Boris Murmann	Stanford U
A. Apsel	Cornell	Rashaunda Henderson	UT-Dallas	Mukhopadhyay	Georgia Tech.
Bertan Bakkaloglu	Arizona State	Sebastian Hoyos	Texas A&M U	Won Namgoong	UT-Dallas
Poras Balsara	UT-Dallas	Roozbeh Jafari	UT-Dallas	Ken O	UT-Dallas
Bhaskar Banerjee	UT-Dallas	Aydin Ilker Karsilayan	Texas A&M U	Vojin Oklobdzija	NM State U.
Leonidas Bieris	UT-Dallas	Sayfe Kiaei	Arizona State	Sule Ozev	Arizona State
Andrew Blanchard	UT-Dallas	Chris Kim	U Minnesota	Sam Palermo	Texas A&M U
Burleson	U Mass	Jaeha Kim	Seoul Nat. U	Larry Pileggi	Carnegie Mellon U
Shawn Blanton	Carnegie Mellon	Peter Kinget	Columbia U	John Ringwood	National U of Ireland Naymooth
Joe Brewer	U Florida	Elias Kougianos	U North Texas	Elyse Rosenbaum	U Ill-Urbana-Champaign
Abhijit Chatterjee	Georgia Tech	Farinaz Koushanfar	Rice University	Jaijeet Roychowdhury	U Cal-Berkeley
Degang Chen	Iowa State U	Hoi Lee	UT-Dallas	M. Saquib	UT-Dallas
Frank De Lucia	Ohio State U	Changzhi Li	Texas Tech U	Naresh Shanbhag	U Ill-Urbana-Champaign
Jia Di	U Arkansas, Fayet.	Donald Lie	Texas Tech U	Michael Shur	RPI
Kamran Entesari	TAMU	Peng Li	Texas A&M U	Jose Silva-Martinez	Texas A&M U
Brian L. Evans	UT-Austin	Xin Li	Carnegie Mellon	V. Stojanovic	MIT
Brian Floyd	NC State U	Jin Liu	UT-Dallas	Murat Torlak	UT-Dallas
Randy Geiger	Iowa State U	Dongsheng Ma	U Arizona	Eric Vogel	UT-Dallas
Ranjit Gharpurey	UT- Austin	H.A. Mantooth	U Arkansas	Xi-Cheng Zhang	RPI
Ping Gui	Southern Methodist	Yiorgos Makris	UT-Dallas	Dian Zhou	UT-Dallas
Pavan K. Hanumolu	Oregon State U	Richard McMahon	Cambridge U		
Ramesh Harjani	U Minnesota	Saraju Mohanty	U North TX		

Table 1: Principal and Co-Principal Investigators of TxACE during reporting period

SUMMARIES OF RESEARCH PROJECTS

The 70 research projects funded through TxACE during 2010-2011 are listed in Table **2** below by Semiconductor Research Corporation task identification number.

Table 2: Funded research projects at TxACE by SRC task identification number
(FA: Fundamental Analog, EE: Energy Efficiency, HC: Healthcare, S&S: Safety and Security)

#	Task	Thrust	Task Title	PI	Institution
1	1836.003	FA	Temperature Compensated, High Common Mode Range, Cu-Trace Based Current Shunt Monitors	Bakkaloglu, Bertan	Arizona St
2	1836.004	FA	Robust Design of Low Power Small Area Data Converters in Low Voltage Digital Processes	Geiger, Randall	Iowa St
3	1836.006	FA	Multi-Core and Distributed Parallel Simulation for Design and Verification of Custom Digital and Analog ICs	Li, Peng	Texas A&M University
4	1836.008	S&S	Digital Assisted Millimeter-Wave CMOS Circuits	O, Kenneth	UT-Dallas
5	1836.013	FA	Wideband Receiver Architectures in Digital Deep Submicron CMOS	Hoyos, Sebastian	Texas A&M University
6	1836.017	EE	Performance-Oriented DVS-Compatible Single-Inductor Multiple-Output Power Converters	Ma, Brian	UT-Dallas
7	1836.018	EE	Transistor Sizing and Voltage Scaling for Minimal Energy at Fixed Performance	Oklobdzija, Vojin	UT-Dallas
8	1836.019	FA	Digitally-Enhanced Energy-Efficient High-Speed I/O Links	Shanbhag, Naresh	U of Illinois Urbana-Champaign
9	1836.020	FA	Low-Complexity High-Performance Analog-to-Digital Converters in Submicron CMOS	Moon, Un-Ku	Oregon St
10	1836.021	FA	CAD Algorithms and Tools for Fast and Accurate PLL Design in the Presence of Variability	Roychowdhury, Jaijeet	U of California-Berkeley
11	1836.022	FA	High-Speed MIMO Signaling Techniques for Single-Ended Parallel I/O	Harjani, Ramesh	U of Minnesota
12	1836.028	FA	Tools and Algorithms for Behavioral Model Generation of Analog/Mixed-Signal Circuits	Mantooth, Homer Alan	Arkansas
13	1836.030	FA	Fast PVT-Tolerant Physical Design of RF IC Components	Mohanty, Saraju	U North Texas
14	1836.031	FA	Variation Tolerant Analog Design based on Generalized Kharitonov/Lyapunov Theory	Zhou, Dian	UT-Dallas
15	1836.032	S&S	Millimeter Wave Phase-Locked Loop Design with Enhanced Tolerance to Process and Temperature Variation	Gharpurey, Ranjit	UT-Austin
16	1836.033	S&S	MIMO Radar for Pixel Reduction in mm-Wave Imaging	Saquib, Mohammad	UT-Dallas
17	1836.034	S&S	77-81 GHz CMOS Transceiver with Built-In Self Test and Healing	Banerjee, Bhaskar	UT-Dallas
18	1836.035	S&S	Development of CMOS Sub-Terahertz Receivers for Spectrometers	Banerjee, Bhaskar	UT-Dallas
19	1836.036	S&S	Signal Generation for 200-300 GHz Spectrometer	O, Kenneth	UT-Dallas
20	1836.037	S&S	Development of Antenna and Chip Interface Systems for Millimeter Wave and Sub-Millimeter Wave Applications	Henderson, Rashaunda	UT-Dallas
21	1836.038	FA	A Hybrid 14-bit Analog-to-Digital Converter for Broadband Applications	Silva-Martinez, Jose	Texas A&M University
22	1836.039	S&S	UxIDs: Unclonable Mixed-Signal Integrated Circuits Identification	Koushanfar, Farinaz	Rice University
23	1836.040	FA	Energy-Efficient CMOS 10GS/s 6-bit ADC with Embedded Equalization	Palermo, Sam	Texas A&M University

Table 2: continued

#	Task	Thrust	Task Title	PI	Institution
24	1836.041	EE	A High-Efficiency Single-Inductor Multiple-Input Multiple-Output Integrated DC/DC Converter for Energy-Harvesting Applications	Lee, Hoi	UT-Dallas
25	1836.042	HC	Adaptive Data Prediction Based Receiver for Power-Efficient High-Resolution Ultrasound Imaging Systems	Ma, Brian	UT-Dallas
26	1836.043	HC	High-Voltage Amplifier Technology	Gui, Ping	Southern Methodist
27	1836.044	FA	Statistical Models and Methods for Design and Test of Non-Digital Components	Li, Xin	Carnegie Mellon
28	1836.045	S&S	Frequency Channelized ADC for Wide Bandwidth Systems	Namgoong, Won	UT-Dallas
29	1836.046	FA	Reconfigurable Antenna Interface for Low-Power Wireless Sensor Nodes	Allstot, David	U of Washington
30	1836.047	S&S	Integration of Millimeter Wave Antennas Using System in Package Techniques	Henderson, Rashaunda	UT-Dallas
31	1836.048	S&S	Millimeter and Submillimeter Gas Sensors: System Architectures for CMOS Devices	De Lucia, Frank	Ohio State
32	1836.052	HC	An Ultra-low Power Signal Processing with Smart Analog-enabled Pre-Conditioning Stage for Inertial Sensing Applications	Jafari, R.& Namgoong, W.	UT-Dallas
33	1836.053	EE	High-Efficiency Highly-Integrated LED Driver Systems for Solid-State Lighting Applications	Lee, Hoi & Zhou, Dian	UT-Dallas
34	1836.054	S&S	Silicon Based Beamforming Arrays for Millimeter Wave Systems	Torlak, Murat	UT-Dallas
35	1836.055	HC	SPICE Models and Analog Circuits for Nanoscale Silicon Chemical- and Biological-Sensors	Vogel, Eric	UT-Dallas
36	1836.057	FA	High Accuracy All-CMOS Temperature Sensor with Low-Voltage Low-Power Subthreshold MOSFETs Front-End and Performance-Enhancement Techniques	Li, Changzhi	Texas Tech University
37	1836.058	FA	Hierarchical Model Checking for practical Analog/Mixed-Signal Design Verification	Li, Peng	Texas A&M University
38	1836.059	FA	Power-Efficient 10-20GS/s ADCs for High-Speed Communications	Liu, Jin	UT-Dallas
39	1836.060	FA	Design Techniques for Scalable, Sub-1mW/Gbps Serial I/O Transceivers	Palermo, Sam	Texas A&M University
40	1836.061	HC	Analog Computing in Human Cells	Bleris, Leonidas	UT-Dallas
41	1836.062	EE	System-Level Models and Design of Power Delivery networks with On-Chip Voltage Regulators	Li, Peng	Texas A&M University
42	1836.063	EE	Power line Communications for Enabling Smart Grid Applications	Evans, Brian	UT-Austin
43	1836.064	HC	Ultra-Low-Power Analog Front-End IC Design for Implantable Cardioverter Defibrillator	Lie, Donald	Texas Tech University
44	1836.065	FA	Energy Efficient Comparator Elements for A/D Converters and High-Speed I/Os	V. Stajanovic	MIT
45	1836.066	HC	A Fully-Integrated CMOS Platform for Microwave-Based Label-Free DNA Sensing	Entesari, Kamran	Texas A&M University
46	1836.067	S&S	Characterization of CMOS Basic Building Blocks for Sub-THz Wideband Transmitters	Hella, Mona	Rensselaer Polytechnic
47	1836.068	FA	Global Convergence Analysis of Mixed-Signal Systems	Kim, Jaeha	Seoul National University
48	1836.069	EE	Electronic Systems for Small-Scale Wind Turbines	McMahon, Richard	Cambridge University

Table 2: continued

#	Task	Thrust	Task Title	PI	Institution
49	1836.070	EE	Optimum Control of Power converters	Ringwood, John	National U of Ireland Naymooth
50	1836.071	EE	Design of Photovoltaic (PV) Power Harvesting CMOS ICs	Hassibi, Arjang	UT-Austin
51	1836.072	FA	Low Cost Test of High Speed Signals	Chatterjee, Abhijit	GA Tech
52	1836.073	FA	Coverage and Test Methodology	Makris, Yiorgos	UT-Dallas
53	1836.074	S&S	Sub-45nm Circuits for True Random Number Generation and Chip Identification	Burleson	U Mass
54	1836.075	FA	Design of 3D Integrated Heterogeneous Systems	Mukhopadhyay	GA Tech
55	1836.076	EE	Ultra-Low Power Delay-Insensitive Asynchronous Circuits	Di	U Arkansas/ Fayet
56	1836.077	FA	Statistical Characterization of Circuit Aging	Chris Kim	U Minnesota
57	1836.078	FA	High-Resolution, Charge-Based A/D Converters for Nano-CMOS Technologies	Boris Murmann	Stanford
58	1836.079	S&S	CMOS THz Generation and Detection	Mona Hella	RPI
59	1836.080	FA	Variation-Tolerant Noise-Shaping ADCs With Embedded Digital Bias and V(DD) Scalable from 0.5V to 1.2V for Nanoscale CMOS	Peter Kinget	Columbia
60	1836.081	EE	Combined Inductive/Capacitive DC-DC Converter for Efficient Dynamic Voltage Scaling	Ramesh Harjani	U Minnesota
61	1836.082	S&S	Low-Cost Energy-Efficient 60GHz Transceivers with Built-In Test (BIST)	E. Alon	U Cal-Berkeley
62	1836.083	S&S	Built-In Test for Millimeter-Wave Phased Arrays	Brian Floyd	NCSU
63	1836.084	FA	Analog, Mixed-Signal and RF/High Speed Test	Sule Ozev	Ariz. SU
64	1836.085	FA	CMOS Switched-Capacitor Power Amplifier Techniques	David Allstot	U Washington
65	1836.086	FA	Variation Tolerant Calibration Circuits for High Performance I/O	A. Apsel	Cornell
66	1836.087	FA	An Anyrate Reference-less Digital Clock-Data-Recover (CDR) with Decoupled Jitter Transfer and Jitter Tolerance Bandwidths	Ping Gui	SMU
67	1836.088	EE	Efficient Digital-Intensive Wireless Transmitters Utilizing Switching Mode PAs	Ranjit Gharpurey	UT- Austin
68	1836.089	EE	Energy Efficient Comparator Elements for A/D Converters and High-Speed I/Os	Vojin Oklobdjiza	NM SU
69	1836.090	EE	Digitally-Enhanced Clocking Strategies to Improve Energy-Efficiency of Serial Links	Pavan Hanumolu	Oregon SU
70	1836.091	FA	High-Data Rate Low-Cost Dielectric Waveguide Interconnects on Flexible Plastic Substrates	Deji Akinwande	UT-Austin

ACCOMPLISHMENTS

TxACE has made significant research progress. Table 3 lists the major research accomplishments for the center during September 1st of 2010 to August 31st of 2011, while Table 5 summarizes the number of publications and inventions resulting from TxACE research during the period. The TxACE researchers have published 68 conference papers and 24 journal papers. They have also made 5 invention disclosures and filed 2 patents. The list of publications are included as Appendix II. Following the tabulation, brief summaries of each project are provided.

Table 3: Major TxACE Research Accomplishments (September 2010 through August 2011)

Category	Accomplishment
Circuits (Health Care)	Constructed recombinant proteins that can transduce endogenous information outside of a cell. These recombinant proteins "carry" tags that can be identified from a BioFET. (1836.061, PI: L. Bleris, University of Texas at Dallas)
Circuits (Health Care)	A granular decision making approach has been proposed. It reduces the microcontroller (MCU) active cycle to 25.2% resulting in 78.2% reduction in power consumption. This configuration could maintain 99.0% sensitivity on the test data. (1836.052, PI: R. Jafari & W. Namgoong, University of Texas at Dallas)
Circuits (Health Care)	Demonstrated a fully-differential high-voltage (HV) linear amplifier using TI's 0.7 µm LBCSOI 120 V technology to achieve a signal swing of 180 V and extremely low HD2 (< - 58 dB). (1836.043, PI: P Gui, Southern Methodist University)
Circuits (Health Care)	Developed a SPICE Macromodel of Field-Effect-Transistor based nanoscale silicon biological sensors. (1836.055, Eric Vogel, University of Texas, Dallas)
Circuits (Health Care)	Demonstrated the first in-vitro photo-voltaic driven CMOS implanted MRI compatible electrocardiography sensor. (1836.071, PI: A. Hassibi, University of Texas, Austin)
Circuits (Safety and Security)	Demonstrated key building blocks for a 400-GHz phase locked loop along with a 560-GHz signal generation circuit, both in 45-nm CMOS. (1836.036, PI: K. O, Univ. Texas, Dallas)
Circuits (Safety and Security)	Demonstrated a Physically Unclonable Function (PUF) circuit in 45nm CMOS, and characterized a True Random Number Generator (TRNG) circuit over process variation. (1836.074, PI: W. Burleson, Univ. Massachusetts)
Circuits (Safety & Secu.)	Demonstrated a compact (200 μm^2) Schottky Diode detector for measurements of voltages at 70-110 GHz using DC measurements (1836.008-1836.010, Kenneth K. O, University of Texas, Dallas)
Circuits (Safety & Secu.)	Applied MMSE and Space time block coding in mm-wave imaging to reduce receiver complexity and to mitigate the interference among transmitted signals, respectively (1836.033, Mohammad Saquib, University of Texas, Dallas)
Circuits (Energy Efficiency)	Developed a physical-statistical model of asynchronous impulsive noise in power line communication (PLC) networks. Noise mitigation: proposed two non-parametric algorithms for impulsive noise mitigation in OFDM PLC systems. (1836.063, PI: Brian L. Evans, Univ. of Texas at Austin)
Circuits (Energy Efficiency)	Demonstrated fully integrated parallel inductive and capacitive DC-DC converters with a 450X output range: ~60% efficiency from 1 mA to 50 mA, ~70% efficiency 100 mA to 300 mA output current (1836.081, PI: R. Harjani, University of Minnesota).
CAD (Energy Efficiency)	Developed a fast simulation engine where large on-chip power grids are analyzed efficiently using a fast GPU-based iterative algorithm while active LDO and package circuitries are processed on a CPU. (1836.062, PI: P. Li, Texas A&M University)

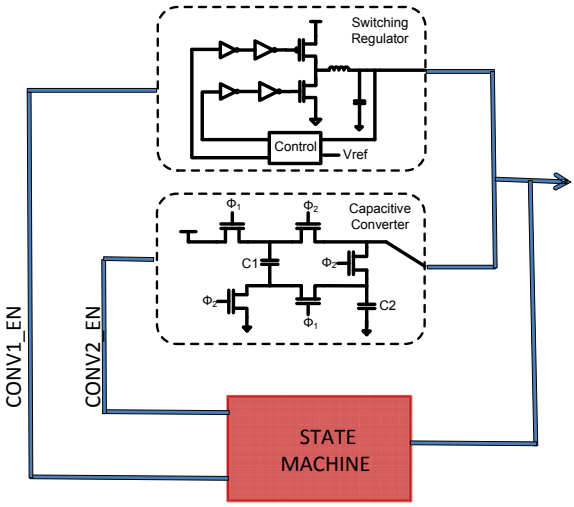
Table 4: Major TxACE Research Accomplishments (September 2010 through August 2011)

Category	Accomplishment
Circuits (Fund. Analog)	Demonstrated a temperature sensor front end that can operate at V_{DD}=0.4 V using a MOS transistors biased in sub-threshold and a bulk driven OpAmp. (1836.057, PI: C. Li, Texas Tech University)
CAD (Fund. Analog)	Developed a unified statistical analysis engine for SRAM performance, yield, reliability and testability. Using a novel Gibbs sampling algorithm, accuracy and speed of SRAM statistical analyses were improved by 3~10X. (1836.044, PI: Xin Li)
Circuits (Fund. Analog)	Demonstrated MIMO Cross talk cancellation in a 9Gb/S link by improving vertical and horizontal eye opening by 29% (mV) and 32% (UI), respectively (1836.022, Ramesh Harjani, University of Minnesota)
Circuits (Fund. Analog)	Demonstrated a flash ADC synthesized with a digital flow that achieves 35 dB SNDR with 1 MHz input up to sampling rate of 210 MSPS (1836.020, PI: U. Moon, Oregon State University)
Circuits (Fund. Analog)	Demonstrated a transimpedance amplifier with an active feedback network that can tolerate 10-mA blocker at 50 MHz. (1836.038, PI: Jose Silva-Martinez, Texas A&M)
Test (Fund. Analog)	Developed a new ADC spectral testing algorithm that achieves accurate spectral testing using available INL test results and proper signal processing. (1836.004, PI: R. Geiger, Iowa State University)

Table 5: TxACE number of publications during the reporting period

Conference Papers	Journal Papers	Invention Disclosures	Patents Filed
68	24	5	2

Energy Efficiency Thrust



Summary of Accomplishments

Circuits	High efficiency over a 450x output power range; Automated mode switching depending on the load current; Passive supply resonance reduction technique; Resonance reduction circuitry implemented underneath the bond pad. (1836.081, PI: Ramesh Harjani, University of Minnesota)
Circuits	Designed and developed a power amplifier with variable output power without the use of a supply voltage modulator based on efficient switch-based PA architecture and switched-capacitor circuits. (1836.085, PI: David Allstot, University of Washington)
Circuits (Energy Efficiency)	Developed a physical-statistical model of asynchronous impulsive noise in power line communication (PLC) networks. Noise mitigation: proposed two non-parametric algorithms for impulsive noise mitigation in OFDM PLC systems. (1836.063, PI: Brian L. Evans, Univ. of Texas at Austin)
CAD (Energy Efficiency)	Developed a fast simulation engine where large on-chip power grids are analyzed efficiently using a fast GPU-based iterative algorithm while active LDO and package circuitries are processed on the CPU. (1836.062, PI: P. Li, Texas A&M University)

TASK 1836.003, TEMP. COMPENSATED, HIGH COMMON MODE RANGE, CU-TRACE BASED CURRENT SHUNT MONITOR AMPLIFIER

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SAYFE KIAEI, ARIZONA STATE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

A current shunt monitor that accurately amplifies small voltages typically around 10mV in the presence of large common-mode voltage up to 26V is presented. The design has done in 0.7um CMOS process with less than 10uV of input offset and 1uV/$\sqrt[2]{Hz}$ of flicker noise. CMRR over 120dB is also achieved.

TECHNICAL APPROACH

Instead of using external sensing resistor in the current path, existing PCB Cu-trace is used as sensing resistors for cost reduction by eliminating external components in mass production. Better internal resistive matching and equal resistance variation over all the process corners and temperatures achieved by designing Input sensing (R_S) and gain (R_G) resistors in ratio, $\frac{R_G}{R_S} = 50$. A switching current mode FIR filter is used to cancel chopping ripples in current domain instead of using conventional voltage mode ripple reduction techniques that require extra current to voltage conversion step which could be a source of incurring noise.

SUMMARY OF RESULTS

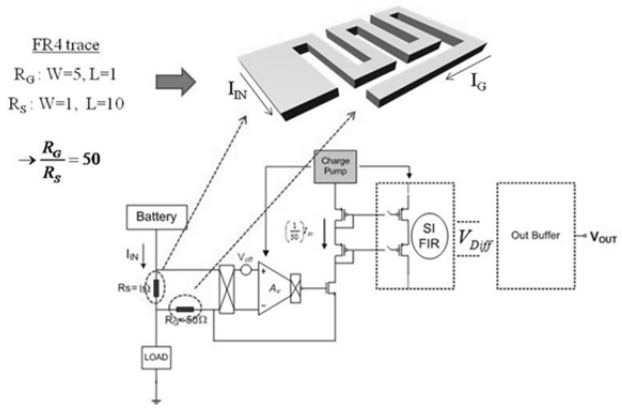

Figure 1: Matched input resistors on an FR4 trace.

The patterning of proposed Cu-Trace resistors is shown in Figure 1. Input chopping technique is applied to fulfill less than 10uV of input offset requirement. Since chopping technique brings out trade-offs such as ripples due to the switching, there needs to be a function that can suppress down the ripples at every chopping frequency. A switching current mode FIR filter which samples and averages the two different phase chopped input signals while reducing the chopping ripples with its first order hold sinc^2 function is implemented. The switching current mode (SI) FIR filter not only reduce down the ripple by its second order notching mechanism, but also recovers original offset-free DC input current by averaging the offset-containing input signals. The following first order hold sinc^2 function as in eq. (1) is realized in the circuit in Figure 2.

$$\left|\frac{1-e^{-sT}}{s}\right|^2 = T\frac{\left|sin\left(\frac{wT}{2}\right)\right|^2}{\left|\frac{wT}{2}\right|^2} = Tsinc^2\left(\frac{wT}{2}\right) \quad (1)$$

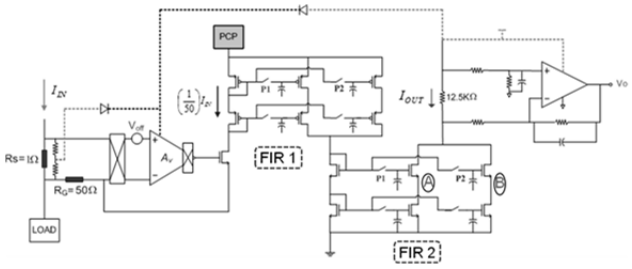

Figure 2: Detailed diagram of first order hold sinc^2 FIR.

Overall, the presented instrumentation amplifier has clear rail to rail operation with less than 10uV input referred offset and CMRR of 120 dB. The device has been fabricated with 0.7 um AMIS (ON Semiconductor) I2T100 process.

Keywords: Choppers, Current sensing, Instrumentation amplifier, operational amplifier, ripple/residue reduction

INDUSTRY INTERACTIONS

Texas Instruments Tucson HPA (High Performance Analog) group work closely with ASU scientists

MAJOR PAPERS/PATENTS

[1] H.S. Yeom, B. Bakkaloglu, "High Common Mode Range, Cu-Trace Based Current Shunt Monitor Amplifier," (Invited) SRC 2010 TECHCON, September, 2010, Austin, Texas.

[2] H. S. Yeom and B. Bakkaloglu, "0V-30V Common Mode Range, 120dB CMRR, and 10nV/$\sqrt{Hz}$ Noise Floor CSM IC with an Embedded ΣΔ Frequency Modulated Digital Output Interface ADC Block," *Journal of Analog Integrated Circuits and Signal Processing* (Accepted)

TASK 1836.062, SYSTEM-LEVEL MODELS AND DESIGN OF POWER DELIVERY NETWORKS WITH ON-CHIP VOLTAGE REGULATORS

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SIGNIFICANCE AND OBJECTIVES

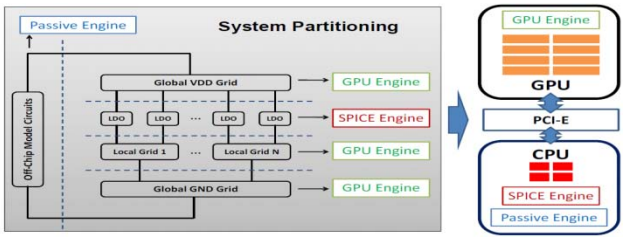
The design of power delivery networks (PNDs) is a key avenue and a challenge for achieving power efficiency. We develop models and holistic system-level design strategies to achieve the optimal PDN system performance trade-offs, and facilitate joint design optimization of on-chip voltage regulators and passive on-die power grids.

TECHNICAL APPROACH

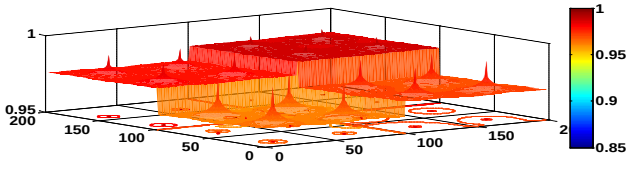
To enable efficient design space exploration for large PDNs with multiple integrated voltage regulators, system-oriented design models and a simulation engine are being developed. More detailed system design will be facilitated via a simulation-based optimization framework aided by our models and simulation engine. Holistic design methodologies will be developed to co-optimize active voltage regulators and passive on-chip power grids, which is critical for achieving the best system-level design tradeoffs between supply noise, power efficiency, area overhead and stability.

SUMMARY OF RESULTS

Simulating a large PDN is a daunting task due to the sheer complexity. We developed a fast simulation engine where large on-chip power grids are analyzed efficiently using a fast GPU-based iterative algorithm while active LDO and package circuitries are processed on the CPU.



(a)



(b)

Figure 1: (a) GPU-accelerated simulation engine, (b) simulated supply voltage for a four-domain PDN w/ 16 integrated LDOs.

The simulation engine is illustrated in Figure 1 (a) and the simulated supply voltage for a large PDN with four voltage domain is shown in Figure 1 (b).

Using our simulation infrastructure, we are currently developing a system-level design framework for optimizing PDNs with multiple integrated voltage regulators (e.g. LDOs). Under a limited setting, Figure 2 illustrates how the integration of LDOs may lead to tradeoffs between supply noise (voltage droop) and power efficiency. In this case, only the number of integrated LDOs is considered as a design variable. Clearly, integration of LDOs does lead to suppression of supply noise. Equally important, tradeoffs between supply noise and power efficiency shall be systematically considered and optimized.

Our framework will ultimately allow us to jointly optimize both the passive power grids and the active voltage regulators under the same network setting; it will also make it possible to achieve the best design tradeoffs between key system design specifications including supply noise, power efficiency, silicon area and stability.

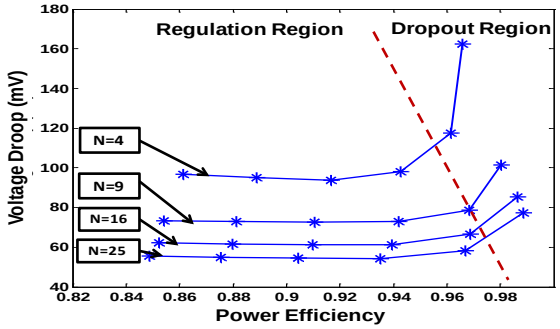


Figure 2: Design tradeoffs as functions of number of LDOs.

Keywords: power delivery, on-chip voltage regulation.

INDUSTRY INTERACTIONS

IBM and AMD.

MAJOR PAPERS/PATENTS

[1] Z. Zeng et al, "IC Power Delivery: Voltage Regulation, Conversion and System-Level Co-Optimization," IEEE TVLSI, 2011 (submitted).

[2] S. Lai et al, "A Fully On-Chip Area-Efficient CMOS Low-Dropout Regulator with Fast Load Regulation, Analog IC and Signal Processing, 2011 (submitted).

TASK 1836.063, POWERLINE COMMUNICATION FOR ENABLING SMART GRID APPLICATIONS

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SIGNIFICANCE AND OBJECTIVES

Within a smart grid, we seek to enable higher data rate monitoring and controlling applications for making homes and small businesses more efficient in their use of energy. We focus on the "last mile" of power delivery from a concentrator to its local area subscribers along medium-voltage and low-voltage lines.

TECHNICAL APPROACH

We develop adaptive methods and prototypes to enhance data rates in PLC networks. To enable our adaptive methods, we characterize the powerline channels and noise statistics based on the properties of the PLC networks and the measured data. We propose learning-based non-parametric algorithms to mitigate impulsive noise in Orthogonal Frequency-Division Multiplexing (OFDM) PLC systems. To evaluate the transceiver algorithms in performance vs. complexity tradeoffs, we implement a single-channel PLC prototype. The methods and prototype will be extended to a multi-channel PLC system, exploiting the diversity from three phases on low-voltage lines and three copper wires in the inhome power systems.

SUMMARY OF RESULTS

Asynchronous impulsive noise limits communication performance in powerline communication (PLC). We derive a canonical statistical-physical model of the instantaneous statistics of asynchronous noise based on the physical properties of the PLC network, and validate the distribution using simulated and measured PLC noise data. The results can be used to analyze and mitigate the effect of the asynchronous noise on PLC systems.

In OFDM PLC systems, the fast Fourier transform (FFT) at the receiver spreads out the energy of impulsive noise across all subcarriers. We apply sparse Bayesian learning techniques to estimate and mitigate impulsive noise in OFDM systems without the need for training. We propose two nonparametric iterative algorithms, which do not assume any statistical impulsive noise models. The first algorithm estimates impulsive noise by its projection onto null and pilot tones; the second algorithm jointly estimate the OFDM symbol and impulsive noise utilizing information on all tones. In our simulations, the estimators achieve 5dB and 10dB SNR gains in communication performance respectively, compared to conventional OFDM receivers.

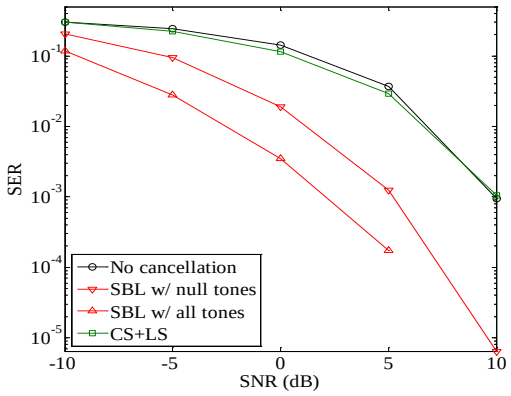

Figure 1: Symbol error rate (SER) vs. signal-to-noise ratio (SNR) for the conventional OFDM receiver (no cancellation), our non-parametric sparse Bayesian learning (SBL) methods, and a reference algorithm using compressive sensing and least squares estimation (CS+LS).

We implement a 1x1 OFDM PLC prototype. It includes a software package running transceiver algorithms on National Instruments (NI) embedded computers, and an analog front-end (AFE) interface connecting the NI hardware with Texas Instruments PLC AFE.

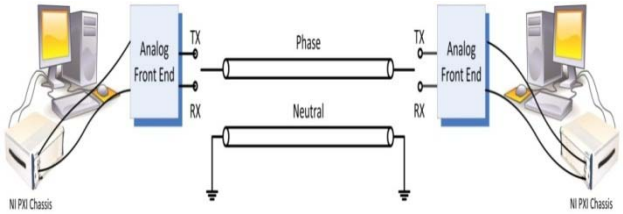

Figure 2: A 1x1 OFDM PLC prototype.

Keywords: Powerline communication, smart grid, impulsive noise, OFDM, prototype.

INDUSTRY INTERACTIONS

Texas Instruments, Freescale, IBM

MAJOR PAPERS/PATENTS

[1] M. Nassar et al, "Statistical Modeling of Asynchronous Impulsive Noise in Powerline Communication Networks", IEEE Globecom 2011.

[2] J. Lin et al, "Non-Parametric Impulsive Noise Mitigation in OFDM Systems Using Sparse Bayesian Learning", IEEE Globecom 2011.

TASK 1836.069, WIND TURBINE EMULATOR FOR TESTING OF SMALL-SCALE WIND GENERATORS AND ASSOCIATED POWER ELECTRONICS

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MARK TATLOW, UNIVERSITY OF CAMBRIDGE, MRT39@CAM.AC.UK

SIGNIFICANCE AND OBJECTIVES

Wind power is an attractive renewable energy resource. This project focuses on improving the performance of domestic-scale wind turbines. The first step is developing a wind turbine emulator rig to enable new designs to be tested in a controlled and reproducible way.

TECHNICAL APPROACH

Modeling of the emulator rig was done in MATLAB/Simulink and specifications for the rig were developed based on the simulations. The model was designed to follow a torque-speed curve of a real turbine for particular wind speeds. The model takes in turbine parameters (blade radius, inertia), wind speed and generator torque to determine the shaft rotational speed. The setup consisted of a permanent magnet (PM) machine and commercial converter as the prime mover (wind turbine) coupled to a commercial PM generator. A buck-boost converter controlled the amount of power (torque) taken out of the generator.

SUMMARY OF RESULTS

Following construction of the rig, testing of the emulator is now in progress. The emulator is controlled to follow the torque-speed curve of a real-life wind turbine for a particular wind speed.

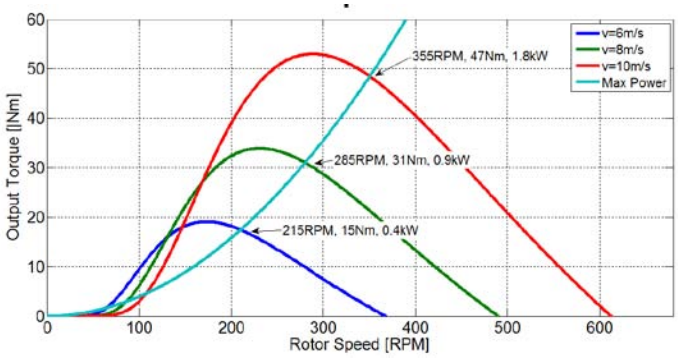

Figure 1 Rotor speed vs. generator torque for varying wind speeds

The experimental results show the operation of the emulator for a 6 m/s (13 mph). These results match the simulated results thus proving that the test-rig can simulate a real wind turbine's static and dynamic conditions over a range of wind speed.

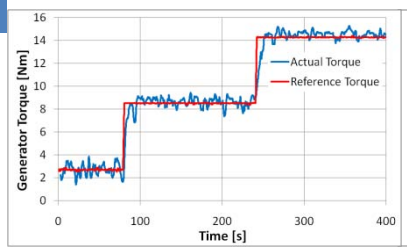

Figure 2 Generator torque

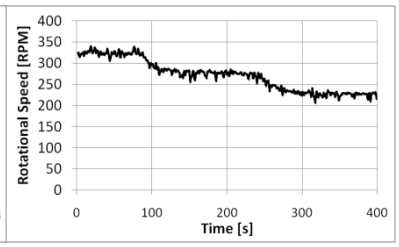

Figure 3 Rotational speed

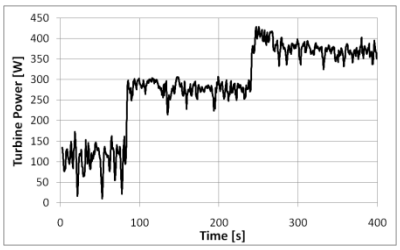

Figure 1 Output power

Fig. 1 and Fig. 4 show that when the generator torque is 15 Nm (between 250-400s), maximum power (380W) is being taken out of the system and this corresponds to the maximum power point.

Further testing of the emulator will include testing the rig over the entire wind speed range from 3-10m/s (7–22mph). Investigating and implementing maximum power point tracking algorithms and testing the generator under "gusty" wind conditions

In the second and third year of the project, sensorless control strategies will be investigated and implemented with the aim of reducing cost and improving efficiency. These will be evaluated on the test rig. Considerations of real-life prospects for the system will be then be investigated and opportunities for TI devices identified.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Wasynizuk, Man, Sullivan., **"***Dynamic behaviour of a class of wind turbine generators during random wind fluctuations,"* IEEE Transactions on Power Apparatus and Systems, Vol. PAS-lOO, No. 6, pp. 2837-2845.

[2] Morren, Pierik, De Haan**.,** **"***Inertial Response of Variable Speed Wind Turbines."* 2006, Electrical Power Systems Research 76, pp. 980-987.

TASK 1836.070, OPTIMUM CONTROL OF POWER CONVERTERS

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SIGNIFICANCE AND OBJECTIVES

Transformer primary-side sensing control for a flyback converter has been investigated, but to date no research has been put into extending this control strategy for the system operating at both continuous and discontinuous modes. The project aims to maximize the flyback converter efficiency at all loads using the primary-side sensing approach.

TECHNICAL APPROACH

The accuracy of the primary-sensing method largely depends on the sampling instant and the voltage drop in transformer windings, which is a function of parasictic components and operating conditions. To achieve precise output voltage regulation at all loads, an adaptive estimation algorithm is suggested to track the output voltage variation from indirect measurements. Based on this estimated signal, along with the input voltage and the primary current, the optimization block calculates the optimal switching frequency which minimizes the power loss in the flyback converter. The controller is implemented using digital current mode control.

SUMMARY OF RESULTS

The controller for a wide load range flyback converter is illustrated in figure 1. The key factor, which decides the performance of the system, is the adaptive compensation scheme and the online optimization procedure used in the adaptive observer and efficiency optimization block respectively.

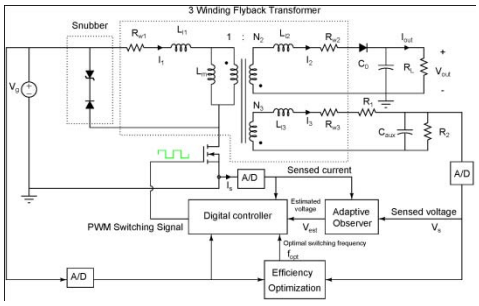

Figure 1: Block diagram of the primary-side sensing control for a flyback converter. The adaptive observer block is utilized to dynamically compensate for the voltage drop under load variation, while the efficiency optimization block suggests the switching frequency from the estimation system losses.

In observer theory, an accurate observation requires complete information of the transformer model. Though different models have been suggested to analyze the primary-sensing error for the flyback converter, there is little information on how to precisely extract the component values from a practical flyback transformer. Therefore, our initial studies focus on the transformer parameter extraction using system identification methods. The complete transformer model and a simplified version for observer design are shown in figure 2.

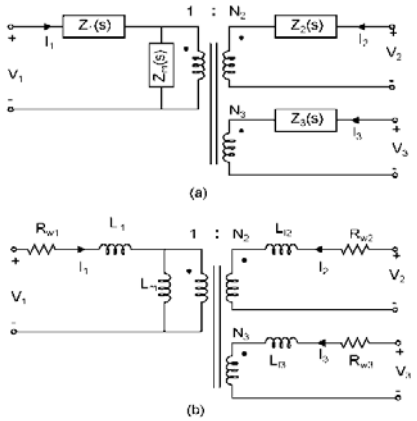

Figure 2: (a) Complete model of 3-winding flyback transformer (b) Simplified model for observer design.

In the second and third years, the main tasks of the project are on the implementation of the suggested controller using the evaluation flyback converter kit and verifying the simulation and experimental results. Besides that, a theoretical investigation on the stability of the observer and closed-loop system under different operating conditions is necessary. An extension of the observer technique to other converter configurations (e.g. forward type, etc) will also be considered.

Keywords: Primary-sensing technique, flyback, power converter, efficiency, optimization.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

TASK 1836.081, COMBINED INDUCTIVE/CAPACITIVE DC-DC CONVERTER

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SIGNIFICANCE AND OBJECTIVES

This research aims to build highly efficient converters which can support very wide output power range. The main application of such a converter is to power multiple power domains with DVS, demanding fully integrated implementation. Hence, reduction of area occupied by the converter is another goal of this project.

TECHNICAL APPROACH

Different converter architectures are suitable for different regions of operation. Inductive switching converters are highly efficient at higher output powers whereas capacitive converter have been shown to be efficient at lower output powers. Combining the two converter architectures in a single implementation can support wide output power range achieving a high efficiency. In order to conserve area the passive components are reused among the parallel converters. Also implementation digital circuitry beneath the inductor of the converter will increase the area efficiency.

SUMMARY OF RESULTS

Different converter architectures were surveyed and a parallel converter architecture was selected for implementation to achieve the goal of high efficiency over a wide output power range.

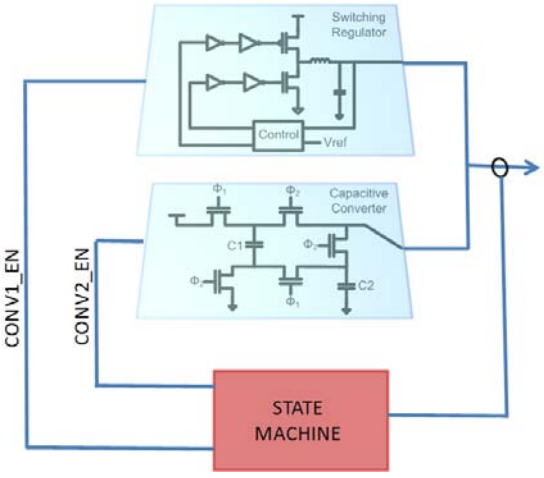

Figure 1: Parallel converter architecture

The converter architecture comprises of inductive switching converter in parallel with a capacitive converter as shown in Figure 1. The inductive switching converter supports the higher power range whereas the capacitive converter is operational for lower powers, which in-turn has additional modes of operation. A state machine selects the appropriate controller based on the power demand of the load, while completely turning off the other. The theoretical efficiency of such a converter for 32nm implementation is shown in Figure 2.

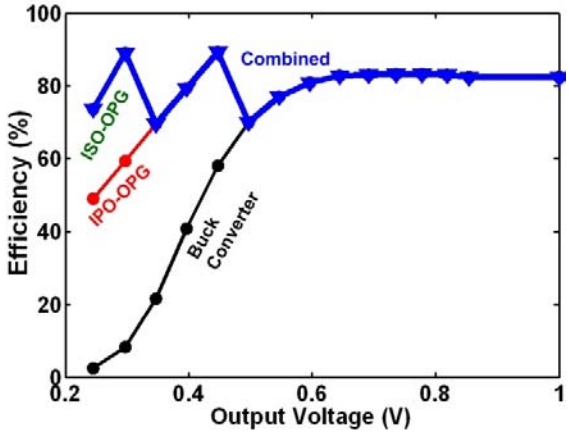

Figure 2: Theoretical expected efficiency of the parallel converter architecture

In order to achieve area efficiency the passive components of the converter can be shared between the two converters. Area efficiency can be further increased by implementing digital circuitry underneath the inductor, feasibility of which has been shown using a test-chip implemented in 130nm CMOS technology [2].

We have already demonstrated switching inductive fully integrated converter [1][3].

Keywords: parallel converter, switching inductive converter, capacitive converter.

INDUSTRY INTERACTIONS

Intel, IBM and Freescale

MAJOR PAPERS/PATENTS

[1] S. S. Kudva and R. Harjani, “Inductors above digital circuits: towards compact on-chip switching regulator,” Techcon 2010.

[2] S. S. Kudva and R. Harjani, “Fully integrated on-chip DC-DC converter with a 450x output range,” IEEE Custom Integrated Circuits Conference, September 2011.

[3] S. S. Kudva and R. Harjani, “Fully integrated on-chip DC-DC converter with a 450x output range,” (Invited) To appear in IEEE Journal of Solid-State Circuits, August 2011.

TASK 1836.085, CMOS SWITCHED-CAPACITOR POWER AMPLIFIER TECHNIQUES

PROF. DAVID ALLSTOT, THE UNIVERSITY OF WASHINGTON AT SEATTLE, ALLSTOT@UW.EDU

SIGNIFICANCE AND OBJECTIVES

CMOS power amplifiers have been demonstrated and used in mobile communication systems. However, most of the conventional CMOS PAs have limited efficiency for a modulated signal with a high peak-to-average ratio (PAR). The switched-capacitor power amplifier (SCPA) topology has been developed to provide higher efficiency in high-PAR applications. This project will develop a high power SCPA using a transformer-based power combiner.

TECHNICAL APPROACH

The inefficiency when amplifying non-constant (non-CE) envelope signals happens because the PA achieves peak efficiency only when operated at its saturated output power level; moreover, the efficiency decreases quadratically with reduced output voltage. Hence, it is desirable to operate the PA as close to saturation as possible. To this end, many efforts have been made to enable the use of switching amplifier topologies using external linearization methods such as envelope elimination and restoration (EER). Recently, a technique that utilizes an SCPA with an EER method has shown promise in achieving high-efficiency simultaneously with moderately high output power. To provide higher output power, an SCPA topology with a transformer-based power combining is being utilized and developed.

SUMMARY OF RESULTS

A SCPA using a four-way power-combining technique, shown in Figure 1, is implemented so that it can be configured in either an *all-switching* mode that allows for increased output power or a *sequential switching* mode that exhibits increased dynamic range of the output power. It allows amplification of non-CE modulated signals while using transistors in their more energy-efficient switching mode of operation. [1]

In order to increase the total peak output power above that available from one SCPA core, a four-way transformer power-combiner is employed. The transformer is designed such that each SCPA core drives one parallel winding of the secondary, while the primary sums the induced currents. Two bits are reserved for the control of the four unit SCPAs which can be employed in *all-switching* or *sequential-switching* modes.

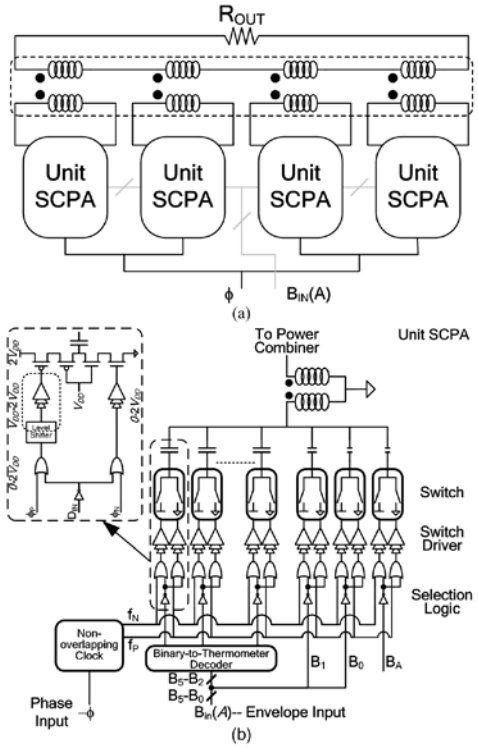

Figure 1: (a) Block diagram of the four-way power-combined SCPA and (b) a schematic of the unit SCPA.

A power-combined SCPA is fabricated in a 90nm RF CMOS process. The PA operates at a center frequency of 2 GHz. Using the transformer-based power-combining technique, the four-way power combining SCPA delivers a high peak output power and efficiency of 27 dBm and 26%, respectively. For 64 QAM OFDM-modulated signals, it achieves an average output power and efficiency of 20.3 dBm and 15.1 %, respectively.

Keywords: CMOS, EER, polar transmitters, power amplifiers, switched-capacitor power amplifier.

INDUSTRY INTERACTIONS

Intel, Freescale

MAJOR PAPERS/PATENTS

[1] S.M. Yoo, J. S. Walling, E.C. Woo, and D. J. Allstot, "A power-combined switched capacitor power amplifier in 90nm CMOS," *IEEE Radio Frequency IC Symposium*, pp. 149-152, June 2011.

TASK 1836.088, EFFICIENT SWITCHING MODE DIGITAL-INTENSIVE WIRELESS TRANSMITTERS UTILIZING SWITCHING MODE PAS

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SIGNIFICANCE AND OBJECTIVES

The efficiency of radio frequency transmitters and power amplifiers (PA) continues to pose a significant challenge in the design of battery-operated wireless communication systems as well as in base station applications. In this work we will investigate the use of switching power amplifiers and suitable modulation schemes for enhancing efficiency.

TECHNICAL APPROACH

Two-level modulation schemes such as PWM are well suited for use with efficient switching power amplifiers. These schemes are inherently digital friendly and therefore can be implemented in low-cost CMOS technologies. A PWM based approach that relaxes the requirement for high quality reference signal generation will be employed as part of this work. High-speed Class-D switching PAs in CMOS will be utilized for enhancing efficiency. Minimization of in-band spurs is a key design goal. A passive external band-pass filter will be employed to reduce out-of-band spurs.

SUMMARY OF RESULTS

A classical PWM generates its output by comparing the input to a ramp signal. This approach becomes progressively challenging as the bandwidth increases, as the ramp rate needs to be orders of magnitude higher than the signal bandwidth in order to maintain the linearity of the modulation. A modified feedback based PWM generator is utilized to achieve adequate bandwidth.

A key issue in the use of switching modulation schemes for wireless applications arises from the high spurious content in these waveforms. When used in wireless applications, it is critical that the spurious products not corrupt the in-band signal. Based on simulations of the PWM generator and the digital upconverter, we have implemented a spectral planning scheme to avoid the appearance of in-band spurs. The approach relies on the proper selection of the PWM clock and the upconversion LO.

Critical design challenges at the circuit level include the design of the upconversion mixer. This design needs to be sufficiently high speed to accommodate the sharp pulse edges generated by the digital modulation scheme. This mixer has been designed in a 0.13 µm CMOS process.

Another design that has been addressed in simulation is the IQ combiner at the output of the switching PAs. This design is required to combine two quadrature high-speed digital streams at the PA outputs. Critical requirements include quadrature accuracy of the combiner and its bandwidth. An LC network has been designed for this purpose.

The design is optimized modulation specifications of the 3G WCDMA standard.

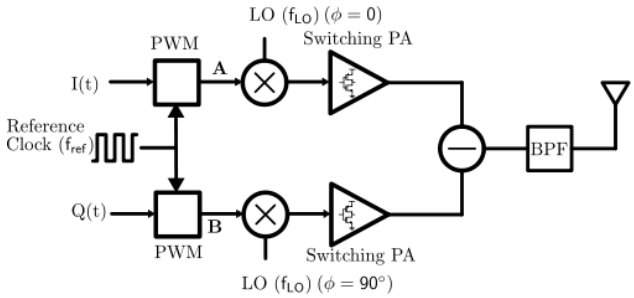


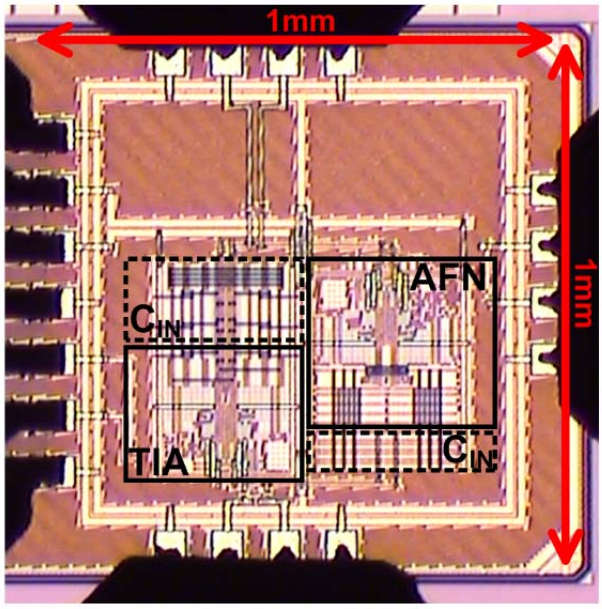
Fig. 1: Architecture of switching PA based digital-intensive transmitter

Keywords: PWM, digital modulation, wireless transmitters, switching mode PAs.

INDUSTRY INTERACTIONS

Texas Instruments

Fundamental Analog Thrust



Summary of Accomplishments

Circuits (Fund. Analog)	Demonstrated a temperature sensor front end that can operate at V_{DD}=0.4 V using a MOS transistors biased in sub-threshold and a bulk driven OpAmp. (1836.057, PI: C. Li, Texas Tech University)
CAD (Fund. Analog)	Developed a unified statistical analysis engine for SRAM performance, yield, reliability and testability. Using a novel Gibbs sampling algorithm, accuracy and speed of SRAM statistical analyses were improved by 3~10X. (1836.044, PI: Xin Li)
Circuits (Fund. Analog)	Demonstrated MIMO Cross talk cancellation in a 9Gb/S link by improving vertical and horizontal eye opening by 29% (mV) and 32% (UI), respectively (1836.022, Ramesh Harjani, University of Minnesota)
Circuits (Fund. Analog)	Demonstrated a flash ADC synthesized with a digital flow that achieves 35 dB SNDR with 1 MHz input up to sampling rate of 210 MSPS (1836.020, PI: U. Moon, Oregon State University)
Circuits (Fund. Analog)	Demonstrated a transimpedance amplifier with an active feedback network that can tolerate 10-mA blocker at 50 MHz. (1836.038, PI: Jose Silva-Martinez, Texas A&M)
Test (Fund. Analog)	Developed a new ADC spectral testing algorithm that achieves accurate spectral testing using available INL test results and proper signal processing. (1836.004, PI: R. Geiger, Iowa State University)

TASK 1836.004, ROBUST DESIGN OF LOW POWER SMALL AREA DATA CONVERTERS IN LOW VOLTAGE DIGITAL PROCESSES

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SIGNIFICANCE AND OBJECTIVES

AMS BIST is seen as the ultimate solution to embedded AMS testing and has been extensively studied. However, success has been very limited due to the bottleneck challenge in realizing accurate on-chip signal sources and measurement devices required by existing approaches.

This project will develop a practical AMS BIST technology and demonstrate its use in an embedded ADC. The project will further use the test results in a BIST based calibration scheme to improve the ADC performance.

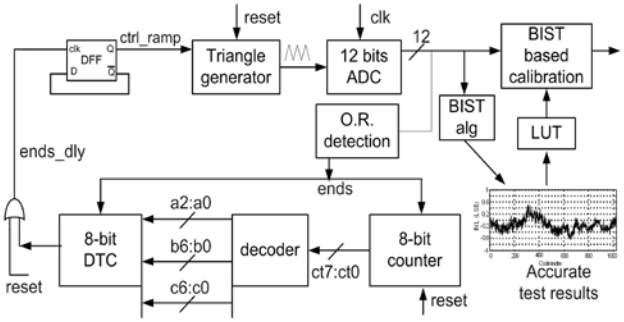
TECHNICAL APPROACH

In SRC Project #953, new FRE/FRM methods were introduced and patented for accurately testing ADCs and DACs using signal sources and measurement devices with performance orders of magnitude lower than that of the device under test. These methods will be adopted in this project and will be developed into a practical approach to embedded ADC BIST. An existing low power small area ADC embedded in a micro-controller in 65nm technology from Texas Instruments has been identified as the vehicle to demonstrate the approach.

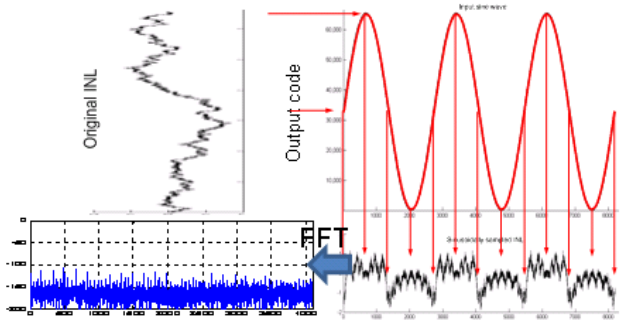
SUMMARY OF RESULTS

Several types of low cost on-chip signal generators have been designed. [1] Simulation results show that their performance is sufficient for medium to high resolution ADC test. To enable the patented FRE approach, a constant shift generator is needed and the shift constancy needs to be maintained at sufficient levels. Several such shifters have been designed and simulated. An overall strategy is developed for using these signal sources, constant shifters, and the FRE algorithm in a BIST setting for test cost reduction, in-field testing, and test based self calibration. [2] Finally, a new phase control strategy with very simple circuit block is developed to achieve on-chip coherent sampling even in the presence of large process variations. [3] All of these have been integrated with the identified embedded ADC (see first figure) and taped out for fabrication.

Another major contribution is a new ADC spectral testing algorithm that achieves accurate spectral testing without requiring dedicated data acquisition for it. Instead it uses available INL test results and proper signal processing to compute the ADC's spectral performance parameters. The method is illustrated in the second figure. [4]



BIST and BIST based calibration of embedded ADCs with complete on-chip signal generator and test control circuitry



Accurate spectral testing from available INL results, without additional data acquisition

Keywords: ADC design, ADC BIST, BIST based calibration, ADC spectral testing, ADC linearity testing

INDUSTRY INTERACTIONS

Texas Instruments.

MAJOR PAPERS/PATENTS

[1] J. Duan, et al, "Cost Effective Signal Generators for ADC BIST," IEEE International Symposium on Circuits and Systems, Taipei, Taiwan, pp. 13-16, May 2009.

[2] B. Vasan, et al, "Built In Self Test (BIST) for Test Cost Reduction, In-field Testing, and Test-based Self-Calibration of High Performance Analog and Mixed-Signal Systems," 35th Annual GOMACTech Conference, pp. 407-410, March 2010.

[3] Jingbo Duan, Degang Chen, and Randy Geiger, "Phase Control of Triangular Stimulus Generator for ADC BIST," IEEE International Symposium on Circuits and System, pp. 1935-1938, June 2010.

[4] Jingbo Duan, Le Jin, and Degang Chen, "A New Method for Estimating Spectral Performance of ADC from INL," International Test Conference, Nov, 2010.

TASK 1836.006, MULTI-CORE AND DISTRIBUTED PARALLEL SIMULATION FOR DESIGN AND VERIFICATION OF CUSTOM DIGITAL AND ANALOG ICS

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SIGNIFICANCE AND OBJECTIVES

Transistor-level circuit simulation is a fundamental, yet computationally intensive, design and verification enabler for wide ranges of digital and analog circuits. We address the significant simulation challenge by developing novel parallel simulation paradigms on multi-core and distributed computing platforms.

TECHNICAL APPROACH

To cope with design complexity, novel parallel computing paradigms are developed to exploit rich simulation application-level parallelisms. The proposed parallel simulation algorithms will be algorithmically efficient, geared to minimize inter-processor communication overhead, achieve good scalability, and simplify parallel programming implementation. We develop algorithms that leverage parallelism at all levels of the simulation flow, within a single algorithm or across multiple algorithms. We develop methodologies to facilitate static and runtime simulation code optimization.

SUMMARY OF RESULTS

Stable numerical integrations that lead to natural parallelization have been investigated. We adopted and extended the recently developed (telescopic) projective integration methods for highly efficient parallel circuit simulation in the time domain. This framework also allows for stable integration backwards in time, as shown in Figure 1.

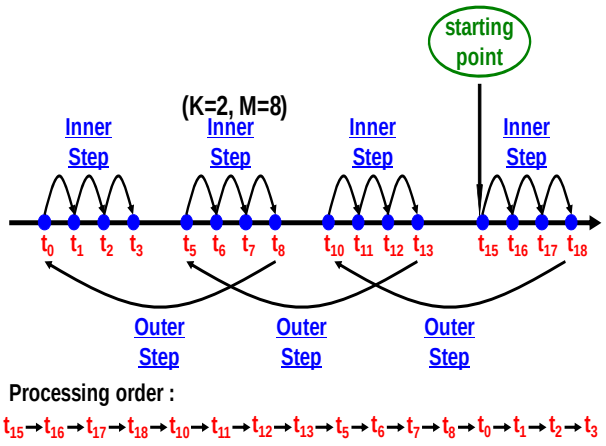
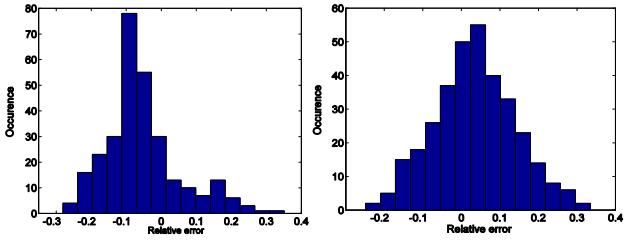


Figure 1: Stable numerical integration backwards in time.

Using this, we have developed a novel bi-directional parallel simulation approach that simultaneously solves an initial-value and final-value DAE problems in two opposite directions of time. This approach provides additional parallel speedups for timing simulation of digital circuits and periodic steady-state analysis of analog and RF circuits.

We have developed a hierarchical multi-algorithm parallel circuit simulation (HMAPS) framework that exploits coarse-grained inter-algorithm by launching multiple simulation algorithms in parallel for a given simulation task. The diversity in choosing various simulation algorithms and allocating parallel resources at both the intra- and inter-algorithm levels, however, creates a large configuration space. Parallel performance models have been developed to accurately predict the runtime of a given HMAPS configure, as shown in Figure 2. Based on this, we have developed a methodology that automatically finds the near optimal code configuration over a large configuration space either statically or at runtime, leading to significant speedups.



Transistor dominant Circuit Clock mesh

Figure 2: parallel runtime prediction for 300 HMAPS configurations.

Keywords: Circuit simulation, parallelization, transient analysis, steady-state analysis, parallel code optimization.

INDUSTRY INTERACTIONS

Texas Instruments, Intel, AMD, Freescale

MAJOR PAPERS/PATENTS

[1] W. Dong and P. Li, "Parallel circuit simulation with adaptively controlled projective integration," ACM Trans. on Design Automation of Electronic Systems (accepted).

[2] X. Ye and P. Li, "On-the-fly runtime adaptation for efficient execution of parallel multi-algorithm circuit simulation," IEEE/ACM ICCAD, 2010.

TASK 1836.013, WIDEBAND RECEIVER ARCHITECTURES IN DIGITAL DEEP SUBMICRON CMOS

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DR. JOSE SILVA-MARTINEZ, TEXAS A&M UNIVERSITY, COLLEGE STATION

SIGNIFICANCE AND OBJECTIVES

Provide innovative solutions to achieve high performance and low power consumption required in continuous-time (CT) ΔΣ analog-to-digital converters (ADCs) for multi-standard receivers. Apply the proposed system- and circuit-level techniques to the design of a low power CT ΔΣ ADC. Implementation of a CMOS chip prototype for the ADC and obtain experimental measurements to demonstrate the potential of the proposed solutions.

TECHNICAL APPROACH

The main approach is to achieve the required flexibility in multi-standard RF receivers by exploiting the enormous momentum in digital signal processors. Particularly, the incoming signal at the receiver input is to be digitized as early as possible while filtering operations and channel selection are performed in the digital domain. In this context, CT ΔΣ modulators show up as an attractive option. There are two main challenges for that ADC to achieve the required performance within a multi-standard receiver:

1. Pulse width jitter associated with the clock of the feedback digital-to-analog converters (DACs).
2. Tolerance to OOB blockers in terms of loop filter linearity and noise folding.

Solutions to these two critical problems are being addressed by the ongoing research effort in this project.

SUMMARY OF RESULTS

The block-diagram in Fig. 1 illustrates the proposed hybrid DAC with jitter tolerance solution that is based on high-pass shaping the noise generated by pulse-width jitter in the feedback DAC. A second-order single-bit ΔΣ modulator is used a test vehicle to demonstrate the performance of the adopted jitter suppression solution.

The plots in Fig. 2 show that the proposed solution can achieve jitter-tolerance that can be as large as 20 dB over non-returning-to-zero (NRZ) DACs and comparable to switched-capacitor-resistor (SCR) DAC implementations. The proposed hybrid DAC solution doesn't entail any extra requirements on the slew-rate or gain-bandwidth of the op-amp in the load integrator.

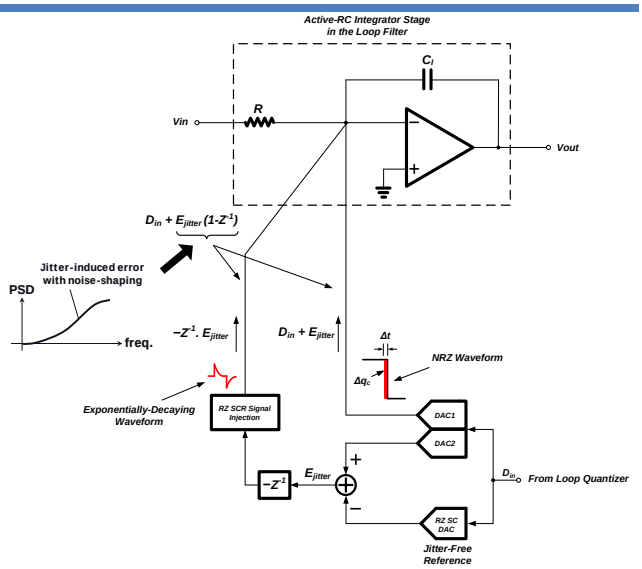

Figure 1: Proposed Hybrid-DAC based on spectral shaping of jitter induced errors.

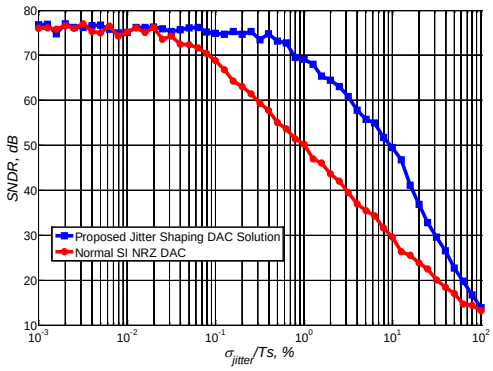

Figure 2: Jitter Tolerance performance of proposed DAC solution vs NRZ DAC.

INDUSTRIAL LIAISONS

Venkatesh Srivinisan, Texas Instruments Inc., Dallas TX

MAJOR PAPERS/PATENTS

[1] R. Saad and S. Hoyos, "Feed-Forward Spectral Shaping Technique for Clock-Jitter Induced Errors in Digital-to-Analog Converters," IET Electronics Letters, vol. 47, no. 3, pp. 171–172, Feb. 2011.

[2] R. Saad, S. Hoyos, and J. Silva-Martinez, "Clock Jitter Shaping Technique for Continuous-Time Analog-to-Digital Converters," SRC/GRC Patent Program, patent filed, September 2010.

TASK 1836.019, DIGITALLY ENHANCED ENERGY-EFFICIENT HIGH-SPEED I/O LINKS

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SHANBHAG@ILLINOIS.EDU
ELYSE ROSENBAUM, UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN

SIGNIFICANCE AND OBJECTIVES

Design of high-speed and low-power analog mixed-signal circuits in nanoscale CMOS is made challenging due to a number of issues such as reduced supply voltage. These problems are exemplified in multi-Gb/s I/O links, whose prevalence in modern electronic systems motivates us to seek cost-effective solutions.

TECHNICAL APPROACH

The goal of this project is to exploit the capability of DSP and ECC to reduce power and enhance ESD resiliency in high-speed I/O links. I/O link specific ECC will be explored in terms of BER, latency, encoder and decoder architectures. BER-optimal rather than SFDR-optimal ADC architectures will be developed. An ESD-protected multi-Gb/s I/O link embodying some of these ideas will be implemented.

SUMMARY OF RESULTS

We have demonstrated the benefits of our systems-assisted approach via both analytical studies and two IC prototypes. We have shown that short (block length = 63-to-255) BCH codes in a 20-in FR4 link carrying 10-Gb/s data results in: 1) an 18-mW/Gb/s savings in the ADC; 2) a 1-mW/Gb/s reduction in transmit driver power; 3) up to 6× improvement intransmit jitter tolerance. These results indicate that ECC is effective in designing robust, low-power high-speed I/O links.

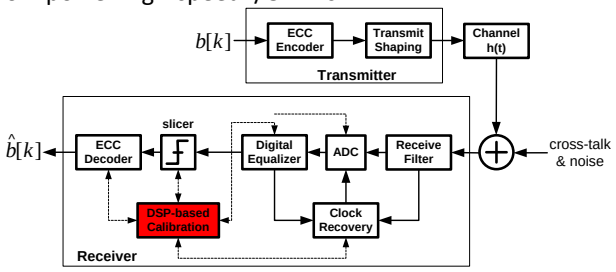
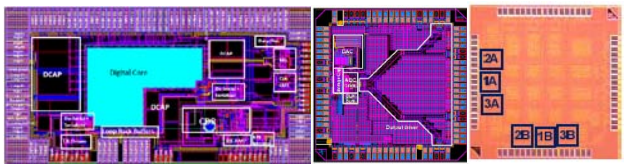


Figure 1: Overview of a systems-aware mixed-signal high-speed I/O link.

For ADC-based high-speed I/O links, we have shown [1] that a BER-optimal ADC, where the ADC reference levels are chosen based on channel output statistics, provides the following advantages in a 20-in FR4 link carrying 10-Gb/s data: 1) the ADC shaping gain is > 30dB at a BER=10^{-15} for a 3-b ADC, and 2) a 3-b BER optimal ADC gives 10^{6}X reduction in BER over a 4-b conventional ADC at an SNR of 32 dB. This corresponds to a power savings of 50% in the ADC. A 4b, 4GS/s ADC prototype IC in 90nm was taped-out in June 2011.

A receiver test chip was designed and tested in a low-power 90-nm CMOS technology to demonstrate a g_m-boosted negative capacitance circuit for input port bandwidth extension. The g_m-boosted circuit leverages the inherent gain of the receive amplifier to improve the circuit's ability to negate the capacitive parastics at the input port of the receiver. Measured results show a 1.23X bandwidth enhancement with a > 7kV HBM ESD resiliency, which is better than the 5.5kV achieved via conventional techniques.



(a) (b) (c)

Figure 2: Prototype ICs all in 90nm: (a) 6.5Gb/s ECC-based I/O trans., (b) 4Gb/s 4b BER-opt. ADC, and (c) Gm-boosted RX.

In the remainder of this last year of our project (end date: Dec. 2011), we plan to: 1) report the test results of an ECC-based 6 Gb/s low-power transceiver, 2) report test results of a 4-b BER-aware ADC for a 4 Gb/s I/O link in a 90nm CMOS process.

Keywords: high-speed I/O, DSP, ESD, ECC, low-power

INDUSTRY INTERACTIONS

Texas Instruments, Intel, AMD, IBM

MAJOR PAPERS/PATENTS

[1] R. Narasimha, N. R. Shanbhag, and A. C. Singer, "BER-aware adaptive ADC-equalizer receiver for communication links," IEEE SiPS 2010.

[2] N. R. Shanbhag and A. C. Singer, "System-assisted mixed-signal design," Design and Test in Europe (DATE), Grenoble, France, March 2011. (invited)

[3] A. Faust, A. Srivastava, E. Rosenbaum, "Effect of on-chip ESD protection on 10Gb/s receivers," EOS/ESD Symposium, Sept. 2011.

TASK 1836.020, LOW-COMPLEXITY HIGH-PERFORMANCE ANALOG-TO-DIGITAL CONVERTERS IN SUBMICRON CMOS

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SIGNIFICANCE AND OBJECTIVES

The reduced supply and intrinsic gain prevalent in submicron CMOS technologies limit the achieved performance in analog-to-digital converters in those technologies. The techniques presented in this summary offer ways to obtain reduce power, increase SNR and lower design cost.

TECHNICAL APPROACH

The power- and area-saving techniques are implemented in two separate prototype ICs. The first prototype is a bi-directional noise-shaped quantizer. With a small modification in the discharging phase of the traditional dual/single-slope ADCs, first-order noise shaping has been achieved. This ADC replaces the flash ADC in DSM and not only removes all the capacitive loading of the flash ADC, but it also adds a first order of noise-shaping. The second prototype is a fully synthesized stochastic ADC using 3-input NAND gates to act as analog comparators.

SUMMARY OF RESULTS

The proposed bi-directional noise-shaped quantizer has been used as the quantizer of a 2nd order loop DSM. This quantizer has been merged with the active and also replaces the flash ADC. The bi-directional discharging halves the speed requirements of the counting clock. The fabricated prototype in 0.18um CMOS process achieves over 78dB SNDR at 50MHz sampling speed and oversampling ration of 24. The analog power consumption is only 1.35mW [1].

The second ADC is synthesized entirely from Verilog code in 90nm digital CMOS using a standard digital cell library. An analog comparator is generated by cross-coupling two 3-input NAND gates. Over 35dB SNDR is achieved with a 1MHz input up to a sampling rate of 210MSPS [2].

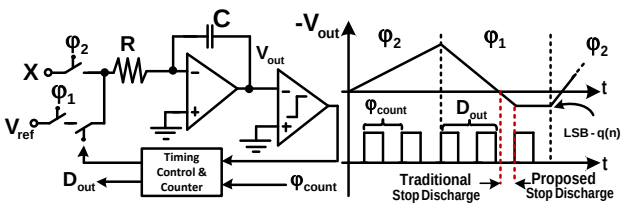

Figure 1: The noise-shaped integrating quantizer

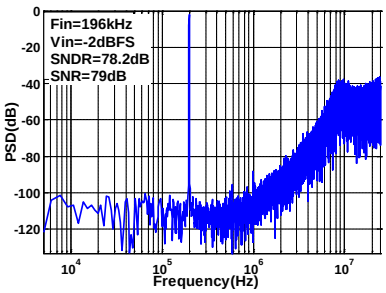

Figure 2: Measured output spectrums of the proposed quantizer used in a 2nd order delta-sigma loop.

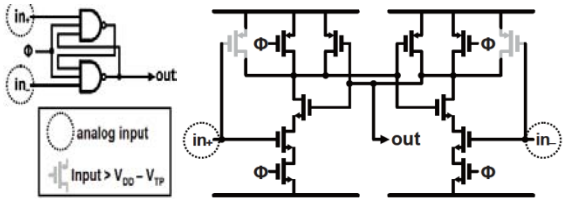

Figure 3: 3-input NAND gates as analog comparators.

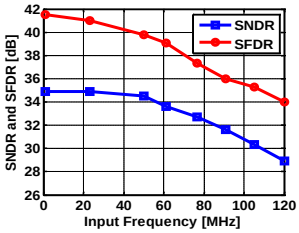

Figure 4: Measured output SNDR and SFDR.

Table 1: Performance Summary

	VDD	ENOB	BW	Power	Area
Chip 1	1.5V	12.7b	1MHz	2.8mW	.44mm^2
Chip 2	1.2V	5.7b	125MHz	34.8mW	.18mm^2

Keywords: dual-slope ADC, noise-shaped quantizer, synthesizable

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] N. Maghari and U. Moon, "A Third-Order DT ΔΣ Modulator Using Noise-Shaped Bi-directional Single-Slope Quantizer," ISSCC, Feb 2011, pp 474-475.

[2] S. Weaver, B. Hershberg, and U. Moon, " Digitally Synthesized Stochastic Flash ADC Using Only Standard Digital Cells," VLSI 2011

TASK 1836.022, HIGH-SPEED MIMO SIGNALING TECHNIQUES FOR SINGLE-ENDED PARALLEL I/O

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SIGNIFICANCE AND OBJECTIVES

Demand for higher data throughput in processor-memory I/Os increasingly forces the I/O number/chip and data rates/pin to increase. The proximity in current I/Os make a coupling interference becomes a significant noise source. The goal of task is to develop efficient MIMO techniques to reduce crosstalk and improve multi-Gbps NRZ signaling.

TECHNICAL APPROACH

Chip-to-chip I/O signaling has relatively time-invariant channels where simplified MIMO crosstalk techniques (XTC) can be used. The parallel decomposition of the MIMO channels can be obtained by manipulating the channel input and output using receiver shaping. Through MIMO algorithm, we not only reduce crosstalk but also improve signaling bandwidth of I/Os. For low-power and low-area, the MIMO algorithm has been implemented with passive RC-CR continuous IIR filters, as shown in Fig 1. The detail information of algorithm and its implementation are presented in [1] and [2].

SUMMARY OF RESULTS

Tektronix AWG 7102C transmit 4 independent 9-11 Gb/s NRZ signals with 2^7-1 pattern length into 4 parallel single-ended channels and Infiniium DSO81204A monitor the received signals impaired by crosstalk as well as crosstalk equalized signals at the receiver outputs. The received eye in channel 2 at 9 Gb/s shows eye opening of 48/642 mV_{p-p} vertically and 40/111 ps horizontally because of 2

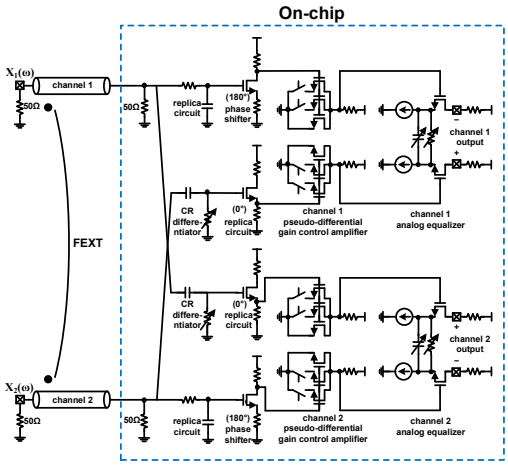

Figure 1: low power and low complexity implementation of MIMO algorithm (Multi-lane MIMO XTC algorithm and architecture is before publication but shown in the final report)

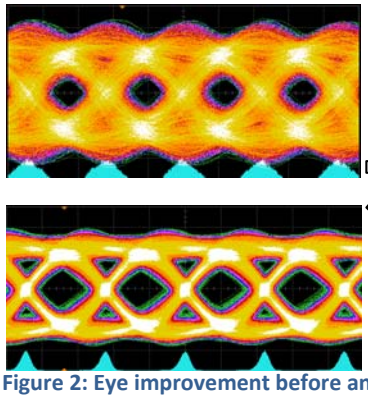

Figure 2: Eye improvement before and after MIMO XTC

uncorrelated aggressors from adjacent channels. After MIMO XTC, the eye-opening is improved by 29% vertically and 32%UI horizontally. The jitter standard deviation (σ_{p-p}) is reduced from 12.9 ps to 6.1 ps. The BER performances are measured by BERT scope 17500C and the achieved BER at the eye-center is 10^{-12}. The measurement results of other 3 channels are summarized in the report [P060728].

Ref	Tech (nm)	Speed (Gb/s)	J_{pp}↓/Eye↑ (UI%/mV%)	Power (pJ/b)	Area (mm^2)
JSSC 06'	130	10	28/0	8	0.024 (XTC)
CICC 08'	180	5	10.4 / 11	6	0.035 (RX)
CICC 06'	180	12.8	14.5/15	25	3.75 (TX)
This work	65	9	32 / 29	1.78	0.036 (XTC)
		11	49.8 / 15.7		

Comparison table

Our scheme shows the lowest power at highest data rates among the latest publications. Our key strategy is to handle the continuous crosstalk problem with continuous-IIR filter and achieves the best performance.

Keywords: MIMO XTC, Continuous-time IIR XTC, Far-end crosstalk (FEXT), ISI, Equalization

INDUSTRY INTERACTIONS

Intel, AMD

MAJOR PAPERS/PATENTS

[1] Taehyoun Oh and Ramesh Harjani, "A 5 Gb/s 2×2 MIMO Crosstalk Cancellation Scheme for High-Speed I/Os", *IEEE CICC*, Sept 2010

[2] Taehyoun Oh and Ramesh Harjani, "A 6 Gb/s MIMO Crosstalk Cancellation Scheme for High-speed I/O," *IEEE JSSC*, Aug 2011

TASK 1836.028, TOOLS AND ALGORITHMS FOR BEHAVIORAL MODEL GENERATION OF ANALOG/MIXED-SIGNAL CIRCUITS

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SIGNIFICANCE AND OBJECTIVES

Manually creating circuit behavioral models is time consuming and the lack of fast simulation models can hamper chip level verification. This research promises to speedup model generation and system simulation. The objective is to develop algorithms and tools for extracting behavioral models from the circuit level for linear and switching regulators.

TECHNICAL APPROACH

The proposed approach leads the user though intuitive questions which allow the tool to understand the important characteristics of the circuit of interest. It then analyses the circuit configurations based on the circuit netlist and applies algorithms for signal path tracing, model topology formulation and characterization developed for modeling linear regulators. Beyond that, a template based PWM (Pulse Width Modulation) switch model is used to achieve CCM (Continuous Conduction Mode) to DCM (Discontinuous Conduction Mode) automatic transition for switching regulators. The same approach may be applied to generate a unified model topology for multi-type switch converters (i.e. Buck, Boost, Buck-Boost). All the algorithms are expected to generate model topologies automatically and produce a model in HDL (Verilog-A) code.

SUMMARY OF RESULTS

The model topology formulation algorithm developed for LDO regulators is shown in Figure 1 and Figure 2 shows the LDO modeling tool architecture. The model for an example LDO circuit produces a good match to the original circuit with up to 10X simulation speed up. Through the interactive user interface, the process of the model code generation is less than twenty minutes for the example circuit.

The surveys and reviews on the behavioral modeling approaches of switching mode regulators have been completed. A preliminary Verilog-A PWM average switch model was proposed to model the switching position of the regulators. The ongoing research will focus on the automatic characterization algorithms for the PWM average switch model.

Keywords: Model, Automation, SPT, MTF, LDO, Switching regulators

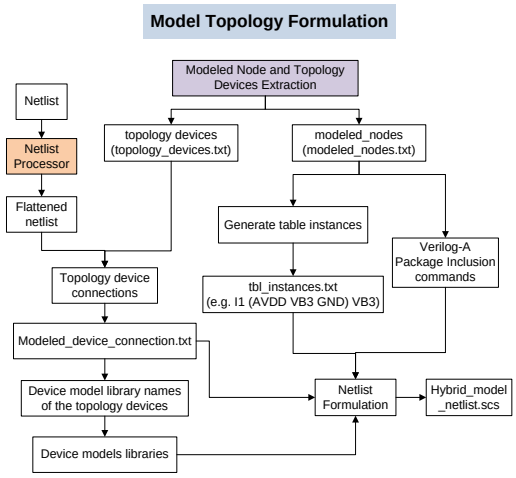

Figure 1: Model Topology Formulation Algorithms

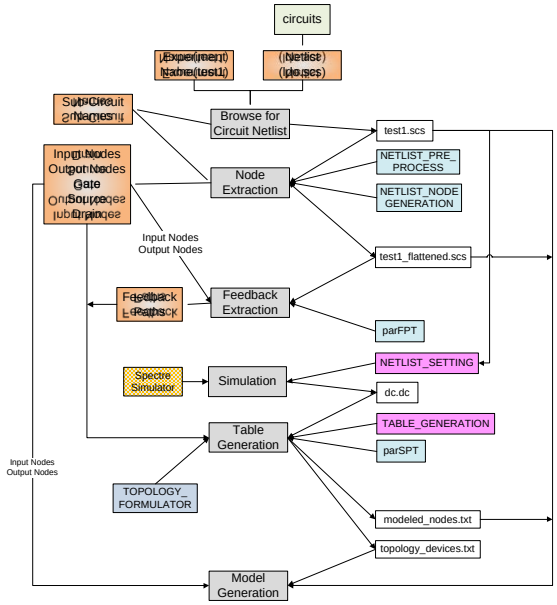

Figure 2: Architecture design of LDO modeling tool

INDUSTRY INTERACTIONS

Texas Instruments

TASK 1836.030, FAST PVT-TOLERANT PHYSICAL DESIGN OF RF IC COMPONENTS

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SIGNIFICANCE AND OBJECTIVES

PVT variability makes it hard to achieve "safe" designs in nanoscale CMOS technologies and also reduces yield. However, no major attempts have been made to address these for RFICs due to increased complexity and bottlenecks of analog simulation. We investigate fast physical design and optimization techniques for RF ICs such that the resulting designs are PVT tolerant.

TECHNICAL APPROACH

To have a process-variation robust design accounting for parasitics, power, and temperature, we investigate a new "PVT tolerant RF IC design flow". In a standard RF IC design flow, multiple iterations between the front-end circuit design and back-end layout are required to achieve parasitic closure. Such a manual approach requires X number of iterations. The proposed design flow reduces the number of manual iterations to 1, by performing the X number of iterations on a parasitic parameterized netlist instead of the layout. Hence, **this novel flow reduces the X number of manual iterations required for parasitic closure, to 1 manual iteration**. Accurate metamodeling and optimization algorithms are investigated for ultra-fast physical-design optimization.

SUMMARY OF RESULTS

The effects of PVT variation on the performance of RF IC components is analyzed. A current-starved VCO circuit is used as a case study. The physical design of the VCO is performed using a 90*nm* CMOS PDK (Fig. 1). The simulations were performed on the full-blown (RLCK) parasitic-extracted netlist of the VCO. The statistical distribution of the center frequency proved its Gaussian nature for correlated variations. **The accurate design flow achieved 16.4% power (leakage) minimization with 10% degradation in center frequency compared to the target frequency** [1]. Sampling techniques such as Monte Carlo, Latin Hypercube Sampling (LHS), Design of Experiments (DOE), are compared for speed and accuracy, and polynomial metamodels are obtained for a ring oscillator and LC-VCO [2]. An ultra-fast design-flow that combines metamodels and optimization algorithms is investigated [2]. For a ring oscillator circuit, **the simulated annealing optimization is faster by 951× than the exhaustive search** and 6× faster than the tabu search optimization (Fig. 2).

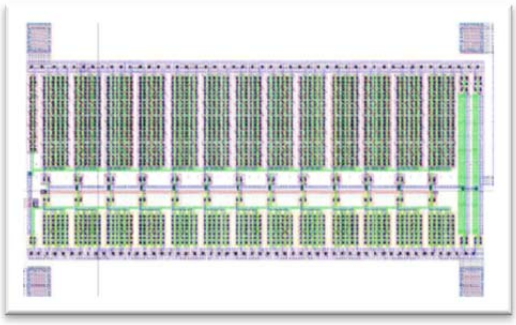

Figure 1: P4VT Optimal Dual-Threshold VCO Layout.

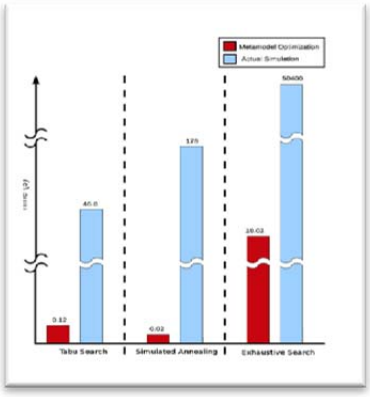

Figure 2: Comparison of Running Time of the Optimization.

Keywords: Process Variation, Parasitic Effects, Metamodeling, Optimization, Nano-CMOS, RF Circuits

INDUSTRY INTERACTIONS

Priyadarsan Patra, Intel Corporation

MAJOR PAPERS/PATENTS

[1] S. P. Mohanty et al., "A P4VT (Power-Performance-Process-Parasitic-Voltage-Temperature) Aware Dual-*VTh Nano-CMOS VCO", in Proc. 23rd Intl. Conf. VLSI Design*, pp. 99--104, 2010.

[2] O. Garitselov et al., "Nano-CMOS Mixed-Signal Circuit Metamodeling Techniques: A Comparative Study", in *Proc. 1st ISED*, pp. 191-196, 2010.

[3] O. Garitselov et al., "Fast Optimization of Nano-CMOS Mixed-Signal Circuits Through Accurate Metamodeling", in *Proc. 12th ISQED*, pp. 405--410, 2011.

TASK 1836.031, VARIATION TOLERANCE ANALOG DESIGN BASED ON GENERALIZED KHARITONOV/LYAPUNOV THEORY

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DIAN ZHOU, UNIVERSITY OF TEXAS AT DALLAS

SIGNIFICANCE AND OBJECTIVES (50 WDS)

In today's VLSI technology, the manufactured fluctuations are unavoidable. We propose an efficient method, in spirit of the Kharitonov's theorem, to compute the likely performance range of linear analog circuit with process variations. This approach reduces the computational burden to evaluation of at most 48 critical transfer functions.

TECHNICAL APPROACH (100 WDS)

The geometrical properties of Kharitonov's theorem state that phase and magnitude response of a family of interval polynomials are bounded by four Kharitonov polynomials in this family. Assume the behavior of a linear analog circuit is governed by an interval transfer function which is the ratio of two families of interval polynomials. Therefore the magnitude and phase response of the interval transfer function can be calculated from the overall combinations of eight Kharitonov polynomials for the numerator and denominator interval polynomial families.

SUMMARY OF RESULTS

The envelop of 48 critical Kharitonov-type transfer functions can yield variation range of magnitude response, whereas 16 critical Kharitonov-type transfer functions are sufficient to calculate the variation range of phase response. Take a RAFFC three-stage amplifier as example, and the derived transfer function is:

$$A_v(s)=\frac{-1-s\dfrac{C_{C1}}{g_{mb}}}{\dfrac{1}{A}(1+\dfrac{s}{\omega_{P1}})[1+s\dfrac{C_{C1}+C_L}{g_{m3}C_{C1}}C_{C2}+s^2\dfrac{C_{C2}C_L}{g_{mb}g_{m3}}]}$$

where $A=g_{m1}r_{01}g_{m2}r_{02}g_{m3}r_{03}$, $\omega_{p1}=1/C_{C1}r_{01}g_{m2}r_{02}g_{m3}r_{03}$. Assume there is ±10% tolerance level to every parameter. Fugure.1 (a) and (c) display the envelop of magnitude and phase response of RAFFC circuit which is calculated from 48 and 16 Kharitonov-type critical transfer functions. Figure.1 (b) and (d) show the envelop and 500 Monte Carlo samples when every parameter is sampled randomly from its variation range. It is obvious that the samples are well enclosed by the envelops. The simulation of 500 samples spends 2.47h, but underestimates the variation range. The magnitude and phase envelop yields the exact bounds within 15.2354s and 11.1191s respectively. From the envelops, we can also tell that the gain of RAFFC circuit may vary from 106dB to 118dB, whereas the variation range of phase margin lies within [45.5°, 178°].

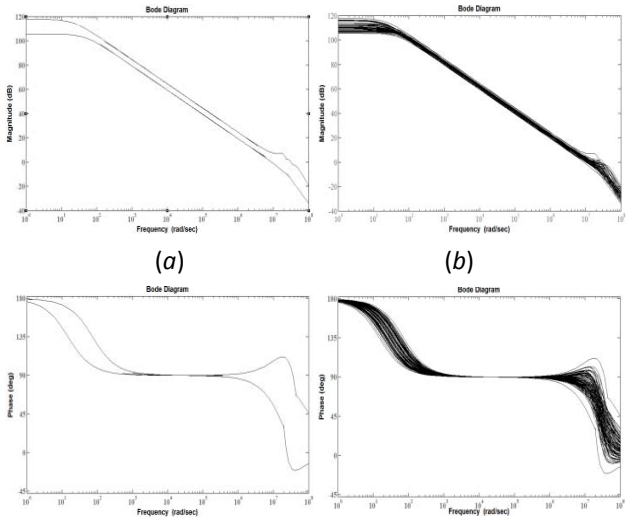

Figure.1 (a) The envelop of magnitude response; (b) The envelop and 500 Monte Carlo samples of magnitude response; (c) The envelop of phase response; (d) The envelop and 500 Monte Carlo samples of phase response

Next step, we will extend the proposed approach to other interested performance metrics and nonlinear circuits. We will also study the Lyapunov theory, and apply it in the robust analysis of VLSI circuits in the time domain.

Keywords: Kharitonov's theorem, interval polynomial, gain, phase margin.

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] L. Qian et al., "Worst Case Analysis of Linear Analog Circuit Performance Based on Kharitonov's Rectangle," (Submitted) 2010 ICSICT.

[2] L. Qian et al, "Performance Robustness Analysis of VLSI Circuits with Process Variations Based on Kharitonov's Theorem," (Submitted) 2010 DCAS.

TASK 1836.038, BLOCKER-ROBUST TRANSIMPEDANCE AMPLIFIER FOR CO-EXISTING RADIO RECEIVERS

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AYDIN ILKER KARSILAYAN, TEXAS A&M UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

Commonly disregarded, the response out-of-band (OOB) of transimpedance amplifiers is highly significant to the linearity and, hence, sensitivity of zero-IF receivers for systems in which multiple radios coexist. Addressing the matter, a TIA robust against saturation or cross-modulation by blocking signals near the band edge has been developed.

TECHNICAL APPROACH

Capacitively coupled around a single-pole TIA, an active feedback network (AFN) produces an alternate low impedance path to divert large signals OOB away from the input nodes. The AFN is based on an active-RC high-pass circuit that minimizes its impact at low frequencies but boosts its gain beyond the bandwidth of the single-pole TIA (10MHz), producing a sharp transition between in-band and OOB regions in the overall forward path. Using a class-AB biased output stage, the amplifier in the AFN drives high currents to absorb signals of up to ±10mA across a wide frequency band (0.05-1GHz), consuming reasonable power.

SUMMARY OF RESULTS

Figures 1(a) and 1(b) show the schematic and micrograph of the Blocker-Robust TIA implemented, respectively. The prototype IC was fabricated in a 45nm CMOS process in the spring of 2010 and tested by direct wafer probing. The device occupies an active area of 0.25mm^2 and draws 17mA from a 2.5V supply, mostly quiescent current in the output stages of the fully-differential amplifiers (~60%).

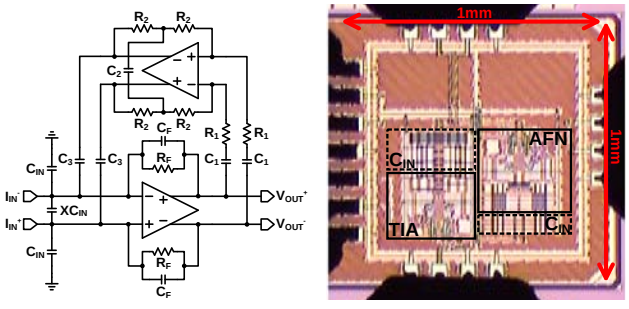

Figure 1: (a) Schematic of Blocker-Robust TIA designed (b) Micrograph of 45nm CMOS prototype implemented.

Magnitude response measurements verified proper device functionality of the device (66dBΩ gain, 10MHz bandwidth) and showed that the proposed solution yields 18dB greater attenuation at 50MHz compared to a conventional first-order response from a single-pole TIA with the same bandwidth.

As shown in Figure 2, single-tone P1dB test data confirmed that compression/expansion of gain occurs when the input current to the blocker robust TIA reaches ±10mA at and beyond 50MHz, verifying the robustness to large interferers gained through the AFN.

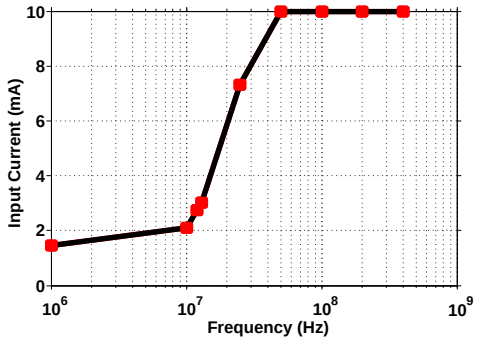

Figure 2: Measured single-tone P1dB – peak input current causing gain compression/expansion.

The ability of the design to prevent blocking in-band was checked through measuring the gain of a 10uA, 6MHz signal in presence of a large tone near the band edge. It takes a ±9mA signal at and beyond 40MHz to compress the in-band signal by 1dB.

The performance achieved suits the stringent filtering and linearity needs of receivers for systems where multiple radios coexist and harmful interferers abound. It may allow for relaxation of ADC design specifications and, potentially, simplification of RF pre-select filtering.

Keywords: Transimpedance amplifier, linearity, blocker filtering, cmos, active feedback, receiver, coexistence

INDUSTRY INTERACTIONS

Intel Corporation

MAJOR PAPERS/PATENTS

[1] A. Perez-Carrillo, et al, "A Large-Signal Blocker Robust Transimpedance Amplifier for Coexisting Radio Receivers in 45nm CMOS," IEEE RFIC, June 2011.

TASK 1836.040, ENERGY-EFFICIENT CMOS 10GS/S 6-BIT ADC WITH EMBEDDED EQUALIZATION

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SIGNIFICANCE AND OBJECTIVES (50 WDS)

The proposed ADC system aims to significantly improve the energy efficiency of Nyquist-rate ADCs in high-speed applications. Partial equalization is embedded in the ADC to achieve a higher efficiency for the ADC-based receiver. Time-interleaving of successive-approximation-register (SAR) ADCs is used to achieve this goal.

TECHNICAL APPROACH (100 WDS)

SAR ADC architectures have the potential to achieve excellent energy efficiency for medium resolution ADCs in sub-100nm CMOS technologies. In order to achieve the required conversion rate, a time-interleaved structure is used. The target design is a 6-bit 10GS/s ADC with figure of merit (FOM) better than 0.3pJ/conversion-step. To further relax the digital processing and achieve better efficiency for the whole receiver, especially for high-speed link applications, ADC with embedded partial equalization is considered.

SUMMARY OF RESULTS

A prototype 6-bit 2.5GS/s with 2 parallel sub-ADCs is designed in a 90nm CMOS technology. Eight time-interleaved unit SAR ADCs with one front-end T/H constitute each sub-ADC. Figure 1 shows the layout of the chip. Main blocks are 8-phase generator, time-interleaved ADC core, and a 24kb SRAM for storing the output of the ADC for easier performance measurement.

Calibration schemes are devised to compensate for the mismatch between the sampling phases of the T/Hs, and the offset mismatch between comparators of unit ADCs. The post-layout power breakdown of the chip is shown in Table 1. A novel embedded DFE scheme is utilized with low power/area overhead. Post-layout simulations show THD of -29.3dB at 5GHz input frequency.

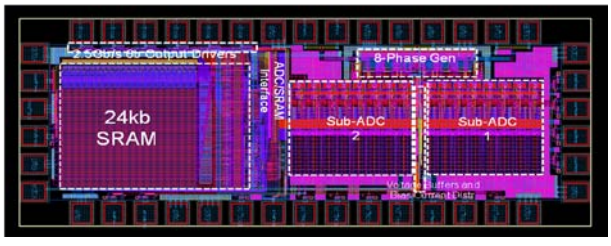

Figure 1: The chip layout of the prototype 6-bit 2.5GS/s ADC in 90nm CMOS technology

Table 1: Post-layout power breakdown of 6-bit 2.5GS/s ADC in LP 90nm CMOS technology (V_{DD} = 1.3V)

Block		Power (mW)
Each 1.25GS/s Sub-ADC	T/H	2.2
	Comparators + SAR logic	6.48
	Local CLK distr.	1.1
	Total sub-ADC core	9.78
Ref/CM voltage buffers		6.9
Total 6b 2.5GS/s prototype ADC		26.46
8-phase gen. + Global CLK distr.		5.4

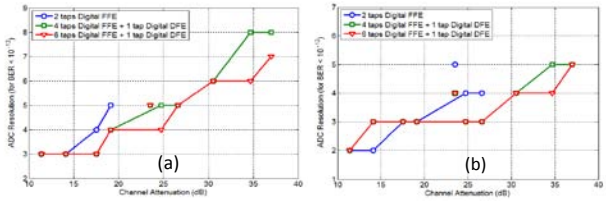

Figure 2: ADC resolution requirement for 10Gbps receiver with (a) all digital equalization, and (b) 2-tap embedded FFE and back-end digital equalization

The performance impact of embedding partial equalization, DFE or FFE, in ADC-based receivers is analyzed in [1]. Figure 2 compares the required front-end ADC resolution to achieve BER<10^{-12} with and without embedded feed-forward equalization (FFE). It is shown that embedded FFE results in savings of ADC resolution; hence, smaller power of the whole system. As future work, embedding both FFE and DFE efficiently in time-interleaved SAR ADC is planned.

Keywords: Analog-to-digital converter, embedded equalization, energy efficient, successive approximation register (SAR), time interleaved

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] A. Shafik, K. Lee, E. Zhian Tabasy, and S. Palermo, "Embedded equalization for ADC-based serial I/O receivers," submitted to 20th IEEE EPEPS, October 2011, San Jose, USA.

TASK 1836.044, STATISTICAL MODELS AND METHODS FOR DESIGN AND TEST OF NON-DIGITAL COMPONENTS

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SHAWN BLANTON AND LAWRENCE PILEGGI, CARNEGIE MELLON UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

Develop, implement, and validate through experiment the statistical models and methods for the design of SRAM bit cells and their surrounding analog periphery circuits with user-provided constraints on performance, yield and quality.

TECHNICAL APPROACH

A unified statistical analysis engine is developed to predict SRAM performance, yield, reliability and testability by fast Monte Carlo method. The proposed engine adapts the recent advance of Gibbs sampling from the statistics community to adaptively search the variation space and speed up the convergence of Monte Carlo analysis. Our experimental results demonstrate that the proposed Gibbs sampling method achieves 3~10× runtime speedup over other state-of-the-art techniques without surrendering any accuracy.

SUMMARY OF RESULTS

SRAM bit cells are generally designed with minimum-size devices, and can be significantly affected by large-scale process variations posed by nanoscale manufacturing technology. It becomes increasingly critical to evaluate the statistical behavior of SRAM bit cells both efficiently and accurately. Since bit cells typically have extremely small failure probability, a simple Monte Carlo method suffers from slow convergence rate as only few random samples will fall into the failure region. To improve the sampling efficiency, importance sampling has been proposed to directly sample the failure region based on a distorted probability density function (PDF), instead of the original PDF of process variations.

Applying importance sampling to SRAM analysis, however, is not trivial. Ideally, in order to maximize prediction accuracy, we should sample the failure region that is most likely to occur. Such a goal, however, is extremely difficult to achieve, since we never know the exact failure region in practice. Motivated by this observation, a novel Gibbs sampling method is developed to improve the efficiency of importance sampling. Unlike the traditional Monte Carlo algorithm that samples a given PDF, the proposed Gibbs sampling approach does not need to know the sampling PDF explicitly. Instead, it adaptively searches the failure region and then generates random samples in it. From this point of view, Gibbs sampling can be conceptually viewed as a unique Monte Carlo method with an integrated optimization engine which allows us to efficiently explore the failure region.

As a demonstration example, we consider an industrial 6-T 65nm SRAM cell. For comparison purpose, three different importance sampling methods are implemented to estimate the failure probability: (1) mixture importance sampling (MIS), (2) minimum-norm importance sampling (MNIS), and (3) Gibbs sampling (proposed). Figure 1 shows the estimated failure probability (normalized) as a function of the number of random samples. Note that the proposed Gibbs sampling is substantially more accurate than the other two traditional methods (i.e., MIS and MNIS) given the same number of random samples.

In the future, we will take advantage of the high efficiency of the proposed Gibbs sampling method to further study the design trade-offs (e.g., speed, power, yield, reliability, testability, etc.). We will also use the proposed statistical analysis engine to study SRAM reliability and testability.

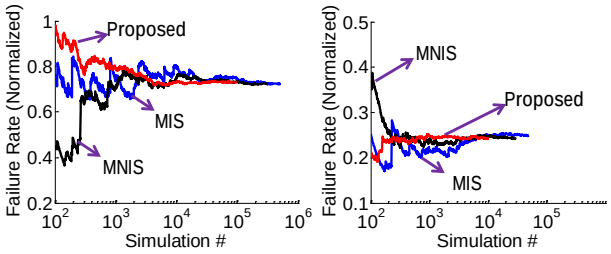

Figure 1: Convergence rate of different Monte Carlo algorithms for SRAM failure rate prediction: (left) read noise margin, and (right) write noise margin.

Keywords: memory, parametric yield, statistical analysis

INDUSTRY INTERACTIONS

Texas Instruments, Freescale, IBM

MAJOR PAPERS/PATENTS

[1] C. Dong and X. Li, "Toward a unified statistical analysis engine of SRAM yield, reliability and testability via Gibbs sampling," SRC TECHCON, 2010.

[2] C. Dong and X. Li, "Efficient SRAM failure rate prediction via Gibbs sampling," IEEE DAC, 2011.

TASK 1836.046, RECONFIGURABLE ANTENNA INTERFACE FOR LOW POWER WIRELESS SENSOR NODES

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KARTHIK NATARAJAN, UNIVERSITY OF WASHINGTON

SIGNIFICANCE AND OBJECTIVES

Transmitters for ultra-low-power sensor networks are continuously evolving to transmit low output power in a highly efficient manner. To this end, various architectures have been introduced that trade off distinct advantages and disadvantages. A comparison of several recent transmitter architectures is presented in terms of power efficiency.

TECHNICAL APPROACH

Several interesting architectures for implementing the radio in a wireless sensor node have been proposed recently. The direct modulation approach described by Cho, et al. [1] uses a low-power oscillator followed by a PA/antenna interface. In order to save power, the architectures presented by Bohorquez, et al. [2] and Chee, et al. [3] eliminate the PA and couple the oscillator directly to the antenna which is used as an inductive element.

SUMMARY OF RESULTS

In order to totally eliminate losses from the PA, the approach of Bohorquez, et al. [2] (Fig. 1) simply does not use one; instead, the (power) oscillator drives the antenna directly while simultaneously using it as the inductive element in its resonant tank.

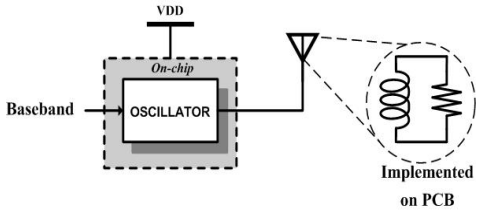

Figure 1: Sensor node with an oscillator driving an off-chip antenna.

Clearly, this solution reduces the number of circuits; however, it transfers most of the overall power budget to the (power) oscillator.

In a direct modulation transmitter (Fig. 2), a PA stage provides a buffer interface between the oscillator and the antenna. In a typical implementation, the oscillator is a digitally-controlled oscillator (DCO) operating with an NMOS (or CMOS) cross-coupled transistor pair(s).

A plot of the total power consumed by the three different transmitters versus PA gain is shown in Fig. 3. The three architectures include an oscillator directly driving an antenna with no PA, an oscillator with on-chip

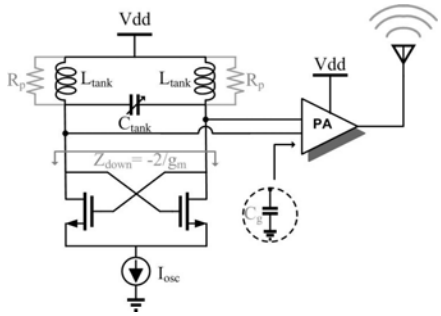

Figure 2: A direct modulation transmitter with a DCO driving the PA.

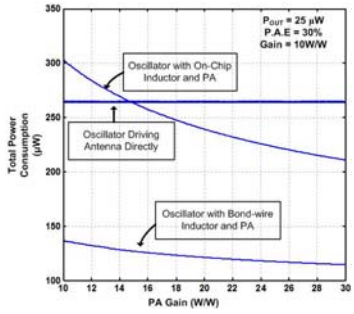

Figure 3: Total power consumption versus PA gain.

inductors driving a PA and an oscillator with bond-wire inductors driving a PA. When the level of integration is not an issue (i.e., off-chip components are allowed) it is noted that the oscillator with the high-*Q* (30-70) bond-wire and external inductors always uses less power than the other two architectures. If an efficient PA with gain > 20 is available, a PA with on-chip inductors (*Q* ≈ 5-10) is more efficient than an oscillator directly coupled to the antenna; however, for smaller PA gain, the directly-driven antenna should be chosen.

Keywords: BAN, Sensor Node, Class C, Reconfigurable

REFERENCES

[1] N. Cho, et al., "A 10.8 mW body channel communication/MICS dual-band transceiver for a unified body sensor network controller," *IEEE JSSC,* vol. 44, pp. 3459-3468, Dec. 2009.

[2] J. Bohorquez, et al., "A 350 µW CMOS MSK transmitter and 400 µW OOK super-regenerative receiver for medical implant communications," *IEEE JSSC,* vol. 44, pp. 1248-1259, April 2009.

[3] Y. Chee, et al., "An ultra-low-power injection locked transmitter for wireless sensor networks," *IEEE JSSC,* vol. 41, pp. 1740-1748, Aug. 2006.

TASK 1836.057, HIGH ACCURACY ALL-CMOS TEMPERATURE SENSOR WITH LOW-VOLTAGE LOW-POWER SUBTHRESHOLD MOSFETS FRONT-END AND PERFORMANCE-ENHANCEMENT TECHNIQUES

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SIGNIFICANCE AND OBJECTIVES

Modern digital VLSI technology calls for aggressive device/supply scaling and results in rapidly increasing power density, which presents great challenges to analog building blocks such as temperature sensor. This project will investigate advanced temperature sensor for dynamic thermal management in high performance digital processors.

TECHNICAL APPROACH

Traditionally, substrate PNP transistors are used in CMOS process as the temperature-sensing device. In order to further reduce the supply voltage, chip area, self heating effect, and make it compatible with modern digital processes, subthreshold MOSFETs and Schottky diodes will be investigated to replace substrate BJT as the core device. Bulk-driven technology will be investigated for low-voltage operation. Compared with limited prior art trials, this research aims to improve the precision of low-voltage operation by techniques such as automatic tuning, dynamic offset cancellation, dynamic element matching, and curvature correction. Special calibration techniques will be studied for the new sensing devices.

SUMMARY OF RESULTS

CMOS subbandgap reference circuits operating at low supply voltages were designed and tested [1-2]. To support low-voltage operation, the reference circuit uses NMOS transistors operating in subthreshold and a bulk-driven error correction amplifier. The simplified circuit, measurement results and chip microphotographs are shown in Fig. 1. The chip fabricated in AMI 0.5 µm CMOS technology can operate with a 1 V supply voltage to produce a reference voltage of 337 mV with a temperature coefficient of 9.9 ppm/^{0}C and a voltage coefficient of 290 ppm/V. The chip fabricated in UMC 0.13 µm CMOS technology can operate with a 0.4 V supply voltage.

Schottky diodes designed and fabricated in standard 45nm/90nm/130nm digital CMOS process have been characterized at different temperatures to obtain the statistical and temperature properties. The results are being summarized to submit for publication.

Three new designs are under fabrication/test. They include a low-voltage inverter-based sigma delta modulator, a 2×2 sensor front-end with dynamic element matching and subthreshold CMOS, and a sensor front-end with 8×8 Schottky diode array and modulated dynamic element matching.

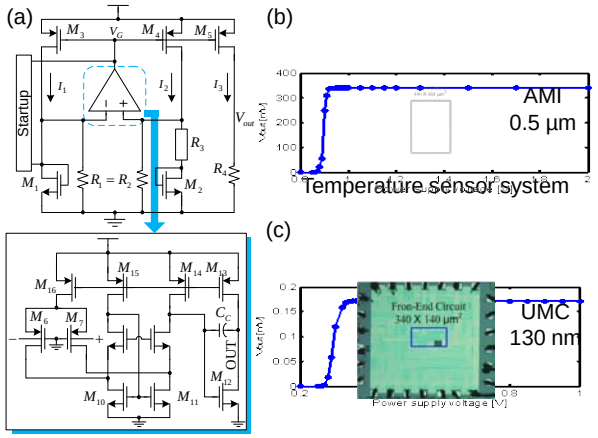

Figure 1: Simplified circuit (a) and measurement results of V_{ref} generated by sub-1V front-end in 0.5 µm CMOS process (b) and 0.4-V front-end in 130nm CMOS process (c) respectively.

In the second and third years of this project, the focus will be moved to system level design and test of scattered thermal sensing architecture that can be deployed in digital processors. Low-voltage operation that is robust against process variation, mismatch, and 1/f noise will be a key achievement. Low-cost calibration for the specific sensor devices will be provided.

Keywords: temperature sensor, subthreshold MOSFET, Schottky diode, dynamic element matching, calibration

INDUSTRY INTERACTIONS

Texas Instruments, Intel, IBM, and GLOBALFOUNDRIES

MAJOR PAPERS/PATENTS

[1] Y. Yang, et. al, "All-CMOS Subbandgap Reference Circuit Operating at Low Supply Voltage," IEEE ISCAS, Rio de Janeiro, Brazil, May 15~18, 2011.

[2] S. Block, et. al, "0.6-2.0 V, All-CMOS Temperature Sensor Front-End Using Bulk-Driven Technology," IEEE DCAS, TX, November 2010.

[3] Y. Yang, et. al, "Modeling and Optimization of Fast-Settling Time Gain-Boosted Cascode CMOS Amplifiers", IEEE SoutheastCon, March, 2010.

TASK 1836.058, HIERARCHICAL MODEL CHECKING FOR PRACTICAL ANALOG/MIXED-SIGNAL DESIGN VERIFICATION

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SIGNIFICANCE AND OBJECTIVES

Analog/mixed-signal (AMS) verification is a significant challenge to date and is confronted by the continuous nature of analog operations and complex analog behaviors. This project will develop hierarchical analog behavioral model equivalence checking techniques with an aim of enabling verification of large AMS designs.

TECHNICAL APPROACH

We propose a hierarchical model equivalence checking based verification approach, which is not completely formal, but yet systematic and applicable to large designs. A block-level behavioral model is compared with the corresponding electrical-level implementation (SPICE netlist) through equivalence checking in which signals are mapped between the behavioral and electrical domains with proper inclusion of electrical details or signal abstraction. The success in checking all the block-level models will enable the verification of the entire AMS design based on simplified behavioral models. A methodology that allows for iterative refinement of a behavioral model upon equivalence check failure will be also investigated.

SUMMARY OF RESULTS

As a first step towards analog behavioral model equivalence checking, we define proper mapping functions that relate signals in two domains: behavioral and electrical signal domains, as shown in Figure 1. Proper construction of such mapping functions is critical as checking a behavioral model against its electrical implementation (e.g. SPICE netlist) must take place across the two signal domains. In particular, we map a given behavioral input into the electrical domain by including certain electrical signal details (one-to-many mapping). This leads to a set of mapped electrical inputs. These electrical inputs are used to exercise the electrical implementation to produce a set of electrical outputs, which are then mapped back to the behavioral domain (many-to-one mapping) so as to be compared with output of the behavioral model. The two models are deemed equivalent if the maximum deviation between their outputs is less than a threshold for a chosen set of input stimuli.

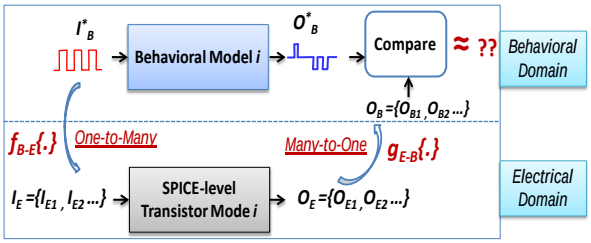

Figure 1: Mappings between behavioral & electrical domains.

With the mapping functions properly defined for a given analog circuit block, the equivalence checking can be done in an automated fashion using the algorithm flow shown in Figure 2. This optimization-based approach interfaces with a circuit simulator to find the maximum deviation between the two models. The proposed methodology has been initially demonstrated for the verification of a PLL that consists of several blocks.

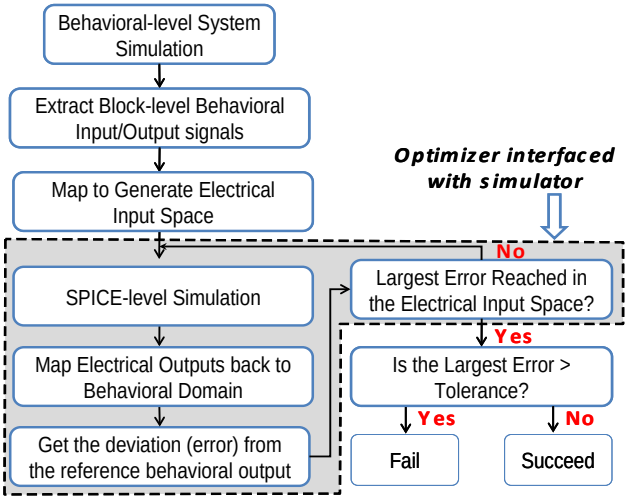

Figure 2: Optimization-based model equivalence checking.

Keywords: Analog verification, behavioral model equivalence checking.

INDUSTRY INTERACTIONS

Freescale Semiconductor

MAJOR PAPERS/PATENTS

[1] A. Singh and P. Li, "On behavioral model equivalence checking for large analog/mixed signal systems," IEEE/ACM Int. Conf. on Computer-Aided Design, November 2010.

TASK 1836.059, POWER-EFFICIENT 10-20GS/S ADCS FOR HIGH-SPEED COMMUNICATIONS

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SIGNIFICANCE AND OBJECTIVES

Next generation high-speed communication systems demand wide-bandwidth ADCs with sampling rate beyond 10GS/s. In serial links, wide-bandwidth ADCs followed by DSPs allow sophisticated equalization to correct fiber impairments and enhance channel spectral efficiency. Additionally, emerging wireless applications of the 10GHz UWB and newly unlicensed millimeter-wave-bands also demand such high-speed ADCs.

TECHNICAL APPROACH

The current state of the art ADC around 10-20GS/s achieves 24GS/s sample rate in 90nm CMOS. However, its power consumption is quite high at 1.2W (5pJ/conversion-step FOM, 5ENOB @ low frequencies). Yet, this is the best compared with previous ADCs around 10-20GS/s in CMOS, SiGe, and InP HBT technologies in terms of power and FOM. Another design uses two interleaved flash ADCs to achieve 12.5GS/s rate with 4.5-bit resolution. This research will investigate techniques for power-efficient 10-20GS/s ADCs with a FOM<0.1pJ/conversion-step and 5ENOB.

SUMMARY OF RESULTS

This research investigates using time-interleaved flash converters to achieve 10-20GS/s sampling rates. The accuracy of a flash ADC in CMOS is dominated by random offsets of comparators due to device mismatches. To improve the accuracy, large devices are needed to minimize device mismatches. However, this presents more parasitic capacitance to reduce the speed. To maintain a certain speed, larger current, therefore, larger power is required. Using offset calibration, smaller devices can be used to achieve the desired accuracy. Therefore, the speed is improved and the power consumption can be smaller, leading to better FOM.

Two new digitally controlled trimming offset calibration techniques have been proposed to calibrate preamplifier and comparator offsets and to minimize the loading of the calibration devices on the critical signal path to enhance ADC bandwidth.

Keywords: Time interleaved ADC, Flash ADC, ADC calibration, Power efficiency

INDUSTRY INTERACTIONS

Texas Instruments, IBM, Freescale

MAJOR PAPERS/PATENTS

[1] J. Yao and J. Liu, "A 5-GS/s 4-Bit Flash ADC with Triode-Load Bias Voltage Trimming Offset Calibration in 65-nm CMOS," in *Proc. Custom Integrated Circuit Conference*, Sept. 2011

TASK 1836.060, DESIGN TECHNIQUES FOR SCALABLE, SUB-1mW/Gbps SERIAL I/O TRANSCEIVERS

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PROF. PATRICK CHIANG, OREGON STATE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

Interface architectures which allow for high data rates at improved power efficiency levels are required to satisfy the growing I/O bandwidth in power-constrained environments. This project aims to improve the power efficiency of serial I/O transceivers to sub 1mW/Gbps for data rates ranging from 5-10Gbps.

TECHNICAL APPROACH

To enable the improvements in energy efficiency, a source-synchronous link is designed and implemented to operate over a wide range of data rates. Key features of the design include

- Half-rate transmitter and quarter rate receiver structures.
- Supply-scalable circuits to enable dynamic power management.
- A hybrid voltage-mode driver with low-complexity, high-resolution current-mode equalization.
- Resonant global clock distribution with switchable inductor for wide range of operation.
- Improved return-loss through inductive terminations.
- A novel multi-point injection locked ring oscillator that enables wide locking range and precise quadrature phase generation.

SUMMARY OF RESULTS

Figure 1 shows the complete block diagram of the designed link. The supply voltage is scaled with data rate to improve the power efficiency over the full range of operation. A prototype was completed and fabricated through MOSIS using the IBM 90nm process. Figure 2 shows the chip layout . The prototype includes two full transceiver links plus a forwarded clock transmitter.

Figure 1: Serial I/O transceiver architecture.

Analysis of jitter tracking in source-synchronous links was also completed. The performance impact of source synchronous link architectures and their tolerance to clock-to-data skew was explored. The study showed improvement in jitter tolerance accompanied with using injection locked oscillators for clock deskew at the receiver [1].

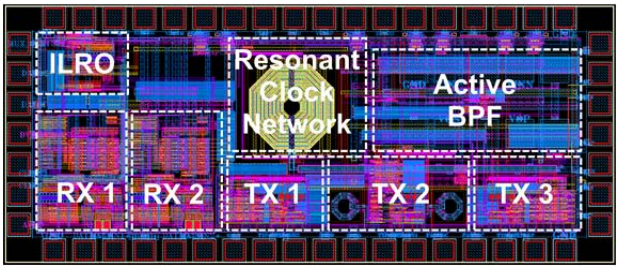

Figure 2: Chip layout in IBM 90nm Process.

In the second year of the project, the fabricated prototype will be tested and characterized to validate all the key ideas presented. The focus will move to further improve the energy efficiency of the link through scaling the supply voltage of all blocks to near-threshold operation [2]. The work will also extend to explore the optimal multiplexing ratio at which the transmitter would achieve maximum energy efficiency.

In the third year, this project will present a full 4-to-8-channel link including all clock generation circuitry. The emphasis of this design will be on improving wake-up times of the complete link. Further emphasis will be on power regulation methods to achieve improved turn on time for the full link.

Keywords: Voltage Mode Driver, Source Synchronous Clocking, Injection Locked Oscillator.

INDUSTRY INTERACTIONS

IBM, Intel, Texas Instruments.

MAJOR PAPERS/PATENTS

[1] A. Ragab, Y. Liu, K. Hu, P. Chiang, and S. Palermo, "Receiver Jitter Tracking Characteristics in High-Speed Source Synchronous Links," (submitted).
[2] K. Hu, T. Jian, S. Palermo, and P. Chiang, "Low-Power 8Gb/s Near-Threshold Serial Link Receivers Using Super-Harmonic Injection Locking in 65nm CMOS," CICC 2011.

TASK 1836.068, GLOBAL CONVERGENCE ANALYSIS OF MIXED-SIGNAL SYSTEMS

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SIGNIFICANCE AND OBJECTIVES

Today, many modern mixed-signal systems including oscillators, phase-locked loops, and DC-DC converters suffer from fatal start-up failures due to ill-defined initial states, yet their existence is extremely difficult to detect using a brute-force simulation approach. This task aims to find practical tools and methodologies to prevent such global convergence failures.

TECHNICAL APPROACH

This task seeks practical methods or tools rather than a rigorous mathematic proofing tool since a theoretical approach to establish a global stability of a general system has been an unsolved problem for nearly a century.

So far, two approaches have been investigated in this task: (1) cluster split detection algorithm and (2) indeterminate state ('X') elimination approach [1-2]. The former detects the existence of false convergence states while the latter prevents the false convergence by advising designers where to add resets. Both approaches involve running multiple circuit simulations with randomly initialized states and one of the objectives is to minimize its computational cost.

SUMMARY OF RESULTS

The first approach, cluster split detection, detects the existence of false convergence states by examining whether multiple state points each originated from a randomly chosen initial state form more than one disjoint clusters in the state space.

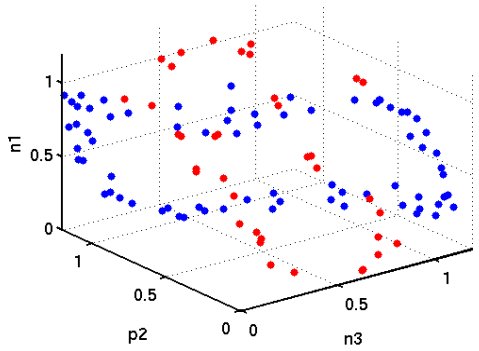

Figure 1: Detection of false convergence states using cluster split detection algorithm. Illustration for a coupled ring oscillator that has two possible oscillation modes.

The second approach, indeterminate state ('X') elimination, is in fact analogous to the way the start-up failures are prevented in digital systems. The unknown states (called X's in modern logic simulators) for analog circuits are identified based on the entropy of the state distribution (Fig. 2). Then the designers are advised to add resets where the X's are found, yielding a system which will always start from a known state upon reset.

The two described approaches have been demonstrated on real circuit examples including oscillators, phase-locked loops, and DC-DC converters.

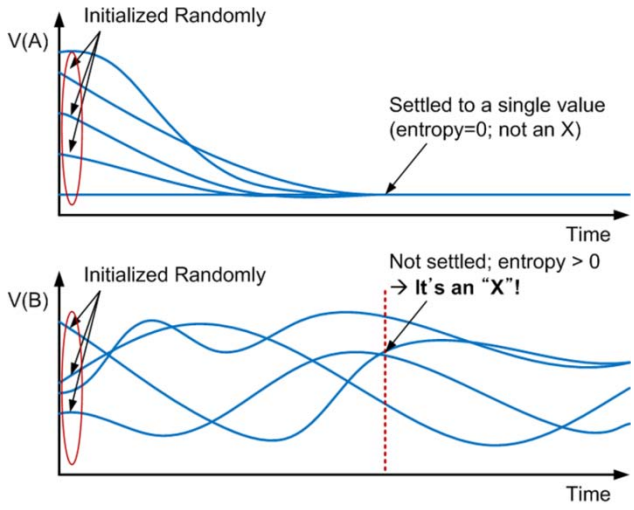

Figure 2: Determination of unknown states ('X') for analog circuits based on entropy analysis. If a circuit node voltage does not settle to a single possible value within a certain time, it is deemed an 'X' and may have to be initialized at start-up.

Keywords: Global convergence, start-up failures, mixed-signal systems, circuit simulation, formal analysis.

INDUSTRY INTERACTIONS

Texas Instruments.

MAJOR PAPERS/PATENTS

[1] S. Youn, J. Kim, M. Horowitz, "Global Convergence Analysis of Mixed-Signal Systems," ACM/IEEE Design Automation Conference (DAC), June 2011.

[2] S. Youn, J. Kim, M. Horowitz, "Preventing Global Convergence Failures in Mixed-Signal Systems by Eliminating Indeterminate States," Frontiers in Analog Circuit Synthesis and Verification (FAC), July 2011.

TASK 1836.072, LOW COST TEST OF HIGH SPEED SIGNALS

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SIGNIFICANCE AND OBJECTIVES

The goal of this project is to reduce the cost of traditional high speed test setup by replacing high speed test equipment with low cost equipment and back end signal processing.

TECHNICAL APPROACH

The cost of high speed signal acquisition is dominated by equipment cost. By the use of intelligent signal processing algorithm, the use of costly equipment can be restricted to a single front end component. However, it must be ensured that the algorithm used is light weight enough to be implemented on a low latency test setup where the time of signal acquisition is important.

The two major techniques that are being considered for this project are jitter expansion and incoherent under sampling of data. While jitter expansion can provide a simple solution to the problem of sub pico-second jitter measurement, waveform reconstructed from under-sampled data can be used for system performance characterization at extremely high speed without the use of a waveform-synchronous trigger.

SUMMARY OF RESULTS

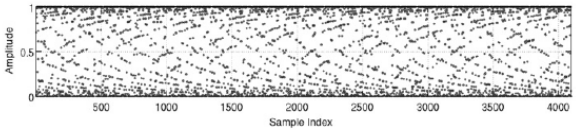

Figure 1(a)

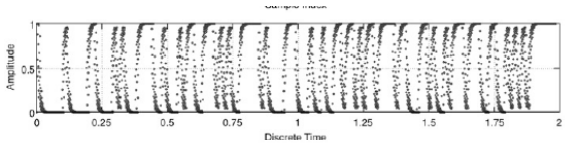

Figure 1(b)

Figure 1: (a) Raw under sampled data of PRBS waveform (b) Reconstructed waveform

This project is primarily focused on reconstruction and characterization of periodic waveform. This includes single tone, multi-tone and pseudo random bit sequence, and thus covers most waveform commonly used for test purpose. Interestingly, an algorithm that is developed for periodic waveform can also be used for extraction of the eye of a general bit stream with minor modification. This is because the eye is derived by folding the signal waveform over one unit interval and is invariant to translation by integer multiple of unit interval.

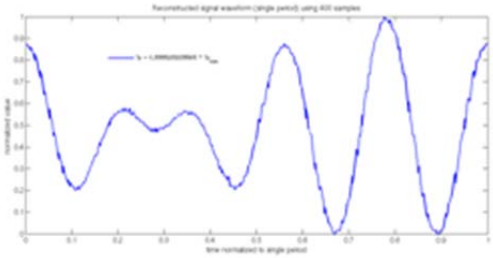

Figure 2: Reconstructed two-tone waveform. x-axis is time normalized to one waveform period, y-axis is sample values normalized to max amplitude.

In figure 1 we present an example of reconstruction of pseudo random bit sequence from incoherently under-sampled data points. Figure 1a shows the raw acquired data arranged in a time base modulo some arbitrary period; while, figure 1b shows the same samples arranged in a time base modulo the actual period of the PRBS waveform. In figure 2 we show a reconstructed two tone waveform. We have developed a time domain cost metric for estimation of frequency which leads to a saving of O(log N) calculations per iteration compared to frequency domain cost metric. It also requires 5 times less number of samples to achieve same accuracy of frequency estimation.

Keywords: High-Speed, test, under-sampling, jitter measurement

INDUSTRY INTERACTIONS

Intel
Texas Instruments

MAJOR PAPERS/PATENTS

[1] Debesh Bhatta et al. Time Domain Characterization and Test of High Speed Signals Using Incoherent Subsampling, ATS 2011 (Accepted for presentation)

[2] Hyn Choi et al Signal Acquisition of High-Speed Periodic Signals Using Incoherent Sub-Sampling and Back-End Signal Reconstruction Algorithms, IEEE Trans. VLSI Syst. 2011

TASK 1836.073, A MODEL-VIEW-CONTROLLER (MVC) PLATFORM FOR ADAPTIVE TEST

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SIGNIFICANCE AND OBJECTIVES

Adaptive test is an emerging approach to dynamically modify the test plan for RF devices with high specificity: per wafer or per device. This project will develop a model view controller (MVC) framework and statistical learning theory/machine learning methods necessary to support industrial adaptive test.

TECHNICAL APPROACH

We will architect an adaptive test MVC framework with: (i) Models, which will serve as abstractions of existing industry production databases, (ii) Views, which will provide test engineers feedback on adaptive test algorithms, and (iii) Controllers, which will contain modular adaptive test components to be employed at each stage of testing. We anticipate treating these adaptive test components as "applications", which consist of algorithms for each stage of data collection and processing (inline/kerf, wafer final test, module final test, field returns, etc.). By standardizing the controller platform we can encourage the emergence of an adaptive test "application ecosystem", simplifying deployment.

SUMMARY OF RESULTS

There is growing industrial interest in deploying so-called “adaptive test”, or dynamically modifying the test plan. Adaptive test is particularly challenging for analog and RF testing, where testing is already a complicated and expensive endeavor. In this project, we posit that achieving meaningful results for adaptive test in the analog and RF test domain will require statistical models that are at parity of sophistication with the complexity of the test problem. To address this, we develop a model-view-controller architecture that responds to the challenges of adaptive test for analog and RF devices with an elegant and modular solution, enabling rapid deployment of novel statistical methods as they become available, while keeping test engineers well-informed about the inner workings of the deployed adaptive test system.

Our first case study in an MVC adaptive test solution was early test metric estimation for analog and RF devices. We developed MVC components to enable us to generate synthetic populations of more than 1 million devices (via a non-parametric kernel density estimation controller) from early production hardware, and predict expected test escape and yield loss test metrics with a very high degree of accuracy. The results of this study are shown in Figure 1, where the blue and red solid horizontal lines represent the estimated test escapes and yield loss relative to the long-term means, as shown in Figure 1.

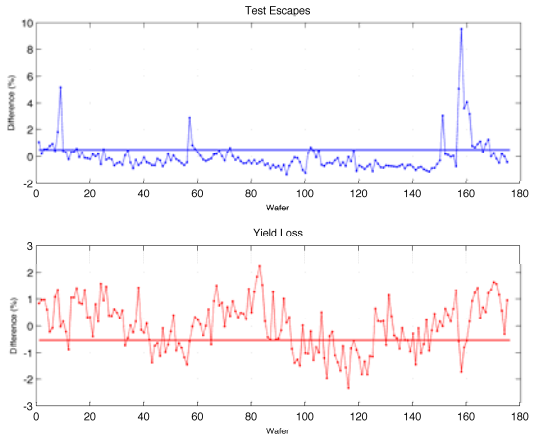

Figure 1: Test metric estimation

In the second and third years of the project, we plan to extend our framework to near real-time and real-time adaptive test applications, while also developing scalability via cloud computing infrastructure, as outlined in our submitted Design & Test paper. Further work will ultimately lead to a mature MVC platform that enables straightforward and manageable deployment of adaptive test methodologies that leverage state-of-the-art statistical learning theory, machine learning, and massively parallel computing for cutting edge testing.

Keywords: analog/RF, adaptive test, test metric estimation, machine learning

INDUSTRY INTERACTIONS

Texas Instruments, IBM

MAJOR PAPERS/PATENTS

[1] N. Kupp et. al. “On Proving the Efficiency of Alternative RF Tests,” ICCAD 2011 (accepted).

[2] N. Kupp et. al. “PPM-Accuracy Error Estimates for Low-Cost Analog Test: A Case Study,” IMS3TW 2011 (best student paper award).

[3] N. Kupp et. al. “Applying the Model-View-Controller Paradigm to Adaptive Test,” IEEE Design & Test 2011 (submitted).

TASK 1836.075, DESIGN OF 3D INTEGRATED HETEROGENEOUS SYSTEM

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SUNG-KYU LIM, GEORGIA INSTITUTE OF TECHNOLOGY

SIGNIFICANCE AND OBJECTIVES

The proposed research is a pioneering effort in *3D integrated heterogeneous system (3D-IHS)*. This objective of this research is to address the integration challenges of highly different circuits/systems with varying technology, power profiles, operating voltage, and clock domains through the 3D technology using Through-Silicon-Via (TSV).

TECHNICAL APPROACH

The performance, power, and reliability of a 3D-Integrated Heterogeneous System (3D-IHS) depend on the functionality, power profile, and frequency of individual dies; the non-uniformity in their physical environments; die-to-die coupling; and die-to-package coupling. This research will develop design methods for the 3D-IHS and transform them into design tools and silicon prototype. This project will develop design methods and tools for power/clock delivery, signal integrity, and die-to-die communication in 3D integrated heterogeneous systems. The technical approach integrates modeling, circuit techniques, and physical design to deliver design tools and silicon prototype.

SUMMARY OF RESULTS

The anticipated results of this project includes (a) analysis of challenges to 3D integration of highly different circuits/systems with varying technology, power profiles, operating voltage, and clock domains using TSVs; (b) design methods for 3D integrated heterogeneous systems (3D-IHS), and (c) their demonstration considering case studies for high-performance and embedded applications. Our current progress has made following major observations:

- *TSV Defects and Signal Recovery:* We have developed an on-chip test and signal recovery circuit to detect TSV defects and if required perform signal recovery [1]. The circuit detects the resistive shorts through the oxide liner in a TSV before bonding and variation in TSV/bonding resistance after bonding considering open. The test circuit reconfigures itself as a signal recovery circuit for TSVs with weak defects to maintain the signal fidelity of the system.
- *TSV*-to-TSV coupling: We have modeled the TSV-to-TSV coupling in 3D ICs [2]. A full-chip analysis flow is developed based on the coupling model. Analysis results showed that TSVs cause significant coupling noise and timing problems despite that TSV count is much smaller compared with the gate count. TSV shielding and buffer insertion are explored as possible approaches to alleviate TSV-to-TSV coupling. We show that both approaches are effective in reducing the TSV-caused-coupling and improving timing.
- *TSV*-to-Device Interaction: We have showed the interactions 3D Via potential and electrical behavior of neighboring transistors. Considering a 3D stack of Fully-Depleted Silicon-On-Insulator (FDSOI) devices and using device simulation, we have shown that the back-gate electric field of FDSOI devices can be significantly modulated by potential of Through-Oxide-Via (TOVs) placed in close proximity [3]. Consequently changes in the TOV potential result in variation in threshold voltage and leakage current of neighboring FDSOI devices.
- Clock-Delivery in 3D ICS and Effect of 3D Vias: We have presented 3D clock delivery methods. Our methodology optimizes the number of TSVs and buffers, and their placements to design robust 3D clock trees [4]. We have observed that increasing the number of TSVs significantly reduces the clock skew. Further, the use of multiple TSVs in the 3D clock tree helps reduce the variability in the clock-skew due to process variations in TSVs, transistors, and 2D wires.

Keywords: 3D integration, Heterogeneous System, Signal Integrity, Die-to-die coupling, Through-Silicon-Vias

INDUSTRY INTERACTIONS

Global Foundries, IBM, and Intel Corp,

MAJOR PAPERS/PATENTS

[1] M. Cho, et. al. "Pre-bond and Post-bond Test and Signal Recovery Structure to Characterize and Repair TSV Defect Induced Signal Degradation in 3D System," accepted for publication in *IEEE TCPMT*.

[2] C. Liu, et. al. "Full-Chip TSV-to-TSV Coupling Analysis and Optimization in 3D IC", DAC, 2011.

[3] A. Trivedi et. al. "Through-Oxide-Via Induced Back Gate Effect in 3D Integrated FDSOI Devices," *IEEE EDL, vol 32, no. 8, Aug. 2011*, pp. 1020-1022

[4] X. Zhao*, et. al. "*Variation-Tolerant and Low-Power Clock Network Design for 3D ICs," *ECTC*, 2011

TASK 1836.076, ULTRA-LOW POWER DELAY-INSENSITIVE ASYNCHRONOUS CIRCUITS

PI: DR. JIA DI, UNIVERSITY OF ARKANSAS, JDI@UARK.EDU
CO-PI: DRS. SCOTT C. SMITH AND H. ALAN MANTOOTH

SIGNIFICANCE AND OBJECTIVES

Leakage power has become a critical factor for deep submicron digital CMOS ICs. This project will evaluate the integration of MTCMOS power gating with delay-insensitive asynchronous logic for reducing leakage in both active and standby modes, as well as explore the ultra-low voltage asynchronous circuit design opportunity.

TECHNICAL APPROACH

Since the spacer cycle of a dual-rail delay-insensitive asynchronous component is equivalent to gating the power of this component and forcing the output to logic 0, these circuits can enter sleep mode after every data cycle, while the circuit is in operation, and the handshaking signals between registers can be used as sleep control signals to control the power gating transistors. This approach has several merits: 1) limiting leakage in both active and sleep modes; 2) alleviating the effort and complexity of designing the sleep signal generation mechanism; 3) reducing the area overhead; and 4) facilitating the tool flow development.

SUMMARY OF RESULTS

Delay-insensitive asynchronous logic like the NULL Convention Logic (NCL) utilizes dual-rail encoding to achieve delay-insensitivity. The truth table of a dual-rail signal is shown in Table 1. The architecture of NCL systems consists of delay-insensitive combinational logic sandwiched between NCL registers, which use handshaking signals to coordinate circuit behavior. After a DATA state, the circuit needs to undergo a NULL state before the next DATA state in order to avoid the previous data being overridden by the next data.

Table 1: Dual-Rail Signal Truth Table

State	DATA0	DATA1	NULL	Invalid
Rail 1	0	1	0	1
Rail 0	1	0	0	1

NCL circuits are comprised of 27 threshold gates. The primary type of threshold gate is the THmn gate, where $1 \leq m \leq n$. THmn gates have n inputs; at least m of the n inputs must be asserted before the output will become asserted; and NCL threshold gates are designed with *hysteresis* state-holding capability, such that after the output is asserted, all inputs must be deasserted before the output will be deasserted.

MTCMOS power gating structure is incorporated into each threshold gate. Due to the removal of reset and hysteresis functions, the resulting gates are actually smaller, as shown in Figure 1 (circuited transistors are high-V_t). Moreover, sleeping instead of propagating NULL allows for the use of input-incomplete functions, which significantly reduces area.

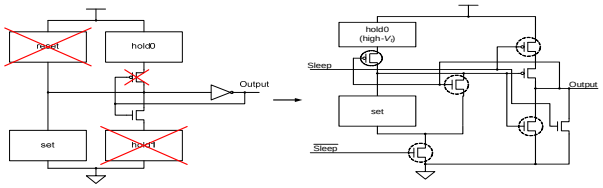

Figure 1: Incorporating MTCMOS Power Gating into NCL Threshold Gates

In order to maintain delay-insensitivity and maximize leakage saving, a series of innovations including early-completion detection, sleep-enabled register and completion detection unit design, have been applied. Handshaking signals, which indicate the DATA/NULL status of pipeline stages, can be used as sleep control signals. Figure 2 shows the overall MTCMOS NCL (MTNCL) architecture.

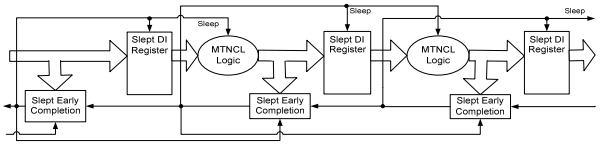

Figure 2: MTNCL Architecture with Sleeping Combinational Logic, Completion Detection, and Registers

Keywords: MTCMOS, delay-insensitive, asynchronous, ultra-low power, CAD tool

INDUSTRY INTERACTIONS

Texas Instruments, Intel, IBM

MAJOR PAPERS/PATENTS

[1] L. Zhou, S. Smith, and J. Di, "Bit-Wise MTNCL: an Ultra-Low Power Bit-Wise Pipelined Asynchronous Circuit Design Methodology," *2010 IEEE Midwest Symposium on Circuits and Systems*, August 2010

[2] D. Coleman and J. Di, "Analysis and Improvement of Delay-Insensitive Asynchronous Circuits Operating in Subthreshold Regime," *Journal of Low Power Electronics*, Vol. 6, NO. 2, pp. 320-324, August 2010

TASK 1836.077, STATISTICAL CHARATERIZATION OF CIRCUIT AGING

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SIGNIFICANCE AND OBJECTIVES

Interconnects used in clock buffers, signal buses, network-on-chips, memory wordlines/bitlines, and high-speed I/Os are critical components in modern ICs. The resistance and capacitance associated with long wires, which have not scaled well in advanced processes, may result in aging behavior in interconnect dominated paths that is drastically different from logic dominated paths. Although there have been previous works showing the impact of fanout load on transistor aging, practically no attention has been paid to the aging behavior in interconnects with long wire loads. For the first time, this work presents measurement results highlighting the dependence of Bias Temperature Instability (BTI) and Hot Carrier Injection (HCI) induced aging on wire length.

TECHNICAL APPROACH

The previous "all-in-one" silicon odometer framework [3-4] was adopted to separate the BTI and HCI contributions with picosecond order resolution and microsecond measurement interrupts. Measurements from a 65nm test chip show that BTI-induced degradation decreases with longer interconnect lengths while HCI exhibits a non-monotonic behavior with interconnect length. A simple model is proposed using circuit parameters that affect the BTI and HCI degradation in interconnect drivers.

SUMMARY OF RESULTS

Interconnect length vs. BTI: The BTI induced frequency shifts after 19 hours of stress at 2.4V are shown in Fig. 1. The amount of BTI aging monotonically decreases with longer interconnect lengths for the different stress conditions. This can be explained by the longer transition time with longer wires which results in a shorter time period the transistors are exposed to a full BTI stress bias. Fig. 1 also reveals a weaker interconnect length dependency for a lower AC stress frequency of 100MHz due to the smaller fraction of time spent on signal transition compared to a higher frequency of 300MHz.

Interconnect length vs. HCI: The effect of HCI in Fig. 2 shows a non-monotonic relationship with wire length. This is a somewhat unexpected trend and can be attributed to two factors: (i) a longer wire reduces the peak current through the transistors which has the effect of a smaller effective stress voltage. The reduction in stress voltage can be expressed as the ratio between the transistor resistance and the wire resistance. (ii) A longer wire makes the current pulse wider due to the larger wire capacitance which has the effect of increasing the effective stress time compared to a shorter wire. The combined effect can be used to explain the non-monotonic relationship in Fig. 2.

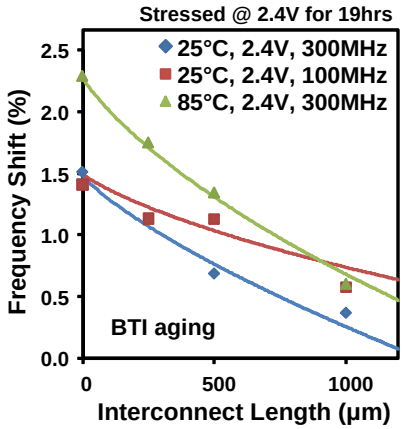

Figure 1: Measured BTI data (in markers) and modeling results (lines) show good agreement.

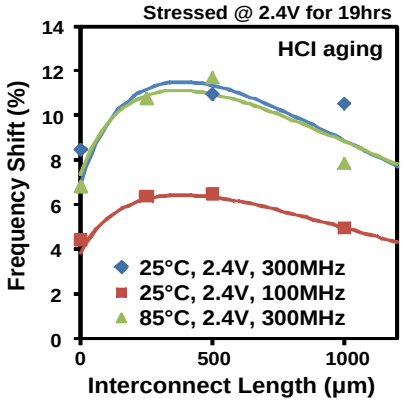

Figure 2: Measured HCI data (in markers) and the proposed HCI model (lines) show good agreement across different interconnect lengths and stress conditions.

Keywords: interconnect odometer, BTI, HCI.

INDUSTRY INTERACTIONS

Regular telecom with Texas Instruments, Freescale, IBM
PI visits: Intel, Global Foundries

MAJOR PAPERS/PATENTS

[1] X. Wang, P. Jain, D. Jiao, C.H. Kim, "Impact of Interconnect Length on BTI and HCI Induced Frequency Degradation", IEEE International Electron Devices Meeting (submitted)

TASK 1836.078, HIGH-RESOLUTION, CHARGE-BASED A/D CONVERTERS FOR NANO-CMOS TECHNOLOGIES

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SIGNIFICANCE AND OBJECTIVES

The successive approximation register (SAR) ADC architecture is attractive for integration in aggressively scaled CMOS, primarily since it does not rely on linear amplification blocks. This project aims to push the performance of SAR ADCs to the next level achieving both high resolution (~12bits) and high speed (>150MHz) in 40/65nm CMOS technology. These specifications are required e.g. in wireless base station receivers.

TECHNICAL APPROACH

Aggressive scaling of unit capacitances in a SAR ADC allows the designer to set the input capacitance according to the thermal noise limit, resulting in lower switching energy and faster conversion speed. Recently published SAR ADC's have reported unit capacitors in the range of 0.5 – 1 fF, but little data is available for their matching characteristics. An innovative test structure to measure these mismatch characteristics has been designed and sent out for fabrication. In addition, a prototype IC to validate the idea of time constant matching is currently being designed. Findings from the above-described two chips will be used to design the final SAR ADC targeting resolution >12 bits, and f_s = 200 MHz.

SUMMARY OF RESULTS

The top level schematic of the test structure designed to measure mismatch characteristics of small unit caps is shown in Figure 1. It consists of a capacitance array, a comparator and a thermometer coded resistive DAC. The comparator and the resistive DAC together operate as a linear SAR ADC. The capacitances in the array are switched in order to generate a (mismatch-induced) error voltage that is subsequently digitized using the SAR ADC. These digital codes are then used to estimate the mismatch variance of the unit caps used in the array. For this prototype IC, two sets test structures were designed with unit capacitances of 0.5 fF and 1.5 fF, respectively. 48 such test structures each were put on the die to guarantee sufficient statistics. The chip layout is shown in Figure 2 Measurement result for this chip will be available in early 2012.

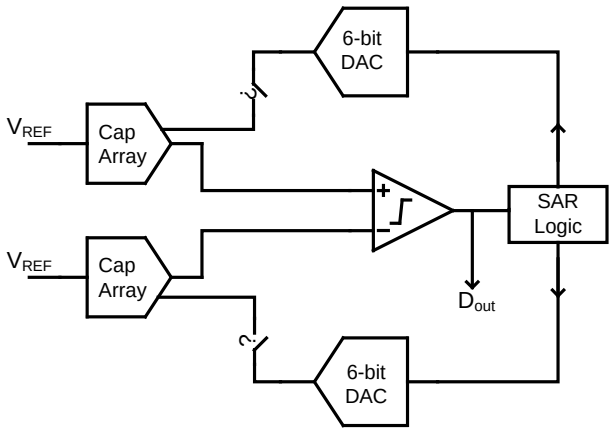

Figure 1: Test structure for measuring variance of small capacitors. Two such structures with unit caps of 0.5 fF and 1.5 fF have been designed.

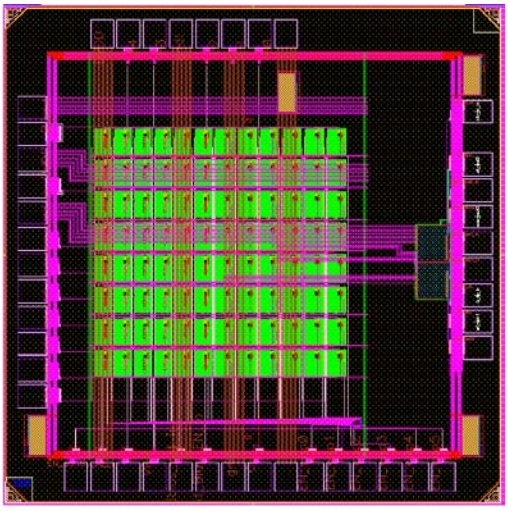

Fig.2 Layout of the chip designed to measure the mismatch characteristics of small capacitances.

Keywords: Capacitor matching, Time constant matching, CMOS, Successive approximation, ADC

INDUSTRY INTERACTIONS

Texas Instruments, Freescale

TASK 1836.080, VARIATION-TOLERANT NOISE-SHAPING ADCS WITH EMBEDDED DIGITAL BIAS AND VDD SCALABLE FROM 0.5V TO 1.2V FOR NANOSCALE CMOS

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SIGNIFICANCE AND OBJECTIVES

We introduced and demonstrated different design techniques and architectures for analog circuits down to 0.5V in earlier research. However, with the continued advances in CMOS technologies and applications, it is desirable to develop digital assisted solutions for high performance interface circuits that can operate under flexible supply voltages. This project proposes to investigate the in-situ digital biasing techniques for supply scalable analog interfaces on nano-scale CMOS processes.

TECHNICAL APPROACH

A supply scalable continuous-time sigma delta modulator with embedded digital biasing will be designed and fabricated to learn about the opportunities of digital intensive biasing techniques. A continuous-time implementation offers relaxed sampling network requirements and largely eliminates signal-path switches which is advantageous for low voltage operation. Digital biasing loops will be investigated for scalable supply operation and further avoids the use of large area of passive components. It is anticipated that the digital intensive biasing solutions will be very compact and flexible so that they enable in-situ biasing for each block.

SUMMARY OF RESULTS

The architecture of a cascaded 2-1 CT sigma-delta modulator with digital noise cancellation filters is shown in Figure 1.

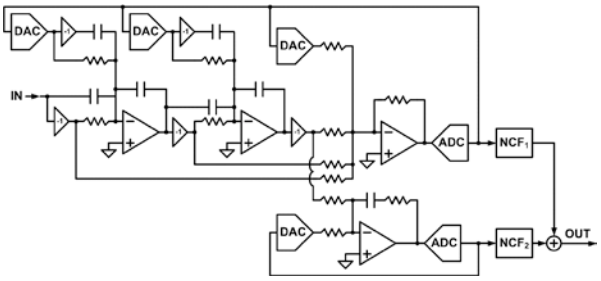

Figure 1: Architecture of a cascaded 2-1 CT SDM.

By using system level simulations, the design requirements of building blocks have been evaluated, such as operational trans-conductance amplifier unity-gain bandwidth, DC gain and continuous-time filter component value (RC) tolerance.

For the scalable supply operation, a digital supply monitoring circuit that depends on the supply voltage is planned to setup the bias configuration. To optimize the signal swing at the different supplies, a digital biasing loop to the common-mode biasing is proposed in this project. An example of an amplifier with digital biasing loop that is currently under investigation is shown in Figure 2.

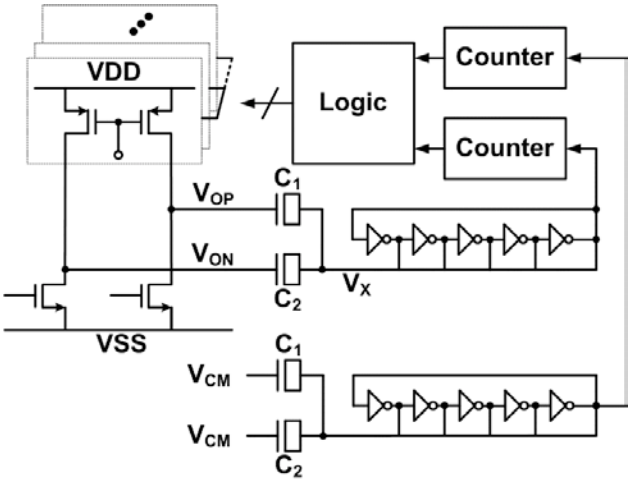

Figure 2: An example of an amplifier with digital biasing loop.

INDUSTRY INTERACTIONS

Doug Garrity, Freescale

Manar El-Chammas, Texas Instruments

TASK 1836.084, SINGLE SET-UP DETAILED TESTING OF WIRELESS TRANSCEIVER FRONT-ENDS USING DIGITAL PROCESSING

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SIGNIFICANCE AND OBJECTIVES

Loop-back testing has many advantages for RF transceivers, including the elimination of RF testers and ease of on-chip implementation. However, it is rarely used due to the coupling between RX and TX parameters. This project aims at developing techniques for detailed characterization in the loop-back mode.

TECHNICAL APPROACH

In the loop-back mode, signals are applied at the transmitter input and are captured at the receiver output. These signals are all in the baseband domain. The input-output relation of this complete path is affected by all parameters of the system and this relation is often complex. An analytical model of the system can be derived including all the parameter of interest but cascading the behavior of blocks in the path. This model can be used to extract the parameters of the system through signal processing and intelligent signal design that helps in decoupling the effects of various parameters.

SUMMARY OF RESULTS

The analytical model of a transceiver system includes the behavior of the system blocks, such as DACs, LNAs, filters, etc. and their parameters. Most of the important impairments of the system can be included in the model. These parameters include mismatches in the IQ path, including phase and gain mismatch and time skews. In addition DC offsets and non-linearity coefficients affect the performance of the overall system and need to be characterized. Figure 1 shows an example for the model of the overall transceiver with these parameters.

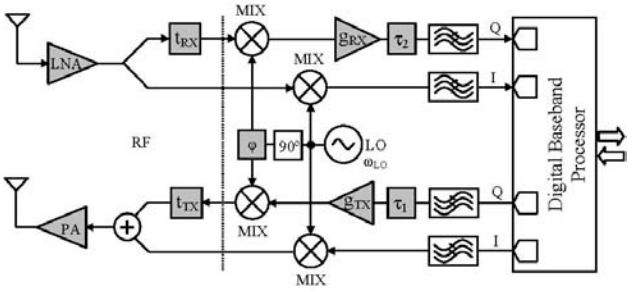

Figure 1: An example of the TX-RX loop-back model that includes the parameters of interest

Based on this model, it is possible to analytically express the output signal based on the input signals and system parameters. The relation between the input-output signals will be a complex function of the modeled system parameters. Once this model is derived, multiple techniques can be used to process the input-output signals to derive the internal parameters of the system. In this work, we have used non-linear signal estimation techniques (NLS) for this purpose. This technique has been demonstrated for simple GSM systems as well as more complex WiMax systems on experimental platforms that span from using multiple test equipments (vector signal generators and analyzers) as devices under test from using off-the shelf components to build transceivers, to using commercial transceivers.

Test signal design is an important part of success for such an approach. At any step of the testing, the power of the modulated test signal significantly affects the accuracy of the extraction process. The test signal power needs to be set in a way to emphasize the effect of desired parameters. In some cases, this is not possible for all the parameters of interest at once. Multi-step extraction techniques have been developed to solve this problem.

Table 1 shows sample results for parameter extraction using two testers as DUT.

Table 1: Extraction Accuracy for a Loop-back System that Includes Two Testers

Parameter	Injected	Mean	ST Dev.	RMS Error
ϕ_{Tx}	5.0°	4.936°	0.202°	0.207°
g_{Tx}	-0.25	-0.256	0.0079	0.095
ϕ_{Rx}	-4.3°	-4.347°	0.146°	0.150°
g_{Rx}	0.1	0.095	0.0038	0.0059
τ_1	38 ns	39.28 ns	0.79 ns	1.49 ns
τ_2	51 ns	48.70 ns	2.23 ns	2.53 ns
DC_I	0.2 V	0.195 V	2.57 mV	5.55 mV
DC_Q	0.15 V	0.155 V	3.95 mV	6.33 mV
Parameter	2-tone	Mean	ST Dev.	RMS Error
$TX-IIP_3$	24.70 dBm	24.32 dBm	0.23 dB	0.43 dB
$RX-IIP_3$	16.97 dBm	17.84 dBm	0.34 dB	0.94 dB

Keywords: RF test, loop-back, RF Built-in-self-test, IQ mismatch, non-linearity

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] E. S. Erdogan and S. Ozev, "Detailed Characterization of Transceiver Parameters Through Loop-Back-Based BiST", IEEE TVLSI, V.18, N.6, June 2010, pp.901-911.

[2] A. Nassery, S. Ozev, M. Verhelst, and M. Slamani, "Extraction of EVM from Transmitter System Parameters", IEEE ETS, pp. 75-80, May 2011.

TASK 1836.086, VARIATION TOLERANT CALIBRATION CIRCUITS FOR HIGH PERFORMANCE I/O

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SIGNIFICANCE AND OBJECTIVES

Process variation degrades operation of analog subsystems and high performance I/O. While sources of process variation are well understood, methods to combat its effects are ad-hoc with power and area costs. This project explores circuit techniques to improve calibration of high performance I/O blocks at a reduced cost.

TECHNICAL APPROACH

Year one of this project focuses on current mode calibration DAC's with improved INL and DNL. This is accomplished through combining two methods. First, extra redundant DAC cells are added to enable elimination of "outlier" high variation cells. Second, cells are selected in an order such that the variation in the sum (INL) is reduced. Careful design of all circuits is required to reduce overhead and allow low power operation.

In subsequent years, similar design techniques will be applied to design of low offset comparators. Stochastic design approaches to reduce variation with knowledge of local correlations will also be explored.

SUMMARY OF RESULTS

Since the initiation of this project in February, methods to improve the linearity of calibration DAC's for application to high performance I/O have been studied and simulated. Based upon these results, an 8 bit current mode calibration DAC with 16 redundant cells has been designed and sent for fabrication. In addition to implementing the redundant cells an encoding/decoding scheme to identify and eliminate high variation cells has been implemented. Figure 1 shows the results of Monte Carlo simulation of DNL a current mode DAC based on the extracted layout. Several Monte Carlo simulations from extracted layout of the DAC were performed, each with improvement in DNL individually (typically between 20-100%).

In addition, a scheme to select rows of the DAC in the best order to preserve INL has also been instantiated and taped out in 65nm CMOS. Matlab simulation of 3-sigma INL shows almost 2X improvement expected for this scheme based upon 5000 samples. This gives an indication of improvements in yield.

Fabricated silicon designs are expected to return for measurement in the fall.

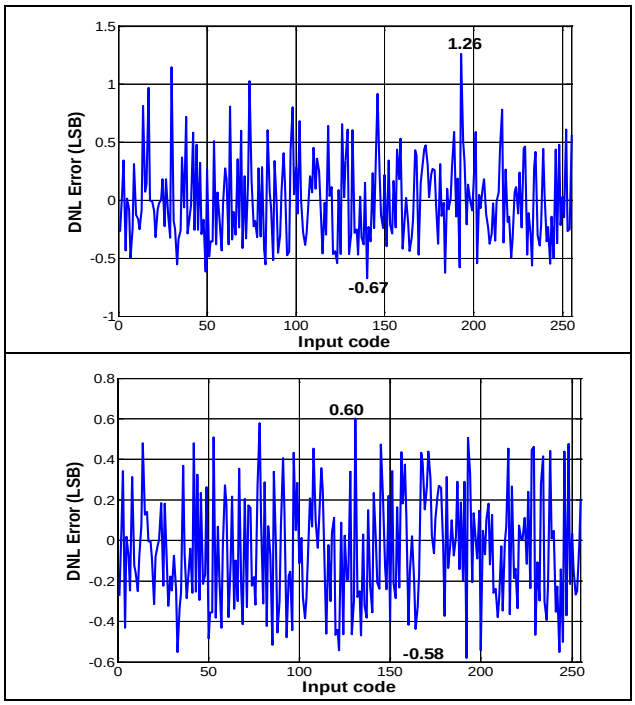

Figure 1: DNL from Monte Carlo simulation based on extracted layout of DAC without (top) and with (bottom) addition of redundant cells. Redundancy improves DNL from 1.26 to 0.6

In years two and three of this project measurement of calibration DAC's will continue, and in addition we will study the design of low input offset receiver comparators. Candidate approaches to improve input matching include adding a redundant input branch that can be eliminated, use of a dynamic matching approach to switch input polarities and average out errors, traditional feedback loops, and use of local stochastic correlation to reduce variation in input pairs. Impact of improved calibration will be measured by applying these designs and DAC designs to models of I/O systems.

Keywords: process variation, calibration, INL, DNL, receiver offset

INDUSTRY INTERACTIONS

Intel, IBM

MAJOR PAPERS/PATENTS

TASK 1836.087, AN ANY-DATA-RATE REFERENCE-LESS DIGITAL CLOCK DATA RECOVERY WITH DECOUPLED JITTER TRANSFER AND JITTER TOLERANCE

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SOUTHEN METHODIST UNIVERSITY PGUI@LYLE.SMU.EDU

SIGNIFICANCE AND OBJECTIVES

Clock-Date-Recovery (CDR) circuits are typically analog intensive, power consuming, occupying large silicon area, and requiring a reference clock. The objective of this project is to design a truly-digital reference-less CDR that can handle any data rate up to 16 Gb/s with small silicon area, low power and superior jitter performance.

TECHNICAL APPROACH

Our CDR architecture employs a novel digital scheme where frequency acquisition and phase detection are performed in lower-speed digital domain, resulting in very low power dissipation and small silicon area. Using a wide-band DCO and wide-band Phase interpolator (PI) along with a frequency locking loop (FLL), the architecture can accommodate data rate from hundreds of MHz to 16 GHz, and automatically detect and acquire the new data rate without the need for an external reference clock. In addition, the DPLL architecture can achieve superior jitter performance by decoupling jitter transfer and jitter tolerance without introducing jitter peaking.

SUMMARY OF RESULTS

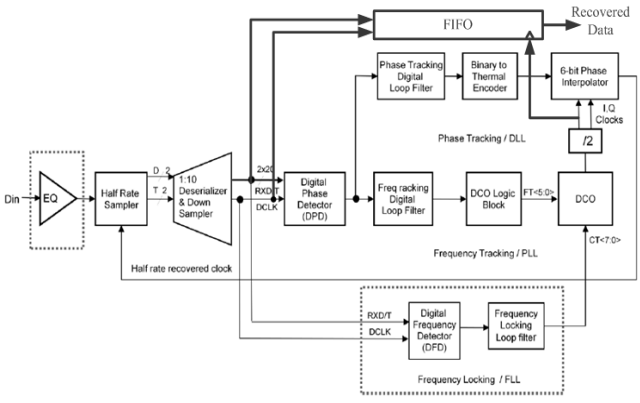


Figure 1: The DPLL-PI-based reference-less digital CDR.

The project started in March 2011. Fig. 1 shows the PI-DPLL-based reference-less CDR architecture. In the first year of the project, an 8-16GHz DCO with octave frequency tuning range is current being designed (shown in Fig. 2(a)). Mutual coupling inductor is employed for large DCO tuning range with minimum Quality factor (Q) degradation and small silicon area (Fig. 2 (b)). A novel 4-8 GHz PI circuit has been designed achieving good linearity with low power. Fig. 2 (c) shows the architecture of the PI consisting of a Trigonometric coefficient PI (TPI) cascaded with a linear coefficient PI (LPI). The schematics of TPI and LPI are shown in Fig. 2 (d) and (e). The first IC consisting of the DCO and PI and their test circuitry will be tape-out in Feb. 2012. In the second and third years of this project the focus will move to implement the entire PI-DPLL-based CDR architecture including the FLL loop and equalization circuit.

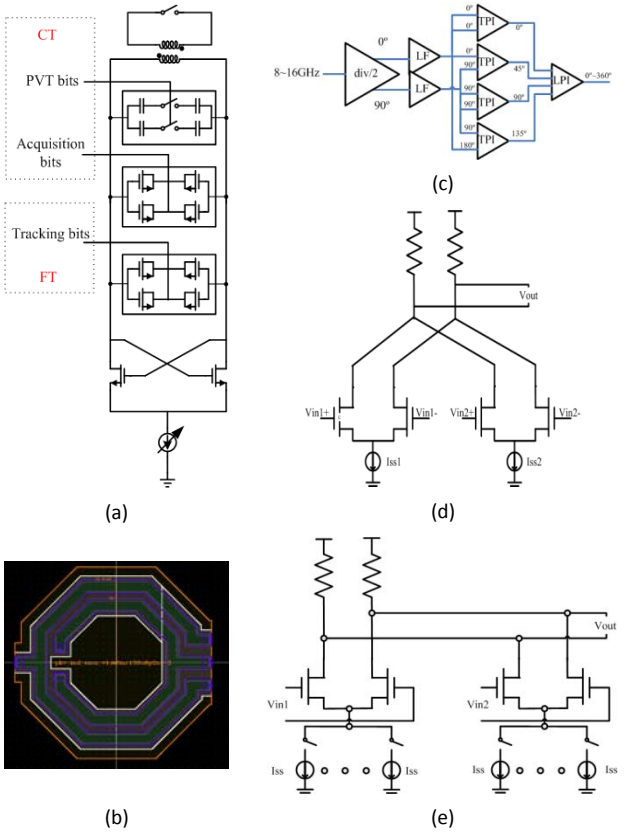


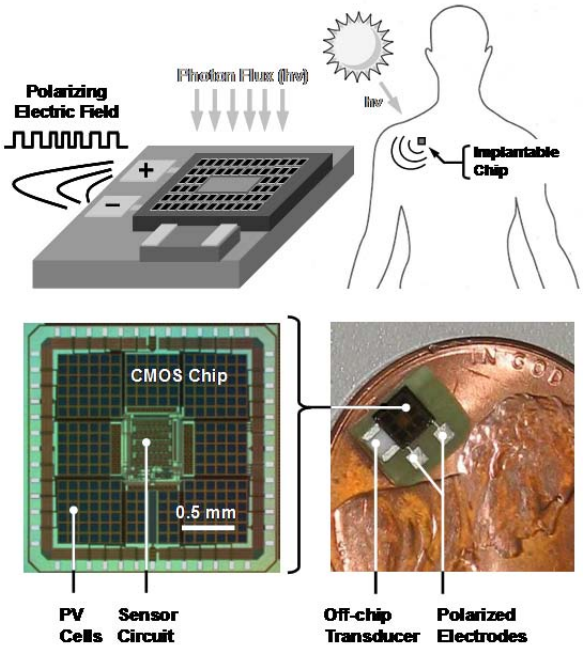
Figure 2: (a) wide-band DCO. (b) mutual-coupling inductor. (c) Wide-band PI architecture. (d) TPI circuit. (d) LPI circuit.

Keywords: Reference-less CDR, DCO, Phase Interpolation, Jitter Transfer, Jitter Tolerance

INDUSTRY INTERACTIONS

Texas Instruments.

Health Care Thrust



Summary of Accomplishments

Circuits (Health Care)	Constructed recombinant proteins that can transduce endogenous information outside of a cell. These recombinant proteins "carry" tags that can be identified from a BioFET. (1836.061, PI: L. Bleris, University of Texas at Dallas)
Circuits (Health Care)	A granular decision making approach has been proposed. It reduces the microcontroller (MCU) active cycle to 25.2% resulting in 78.2% reduction in power consumption. This configuration could maintain 99.0% sensitivity on the test data. (1836.052, PI: R. Jafari & W. Namgoong, University of Texas at Dallas)
Circuits (Health Care)	Demonstrated a fully-differential high-voltage (HV) linear amplifier using TI's 0.7 µm LBCSOI 120 V technology to achieve a signal swing of 180 V and extremely low HD2 (< - 58 dB). (1836.043, PI: P Gui, Southern Methodist University)
Circuits (Health Care)	Developed a SPICE Macromodel of Field-Effect-Transistor based nanoscale silicon biological sensors. (1836.055, Eric Vogel, University of Texas, Dallas)
Circuits (Health Care)	Demonstrated the first in-vitro photo-voltaic driven CMOS implanted MRI compatible electrocardiography sensor. (1836.071, PI: A. Hassibi, University of Texas, Austin)

TASK 1836.042, ADAPTIVE DATA PREDICTION BASED RECEIVER FOR POWER-EFFICIENT HIGH-RESOLUTION ULTRASOUND IMAGING SYSTEMS

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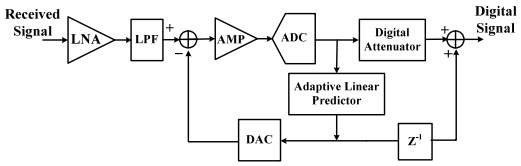
SIGNIFICANCE AND OBJECTIVES

The market demand for a portable ultrasound system is quickly growing, which desires a low-power consumption, high-resolution, and compact-size system. The objective of this research is to develop an adaptive data prediction based (**ADPB**) ultrasound imaging receiver to meet the performance requirements within strict power limits.

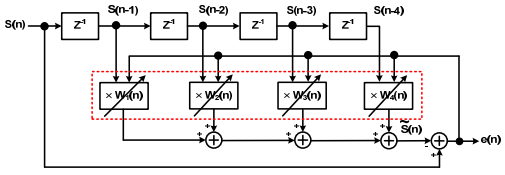
TECHNICAL APPROACH

The architecture of the proposed ADPB receiver is shown in Fig. 1 (a). In such a system, a feedback loop which consists of an amplifier, a mid-resolution ADC, an adaptive linear predictor and a DAC is employed to generate a fine residual signal. The wide dynamic-range requirement can be significantly relaxed by only quantizing the residual signal instead of the original input signal.

A 4th-order Least-Mean-square (**LMS**) algorithm is also proposed to implement the adaptive linear prediction, as shown in the Fig. 1 (b). There are two basic processes: (1) a filtering process, which involves computing the output of a transversal filter produced by a set of tap inputs. (2) An adaptive process, which involves the automatic adjustment of the tap weights of the filter in accordance with the estimation error.



(a)



(b)

Figure 1: The proposed (a) ADPB receiver architecture and (b) the LMS adaptive prediction algorithm.

SUMMARY OF RESULTS

The reconstructed ultrasound image by using the ADPB receiver shows is shown in Fig. 2 with an 83-dB dynamic range.

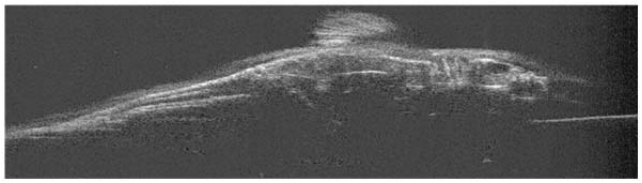


Figure 2: Reconstructed ultrasound imaging by using proposed ADPB receiver.

Table I lists the performance comparison of current industrial products and the proposed ADPB receiver. By removing the time-gain amplifier in traditional ultrasound analog front-end circuitry and employing a low resolution ADC, the power consumption per each channel of the ADPB receiver can be reduced 75%, which is as low as 30 mW. Moreover, due to the linear prediction and feedback mechanism, the output dynamic range of the receiver is up to 83 dB, which is significantly beyond the present commercial products. In this case, the quality of the ultrasound image is garmented.

Table 1: State-of-the-art industrial analog front-end circuitry and ADPB receiver power consumption comparison

Company	TI	ADI	
Products	AFE5805	AD9271	Proposed
Power/Channel (mW)	122	150	30
ADC Resolution (bits)	12	12	10
Dynamic Range (dB)	54	54	83

Keywords: Ultrasound Imaging Receiver, High Resolution, Dynamic Range, Adaptive Data Prediction

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Y. K. Wang et al, "Adaptive Data Prediction Based Receiver for Power-Efficient High-Resolution Ultrasound Imaging Systems", *Advanced Research Institute for Biomedical Imaging Workshop*, Oct. 2009.

[2] Y. K. Wang et al, "Low-Noise CMOS Time-Gain-Compensation Amplifier for Ultrasound Imaging Receivers", submitted to *IEEE Transactions on Circuit and Systems*-II.

TASK 1836.043, HIGH VOLTAGE LINEAR AMPLIFIER TECHNOLOGY

PROF. PING GUI, SOUTHERN METHODIST UNIVERSITY, PGUI@LYLE.SMU.EDU

SIGNIFICANCE AND OBJECTIVES

Existing ultrasound transmitters use high-voltage (HV) pulser drivers to excite the transducer, which have very limited usages in enhanced ultrasonic imaging. This project seeks to design a monolithically integrated HV *linear* amplifier for enhanced ultrasonic imaging quality.

TECHNICAL APPROACH

Ultrasonic transmitter driver requires large signal swing (up to 180V), high slew rate (on the order of V/ns), large bandwidth (1-20 MHz), and low harmonic distortions (below -45dB). We explore different circuit architectures and circuit design techniques to achieve the above design goals. Both fully differential circuit architecture and single-ended totem-pole topologies are explored. Novel circuit blocks such as current-feedback amplifiers and dynamic biasing are designed to increase the bandwidth of the HV amplifier bandwidth and power efficiency respectively. On the system level, digital pre-distortion (DPD) technique is employed to further improve on the linearity, bandwidth, and reduce the power consumption.

SUMMARY OF RESULTS

In the first year of the project, we successfully designed, implemented, and demonstrated a fully-differential high-voltage (HV) linear amplifier using TI's 0.7 µm LBCSOI 120 V technology to achieve a signal swing of 180 V and extremely low HD2 (< - 58 dB). The results achieved exceed the performance of TI's existing TX517 chip. One drawback of the fully-differential structure is that a transformer is needed at the output to combine the differential signal into a single-ended (SE) signal. In this aspect, it is desirable to have a SE HV linear amp with comparable performance. However, a SE amplifier typically suffers from high HD2. We proposed a digital pre-distortion (DPD) technique to reduce the harmonic distortions in a SE linear amplifier. In the second year of the project, we designed an SE rail-to-rail HV linear amplifier using a 200 V CMOS technology. Current-feedback amplifier technique is used to obtain high slew rate and high bandwidth. Dynamic biasing technique is used for improved power efficiency. System-level DPD improves the linearity and further increases the bandwidth and power efficiency. The second version of the monolithic IC will be taped-out in Oct. 2011. Figure 1 depicts the system block diagram of the HV current feedback rail-to-rail class-AB with the DPD scheme. Fig. 2(a) shows the current-feedback output amplifier, and 2(b) is the measured frequency spectrum with low HD2 achieved using DPD. The third year of the project will focus on the measurement of the proposed HV IC architecture and circuits, and characterization of the reliability of the HV devices and technology.

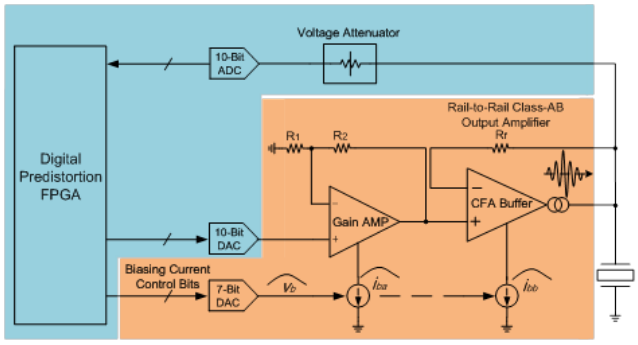


Figure 1: HV current feedback rail-to-rail class-AB linear amplifier with digital pre-distortion scheme.

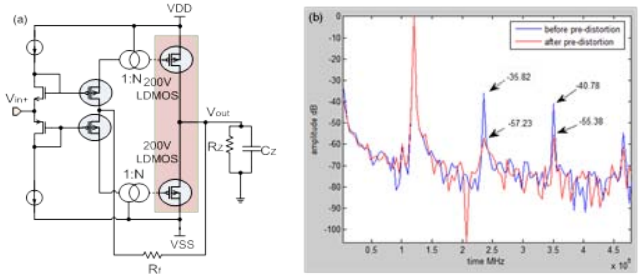


Figure 2: (a) Current-feedback output amplifier. (b) Measured frequency spectrum showing a 20 dB improvement in the linearity by using digital pre-distortion technique.

Keywords: high-voltage, linear amplifier, HD2, power efficiency, pre-distortion, ultrasound.

INDUSTRY INTERACTIONS

Texas Instruments.

MAJOR PAPERS/PATENTS

[1] Z. Gao, et al., "An High Voltage Linear Amplifier for Ultrasound Transmitter" SRC TECHON, Austin TX, Sept. 2010.

[2] Z. Gao, et al., "A Digital-Feedback Pre-distortion Technique for Integrated High-Voltage Ultrasound Transmitting Power Amplifiers" IEEE International Ultrasonic Symposium, Oct. 2011 (accepted).

[3] Z. Gao, et al., "A High Slew-Rate High-Voltage Linear Amplifier for Ultrasonic Imaging Applications in a High-Voltage SOI technology" IEEE Transactions on UFFC (submitted).

[4] Z. Gao, et al., "A Look-up-Table Digital Pre-distortion Technique for High-Voltage Power Amplifiers in Ultrasonic Applications" IEEE Transactions on UFFC (submitted).

TASK 1836.052, AN ULTRA-LOW POWER SIGNAL PROCESSING WITH SMART ANALOG-ENABLED PRE-CONDITIONING STAGE FOR INERTIAL SENSING APPLICATIONS

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WON NAMGOONG, UT DALLAS, NAMGOONG@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

We will provide a complete design framework for an ultra low power signal processing module that will activate full signal chain only when patterns of interest from sensors (motion, ECG) are identified. The ultra low power signal processing module will be designed to operate at minimum supply voltage levels.

TECHNICAL APPROACH

We propose an ultra-low power and light-weight analog front end signal conditioning module for inertial sensors that can perform preliminary signal processing without activating the main signal chain. The preliminary signal conditioning will be performed by means of pattern recognition, at the beginning with very low power and low precision, gradually increasing the power and precision. When a particular pattern of interest is likely recognized, the next stage is activated and eventually, the complete signal chain is activated, when necessary, for further comprehensive processing. For patterns of interest that have a low duty cycle (~1%), we expect to reduce the overall power consumption of the system by several orders of magnitudes.

SUMMARY OF RESULTS

The tiered wake-up module, which is composed of several coarse to fine grained screening classifiers, is responsible for screening sensor readings and activating main processing unit upon arrival of an event (or action) of interest. The screening is implemented by template matching using normalized cross correlation and dynamic time warping, implemented in hardware using simple adders and multipliers. The tunable parameters for template matching include the time duration of actions considered for cross correlation calculation, the number and the location of samples within each action, and the bit resolution for samples. This allows to adjust the power and the sensitivity of the signal processing in each template matching block.

For our preliminary study, we collected data from five participants each wearing a 3-axis accelerometer on their waist. Every participant performed seven actions (e.g. 'sit to stand', 'sit to lie', etc.), 20 times each. 'Sit to stand' was assumed to be the target action. We used this data for template generation and matching.

To measure the power consumption of the template matching blocks, they were implemented using Verilog and synthesized with the 180 nm IBM standard cell library. Power measures were further computed with switching activity generated by the real sensor data. The sensor data are often slowly changing, resulting in perhaps small changes in a few LSBs. This generates smaller number of transitions and minimally affects the switching power of the multipliers and adders. On average, the power consumption of the template matching blocks range from 10's to 100's of nW.

Using the proposed Granular Decision Making, the microcontroller (MCU) active cycle reduces to 25.2% resulting in 78.2% reduction in power consumption. This configuration could maintain 99.0% sensitivity on the test data. In practice, the duty cycle of the target activity is much lower than 25%, e.g. < 5%, and applying our approach will result in much more power savings. Note that the power consumption of GDMM is in the order of uW and is negligible compared to mW power budget required for MCU

Keywords: low power signal processing, programmable signal processing block, wake-up circuitry

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] R. Jafari et al., "A Low Power Wake-up Circuitry Based on Dynamic Time Warping for Body Sensor Networks," International Conference on Body Sensor Networks (BSN), May 23-25, 2011, Dallas, TX.

[2] R. Jafari, "Tiered Low Power Wake-up Modules for Lightweight Embedded Systems," Intel. Conf. on Body Sensor Networks (BSN), May 23-25, 2011, Dallas, TX.

[3] H. Ghasemzadeh et al., "Ultra Low Power Granular Decision Making using Cross Correlation: Optimizing Bit Resolution for Template Matching," (Recipient of Best Paper Award) IEEE Real-Time and Embedded Technology and Applications Symp., April 11-14, 2011, Chicago, IL.

TASK 1836.055, SPICE MODELS AND ANALOG CIRCUITS FOR NANOSCALE SILICON CHEMICAL- AND BIOLOGICAL-SENSORS

PROF. ERIC VOGEL, THE UNIVERSITY OF TEXAS AT DALLAS, ERIC.VOGEL@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

Nanoscale chemical and biological sensors have been demonstrated, but little attention has been given to SPICE models and support circuitry. This project will develop physically realistic SPICE models for the sensor device. SPICE model creation will be followed by design of suitable support circuitry for a complete system.

TECHNICAL APPROACH

The design of circuits to support the biological sensor will require a suitable SPICE model which comprehends the unique properties of this device. Generating such a SPICE model in turn requires a thorough understanding of the physics of the sensor and its operating environment. To improve the understanding of the biosensor device physics and generate the necessary data for a suitable SPICE model, a combination of theoretical analysis and TCAD modeling is being utilized. With a SPICE model available, block specifications will be defined and reference support circuits developed.

SUMMARY OF RESULTS

An example of the sensor element under study is shown in Figure 1. Studies during the first year of this project provided understanding of the device physics of the biosensor configuration as well as bias conditions and coupling of the back gate to the overlying electrolyte. During this year, understanding of biasing methods for the biosensor has been refined, and the methods for biasing the sensor have been analyzed and compared. [1]

Development of the biosensor SPICE model has been based on a membrane model which describes the sensor/electrolyte system in terms of various layers (Helmholtz layer, Gouy layer) within the electrolyte and their effect on the site-binding charge at the sensor surface. This model enables calculation of the potential across the various layers within the sensor system, and allows the sensor system to be represented as an equivalent circuit which is implemented as a subcircuit within the SPICE simulator. The equations derived from the membrane model were embedded within the SPICE subcircuit for use during circuit design and simulation. [2] The resulting macromodel is responsive to the pH of the electrolyte as well as the protein concentration of the sample. Response of the biosensor drain current, as modeled in SPICE, as a function of gate voltage and protein concentration is shown in Figure 2.

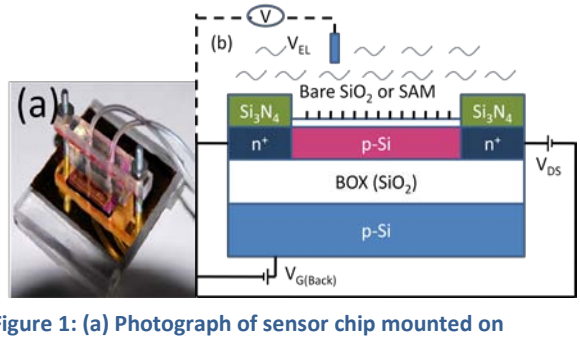

Figure 1: (a) Photograph of sensor chip mounted on microfluidic delivery system (b) Sensor cross-section with measurement circuit.

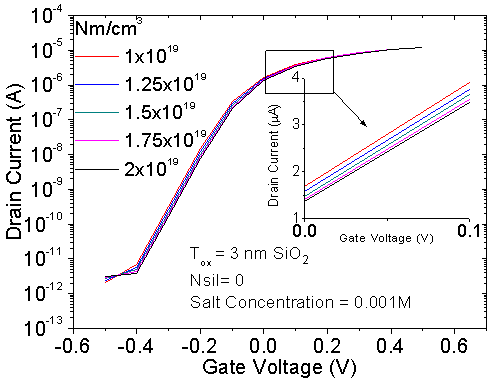

Figure 2: Simulated response of biosensor drain current in response to protein concentration variation based on SPICE macromodel.

In the third year of this project the initial focus will be on fitting the SPICE model more accurately to measured biosensor data. Further work will refine the specifications for support circuitry blocks necessary to form a complete sensing platform and design of support circuitry in a realistic industry process.

Keywords: Chemical, Biological, Sensor, SPICE, model.

INDUSTRY INTERACTIONS

Texas Instruments.

MAJOR PAPERS/PATENTS

[1] R. A. Chapman et al., "Comparison of Methods to Bias Fully Depleted SOI-Based MOSFET Nanoribbon pH Sensors," *IEEE Tran. Elec. Dev.*, June, 2011.

[2] P. G. Fernandes et al., "SPICE Macromodel of Field-Effect-Transistor-based Nanoscale Silicon Biological Sensors,"(submitted).

TASK 1836.061, ANALOG COMPUTING IN HUMAN CELLS

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SIGNIFICANCE AND OBJECTIVES

The objective of this project is the implementation of molecular circuits capable of responding to specific cellular disease-related signals and producing accordingly outputs that can be quantified using biologically modified field-effect transistors.

TECHNICAL APPROACH

Molecular gene circuits with limited capacity have been developed in biochemical and biological contexts [1]. We propose a paradigm shift: we will provide a general-purpose framework for bridging endogenous cellular to extracellular information. We propose to engineer multi-component RNA- and protein- based biosensor circuits designed to: (a) detect complex conditions related to abnormal expression of a number of molecular signals in mammalian cells, (b) upon detection release biologically active modules in order to transduce the information to external devices.

SUMMARY OF RESULTS

Complex combinations of abnormally expressed genes are an excellent indicator of multi-gene disorders. A system capable to detect these conditions may be used as a highly selective tool for diagnosis and treatment (Figure 1).

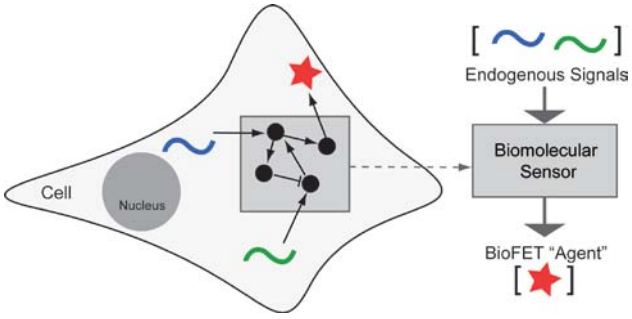

Figure 1: The biomolecular sensor responding to endogenous signals and producing an output that can be quantified by a bioFET.

We will provide a framework for bridging endogenous cellular to extracellular information in a "universal" bioFET, programmable by reagents that are prepared according to the tissue type and disease.

Experimentally, we have been constructing recombinant proteins that can transduce endogenous information outside of a cell (Figure 2). In addition, we engineer these recombinant proteins to "carry" tags that can be identified from a bioFET.

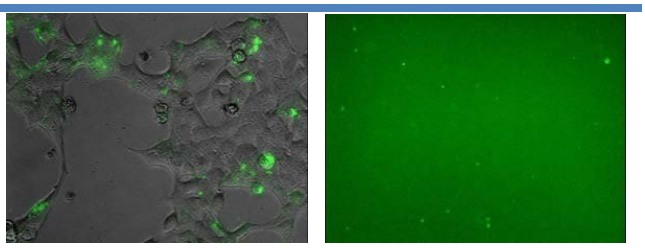

Figure 2: (left) We introduced in kidney cells a fusion of a fluorescent protein to neuromodulin signal that assists in transporting this protein to the membrane, (right) we produced exosomes secreting fluorescent proteins.

We performed extensive modeling and simulations to determine suitable architectures for implementation [2]. From these simulations we selected and currently study a range of candidate molecular circuits (for example the system illustrated in Figure 3).

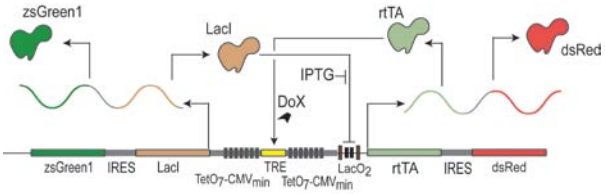

Figure 3: A molecular circuit [3] with coupled positive and negative feedback that can produce oscillations in the output or alternatively operate as a switch between states.

Finally, we identified [4] biological correlates to electrical analog components towards rational and standardized methodologies for gene circuit engineering. We show that gene circuit parameters can be used in a similar manner as varying the values of inductors, resistors, and capacitors when tuning an electrical circuit.

Keywords: Synthetic Biology, Biosensors, and BioFETs.

INDUSTRY INTERACTIONS

Global Foundries

MAJOR PAPERS/PATENTS

[1] Leisner M., L. G. Bleris, et. al. Rationally designed logic integration of regulatory signals in mammalian cells. Nature Nanotechnology, 5, 666–670, 2010.

[2] Jacob White and Leonidas Bleris. Parametric simulations reveal steady state properties of feedforward loop motifs. AIChE Annual Meeting, November 2010.

[3] Jacob White and Leonidas Bleris. Coupled positive and negative feedback architecture. To be submitted.

[4] Taplin Moore, Jacob White, and Leonidas Bleris. Analog computing in cells. To be submitted.

TASK 1836.064, ULTRA-LOW-POWER ANALOG FRONT-END IC DESIGN FOR IMPLANTABLE CARDIOVERTER DEFIBRILLATOR (ICD) DEVICES

TASK LEADER: PROF. DONALD Y.C. LIE, TEXAS TECH UNIVERSITY, DONALD.LIE@TTU.EDU

SIGNIFICANCE AND OBJECTIVES

This project investigates the design details of the ultra-lowpower analog front-end (AFE) integrated circuits (ICs) for an implantable cardioverter defibrillator (ICD). Both system and circuits level design will be considered to minimize its power consumption. Note the AFE IC must be *always* on so its power needs to be minimized.

TECHNICAL APPROACH

For the system-level design considerations of an ICD, we have first looked into the intra-cardiac electrogram (EGM) and its amplitude and frequency ranges for the proposed AFE IC. The measured EGM data is taken from a real human subject available from the *Physionet*, and our AFE IC includes an instrumentation amplifier (INA), a bandpass filter (BPF), a variable gain amplifier (VGA), and an analog-to-digital converter (ADC). Various novel circuits and system design techniques will be explored to reduce its power consumption while still capable of continuously monitoring the heart rate to ensure proper pacing and possible defibrillation.

SUMMARY OF RESULTS

A proposed system [1] allows the two parallel channels sharing the same VGA+ADC pair, where a non-overlapping clock signal is used to control the switches to toggle every 200 ms from the Brady filter to the Tachy filter and vice versa (Fig. 1). At any given time, only one channel of signal flows into the VGA and ADC pair. This method can save power by eliminating a VGA+ADC pair.

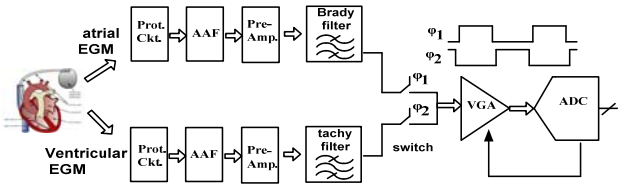

Figure 1: A simplified system diagram of our proposed AFE IC for an ICD, with parallel bradycardia and tachycardia channels sharing the same VGA and ADC to save power

Figure 2 illustrates the proposed single-ended 8-bit successive approximation register (SAR) ADC with reference voltage equal to $V_{REF}/2$ [2] to digitize input signal with the amplitude of [0, V_{REF}]. The proposed SAR ADC reduces the size of binary-weighted capacitor array by 50%, and the average power consumption in the DAC during digitizing by 87.5%.

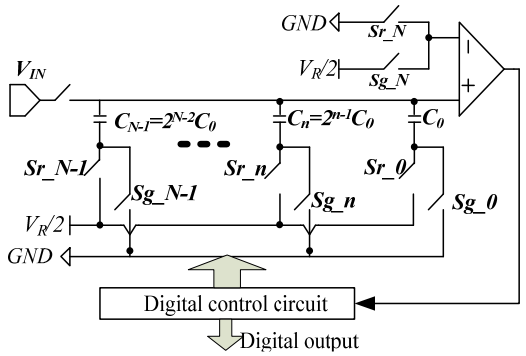

Figure 2: Our proposed ultra-lowpower single-ended SAR ADC

In the 2nd and the 3rd years of this project, our focus will be on the whole AFE IC design (Fig. 3). Moreover, power-efficient IC design techniques will be carefully examined. For example, an ultra-lowpower BPF with sub-threshold CMOS transconductors and wide linear range and a higher resolution low-power ADC are under development.

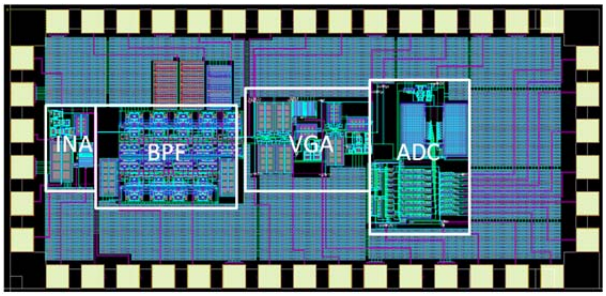

Figure 3: A layout of our proposed ICD AFE IC designed in a 0.35-μm technology (including INA, BPF, VGA and ADC)

Keywords: implantable cardioverter defibrillator (ICD), analog front-end (AFE), ulta-lowpower, sub-threshold.

INDUSTRY INTERACTIONS

Texas Instruments and IBM

MAJOR PAPERS/PATENTS

[1] W. Hu, T. Nguyen, Y.-T. Liu, and D.Y.C. Lie, "Ultralow-power analog front-end circuits and system design for an implantable cardioverter defibrillator (ICD)," Proc. IEEE/NIH Workshop Life Sci. Syst. Applicat., pp. 34-37, NIH Campus, Bethesda, MD, USA, April 7-8 (2011)

[2] D.Y.C. Lie, J. Lopez, and W. Hu, "Low Power RF Wireless Sensor Design with Highly Efficient SiGe Power Amplifier and Ultralowpower ADC", Proc. Government Microcircuit Applicat. Critical Techno. Conf. (GOMAC), pp. 137-140, Orlando, FL, March 21-24 (2011)

TASK 1836.066, A FULLY-INTEGRATED CMOS PLATFORM FOR MICROWAVE-BASED LABEL-FREE DNA SENSING

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SAMUEL PALERMO, TEXAS A & M UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

DNA sensors or biosensors are used to identify and detect various molecules and biochemical analytes. Existing DNA sensors employ expensive label-based detection techniques. Here, recognition of label-free DNA using simple resonators is achieved by detecting resonant frequency changes when the sample is hybridized.

TECHNICAL APPROACH

The proposed system employs microwave resonator-based sensors in a voltage-controlled oscillator (VCO) embedded in a time multiplexed frequency synthesis loop to enhance DNA detection sensitivity. Sensor operation is based on the presence of DNA on top of an electromagnetic (EM) planar resonator inducing a shift in resonant frequency (and corresponding VCO oscillation frequency) due to changes in EM field distribution around the resonator depending on the DNA hybridization state. In the proposed system, correlated double sampling (CDS) is applied at high speed to reduce the effect of flicker noise on the output frequency measurements.

SUMMARY OF RESULTS

There are two main research phases in implementing the proposed system. The first phase is increasing the measurement accuracy of the frequency with minimal additional noise sources. The second phase is how to increase the sensitivity of the frequency shift with the material under test.

The basic idea of the first phase is to put the oscillator in a phase-locked loop (PLL) such that the control voltage changes in response to the presence of the sample.

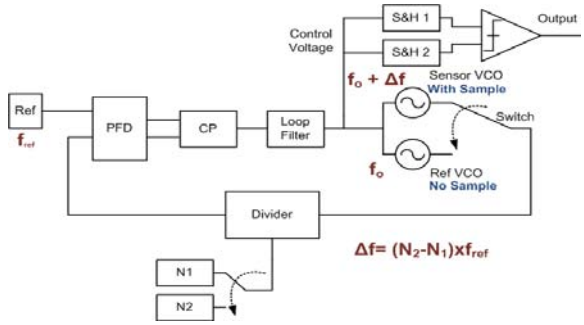


Figure 1: Block diagram of the whole system used to measure the frequency shift due to the sample

If the divider setting is changed such that the control voltage returns to the same value, the frequency shift of oscillation will be the difference between the readings of the divider setting to get the same control voltage.

To enhance the sensitivity of the reading, system analysis of all the noise sources in the PLL was performed. In figure 1, this is the proposed block diagram of the system to enhance the sensitivity by using a correlated double sampling (CDS) approach. There are two oscillators, one with the sample and the other is used as a reference oscillator, with a switch that selects between the oscillators. The PLL will settle after the selection of the oscillator for a certain divider setting N giving a certain control voltage. The frequency shift can be determined as (N2-N1)xf_{ref}, where N1 is divider setting for the sample case and N2 is for the reference case. Figure 2 is the layout of the chip with an 8GHz system that is used for verification of the proposed method.

The second phase will be to study different resonators and their responses to DNA samples. This will be sub-divided into three steps: resonator design, fabrication and gold deposition and DNA testing. The future plan is to perform these steps and to embed the DNA sensor into the implemented integrated circuit.

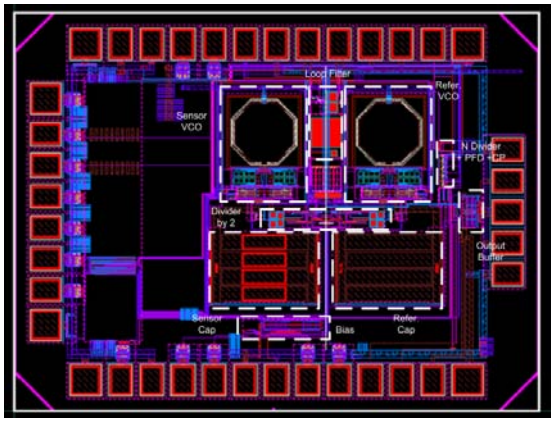


Figure 2: Layout of 1st chip used for sensing

Keywords: DNA, frequency measurement, PLL, biosensor

INDUSTRY INTERACTIONS

N/A

MAJOR PAPERS/PATENTS

N/A

TASK 1836.071, DESIGN OF PHOTOVOLTAIC (PV) POWER HARVESTING CMOS ICS

PROF. ARJANG HASSIBI, UNIVERSITY OF TEXAS AT AUSTIN, ARJANG@MAIL.UTEXAS.EDU

SIGNIFICANCE AND OBJECTIVES

Energy autonomous ICs that can harvest energy from environment are an enabling technology. Unfortunately, the existing energy harvesting methods generally require off-chip transducers that cannot be monolithically integrated with the embedded VLSI systems. We plan to create CMOS-compatible photovoltaic (PV) cells, as energy harvesting elements, and demonstrate their applicability in implantable sensor devices.

TECHNICAL APPROACH

To create CMOS PV energy harvesting system, we will take advantage of the existing photodiodes in the CMOS process. P+/Nwell is the optimal choice, since it offers anode and cathode floating nodes. The general approach in this project is to first design, fabricate and characterize the CMOS PV cells and evaluate their responsivity, I-V curve, and circuit model. In the next phases, we will study various voltage regulator architectures to generate "useful", reliable, and VLSI-compatible voltages from them. The ultimate goal is to use this technology to enable a fully-integrated PV-driven implantable sensor.

SUMMARY OF RESULTS

As the first step, we designed, fabricated and measured the performance of CMOS PV cells in a 0.18 µm process. Based on the results shown in Fig. 1 (the responsivity and the I-V characteristics), we concluded that 10's of µW of power can be harvested in ambient light conditions (indoor light) per mm^2. This amount of power is quite sufficient for many low power ICs applications. Examples are sensor nodes, low-power DSP units and burst-mode communication node. Furthermore, we implemented the CMOS PV cells in an implantable sensor system. As shown in Fig. 2, in this 2.5mm x 2.5mm sub-µW integrated system, the *in-vivo* physiological signals are first measured by using a sub-threshold ring oscillator-based sensor, the acquired data is then modulated into a FSK signal, and finally transmitted neuromorphically to the skin surface by using a pair of polarized electrodes. The total area for diode is this is approximately 3.5 mm^2. The results of this research have been published [1-2].

Keywords: Photovoltaic, Implanted Devices, Sensor, CMOS, Energy Harvesting

INDUSTRY INTERACTIONS

Freescale Semiconductor

Texas Instrument

TSMC (foundry support – not SRC funding)

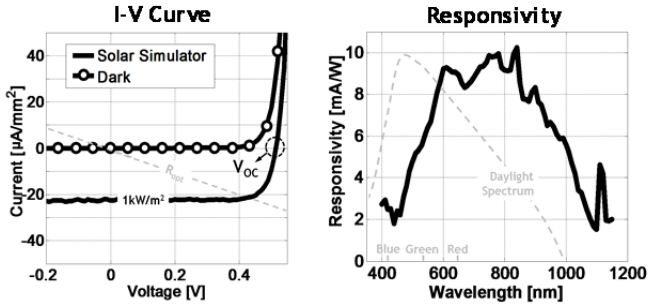


Figure 1: Characteristics of P+/Nwell PV Cell in a 0.18 µm CMOS process.

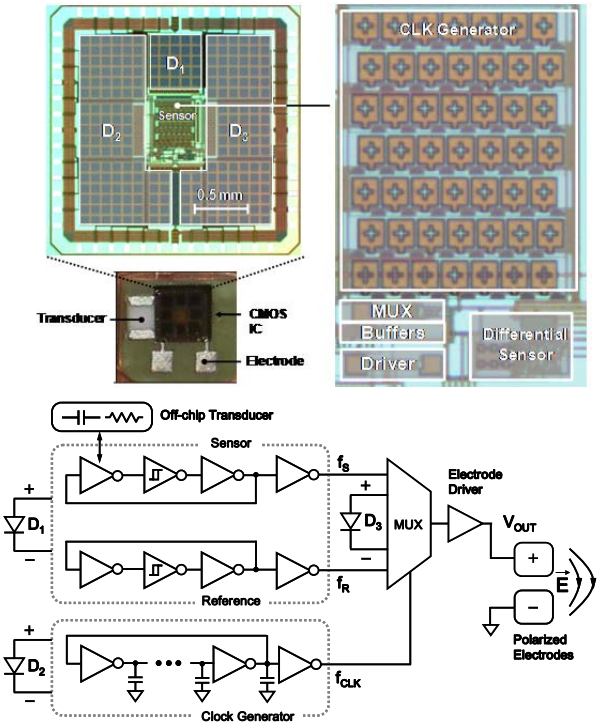


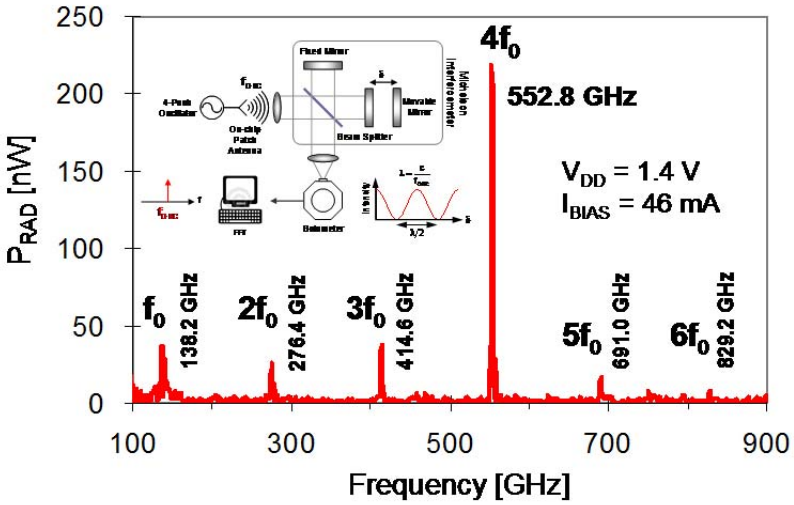
Figure 2: PV-driven implantable sensor chip micrograph and architecture.

MAJOR PAPERS/PATENTS

[1] Ayazian et al., "A Photovoltaic-Driven and Energy-Autonomous CMOS Implantable Sensor," Tech. Dig. of *VLSI Symp.* (2011).

[2] Ayazian et al., "A Photovoltaic-Driven and Energy-Autonomous CMOS Implantable Sensor," I (to appear) IEEE T. BIOCAS J. (2011).

Safety and Security Thrust



Summary of Accomplishments

Circuits (Safety and Security)	Demonstrated key building blocks for a 400-GHz phase locked loop along with a 560-GHz signal generation circuit, both in 45-nm CMOS. (1836.036, PI: K. O, Univ. Texas, Dallas)
Circuits (Safety and Security)	Demonstrated a Physically Unclonable Function (PUF) circuit in 45nm CMOS, and characterized a True Random Number Generator (TRNG) circuit over process variation. (1836.074, PI: W. Burleson, Univ. Massachusetts)
Circuits (Safety & Secu.)	Demonstrated a compact (200 m^2) Schottky Diode detector for measurements of voltages at 70-110 GHz using DC measurements (1836.008-1836.010, Kenneth K. O, University of Texas, Dallas)
Circuits (Safety & Secu.)	Applied MMSE and Space time block coding in mm-wave imaging to reduce receiver complexity and to mitigate the interference among transmitted signals, respectively (1836.033, Mohammad Saquib, University of Texas, Dallas)

TASK 1836.008-010, DIGITAL ASSISTED MM-WAVE CMOS CIRCUITS

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SIGNIFICANCE AND OBJECTIVES

To improve yield and shorten time to market of millimeter wave CMOS circuits, this task is Investigating the feasibility of incorporating digitally-controlled built-in tuning in millimeter wave circuits that mitigates the impact of process variations, modeling uncertainty of passive and active components.

TECHNICAL APPROACH

Detectors placed at the input and output of front-end amplifiers and mixer outputs of an RF transceiver can be used for measurements needed for tuning/calibrating the receiver and transmitter. The key challenges for realizing a digital assisted system operating at millimeter wave frequencies are (1) inexpensively injecting test signals, (2) incorporating tuning elements which do not add significant parasitics and degrade circuit performance, and (3) realizing high impedance broadband detectors with sufficient dynamic range. This effort will understand these challenges, and the limitations in the context of a 77-GHz reconfigurable low noise and power amplifiers fabricated in 45-nm CMOS.

SUMMARY OF RESULTS

Test structures of tunable components including variable capacitors, inductors, and loads have been simulated and fabricated in 45-nm CMOS. The variable inductors have the measured maximum to minimum inductance ratio of ~1.1 instead of the simulated value of ~1.8. The Q-factor of variable inductors at 77 GHz is ~10. A tunable millimeter wave low noise amplifier in Figure 1 has been fabricated. The four stage amplifier includes four tunable inductors that can tune the inter-stage matching. In simulations, the gain center frequency can be tuned from 76 to 82 GHz. In measurements, the amplifier is tuned around 60 GHz. Additionally, because of the limited inductor tuning range, the center frequency can be tuned only between 58 and 61 GHz. The peak gain is ~10 dB.

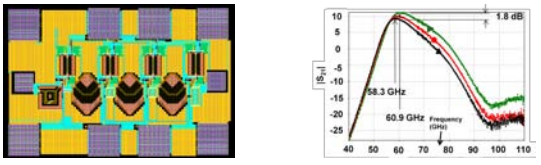

Figure 1: Tunable amplifier layout and measurements

Test structures of diode detectors are also fabricated in the same process technology. The insertion of high impedance detector introduces less than 0.5dB loss up to 50 GHz. The rms diode detector has measured dynamic range greater than 30 dB. The insertion loss could not be measured above 50 GHz because of the GS and SG bond pads for the structures. New structures using GSG pads have been taped out.

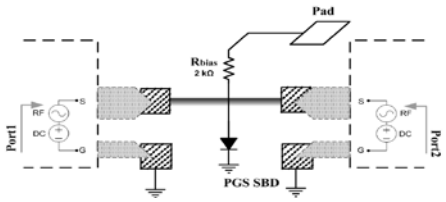

Figure 2: Diode detector insertion loss measurements

Based on the measurements, the LNA and detector have been redesigned, integrated and taped out for fabrication. Detectors will also be integrated into the power amplifier. Lastly, techniques for tuning a set of circuit parameters, including gain, linearity, and noise performance will be investigated.

Keywords: tunable, mm-wave, low noise amplifier, power amplifier.

INDUSTRY INTERACTIONS

Texas Instruments and Freescale

MAJOR PAPERS/PATENTS

[1] N. Zhang and K. K. O, "W-Band Pulsed Radar Receiver in Low Cost CMOS," 2010 CICC, pp. , September, 2010, San Jose, CA.

[2] C. Mao et al., "Diodes in CMOS for MM and Sub-MM Wave Circuits," **(Invited)** 2010 Intl. Sym. on VLSI Tech., Systs and Apps, April, 2010, Hsinchu, Taiwan.

[3] C. Mao and K. K. O, "60-GHz Hybrid Transmit/Receive Switch Using p-n Diode and MOS Transistors," 2009 Symposium on VLSI Circuits, pp. 248-249, June 2009, Kyoto, Japan.

[4] N. Zhang et al., "CMOS Freq. Gen. Syst for W-Band Radar," 2009 Symp. on VLSI Circs., pp.126-127, June 2009, Kyoto, Japan.

[5] C. Mao et al., "65/130 GHz diode freq. doubler in 0.13-μm CMO," IEEE JSSC, vol. 44, no. 5, pp. 1531-1538, May 2009.

TASK 1836.032, MILLIMETER-WAVE PHASE-LOCKED LOOP DESIGN WITH ENHANCED TOLERANCE TO PROCESS AND TEMPERATURE VARIATION

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SIGNIFICANCE AND OBJECTIVES

A key challenge to the manufacturability and robustness of designs at mm-wave frequencies arises from process and temperature (P&T) induced variations. This research focuses on the design of a phase-locked loop (PLL) based mm-wave frequency synthesizer for 77 GHz RADAR applications that is robust to such variations.

TECHNICAL APPROACH

The impact of process and temperature variations on PLL circuits will be investigated and critical sensitivities will be identified through simulation. Circuit and architectural solutions to minimize changes in performance metrics, and prevent catastrophic failures due to such variations will be implemented. Architectures that can provide adequate frequency span of circuits, such as oscillators and dividers, in order to compensate for process variations, without compromising the phase noise of the synthesizer will be investigated. Circuit techniques for controlling the gain and amplitude response of the phase detector and inter-stage buffers will be explored. The compensation techniques will be optimized for ensuring minimal power and area overhead.

SUMMARY OF RESULTS

A key design challenge in PLLs arises from variations in the VCO center frequency with process and temperature. In order to span a specific range of frequencies, the VCO needs to be designed with sufficient margin to accommodate these variations. Further these oscillators exhibit an inherent trade-off between phase noise and tunability.

To alleviate this trade-off, a dual-mode VCO has been proposed and designed. The design relies on active core reconfiguration around an LC resonator, as opposed to switching passive elements within the resonator. This allows for two modes of operation, with minimal change in the inductance-to-resistance ratio of the resonator. This in turn minimizes phase noise variation.

The above topology has been designed with nearly 10% tuning range at 64GHz in a 0.13 μm process. The main limitation on tuning range in this process is seen to arise from the parasitic capacitance of cross-coupled devices. In order to compensate the varactor loss, the cross-coupled devices of the VCO need to be sized to a provide a minimum negative resistance. At relatively longer channel length of 0.13 μm, larger device sizes are required compared to state of the art CMOS nodes, which leads to greater parasitic capacitance.

The impact of temperature variation has also been studied. This variation mechanism is seen to degrade tunability by approximately 2% due to change in varactor capacitance and C_{gs} of the cross-coupled devices of the VCO. We have investigated the use of PTAT back gate compensation in an inversion mode varactor to compensate frequency shift due to temperature variation.

Temperature variation is seen to have a significant impact on phase noise. A key source of degradation at high temperatures arises from the resistance of the inductor metal, which has a positive temperature coefficient. A decrease in the quality factor with temperature degrades the swing, and in turn the phase noise. This degradation is compensated through bias current control.

In mm-wave applications, injection locked frequency dividers (ILFDs) are often employed in the first divider stage. These designs can operate at much higher frequencies, since they use resonant tanks, however they suffer from limited locking range. We have recently designed a low-power, wide tuning range ILFD. By using a larger Vgs on the input device compared to the LC tank of the ILFD, a locking range in excess of 20% is achieved.

Keywords: Frequency synthesis, phase-locked loop, variability, voltage-controlled oscillator, mm-wave design

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] R. Gharpurey *et al.*, A Single-Tank Dual-Band Reconfigurable Oscillator, VLSI Symp. 2006, pp. 176-177

[2] S. Agarwal *et al.*, A Dual-mode Wide-band CMOS Oscillator, IEEE DCAS Workshop, 2009, 64-66

TASK 1836.033, MIMO RADAR FOR PIXEL REDUCTION IN MM-WAVE IMAGING

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SIGNIFICANCE AND OBJECTIVES

The millimeter (*mm*) wave imaging system is well-suited for many safety and security applications for its exquisite properties and currently employs traditional radar technology. This imaging system is expensive and the system cost depends largely on hardware components used to manufacture transceivers/antennas. To reduce that cost, multiple-input-multiple-output (MIMO) radar technologies and smart image processing techniques are incorporated into the mm-wave framework.

TECHNICAL APPROACH

Recent studies suggest that MIMO radar yields better image resolution than the conventional one. However due to parallel transmission of the probing signals, MIMO system suffers from interference and therefore, we employ the minimum mean square error (MMSE) receiver. We also employ space-time block code (STBC) technique to eliminate the effect of interference between transmitted waveforms. STBC was originally proposed for wireless communication systems to increase the channel capacity via transmitting parallel independent waveforms. Our numerical results demonstrate that depending on the system configuration, MIMO radar with STBC and MMSE receiver is capable of providing the same image resolution as the traditional one but with almost 60% less antennas. Our above study did not consider hardware (e.g. A/D converter) related issues. They will be investigated thoroughly in future.

SUMMARY OF RESULTS

Now we present some numerical results to demonstrate that compared to the traditional radar, MIMO radar is capable of operating with a fewer number of transceivers without sacrificing the image quality. In our simulation, we consider a concealed weapon (revolver) as our test target; see Fig. 1 (left). The target area is divided into 24 range and 61 angle bins. Signal-to-noise ratio (SNR) is set to 20dB and probing waveforms are Hadamard codes scrambled with PN sequences. Fig. 1 (right) shows the image constructed with the traditional radar technology equipped with 16 antennas, where number of transmitter (*M)* = 1 and number of receiver (*N)* = 15. In Fig. 2 (left), it can be noticed that a MIMO radar system with M = 3 and N = 8 is capable of providing slightly better image resolution than the traditional one. Fig. 2 (right) demonstrates that further reduction of antennas is achieved when time reversal STBC technique is employed. In summary, MIMO radar technology is capable of providing the same image resolution as the traditional one but with significantly less number of antennas.

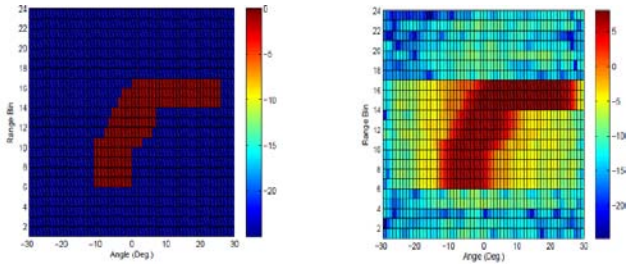

Figure 1: (left) Original target; (right) Traditional radar image with 16 antennas. Here *M* = 1 and *N* = 15.

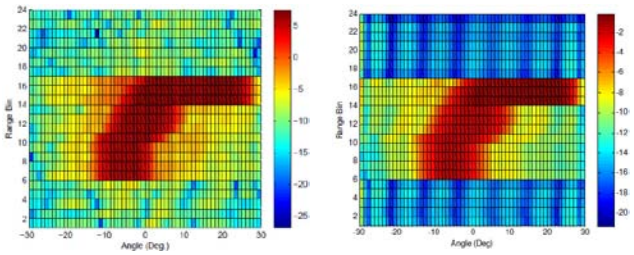

Figure 2: (left) MIMO radar image with 11 antennas. Here *M* = 3 and *N* = 11; (right) MIMO radar image with 7 antennas. Here *M* = 2 and *N* = 5 and STBC is employed with MMSE like receiver.

Keywords: millimeter wave (mm-wave) radar, multiple input multiple output (MIMO) antenna array, space-time block code (STBC), minimum mean square error (MMSE), image resolution.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS

[1] A. Z. Sadeque, T. Ali, M. Saquib and M. Ali "MIMO radar imaging for target detection and localization in sensor network," IEEE Systems Journal, May, 2011 (submitted).

TASK 1836.034, 77-81 GHZ CMOS TRANSCEIVER WITH BUILT-IN SELF-TEST AND HEALING

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SIGNIFICANCE AND OBJECTIVES

This work focuses on developing Built-in Self-Test (BIST) techniques for millimeter-wave (mmW) CMOS integrated transceivers for 77 GHz automotive radar applications. Testing is one of the key factors raising the cost of manufacturing mmW ICs. This research focuses on understanding the architectural trade-offs and testing algorithms, and developing circuits that can enable loopback based BIST techniques for mmW transceivers in standard CMOS technologies.

TECHNICAL APPROACH

In order to perform BIST on a mmW CMOS transceiver, we need to enable a 'loopback' path between the transmitter and the receiver (if they are integrated on the same IC). Fig. 1 below represents the concept.

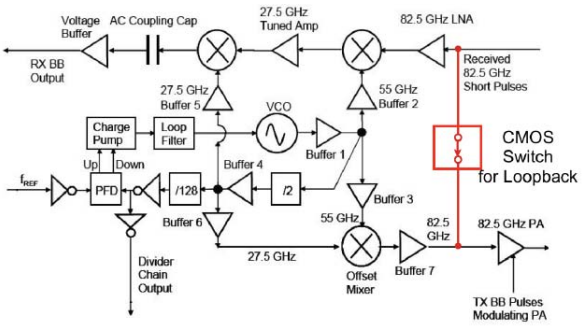

Figure 1: Schematic of the 77 GHz transceiver with 'loopback' bath between the receiver and the transmitter to enable BIST.

The key challenges to this approach are: a) the isolation in the switch (between ON and OFF states) needs to be very high to be able to discern between actual loopback signal and the leakage signal through the silicon substrate; b) develop an algorithm to be able to systematically test the whole chain for correct functionality.

SUMMARY OF RESULTS

We have designed and fabricated a high isolation single-pole-single-throw (SPST) CMOS switch in a 45 nm technology. The schematic concept and the layout is shown in Fig. 2.

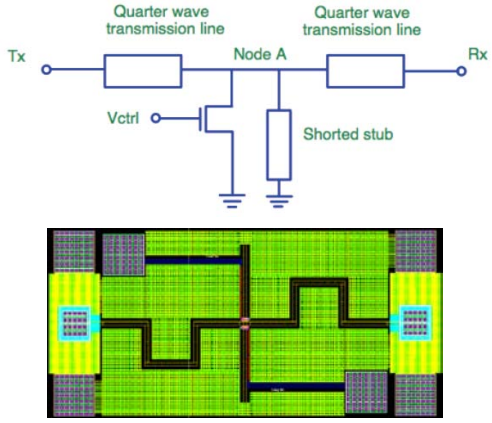

Figure 2: Schematic of the SPST switch and its layout.

The simulation results show that the switch has a loss of about 3 dB at 77 GHz while having an isolation of approximately 17 dB when in the OFF state. The simulation results are shown in Fig. 3 below.

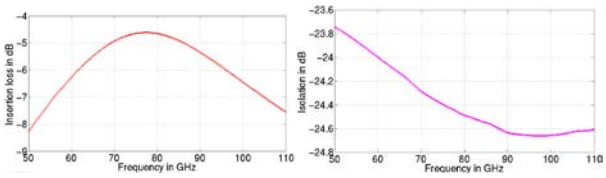

Figure 3: Simulation results of S_{21} for the switch in ON and OFF states. The switch provides an isolation > 20 dB between the ON and OFF states.

In the third year, the project will focus on extending the designs to smaller and better switches and also to develop a systematic testing plan to complete the BIST scheme.

Keywords: BIST, millimeter-wave, CMOS.

INDUSTRY INTERACTIONS

Texas Instruments, Freescale.

MAJOR PAPERS/PATENTS

[1] T. Mahzabeen, et. al., "A 77 GHz CMOS Switch with High-Isolation for Loopback Testing", (under preparation for IEEE MWCL).

TASK 1836.035, DEVELOPMENT OF CMOS SUB-THZ RECEIVERS FOR SPECTROMETERS

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SIGNIFICANCE AND OBJECTIVES

This work focuses on developing CMOS integrated receiver for spectrometer covering 180GHz-300GHz frequency band. Wireless spectroscopy can be used to identify different chemicals in a gas sample, which respond uniquely to electromagnetic waves, undergoing rotational and vibrational transitions at different frequencies. Wireless detection of some chemicals can find widespread use in safety and security as well as health care applications.

TECHNICAL APPROACH

As shown below in Fig.1, the 'sample-under-test' is excited with signals at a series of electromagnetic frequencies, and the transmitted waveform is down-converted and analyzed to determine the chemical contents in a sample. To cover the entire spectrometer band of 180-300 GHz we proposed that the receiver will be split-up into six sub-bands, covering 20GHz bands each so in all we have six receivers. In order to optimize the overall system performance, multiple architectures are analyzed and explored. Preliminary system level results indicate that the system Noise Figure achieved is < 18dB for an input RF power of -50dBm for direct down conversion receiver.

The key building block for the receiver is the front-end mixer. With current CMOS technology it is not possible to design active mixers using transistors at these frequencies. However, the high cut-off frequencies of Schottky Barrier Diodes (SBDs) in standard CMOS technology, allows us to design anti-parallel-diode-pair (APDP) based subharmonic passive mixers covering the 180-300 GHz bands. An anti-parallel diode pair (APDP) based mixer has been designed in a UMC 130nm CMOS process. The simulation results indicate a conversion loss of about -16dB for a 200GHz RF signal down-converted to an IF of between 10-20 MHz.

SUMMARY OF RESULTS

A 180-200 GHz APDP diode pair has been designed and fabricated in a UMC 130 nm CMOS technology (Fig. 1).

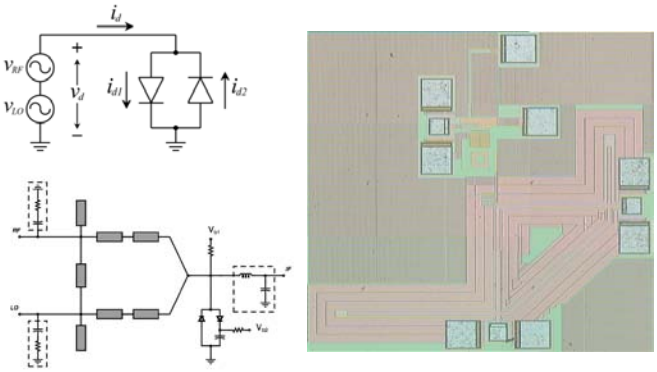

Figure 1: (a) Schematic of the APDP mixer. (b) Die-Photograph of the mixer.

Fig. 3 shows the measured output spectrum of the mixer where an RF frequency of 192 GHz is downconverted to an IF of 15 MHz using an LO of 95.9925 GHz.

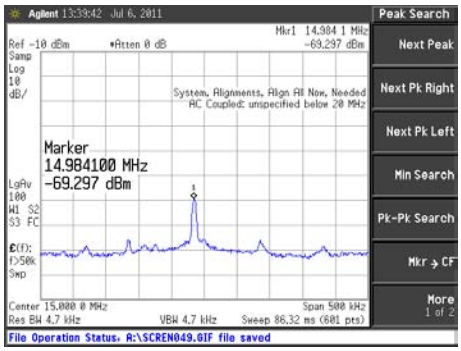

Figure 2: Measured spectrum of the intermediate frequency (IF) after downconversion.

In the third year, the project will focus on building the direct conversion receiver for the 180-300 GHz band.

Keywords: THz CMOS, spectroscopy, APDP Mixer.

INDUSTRY INTERACTIONS

Texas Instruments, Intel, IBM Research.

MAJOR PAPERS/PATENTS

[1] M. F. Hanif, et. al., "Development of CMOS Sub-THz Receivers for Spectrometer", to appear at SRC Techcon 2011.

TASK 1836.036, SIGNAL GENERATION FOR 200-300 GHZ SPECTROMETERS

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SIGNIFICANCE AND OBJECTIVES

As part of the effort to help open up high millimeter and sub-millimeter wave frequency range for moderate volume and cost applications, this task is studying the feasibility of realizing a transmitter in CMOS for a rotational spectrometer that detects harmful molecules and analyzes breath.

TECHNICAL APPROACH

This task will study the feasibility of realizing a transmitter for a rotational spectrometer in CMOS. The transmitted power should be ~10-100 μW. The main challenge is increasing the output frequency range, power, and frequency for phase locked signals. To realize a fast scan rate with a 10-kHz step, use of a fractional-N synthesizer will be investigated. The oscillator will operate at lower frequency than the output. The output signal is generated using a combination of an N-push technique and non-linear effects. This task will help generate the LO signal for the receiver.

SUMMARY OF RESULTS

To examine the feasibility of phase locking 300-GHz signal, a 195-GHz frequency divide four circuit driven by a 195-GHz oscillator with a 390-GHz push-push output similar to that shown in Figure 1 is fabricated in TI 45-nm CMOS. The divider successfully locked to 192.2-195.5 GHz indicating that it is possible to phase lock 390 GHz signal in CMOS. The measured radiated output power was also increased to 0.3 μW at 385GHz.

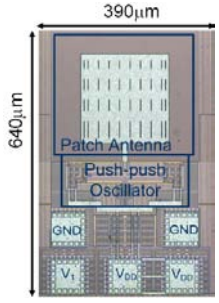

Figure 1: A 410-GHz oscillator fabricated in 45-nm CMOS. It integrates a patch antenna for quasi-optical measurements. Output power is 50 nW. It is reported in 2008.

The output power and locking range of 390-GHz oscillator is still too low for the spectrometer. To sufficiently increase these, most likely the oscillator should operate at even lower frequency. As mentioned, the output signal is generated using a combination of an N-push technique and non-linear effects. For instance, Figure 2 shows a 4-push oscillator that is used to generate 556GHz signal. The performance trade-off for operating the oscillator at 2, 4, and 8 times below the output frequency has been evaluated. It appears that operation at 8 times below the output frequency should allow generation of sufficient output power and tuning range for a single transmitter to cover the 180-300 GHz output range. Test structures for this circuit are being designed. Incidentally, the measured radiated output power of 4-push oscillator in Figure 2 is ~ 220 nW. This has ~4X and ~1.5X higher output power and operating frequency than that in Figure 1.

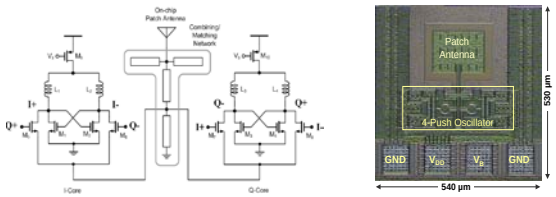

Figure 2: Architecture for signal generator. A 4-push oscillator for 556-GHz signal generation.

Approaches to achieve a fast scan rate (~ 1GHz/sec) with a step size of 10 kHz in a fractional-N synthesizer are also being researched. A test PLL will be taped out this fall.

Keywords: rotational spectrometer, transmitter, CMOS, millimeter-wave.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] K. K. O et al., "Sub-MM wave CMOS IC's and Systems," **(Plenary)** Invited to 2011 RFIT.

[2] D. Shim et al., "553-GHz Signal Generation in CMOS Using a Quad.-Push Osc.," 2011 Symp. on VLSI Circuits.

[3] D. Shim et al., "Paths to Terahertz CMOS Integrated Circuits," **(Invited)** 2009 Custom Integrated Circuits Conference.

[4] E.-Y. Seok et al., "Paths to Terahertz CMOS Integrated Circuits," IEEE Journal of Solid State Circuits, vol. 45, no. 8, pp. 1554 -1564, August 2010

TASK 1836.037, DEVELOPMENT OF ANTENNA AND CHIP INTERFACE SYSTEMS FOR MILLIMETER WAVE AND SUB-MILLIMETER WAVE APPLICATIONS

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ANDREW BLANCHARD, UNIVERSITY OF TEXAS AT DALLAS

SIGNIFICANCE AND OBJECTIVES

Feasibility study to develop techniques for designing and integrating high performance passive and RF matching components in the millimeter and sub-millimeter wave band. Techniques to improve radiation characteristics for antennas integrated into a CMOS processing strategy. This work is significant to developing cost-effective packaging for millimeter wave CMOS systems.

TECHNICAL APPROACH

The technical approach is to improve performance of planar antennas by using novel broadband geometries as compared to microstrip patches. The antennas will be integrated with CMOS ICs using a post-CMOS fabrication process utilizing photo-definable dielectric layers and gold metallization. Broadband antenna design and matching will be incorporated to minimize mismatch between the IC and antenna. Multiple transmission lines will be studied for optimizing CMOS integration. Simulation tools include FEKO for antenna design and Ansoft HFSS for interconnect and integration design. These results will lead to affordable mm-wave CMOS electronics for automotive radar and spectrometers for harmful molecule detection.

SUMMARY OF RESULTS

Figure 1 shows the top view of the 160 GHz broadband aperture antenna simulated in three environments. The antenna area is 2.7mm x 1.38 mm. In all cases, the antenna sits on benzocyclobutene (BCB) polymer dielectric (er = 2.65). The “ideal” case represents the antenna metal on BCB (120 micron thick) in free space. The “on silicon” case represents the antenna metal on BCB (120 micron thick) and a CMOS substrate (500 micron thick). The “w/ EBG” case represents the antenna metal on BCB (110 micron thick) an electromagnetic bandgap (EBG) layer (220 micron thick) and a CMOS substrate (500 micron thick). With the EBG, the antenna area increases to 3.23 mm x 2.04 mm.By including the EBG patch and via, the broadband nature of the antenna is preserved (53% ideal to 29% w/EBG) and the antenna radiation pattern is improved (8dB ideal to 11 dB w/EBG) as shown in Fig. 2. The feed line for the antenna is coplanar waveguide (CPW) and attenuation results for three geometries are shown in Table 1 at 100 GHz.

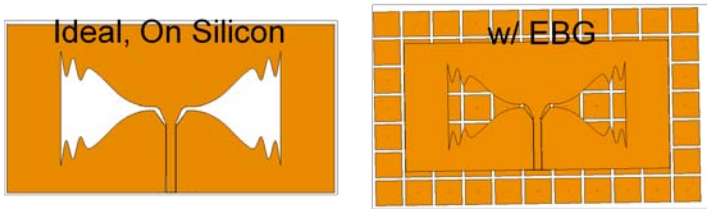

Figure 1: Broadband planar aperture antenna in the following environments: ideal, on silicon, with EBG.

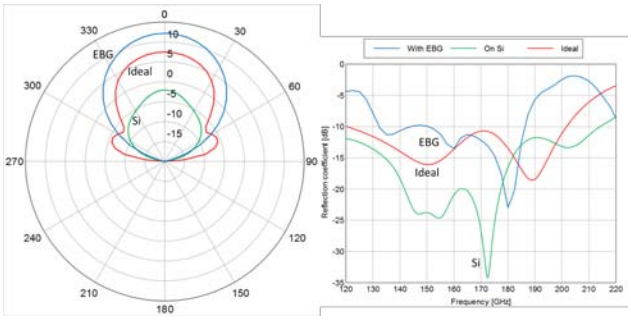

Figure 2: Simulated return loss and 155 GHz radiation pattern.

Table 1: Attenuation of CPW lines at 100 GHz

CPW	w(µm)	g (µm)	w+2g (µm)	(dB/mm)
1	52	10	72	1.76
2	20	10	40	1.24
3	12.5	10	32.5	1.13

Keywords: aperture antennas, broadband, benzocylobutene, coplanar waveguide, integration

INDUSTRY INTERACTIONS

Intel, Texas Instruments

MAJOR PAPERS/PATENTS

[1] R. Islam et al., “Performance of Coplanar Interconnects for Millimeter-Wave Applications,” submitted to IEEE 2012 SiRF.

[2] R. Pierce et al, “Broadband Modified Bowtie Aperture Antenna,” SRC TechCon 2010, September 2010, Austin, TX.

TASK 1836.045, FREQUENCY CHANNELIZED ADC FOR WIDE BANDWIDTH SYSTEMS

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SIGNIFICANCE AND OBJECTIVES

The objective of this work is to develop a new approach for achieving low-power, compact, medium-to-high resolution (≥ 6 ENOB) analog-to-digital conversion for multi-gigahertz wideband signal.

TECHNICAL APPROACH

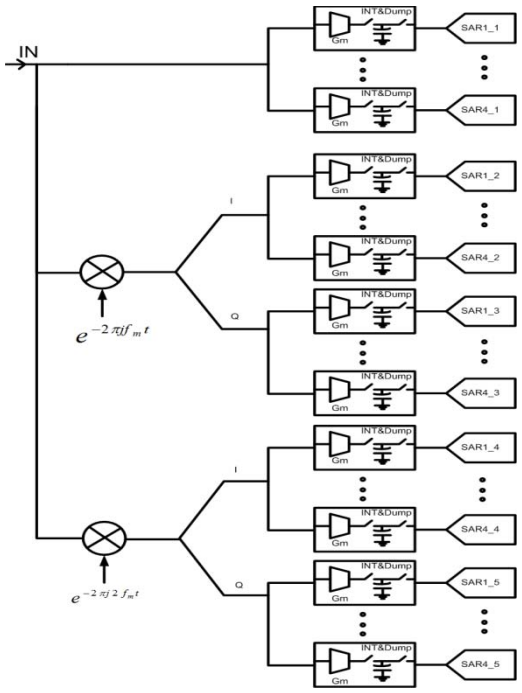
As designing both high resolution and high sampling frequency data converter is difficult, the wideband signal can be decomposed into narrower frequency subbands then digitized using narrowband ADCs that operate at a fraction of the signal Nyquist rate. The proposed architecture should enable more efficient medium-to-high resolution (≥ 6 ENOB) data conversion of a multi-gigahertz wideband signal.

SUMMARY OF RESULTS

To digitize a multi-gigahertz bandwidth signal, a commonly used approach is to time-interleave multiple ADCs, each operating at a fraction of the desired sampling frequency. Such time-interleaved ADC (TIA) suffers from numerous implementation challenges, mostly resulting from the large input bandwidth that each ADC must support. A fundamental problem of the time-interleaved architecture is the mismatches among the demultiplexing channels. These mismatches are especially pronounced when operating at high data rates, as small transistors with corresponding small input capacitance are employed to meet the bandwidth requirements. The resulting offset problems often increase the design complexity by requiring additional compensation circuitries. Another important drawback is the high sensitivity to sampling jitter caused by aliasing of the wideband input signal and the need to generate accurate multi-phase clocks.

Instead of channelizing by time-interleaving ADCs, we are currently designing an ADC that decomposes the received signal into multiple frequency subbands before sampling. As designing bandpass filters centered at high frequencies to generate the multiple frequency subbands is difficult, especially in integrated circuits, the wideband signal can be decomposed using a bank of mixers and lowpass filters. To reduce area, the lowpass filters are implemented as integrate-and-dump filters. This architecture mitigates many of the TIA implementation challenges. In addition, it can be shown that significant reduction in power consumption can be achieved.

The chip we are designing is shown in the figure below. The input signal is decomposed into three subbands. Each subband output is 4-way time-interleaved. Since there are one real subband and two complex subbands, we can view this architecture, which consists of 5-banks of 4-way time-interleaved sub-ADCs, as effectively achieving 20-way time-interleaving. The chip will be submitted for fabrication soon.



Keywords: ADC, digital compensation, frequency channelization

INDUSTRY INTERACTIONS

Texas Instruments, Freescale

MAJOR PAPERS/PATENTS

None to date

TASK 1836.047, INTEGRATION OF MILLIMETER WAVE ANTENNAS USING SYSTEM IN PACKAGE TECHNIQUES

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SIGNIFICANCE AND OBJECTIVES

Feasibility study to develop new techniques for the integration of broadband, high performance antennas with state-of-the-art millimeter wave CMOS circuits. Support the development of low cost automotive radar and spectrometer applications. This work is significant to achieving packaged performance metrics while being affordable.

TECHNICAL APPROACH

The technical approach is to optimize performance of foundry CMOS silicon circuits with broadband antennas integrated onto a low-cost package substrate. Flip-chip assembly and high performance transmission line feeds will be used to attach the IC to the substrate and provide the smallest footprint. Simulation is used to predict loss tangent influence and fabrication is used to confirm the results.

SUMMARY OF RESULTS

50-Ohm coplanar waveguide (CPW) and microstrip transmission lines have been simulated and fabricated on Rogers RT/duroid (ε_r = 2.2, tan δ = 0.0009) and Isola Global's FR408 (ε_r = 3.65, tan δ = 0.013). Fig. 1 shows the top view of the lines fabricated on duroid along with a transition from CPW to microstrip for ground-signal-ground measurements. One microstrip transition uses a small via to connect the top and bottom ground metals while a second transition uses electromagnetic techniques to couple energy from the top ground to the bottom. Figure 2 shows the measured versus simulated (Ansoft HFSS) S-parameter performance of a 1 mm coplanar line. Fabrication of the lines for millimeter wave applications require narrow gaps that are less than 25 microns. The standard foundry process requires gaps that are 30 microns wide. Novel etching techniques are being employed to account for etching thick layers of copper while trying to achieve the dimensions shown in Table 2. Transmission lines and transitions fabricated on laminate substrates at UT Dallas and by a vendor will be compared up to 110 GHz.

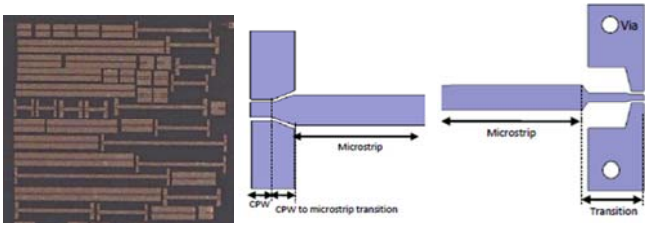

Figure 1: Photograph of fabricated CPW and microstrip lines.

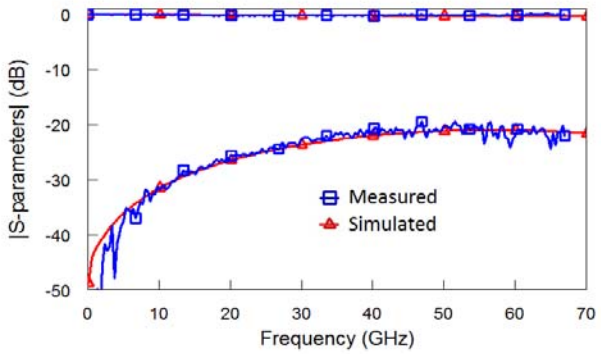

Figure 2: Measured vs. simulated 1 mm CPW line.

Table 1: Coplanar waveguide attenuation comparison.

Technology	w (m)	g (m)	Attenuation (dB/mm)
RT/duroid	90	15	0.07
GaAs	120	40	0.09
CMOS w/o p^+well	9.5	4	1.0
CMOS w/ BCB	60	8	0.96
FR408	135	40	0.13

Keywords: antenna in package, coplanar waveguide, FR4, millimeter wave CMOS

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] S. Aroor, et. al., "Characteristics of Interconnects on FR408 at Millimeter-Wave Frequencies, submitted to Journal of Microelectronics and Electronic Packaging, 2011.

TASK 1836.048, MILLIMETER AND SUBMILLIMETER GAS SENSORS: SYSTEM ARCHITECTURES FOR CMOS DEVICES

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SIGNIFICANCE AND OBJECTIVES

The objective of this project is to develop an approach to a compact and inexpensive gas sensor based on millimeter and submillimeter (mm/submm) spectroscopy and implemented in CMOS technology. The dramatic cost, size, and power savings of CMOS will make this attractive sensor competitive in the mass market.

TECHNICAL APPROACH

We have demonstrated that powerful and unique sensors in the mm/submm spectral region are now practical. This task (coordinated with other tasks that will provide the necessary CMOS antennas, receivers, and transmitters) seeks to develop and demonstrate architectures appropriate for the mass market. This will be accomplished by an iterative interaction between our sensor design background, the development of an intermediate approach based on mass-market technology, and the CMOS design teams. New applications will be developed and demonstrated.

SUMMARY OF RESULTS

This project is designed to interface closely with three CMOS development projects. These projects are to develop a probe source for the gas sensor, a sensitive heterodyne receiver, and antennas to transmit the microwave power from the source, through the gas interaction region, and onto the detector.

Last year, with our CMOS collaborators, we arrived at a design for each of the three elements and these CMOS development activities are underway. We have now provided an end-to-end analysis of the dynamic range and sensitivity of this design as well as a comparison with our baseline systems. We have also carried out a detailed analysis of the impact of the clutter due to atmospheric gases on submillimeter gas sensors [1].

In parallel with this effort we are developing systems based on the best available mass-market technology. Figure 1 shows spectroscopic results from a system based entirely on a commercially available chip set from Hittite.

We have also considered and evaluated as a gas sensor an integrated Rx/Tx system from IBM. We are in the process of signing a joint research agreement that will provide one of these units to OSU, along with technical support from IBM. We continue our work with TI as they develop an in-house mm/submm system. We are working with them as they adapt an existing synthesizer for use in their system as well as for our use and evaluation.

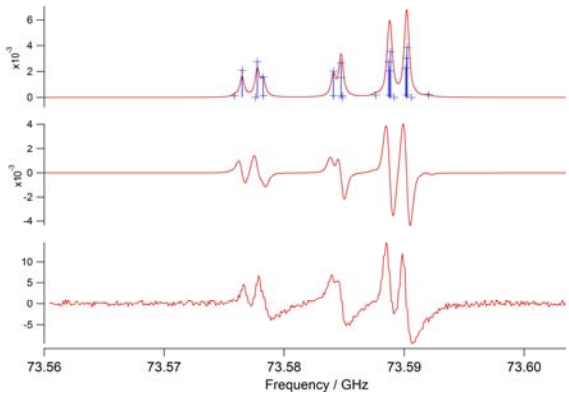

Figure 1. A comparison between theory (upper two panels) and experiment (lower panel) for gas sensor based on Hittite 'wireless' communications parts.

Interactions with Applied Materials and UT-D have lead, respectively, to considerations of two applications: Diagnostics and process control of semiconductor plasma reactors and applications in medical breath analysis. For the former we are in advanced discussions about how to move forward to a demonstration and for the latter we will provide spectroscopic laboratory support.

Keywords: compact submillimeter spectroscopic gas sensor

INDUSTRY INTERACTIONS

Texas Instruments, IBM, Applied Materials

MAJOR PAPER

[1] Medvedev, Neese, De Lucia, and Plummer, Applied Optics 50, 3028 (2011).

TASK 1836.054, SILICON BASED BEAMFORMING ARRAYS FOR MILLIMETER WAVE SYSTEMS

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SIGNIFICANCE AND OBJECTIVES

The completed tasks include a complete integration of a seven-channel receiver system that operates at 2.4 GHz, designing, building and testing 2.4 GHz antenna array for the receiver system, an experimental investigating on the beamforming algorithms using an experimental phased-array system, designing antenna array in the millimeter wave range, and building a simulator for millimeter wave imaging algorithms.

TECHNICAL APPROACH

There are many challenges and opportunities for integration of antenna arrays into silicon substrate for millimeter imaging systems. We have analyzed an architecture with digitally controlled RF phase shifters to achieve a high beamforming gain for millimeter wave imaging systems. We incorporate antennas designed for silicon on chip and verify the design via antenna simulators and paln to conduct actual measurements using UTD's antenna measurement chamber. Finally, we will incorporate beamforming array into silicon on chip mm-Wave radio with the aid of our industrial and TXACE collaborators.

SUMMARY OF RESULTS

One of the main goals of this project is to implement a mm-Wave imager using CMOS technology. To achieve this goal, as a first step, we have been working on a simulator that implements a 2D image reconstruction algorithm. Our algorithm assumes that the object being scanned is in the near field. Our algorithm utilizes the use of Fourier transforms. The main idea is that there are two apertures. The first one is the scanned aperture where the transceiver is located and the target aperture where the target is located. The transceiver has a wide beam width antenna. The scanned aperture is divided into points in the x-y direction. The transceiver moves at each point, transmits a wide beam width signal that hits the target and gets received by the receiver. The received signal shown in the equation below contains information about the target. This information include the amplitude which is determined by the strength of the reflected signal and the accompanied delay (phase) from each point on the target aperture.

$$s(x',y') = \iint f(x,y)e^{-j2k\sqrt{(x-x')^2+(y-y')^2+{z_0}^2}}$$

where $f(x,y)$ is the reflectivity function of the image. The image is approximately estimated based on the narrow band reconstruction algorithm as follows:

$$f(x,y) = FT_{2D}^{-1}\left[FT_{2D}[s(x',y')]\sqrt{4k^2-k_x^2-k_y^2}\,e^{-j\sqrt{4k^2-k_x^2-k_y^2}\,z_0}\right]$$

This reconstruction algorithm can be readily implemented using FFT's for efficient processing. We present simulation results using the above algorithm for the reconstruction of a point scatterer. Assuming a point scatterer gives the Point Spread Function (PSF) of this imaging system. The first set of results will provide a narrow band system at 60 GHz, with a square 128*x*128 element array of Transmitter/Receiver elements with $\frac{\lambda}{4} = 1.25mm$ element spacing. The point target is placed at a distance of 80mm from the array. In Figure 1, we illustrate the PSF using the reconstruction algorithm given in (2) from linear sequentially switched array.

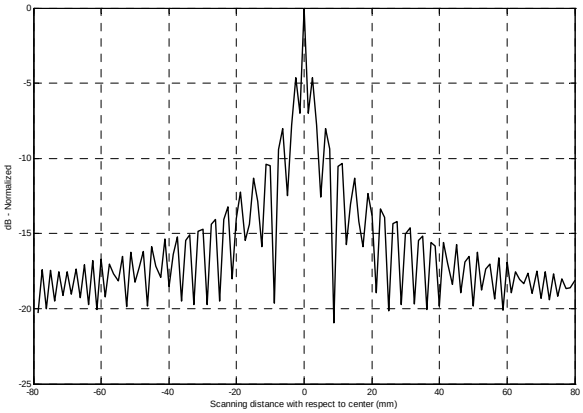


Figure 1: Point spread function for source at x=0mm, y=0mm, and z=80mm.

We have developed of a 2.4 GHz antenna array for verification of the mathematical imaging models [1].

Keywords: Millimeter waves, imaging, beamforming, silicon antennas, antenna array

INDUSTRY INTERACTIONS

Texas Instruments, IBM

MAJOR PAPERS/PATENTS

[1] A. Morshedi and M. Torlak, "Measured Comparison of Dual-Branch Signaling over Space and Polarization Diversity," IEEE Trans. On Antennas and Propagation, no. 5, vol. 59, May 2011, pp. 1678 - 1687

TASK 1836.067, CHARACTERIZATION OF CMOS BASIC BUILDING BLOCKS FOR SUB-THZ WIDEBAND TRANSMITTERS

PROF. MONA HELLA, MICHAEL SHUR, AND X.C-ZHANG, RENSSELAER POLYTECHNIC INSTITUTE, HELLAM@ECSE.RPI.EDU

SIGNIFICANCE AND OBJECTIVES

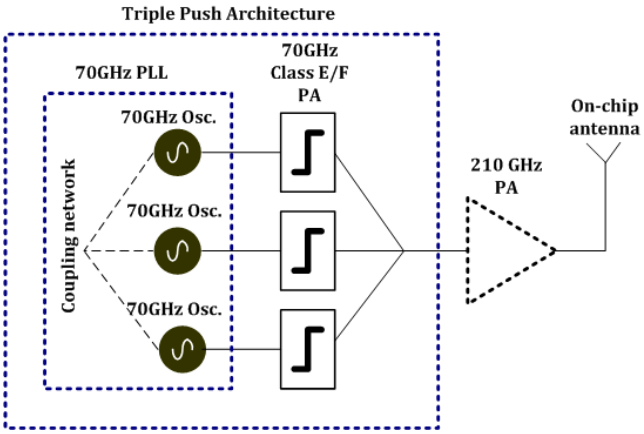
As the electronic industry continues to make progress, higher operating frequencies are desired to meet larger bandwidth communication, higher imaging resolution, and facilitate antenna integration with on-chip transceivers. The objective of this proposal is to develop an optimum design procedure for efficient wide band transmitters in the WR5 (140-220GHz) range, and bench mark the resulting transmitter architectures against existing discrete sub THz systems.

TECHNICAL APPROACH

To increase the output power of CMOS sub THz sources, active combining using power amplifier stages will be incorporated in harmonic based N-push oscillators. This technique will be compared against the amplification at lower frequency and using frequency multipiers. Spatial combining and traditional on-chip combiners such as Wilkinson and transformer combiners will also be considered. In the mm-wave and sub-THz regions, the quality factor of the varactors in any oscillator dominates the tank losses. Achieving wide tuning range would require other techniques for frequency tuning. This will be done using magnetic tuning or tuning based on changing the properties of the active devices in the oscillator core.

SUMMARY OF RESULTS

Signal generation is a challenge at sub THz frequencies due to the limitation of fmax of the CMOS process and the low quality factor of passive components due to substrate losses. Our approach is based on using a triple push oscillator with active combining network where three coupled fundamental oscillators generate identical signals which are $2\pi/3$ apart in phase as shown in Fig. 1. Advantages of N-push oscillators include better tuning range and lower phase noise. The core oscillator is designed at 73GHz using Colpitts topology. A buffer stage is used as a nonlinear class amplifier to boost the third harmonic at 219 GHz. The core inductors in the oscillator were designed using a nested configuration for area savings, while the buffer inductance uses a shielded coplanar waveguides which act as a combining network to boost the third harmonic and suppress the lower harmonics. The use of shielded coplanar waveguides is particularly noteworthy owing to its ability



to shorten the length of the transmission line and lower the effect of substrate loss. Table 1 summarizes the results of the oscillator to date. Future work includes the integration of additional amplification stages and on-chip and or spatial power combining.

Type	Technology	Frequency (GHz)	Power (dBm)	Tuning Range (GHz)
ILFD	65nm CMOS	116	-15	116.1-116.4
Fund.	InP	267.4	-5.1	NA
Push--push	90nm CMOS	131	-15.2	129.8-132
Push--push	0.13µm CMOS	192	-20	191.4-192.7
Push-push	45nm CMOS	410	-47	409-413
Triple-push	0.13µm CMOS	256	-17	Fixed freq.
Triple-push (this work)	**90nm CMOS**	**210**	**-3.2**	**210-231**

Keywords: N-push operation, on-chip power combiners, CMOS THz generation, VCOs, power amplifiers.

INDUSTRY INTERACTIONS

Texas Instruments.

MAJOR PAPERS/PATENTS

[1] B. Catli, M. M. Hella., "Triple Push Operation for Combined Oscillation/Divison Functionality in Millimeter-Wave Frequency Synthesizers" *IEEE Journal of Solid State Circuits*, August 2010.

TASK 1836.074, SUB-45NM CIRCUIT DESIGN FOR TRUE RANDOM NUMBER GENERATION AND CHIP IDENTIFICATION

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CHRISTOF PAAR, UNIVERSITY OF MASSACHUSETTS / U. BOCHUM, GERMANY

SIGNIFICANCE AND OBJECTIVES

Variations in fabrication process and operating conditions affect the reliability and performance of modern digital circuits. True Random Number Generators (TRNGs) and Physical Unclonable Functions (PUFs) are important cryptographic primitives sensing variability as randomness and secret. This project explores the modeling, analysis and variability aware design of TRNGs and PUFs.

TECHNICAL APPROACH

The project explores the effect of variation in fabrication process and operating conditions on metastability based TRNG and delay based arbiter PUF circuits. The variations in transistor parameters and on-chip thermal noise (the source of randomness) are modeled in SPICE using 45nm NCSU models to have random Gaussian distribution. Monte-Carlo simulations are run for 10K-100K cycles. Bit entropy is used as the basic measure of randomness of the bits simulated. The arbiter PUF circuits are simulated and taped out in 45nm CMOS with special design to near threshold operations. Simulation methodologies and post-silicon validation platform have been proposed to evaluate PUF uniqueness, reliability and security.

SUMMARY OF RESULTS

TRNG: An ideal metastability based TRNG is expected to generate bits with a bit entropy very close to 1. But, with increasing across chip variation and device mismatch, the output is observed to be more deterministic. The bit entropy of the output falls down to 0.6 with 4% mismatch in the effective lengths of the pull-down transistors. The XOR function and von Neumann corrector extracts entropy close to 1 without significant drop in bit-rate for upto 3% device mismatch. We explore a hybrid self-calibration technique using coarse grain circuit calibration followed by continuous algorithmic correction using either the XOR function or the von Neumann correction to provide a fine grained entropy extraction. Results indicate that the hybrid calibration technique provides upto 4X improvement in both the bit entropy and bit-rate for intra-die transistor length variations as much as 10%. The control logic for the state machine of the self-calibration occupies a negligible 128um^2 of area and contributes to 0.82fJ per TRNG bit. At 1Gbps, the overall energy consumption of the TRNG is 0.5 pJ/bit. Future directions for this project will be to explore efficient methodology for analysis, stochastic models for the TRNG circuit and variability aware design.

PUF: An arbiter-based PUF can sense the total delay mismatch of two long gate chains and provide a uniqueness identification of each PUF chip with challenge-response pairs (CRPs). We proposed a statistical analysis approach to verify the functionality, uniqueness, reliability and security of 45nm arbiter PUFs. Simulation shows that using advanced technologies and reducing supply voltage can significantly improve PUF uniqueness with negligible reliability and security compromises. Results from test chips further demonstrated that our 45nm PUF implementation has improved the uniqueness by 27% over an earlier 180nm implementation.

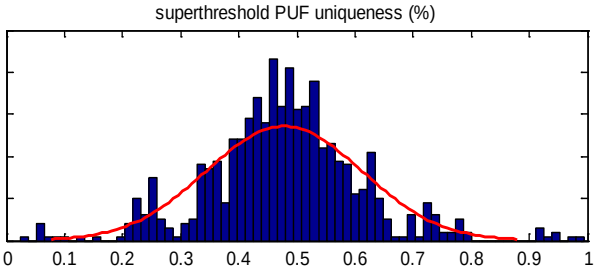

Figure 1: Uniqueness distribution of PUF test chips

Future directions include error correcting codes or selective challenge methods to mitigate the PUF reliability issues due to reduced noise margin under low operation voltage.

Keywords: True Random Number Generator (TRNG), Physical Unclonable Function (PUF), SPICE, Variability.

INDUSTRY INTERACTIONS

Intel, IBM

MAJOR PAPERS/PATENTS

[1] V. Suresh *et al.*, "A Hybrid Self-calibration Technique to Mitigate the Effect of Variability in TRNG," VARI, 2011.

[2] V. Suresh, *et al.*, "Techniques for Robust TRNG in Nanometer CMOS", TECHCON, 2011.

[3] L. Lin, *et al.*, "45nm Arbiter-Based Physical Unclonable Function Design", TECHCON, 2011.

TASK 1836.079, CMOS THZ DETECTION

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SIGNIFICANCE AND OBJECTIVES

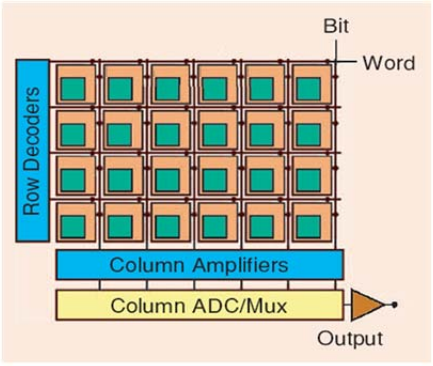
The successful development of practical, room-temperature THz systems, composed of tunable sources and detectors, in low cost CMOS technology will increase the applications of the THz regime from large and costly scientific instruments to future markets in security, nondestructive industrial quality control, and medical-diagnosis. This project investigates design methodologies for high sensitivity, low noise CMOS THz detector arrays.

TECHNICAL APPROACH

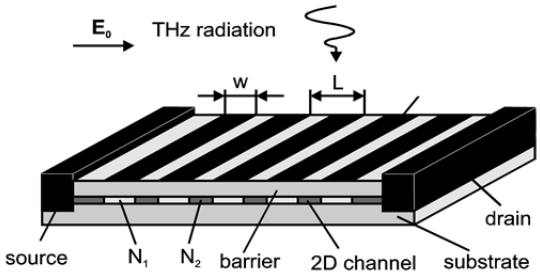
Dyakonov and Shur have developed the theoretical framework on plasma-wave-induced phenomena in the channels of FETs. The nanometer size FET is an ideal fit as a THz sensitive element for a single transistor detector or an element of array. The detected THz signal of each individual plasma wave nano-FET is a function of the gate bias and width, THz beam orientation, spectral profile and polarization. In this project, a THz imaging receiver will be implemented in 65nm CMOS technology. For the single FET THz detector, the effects of technology scaling on device behavior will be investigated, including the effect of parasitics. While biasing in deep saturation region has been shown to increase FET responsivity by a least 2X, this comes at the expense of increased noise. Optimum biasing/physical design and circuit techniques for noise reduction will be exploited. On-chip antennas will be employed to improve signal coupling to the THz detector. The improvement for on-chip integrated antennas such as dipole, and patch antennas will be quantified. Further improvement in the THz detector when introducing delays between the signal coupled to the gate and drain will be experimentally verified.

SUMMARY OF RESULTS

A number of FET array structures with and without antennas have been fabricated. Several designs and dimensions have been considered. A 2-D device array of FETs connected in parallel that is 1.5 mm x 1.5 mm to capture the entire beam of THz at 200 GHz. Connecting metal layers were designed using EM simulations to ensure optimum coupling efficiency. Furthermore, simple two-device arrays of varying widths were fabricated, both in series and in parallel. These structures will be used to characterize large array structures, with the small ones serving as the most basic building unit. Finally, one-device structures of varying widths were fabricated in order to characterize device input impedance at the gate.



Imaging Receiver formed of CMOS THz detector array



Possible schematic of a grating-gate FET structure to increase THz coupling

A significant research effort is focused in this project on antenna designs to enhance coupling at 0.2THz, 0.6THz, and 1.63THz. For the antenna design, each antenna structure was optimized and chosen based on the minimum reflection coefficient. Optimization was performed in HFSS using optometric parameter simulation on antenna width, length, and quarter-wave transformer dimensions in the case of patch antennas. Simulation results yielded the optimal dimensions for each resonant frequency, and also showed the robustness of designs to impedance variations.

Keywords: plasma-wave detectors, CMOS FET THz detection, THz imaging systems

INDUSTRY INTERACTIONS

Texas Instruments.

MAJOR PAPERS/PATENTS

[1] V. V. Popov, N. Pala, and M. S. Shur, “Room temperature terahertz plasmonic detection by antenna arrays of field-effect transistors”, submitted to International Journal of High Speed Electronics and Systems

TASK 1836.082, LOW-COST ENERGY-EFFICIENT 60GHZ TRANSCEIVERS WITH BUILT-IN SELF-TEST (BIST)

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PROF. ALI NIKNEJAD, UC BERKELEY, NIKNEJAD@EECS.BERKELEY.EDU

SIGNIFICANCE AND OBJECTIVES

Although CMOS-based 60GHz transceivers have entered commercial production, the cost and power consumption of these designs must be reduced substantially to enable broad adoption. This project will therefore explore techniques to both drastically improve 60GHz transceiver energy-efficiency and to eliminate the need for expensive mm-wave packaging and external testing.

TECHNICAL APPROACH

The cost of mm-wave transceivers is often dominated by packaging and testing considerations. A key thrust of this project is therefore to explore efficient and compact on-chip mm-wave antenna arrays in order to enable the use of inexpensive packaging as well as built-in self-testing of the entire signaling path. Furthermore, aggressive power reduction is being pursued through optimized design of both the mm-wave and baseband CMOS circuits. Specifically, high-impedance and low-overhead circuitry phase-array elements are critical to reducing the power of the mm-wave circuitry, and a mixed-signal processing approach appears promising in achieving drastic reductions in baseband power.

SUMMARY OF RESULTS

Current 60GHz CMOS transceiver designs utilize 16-32 element phase-arrays on both the transmitter and the receiver, with power consumption and package and/or chip area growing quickly as the mm-wave components within each element are replicated. Given these costs, and particularly for relatively short-distance links, the number of antenna elements must be carefully optimized. Initial studies have therefore focused on creating a framework including link budget considerations as well as circuit-level details under which this optimization can be performed. Preliminary results from the framework indicate that asymmetric architectures with a larger number of transmitter antenna elements may be advantageous. Improving transmitter efficiency at low per-element output power is critical to realizing this potential, and hence designs to realize this goal are currently being explored.

The other main initial thrust of this project has been on exploring the antenna efficiency, directivity, area, and system/package implications/tradeoffs of on-chip antennas. Slot-loop and leaky wave on-chip antennas both appear capable of achieving efficiencies greater than 20-30% at mm-wave frequencies. Slotted designs appear promising in terms of compactness, while the leaky wave structure can eliminate the need for explicit TR switches.

In upcoming years this project will continue to focus on the initial studies outlined above as well as self-testing techniques and baseband design. Experimental demonstrations of on-chip antennas and low-power transmitter elements in a 65nm CMOS technology are planned for the second year. Furthermore, these core concepts will be developed and explored at higher carrier frequencies (>100GHz) where antenna integration may be even more compelling.

Keywords: mm-wave, antennas, low-power, mixed-signal

INDUSTRY INTERACTIONS

Texas Instruments, Intel, IBM

MAJOR PAPERS/PATENTS

TASK 1836.083, BUILT-IN TEST FOR POWER-EFFICIENT MILLIMETER-WAVE ARRAYS

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SIGNIFICANCE AND OBJECTIVES

This program will develop orthogonal code-based built-in-test techniques for millimeter-wave arrays which will allow for simultaneous testing of all elements in the array at either circuit or package level, reducing the time and cost of test. Power-efficient 60-GHz transmitter structures with BIST will be demonstrated.

TECHNICAL APPROACH

A low-power 60-GHz phased-array transmitter prototype with built-in-self-test will be developed in 0.12-µm SiGe BiCMOS technology and then scalable test techniques will be developed for this demonstration platform. These test techniques will exploit code-division multiple-access techniques to allow for simultaneous or parallel testing of all array elements. CDMA-based test techniques will be compared to both external test and traditional BIST techniques. A single transmit chain will be developed followed by a four-element 60-GHz phased-array prototype.

SUMMARY OF RESULTS

This project kicked off in March 2011. In the first five months, baseline 60-GHz transmitter circuits have been designed, including a 60-GHz power amplifier (PA) and a 60-GHz passive phase shifter, both in 0.12-µm SiGe BiCMOS technology. One critical objective for the project is to explore novel power-efficient circuit and system topologies. As a first step towards this goal, the baseline 60-GHz circuits have been developed for lowest possible power consumption. The PA targets state-of-the-art power-added efficiency performance (i.e., >20%), whereas the phase shifter targets a novel topology to allow for all-passive 360° phase-shift coverage. These circuits will be taped out in August 2011 using IBM SiGe-8HP technology through MOSIS.

In the upcoming year, the phase-shifter and PA design will be integrated together to form a single-element 60-GHz transmit chain. On-chip sensors for power and temperature will be embedded at multiple places through the transmitter chain to allow for measurement of output power, gain, and phase shift. Additionally, variable amplifier and/or variable phase-shifters within this front-end will be designed to allow for direct modulation with simple orthogonal codes which in turn will allow for the parallel testing of multiple array elements.

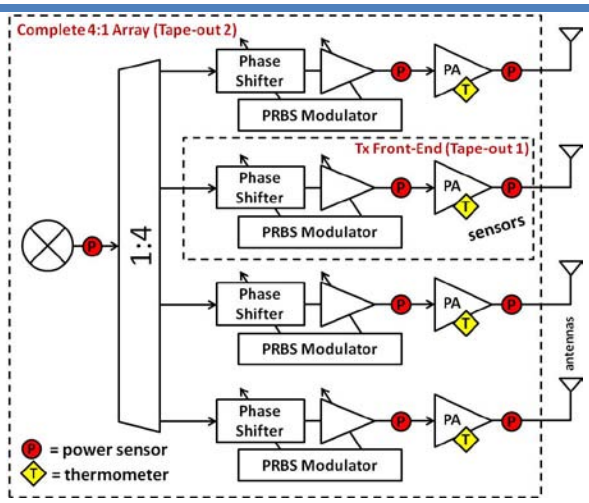

Figure 1: Block diagram of proposed 60-GHz phased-array prototype with built-in-test capabilities.

This single transmitter chain will be taped out in late 2011/early 2012 in IBM SiGe BiCMOS 8HP technology. After fabrication, both the individual PA and phase shifter circuits as well as the single-element transmitter chain will be measured and the results will be correlated to simulations. Finally, in the coming year, system-level simulations will be started to evaluate CDMA-based built-in-test techniques for parallel testing of elements in the array.

Keywords: millimeter-wave, phased-arrays, built-in test, 60-GHz, CDMA

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

None

APPENDIX I, TEXAS ANALOG CENTER OF EXCELLENCE FACILITY

The University of Texas at Dallas (UTD) has prepared a ~7500 ft^2 area on the 3rd floor of Engineering and Computer Science North building to form an enhanced centralized group of laboratories dedicated to analog engineering research and research training.

Figure is a 3D sketch of the facility. The facility includes RF and THz, Integrated System Design, Embedded Signal Processing, and Analog & Mixed Signal laboratories as well as CAD/Design laboratory structured to promote collaborative research**.** Figure I.2 presents the facility floor plan showing the dimensions of each laboratory.

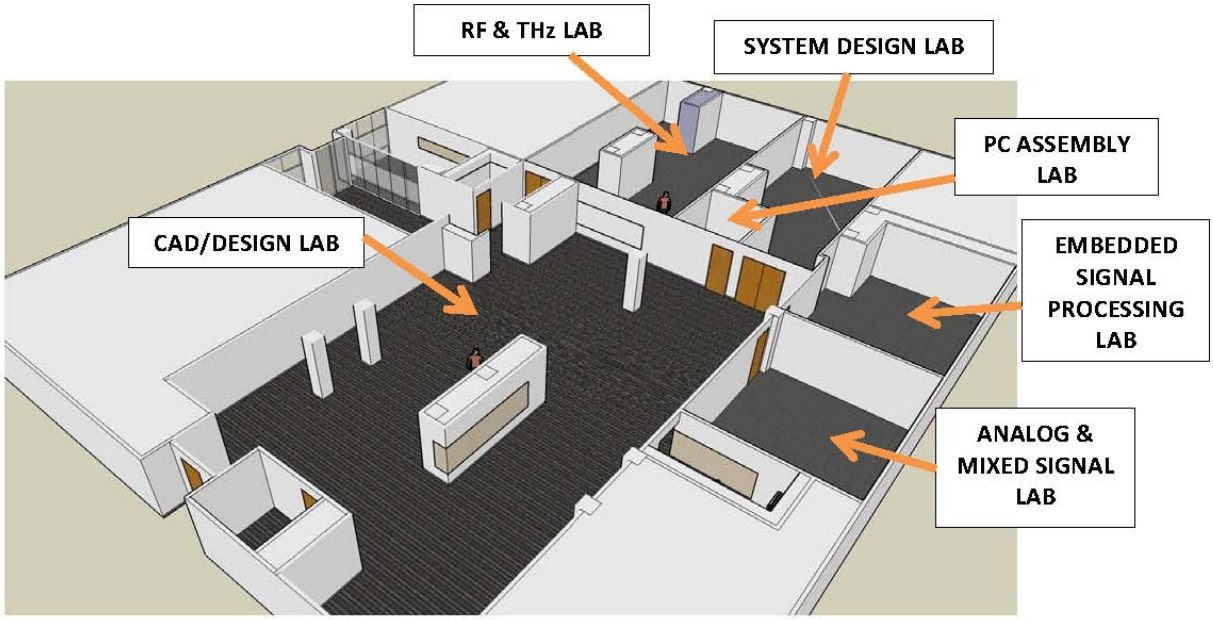

Figure I.1: TxACE Analog Research Facility sketch

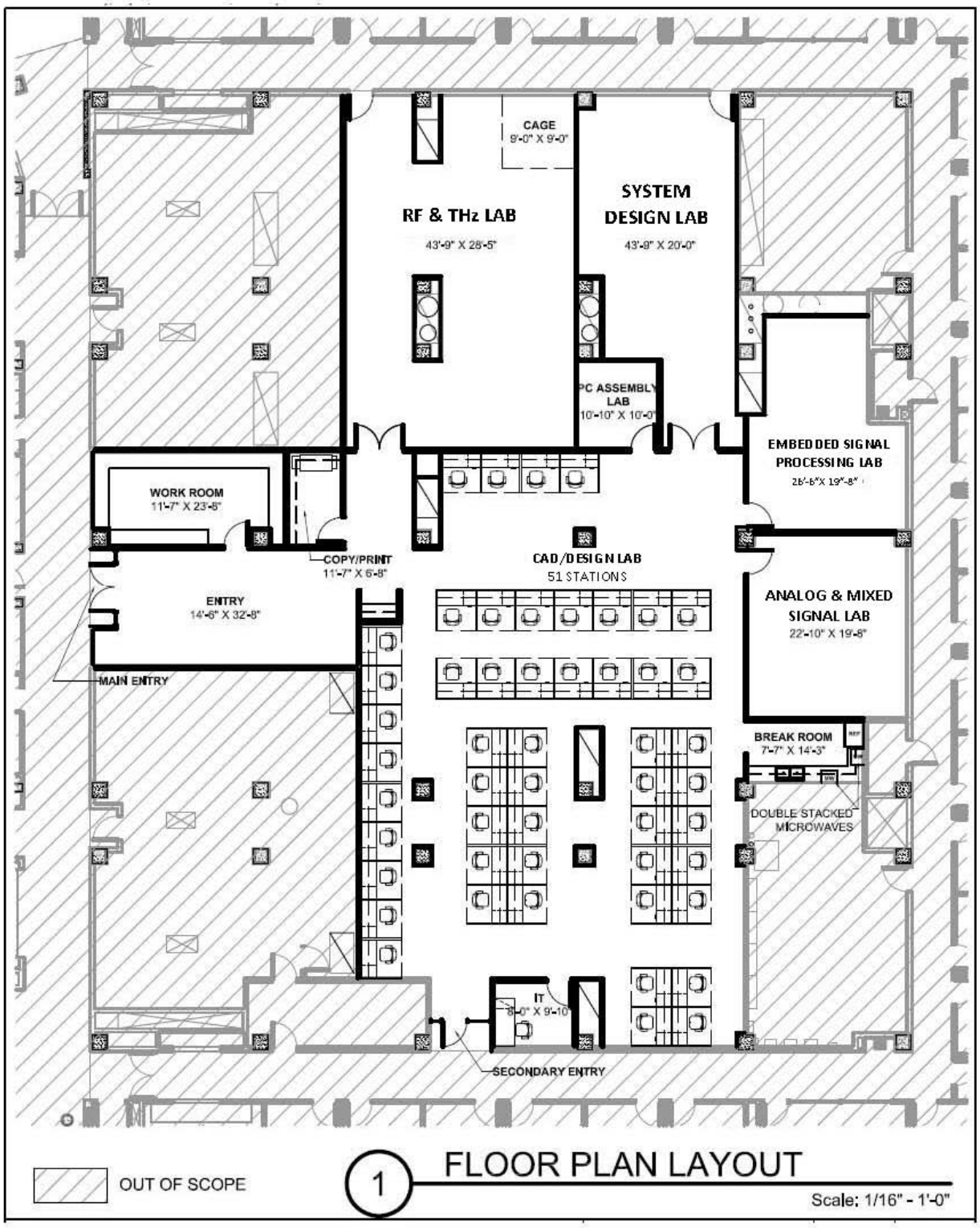

Figure I.2: TxACE Analog Research Facility floor plan

APPENDIX II, PUBLICATIONS OF TXACE RESEARCHERS

CONFERENCE PUBLICATIONS

(1) H.S. Yeom and B. Bakkaloglu, "Temperature Compensated, High Common Mode Range, Cu-Trace Based Current Shunt Monitor Amplifier", SRC TECHCON2010 Conference, Austin, TX, Sep. 2010.

(2) Vasan, B.K.; Geiger, R.L.; Chen, D.J.; , "Linearity testing of ADCs using low linearity stimulus and Kalman filtering," Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS), pp.3032-3035, May 30 2010-June 2 2010.

(3) Vasan, B.K.; Chen, D.J.; Geiger, R.L.; , "Linearity testing of Analog-to-Digital Converters using imprecise sinusoidal excitations," Proceedings of the IEEE 2010 National Aerospace and Electronics Conference (NAECON), vol., no., pp.334-337, 14-16 July 2010.

(4) Vasan, B.K.; Chen, D.J.; Geiger, R.L.; , " Analog to Digital Converters (ADC) Non Linearity Testing with Low Linearity Monotonic Signals," Proceedings of the IEEE 2011 International Instrumentation and Measurement Conference (I2MTC), (To appear May 2011).

(5) Jingbo Duan and Degang Chen , “SNR Measurement Based on Linearity Test for ADC BIST” IEEE ISCAS May 2011 (To appear).

(6) Jingbo Duan, Le Jin and Degang Chen , A N“ew Method for Estimating Spectral Performance of ADC from INL” IEEE ITC 2010, pp. 1-10, Nov. 2010.

(7) Jingbo Duan, Degang Chen and Randall Geiger, “Sensorless Temperature Measurement Based on ADC Input Noise Measurement,” IEEE NAECON, pp. 208-211, July 2010.

(8) Jingbo Duan, Le Jin and Degang Chen , “Dynamic Performance Estimation Based on INL for ADC BIST,” IEEE ISCAS, pp. 3028-3031, May 2010.

(9) Jingbo Duan, Degang Chen and Randall Geiger, “Phase Control of Triangular Stimulus Generator for ADC BIST,” IEEE ISCAS, pp. 1935-1938, May 2010.

(10) Siva Sudani, M. Wu, D. Chen, “A Novel Robust and Accurate Spectral testing method for Non-coherent sampling” International Test Conference, October 2011.

(11) Siva Sudani, Degang Chen, Randy Geiger, “A 2-FFT Method for on-chip spectral testing without requiring coherency”, International Instrumentation and Measurement Technology Conference, May 2011.

(12) Siva Sudani, M. Wu, D. Chen, "A Novel Robust and Accurate Spectral Testing Method for Non-coherent Sampling", TECHCON 2011.

(13) Xiaoji Ye and Peng Li, "On-the-fly runtime adaptation for efficient execution of parallel multi-algorithm circuit simulation", in Proc. of IEE/ACM Int. Conf. on Computer-Aided Deisgn, Nov 2010.

(14) Xiaoji Ye and Peng Li, "Parallel program performance modeling for runtime optimization of multi-algorithm circuit simulation", in Proc. of ACM/IEE Design Automation conf. pp. 561-566, June 2010.

(15) N.Zhang nd K.K.O, "W-Band Pulsed Radar Receiver in Low Cost CMOS", 2010 Custom Integrated Circuits Conference, pp., Sept 2010, San Jose, CA.
(16) R. Saad, E. Sobhy, and S. Hoyos, “A 384-MHz Continuous-Time Delta-Sigma Modulator Using a Hybrid Feedback DAC Based on Spectral Shaping of Jitter Induced Errors,” SRC TECHCON 2011 Proceedings, Paper/Poster Number: 2.7, to appear September 2011.
(17) R. Saad and S. Hoyos, “Sensitivity Analysis of Pulse-Width Jitter Induced Noise in Continuous-Time ΔΣ Modulators to Blockers,” IEEE International Symposium on Circuits and Systems 2011 (ISCAS 2011).
(18) R. Saad, S. Hoyos, and J. Silva-Martinez, “Hybrid Clock-Jitter Error Shaping Technique for Feedback Digital-to-Analog Converters (DACs) in Continuous-Time Sigma-Delta Modulators,” SRC TECHCON 2010 Proceedings: Technology and Talent for the 21st Century, Paper/Poster Number: 14.3, September 2010.
(19) Y. Zhang, D. Ma, "A 50.3ns Transient-Response CR-Free SIMO Power converter with Adaptive Current compensation", IEEE VLSI Symposium on Circuits, Kyoto, Japan, June 2011, (Accepted).
(20) Y. Zhang, D. Ma, "Integrated SIMO DC-DC Converter with on-line Charge Meter for Adaptive PCCM Operation", IEEE International Symposium on Circuits and Systems (ISCAS), Rio de Janerio, Brazil, May 2011, (Accepted).
(21) Y. Zhang, R. Bondade, D. Ma, S. Abedinpour, "An Integrated SIDO Boost Power converter with Adaptive Freewheel Switching Technique", the 2010 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 3516-3522, Atlanta, GA, Sept 2010.
(22) R. Narasimha, N.R. Shanbhag, and A.C. Singer, "BER-aware adaptive ADC-equalizer receiver for communication links", IEEE Signal Processing Systems, 2010.
(23) S. Weaver, B. Hershberg, and U. Moon, "Digitally synthesized stochastic flash ADC using only standard digital cells," IEEE Symp. VLSI Circuits, Jun. 2011 (Accepted).
(24) O. Rajaee and U. Moon, "A 12-ENOB 6X-OSR noise-shaped pipelined ADC utilizing a 9-bit linear front-end," IEEE Symp. VLSI Circuits, Jun. 2011 (Accepted).
(25) N. Maghari and U. Moon, "A third-order DT delta-sigma modulator using noise-shaped bidirectional single-slope quantizer," IEEE Int. Solid-State Circuits Conf., pp. 474-475, Feb. 2011.
(26) S. Weaver, B. Hershberg, and U. Moon, "ENOB calculation for ADCs with input-correlated quantization error using a sine-wave test," IEEE Int. Conf. Microelec., Dec. 2010.
(27) S. Weaver, B. Hershberg, and U. Moon, "PDF folding for stochastic flash ADCs," IEEE Int. Conf. Elec. Circuits Syst., Dec. 2010.
(28) N. Maghari, S. Weaver, and U. Moon, "A +5dBFS third-order extended dynamic range single-loop delta-sigma modulator," IEEE Custom Int. Circuits Conf., Sep. 2010.
(29) T. Musah and U. Moon, "Pseudo-differential zero-crossing-based circuits with differential error suppression," IEEE Int. Symp. Circuits Syst., pp. 1731-1734, May 2010.

(30) N. Maghari and U. Moon, "Precise area-controlled return-to-zero current steering DAC with reduced sensitivity to clock jitter," IEEE Int. Symp. Circuits Syst., pp. 297-300, May 2010.
(31) N. Maghari and U. Moon, "A double-sampled path-coupled single-loop delta-sigma modulator using noise-shaped integrating quantizer," IEEE Int. Symp. Circuits Syst., pp. 4005-4008, May 2010.
(32) T. Oh and Ramesh Harjani, "A 5GB/s 2x2 MIMO Crosstalk Cancellation Scheme for High-Speed I/Os", IEEE Custom Integrated Circuits conference, Sept 2010.
(33) T. Oh and Ramesh Harjani, "A 10 Gb/s MIMO Channel Equalization and Crosstalk Cancellation Architecture for High-Speed I/Os", TECHCON, Sept 2011 (paper)
(34) O. Garitselov, S.P. Mohanty, and E. Kougianos, "Fast Optimization of Nano-CMOS Mixed-Signal Circuits Through Accurate metamodeling", in Proc. 12th IEEE International Symposium on Quality Electronic Design (ISQED), pp. 615-620, 2011.
(35) O. Garitselov, S.P. Mohanty, E. Kougianos, and P. patra, "Nano-CMOS Mixed-Signal Circuit Metamodeling Techniques: A Comparative Study", in Proc. International Symposium on Electronic System Design, pp. 191-196, 2010.
(36) Liuxi Qian, Dian Zhou, Sheng-Guo Wang, Xuan Zeng, "Worst case analysis of linear analog circuit performance based on Kharitonov's rectangle", 10th IEEE International Conference on Solid-State and Integrated Circuit Tehcnology (ICSICT), Page(s): 800-802, 2010.
(37) D. Shim, D. Koukis, D. Arenas, D.B. Tanner, and K.K.O, "553-GHz Signal Generation in CMOS Using a Quadruple-Push Oscillator", 2011 VLSI Symposium on Circuits, June 2011 (Accepted).
(38) R.G. Pierce, "Broadband modified bowtie aperture antenna", SRC TECHCON, pp. 1-4, Sept. 2010, Austin, TX.
(39) R. Islam, B. Salam, D.B. Schlieter and R. Henderson, "Performance of Planar Transmission Lines for Millimeter-Wave CMOS", SRC TECHON 2010, Sept. 2010, Austin, Texas.
(40) J. silva-Martinez, et.al., "A Blocker Tolerant Broadband Analog-to-Digital converter Architecture", SRC TECHCON Conference, SRC, Sept 2010, Austin, Texas.
(41) A. Perez-Carrillo, S. Taylor,A. Karsilayan and J. Silva-Martinez, "A Large-Signal Blocker robust Transimpedance Amplifier for coexisting Radio Receivers in 45nm CMOS", IEEE RFIC Symposium, 2011, June 2011.
(42) H.M. Geddad, S.S. Taylor, J. Silva-Martinez, "P1dB > 0dBm, NF <3dB, Fully Balanced Low-Noise Transconductance Amplifier in 45nm CMOS" ESSCIRC 2011 (Accepted).
(43) Z. Gao, P. Gui, Ismail Ogzusman, Xiaochen Xu, Max Melson, Rick Jordanger, Karthik Vasanth, "An High Voltage Linear Amplifier for Ultrasound Transmitter", SRC TECHCON, Austin, TX, Sept 2010.
(44) Changdao Dong and Xin Li, “Efficient SRAM failure rate prediction via Gibbs sampling,” IEEE/ACM Design Automation Conference (DAC), 2011.

(45) C. F. Neese, I.R. Medvedev, F. C. De Lucia, G.M. Plummer, C. Ball and A. Frank, "A submillimeter chemical sensor", Proceedings of the OSU International Symposium on Molecular Spectroscopy OSU Columbus, Ohio, p. 158 (2010).
(46) Impact of Back-Gate Biasing on Ultra-thin Silicon-On-Insulator-Based Nanoribbon Sensors P. G. Fernandes, R.A. Chapman, O. Seitz, H.J. Stiegler, H.-C. Wen, Y.J. Chabal, and E.M. Vogel
Proc. IEEE International SOI Conference, (2010).
(47) S. Block, Y. Li, Y. Yang, C. Li, "0.6-2.0 V, All-CMOS Temperature Sensor Front-End using Bulk-Driven Technology", IEEE Dallas Circuits and Systems Workshop, Dallas, TX Nov. 2010.
(48) L. Lu, C. Li, J. Lin, "A regulated 3.1-10.6 GHz Linear Dual-Tuning Differential Ring Oscillator for UWB Applications", IEEE International Symposium on Circuits and systems, Rio de Janerio, Brazil, May 15-18, 2011.
(49) Y. Yang, D.M. Binkley, L. Li, C. Gu, C. Li, "All-CMOS subbandgap Reference Circuit Operating at Low Supply Voltage", IEEE International Symposium on Circuits and Systems, Rio de Janerio, Brazil, May 15-18, 2011.
(50) Amandeep Singh and Peng Li, "On behavorial model equivalence checking for large analog/mixed signal systems", in Proc. Of IEEE/ACM Int. Conf. on Computer-Aided Deisgn, Nov 2010.
(51) Jacob T. White and Leonidas Bleris, "Characterizaton of Nonlinear Feedback using a Synthetic Circuit in Human Cells", 27th Southern Biomedical Engineering conference, 2011, Arlington, TX.
(52) W. Hu, T. Nguyen, Y.-T. Liu and D.Y.C. Lie, "Ultralowpower Analog Front-End circuits and System Design for an Implantable Cardioverter Defibrillator", Proc. The 5th Annual IEEE-NIH Life Science Systems and Application Workshop (LiSSA'11), pp.34-37, NIH Campus, Bethesda, Maryland, April 7-8, 2011.
(53) D.Y.C. Lie, W. Hu and J. Lopez, "Low Power RF Wireless Sensor Design with Highly Efficient SiGe Power Amplifier and Ultralowpower ADC", Proc. Government Microcircuit Applications and Critical Technology Conference (GOMAC), pp.137-140, March 21-24, Orlando, FL, March 2011.
(54) Sangho Youn, Jaeha Kim, Mark Horowitz, "Global Convergence Analysis of Mixed-Signal Systems:, Design Automation Conference, June 2011.
(55) Sangho Youn, Jaeha Kim, Mark Horowitz, "Preventing Global Convergence Failures in Mixed-Signal Systems by Eliminating Indeterminate States", Frontiers in Analog Circuit (FAC) Synthesis and Verification, 2011.
(56) Sahar Ayazian, Eric Soenen and Arjang Hassibi, "A Photovoltaic-Driven and Energy-Autonomous CMOS Implantable Sensor", VLSI Circuits Symposium 2011 (Accepted).

(57) N. Kupp, H. Huang, p. Drineas, Y. Makris, "Cost-Benefit Analysis of Post-Production Performance Calibration in Analog/RF Devices", IEEE Design and Test of Computers (D&T), 2011 (Accepted).

(58) N. Kupp, H. Stratigopoulos, P. Drineas, Y. Makris, "A Case Study in Feature Selection methods for Alternate Test", Proceedings of the SRC TECHCON, Sept. 2011, Austin, TX.

(59) N. Kupp, H. Stratigopoulos, P. Drineas, Y. Makris, "PPM-Accuracy Error Estimates for Low-Cost analog Test: A Case Study", Proceedings of the IEEE International Mixed Signals, Sensors, and Systems Workshop (IMS3TW), 2011 (Accepted).

(60) N. Kupp, M. Slamani, Y. Makris, "Correlating Inline Data with Final Test Outcomes in Analog/RF Devices", Proceedings of the IEEE Design Automation and Test in Europe Conference (DATE), pp. 812-817, 2011.

(61) D. Maliuk, H. Stratigopoulos, H. Huang, Y. Makris, "Analog Neural Network Design for RF Built-In Self-Test", proceedings of the IEEE International Test conference (ITC), pp 23.2.1-23.2.10, 2010.

(62) N. Kupp, H. Huang, P. Drineas, Y., Makris, "Post-Production Performance Calibration in Analog/RF Devices", Proceedings of the IEEE International Test Conference (ITC), pp. 8.3.1-8.3.10, 2010.

(63) D. Maliuk, H. Stratigopoulos, Y. Makris, "An Analog VLSI Implementation of a Multilayer Perceptron and its Application Towards Built-In Self-Test in Analog Circuits", proceedings of the IEEE International On-Line Test Symposium (IOLTS), pp. 71-76, 2010.

(64) Vikram Suresh and Wayne Burleson, "A Hybrid Self-calibration Technique to Mitigate the Effect of Variability in TRNG" CMOS VARI conference, Grenoble, May 2011.

(65) Wayne Burleson, "Physical layer Security and Privacy with Ultra-Wideband" IEEE Symposium on Medical Information and Communication Technology (ISMICT) 2011, Montreux, Switzerland, March 2011. (invited talk).

(66) Sudhir Kudva and Ramesh Harjani, "Inductors Above Digital circuits: Towards Compact On-Chip Switching Regulators", TECHCON, Sept 2010.

(67) Sudhir Kudva and Ramesh Harjani, "Fully Integrated On-Chip DC-DC Converter with a 450x Output Range", IEEE Custom Integrated Circuits Conference, Sept 2010.

(68) Sudhir Kudva and Ramesh Harjani, "A Zero -Area, Zero-Power Supply Resonance Reduction Technique", TECHCON, Sept 2011.

JOURNAL PUBLICATIONS

(1) H.S. Yeom and b. Bakkaloglu, "0V-30V Common Mode Range, 120dB CMRR, and 10nV/√Hz Noise Floor Current Shunt Monitor IC with an Embedded ΣΔ Frequency Modulated Digital Output Interface ADC Block", Journal of Analog Integrated Circuits and Signal Processing (Accepted).

(2) H.S. Yeom and B. Bakkaloglu, "Temperature Compensated, 0V to 26V Common Mode Range, Cu-Trace Based Current shunt monitor with 10nV/√Hz Noise Floor", IEEE Trans. Circuits Syst. II.
(3) Wei Dong and Peng Li, "Parallel circuit simulation with adaptively controlled projective integration", in ACM Trans. On Design Automation of Electronic Systems, 2010 (Accepted).
(4) Xaioji Ye, Wei Dong, Peng Li and Sani Nassif, "Hierarchical multialgorithm parallel circuit simulation", in IEEE Trans. on Computer-Aided Deisgn of Integrated Circuits and Systems, vol. 30, issue 1, pp. 45-58, January 2011.
(5) R. Saad and S. Hoyos, "Sensitivity Analysis of Continuous-Time ΔΣ Modulators to Out-of-Band Blockers in Future SAW-Less Multi-Standard Receivers," Submitted For Publication in IEEE Transactions of Circuits and Systems I: Regular Papers.
(6) R. Saad and S. Hoyos, "Feed-Forward Spectral Shaping Technique for Clock-Jitter Induced Errors in Digital-to-Analog Converters," IET Electronics Letters, vol. 47, no. 3, pp.171-172, February 2011.
(7) R. Saad and S. Hoyos, "Sensitivity of single-bit continuous-time analogue-to-digital converters to out-of-band blockers," IET Electronics Letters, vol. 46, no. 12, pp.826-828, June 2010.
(8) Y. Zhang, R. Bondade, D. Ma, "On-Chip SIMO Power converter Design with Adaptive Cross Regulation and Supply Variation Control for Power-Efficient VLSI Systems", Special Issue on Low Power Design and Verification Techniques, Journal of Low power Electronics (JOLPE), Vol. 7, No. 1, pp. 71-86, Feb 2011.
(9) R. Bondade, D. Ma, "Hardware-Software Co-Design of an Embedded Multiple-Supply Power Management Unit for Multicore SoCs using an Adaptive Global/Local Power Allocation and Processing Scheme", ACM Trans. on Design Automation of Electronic Systems (TODAES) (Accepted).
(10) R. Narasimha and N. R. Shanbhag, "Design of energy-efficient high-speed links via forward error-correction (FEC)", IEEE TCAS-II, May 2010.
(11) T. Musah and U. Moon "Correlated level shifting integrator with reduced sensitivity to amplifier gain," Electron. Lett., vol. 47, no. 2, pp. 91-92, Jan. 29, 2011.
(12) B. Hershberg, S. Weaver, and U. Moon, "Design of a split-CLS pipelined ADC with full signal swing using an accurate but fractional signal swing opamp," IEEE J. Solid-State Circuits, vol. 45, no. 12, pp. 2623-2633, Dec. 2010.
(13) Mahamoud Reza Ahmadi, Amir Amirkhany and Ramesh Harjani, "A 5 Gbps 0.13um CMOS Pilot-Based Clock and Data Recovery Scheme for High-Speed Links", IEEE Journal of Solid State Circuits, August 2010.
(14) T. Oh and Ramesh Harjani, "A 6 Gb/s MIMO Crosstalk Cancellation Scheme for High-Speed I/Os", to appear in IEEE Journal of Solid-State Circuits, CICC special issue, August 2011.

(15) Tracey Y. Zhou, Hang Liu, Dian Zhou, Tuna B. Tarim: "A Fast Analog Circuit Analysis Algorithm for Design Modification and Verification, IEEE Trans. On CAD of Integrated Circuits and Systems 30(2): 308-313.
(16) E.-Y. Seok, D. Shim, C. Mao, R. Han, S. Sankaran, C. Cao, W. Knap, K.K.O, "Paths to Terahertz CMOS Integrated Circuits", IEEE Journal of Solid State Circuits, Vol. 45, No. 8, pp. 1554-1564, August 2010.
(17) Wang, M. Koen, D. Ma, "Low-Noise CMOS TGC Amplifier with Adaptive Gain Control for Ultrasound Imaging Receiver", IEEE Trans. On Circuits and Systems, Part II, (TCAS-II), pp. 26-30, Vol. 58, No. 1, Jan 2011.
(18) F.C. De Lucia, "The Submillimeter: A Spectroscopist's View", J. Mol. Spec. 261, P1 (2010).
(19) I.R. Medvedec. C.F. Neese, G.M. Plummer, and F. C. DeLucia, "Impact of atmospheric clutter on Doppler-limited gas sensors in the submillimeter/terahertz", Applied Optics, 2011 (Accepted).
(20) A. Morshedi and M. Torlak, "Measured Comparison of Dual-Branch Signaling Over Space and Polarization Diversity", IEEE Trans. On Antennas and Propagation, Vol. 59, No. 5, May 2011, pp 1678-1687.
(21) Effect of mobile ions on ultrathin silicon-on-insulator-based sensors
P. G. Fernandes, O. Seitz, R. A. Chapman, H. J. Stiegler, H.-C. Wen, Y. J. Chabal, and E. M. Vogel
Applied Physics Letters, 97, 034103 2010.
(22) Comparison of Methods to Bias Fully Depleted SOI-Based MOSFET Nanoribbon pH Sensors R. A. Chapman, Fellow, P. G. Fernandes, O. Seitz, H. J. Stiegler, H.-C. Wen, Y. J. Chabal, and E. M. Vogel, IEEE Transactions on Electron Devices on 3/15/2011 (Accepted).
(23) Mahmoud Reza Ahmadi, Amir Amirkhany and Ramesh Harjani, "A 5 Gbps 0.13um CMOS Pilot-Based Clock and Data Recovery Scheme for High-Speed Link", IEEE Journal of Solid State Circuits, August 2010.
(24) Sudhir Kudva and Ramesh Harjani, "Fully Integrated On-Chip DC-DC Converter with a 450x output Range", IEEE Journal of Solid-State Circuits, for the CICC August special issue 2011 (Accepted).

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