



# TEXAS ANALOG CENTER OF EXCELLENCE

Annual Report 2015 – 2016



# TxACE MISSION

The Texas Analog Center of Excellence seeks to create fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, health care, and public safety and security.

## TxACE THRUSTS



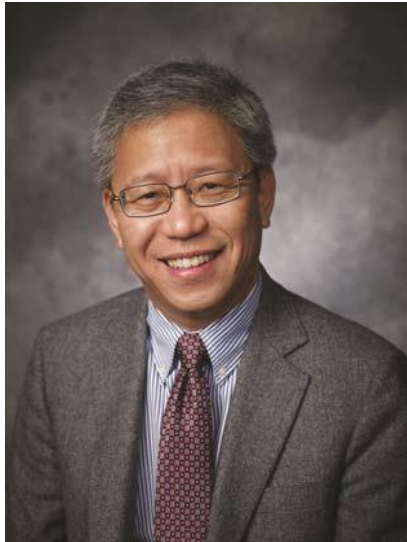
## TxACE 2015-2016 ANNUAL REPORT

The Texas Analog Center of Excellence (TxACE), located at the University of Texas at Dallas is the largest analog research center based in an academic institution. Analog and mixed signal integrated circuits engineering is both a major opportunity and challenge. Analog circuitry is emerging as a critical component of nearly every product of the ~\$350 billion per year integrated circuits industry, as a part of sensing, actuation, communication, power management and others. Digital integrated circuits such as microprocessors, logic circuits and memories are now integrating analog functions such as input/output circuits, phase locked loops, temperature sensors and power management circuits. It is also common to find microcontrollers with multiple analog-to-digital and digital-to-analog converters. These circuitries impact almost all aspect of modern life: safety and security, health care, transportation, energy, entertainment and many others.

Creation of advanced analog and mixed signal circuits and systems depends on the availability of engineering talent for analog research and development. TxACE was established to help translate the opportunity into economic benefits by overcoming the challenge and meeting the need. Support for TxACE has been provided through a collaboration of the state of Texas, Texas Instruments, the Semiconductor Research Corporation, the University of Texas System, and the University of Texas at Dallas.

The research tasks are organized into four research thrust areas: Health Care, Safety and Security, Energy Efficiency and Fundamental Analog. The scope of investigation extends from circuits operating at dc through terahertz, data converters that sample at a few samples/sec to 10's of Giga-samples/sec, ac-to-dc and dc-to-dc converters working at  $\mu\text{W}$  to Watts, energy harvesting circuits, sensors and many more. Significant improvement on existing mixed signal systems and new applications are anticipated. Students who have been exposed to hands-on innovative research are forming the leading edge of analog talent flow into the industry. Close collaboration with and responsiveness to industry needs provide focus to the educational experience.

## DIRECTOR'S MESSAGE



The Texas Analog Center of Excellence (TxACE) is leading analog research and education. Last year, TxACE researchers published 26 journal and 74 conference papers. They also filed one patent disclosure and one patent, and three patents were granted. Twenty-seven Ph.D. and five M.S. students of TxACE have graduated.

The Center funded 55 research tasks led by 41 principal investigators from 19 academic institutions, including two international universities. Five universities (SMU, Rice, Texas A&M, UT Austin, UT Dallas) were from the state of Texas. The Center supported 145 graduate and undergraduate students.

The Center accomplished much. There are too many to list all here. A selected list includes demonstrations of a power- and area-efficient 24GS/s, 6b, 16-way time-

interleaved ADC array with energy efficiency of less than 1mW-sec/GS, rotational spectroscopy using a 208-250 GHz transmitter and a 225-280 GHz receiver fabricated in 65-nm CMOS for detection of Ethanol in breath, a 2.4-GHz RF front-end with noise figure of 6.6dB with power consumption of 194 $\mu$ W, and a 50-GHz wireless impulse receiver for timing synchronization with sub-ps timing accuracy.

The TxACE laboratory is continuing to help advance integrated circuit research by making its instruments available to researchers and our industrial partners all over the world.

Dr. Swaminathan Sankaran and Django Trombley of TI, long time and dedicated industrial liaisons of TxACE research have received the SRC Mahboob Khan Outstanding Liaison Awards. I would like to congratulate them and thank all our liaisons for their dedication and commitment to improving our research.

I would like to thank the students, principal investigators and staff for their efforts, and UT Dallas, the University of Texas System, TI, and SRC, as well as many friends of TxACE all over the world for their generous support. I look forward to another year of working with the TxACE team to make our world better through our research, education and innovation.

**Kenneth K. O., Director TxACE  
Texas Instruments Distinguished  
University Chair Professor  
The University of Texas at Dallas**

## BACKGROUND & VISION

The \$350 billion per year integrated circuits industry is evolving into an analog/digital mixed signal industry. Analog circuits are providing or supporting critical functions such as sensing, actuation, communication, power management and others. These circuits impact almost all aspect of modern life including safety and security, health care, transportation, energy, and entertainment. To lead this change, in particular to lead analog and mixed signal technology education, research, commercialization, manufacturing, and job creation, the Texas Analog Center of Excellence was announced by Texas Governor Rick Perry in October 2008 as a collaboration of the Semiconductor Research Corporation, the state of Texas through its Texas Emerging Technology Fund, Texas Instruments Inc., the University of Texas system and the University of Texas at Dallas. The Center seeks to accomplish the objectives by creating fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, healthcare, and public safety and security as well as by improving the research and educational infrastructure.

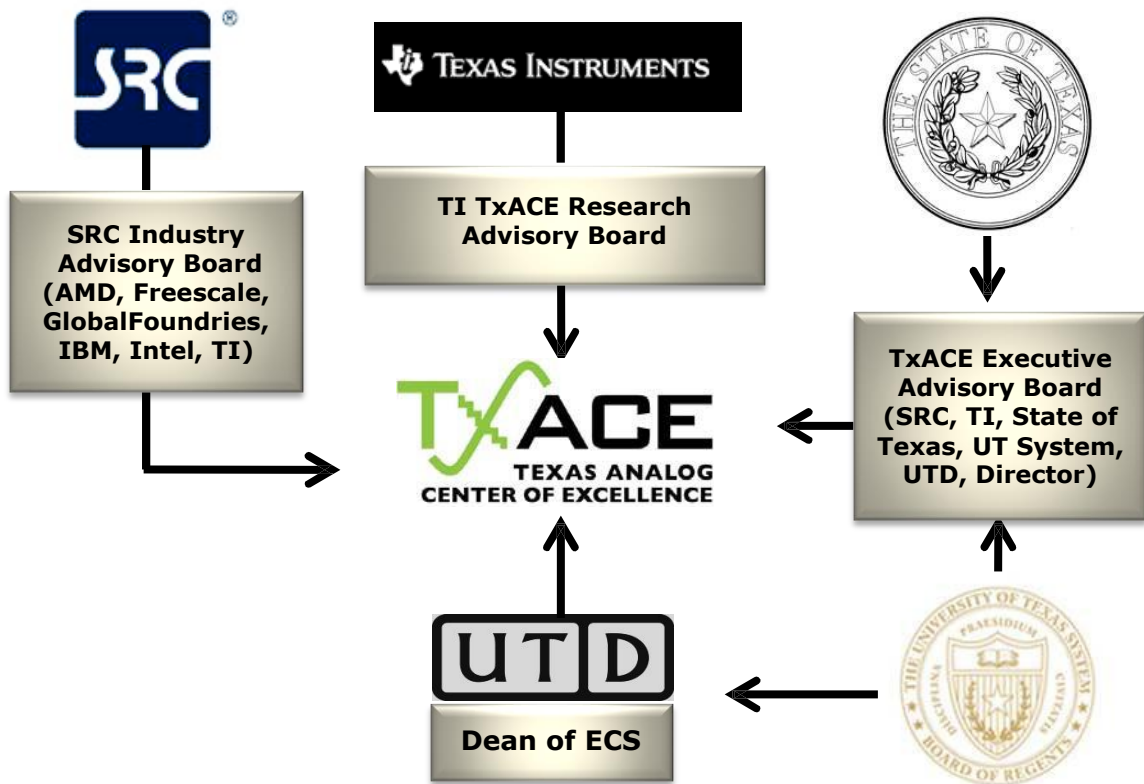


Figure 1: TxACE organization relative to the sponsoring collaboration



**CENTER ORGANIZATION**

The Texas Analog Center of Excellence is guided by agreements established with the Center sponsors. Members of the industrial advisory boards identify the research needs and select research tasks in consultation with the Center leadership. Figure 1 diagrams the relationship of TxACE to the members of the sponsoring collaboration.

*The internal organization of the Center is structured to flexibly perform the research mission while fully embracing the educational missions of the University.*

Figure 2 shows the elements of the organization. The TxACE Director is Professor Kenneth O. The research is arranged into four thrusts that comply with the mission of the Center: Safety and Security, Health Care, Energy Efficiency and Fundamental Analog Research. The fourth thrust consists of vital research that cuts across more than one of the first three research thrusts. The thrust leaders are Prof. Brian A. Floyd of North Carolina State University for safety and security, Prof. Yun Chiu of UT Dallas for health care, and Prof. D. Ma of the UT Dallas for energy efficiency. The thrust leaders form the executive committee. The committee, along with the director, forms the leadership team that works to improve the research productivity of center by increasing collaboration, better leveraging the diverse capabilities of principle investigators of the Center, and lowering research barriers. The leadership team also identifies new research opportunities for consideration by the Industrial Advisory Boards.

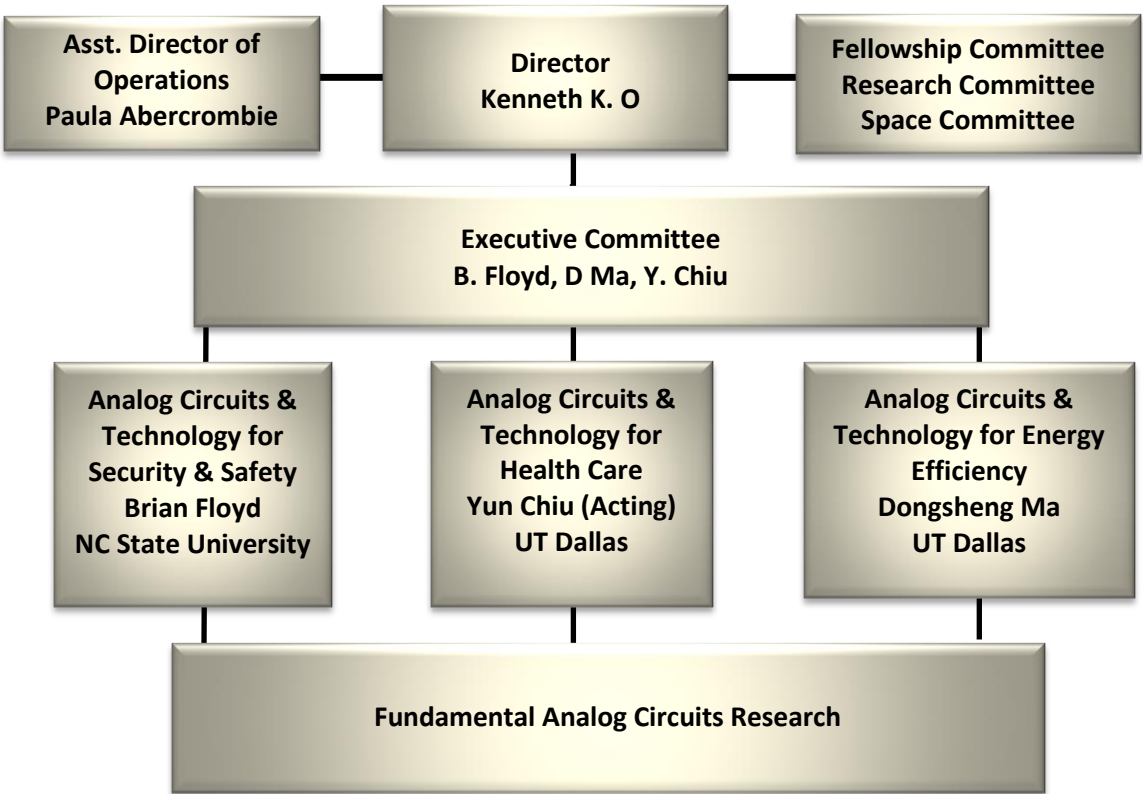


Figure 2: TxACE organization for management of research

(Thrust leader: Brian Floyd, NC State University)

TxACE is developing analog technology that enhances public safety and security. The projects are intended to enable a new generation of devices that can scan for harmful substances by researching 200-300 GHz silicon ICs for use in spectrometers. The thrust is also working to significantly reduce the cost of millimeter wave imaging and on-vehicle radar technology for automotive safety by researching circuit techniques that can improve manufacturing and simplify test and packaging, as well as signal processing techniques that reduce system complexity. Lastly, this thrust is investigating vibration sensors.

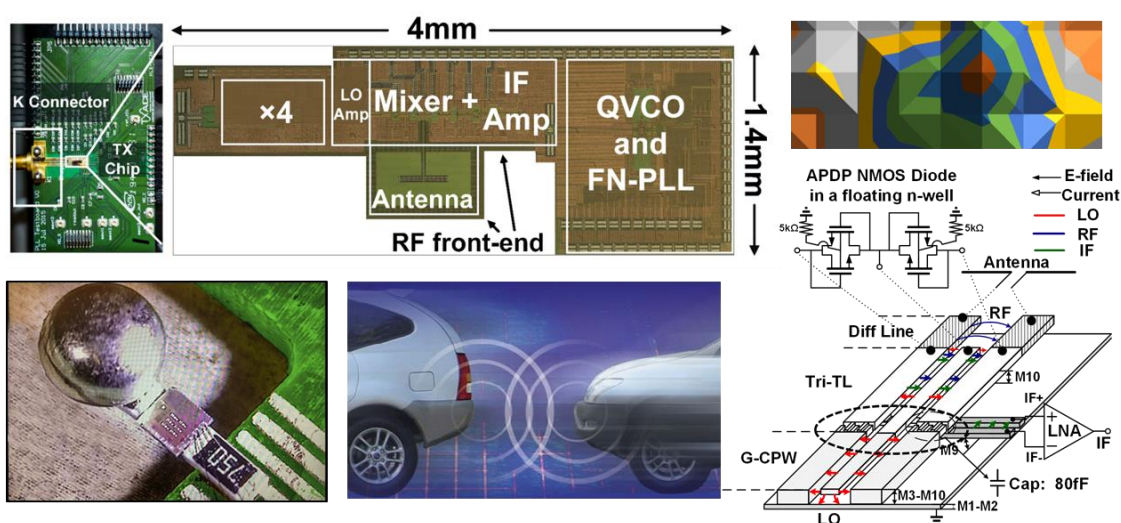


Figure 3: (Top left) 200-260 GHz CMOS transmitter for rotational spectroscopy (K. O, UT Dallas), (Top right) Magnitude of field inside a dielectric waveguide (D. MacFarlane, SMU), (Bottom Left) Vibration sensor compatible with conventional silicon IC and packaging technologies (S. Pourkamali, UT Dallas), (Bottom Right) 200-300 GHz RF front-end of a receiver for rotational spectroscopy (W. Choi, UT Dallas)

## HEALTH CARE

(Thrust leader: Yun Chiu (Acting), University of Texas, Dallas)

Analog and RF integrated circuit technology is the essential interface enabling the power, speed and miniaturization of modern digital microelectronics to be brought to bear on an array of medical issues, including medical imaging, patient monitoring, laboratory analyses, bio-sensing and new therapeutic devices. TxACE is working to identify and support analog circuit research challenges that have the potential to enable important health-related applications. More specifically, TxACE is working to develop an affordable rotational spectrometer that can be used in breath analyses for health monitoring, a CO<sub>2</sub> sensor for both health and industrial applications, and energy efficient radios for wearable wireless body area networks.

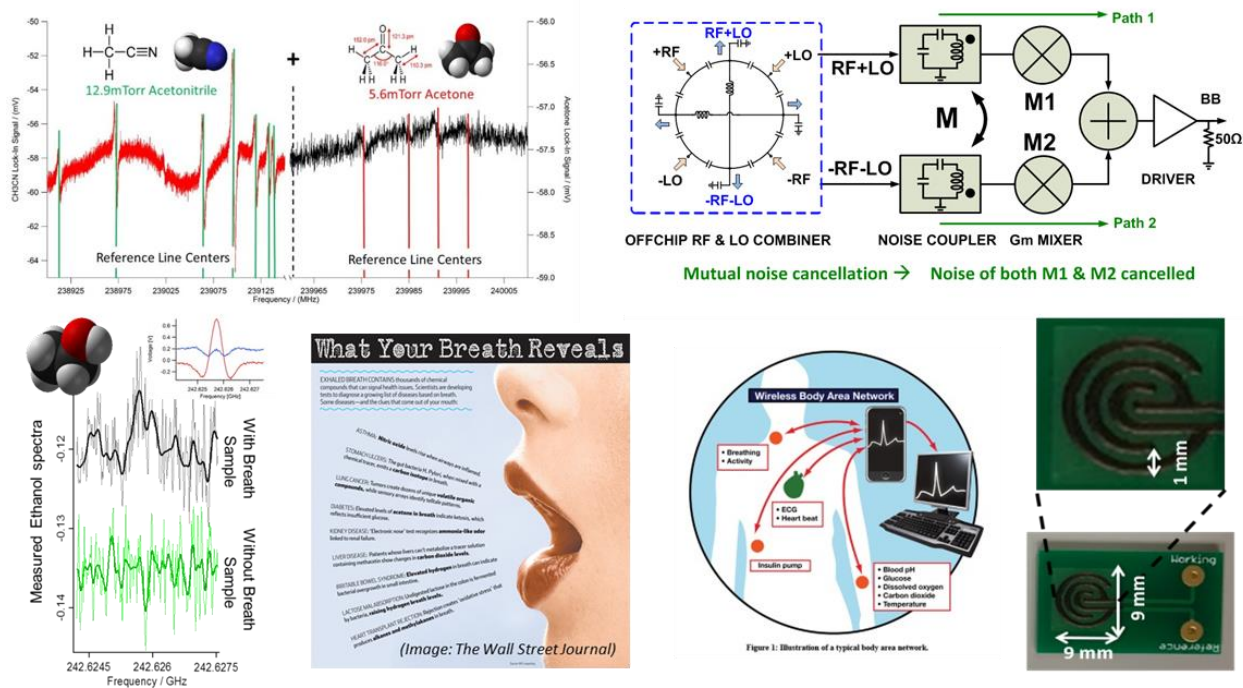
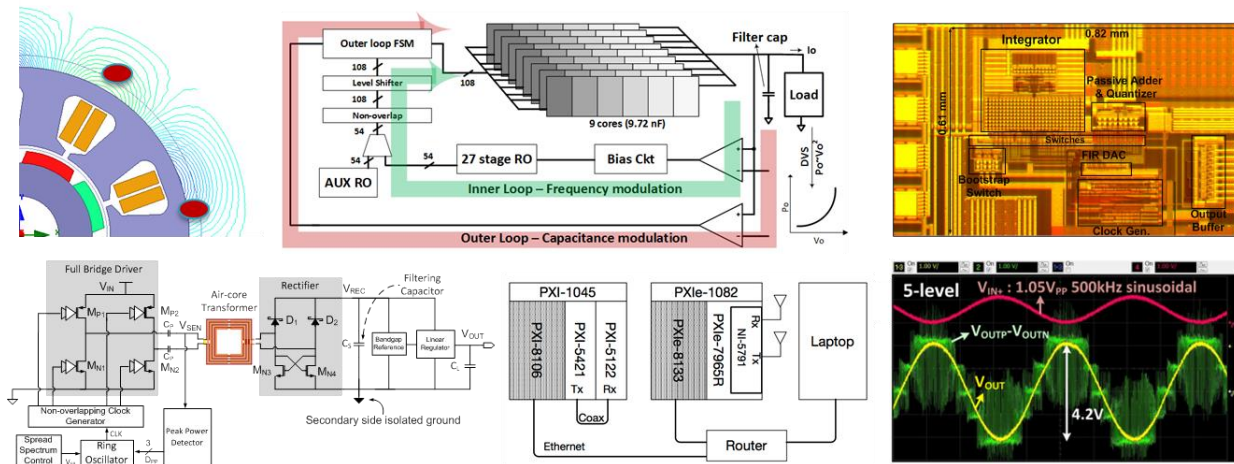


Figure 4: (Left) Breath analyses using a rotational spectrometer (K. O & W. Choi, UT Dallas), (Top right) Receiver for wearable wireless body area networks (R. Harjani, U. of Minnesota), (Bottom right) CO<sub>2</sub> sensor (S. Prasad, UT Dallas)

## ENERGY EFFICIENCY

(Thrust leader: Dongsheng Brian Ma, UT Dallas)

TxACE is committed to alleviate the global energy problem by improving the energy efficiency of electronic systems as well as by developing analog technologies that can make energy generation and distribution more efficient. The Center is also working to energize and power long-lasting in-situ microscale devices such as wireless microsensors, biomedical implants, and portable microelectronics.



**Figure 5: (Top left) Simulated flux leakage in a motor (B. Akin, UT Dallas), (Top center) Programmable DC-DC with custom capacitors (R. Harjani, U. of Minnesota), (Top right) Multi-step incremental ADC (G. Temes, Oregon State University), (Bottom left) Fully integrated Isolated DC-DC converter (B. Bakkaloglu, Arizona State University), (Bottom center) power-line/wireless communication testbed (N. Al-dhahir, UT Dallas, B. Evans, UT Austin), (Bottom right) Measured waveform at the output of the 2/3/5-level PA for power-line communication with 500kHz sinusoidal input (R. Gharpurey, UT, Austin)**

(Thrust leader: TBA)

Research in this thrust focuses on cross-cutting areas in Analog Circuits which impact all of the TxACE application areas (Energy Efficiency, Health Care, Public Safety and Security). The list of research includes design of a wide variety of analog-to-digital converters, communication links, temperature sensors and I/O circuits, development of CAD tools, and testing of integrated circuits.

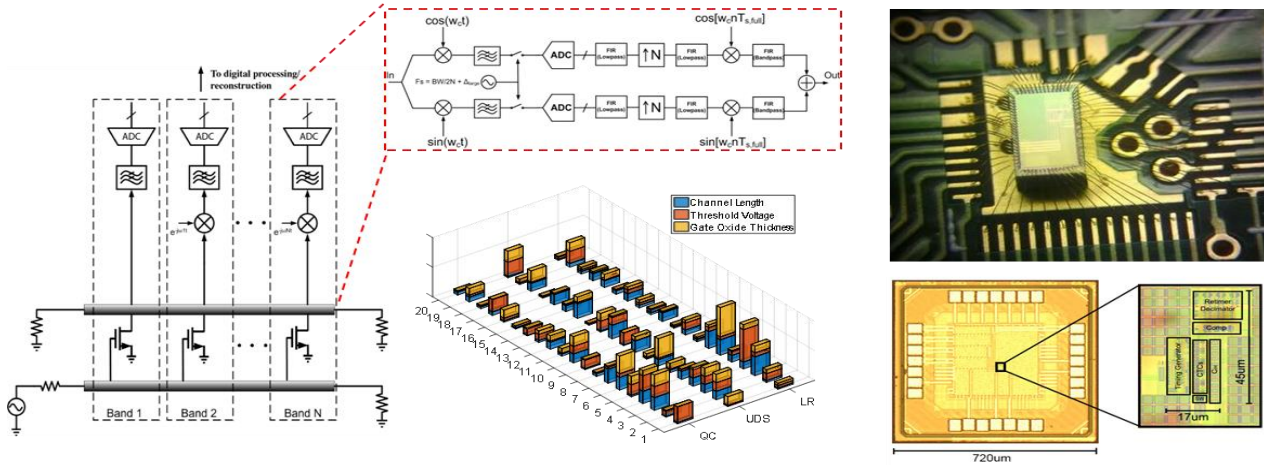


Figure 6: (Left) Conceptual diagram of frequency interleaved-ADC front-end (A. Niknejad, UC Berkeley), (Top right). 25GS/S 6b TI binary search ADC (Y. Chiu, UT Dallas), (Bottom center) Parameter weights of 60 transistor-level variation (i.e. channel length, threshold voltage, gate-oxide thickness) parameters for three performances of the LDO inferred by RVFM (Relevance Feature and Vector Machine) from the training data: quiescent current (QC), undershoot (UDS), LR (load regulation) (P. Li, TAMU), (Bottom right) Die photo of 6bit 1GS/s charge injection cell based ADC (M. Flynn, U. of Michigan)



## TXACE ANALOG RESEARCH FACILITY

The centralized group of laboratories of the Texas Analog Center of Excellence dedicated to analog engineering research and training occupies a ~8000 ft<sup>2</sup> area on the 3rd floor of the Engineering and Computer Science North building (Figure 7). The facility includes RF and THz, Integrated System Design, Embedded Signal Processing, and Analog & Mixed Signal laboratories as well as CAD/Design laboratory structured to promote collaborative research. The unique instrumentation capability includes network analyses and linearity measurements up to 325 GHz, spectrum analysis up to 120 THz, and cryo-measurements down to 2°K. The Center also added a pulsed multiple harmonic load and source pull measurement set up (up to 60 GHz for the third harmonic) and a 325 GHz antenna measurement set up. The close proximity of researchers in an open layout enables natural interaction and compels sharing of knowledge and instrumentation among the students and faculty. The TxACE analog research facility is one of the best equipped electronics laboratories. The laboratory is available for use by TxACE researchers and industrial partners all over the world.

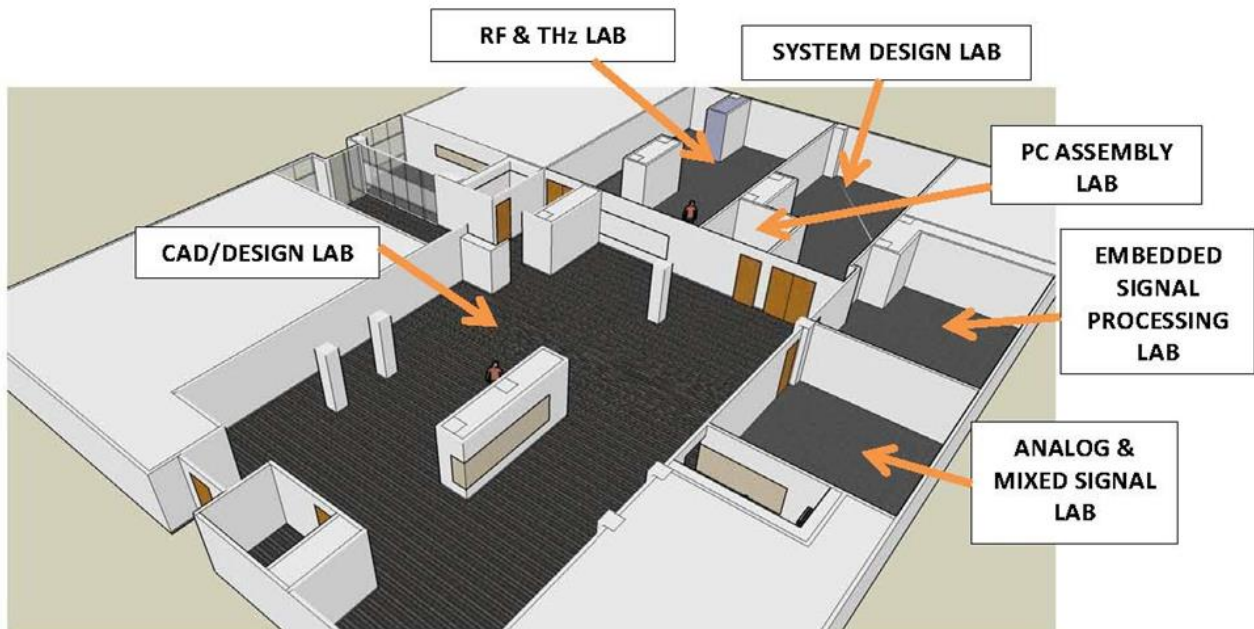


Figure 7: TxACE Analog Research Facility

## RESEARCH PROJECTS AND INVESTIGATORS

The Texas Analog Center of Excellence (TxACE) is the largest university analog technology center in the world. Table 1 lists the current principal investigators of the 55 tasks from 19 academic institutions funded by TxACE. Five universities (Rice, SMU, Texas A&M, UT Austin, UT Dallas) are from the state of Texas. Thirteen are from outside of Texas. Two (Seoul National University, Korea and the University of Cambridge, United Kingdom) (Figure 8) are from outside of the US. Of the 41 investigators, 19 are from Texas. During the past year, the Center supported 125 Ph.D., 15 M.S., and 5 B.S. students. Twenty-seven Ph.D. and five M.S. degrees were awarded to the TxACE students.

Investigator	Institution	Investigator	Institution	Investigator	Institution
N. Al-Dahir	UT Dallas	R. Harjani	U Minnesota	A. Niknejad	UC Berkeley
B. Akin	UT Dallas	R. Henderson	UT Dallas	B. Nikolic	UC Berkeley
A. Babakhani	Rice U	B. Kim	CUNY	K. O	UT Dallas
B. Bakkaloglu	Arizona State	J. Kim	Seoul Nat.	S. Ozev	Arizona State
D. Blaauw	U Michigan	P. Kinget	Columbia	S. Palermo	Texas A&M
D. Chen	Iowa State	H. Lee	UT Dallas	S. Pourkamali	UT Dallas
Y. Chiu	UT Dallas	M. Lee	UT Dallas	S. Prasad	UT Dallas
W. Choi	UT Dallas	P. Li	Texas A&M	A. Raychowdhury	Georgia Tech
F. De Lucia	Ohio State	D. Ma	UT Dallas	E. Rosenbaum	UIUC
M. Flynn	U Michigan	D. MacFarlane	SMU	R. Shi	U Washington
R. Geiger	Iowa State	Y. Makris	UT Dallas	G. Temes	Oregon State
R. Gharpurey	UT Austin	R. McMahon	Cambridge	M. Torlak	UT Dallas
P. Gui	SMU	U.-K. Moon	Oregon State	D. Wentzloff	U Michigan
P. Hanumolu	UIUC	S. Mukhopadhyay	Georgia Tech		

**Table 1: Principal Investigators (September 2015 through August 2016)**

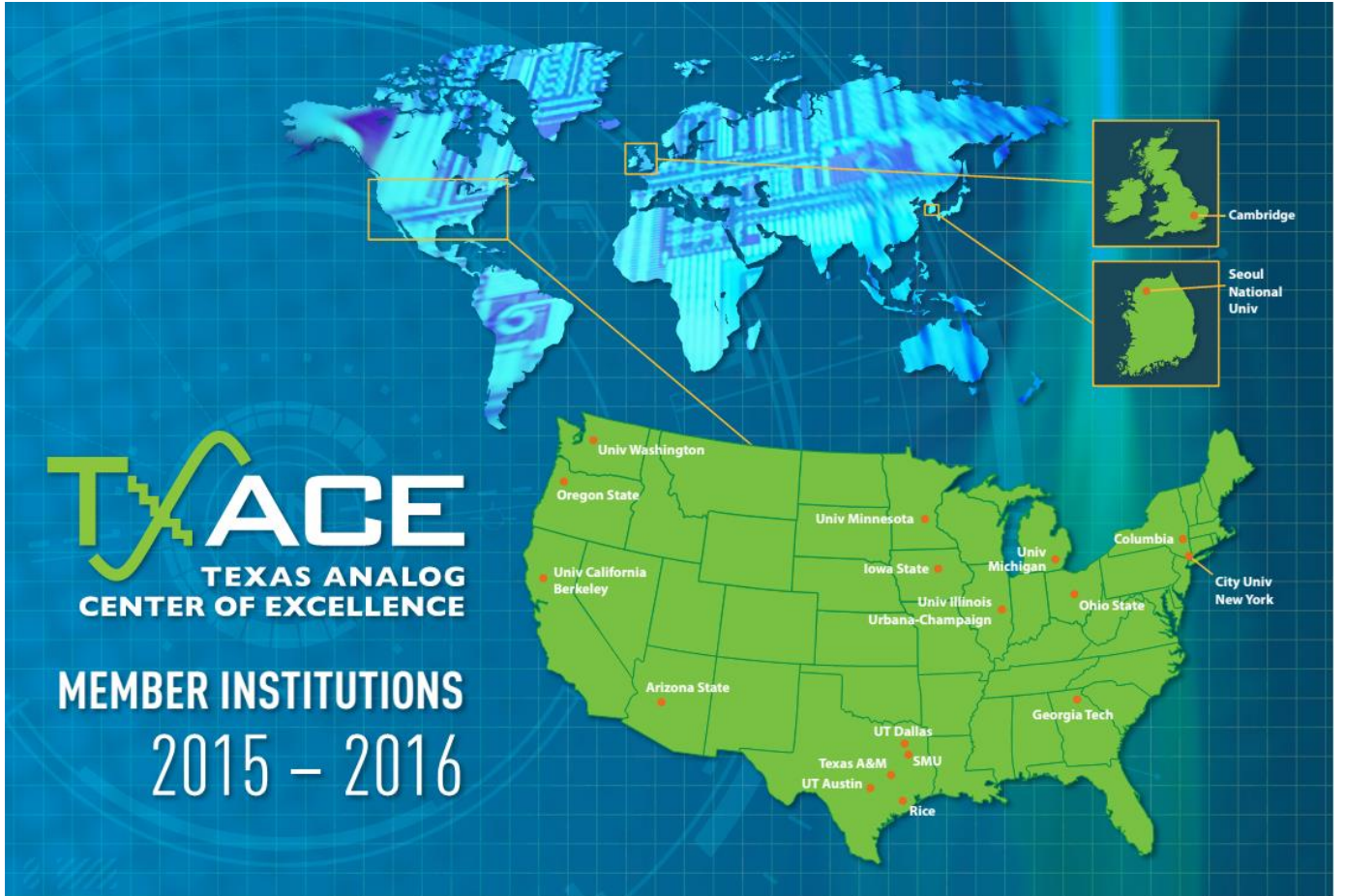


Figure 8: Member institutions of Texas Analog Center of Excellence

## SUMMARY OF RESEARCH PROJECTS

The 55 research projects funded through TxACE during 2015-2016 are listed in Table 2 below by the Semiconductor Research Corporation task identification number.

**Table 2: Funded research projects at TxACE by SRC task identification number (FA: Fundamental Analog, EE: Energy Efficiency, HC: Healthcare, S&S: Safety and Security)**

	Task	Thrust	Title	Task Leader	Institution
1	1836.069	EE	Electronic Systems for Small-scale Wind Turbines	McMahon, Richard	Cambridge
2	1836.081	EE	Combined Inductive/Capacitive DC-DC Converter	Harjani, Ramesh	Univ. of Minnesota
3	1836.087	FA	A High-Speed Low-Power Clock Data Recovery (CDR)	Gui, Ping	SMU
4	1836.095	FA	Test Generation for Mixed-Signal Design Verification and Post-Silicon Debugging	Shi, Richard	Univ. of Washington
5	1836.096	FA	Mixed-Signal Design Centering in Deeply Scaled Technologies	Nikolic, Borivoje	UC Berkeley
6	1836.098	HC	Sub mW Wireless Transceiver Frontends for Body Area Networks	Harjani, Ramesh	Univ. of Minnesota
7	1836.106	EE	IF-Sampling CMOS ADC Front-End with 100-dB Linearity	Chiu, Yun	UT Dallas
8	1836.109	FA	New Paradigms for High-Performance Amplification	Moon, Un-Ku	Oregon State
9	1836.110	EE	Distributed Power Delivery Architecture for 2D and 3D Integrated Circuits	Mukhopadhyay, Saibal	Georgia Tech
10	1836.111	FA	Advanced ADC-Based Serial Link Receiver Architectures	Palermo, Samuel	Texas A&M
11	1836.112	EE	Shortstop: Fast Power Supply Boosting	Blaauw, David	Univ. of Michigan
12	1836.113	FA	Synthesized Cell-Based ADPLL Implementation for Accelerated Design	Wentzloff, David	Univ. of Michigan
13	1836.115	EE	Analysis and Characterization of Switched-Mode DC-DC Power Converters	Li, Peng	Texas A&M
14	1836.116	EE	Efficient PA Architectures for Powerline Communications	Gharpurey, Ranjit	UT Austin
15	1836.117	FA	Performance and Reliability Enhancement of Embedded ADCs with Value-Added BIST	Geiger, Randall	Iowa State
16	1836.118	EE	Low Noise, Low Ripple Fully Integrated Isolated DC-DC Converters for Signal Chain Applications	Bakkaloglu, Bertan	Arizona State
17	1836.119	S&S HC	Demonstration of 180-300 GHz Transmitter for Rotational Spectroscopy	O, Kenneth	UT Dallas

	Task	Thrust	Title	Task Leader	Institution
18	1836.120	S&S HC	Evaluation of Frequency and Noise Performance of CMOS 180 – 300 GHz Spectrometer Transmitter and Receiver Components	Lee, Mark	UT Dallas
19	1836.122	S&S HC	On-Chip Integration Techniques for 180-300 GHz Spectrometers	Henderson, Rashaunda	UT Dallas
20	1836.123	EE	Test Techniques and Fault Modeling for High Voltage Devices and Boards	Kim, Bruce	CUNY
21	1836.124	EE	Study and Analysis of Fast Power-On Clock Multipliers in the Presence of PVT Variations	Hanumolu, Pavan Kumar	UIUC
22	1836.125	FA	10GS/s+ Resolution-Scalable (4-7bits) ADCs	Flynn, Michael	Univ. of Michigan
23	1836.126	S&S HC	Design Spin Reduction via Integrated THz Design: Applications, Physics, and System Engineering	De Lucia, Frank	Ohio State
24	1836.127	FA	Precision Test without Precision Instruments	Chen, Degang	Iowa State
25	1836.128	FA	Statistical Analog Design Property Checking	Li, Peng	Texas A&M
26	1836.129	FA	Study Of Burst-Mode Data Recovery for High Loss Channels	Hanumolu, Pavan Kumar	UIUC
27	1836.130	EE	Built-In Self-Test Techniques for Test, Calibration, and Trimming of Power Management Units: PMU-BIST	Ozev, Sule	Arizona State
28	1836.131	S&S	Process Variation Anatomy: A Statistical Nexus Between Design, Manufacturing and Yield	Makris, Yiorgos	UT Dallas
29	1836.132	FA	Fault Coverage Analysis of Analog/Mixed-Signal Tests Based on Statistical Dissimilarity	Kim, Jaeha	Seoul National Univ.
30	1836.133	EE	Energy-Efficient Signal Processing Techniques for Smart Grid Heterogeneous Communications Networks	Al-Dhahir, Naofal	UT Dallas
31	1836.134	FA	Hybrid Two-Step PLLs for Digital SoCs in Nanoscale CMOS	Kinget, Peter	Columbia
32	1836.135	S&S	Sub-Picosecond Synchronization of Widely Spaced Imaging Arrays	Babakhani, Aydin	Rice Univ.
33	1836.136	FA	Injection-Locked Ring Oscillators for Clock Distribution in Manycore Processors	Nikolic, Borivoje	UC Berkeley
34	1836.137	FA	50GS/s and Beyond Frequency-interleaved Energy-Efficient ADCs	Niknejad, Ali	UC Berkeley
35	1836.138	EE	Micro-Power Analog-to-Digital Data Converters	Temes, Gabor	Oregon State Univ.
36	1836.139	EE	Enabling Fully-Integrated VHF CLK-Sync Multiphase Switching Regulators on Silicon	Ma, Dongsheng	UT Dallas
37	1836.140	EE	Embedded & Adaptive Voltage Regulators with Practive Noise Reduction for Digital Loads Under Wide Dynamic Range	Raychowdhury, Arijit	Georgia Tech
38	1836.141	FA	IC Design for Resilience Against System-Level ESD	Rosenbaum, Elyse	UIUC
39	1836.142	EE	Low Power Applications of FRAM	Blaauw, David	Univ. of Michigan



	Task	Thrust	Title	Task Leader	Institution
40	1836.143	EE	Design Techniques for Modulation-Agile and Energy-Efficient 60+Gb/s Receiver Front-Ends	Palermo, Samuel	Texas A&M
41	1836.144	EE	High-efficiency High-voltage Power Converters	Lee, Hoi	UT Dallas
42	1836.145	FA	RF and Mixed Signal Quantum CMOS Devices and Circuits	Lee, Mark	UT Dallas
43	1836.146	EE	On-Chip AC-DC Power Conversion with Ground Disturbance Shielding for Environmental Sensing Applications	Ma, Dongsheng	UT Dallas
44	1836.147	S&S HC	Demonstration of 180 – 300 GHz Receiver for Rotational Spectroscopy	Choi, Wooyeol	UT Dallas
45	1836.148	FA	50GSPS+ TI Hybrid SAR ADC Array with Comprehensive DDI Calibration	Chiu, Yun	UT Dallas
46	1836.149	EE	Condition Monitoring of PM/IPM Motors through Axial/Radial Leakage Flux	Akin, Bilal	UT Dallas
47	1836.150	S&S	Robust High Resolution Techniques for Millimeter Wave Radars in Complex Environments	Torlak, Murat	UT Dallas
48	1836.152	S&S	Feasibility of CMOS Transmitter and Receiver for 500-Gbps Communication over Dielectric Waveguide	O, Kenneth K.	UT Dallas
49	1836.153	EE	High-Speed Compact Power Supplies For Ultra-Low-Power Wireless Sensor Applications	Ma, Dongsheng	UT Dallas
50	1836.154	EE	State of The Health (SOH) for IGBTs: Incipient Fault Characterization and Degradation Monitoring	Akin, Bilal	UT Dallas
51	1836.155	S&S	Development of Wideband Vibration Sensors	Pourkamali, Siavash	UT Dallas
52	1836.156	S&S	Transition Design for High Data Rate Links at Submillimeter Wave Frequencies	Henderson, Rashaunda	UT Dallas
53	1836.157	EE	CMOS GSPS 12-Bit SAR ADC Array With On-Chip Reference Buffers	Chiu, Yun	UT Dallas
54	1836.158	S&S	Development of Dielectric Waveguides for the Radiation Applications	Macfarlane, Duncan	SMU
55	1836.159	HC S&S	Findings of Sensor Material Evaluation and Preliminary Testing Covering Sensing Elements, Electrolyte Materials and Porous Membrane	Prasad, Shalini	UT Dallas

## ACCOMPLISHMENTS

TxACE has made significant research progress. Table 3 summarizes the number of publications and inventions resulting from the TxACE research during May 2015 to April 2016, while Table 4 lists the major research accomplishments for the Center during the period. The TxACE researchers have published 74 conference papers and 26 journal papers. They have also filed one invention disclosure and one patent. Three patents were granted. The list of publications is included as Appendix I. Following the tabulation, brief summaries of each project are provided.

**Table 3: TxACE number of publications (May 2015 through April 2016)**

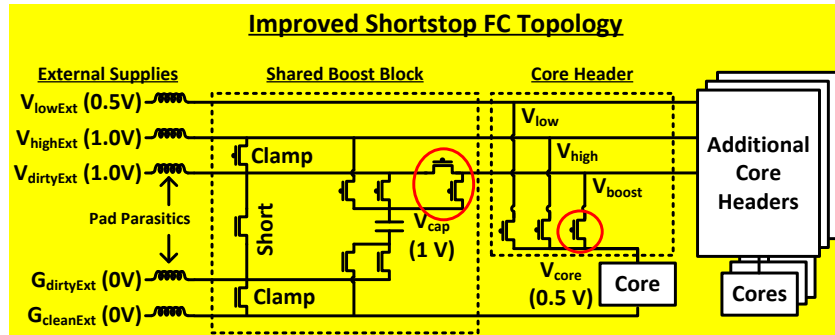
Conference Papers	Journal Papers	Invention Disclosures	Patents Filed	Patents Granted
74	26	1	1	3

**Table 4: Major TxACE Research Accomplishments (May 2015 through April 2016)**

Category	Accomplishment
Fundamental Analog (Test)	A Bayesian learning technique, relevance vector and feature machine (RVFM) for characterizing analog circuits with sparse statistical regression models is proposed. RVFM produces accurate models learned from a moderate amount of data, and computes a probabilistically inferred weighting factor quantifying the criticality of each parameter, hence offering an enabler for variability modeling, failure diagnosis, and test development. (1836.128, PI: P. Li, TAMU)
Fundamental Analog (Circuits)	A charge-injection SAR (or ciSAR), which is based on a charge injection DAC structure is demonstrated. The ADC achieves GHz sampling speed from a single SAR ADC and reduces area by more than half. The prototype in 40-nm CMOS, occupies 0.00058mm <sup>2</sup> and consumes 1.26mW. The measured ENOB is above 5.46b sampled at 1GS/s. The area is 52% of the closest competitor and the Walden FOM is 28.7fJ/conv-step. (1836.125, PI: M. Flynn, U. of Michigan)
Fundamental Analog (Circuits)	A power- and area-efficient 24GS/s, 6b, 16-way time-interleaved ADC array, featuring a voltage-time (v/t) hybrid two-step structure for high-speed and low-power operation, a crosstalk-free SAR DAC topology and a non-hierarchical sampling frontend obviating reference and input buffers, for power and area savings is demonstrated. Fabricated in 28-nm CMOS, the prototype consumes 23mW at 24GS/s and measures an SNDR/SFDR of 35/54dB for a low-frequency input and 29/41dB for a Nyquist input. (1836.148, PI: Y. Chiu, UT Dallas)
Energy Efficiency (Circuits)	Robust operation of fractional-N frequency synthesis using injection locking techniques with rapid on/off operation capability is demonstrated. A prototype fractional-N ILCM (injection locked multiplier) is implemented in 65-nm CMOS and occupies an active area of 0.27mm <sup>2</sup> . The circuit is the first rapid on/off fractional-N clock multiplier to achieve power-on time less than 4ns. It also exhibits the best reported jitter-power FoM by at least 3dB. (1836.124, PI: P. Hanumolu, UIUC)

Category	Accomplishment
Energy Efficiency (Circuits)	A multi-step incremental ADC with multi-slope extended counting is demonstrated. The accuracy is enhanced by reconfiguring it as a multi-slope ADC. Fabricated in 0.18- $\mu\text{m}$ CMOS, the prototype operates at 642 kHz and achieves a peak SNDR = 96.8 dB and DR = 99.7 dB over a 1 kHz bandwidth. The power consumption is 35 $\mu\text{W}$ , which results in an excellent Schreier FoM of 174.6 dB. (1836.138, PI: G. Temes, OSU (Oregon))
Security and Safety Health Care (Circuits)	Low-cost millimeter-wave spectrometers could provide critical capabilities for electronic noses, including breath analysis and detection of harmful molecules. The first ever demonstration of CMOS-based mm-wave spectroscopy is achieved. The 65-nm receiver (1836.147) operates between 225-280 GHz, and includes a down conversion mixer, LO chain, and IF chain. The 65-nm transmitter (1836.119) includes a fractional-N synthesizer, IF amplifiers, and up-conversion mixer, operating between 208-255 GHz. On-chip antennas are used for both transmitter and receiver (1836.122). The chips are demonstrated in a rotational spectroscopy setup (1836.126) to detect Ethanol in human breath (38 ppm). (1836.147, PI: W. Choi, UT Dallas, 1836.122, PI: R. Henderson, UT Dallas, 1836.119, PI: K. O, UT Dallas, 1836.126, PI: F. De Lucia, OSU (Ohio))
Security and Safety (Circuits)	In semiconductor manufacturing, wafer-level testing is a lengthy and expensive procedure particularly for Analog/RF ICs. In this task, an adaptive test cost reduction method has been developed which optimizes the test flow per process signature, allowing a reduction for the test time. This has been demonstrated using industrial datasets for RF transceivers. Up to a 30% test cost reduction has been achieved using the adaptive flow. (1836.131, PI: Y. Makris, UTD)
Security and Safety (Circuits)	Tight synchronization of a distributed array with widely-spaced sparse elements is a key enabler for coherent high-resolution imaging and radar systems. In this task, a 50-GHz wireless impulse receiver with an on-chip antenna has been demonstrated for synchronization with sub-ps timing accuracy. (1836.135, PI: A. Babakhani, Rice)
Health Care (Circuits)	A low-power low-noise 0.7-V mixer-first RF frontend for an IEEE 802.15.6 narrowband receiver which uses frequency translated mutual noise cancellation based on passive coupling is demonstrated in 65-nm CMOS. The figure of merit is 10 dB higher and the power consumption is 194 $\mu\text{W}$ , which is 0.5x lower than the state-of-the-art. The local oscillator power used is -14 dBm. (1836.098, PI: R. Harjani, U. of Minnesota)

# Energy Efficiency Thrust



Category	Accomplishment
Energy Efficiency (Circuits)	Robust operation of fractional-N frequency synthesis using injection locking techniques with rapid on/off operation capability is demonstrated. A prototype fractional-N ILCM (injection locked multiplier) is implemented in 65-nm CMOS and occupies an active area of $0.27\text{mm}^2$ . At 8GHz, it consumes 3.25mW in fractional-N mode and 2.65mW in integer-N mode from a 0.9V supply, of which the DCO and its buffer consume $\sim 2.2\text{mW}$ . The circuit is the first rapid on/off fractional-N clock multiplier to achieve power-on time less than 4ns. It also exhibits the best reported jitter-power FoM by at least 3dB. (1836.124, PI: P. Hanumolu, UIUC)
Energy Efficiency (Circuits)	A multi-step incremental ADC (IADC) with multi-slope extended counting is demonstrated. The accuracy is enhanced by reconfiguring it as a multi-slope ADC in two additional steps. For the same accuracy, the conversion cycle is shortened by a factor of about 29 as compared to the single-step IADC. Fabricated in $0.18\text{-}\mu\text{m}$ CMOS, the prototype operates at 642 kHz and achieves a peak SNDR = 96.8 dB and DR = 99.7 dB over a 1 kHz bandwidth. The power consumption is 35 $\mu\text{W}$ , which results in an excellent Schreier FoM of 174.6 dB. (1836.138, PI: G. Temes, OSU (Oregon))
Energy Efficiency (Circuits)	On-chip supply boosting (Short Stop) is demonstrated in a flip-chip package. Short stop quickly restores a rail from near-threshold to super-threshold when critical code sections are encountered. The implementation uses a transient supply rail and leverages the parasitic and intentional inductance of a package. To address package parasitic variation, an automatic tuning algorithm is incorporated. A $7.9\text{ mm}^2$ , 40-nm CMOS prototype is attached to a custom ball grid array substrate, with integrated in package inductors. Shortstop boosts a $2.7\text{ mm}^2$ core from 0.5 to 0.75V in 4 ns with only 27mV of droop on a shared 0.8V supply rail, marking a 57% faster transition with 67% lower supply noise than a dual supply PMOS header design. (1836.112, PI: D. Blaauw, U. of Michigan)

# TASK 1836.069, ELECTRONIC SYSTEMS FOR SMALL WIND TURBINES

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## SIGNIFICANCE AND OBJECTIVES

This project looks at the electrical system of small-scale wind turbines of power ratings up to 5 kW, particularly micro wind turbines (100 W) deployed in Antarctica, with the aim of reducing the cost of electronics, chiefly by eliminating sensors and replacing them with more advanced control algorithms.

## TECHNICAL APPROACH

The modelling and control of micro-wind turbines for deployment in Antarctica has been performed. First, a model for the generator used in the turbine was validated. Then, wind tunnel measurements were carried out to estimate the tip speed ratio and power coefficient of the turbine. Later on, a simplified sensorless speed estimation algorithm based only on DC side measurements and a Kalman filter for error compensation was tested under different working conditions. Finally, sensorless speed control and active rectification were implemented and compared with other control techniques in terms of system efficiency.

## SUMMARY OF RESULTS

A system level study of micro-wind turbines, looking at their modelling, control and instrumentation was carried out. Two micro-wind turbines were studied in detail: the Ampair 100 and the Rutland 913. Models for the electrical generator and the power coefficient versus tip speed ratio curve were validated with simulations in MATLAB/Simulink and experiments on an emulator test rig. Afterwards, two different sensorless speed estimation techniques were developed and tested by using real wind data from Antarctica and the turbine controller designed by BAS.

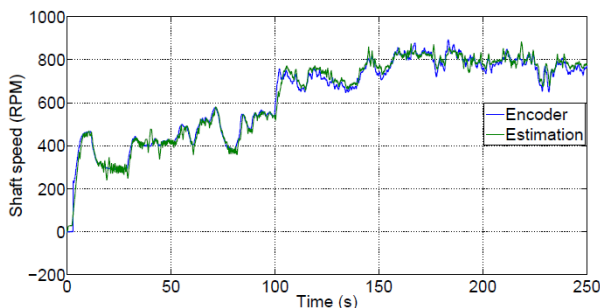


Figure 1: Sensorless speed estimation using only DC measurements- Ampair turbine

The novelty of these sensorless techniques is that only DC side measurements are required. These two

techniques do not depend on the DC to DC converter used in the controller or the rectifier related ripple of the DC measurements. The core algorithm is based on the model of a permanent magnet generator connected to a passive diode rectifier. This arrangement is indeed one of the most commonly used configuration in micro and small-scale wind turbines up to 5 kW.

A comparison of the system efficiency of different control techniques developed for micro wind turbines was also reported. Fig 2 shows the power coefficient measurements at different wind speeds. The grey bars represent the maximum power coefficient measured in the wind tunnel without any controller, just by changing the turbine operation point with a variable resistor. The bars in red correspond to the BAS controller's performance. The blue bars are the power coefficient of the turbine directly connected to a lead acid battery. Finally, the green bars correspond to the power coefficient using sensorless control and active rectification. This technique has the highest power coefficient over the range of wind speeds.

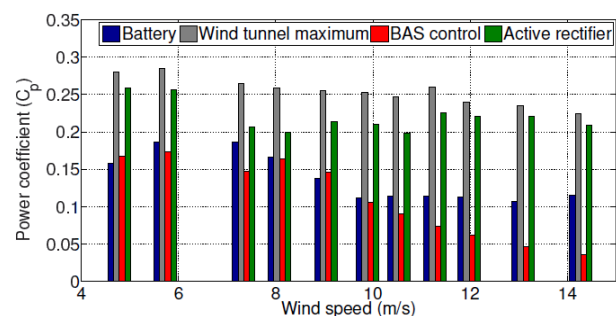


Figure 2: Efficiency comparison

**Keywords:** micro wind turbines, sensorless control, power coefficient, speed estimation, wind tunnel

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

- [1] D Llano, R. McMahon, "Torque observer and extended H infinity filter for sensorless control of permanent magnet generators tested on a wind turbine emulator," 2015 IECON, November, 2015, Yokohama, Japan.
- [2] D Llano, R. McMahon, "Modelling and control of micro-wind turbines for deployment in Antarctica," 2016 PEMD, April, 2016, Glasgow, UK.



# TASK 1836.081, COMBINED INDUCTIVE/CAPACITIVE DC-DC CONVERTER

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## SIGNIFICANCE AND OBJECTIVES

This project focuses on the design of fully integrated combined inductive/capacitive converter. Inductive converters are used for higher loads and capacitive converters are used for lighter loads. The current focus during this year is on the design of programmable and high power density, high-efficiency capacitive converters using custom made composite capacitors.

## TECHNICAL APPROACH

We fabricated a fully programmable switched capacitor DC-DC converter architecture shown in Fig. 1, which supports five step down ( $k:1$ ) voltage ratios ( $k=1, 1.33, 1.5, 2, 3$ ) for a 3000X range of load currents. This architecture mimics a “digital standard cell” approach and is made to be easily scalable with different loads. We propose the use of both capacitive modulation and frequency modulation for load regulation. We introduced [1] custom designed, low leakage, high density composite capacitors as the bucket-capacitors. It is a parallel combination of MIM, MOM (Met1-Met6) and accumulation mode MOS-cap contributing 20%, 20% and 60% of the total capacitance, respectively.

## SUMMARY OF RESULTS

Fig.1 shows the overall architecture of the converter. Capacitive modulation is realized by the asynchronous digital FSM based (marked in red in Fig. 1) system while frequency modulation is a VCO based analog-PID implementation (marked in green). Capacitive modulation implements coarse voltage regulation by turning off/on the switching capacitors. Fig. 2 (bottom) shows the leakage comparison for an inversion mode, source/drain connected accumulation mode and source/drain floating i.e. AFJ (Accumulation Floating Junction as shown in Fig.2 (top)) MOSCAP. We see a 40X leakage current reduction by the proposed Accumulation-Floating Junction AFJ-MOSCAP .

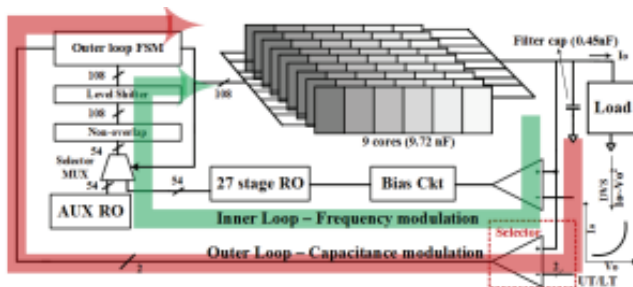


Figure 1: Overall architecture of the programmable DC-DC converter with dual-loop load regulation designed in 65nm

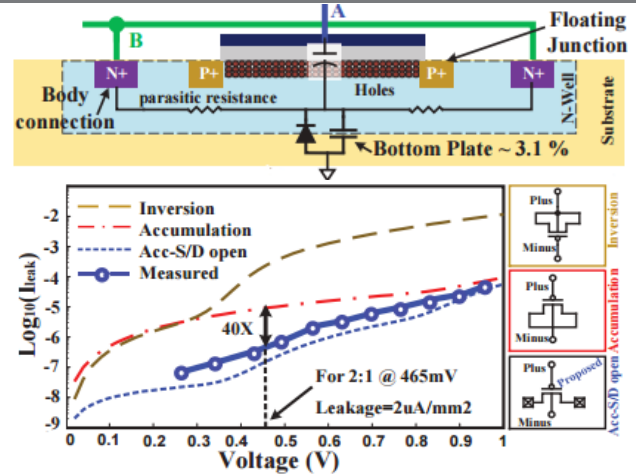


Figure 2: (Top) Structure of AFJ-MOSCAP, (Bottom) Leakage

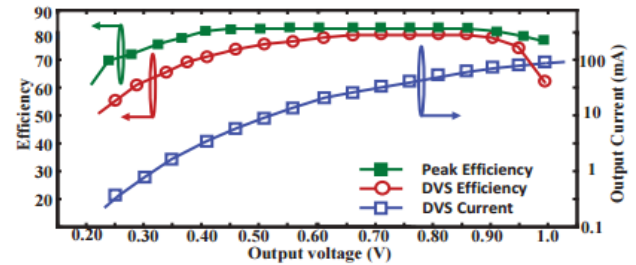


Figure 3: The Efficiency and output load current versus output voltage for a DVS load and efficiency at peak currents

Fig. 3 summarizes the peak efficiencies, DVS load efficiencies and DVS current-voltage relationship. The peak efficiency is 82.1% for output voltage 0.86V at a load current of 143mA. Dual control loop while maintaining zero dark silicon for all five-voltage modes results in a  $1.05 \text{ W/mm}^2$  density with a maximum 54-phase interleaving and reduced output filter capacitor. Programmable time-interleaving boosts the power density and reduces the output voltage ripple.

**Keywords:** combined, DC-DC, converter, inductive / capacitive

## INDUSTRY INTERACTIONS

Texas Instruments and Freescale, IBM, Intel

## MAJOR PAPERS/PATENTS

[1] R. Harjani, S. Chaubey, R. Jain (Intel), “Capacitive DC-DC Converter Design” Tutorial at IEEE International Symposium on Circuits and Systems, Lisbon, 2015.

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# TASK 1836.106, IF-SAMPLING CMOS ADC FRONT-END WITH 100-DB LINEARITY

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## SIGNIFICANCE AND OBJECTIVES

IF-sampling demands stringent tracking bandwidth and linearity performance of analog-to-digital converters, which dictates high supply voltages and bipolar devices to implement the front-end circuitry. We present a calibration technique to linearize the CMOS sample-and-hold circuits for IF-sampling applications that can potentially achieve a spurious-free dynamic range of over 100 dB.

## TECHNICAL APPROACH

A compact derivative-based error model is developed to address the dynamic nonlinearity in CMOS S/H circuits, which is mainly attributed to the nonlinear on-resistance of the MOS transistors. An analog high-pass filter derivative-estimation technique is further proposed to obtain direct derivative information (DDI) of the analog input. The S/H error model is also further simplified due to the availability of DDI with reduced digital computing load.

## SUMMARY OF RESULTS

In order to verify the derivative Sample/Hold (S/H) dynamic error model and the analog high-pass filter (HPF) derivative estimation technique proposed in the previous report, a prototype chip is designated and implemented using GLOBALFOUNDRIES 65nm CMOS LPE process (GF65).

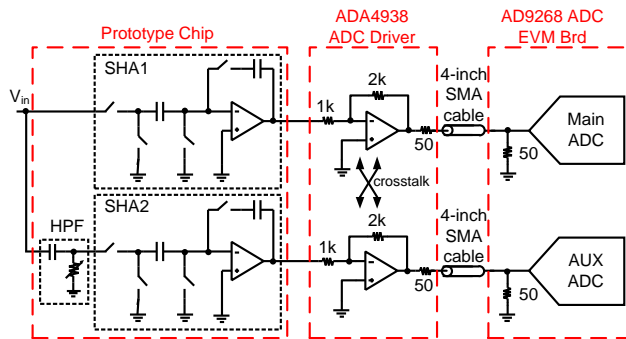


Figure 1: Chip block diagram and testing setup

As shown in the Fig.1, the proposed chip prototype consists of two signal paths, which are the main signal path (SHA1) and the HPF derivative estimation path (SHA2). Both signal paths contain a sample/hold amplifier, which feeds the output voltage to two off-chip commercial quantizers, respectively.

The die photo of the prototype chip implemented in GLOBALFOUNDRIES 65nm CMOS process is shown in

Fig. 2. The total chip area is 1mm<sup>2</sup> with 0.167mm<sup>2</sup> core active area.

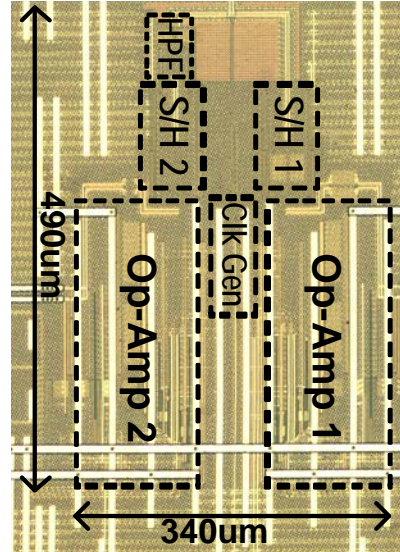


Figure 2: The die photo

Fig. 3 plots the measured SFDR of the test chip vs.  $f_{in}$  and the measured and simulated  $HD_3$  vs. the HPF resistance (i.e., the corner frequency). The SFDR of the S/H is improved up to 40 dB for input frequencies up to 500 MHz.

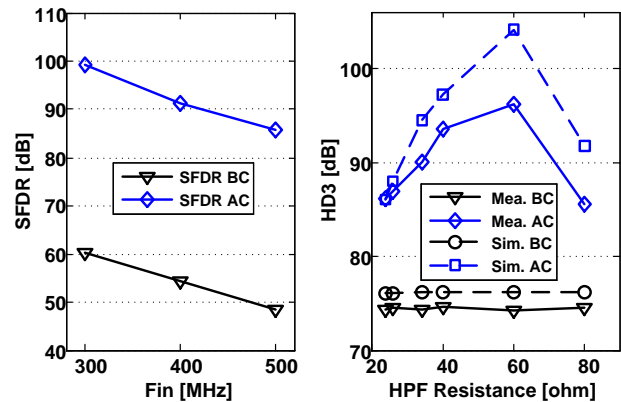


Figure 3: Measured SFDR vs.  $f_{in}$  (Left) and  $HD_3$  (400MHz input) vs. HPF Resistance (Right)

**Keywords:** IF-sampling, digital calibration, S/H circuit, dynamic nonlinearity, direct derivative information

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

# TASK 1836.110, DISTRIBUTED POWER DELIVERY ARCHITECTURE FOR 2D AND 3D INTEGRATED CIRCUITS

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## SIGNIFICANCE AND OBJECTIVES

The primary objective is to design a low-loss, fully integrated, and robust distributed Power Delivery Unit for multicore processors targeting low output voltage from relatively high input voltage. The central innovation is a hybrid down conversion architecture composed of a central switched capacitor (SC) converter and multiple distributed inductive buck (IB) converters.

## TECHNICAL APPROACH

The key technical approaches include design of the hybrid converter stage connecting a switched capacitor back-end and an inductive buck front-end. The key effort of last year focused on optimizing the design of buck stage. A single-inductor-multiple-output based buck stage was designed and integrated (off-chip) with the SC stage. We have also designed a two-phase buck stage. Finally, a very high-frequency buck stage as well as resistive assist based transient management circuits with full-digital control was designed.

## SUMMARY OF RESULTS

**Single-Inductor-Multiple-Output (SIMO):** We have presented a SIMO module that enables smaller passives for a given output power. First, Continuous Conduction Mode (CCM) operation is utilized to deliver higher output power for a smaller inductance; and the cross-regulation in CCM operation is suppressed using a novel power-weighted CCM controller. Second, a modified power stage filter is presented using floating capacitors that utilizes Miller effect to reduce switching frequency of the output while maintaining power quality. The design is demonstrated through a 130nm CMOS test-chip that generates 4 outputs. The measurements demonstrate a 20MHz operation the pulse-width-modulation (PWM) signal of the power stage with 500nH inductor and 1 $\mu$ F total load capacitance while delivering an output power density of 150mW/ $\mu$ H- $\mu$ F. The test-chip demonstrates DVS speed of 120mV/ $\mu$ s, 73% peak efficiency at a load of 40mA, and as high as 40% efficiency improvement using the modified power filer. The SIMO module has been used as the front-end buck stage for the hybrid regulator.

**High-frequency Buck Regulator:** We have designed a bond-wire inductance and on-die capacitance based high-frequency Integrated Voltage Regulator (IVR) with a multi-sampled digital controller. We have also presented a resistive transient assist (RTA) circuit that utilizes multisampling and bypasses the control loop to provide

charges to the output directly from input, thereby improving load and reference transients. An all-digital DCM mode and FET segment control are also included to improve low load efficiency. A 130nm CMOS test-chip demonstrates a 125MHz IVR with a 250MHz compensator. The RTA circuit shows up to 2.5x enhancement of transient settling time. A peak efficiency of 71% is measured.

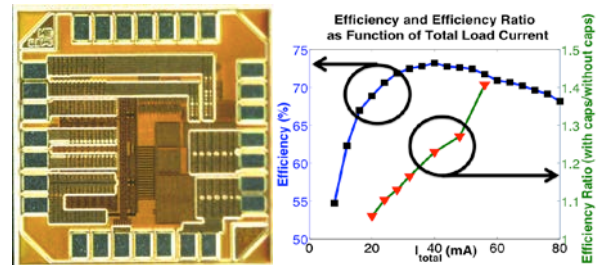


Figure 1: The measurement results for the SIMO

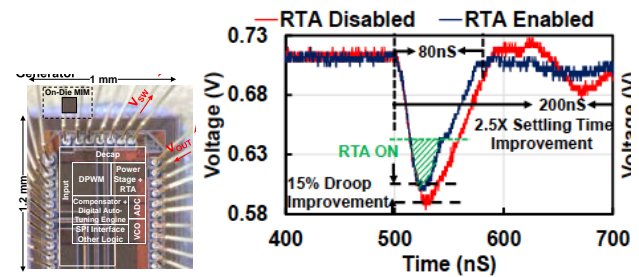


Figure 2: The measurement results of high-frequency IVR

**Keywords:** integrated converters, hybrid conversion, efficiency, high conversion ratio, packaging

## INDUSTRY INTERACTIONS

Intel, IBM, Texas Instruments

## MAJOR PAPERS/PATENTS

- [1] M. Kar, et. al, "A Scalable Hybrid Regulator For Down Conversion of High Input Voltage Using Low Voltage Devices," *IEEE Transaction on Power Electronics*.
- [2] S. Carlo, et. al, "A High Power Density, Dynamic Voltage Scaling Compatible, Single-Inductor Four-Output Regulator using a Power-Weighted CCM Controller and a Floating Capacitor-Based Output Filter," *IEEE Transactions on Power Electronics (TPE)*.
- [3] M. Kar, et. al. "An Integrated Inductive VR with a 250MHz All-Digital Multisampled Compensator and on-Chip Auto-Tuning of Coefficients in 130nm CMOS." *IEEE European Solid State Circuit Conference (ESSCIRC)*, 2016.

# TASK 1836.112, SHORTSTOP: FAST POWER SUPPLY BOOSTING

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DENNIS SYLVESTER, UNIVERSITY OF MICHIGAN

## SIGNIFICANCE AND OBJECTIVES

On-chip supply boosting can quickly restore a microprocessor core's power rail from near-threshold to super-threshold when critical code sections are encountered. We demonstrate a flip-chip implementation of the Shortstop supply boosting technique. To address package parasitic variation, an automatic tuning algorithm is included in the approach.

## TECHNICAL APPROACH

In [1] a wirebonded implementation was demonstrated for Shortstop, but modern high-performance microprocessors are packaged in flip-chip technologies. This work expands upon previous Shortstop work by: (1) demonstrating Shortstop in a custom BGA flip-chip package and showing how in-package inductors can reduce boost latency; (2) introducing a new on-chip self-tuning algorithm that addresses package parasitic variations; and (3) a new architecture and physical design strategy.

## SUMMARY OF RESULTS

The proposed Shortstop architecture was implemented in TSMC 40nm CMOS. Fig. 1 shows a die shot and photo of the test chip attached to the BGA package in a test socket. A custom flip-chip BGA package was used to connect the flip-chip die to a PCB for testing, through a BGA socket. The custom package includes four transient supply rail connections, one with a straight metal trace and three looped metal traces to add inductance of various sizes (0.5nH, 1nH, and 2nH). Inductance was extracted using Ansys HFSS modeling of the package substrate dielectric and copper traces.

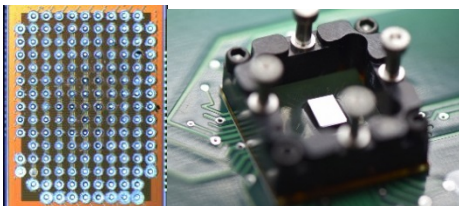


Figure 1: Die photo (left) and packaged die (right)

Fig. 2 shows measured on-chip waveforms of core virtual rail and high voltage rails for Shortstop and baselines. The baseline configurations connect core supply directly to high voltage rail without first connecting to a boost virtual supply rail. In one baseline we current starve the PMOS high voltage header. Shortstop boosts the core from 0.5V to 0.8V (with  $-50\text{mV}$  allowable droop) in 14.2ns, versus 20.6 – 32.4ns in the baseline. Even with

current starving, the baselines exhibit 82–120mV of droop on high supply, while Shortstop suffers just 27mV of droop.

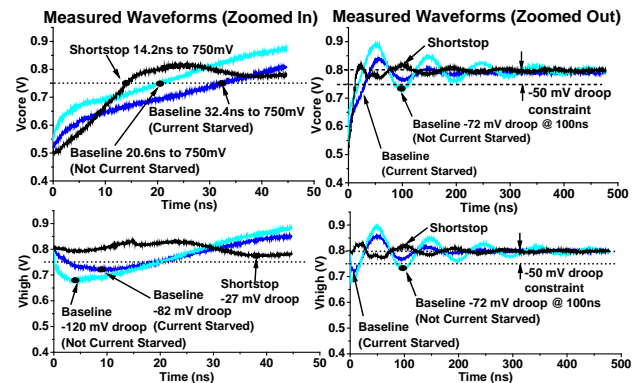


Figure 2: Measured on-chip waveforms of proposed Shortstop flip-chip architecture versus baseline of a dual-rail PMOS header-based baseline architecture

Shortstop boost time and droop was measured versus core size with an in-package inductor of 2nH, when boosting from 0.5V to 0.75V. Compared to the baseline, Shortstop reduces boost time by 36% to 56% for a  $2.5\text{mm}^2$  core while not exceeding 31mV of  $V_{\text{high}}$  droop (82–120mV of droop for the baseline). The smallest core size tested,  $0.64\text{mm}^2$ , has a boost time of 7.8ns, while the largest core of  $2.7\text{mm}^2$  boosts in 14.2ns.

In summary, the Shortstop core supply rail boosting technique is demonstrated in a custom flip-chip package. The design improves upon prior work [1] through a new proposed architecture, a distributed and modular physical design approach applicable to flip-chip microprocessors, and an automatic tuning FSM. Shortstop in flip-chip improves upon a dual-rail PMOS header-based technique with 57% faster transition time and 67% lower supply noise.

**Keywords:** power supply boosting, timing generation, near-threshold computing, dark silicon, dim silicon

## INDUSTRY INTERACTIONS

IBM, Intel

## MAJOR PAPERS/PATENTS

[1] N. Pinckney et al., "Shortstop: An On-Chip Fast Supply Boosting Technique," *VLSI*, 2013.

[2] N. Pinckney, D. Sylvester, and D. Blaauw, "Supply Boosting for High-Performance Processors in Flip-Chip Packages," to appear *ESSCIRC*, 2016.



# TASK 1836.115, ANALYSIS AND CHARACTERIZATION OF SWITCHED-MODE DC-DC POWER CONVERTERS

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## SIGNIFICANCE AND OBJECTIVES

Robust and efficient envelope-following methods are desirable for fast time-domain analysis of converters with various modulation schemes. Furthermore, existing small-signal models are often based on averaged DC behaviors, hence unable to capture frequency responses that are faster than the switching frequency. We develop a more complete multi-harmonic AC model for PWM converters.

## TECHNICAL APPROACH

We have developed a unifying envelope-following method (EF) based upon a numerically robust time-delayed phase condition and several fast simulation techniques including dynamic initial solution prediction, automatic node selection for convergence check, and adaptive envelope stepsize selection [2].

In addition to the time-domain modeling [1, 3], we have also worked on small-signal AC modeling of PWM converters, by developing a multi-harmonic model that provides a complete small-signal characterization of both DC averages and high-order harmonic responses.

## SUMMARY OF RESULTS

Our envelope-following (EF) technique can be broadly applied to PWM, PFM, and PSM (pulse skipping modulation) converters, achieving up to 30X runtime speedups over the transient analysis. Fig. 1 shows a PSM converter, and Fig. 2 shows the simulation of the converter using the proposed EF algorithm.

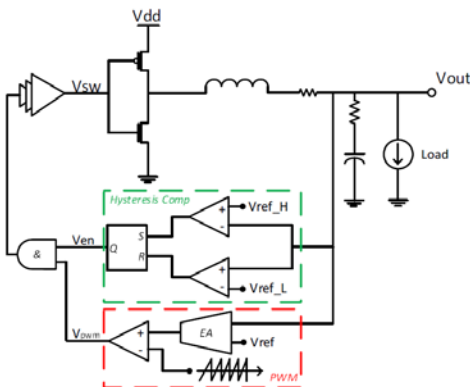


Figure 1: A pulse skipping modulated (PSM) converter

Our PWM AC model captures important high-frequency overshoots and undershoots of the converter response, which are otherwise completely missed by the existing

techniques, offering important guidance for converter design and closed-loop control.

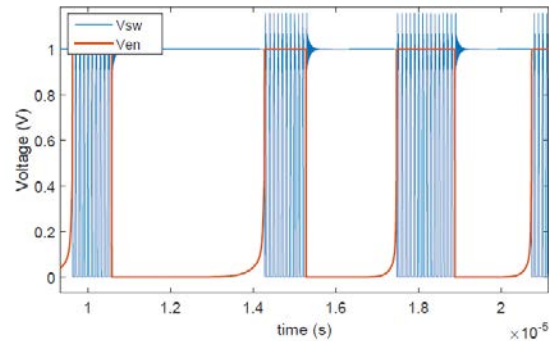


Figure 2: Envelope-following simulation of the PSM converter

Fig. 3 shows that index-0 component of the proposed AC model captures spikes around the switching frequency, which are missed by the conventional small-signal model.

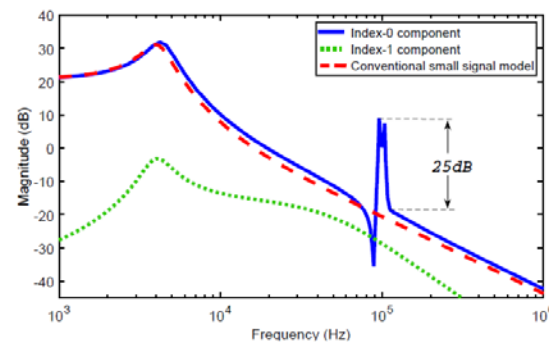


Figure 3: AC responses of a boost converter

**Keywords:** PWM, PFM, PSM, DC-DC converters

## INDUSTRY INTERACTIONS

Texas Instruments, Freescale

## MAJOR PAPERS/PATENTS

[1] Y. Wang et al., "Multi-harmonic nonlinear modeling of low-power PWM DC-DC converters operating in CCM and DCM," IEEE/ACM DATE, Mar. 2016.

[2] Y. Wang et al., "Robust and Efficient Transistor-level Envelope-Following Analysis of PWM/PFM/PSM DC-DC Converters," IEEE TCAD, 2016 (in press).

[3] D. Tannir et al., "Accurate modeling of nonideal low power PWM DC-DC converters operating in CCM and DCM using enhanced circuit averaging techniques," ACM TODAS, 2016 (in press).



# TASK 1836.116, EFFICIENT PA ARCHITECTURES FOR POWERLINE COMMUNICATIONS

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## SIGNIFICANCE AND OBJECTIVES

Using power lines for communications is highly attractive for several end applications, since in principle, this communication medium allows for cost-effective reuse of existing infrastructure. This research addresses the design of power-efficient transmitters for powerline communication systems that support data rates up to several hundreds of kbps.

## TECHNICAL APPROACH

A PWM-based design with a Class-D output stage is employed in the transmitter implementation. Critical performance considerations including efficiency, linearity, and spurious emissions are addressed as part of the design. To support the signal bandwidths, the switching frequency required of the PWM generator can be of the order of several tens of MHz. A PLL-based PWM generator that avoids the requirement for a ramp and high-speed analog comparator is thus employed in the architecture. Multi-level (2/3/5-level) PWM is proposed, which helps to enhance efficiency at peak as well as back-off power, by reducing switching loss.

## SUMMARY OF RESULTS

The transmitter architecture is aligned with standards defined by CENELEC, FCC and ARIB, and targets a signal bandwidth of up to 500 kHz. THD has to be better than 60 dBc, in order to satisfy electromagnetic compatibility. The design must accommodate a time-varying load. Efficiency performance must be maintained over a wide amplitude range, which is achieved by using a switching output stage.

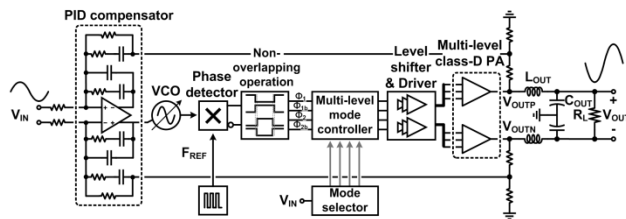


Figure 1: PLL-PWM architecture

A PLL-PWM architecture has been designed in a 130 nm CMOS process for the PLC system (Fig. 1). PWM is generated by comparing the local average of the output of a phase-detector in a PLL to an externally applied analog signal [1]. By replacing amplitude-comparison with phase-domain comparison, the architecture allows

for high-speed PWM generation, without the requirement for a linear ramp signal or high-speed, accurate comparators. In addition, multi-level (2/3/5-level) PWM is employed. In 3- and 5-level PWM operation, the output voltage range is divided into multiple sub-ranges. This reduces the switching voltage levels, which reduces dynamic loss, and improves peak power efficiency, as well as back-off efficiency.

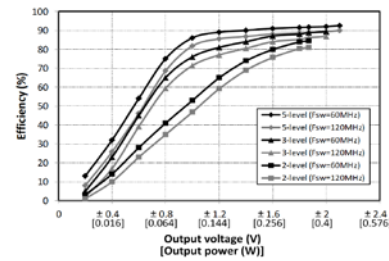


Figure 2: Measured PA efficiency for  $R_L=10 \Omega$

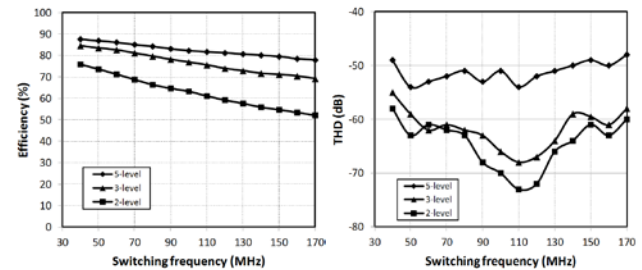


Figure 3: Measured waveforms with sinusoidal input

For 2/3/5-level PA operation, with a 500 kHz sinusoidal input (PAPR = 3dB) and 60 MHz switching frequency, the measured THD is -61/-62/-53 dB and corresponding efficiency is 71/83/86% with 175/200/220 mW output power level, respectively. The efficiency decreases when the switching frequency is increased, since the switching loss is larger, especially for the 2-level PA.

**Keywords:** PWM, powerline transmitters, switching mode PAs, class-D PA, power line communications

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] J. Lu et al., "A CMOS class-D line driver employing a phase-locked loop based PWM generator," IEEE Journal of Solid State Circuits, vol. 49, pp. 729–739, March 2014.

# TASK 1836.118, LOW NOISE, LOW RIPPLE FULLY INTEGRATED DC-DC CONVERTERS FOR SIGNAL CHAIN APPLICATIONS

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 SAYFE KIAEI, ARIZONA STATE UNIVERSITY

## SIGNIFICANCE AND OBJECTIVES

Fully integrated isolated DC-DC converters are an essential component in power monitoring, biomedical, and motor control applications where ground isolation is required. Compare to bulky discrete transformers, fully integrated transformer based approaches have advantage over reliability, weight, size and noise performance and are more suitable for high precision mixed signal applications.

## TECHNICAL APPROACH

In this project, isolated converters that can be integrated with mixed signal building blocks, such as current monitors, ADCs and telecommunication modules will be developed. A fully integrated dc-dc converter is made possible by integrating the low noise power converter with an on-chip coreless transformer. Mature IC processing techniques produce high quality insulation layers, and integrated dc-dc converters typically have superior isolation rating and higher reliability than those with discrete transformers. We will also utilize closed loop calibration techniques that can track the peak power transfer frequency of the integrated transformer, overcoming the impact of process variation on efficiency and noise of the system.

## SUMMARY OF RESULTS

The fully integrated isolated DC-DC converter architecture is represented in Figure 1. An H-bridge driver is utilized to drive a transformer to transfer power across a ground isolation boundary. To ensure power transfer efficiency, an H-bridge driving frequency control unit is included. At secondary side, in order to make rectifiers act fast enough for >100 MHz signal, passive type rectifiers should be used. An LDO is also utilized to regulate the output to high precision. To characterize on-chip EMI noise distribution, noise sensing cells are utilized.

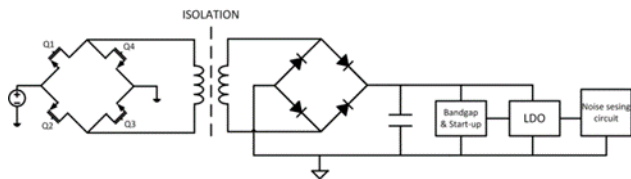


Figure 1: Power transfer block diagram

A coreless on-chip transformer is a key part of our DC-DC converter. To optimize its design, a 3-D model is created

in ANSYS HFSS, a patterned ground shields technique is also added for decoupling transformer from the lossy silicon substrate. On-chip transformer is characterized by a network analyzer, and the measurement results are shown in table 1,

Parameter	$L_p$	$L_s$	$Q_p$	$Q_s$	$k$
Measurement	23.1nH	46.7nH	3.9	3.6	0.46
Simulation	24.5nH	63.0nH	3.53	4.0	0.62
$\Delta$	1.4nH	16.3nH	0.37	0.4	0.16

Table1: Transformer parameters

The proposed fully integrated isolated DC-DC converter is designed and fabricated in an 180nm CMOS technology with a 5V compliant transistor option. The converter core occupies 5.2mm<sup>2</sup>. The converter supplies 0 to 25mA output current at 2V regulated output,  $V_{OUT}$  with input voltage ranging from 3V to 5V. The measured received power of the converter for different driving frequencies is shown in Fig. 2. In the average, the peak power transfer occurs at 111MHz which is the resonant frequency of the primary side. The transferred power at 100MHz is 60% lower than the peak value, making the peak power search an effective approach to increase overall converter efficiency.

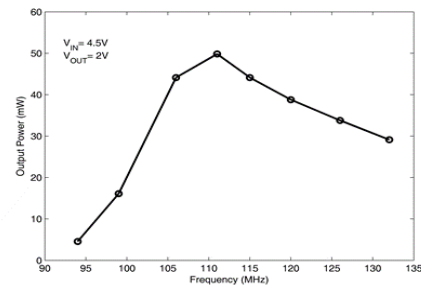


Figure 2: Efficiency vs driving frequency

The on-chip EMI noise distribution is obtained by measuring EMI noise power at the output of EMI sensors located at the transformer secondary side. Measurements show that three locations close to the rectifier region has 2-3dB higher noise compared to other locations.

**Keywords:** EMI, DC-DC, transformer, isolate

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

# TASK 1836.123, TEST TECHNIQUES AND FAULT MODELING FOR HIGH VOLTAGE DEVICES AND BOARDS

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## SIGNIFICANCE AND OBJECTIVES

Our project objectives are 1) develop physics-based fault models for LDMOS transistors, 2) develop parasitic device models, 3) modify ATE load boards for high voltage discharge problems, and 4) provide novel low-cost test techniques for high voltage LDMOS devices.

## TECHNICAL APPROACH

Lateral DMOS transistors are used in various applications. We have identified a new crystal lattice defects in LDMOS transistors. Using positive and negative gate bias voltages, we were able to identify p and n region defects of LDMOS. We worked on computing a multiplication factor (M) to identify defects easily. We continued to enhance our HVPro software tool to test DIB automation and reduce high-voltage testing to protect personnel.

## SUMMARY OF RESULTS

A hardware test measurement apparatus was built to implement a noise reduction scheme [1]. During this reporting period, we have identified several techniques to test LDMOS transistor drivers and summarized them [2]. In Figure 1, two sets of measurements of LDMOS devices are illustrated. The first group is devices with high breakdown voltage (>850V) which has smaller threshold voltage ( $V_T$ ) and larger on-resistance. Both of these characters correspond to high doping concentration of p and n regions in LDMOS. The second group is devices with lower breakdown voltage (~810V) which has comparatively larger  $V_T$  and smaller on-resistance.

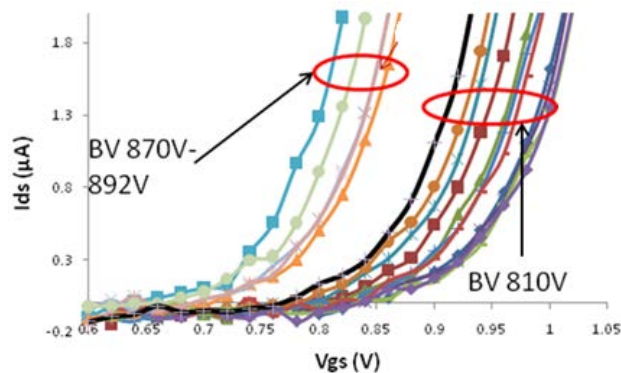


Figure 1: LDMOS Threshold voltage with the breakdown voltage

We have developed other testing methods to reduce the high Avalanche voltage using waveform stimulus and

temperature variations. Fig. 2 shows the total LDMOS test algorithms. The threshold voltage and the on-resistance are measured simultaneously to decide on the relative doping concentration of the p and n regions, respectively. The threshold voltage ( $V_T$ ) is a strong function of the p region doping concentration. As the last step, the junction capacitance is measured to separate the good and the bad parts. The junction capacitance depends on the depletion width created from the applied drain voltage as expressed in equation  $C = \frac{\epsilon_{Si}}{W}$ , where C is the junction capacitance and W is the depletion width. As the maximum electric field is related to the depletion width and hence is the applied drain voltage. The bad parts tend to have a larger slope in the capacitance vs. drain voltage graph. The maximum operating test voltage is 400V. We concluded that the slope of the capacitance vs. drain source voltage plot can be used to identify faulty parts.

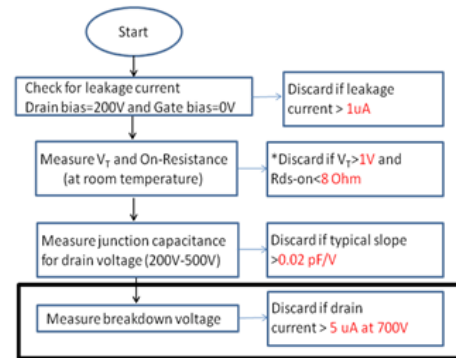


Figure 2: LDMOS Test Technique Flow Chart

**Keywords:** LDMOS, structural defects, avalanche voltage, fault model, high voltage

## INDUSTRY INTERACTIONS

Texas Instruments, GlobalFoundries

## MAJOR PAPERS/PATENTS

[1] Patent: US 8,742,777 B2, "Method and System for testing an Electric Circuit," awarded on June 3, 2014.

[2] S. Mondal, J. Gamboa, B. Kim, "Development of TSV-based Inductors in Power Electronics Packaging," IEEE International Conference on Electronic Packaging Technology, pp. 622-626, Changsha China, August 2015.

# TASK 1836.124, INJECTION-LOCKED FRACTIONAL-N CLOCK MULTIPLIERS

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## SIGNIFICANCE AND OBJECTIVES

The first fractional-N injection-locked clock multiplier that achieves the lowest power and jitter and hence the best figure-of-merit among all the reported fractional-N synthesizers is demonstrated.

## TECHNICAL APPROACH

The key idea behind the proposed fractional-N ILCM can be best understood by considering the case of multiplication factor of 4.25 ( $N=4$ ,  $\alpha=0.25$ ) and the oscillator is initially set to oscillate at  $4.25F_{REF}$ . Noting that the oscillator accumulates an additional delay of  $0.25T_{OSC}$  every reference cycle, phase error between reference clock and oscillator output can be made zero by adding the same amount of phase shift to the reference clock as well. To this end, as depicted in Fig. 1, a digitally controlled delay line (DCDL) is introduced in the injection path and its delay control word DCW is chosen such that added delay is equal to  $T_{OSC}$ ,  $0.75T_{OSC}$ ,  $0.5T_{OSC}$ ,  $0.25T_{OSC}$  in 4 consecutive ( $k+1$ , through  $k+4$ ) reference clock cycles. Note that adding a delay of  $T_{OSC}$  in the  $k+5^{th}$  reference cycle results in having 5 oscillator cycles in between  $k+4^{th}$  and  $k+5^{th}$  injection intervals. This behavior is analogous to cycle swallowing present in classical multi-modulus divider-based fractional-N synthesis and it obviates the need for infinite phase shifting capability of the DCDL. Under this condition, injection signal occurs ideally at the zero crossing of oscillator output, which enables it to pull the oscillator toward phase lock, thus realizing a fractional-N ILCM. In practice, to ensure this gain of the DCDL must be calibrated as described in [1].

## SUMMARY OF RESULTS

A prototype fractional-N ILCM is implemented in a 65nm CMOS technology (see Fig. 2) and occupies an active area of  $0.27\text{mm}^2$ . At 8GHz, it consumes 3.25mW in fractional-N mode and 2.65mW in integer-N mode from a 0.9V supply, of which the DCO and its buffer consume less than 2.2mW. The performance of the ILCM is characterized using an external 125MHz reference clock that has about  $190\text{fs}_{rms}$  integrated jitter from 10kHz to 30MHz. Figure 4 shows the measured phase noise plots at 8GHz output frequency. In integer-N mode, integrated jitter is about  $104\text{fs}_{rms}$ . In fractional-N mode, the in-band phase noise is better than  $-107\text{dBc/Hz}$  at 100kHz offset frequency. The integrated jitter is about  $203\text{fs}_{rms}$  and  $240\text{fs}_{rms}$  when the fractional spur is out-of-band and in-band, respectively. The proposed ILCM achieves the best

power efficiency of  $0.44\text{mW/GHz}$  and the first reported fractional-N clock multiplier with rapid on/off capability. It also achieves the best-reported FoM of  $-255\text{dB}$  (integer-N) and  $-247\text{dB}$  (fractional-N).

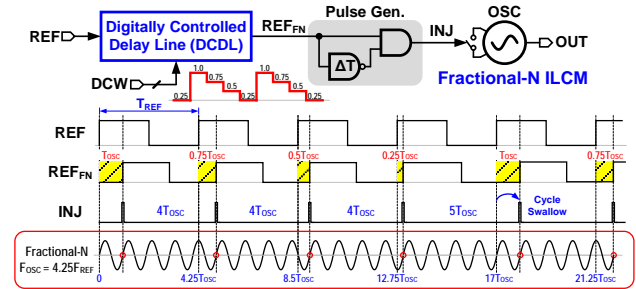


Figure 1: Block diagram of fractional-N injection locked clock multiplier

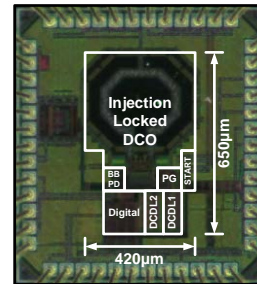


Figure 2: Die photo of prototype fractional-N ILCM

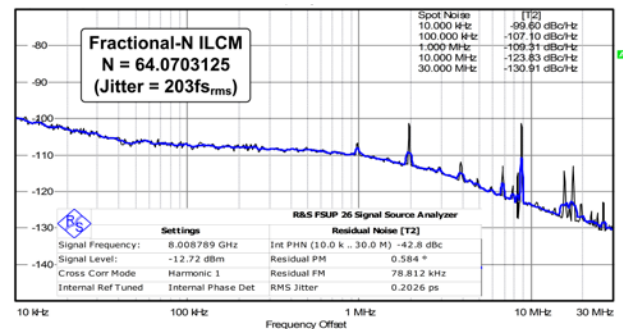


Figure 3: Measured phase noise plot

**Keywords:** fractional-N frequency synthesis, low power

## INDUSTRY INTERACTIONS

Texas Instruments, Intel

## MAJOR PAPERS/PATENTS

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# TASK 1836.130, BUILT-IN SELF-TEST TECHNIQUES FOR TEST, CALIBRATION, AND TRIMMING OF POWER MANAGEMENT UNITS: PMU-BIST

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## SIGNIFICANCE AND OBJECTIVES

This project aims at development of small-footprint adjustable zoom-ADCs and small footprint dynamic measurement circuits for the characterization of loop behavior of LDOs.

## TECHNICAL APPROACH

For the DC measurement approach, we rely on a VCO based converter. A VCO converts a DC signal to frequency. Conversion is typically non-linear but within a certain range, linearity can be achieved. The linear range of voltage-to-frequency conversion needs to be carefully adjusted. The slope of voltage-to-frequency conversion determines the sensitivity. For the dynamic characterization, we need to keep the LDO in a loop to ensure proper operating point. The technique entails applying a small disturbance signal at one point in the loop and observing the response at a different location. The small disturbance will be in the form of a pseudo random signal and the result is accumulated over a longer period to enhance accuracy.

## SUMMARY OF RESULTS

The zoom-in ADC was designed and taped out at TI India. The ADC is being tested during an internship in May 2016. Figure 1 shows the preliminary results from the zoom-in ADC. The INL of the ADC is below the target 1mV for window sizes below 100mV. This would indicate a 2-step conversion for the ADC. The overall measurement time is 20ms per DC measurement and 100ms total for the target range of voltages.

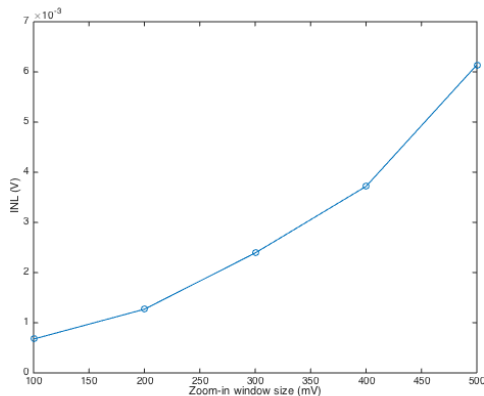


Figure 1: Measurement results for the zoom-ADC: INL versus window size

The dynamic BIST circuit is still under development. Table 1 shows the simulation results for the dynamic BIST with various random (PRBS) patterns of 8148-bit duration each. From these results, we can see that the estimation accuracy for the phase margin is well within the acceptable range and it increases if the results are averaged over various patterns.

PM (°)	Proposed	Baseline	Error
PRBS1	57.4	56.2	1.2
PRBS2	54.9	56.2	1.3
PRBS3	57.0	56.2	0.8
PRBS4	57.6	56.2	1.4
Avg.	56.7	56.2	0.5

Table 1: Simulation results for phase margin (PM) estimation using BIST with different PRBS patterns

**Keywords:** LDO, DC-DC converter, BGR, self-test

## INDUSTRY INTERACTIONS

TI, Freescale

## MAJOR PAPERS/PATENTS

- [1] Navankur Beohar, Priyanka Bakliwal, Sidhanto Roy, Debashis Mandal, Bertan Bakkaloglu, Sule Ozev, "Disturbance-free BIST for Loop Characterization of DC-DC Buck Converters", IEEE VLSI Test Symposium, 2015. (Received for best paper honorable mention award)
- [2] Osman Emir Erol, Sule Ozev, Chandra Suresh, Rubin Parekhji, and Lakshmanan Balasubramanian. "On-chip measurement of bandgap reference voltage using a small form factor VCO based zoom-in ADC." IEEE Design, Automation & Test in Europe Conference, pp. 1559-1562, 2015.
- [3] Liu, Tao, Chao Fu, Sule Ozev, and Bertan Bakkaloglu. "A built-in self-test technique for load inductance and lossless current sensing of DC-DC converters." IEEE VLSI Test Symposium (VTS), 2014. (Received best paper award)



# TASK 1836.133, ENERGY EFFICIENT SIGNAL PROCESSING TECHNIQUES FOR SMART GRID HETEROGENEOUS COMMUNICATION NETWORKS

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## SIGNIFICANCE AND OBJECTIVES

Smart Grids are supported by heterogeneous networks that employ both wireless and powerline communication (PLC) technologies since no single solution fits all scenarios. Hence, we propose a reliable hybrid power line and wireless communication technique for Smart Grids. In addition, we study the coexistence between different Smart Grid wireless communication standards.

## TECHNICAL APPROACH

We focus on the last mile communication link between the utility data concentrator and the residential smart meter. The communication is implemented over power lines in the 3-500 kHz frequency narrow band and also over the unlicensed wireless frequency band from 902 MHz to 928 MHz. The interference on both the narrowband power line communication and the unlicensed wireless communication links is impulsive in nature. To mitigate such impulsive noise on both links, we propose a hybrid PLC/wireless communication technique where both links carry the same information data. We present an efficient combining technique for the received PLC and wireless signals that takes into account the impulsive nature of the interference.

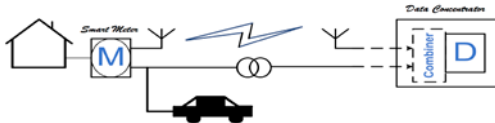


Figure 1: Smart Grid Communications

## SUMMARY OF RESULTS

We propose PLC/Wireless combining techniques that take into account the impulsive noise variations on the two links. For coherent modulation schemes, we compare three PLC/Wireless combining techniques with different performance-complexity tradeoffs, namely, average-SNR combining (ASC), power spectral density combining (PSC) and instantaneous-SNR combining (ISC). The ASC technique has the least complexity but worst performance. The ISC technique has the best performance, but requires a high pilot overhead and high complexity. The PSC technique provides the best performance/complexity tradeoff as it achieves better performance than ASC at a lower complexity than ISC. Figure 2 shows the bit-error-rate (BER) performance for the proposed combining techniques versus the  $E_b/N_o$  of the PLC link and the wireless links, respectively.

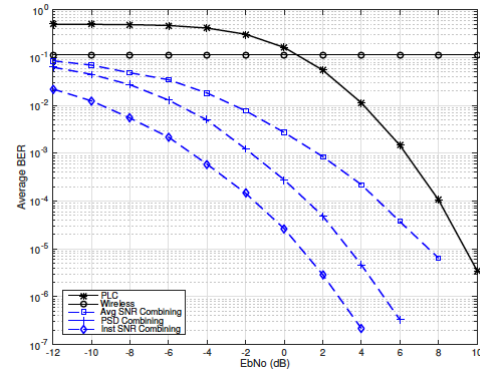


Figure 2: Average BER vs  $E_b/N_o$  of the PLC link for  $E_b/N_o = 0$  dB for the wireless link

Furthermore, for differential modulation schemes, we propose a combining technique that is based on the received signal power and the noise PSD. The proposed technique is shown in Figure 3 to outperform the conventional average SNR and equal gain combining techniques over the whole operating SNR range.

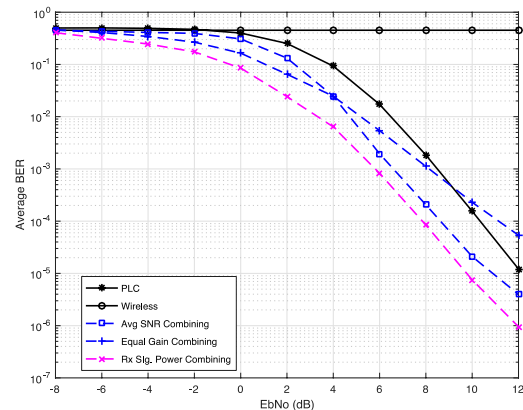


Figure 3: Average BER vs  $E_b/N_o$  of the PLC link for  $E_b/N_o = 0$  dB for the wireless link

**Keywords:** smart grids, power line and wireless communication, diversity, periodic impulsive noise

## INDUSTRY INTERACTIONS

Texas Instruments, NXP Semiconductors

## MAJOR PAPERS

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# TASK 1836.138, MICRO-POWER ANALOG-TO DIGITAL CONVERTERS

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## SIGNIFICANCE AND OBJECTIVES

Integrated sensor interface circuits require power-efficient high-accuracy data converters. In many applications, the best choice is to use incremental A/D converters (IADCs) incorporating extended counting. In this report, we discuss the operation, circuit design and layout of a novel IADC with multi-slope extended counting, which was implemented in a 0.18 $\mu\text{m}$  CMOS technology, and exhibited excellent performance.

## TECHNICAL APPROACH

A multi-step incremental ADC (IADC) with a multi-slope extended counting technique was developed for integrator sensor interface circuits. Each conversion cycle is divided into three steps, and a single active integrator is reused in each step to quantize the residue voltages, as shown in Fig. 1. The accuracy is extended by configuring the IADC as multi-slope ADCs in two additional steps. The slope coefficients are realized by capacitor ratios, which could achieve good matching accuracy. For the same OSR, the proposed multi-step IADC achieved as good an efficiency as a second-order  $\Delta\Sigma$  ADC, but at the reduced cost of only one active component.

## SUMMARY OF RESULTS

The prototype test chip was fabricated in a 0.18 $\mu\text{m}$  CMOS process. It occupies an active area of 0.5mm<sup>2</sup>. The die is packaged in a 48-pin QFN. Clocked at 642kHz, the implemented IADC consumes 35 $\mu\text{W}$ . The analog part consumes 26 $\mu\text{W}$  and the digital part 9 $\mu\text{W}$ . Both analog and digital blocks use a 1.5V supply. A common-mode voltage of 0.75V was used, and the differential full-scale range of the IADC is 2V<sub>p-p</sub>. The achieved PSRR at 50Hz line frequency is at least 102dB.

The measured output power spectrum densities indicate that the IADC achieves an SNDR of 52.2 dB over a 1 kHz bandwidth during the first step. The extended multi-slope counting in the second and third steps enhance the SNDR to 79.8 dB and 96.8 dB, respectively.

The IADC achieved a dynamic range of 99.7 dB, and the peak SNR is 98.4 dB.

The measured power at DC was around -68dBFS, which corresponds to a 0.7mV offset. This offset was found to result from the instrumentation, not from the IADC itself. The chopper stabilization reduced the flicker noise significantly, and decreased the measured output noise from 7.54  $\mu\text{V}$  RMS to 3.76  $\mu\text{V}$  RMS. Table I summarizes the measured performance.

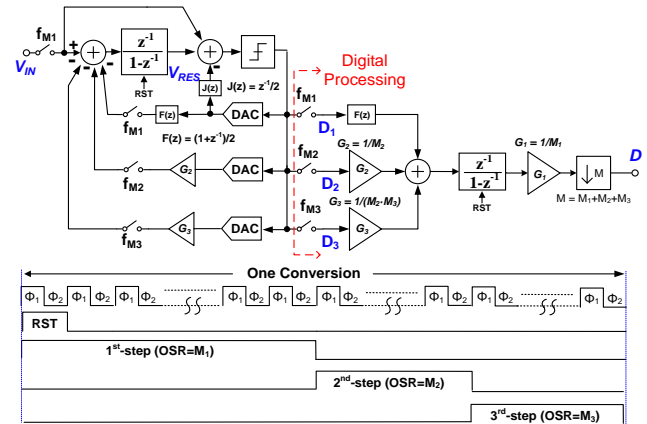


Figure 1: Block diagram of the IADC1 with multi-step extended counting and the simplified timing diagram

Parameter	This Work
Architecture	IADC1 + Multi-Slope
Technology	0.18 $\mu\text{m}$
Area (mm <sup>2</sup> )	0.5
VDD (V)	1.5
Diff. input range	2 VPP
Sampling Freq.	642 kHz
Bandwidth	1 kHz
Power	34.6 $\mu\text{W}$
PSRR	>102dB@ 50Hz
SNDR (dB)	96.8
DR (dB)	99.7
FoM1W (pJ/conv)	0.32

Table 1: Performance Summary

The prototype ADC achieved a FoMW of 0.32 pJ/conv-step and a FoMS of 174.6 dB, both among the best values published for IADCs.

**Keywords:** incremental ADC, extended counting, multi-slope ADC, integrated sensor interface, high-accuracy

## INDUSTRY INTERACTIONS

Texas Instruments, Freescale

## MAJOR PAPERS/PATENTS

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[2] Y. Zhang, C-H Chen, T. He, and G. C. Temes, "A 35 $\mu\text{W}$  96.8dB SNDR 1 kHz BW Multi-Step Incremental ADC Using Multi-Slope Extended Counting with a Single Integrator", Symposium on VLSI Circuits, Hawaii, June 2016, to be presented.

# TASK 1836.139, ENABLING FULLY-INTEGRATED VHF CLK-SYNC MULTIPHASE SWITCHING REGULATORS ON SILICON

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## SIGNIFICANCE AND OBJECTIVES

Voltage regulators in advanced SoCs systems are expected to support transient speed and power density higher than conventional regulators. In this project, the PI plans to investigate three major issues in development of VHF (30-300 MHz range) multiphase switching regulators: high-speed feedback control, clock synchronization, and system miniaturization.

## TECHNICAL APPROACH

For a control scheme, the PI proposed a current-mode hysteretic controller. Compared to its voltage-mode counterparts, this current-mode approach is more robust to the noise in output voltage, as the sensed control vector is inductor current.

From the perspective of system operation and circuit topology, interleaved multiphase topology can effectively improve the system response. By taking advantage of the proposed current-mode hysteretic control, a simple clock synchronization technique is proposed which achieves cycle-by-cycle regulation in each sub-converter.

For system implementation, the PI proposes a monolithic implementation of the regulator, which allows the power flow to follow the desired paths to reduce the parasitic.

## SUMMARY OF RESULTS

In this project, a fully on-chip integrated multiphase converter is proposed, and the system block diagram is shown in Figure 1(a). It is operating in the VHF frequency range, which allows full on-chip integration with bond-wires and on-chip capacitors. The proposed clock synchronization scheme is applied to the hysteretic control, achieving a fixed switching frequency to implement multi-phase operation. A multiphase implementation with VHF (200MHz) operation allows the design to reduce the sizes of input and output capacitors, resulting in full on-chip integration with bond-wires as the main inductors. Consequently, system form factor, transient response, and power density have been significantly improved. The full on-chip integration with bond-wires and on-chip capacitors are illustrated in Figure 1(b).

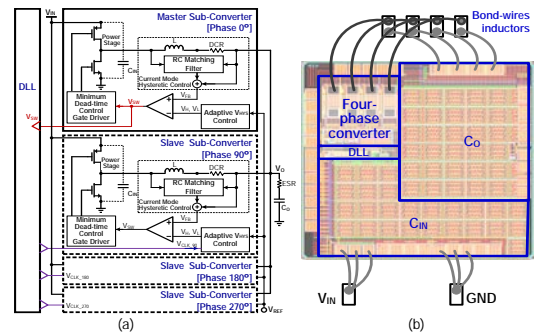


Figure 1: (a) System block diagram, and (b) chip layout

The waveforms of the clock synchronization in all the sub-converters are shown in Figure 2(a). The output ripple is maintained at 4.5 mV because of the precise clock synchronization with low ESR. The simulation results of load transient response with a 300mA/200ps load step are shown in Figure 2(b). In the step-up transient response, the output voltage droop is minimized to 79 mV, which has a 1% settling time of 10 ns.

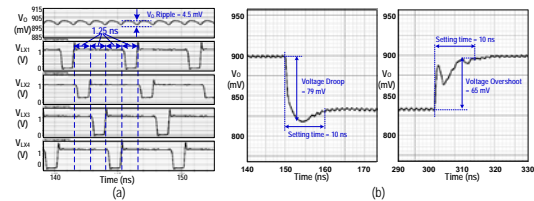


Figure 2: Simulation results: (a) steady-state operation, and (b) load transient response at step-up and step-down

**Keywords:** VHF switching, on-chip integration, multi-phase operation, high-speed feedback control

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

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- [2] M. Song et al., "Phase synchronization techniques in multiphase hysteretic controlled switching power converters," ISSOC, Gyeongju, South Korea, Nov. 2015.
- [3] M. Song et al., "A 200-MHz 4-phase fully integrated voltage regulator with local ground sensing dual loop ZDS hysteretic control using 6.5nH package bondwire inductors on 65nm Bulk," ASP-DAC, Macau, Jan. 2016.

# TASK 1836.140, EMBEDDED & ADAPTIVE VOLTAGE REGULATORS WITH PROACTIVE NOISE REDUCTION FOR DIGITAL LOADS UNDER WIDE DYNAMIC RANGE

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## SIGNIFICANCE AND OBJECTIVES

The primary goal of the project is to develop an integrated power flow architecture for fine-grained spatio-temporal voltage distribution and management in microprocessors and SoCs. We investigate through models, simulations, hardware development and experimentation, novel control topologies and circuit techniques for efficient wide-dynamic range linear and switched capacitor voltage regulators (VRs).

## TECHNICAL APPROACH

This project investigates power flow architecture in microprocessors and SoCs. There are two primary thrusts: (1) development of novel control topologies for all digital linear regulators for Point of Load (PoL) regulation and (2) use of switched capacitor on-die regulators to provide power on demand for distributed IP blocks. In this phase of the program, the major accomplishments have been on the development of novel PoL topologies, circuit prototyping and measurements.

## SUMMARY OF RESULTS

We have investigated two major topologies (1) switched mode control for ultra-fast droop recovery and (2) a novel unified voltage and frequency (UVFR) topology that allows operation of digital load circuits under fine-grained DVFS states while continuing to work during a voltage droop or during PLL relocking. In switched mode control, the LDO differentiates between small signal regulation and the large signal performance. Small signal regulation is handled by an output pole dominant analog loop, whereas the large signal transients are handled by

a digital loop. The requirement of the small signal loop is faster settling and that of the large signal loop is faster rise time. Both of these criteria are simultaneously met. A hybrid LDO based on SMC designed in a 130nm CMOS process features both digital and analog loops (Fig. 1). The design is tailored to meet the requirements of PoL regulation in digital load circuits with wide work-load dynamics. Measurements show peak response time of 18 ns for large load transients, low voltage operation programmability and a peak current efficiency of 98.64%. Motivated by the observation that the main objective of supply voltage regulation in digital systems is meeting timing, we present a Unified Voltage Frequency Regulator (UVFR) that sets the supply voltage based on system timing properties, and minimizes supply noise margins by temporarily modulating the clock frequency. Synthesized from all-digital cells, which generates and co-regulates a local clock and the local supply voltage simultaneously, the UVFR powers a digital load circuit block embedded in a multi-domain SoC. Here a frequency-only reference is provided (FREF) from a shared PLL. The regulated supply (VREG) is locally generated at one point in the loop and a local VCO clock (can be divided by N) which is locked to the reference (FLOC=NFREF) is generated at another point of the same loop (Fig. 2), providing a tightly coupled FLOC-VREG pair and the DVFS state is only defined uniquely by performance (FREF which is equal to FLOC). Measured data on a 130nm test-chip across a wide range of voltage and current inputs reveal peak current efficiency of 99.4% and 27% supply reduction at iso-performance through adaptation and resiliency which are intrinsic to the control loop.

**Keywords:** integrated voltage regulator, discrete control, continuous time control, LDO, switched mode control

## INDUSTRY INTERACTIONS

Intel, IBM

## MAJOR PAPERS/PATENTS

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- [2] Saad Nasir, et al. ISSCC, 2015.
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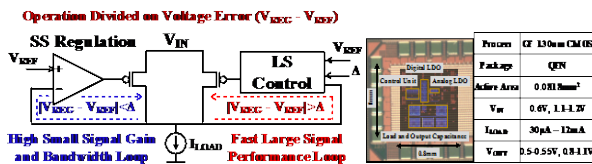


Figure 1: Switched Mode Control for LDO

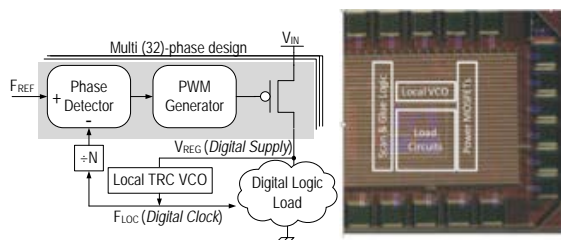


Figure 2: Unified Voltage and Frequency Regulation

# TASK 1836.142, LOW POWER APPLICATIONS OF FRAM

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## SIGNIFICANCE AND OBJECTIVES

Compared to flash, FRAM has significantly faster write access time, lower write energy, smaller peak current and orders of magnitude better endurance. This report details an adiabatic design of FRAM that can reduce the write energy, especially for large block writes.

## TECHNICAL APPROACH

The focus of our research is on ultra-low energy FRAM arrays for millimeter-scale sensor-networks. Millimeter-scale sensor-networks wake-up for short intervals, store sensor data, and transmit data intermittently, all with a very long battery life, requiring ultra-low energy non-volatile memories.

The objectives are to optimize FRAM for ultra-low-power operation. To achieve this we propose an adiabatic technique to write into the FRAM. Switching the bit-line (BL) and program-line (PL) capacitances by resonating them with an inductance, reduces the switching energy significantly.

## SUMMARY OF RESULTS

Figure 1 shows the FRAM array design with adiabatic write capability. The design supports sharing the inductor between multiple banks of FRAM. This allows us to use a single large discrete inductor.

To start, the capacitor in the LC tank is stepped to  $V_{DD}/2$ , which leads PL to resonate between 0 and  $V_{DD}$ . To write new data into a row, the BLs are switched to data adiabatically by controlling the WREN and PLEN, i.e. the starting point and ending point for data '0' is 0 of PL and for data '1' is  $V_{DD}$  of PL.

Each row needs one and a half cycle of resonance of PL to write data, as shown in Figure 2. To maintain the resonance amplitude, a continuous comparator based peak detector is used to monitor PL. It generates pull-up (PU) and pull-down (PD) pulses. The WL signals are overdriven to ' $V_{DD}+V_t$ ' to compensate for the threshold voltage drop.

Figure 3 shows, the write-energy per bit decreases for longer words in an array before stabilizing. The adiabatic design reduces the write energy per bit by 7x, and the read energy per bit by 4x.

Currently, the circuit implementation of the adiabatic FRAM array is being optimized, along with physical design and test harness design. The prototype of the low-power FRAM is scheduled for a September tape-out.

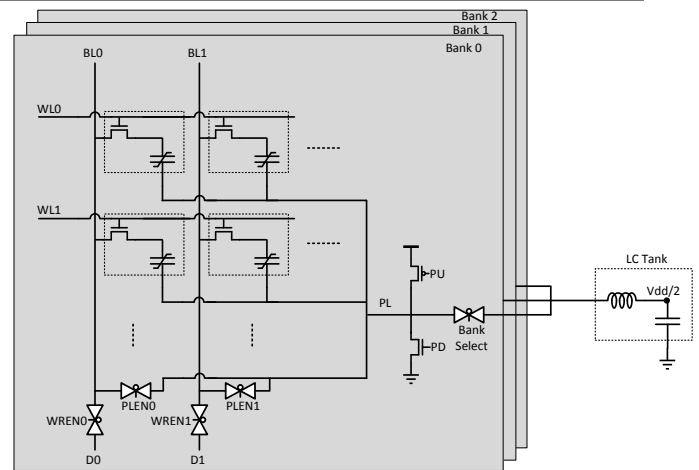


Figure 1: The proposed adiabatic design for FRAM array

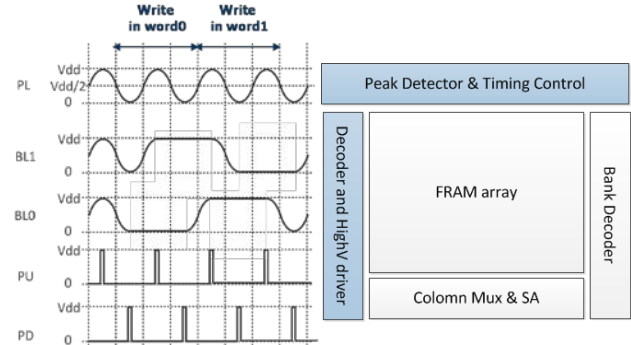


Figure 2: Both BL and PL transition adiabatically for saving energy. Peak detector generates PU/PD to restore amplitude

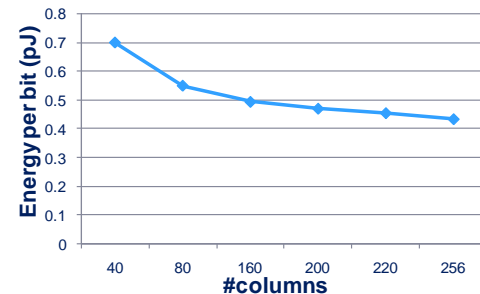


Figure 3: Write energy/bit for increasing number of columns

**Keywords:** sensor-networks, NVM, FRAM, low-power, adiabatic

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

None



# TASK 1836.143, DESIGN TECHNIQUES FOR MODULATION-AGILE AND ENERGY-EFFICIENT 60+GB/S RECEIVER FRONT-ENDS

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## SIGNIFICANCE AND OBJECTIVES

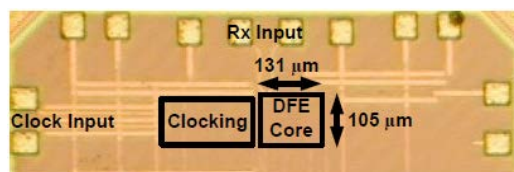
While high-performance I/O circuitry can leverage CMOS technology improvements, unfortunately the bandwidth of the electrical channels used for inter-chip communication has not scaled in the same manner. The high-speed serial link receiver design and modeling techniques proposed here aim to significantly improve interconnect bandwidth density in an energy-efficient manner.

## TECHNICAL APPROACH

In order to investigate design trade-offs, a statistical-modeling framework will be utilized to investigate power-optimum equalization partitioning and modulation format for 60+Gb/s signaling environments. This tool will be used to guide the design of a new modulation-agile receiver front-end which includes a multi-level decision-feedback equalizer (DFE) with multiple IIR feedback taps for efficient long-tail ISI cancellation. Adaptive techniques will also be developed to tune key equalization parameters, such as DFE tap time constants/weights and CTLE settings.

## SUMMARY OF RESULTS

While receivers with DFEs are now in wide use, architectures which employ a common FIR feedback filter



(a)

TABLE I: PERFORMANCE SUMMARY

References	This Work	[4]	[5]	[6]
Data Rate	32 Gb/s / 25 Gb/s	32 Gb/s	25Gb/s	28 Gb/s
Architecture	1-FIR + 2-IIR tap	CTLE + 1 tap DFE	CTLE + 2 tap DFE	CTLE + 15 tap DFE (2-tap speculation)
Clocking	Quarter Rate	Full Rate	Half Rate	Half Rate
Modulation	PAM4	PAM2	PAM2	PAM2
Comparator Type	Regenerative latch	CML	Charge steering latch	Regenerative latch
Total Loss @ Nyquist	17* dB / 21* dB	18 dB	24 dB	35 dB
Eye Width BER	17% / 10 <sup>6</sup>	15% / 10 <sup>9</sup>	44% / 10 <sup>12</sup>	44% / 10 <sup>12</sup>
Supply (V)	1	1	0.73	1
Power (mW)	17.7	13.1	9.3	5.8
(mW/Gbps)	0.55	0.52	0.29**	0.23**
Area (mm <sup>2</sup> )	0.014	0.0175	0.068	0.01
Technology	65-nm	65-nm	45-nm	45-nm
				32-nm SOI

\* Including -9.5 dB of PAM4 modulation loss.

\*\* Doesn't include the clock buffers' power consumption.

\*\*\* DFE power only.

(b)

Figure 1: 32Gb/s PAM4 DFE with 1-FIR and 2-IIR taps: (a) GP 65nm CMOS prototype (b) performance summary

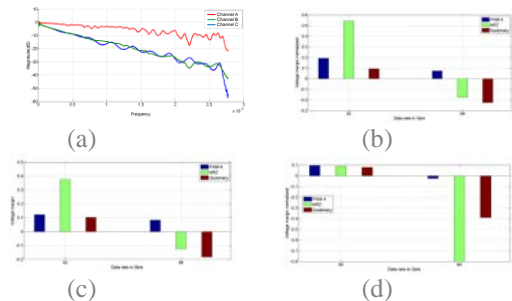


Figure 2: Statistical modeling of 50 and 64Gb/s systems: (a) Channel models with differing loss profiles. Normalized voltage margin for (b) Channel A, (c) Channel B, and (d) Channel C

require an ever-growing number of taps to cancel the long-tail ISI found in typical backplane channels. In order to address this, DFEs with IIR feedback filters have been implemented and shown to improve equalization efficiency for RC-limited and backplane channels. Also, utilizing more spectrally-efficient modulation allows for longer unit interval times can relax timing, while also being potentially better suited for a specific channel loss profile. To address this, a new high-speed PAM4 receiver front-end which includes a multi-level decision-feedback equalizer with 1-FIR and 2-IIR feedback taps for efficient long-tail ISI cancellation was developed in GP 65nm CMOS [1] (Figure 1). The receiver occupies 0.0138 mm<sup>2</sup> area and achieves power efficiencies of 0.55 and 0.52 mW/Gbps with 32 Gb/s and 25 Gb/s PAM4 data, respectively. Under low BER requirements, transient simulations are impractical. In order to investigate this, this project continues to build upon the PI's statistical-modeling framework for high-speed serial links. This tool is utilized to investigate the optimal equalization partitioning and modulation format for 60+Gb/s signaling environments, relevant for applications such as 400Gb Ethernet. As shown in the 50 and 64Gb/s modeling results of Figure 2, the optimal modulation format is a function of the channel loss profile.

**Keywords:** decision feedback equalizer, infinite impulse response (IIR) DFE, receiver, serial link

## INDUSTRY INTERACTIONS

IBM, Texas Instruments

## MAJOR PAPERS/PATENTS

[1] O. Elhadidy et al., "A 32 Gb/s 0.55 mW/Gbps PAM4 1-FIR 2-IIR Tap DFE Receiver in 65-nm CMOS," IEEE VLSI Symp., June 2015.

# TASK 1836.144, HIGH-EFFICIENCY HIGH-VOLTAGE POWER CONVERTERS

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## SIGNIFICANCE AND OBJECTIVES

This research aims to investigate novel soft-switching techniques, synchronous gate driving techniques, and control schemes to significantly advance power efficiency and power density of today's high-voltage DC-DC converters. These developed converter technologies help greatly lower the cost and the energy efficiency of renewable energy systems, telecom systems, automotive systems, etc.

## TECHNICAL APPROACH

A quasi-square-wave (QSW) zero-voltage-switching (ZVS) isolated three-level half-bridge architecture is reported to enable high-voltage isolated converters achieving high power efficiency at high switching frequencies. A new integrated synchronous three-level gate driver as shown in Fig. 1 is also developed to ensure reliability of all eGaN power FETs and provide fast propagation delays for high-frequency converter operation. Moreover, a high-speed dynamic level shifter as shown in Fig. 2 is also proposed in the gate driver.

## SUMMARY OF RESULTS

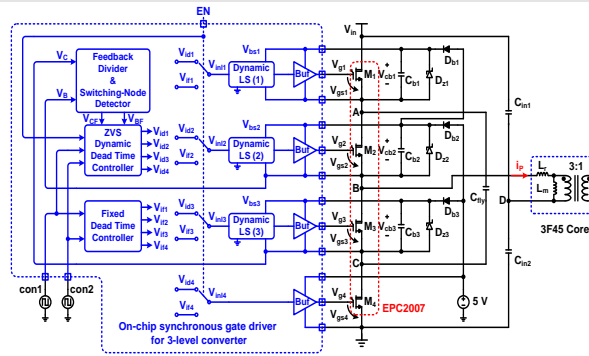


Figure 1: Structure of the proposed three-level synchronous gate driver for isolated QSW-ZVS converter

A hardware prototype of the proposed isolated QSW-ZVS three-level half-bridge converter with the proposed on-chip synchronous gate driver was developed to verify converter performances. The on-chip gate driver was developed in a 0.5 $\mu$ m 100V CMOS process for driving 4 eGaNs (epc2018) in the power stage of the converter. The transformer's turn ratio is 3:1 and the core is 3F45. Based on the measurement results, the proposed converter can successfully operate up to 2MHz and delivers up to 35W output power with the on-chip gate driver. Fig. 3 demonstrates that the top eGaN M1 can achieve ZVS during transition of its turn on for minimizing the switching power loss of the converter

under high input voltage and switching frequency conditions. Fig. 4 shows that the measured converter peak power efficiency is 95.2% and 90.7% at 1MHz and 2MHz, respectively. This outperforms the state of art converters.

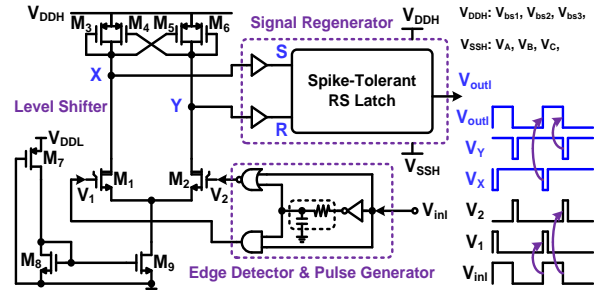


Figure 2: Structure of the proposed dynamic level shifter

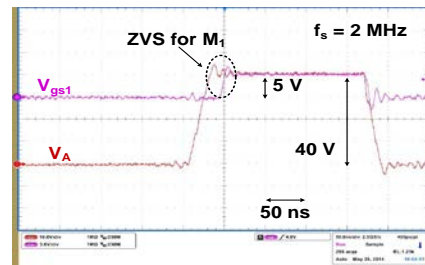


Figure 3: Measured ZVS performance of M1

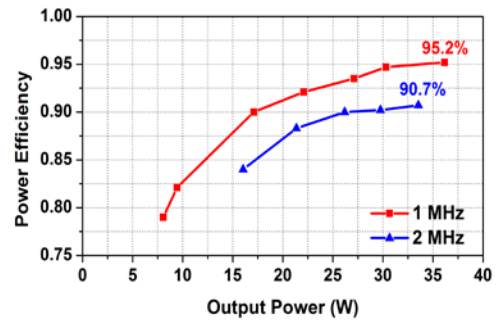


Figure 4: Measured converter power efficiency

**Keywords:** high-voltage DC-DC converters, isolated converters, on-chip synchronous gate driver, three-level converters, zero-voltage switching

## INDUSTRY INTERACTIONS

Texas Instruments, Intel

## MAJOR PAPERS/PATENTS

[1] J. Xue, etc, "A high-efficiency high-frequency GaN-based three-level isolated DC-DC converter with dynamic dead-time controlled synchronous gate drive," SRC *TECHCON Conference*, Austin, TX, USA, Sep. 2015.



# TASK 1836.146, ON-CHIP AC-DC POWER CONVERSION WITH GROUND DISTURBANCE SHIELDING FOR ENVIRONMENTAL SENSING APPLICATIONS

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## SIGNIFICANCE AND OBJECTIVES

This project is to explore the optimal circuit architecture and operation scheme in achieving on-silicon AC-DC power conversion for environmental sensor applications. The power converter under development should be resilient to ground voltage disturbance, along with high power efficiency and small physical form factor.

## TECHNICAL APPROACH

Capacitive power transfer enables implementation of fully integrated power converters. It is resilient to ground voltage surge and noise by using a high-voltage on-chip capacitor, which provides a smaller form factor than a traditional discrete transformer. Thanks to a novel operation scheme, the proposed topology can achieve power transfer efficiency over 50% when it is operating in low power (<20mW) region.

## SUMMARY OF RESULTS

A capacitive isolation technique can replace the bulky transformer-based barriers with on-chip capacitors, and lead to a low-cost monolithic implementation. However, the low capacitance density for high-voltage capacitors and large bottom-plate parasitic capacitance limit the output power level and efficiency of the capacitive power transfer.

As shown in Fig. 1, the resonant circuit architecture for isolation power transmission is proposed. Being differentiated from traditional capacitive coupling, two small inductors are placed on the power path, and form a resonant tank with the isolation capacitor and bottom-plate capacitor. They not only can reduce the impedance from the low-density capacitors on the power path, but also limit the current peak that charge/discharge the bottom-plate capacitors.

Operation of the resonant converter is as follows. DC voltage  $V_{IN}$  is converted by an H-bridge circuit into a square wave,  $V_{SW}$ , at LX node with a frequency of  $f_{SW}$ . When  $f_{SW}=f_{resonant}$ , the fundamental component can pass through the resonant tank. And the full-wave rectifier converts the selected AC power at the output node as DC power supply for loads.

To further reduce system switching loss in low power regions, we proposed a sub-harmonic operation for the resonant converter. Instead of using  $f_{resonant}$  to drive power switches, we can have the resonant tank only response to the higher-order harmonics. As shown in Fig.

2, when the required  $P_{OUT}$  levels decreases, the converter can be running at  $f_{SW}=1/3$  or  $1/5 f_{resonant}$ . So the resonant tank responds to the higher order harmonics, but power loss from the power switches is decreased, and power efficiency is maintained. As shown in Fig. 3, by using the sub-harmonic operation, the system efficiency can be maintained around 50%, and achieve the maximum value of 52% at  $P_{OUT}=25mW$ .

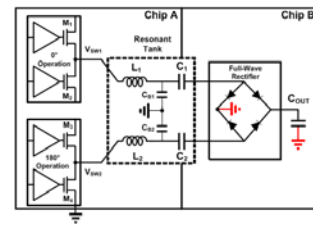


Figure 1: The resonant converter for isolation power transfer

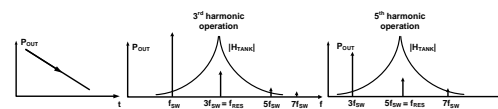


Figure 2: Using sub-harmonic operation to modulate  $P_{OUT}$

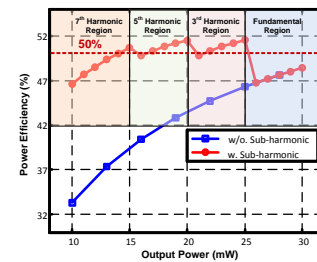


Figure 3: Efficiency vs.  $P_{OUT}$  levels with sub-harmonic operation

The proposed resonant topology with sub-harmonic operation enables the on-chip capacitive isolation power transfer system to achieve higher efficiency at low power transfer. Our future work includes building up a prototype chip and exploring solutions to the on-chip capacitive isolation feedback scheme and data link.

**Keywords:** capacitive isolation technique, resonant converter, AC-DC converter, sub-harmonic operation, high power transfer efficiency

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

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# TASK 1836.149, CONDITION MONITORING OF PM/IPM MOTORS THROUGH AXIAL/RADIAL LEAKAGE FLUX

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## SIGNIFICANCE AND OBJECTIVES

Leakage flux analysis provides diagnosis results independent from motor topology, number and location of defected magnets, motor operating point to name a few, which are essential features for adjustable speed drive applications.

## TECHNICAL APPROACH

A comparison between classical methods such as analyzing back-emf and current and analysis of leakage flux (Fig. 1) is carried out. The dynamic behaviors of the flux spectrum components and effects of sensor location are discussed in detail. It is shown that the leakage flux analysis yields accurate and reliable results than that of analyzing back-emf and currents.

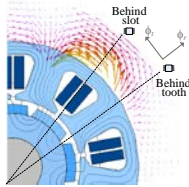


Figure 1: Sensor locations around the motor

## SUMMARY OF RESULTS

The magnet defect fault creates characteristic fault signatures in the current spectrum. The weakness of current waveform analysis is that its frequency spectrum can be different depending on winding configuration, connection type and motor topology. As can be seen from Fig 2(a), characteristic fault signatures in back-emfs spectra do not show up in 36-slot/6-pole, but in leakage flux spectra. Besides, both back-emf and leakage flux spectra are analyzed in which magnet-1 and magnet-3 are broken. Some fault signatures such as 0.5<sup>th</sup> cannot be observed on the back-emf spectrum whereas all fault related signatures do exist in the leakage flux spectrum (Fig. 2(b)). Fig. 2(c) shows the current and leakage flux spectra for 9-slot/8 pole combination, respectively. It is clearly shown that 0.75<sup>th</sup> harmonics do not appear in the current spectrum as shown in Fig. 2(c) whereas all fault related harmonics including 0.75<sup>th</sup> are seen in the leakage spectrum. The signatures at 0.25<sup>th</sup> and 0.5<sup>th</sup> are investigated at different fault and torque/speed levels. The fault signature amplitudes increase in parallel to increasing fault level and the signature amplitudes are pretty stable and hence enable torque and speed independent fault detection (Fig. 3).

## INDUSTRY INTERACTIONS

Texas Instruments

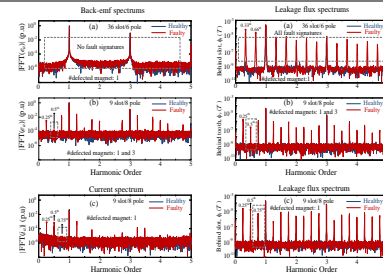


Figure 2: Advantages of leakage flux spectrums

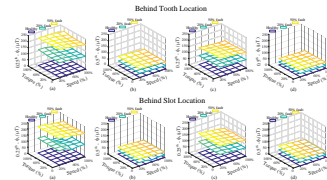


Figure 3: Fault signatures at different locations, leakage flux

**Keywords:** fault diagnosis, condition monitoring, fluxgate sensors, leakage flux spectrum analysis

## MAJOR PAPERS/PATENTS

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# TASK 1836.153, HIGH-SPEED COMPACT POWER SUPPLIES FOR ULTRA-LOW-POWER WIRELESS SENSOR APPLICATIONS

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## SIGNIFICANCE AND OBJECTIVES

High-speed power supplies are highly desirable for wireless sensor nodes (WSNs) to attain fast wake-up/shut-down, conserve the energy and prolong the system life-time. This project seeks to investigate a monolithic, reconfigurable switched-capacitor power converter (SCPC) with fast load transition and dynamic voltage scaling (DVS) capability for sensor systems.

## TECHNICAL APPROACH

A unit switched-capacitor cell consisting of one flying capacitor and five power switches is proposed in this project. The complex reconfigurable power stage is simplified by only connecting multiple unit cells in series or parallel. The designed SCPC can achieve both step-down and step-up conversions to support wide input and output voltage ranges. Meanwhile, by controlling the gain configuration, the proposed SCPC supplies different output voltages for wake-up/shut-down operation. Moreover, the interleaving scheme is adopted in this project with active phase modulation (APM) to enable fast load transient response and maintain efficiency at light load.

## SUMMARY OF RESULTS

The proposed SCPC in this report utilizes a two-stage topology with a unit switched-capacitor (SC) cell to achieve 6 step-down conversion ratios (CRs) and 6 step-up CRs, shown in Figure 1. Once the mode transitions of WSN are detected, the reference voltage for the proposed SCPC will be altered, such as, load step-up during wake-up will cause the reference voltage increase by an offset voltage, and a higher CR is thus selected for DVS tracking. In terms of the shut-down operation, SCPC uses a lower CR to supply low output voltage and reduces the system power consumption. Besides, during the load transitions, the output voltage undershoot/overshoot can be minimized by the corresponding CR change, therefore, the transient response time is also reduced.

To enable fast transient response, the proposed SCPC uses four interleaved phases to increase the equivalent switching frequency and reduce output ripple. Figure 2 is the expected SCPC system architecture. High frequency clock is generated by a voltage-controlled inverter-based ring oscillator, such that, the switching frequency can be easily modulated by the error between the output voltage and the reference voltage. Four interleaving SCPC

phases are implemented with a 90° phase shift, controlled by digital logic circuits. To implement CR reconfiguration during wake-up/shut-down, the reference voltage for integrated CR optimizer can be varied by the offset voltage, which is determined by the load information. Furthermore, the designed SCPC can adaptively control the number of interleaving phases for different load conditions. At light load, the switching behavior is disabled in the redundant interleaving phases, saving dynamic power, to attain higher efficiency. Although the redundant interleaving phases are turned off at light load, the charge is still stored on flying capacitors. Once the switching behavior recovers, the charge can be directly delivered to the load, ensuring fast transient response.

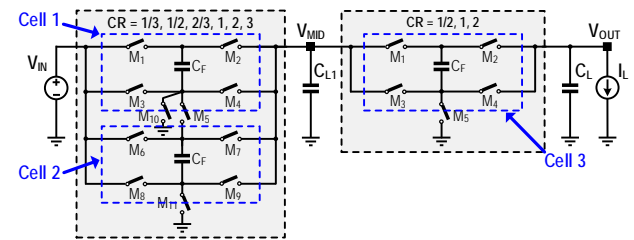


Figure 1: Reconfigurable power stage structure with three unit cells to achieve both step-down and step-up conversions

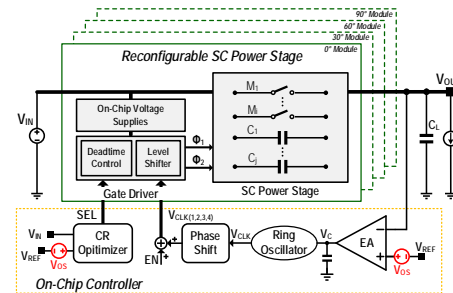


Figure 2: Proposed SCPC system architecture with interleaving 4-phase and CR reconfiguration

The circuit for on-chip controller will be implemented. Besides, alternative low-power control schemes for fast transient response will be investigated to further improve the efficiency and reduce the quiescent current.

**Keywords:** wireless sensor nodes, DC-DC conversion, switched-capacitor, interleaving, fast transient response

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

# TASK 1836.154, STATE OF THE HEALTH (SOH) FOR IGBTs: INCIPIENT FAULT CHARACTERIZATION AND DEGRADATION MONITORING

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## SIGNIFICANCE AND OBJECTIVES

This project aims to investigate incipient faults of IGBT devices and create online fault diagnosis/failure prognosis tools to establish early warning system for future power electronics (PE) systems. Continuously monitoring these systems is essential to prevent unexpected shutdowns and catastrophic failures that may result in fatal accidents or significant operation loss.

## TECHNICAL APPROACH

Device prognostics and failure prediction require accurate device characterization with respect to aging. Furthermore, identifying failure indicators is also required. In this regards, our first goal was to capture variations in all current-voltage characteristics and parasitic elements of IGBTs. Shifts in device characteristics like threshold voltage ( $V_{TH}$ ), input/output/ reverse capacitances ( $C_{ies}$ ,  $C_{oes}$  and  $C_{res}$ ), collector-emitter voltage ( $V_{ce,on}$ ), leakage currents ( $I_{ge}$  and  $I_{ce}$ ) and gate resistance ( $R_g$ ) for new and aged devices were studied.

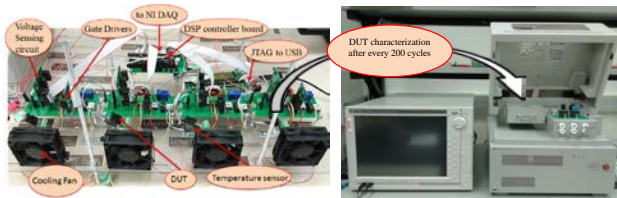


Figure 1: Aging setup schematic

## SUMMARY OF RESULTS

In order to analyze the parametric shifts in IGBTs, an accelerated thermal stress-testing system is built to conduct active temperature-cycling tests on discrete IGBT devices. The aging setup is shown in Fig 1. Samples of 1200V/11A IGBTs were subjected to relatively large temperature swings. Each sample was subjected to temperature swing of 40-200°C. A Keysight curve tracer is used for measuring aged device parameters. Each device is characterized using the curve tracer before and after applying thermal stress protocols. Failure analysis (T-SAM, C-SAM) results suggested possible delamination and void formation in the die-attach layers. By cross-section crack initiation at bond-wire/pad interface was revealed. The crack initiation increased the contact resistance, which was verified by the increase of the on-state collector-emitter voltage. Also, gate-oxide degradation contributes to an increase of gate-threshold voltage.

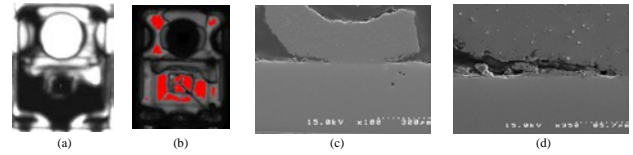


Figure 2: Failure analysis results; (a) T-SAM, (b) C-SAM, (c) full-scale view of a bond wire in an aged IGBT after cross-sectioning and (d) zoomed-in to initiated crack

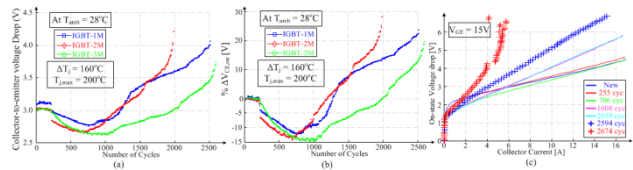


Figure 3: Contact resistance degradation; (a) Online  $V_{ce}$  measurement, (b) % change in online  $V_{ce}$  drop and (c)  $V_{ce}$  vs  $I_{ce}$  measurement

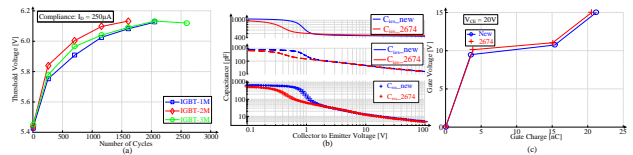


Figure 4: IGBT thermal stress results; (a) threshold voltage ( $V_{TH}$ ), (b) input capacitance ( $C_{ies}$ ), output capacitance ( $C_{oes}$ ) and reverse capacitance ( $C_{res}$ ) and (c) gate charge ( $Q_g$ ) measurement

**Keywords:** failure diagnosis, failure precursor, on-state voltage drop, gate threshold voltage, accelerated thermal aging

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

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# TASK 1836.157, CMOS GPS 12-BIT SAR ADC ARRAY WITH ON-CHIP REFERENCE BUFFERS

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## SIGNIFICANCE AND OBJECTIVES

ADCs that can deliver GS/s, 12-14 bit performance are of critical demand for applications such as wireless base stations, instrumentations, and software-defined radios, and usually consume more than 500 mW. The target of this work is to time-interleave 4 pipelined two-step SAR ADCs to achieve GPS throughputs at a 12-bit resolution with a power consumption of less than 50 mW.

## TECHNICAL APPROACH

The sub ADC used in the time-interleave array is based on the pipelined two-step SAR architecture which can deliver a desirable throughput while maintaining high power efficiency [1]. To further enhance the conversion speed, 2b/cycle conversion scheme is exploited by the first stage [2]. The offsets of first-stage comparators are calibrated in a foreground way to remove the impact on the overall conversion accuracy. Meanwhile, a dynamic amplifier is employed as the inter-stage residue amplifier. Benefiting from the dynamic amplifier, a very power efficient residue amplification that also consumes less time relative to the conventional amplifier is obtained.

## SUMMARY OF RESULTS

The schematic design and layout of the sub ADC have been completed. Now the sub ADC chip is in the process of manufacturing. Figure 1 shows the layout screenshot of the sub ADC. The ADC core only occupies an active area of 460 $\mu$ m x 160 $\mu$ m.

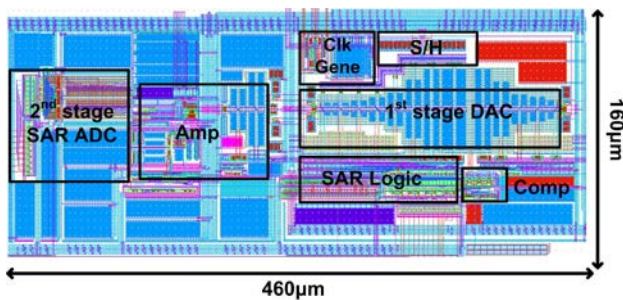


Figure 1: Layout of the sub ADC

Figure 2 shows the post-layout simulated spectrum of the ADC running at 250MHz (with thermal noise). A foreground digital calibration is used to correct DAC mismatch and inter-stage gain error. The simulation result indicates an 80.4dB SFDR and a 68.8dB SNDR with a near-DC input frequency. The SNDR of this ADC with

near-Nyquist input frequency drops to 67.6dB because of the impact of clock jitter.

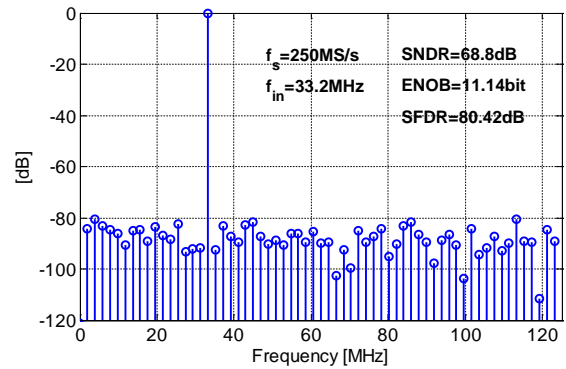


Figure 2: The simulated ADC output spectrum with transient noise

Table 1 summarizes the simulated SNDR of the ADC at different process corners. It can be seen clearly that the ADC is robust over process variations. The power consumption of the ADC is around 7 mW, leading to a figure of merit of 15fj/conv-step. All post-layout simulation results lead us to believe that a 250MS/s, 12b sub ADC with good power efficiency in 65nm CMOS is feasible.

Corner	TT	FS	SF	FF	SS
SNDR (dB)	68.8	68.5	68.5	68.6	68

Table 1: Simulated SNDR at different process corners

**Keywords:** pipelined two-step SAR, dynamic amplifier

## INDUSTRY INTERACTIONS

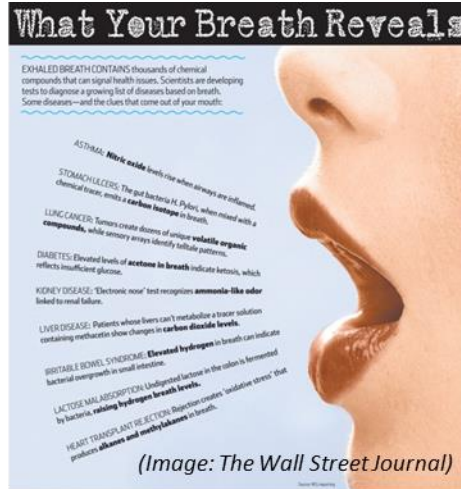
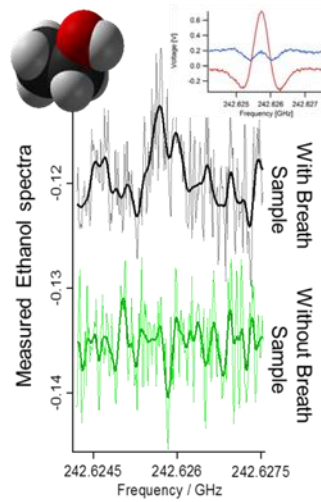
Texas Instruments

## MAJOR PAPERS/PATENTS

[1] Y. Zhou et al., "A 12 bit 160 MS/s Two-Step SAR ADC With Background Bit-Weight Calibration Using a Time-Domain Proximity Detector," IEEE J. of Solid State Circuits, 2015.

[2] H. Huang et al., "A 1.2GS/S 8bit Two-Step SAR ADC in 65nm CMOS with Passive Residue Transfer," IEEE Asian Solid-State Circuits Conference, 2015.

# Health Care Thrust



Category	Accomplishment
Health Care (Circuits)	A transmitter using a fractional-N PLL that generates frequency shift keyed (FSK) signals at 208 to 255 GHz with a 570-Hz frequency step and ~10 μs settling time (1836.119, PI: K. O, UT Dallas) and a 225-280GHz integrated receiver (1836.147, PI: W. Choi, UT Dallas) fabricated in 65-nm CMOS have been incorporated into a rotational spectrometer (1836.126, PI: F. De Lucia OSU (Ohio) and I. Medvedev of Wright State U.) to detect Ethanol in human breath (38 ppm).
Health Care (Circuits)	A low-power low-noise 0.7-V mixer-first RF frontend for an IEEE 802.15.6 narrowband receiver which uses frequency translated mutual noise cancellation based on passive coupling is demonstrated in 65-nm CMOS. Unlike traditional noise-cancelling techniques, symmetrical noise cancellation of a fully differential structure is performed where each path cancels the noise of the other at IF. The figure of merit is 10 dB higher and the power consumption is 194 μW, which is 0.5x lower than the state-of-the-art. The local oscillator power used is -14 dBm. (1836.098, PI: R. Harjani, U. of Minnesota)





# TASK 1836.098, SUB MW WIRELESS TRANSCEIVER FRONTEND FOR BODY AREA NETWORKS

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## SIGNIFICANCE AND OBJECTIVES

The project focuses on developing a low power transceiver frontend to meet the IEEE 802.15.6 Wireless Body Area Networks (WBAN) narrowband specifications from 2360 to 2483MHz.

## TECHNICAL APPROACH

Our design approach is to use novel simple architecture which consumes less power, sub-threshold operation, explore optimal partitioning of functions between analog and digital sections, applying injection locking, noise cancellation, current reuse techniques to minimize power consumption.

## SUMMARY OF RESULTS

The overall block diagram of the transceiver is shown in Figure 1. We have designed and fabricated both the TX and RX. We have taped out and tested the transmitter in IBM 130nm technology. A MUX-based architecture is proposed where modulation occurs at 800MHz (i.e., 1/3rd the RF frequency). The energy efficiency including the estimated power of the PLL is 2.5nJ/bit. Further, this design does not require cap bank calibration, and can support

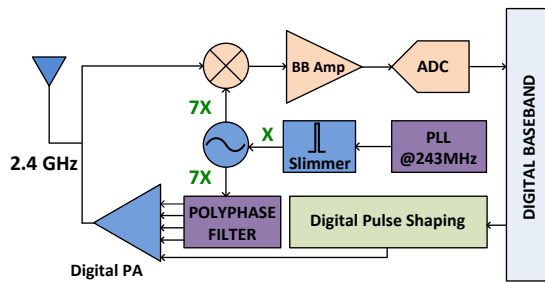


Figure 1: Transceiver architecture

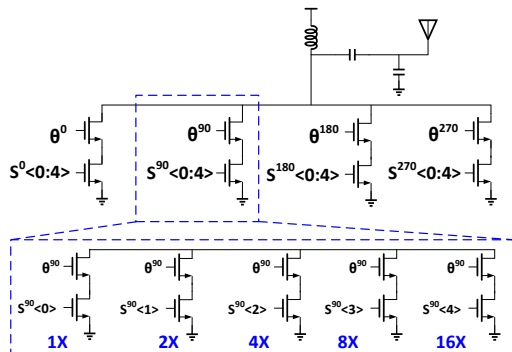


Figure 2: Circuit diagram of the digital PA

a large number of channels (118) even at high GHz frequencies. The modulation scheme is very precise with measured RMS EVM of 3.21%.

We have taped out and tested a low IF receiver using a TSMC 65nm technology. A low power low noise 0.7V mixer first RX frontend is designed which uses passive coupling based frequency translated mutual noise cancellation. This design (Figure 3) improves on all three specifications i.e. FOM, LO power & NF. Further, a novel mutual noise & nonlinearity cancelling LNA has been fabricated in a TSMC 65nm technology. The full system (Figure 1) including TX with a digital PA (Figure 2), RX and PLL has been taped out in GF 130nm RF process in May 2016.

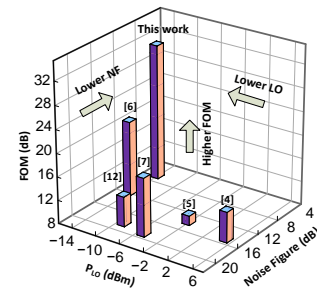


Figure 3: Chart comparing FOM, LO power and NF of RX

**Keywords:** 802.15.6, WBAN, low power RF, injection locked oscillator, noise cancellation

## INDUSTRY INTERACTIONS

Texas Instruments, Intel, Freescale

## MAJOR PAPERS/PATENTS

- [1] M. Rahman, R. Harjani, "A sub-1V 194μW 31dB FOM 2.3-2.5 GHz Mixer-First Receiver Frontend for WBAN with Mutual Noise Cancellation," IEEE Transactions on Microwave Theory and Techniques, April, 2016.
- [2] M. Rahman, M. Elbadry, R. Harjani "An IEEE 802.15.6 Standard Compliant 2.5nJ/bit Multiband WBAN Transmitter using Phase Multiplexing and Injection Locking," IEEE Journal of Solid-State Circuits, May, 2015.
- [3] M. Rahman, R. Harjani "A 0.7V 194μW 31dB FOM 2.3-2.5 GHz RX Frontend for WBAN with Mutual Noise Cancellation using Passive Coupling," IEEE RFIC 2015.
- [4] M. Rahman, M. Elbadry, R. Harjani "A 2.5nJ/bit Multiband (MBAN & ISM) Transmitter for IEEE 802.15.6 based on a Hybrid Polyphase-MUX/ILO based Modulator," IEEE RFIC, June, 2014.

# TASK 1836.159, SENSOR MATERIAL EVALUATION AND PRELIMINARY TESTING COVERING SENSING ELEMENTS, ELECTROLYTE MATERIALS AND POROUS MEMBRANE

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## SIGNIFICANCE AND OBJECTIVES

Evaluation of materials and sensor element design to address current challenges in CO<sub>2</sub> gas sensors, which are stable signal to noise ratio (SNR), drifting sensor performance due to environmental factors, and selectivity of sensing element in varying test matrices. This evaluation needs a controlled environment.

## TECHNICAL APPROACH

This task includes design and fabrication of the sensing element through the selection of electrode, electrolyte and their assembly mechanism. Room Temperature Ionic Liquids (RTILs) and other CO<sub>2</sub> sensitive material candidates will be explored as electrolyte. Electrochemical analysis will be utilized to finalize the sensor stack components. The novelty lies in the approach of utilizing high electrochemical double layer (EDL) capacitance due to RTIL in amplifying the sensor response.

## SUMMARY OF RESULTS

This is the first report being presented under this project for the research conducted for the quarter Jan 2016 to Apr 2016. This task focused on defining the electrode pattern and material for the test vehicle sensing element. Types of sensing elements tested are shown in Figures 1 (a)-(d). Four RTILs selective towards CO<sub>2</sub> were carefully chosen from the literature. Initial investigations of gas response for the RTILs were explored utilizing premixed gas containers (Gamry test box in Figure 1(e)) while the gas mixer is on order. The contact angle and surface tension of RTILs on the silicon and gold surfaces were tested using goniometer to understand the hydrophobicity of RTILs as displayed in Table 1. These RTILs were tested in Nitrogen flow for sensor designs in Figures 1(a) and 1(c) to understand the EDL capacitance formed on the electrode surface using Electrochemical Impedance Spectroscopy (EIS) shown in Table 2. This comparison also contributed towards understanding the role of gold vs CPE electrodes. Hence, the sensing element displayed in Figure 1(d) was selected as the final test vehicle with IDE gold electrodes on PCB. Further steps include testing the RTILs in CO<sub>2</sub> flow of 400 ppm, 750 ppm and 1000 ppm gas concentration to understand diffusion of gas in RTILs, the ability of RTILs to distinguish between different CO<sub>2</sub> concentrations, the response time and recovery time.

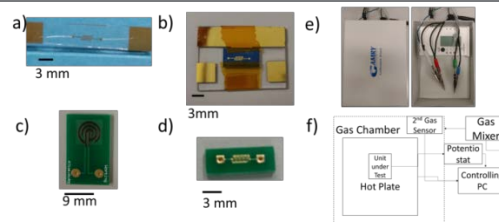


Figure 1: (a) gold electrode on glass substrate, (b) gold electrode on silicon wafer, (c) Carbon Paste electrode (CPE) on PCB, (d) gold electrode on PCB, (e) Preliminary test chamber, (f) Schematic of modified gas chamber

The modified chamber shown in Figure 1(f) will be capable of utilizing LabWindowsCVI, and the control PC will be able to extract real time data from all of the equipment in the figure. This will allow for time stamped data collection for more consistent and repeatable results.

Table 1: RTIL tested and contact angle, surfacetension measurements

RTIL	Contact angle		Standard deviation		Surface Tension (dynes/cm)	Standard deviation (dynes/cm)
	On Si-SiO <sub>2</sub> wafer	On Gold electrodes	On Si-SiO <sub>2</sub> wafer	On Gold electrodes		
EMIM[BF <sub>4</sub> ]	38°	26.5°	0.077°	0.05°	39.51	1.93
EMIM[TFSI]	32.4°	31.9°	2.8°	1.76°	22.91	0.22
EMIM[FAP]	33.2°	36.1°	0.68°	2.8°	24.34	0.91
MMIM[MeSO <sub>4</sub> ]	36.7°	66.1°	4.8°	3.0°	50.98	0.05

Table 2: Results of RTIL testing

	Capacitance on CPE-PCB (μFcm <sup>-2</sup> )	Capacitance on gold-glass (μFcm <sup>-2</sup> )
EMIM [BF <sub>4</sub> ]	0.401	4.150
EMIM [TFSI]	0.904	3.306
EMIM [FAP]	0.838	7.663
MMIM [MeSO <sub>4</sub> ]	1.104	9.038

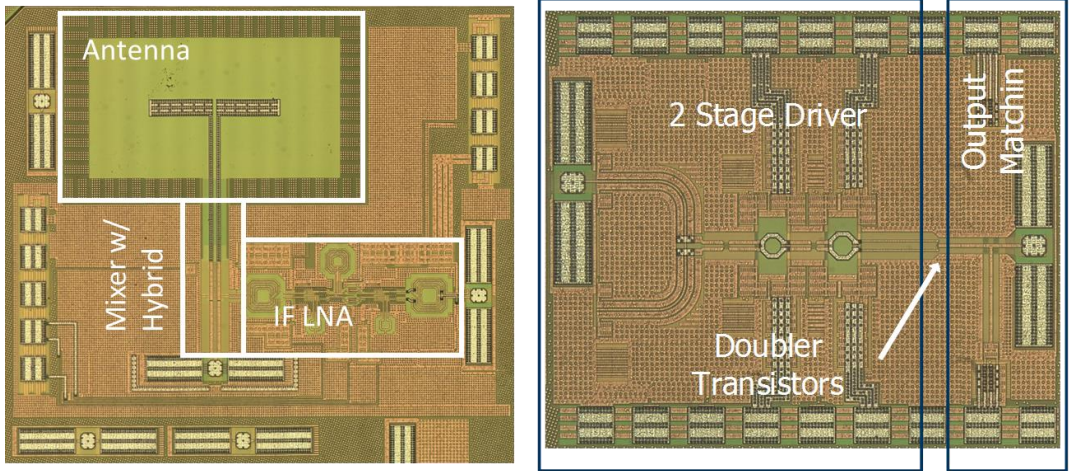
**Keywords:** room temperature ionic liquid, electrochemical impedance spectroscopy, CO<sub>2</sub> sensor

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

## Safety and Security Thrust



Category	Accomplishment
Security and Safety (Circuits)	Low-cost millimeter-wave spectrometers could provide critical capabilities for electronic noses, including breath analysis and detection of harmful molecules. The first ever demonstration of CMOS-based mm-wave spectroscopy is achieved. The 65-nm receiver (1836.147) operates between 225-280 GHz, and includes a down conversion mixer, LO chain, and IF chain. The 65-nm transmitter (1836.119) includes a fractional-N synthesizer, IF amplifiers, and up-conversion mixer, operating between 208-255 GHz. On-chip antennas are used for both transmitter and receiver (1836.122). The chips are demonstrated in a rotational spectroscopy setup (1836.126). (1836.147, PI: W. Choi, UT Dallas, 1836.122, PI: R. Henderson, UT Dallas, 1836.119, PI: K. O., UTD, 1836.126, PI: F. De Lucia, OSU (Ohio))
Security and Safety (Test)	In semiconductor manufacturing, wafer-level testing is lengthy and expensive particularly for Analog/RF ICs. An adaptive test cost reduction method has been developed which optimizes the test flow per process signature, allowing a reduction of test time. This has been demonstrated using industrial datasets for RF transceivers. Up to a 30% test cost reduction has been achieved using the adaptive flow. (1836.131, PI: Y. Makris, UT Dallas)
Security and Safety (Circuits)	Tight synchronization of a distributed array with widely-spaced sparse elements is a key enabler for coherent high-resolution imaging and radar systems. A 50-GHz wireless impulse receiver with an on-chip antenna has been demonstrated for synchronization with sub-ps timing accuracy. (1836.135, PI: A. Babakhani, Rice)



# TASK 1836.119, DEMONSTRATION OF 180-300 GHz TRANSMITTER FOR ROTATIONAL SPECTROSCOPY

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## SIGNIFICANCE AND OBJECTIVES

As part of the effort to help open up the high millimeter and sub-millimeter wave frequency range for moderate volume and cost applications, this task is seeking to demonstrate a 180-300 GHz transmitter in CMOS for a rotational spectrometer that can be used to detect harmful molecules in air and to analyze breaths.

## TECHNICAL APPROACH

The transmitted power should be ~10-100 uW. The main challenges are increasing the output frequency range, power, and frequency for phase locked signals. To realize a fast scan rate with a 10-kHz step, a fractional-N synthesizer is used. The synthesizer also incorporates a frequency modulation function. The output signal generation uses a combination of an N-push technique and frequency multiplication/translation techniques. This task will also help generating the receiver LO signal.

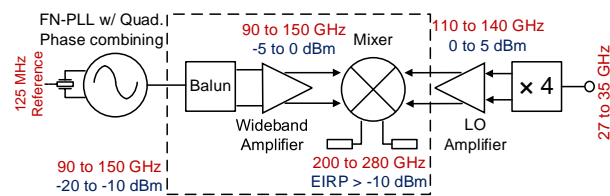


Figure 1: Block diagram of transmitter with power and frequency plans

## SUMMARY OF RESULTS

A 200-280 GHz RF front-end of transmitter (dotted box in Fig. 1) is demonstrated in 65-nm CMOS. The power and frequency plans for the transmitter are also shown in Fig. 1. As the output power requirement is not high and wideband amplification at 90-150GHz is challenging, it is better to use a mixer rather than a frequency multiplier. Compared to self-mixing in a doubler one of the mixing terms (LO), can be generated at higher power over a narrower bandwidth, resulting in a higher conversion gain and power efficiency, especially when the IF input power is low. The mixer based system also helps in scanning, as coarse and fine steps can be split between LO and IF, as well as, filling in frequency gaps sometimes present in broadband VCO's by using LO frequency tuning.

Saturated EIRP of TX front-end is greater than -5dBm over a frequency range of 60GHz. When the input power is -20dBm, EIRP is greater than -10dBm, and achieves percent 3-dB and 6-dB bandwidths of 24% and 33%. The

front-end was integrated with a fractional-N synthesizer to form a transmitter operating at 208-255GHz with EIRP of -18 to -11dBm. The integrated transmitter including a synthesizer is locked at 208 to 255GHz. The measured EIRP and phase noise of the transmitter are also shown in Fig. 2. The transmitter IC mounted in a printed circuit board (Fig. 3) and a CMOS receiver are used in a rotational spectroscopy setup to detect ethanol in human breaths.

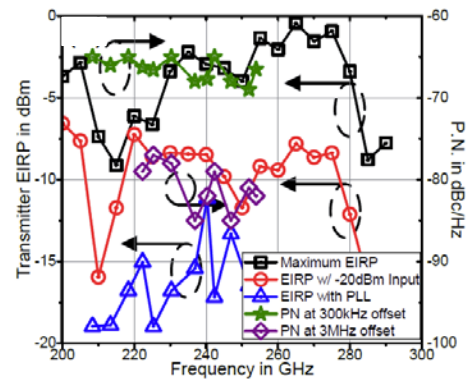


Figure 2: EIRP of transmitter front end (amplifier-mixer chain) and complete TX

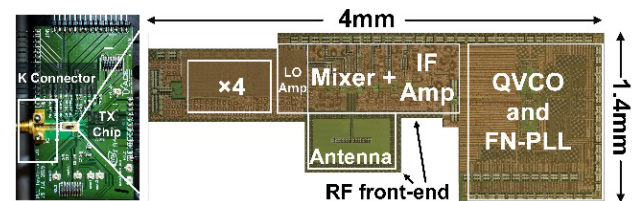


Figure 3: Die Photo and PCB for spectroscopy

**Keywords:** rotational spectrometer, transmitter, CMOS, millimeter-wave

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

- [1] J. Zhang et al., "85-to-127-GHz CMOS Signal Generation using a Quadrature VCO with Passive Coupling and Broadband Harmonic Combining for Rotational Spectroscopy," IEEE Journal of Solid State Circuits, vol. 50, no. 6, pp. 1361-1371, June 2015.
- [2] N. Sharma et al., "200-280GHz CMOS RF Front-End of Transmitter for Rotational Spectroscopy," Accepted to 2016 IEEE Symposium on VLSI Circuits, May 2016.



# TASK 1836.120, EVALUATION OF FREQUENCY AND NOISE PERFORMANCE OF CMOS 180 – 300 GHZ SPECTROMETER TRANSMITTER AND RECEIVER COMPONENTS

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## SIGNIFICANCE AND OBJECTIVES

A gas phase absorption spectrometer in the 100 to 1000 GHz frequency range would be extremely valuable to rapidly and precisely assay a wide range of chemical vapors. This project's objective is to quantitatively evaluate passive materials and passive and active devices for suitability as millimeter-wave components to be integrated into a spectrometer system.

## TECHNICAL APPROACH

In the past year, this project undertook: (1) construct and validate a numerical model to extract millimeter-to-submillimeter wave complex index of refraction values as a function of frequency from measured reflection and transmission data on various dielectric materials of interest; and (2) set-up of the Fourier transform spectrometer to measure the frequency spectrum of CMOS oscillators broadcasting into free-space.

## SUMMARY OF RESULTS

In collaboration with Dr. Rashaunda Henderson and Dr. Sam Shichijo, we have taken detailed high-resolution reflection and transmission data across a broad range of frequencies on various dielectric materials of interest to millimeter- and sub-millimeter wave circuits, including benzocyclobutene (BCB), polyethylene naphthalate (PEN), and the photoresist SU8. We also constructed a numerical model to solve the simultaneous non-linear equations relating the measured data to the real and imaginary parts of the index of refraction at each frequency. An example of an extracted complex index of refraction spectrum for BCB is shown in Fig. 1. In the design and simulation of high-frequency circuits using dielectric materials, the information is critical but are nearly absent in the literature or materials databases across this frequency regime.

In collaboration with Zeshan Ahmad and Dr. Ken O, we adapted the Fourier transform spectrometer (FTS) to measure the free-space broadcast spectrum of an advanced CMOS multiplier circuit across a broad frequency range. A significant difficulty was that the multiplier circuit was unpackaged. Consequently, the input signal at  $f_0$  as well as all DC biases must be brought on chip using external probes. To accommodate this, we designed and constructed a suitable ad hoc probe station at the FTS external input.

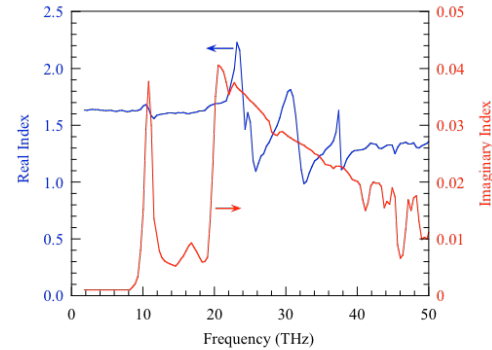


Figure 1: Modeled real (blue) and imaginary (red) index of refraction of the BCB from FTS reflection and transmission measurements across a broad range of frequencies

Fig. 2 shows the spectrum of a 420 to 980 GHz multiplier. The FTS can capture not just the desired output frequency, but also a full range of harmonics. In this way the efficiency of the multiplier can be tested – how much output at non-desired harmonics is suppressed.

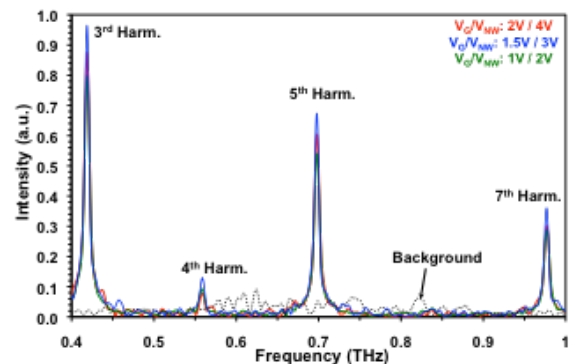


Figure 2: Broadband free-space output spectrum of a 420 to 980 GHz multiplier oscillator circuit (unpacked) as measured on a terahertz Fourier transform spectrometer

**Keywords:** millimeter-wave, terahertz, spectrometer, dielectric loss, power meter

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] Z. Ahmad, M. Lee, K. K. O, "1.4THz, -13dBm-EIRP Frequency Multiplier Chain Using Symmetric- and Asymmetric-CV Varactors in 65nm CMOS", Proc. of 2016 IEEE ISSCC, (2016).



# TASK 1836.122, ON-CHIP INTEGRATION TECHNIQUES FOR 180-300 GHz SPECTROMETERS

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## SIGNIFICANCE AND OBJECTIVES

The objectives of this work are to develop techniques to integrate broadband antennas with RFICs for a 180-300 GHz CMOS-based spectrometer demonstration.

## TECHNICAL APPROACH

The technical approach includes the development of fabrication processes to integrate broadband antennas with standard processed CMOS ICs; and characterization of those antennas and co-development of broadband on-chip antennas. In addition two approaches to characterize the antennas have been pursued, one method uses a standard technique with a near-field scanner and the other involves Fourier transform infrared (FTIR) spectroscopy.

## SUMMARY OF RESULTS

Monolithic and hybrid standalone antennas were fabricated in the UT Dallas cleanroom using multilayer polymers process and thin-film metal. The standard antenna measurement scanner consists of a transmitting antenna under test (AUT) connected to the RF source and a receiving antenna connected to a power meter. The antenna testing system at UT Dallas fixes the AUT while the probe antenna moves. The system is manufactured by NSI and consists of a stepper motor system that will cover the sphere in the near or farfield of the AUT and provide the step size of +/- 1 degree up to 500 GHz. The antennas designed for the 180-300 GHz system require RF probes for measurement given that their physical size and the wavelength are on the order of millimeters. It is difficult to measure the AUT with an RF probe which also resembles an AUT with ground-signal-ground metal probe.



Figure 1: (Left) 180-300 GHz hybrid CPW fed modified bowtie antenna with probe; (Right) 280 GHz microstrip patch

One method of characterizing antennas in the submillimeter wave range is by FTIR spectroscopy. This technique measures the frequencies at which the

antennas absorb radiation similar to return loss measurements. In this case the antenna must be terminated in its internal impedance. The aperture bowtie antenna has been designed to have a 50 ohm input impedance so the fabricated antennas have to be terminated using thin film tantalum nitride resistors. The terminated aperture bowtie is being characterized with a Bruker Vertex 80v FTIR reflectance measurement.

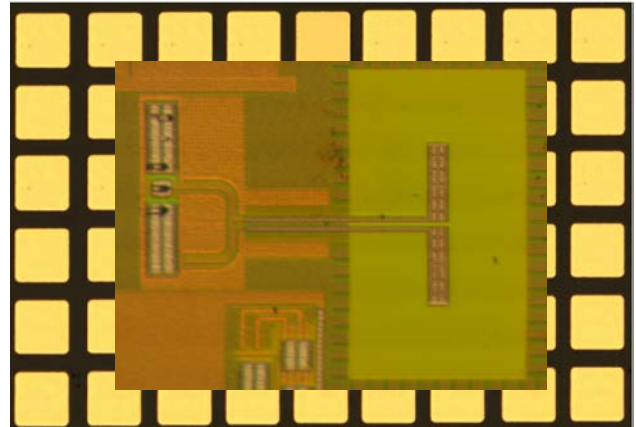


Figure 2: 200 GHz on-chip dipole antenna with AMC substrate to facilitate broad bandwidth

The spectrometer demonstrator, a receiver frontend circuit with an on-chip dipole antenna was fabricated using a 65 nm UMC technology. To increase the bandwidth (BW) of the dipole and in collaboration with K. K. O's group, a phase compensated artificial magnetic conductor (PC-AMC) was fabricated on a SU-8/FR408 substrate using an array of 30 um x 30 um Au structures with 10 um spaces. Figure 2 shows the standalone antenna with AMC substrate that provided 95 GHz BW.

**Keywords:** aperture antennas, patch antennas, artificial magnetic conductors reflection plane

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

- [1] R. Henderson et al., "Millimeter-wave performance of broadband aperture antenna on laminates," *Antenna Measurement & Techniques Association Conference*, Long Beach, CA 2015.
- [2] Q. Zhong, W. Choi, C. Miller, R. Henderson, K. O., "210-305 GHz CMOS receiver for rotational spectroscopy," *International Solid-State Circuits Conf.*, San Francisco, CA 2016.

# TASK 1836.126, DESIGN SPIN REDUCTION VIA INTEGRATED THZ DESIGN: APPLICATIONS, PHYSICS, AND SYSTEM ENGINEERING

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## SIGNIFICANCE AND OBJECTIVES

The objective of this project is to develop a THz System Engineering Tool that allows for analysis of systems based on the characteristics of their building blocks and to validate it by applications to systems of interest. These systems include CMOS gas sensors and systems for process diagnostics and control.

## TECHNICAL APPROACH

This effort includes: (1) Diagnostics and process control in semiconductor plasma reactors, and (2) in parallel the development of CMOS systems for this application, as well as more generally for gas sensors. We are also developing a computational System Evaluation Tool to aid in the design of these CMOS circuits.

## SUMMARY OF RESULTS

Our work has focused on two main areas: (1) System design simulations for CMOS Tx/Rx fabrication at UT-D (and testing and evaluation of the Tx/Rx at OSU), and (2) Spectroscopic diagnostics for semiconductor reactor plasmas with Applied Materials. It is desirable in an Rx that the noise limit come from the input to the first iF amplifier. This requires enough IF gain so that this noise dominates the noise in later stages.

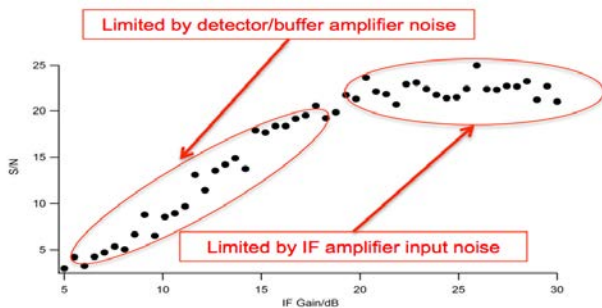


Figure 1: Signal to noise for a spectrum as a function of IF gain

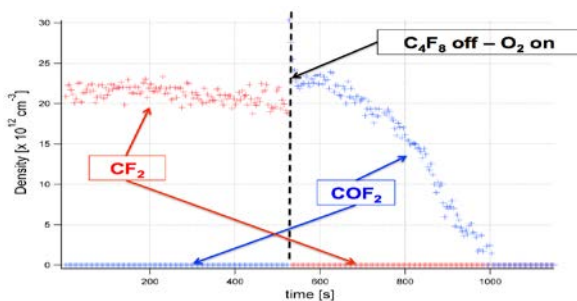


Figure 2: Spectroscopic monitoring of a cleaning cycle

However, if this gain is too large, the dynamic range of the system is reduced. Figure 1 shows this effect.

CHF <sub>4</sub> Flow On	Global Fit Results	
Pressure Gauge (mtorr)	Pressure (mtorr)	Rot. Temp. (K)
0.4 - 0.5	0.257	255.006
1.1 - 1.2	1.037	291.682
2.1 - 2.2	2.019	296.681
3.1 - 3.2	2.901	294.548
4.1	3.815	295.444
5.0	4.737	296.457
5.9 - 6.0	5.845	294.213
6.9	6.780	294.662
7.7 - 7.8	7.683	294.730
8.7	8.516	293.885
9.6	9.427	294.247
10.3 - 10.5	10.352	294.721
11.3	11.288	295.584
12.1 - 12.3	12.179	295.708
13.0 - 13.1	13.007	295.442
13.7 - 13.9	13.946	296.215

In plasma diagnostics, Both line-shapes and relative line strengths contain information about number density and temperature. The Table shows the excellent agreement between spectroscopic results and conventionally measured values. Figure 2 shows spectroscopic monitoring of the condition of the

reactor surfaces. For the first 500 seconds a C<sub>4</sub>F<sub>8</sub> plasma was run and one of its reaction products, CF<sub>2</sub>, was monitored. At the end of this period, the C<sub>4</sub>F<sub>8</sub> flow was turned off and an O<sub>2</sub> cleaning plasma struck. This figure shows that the C<sub>4</sub>F<sub>8</sub> residue persisted for about another 500s.

**Keywords:** terahertz, spectroscopy, plasmas

## INDUSTRY INTERACTIONS

Applied Materials, Texas Instruments, IBM, Intel

## MAJOR PAPERS/PATENTS

- [1] Helal et al., "In situ measurements of the abundances and temperatures of the constituents of semiconductor manufacturing plasmas via terahertz absorption spectroscopy: comparison with theoretical models," 62<sup>nd</sup> American Vacuum Society Symposium and Exhibition.
- [2] De Lucia, F. C.. "Submillimeter Studies of Molecular Plasmas: Applications to Semiconductor Plasma Processing," (Invited) 62<sup>nd</sup> American Vacuum Society Symposium and Exhibition.
- [3] Helal, et al., "Submillimeter absorption spectroscopy in semiconductor manufacturing plasmas and comparison to theoretical models," International Symposium on Molecular Spectroscopy.

# TASK 1836.131, PROCESS VARIATION ANATOMY: A STATISTICAL NEXUS BETWEEN DESIGN, MANUFACTURING & YIELD

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## SIGNIFICANCE AND OBJECTIVES

In semiconductor manufacturing, wafer-level testing is a lengthy and expensive procedure particularly for Analog/RF integrated circuits. We proposed a methodology to optimize the test flow of every wafer according to its process signature, in order to reduce the test cost. In this method, process signature of a given wafer is extracted through e-test measurement, then the optimized test flow will be selected and applied to the wafer during probe measurements.

## TECHNICAL APPROACH

We developed an adaptive test cost reduction method, which optimizes the test flow per process signature. Indeed, depending on how a wafer has been impacted by process variations, the wafer may go through complete test flow or a reduced test flow in order to lower the probe test time. A reduced test flow is a subset of complete test flow in which some of test groups are eliminated. The proposed technique is based on the following principles, in order to be readily deployable with minimal test operations support: i) The granularity at which test elimination decisions are made is at the test group level rather than test item, ii) The granularity of the adaptation decision is at the wafer-level, i.e., all die on a wafer are subjected to the same test flow, iii) The decision has to be driven by a signature which reflects how process variations have affected a particular wafer, and iv) The decision has to be available prior to insertion of the wafer in the probe station and cannot be informed by measurements taken at probe. Fig. 1 depicts an overview of our proposed methodology.

The first step is to identify appropriate subset of test groups which could potentially be applied to a wafer. Since our target device has 10 test groups, an exhaustive search is employed to generate all possible subset of complete test flow as reduced test flows.

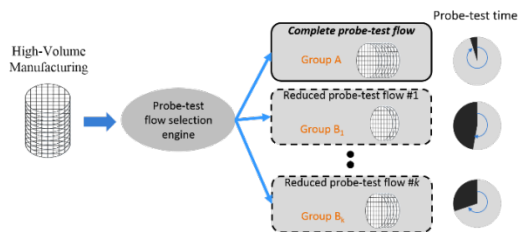


Figure 1: Wafer-level probe-test flow selection

The next step is to extract process signature from e-test measurements. E-test data contains many types of

parameters, mainly focusing on simple physical/electrical characteristics reflecting the position of a wafer in the process space. Therefore, prior to crafting a wafer signature based on the e-tests, we apply a non-linear dimensionality reduction algorithm to map e-test data onto lower count of dimension. Finally, for each process signature, we need to assign an appropriate test flow such that we maximize test cost reduction while retaining the test escape rate below a target Defective Parts Per Million (DPPM) level. To accomplish this, we proposed an optimization algorithm based on integer linear program (ILP). The output of optimization algorithm determines optimized probe-test flow for each process signature.

## SUMMARY OF RESULTS

We evaluate the effectiveness of our proposed methodology using industrial dataset of an RF transceiver. Fig. 2 demonstrates the test cost vs. test quality trade-off for various DPPM levels. The horizontal axis is the target DPPM level (arbitrary unit). It varies from single digit DPPM to a few hundred. The vertical axis shows the percentage of test cost reduction. As it can be seen, the adaptive nature of the proposed test flow selection enables the exploration of test cost vs. test quality even for very low DPPM levels.

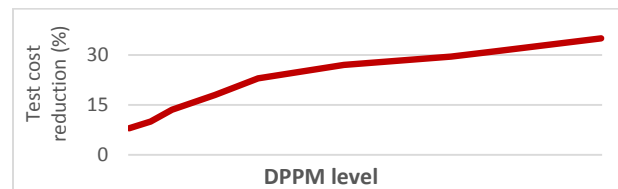


Figure 2: Test cost reduction vs. test accuracy

**Keywords:** process signature, test cost reduction, test flow optimization, test escape rate

## INDUSTRY INTERACTIONS

Texas Instruments, Intel, GlobalFoundries

## MAJOR PAPERS/PATENTS

- [1] A. Ahmadi, A. Nahar, B. Orr, M. Pas, and Y. Makris, "Wafer-Level Process Variation-Driven Probe-Test Flow Selection for Test Cost Reduction in Analog/RF ICs," IEEE VLSI Test Symposium, 2016.
- [2] A. Ahmadi, C. Xanthopoulos, A. Nahar, B. Orr, M. Pas, and Y. Makris, "Harnessing Process Variations for Optimizing Wafer-level Probe-Test Flow," submitted to IEEE International Test Conference, 2016.

# TASK 1836.135, SUB-PICOSECOND SYNCHRONIZATION OF WIDELY SPACED IMAGING ARRAYS

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## SIGNIFICANCE AND OBJECTIVES

Tight synchronization of a distributed array with widely-spaced sparse elements is a key enabler in coherent combining of signals in space. The objective of this project is to build a wireless synchronization link capable of synchronizing a master node to multiple slave nodes with timing jitter of 500fsec in less than 10nsec.

## TECHNICAL APPROACH

To achieve wireless synchronization with sub-picosecond accuracy, we have designed and fabricated an impulse receiver based on self-mixing technique to detect picosecond impulses and to extract their repetition rate with a low timing jitter. When a broadband Gaussian-modulated frequency comb is passed through a nonlinear block, realized by a single-transistor mixer, different frequency tones mix with each other and produce the repetition tone at the output. The receiver also includes an input amplifier chain at 50 GHz, tunable baseband amplifiers for the repetition rate, and is implemented with a broadband on-chip antenna so that it can detect ultra-short pulses.

## SUMMARY OF RESULTS

The overall architecture of the impulse receiver is illustrated in Fig. 1. The broadband pulses are received by an on-chip bowtie antenna, and amplified in U-band. A bipolar transistor produces the repetition rate from the received frequency tones and the synchronized clock is amplified using a tunable baseband amplifier, made by switches and varactors.

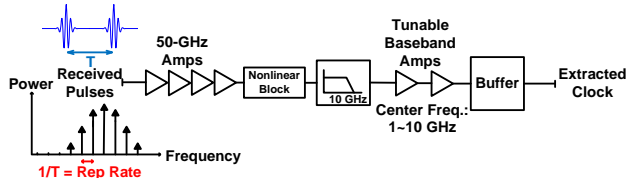


Figure 1: Architecture of the ultra-short impulse receiver

The receiver was fabricated in IBM 0.13 $\mu$ m SiGe BiCMOS process [1]. A custom-designed picosecond pulse radiating chip was used to test the performance of the receiver. The test setup and measurement results in time and frequency domains are shown in Fig. 2. The output of the receiver has an rms timing jitter of 1 ps. This is the first time that picosecond pulses, radiated and detected by silicon chips, have been used to demonstrate sub-psec wireless time transfer.

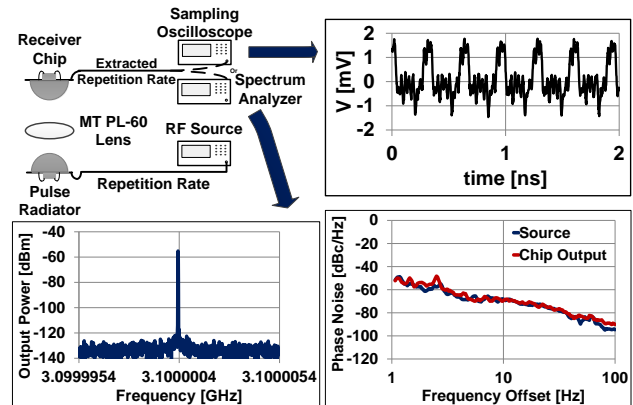


Figure 2: Time-domain and frequency-domain measurement results of the wireless time transfer setup using radiated picosecond pulses

The chip photo is shown in Fig. 3. It occupies an area of 1.89 mm<sup>2</sup> and draws 146 mW of power from a 2.5V power supply.

To achieve an even better timing accuracy in the synchronized signal, an alternate receiver that detects pulse repetition rate by injecting it to a divide-by-eight frequency divider is designed. This architecture is designed in Globalfoundries 65nm CMOS process along with an impulse sampler and is going to be tested in the following year. The chip layout is shown in Fig. 3.

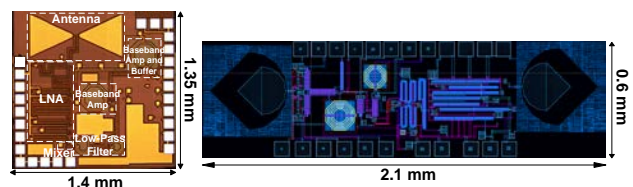


Figure 3: Chip micrograph of the mixer-based impulse receiver (left), and layout of the designed injection-locking-based receiver (right)

**Keywords:** wireless time synchronization, millimeter-wave, low-noise receiver, ultra-short pulses, biCMOS integrated circuits

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] B. Jamali and A. Babakhani, "Sub-picosecond Wireless Synchronization Based on a Millimeter-Wave Impulse Receiver with an On-chip Antenna in 0.13m SiGe BiCMOS," IEEE MTT-S Int. Microwave Symp. , May 2016.



# TASK 1836.147, DEMONSTRATION OF 180-300 GHz RECEIVERS FOR ROTATIONAL SPECTROSCOPY

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## SIGNIFICANCE AND OBJECTIVES

Sub-mm-wave rotational spectroscopy enables detection of gas molecules with absolute specificity. One of the key building blocks for affordable rotational spectrometers is a CMOS transceiver. Since the transmitter power is limited up to only 100  $\mu$ W to prevent saturation, highly sensitive receivers are required. In this task, the development of wideband integrated receivers for rotational spectrometers will be investigated.

## TECHNICAL APPROACH

A highly-integrated and wideband receiver is proposed and fabricated in a 65-nm CMOS process. The receiver is based on a sub-harmonic passive mixer using an NFET-based APDP. A 120-GHz LO driver chain and a 20-GHz IF low noise amplifier followed by an AM detector are co-designed and integrated with the mixer to improve sensitivity. A wideband hybrid for RF/LO/IF combining and isolation is proposed and designed. Integration and co-optimization of wideband radiators is also investigated. The performance of the receiver is evaluated both in radiation measurements and actual spectrometer system.

## SUMMARY OF RESULTS

Figures 1 and 2 depict the block diagram and the chip die photograph of the wideband receiver fabricated using a 65-nm CMOS process, respectively.

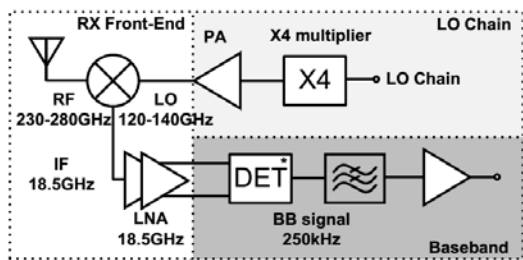


Figure 1: Block diagram and circuit schematic of the wideband (230-280 GHz) receiver for rotational spectroscopy

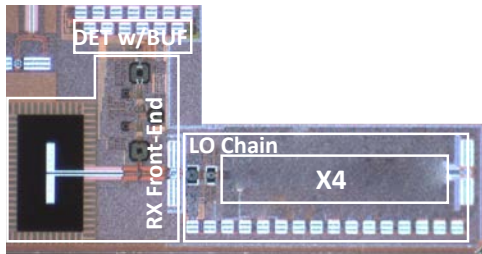


Figure 2: Photograph of the receiver in 65-nm CMOS process

The fabricated RX is mounted on a low-cost PCB. From radiation measurements, it is found that the RX exhibits responsivity of 400-1200  $\text{kV/W}$  and noise equivalent power of 0.4 to 1.2  $\text{pW/VHz}$  from 225 to 280 GHz. The RX is evaluated in a rotational spectroscopy system at the Ohio State University (Prof. Frank De Lucia). The setup for the spectrometer experiments using the fabricated receiver (RX DUT) and commercial off-the-shelf transmitter from Varginia Diode Inc. (VDI) is shown in the Figure 3. Multiple gas molecules are characterized using the setup to demonstrate the capability of receiver. Figure 4 shows measured spectrum of 5.2mTorr Ethanol. EtCN and Acetone contamination, which has significantly lower concentration than Ethanol, is also detected.

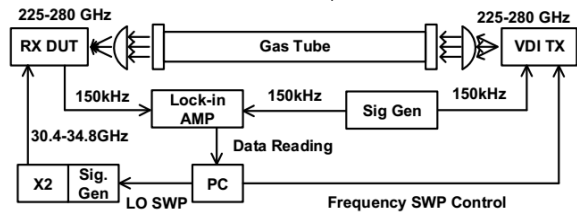


Figure 3: Measurement setup for rotational spectroscopy experiment using the receiver (RX DUT)

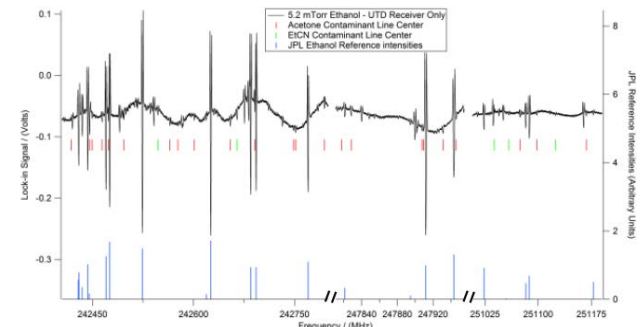


Figure 4: Measured spectrum of 5.2mTorr Ethanol with EtCN and Acetone contamination

**Keywords:** integrated receiver, on-chip radiator, passive mixer, rotational spectroscopy, wideband receiver

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

- [1] Q. Zhong *et al.*, "A 210-to-305GHz CMOS receiver for rotational spectroscopy," IEEE ISSCC, Jan., 2016, San Francisco, CA, USA.
- [2] Q. Zhong *et al.*, "225-280GHz Receiver for Rotational Spectroscopy," IEEE RFIC, May, 2016, San Francisco, CA.



# TASK 1836.150, ROBUST HIGH RESOLUTION TECHNIQUES FOR MILLIMETER WAVE RADARS IN COMPLEX ENVIRONMENTS

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## SIGNIFICANCE AND OBJECTIVES

This task focuses on developing robust high resolution estimation techniques for millimeter wave imaging in complex surroundings. While developing the high resolution techniques computational cost reduction is also emphasized.

## TECHNICAL APPROACH

Adaptive algorithms which modify their behavior according to changing surroundings of the vehicle need to be used for the high resolution imaging to work in dynamic multipath environments. This implies that the imaging algorithm should use spatial and temporal filters which adapt to the level of clutter in the system.

## SUMMARY OF RESULTS

Along with the reflections from the objects to be imaged, additional reflections may be received from the unwanted objects which is known as clutter. Following equations shows implementation of adaptive filter using an FMCW radar. The filter operates in Doppler and angular domains. Let us first consider multidimensional data obtained across time and aperture

$$d(l, n, p) \approx \sum_1^Q \rho_q e^{j2\pi \left[ \frac{(K\tau_{lq} + f_{dq})n}{f_s} + f_c \tau_{ql} + pT f_{dq} \right]}$$

where  $f_{dq}$  is the Doppler shift and  $\tau_{lq} = \frac{2R_q + ld \sin \theta_q}{c}$  contains the direction of arrival information about the  $q^{\text{th}}$  target. Once the data are acquired the noise correlation  $R_{nn}$  is found calculating the clutter across range bins in which a target is not present. Fig. 1 shows how the data are filtered using the adaptive noise filter.

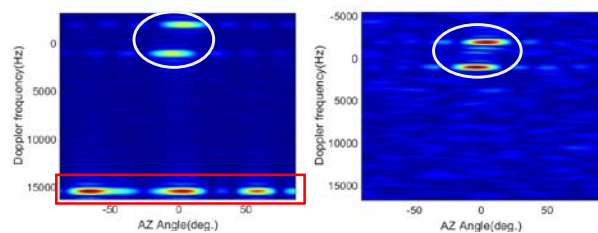


Figure 1: Azimuth-Doppler plot of system with clutter (left) and clutter removed with adaptive filter (right)

Now to increase the directional capability of the system we propose to use multiple transmit and receive antenna elements. With the simultaneous transmission of orthogonal waveforms from many transmitters effective

size of antenna array is increased. We verify this scheme by implementing time division multiplexing which is demonstrated in Fig. 2. Other multiple transmit antenna schemes include use of random phase shifts, orthogonal time frequency ramps, etc.

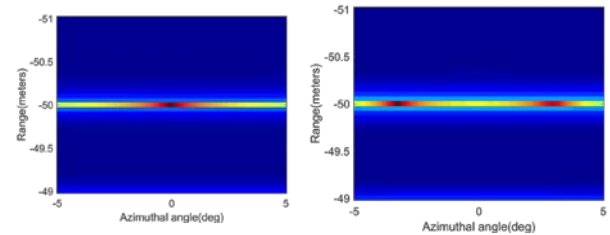


Figure 2: A scheme using single transmit antenna (left) which cannot resolve closely spaced targets; limitations are overcome using multiple transmit antennas (right)

In addition to making estimation techniques robust, their complexity is reduced using techniques such as beamspace projection and compressive sensing. The implementation complexity of beamspace algorithms is analyzed in depth to estimate exact computational savings. As simple Fourier transform makes the observation subspace sparse (also seen from both figures objects are present only in certain locations), compressive sensing principle and minimization recovery algorithms can be applied.

Moreover, while imaging the mobile targets, tracking them using sophisticated algorithms such as extended Kalman filter can help in reducing estimation errors. The tracking algorithm is verified for two dimensional position of the targets. We propose to use different multiple transmit receive antenna schemes along with complexity reduction techniques which will make an imaging system implementable and robust. An overview of the related algorithms used in Automotive radars has been presented in [1].

**Keywords:** mm-wave imaging, space time adaptive processing, MIMO radar, clutter reduction

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] S. Patole, M. Torlak, D. Wang and M. Ali, "Automotive Radars: A Review of Signal Processing Techniques," IEEE Signal Processing Magazine, May 2016, submitted.

# TASK 1836.152, FEASIBILITY OF CMOS TRANSMITTER AND RECEIVER FOR 500-GBPS COMMUNICATION OVER DIELECTRIC WAVEGUIDE

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## SIGNIFICANCE AND OBJECTIVES

The increasing bandwidth of silicon integrated circuits technology is enabling a waveguide interconnection system using sub-millimeter waves that can support communication at 500-Gbps and higher. If successful, this technology will provide a bandwidth approaching that of optical systems, while bypassing the photonic component integration and coupling/packaging challenges of optical systems.

## TECHNICAL APPROACH

This project in conjunction with the efforts on developing transitions and dielectric waveguides will investigate the feasibility of 500 Gbits/sec electronic communication over a 1-m dielectric waveguide using circuits fabricated in 65-nm CMOS. Use of a combination of frequency division multiple access (FDMA) (Five frequency channels), polarization division multiple access (PDMA) and a higher order signal modulation scheme will be investigated. To demonstrate the feasibility, a 120-Gbps demonstration circuit incorporating two frequency bands and two polarization modes will be implemented. Based on the results, implementation plans for a 500-Gbps dielectric waveguide communication system will be formulated.

## SUMMARY OF RESULTS

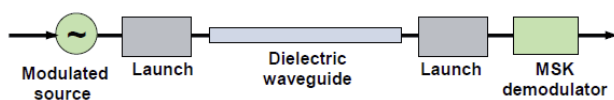


Figure 1: Conceptual diagram of the dielectric waveguide communication system

Figure 1 shows a conceptual diagram of the dielectric waveguide system. It consists of transmitter, a transition/launch from the transmitter to a waveguide, a waveguide, a transition/launch from a waveguide to a receiver, and a receiver.

Table 1: Channels of the dielectric waveguide communication system

	Center Frequency (GHz)		Center Frequency (GHz)
Channel 1 (P1)	180 (157.5-202.5)	Channel 2 (P2)	180 (157.5-202.5)
Channel 3 (P1)	225 (202.5-247.5)	Channel 4 (P2)	225 (202.5-247.5)
Channel 5 (P1)	270 (247.5-292.5)	Channel 6 (P2)	270 (247.5-292.5)
Channel 7 (P1)	315 (292.5-337.5)	Channel 8 (P2)	315 (292.5-337.5)
Channel 9 (P1)	360 (337.5-382.5)	Channel 10 (P2)	360 (337.5-382.5)

Table 1 summarizes the channel assignment. The system

uses 5 frequency bands supporting two polarization channels for a total of 10 channels.

Table 2 lists key assumptions/targets and summarizes the link margin analysis for 30-Gbps 1-m communication over a channel (1 frequency channel with a given polarization). These assumptions are being verified and updated by simulation studies using a 65-nm CMOS process as well as the measurement results from Tasks 1836.147 and 1836.119 investigating the transmitter and receiver for rotational spectroscopy applications. Power generated by the transmitter of -8 dBm and receiver noise figure of 20 dB appear to be possible. Including 3-dB losses for multiplexers, link margin of ~8 dB is projected.

Frequency (THz)	0.18 to 0.36	Received power (dBm)	-23.5
Range (m)	1	Thermal noise density (dBm/Hz)	-174
TX power to transition (dBm)	-8	Noise figure of receiver (dB)	20
Propagation loss	2.5	Bandwidth (bits/s (dB-Hz)) 30Gbps	105
RX transition loss (dB)	3.5	$E_b/N_0$ (BER of $1 \times 10^{-10}$ ) (dB)	15.8
RX multiplexer loss (dB)	3.0	Sensitivity (dBm)	-33.2
TX transition loss (dB)	3.5	Link margin (dB)	9.7
TX combiner loss (dB)	3.0		

Table 2: Link margin analyses and key performance targets

The transmitter and receiver architectures as well as specifications of sub-blocks have been finalized, and transmitter and receiver prototypes operating around 300GHz are being designed for fabrication using a 65-nm CMOS process. In addition, test strategies for the transmitter and receiver including developing an IC implementation of modulated signal generator have been formulated and being implemented.

**Keywords:** dielectric, waveguide, communication, sub-millimeter, waves

## INDUSTRY INTERACTIONS

Texas Instruments, Intel

## MAJOR PAPERS/PATENTS

[1] Z. Ahmad, I. Kim, and K. K. O, "0.39-0.45THz Symmetric MOS-Varactor Freq. Tripler in 65-nm CMOS," 2015 IEEE RFIC Symposium, May 2015, Phoenix, AZ.

[2] Z, Ahmad and K. K. O, "0.65-0.73THz Quintupler with an On-Chip Antenna in 65-nm CMOS," 2015 IEEE VLSI Symp. on Circuits, pp. C310-C311, June 2015, Kyoto, Japan.

[3] N. Sharma and K. K. O, "160–310 GHz Frequency Doubler in 65-nm CMOS with 3-dBm Peak Output Power," Accepted to 2016 IEEE RFIC Symposium, San Francisco, CA.

# TASK 1836.155, DEVELOPMENT OF WIDE-BAND VIBRATION SENSORS BASED ON TEXAS INSTRUMENTS EXISTING PROCESS PLATFORMS

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## SIGNIFICANCE AND OBJECTIVES

The objective of this research is to design, implement, characterize and optimize a very low power consuming chip-scale vibration sensor that can operate over a wide range of frequency from DC to 10kHz with a resolution of 1mg or better.

## TECHNICAL APPROACH

The aim of this research is to realize vibration sensors using CMOS processed chips without adding any extensive modifications to an existing CMOS process platform. The plan is to utilize a CMOS processed, thinned-down electronic chip as the mechanical component itself which would respond to vibrations in the form of bending that would influence the tensile and compressive stresses on different locations of the chip. These stresses can be then detected by placing a highly piezoresistive coefficient material at the maximum stress locations.

## SUMMARY OF RESULTS

Fabricated CMOS chips were thinned down to  $\sim 70\mu\text{m}$  using a maskless Deep Reactive Ion Etch (DRIE) process to enhance the effect of the stress on the piezoresistors. A bulky mass made of solder wire was then attached to the edge of the CMOS chip using a highly adhesive glue. By changing the magnitude of the mass from the edge of the chip, the sensitivity and the resonance frequency could be modulated within a certain range. The chip was attached to the edge of a stiff object as shown in Figure 1. To measure the effect of vibration on the CMOS chip, a speaker/sub woofer was used to create sinusoidal vibrations at different frequencies using a PC. An off-the-shelf commercial Analog Devices vibration sensor (ADIS 16228) was used to measure the amplitude of the generated vibrations. The change of the output voltage across the piezoresistors, designed in a Wheatstone bridge fashion, were recorded for vibrations at 50Hz-400Hz. Three variations of the CMOS chips with different chip thicknesses/solder mass combinations were tested and characterized. Figure 2 illustrates the resonance response of the three sensors. A parallel operation of the three chips would enable a 0-400 Hz wideband vibration sensor with at least a 10mV/g sensitivity. Table 1 summarizes the resonance frequencies and sensor bandwidth for the three different cases.

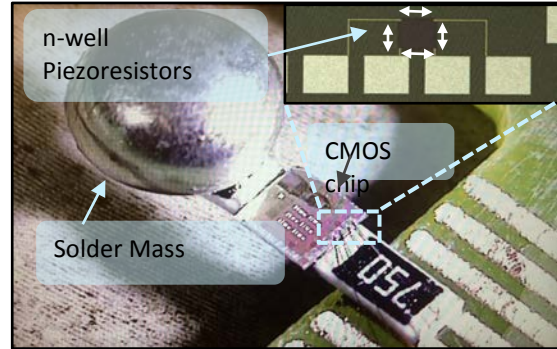


Figure 1: Test setup for the CMOS chip

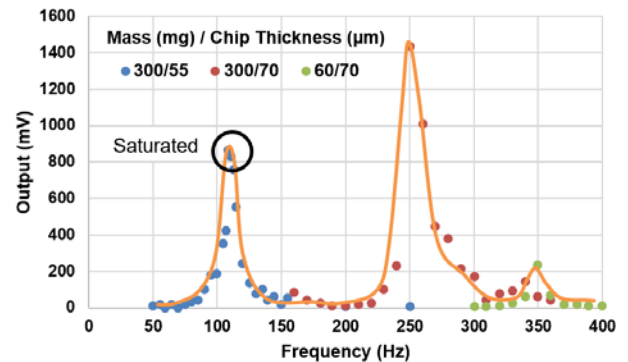


Figure 2: Resonance response obtained from the three chips for vibrations in the 0-400Hz range

Table 1: Summary of the three device characterizations

Solder Mass (mg)/ Chip Thickness ( $\mu\text{m}$ )	Resonance Frequency (Hz)	Bandwidth ( $>10\text{mV/g}$ Sensitivity)
300/55	110	0-175
300/70	250	140-360
60/70	350	315-400

**Keywords:** high sensitivity, vibration sensor, low power, CMOS MEMS, wide-band

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1]. V. Qaradaghi, M. Mahdavi, A. Ramezany, and S. Pourkamali, "MEMS Resonant Sensors for Real-Time Thin Film Shear Stress Monitoring", In Press, IFCS 2016.

# TASK 1836.156, TRANSITION DESIGN FOR HIGH DATA RATE LINKS AT SUBMILLIMETER WAVE FREQUENCIES

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## SIGNIFICANCE AND OBJECTIVES

This project focuses on the design of interface components and multiplexers for the development of 500 Gbps communication links using a 1m fiber in collaboration with those who are completing the IC transceiver design (by O) and polymer-based fiber development (by MacFarlane).

## TECHNICAL APPROACH

The approach focuses on designing a multilayer PCB-based waveguide to transition the transceiver signal from the IC to a dielectric fiber. In addition five transceiver circuits covering bands from 180 to 360 GHz have to be combined through a multiplexer circuit to feed into the waveguide. The single output will be fed into an antenna that will excite the waveguide and transfer the signal through the 1m fiber.

## SUMMARY OF RESULTS

Results include the fabrication and characterization of a 3-7 GHz rectangular waveguide (RWG) assembled using 30 printed circuit board (PCB) layers that are 1.78 mm thick. This design adopted PCB techniques used to form substrate integrated waveguide (SIW). Solid metal in the PCB is used to define the horizontal walls of the SIW. The vertical walls of waveguide are defined by single layer vias spaced shorter than  $0.05 \times \text{wavelength}$  of the highest operating frequency and fabrication requirements. This method is used to construct a typical RWG defined where  $a=2b$ , but is not directly metallized on all sides.

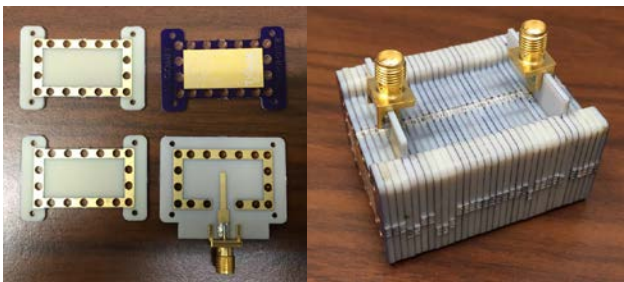


Figure 1: Printed circuit board RWG assembled with 30 layers of FR408 to create a single waveguide

Simulated and measured performance agree well such that the cutoff frequency defined by the cross-section of the dielectric RWG matches. The signal representing the single broadband transceiver output transitions from a microstrip to antenna probe using the FR4 packaging substrate. Proper optimization of the probe with ANSYS

HFSS is used to maintain the bandwidth of the waveguide. A set of multiplexers must be incorporated with the transceiver designs (by O) in order to combine five RF signals into a single output (from 180 to 360 GHz) that feeds a waveguide structure described earlier. Figure 2 shows an example of a 2<sup>nd</sup> order multiplexer design that uses square directional sections that are approximately a wavelength long. This type of design is compact and aids in achieving the isolation requirements for this system. Figure 3 shows the simulated results for five channels of the multiplexer architecture.

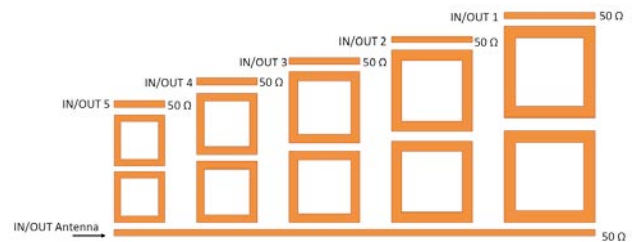


Figure 2: Second order multiplexer design that covers 180-360 GHz using microstrip directional filter topology

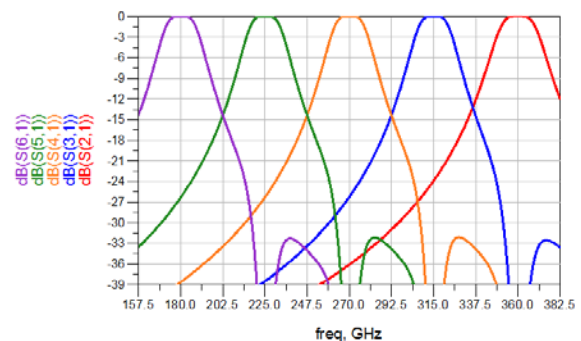


Figure 3: Simulated frequency response of 2<sup>nd</sup> order Butterworth multiplexer. No dielectric or metal losses have been included.

**Keywords:** printed circuit board, multiplexer, Rectangular waveguide, filter

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] M. Gomez, R. Henderson, et al., "Printed circuit board rectangular waveguide with full band microstrip to waveguide transition," 2016 Texas Symposium on Wireless and Microwave Circuits and Systems, March 2016, Waco, TX.



# TASK 1836.158, DEVELOPMENT OF DIELECTRIC WAVEGUIDES FOR THZ RADIATION APPLICATIONS

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## SIGNIFICANCE AND OBJECTIVES

The task comprises the design, fabrication, characterization and application of square dielectric waveguides for the propagation of THz and near-THz radiation using a “holey” cladding fiber structures to engineer the macroscopic refractive index profile. Avoiding dopants in the core improves the loss performance of the waveguide. The waveguides support other TxACE tasks to demonstrate high-speed data transmission between electronic chips and boards.

## TECHNICAL APPROACH

The waveguide was designed using FDTD simulation. Cyclic Olefin Copolymer (COC) was chosen from among commonly used dielectric materials due to its low loss (0.2 dB/cm compared to 8.6 dB/cm for PMMA) in the frequency band of interest. An improved fabrication platform comprises four heaters (controlled by adjustable Variac) sandwiched between two hollow metal shells. The fiber is pulled with a constant force by a DC motor. The mode profile of the waveguide is measured using a VNA and extender modules (220GHz to 325 GHz) and mapped using a pinhole covering the receiver and stepped across the waveguide cross section.

## SUMMARY OF RESULTS

The researcher’s work during the second year concentrated on (1) fabrication of the waveguide designed and simulated in year one, (2) improving the previously developed fabrication platform which reduced thickness variation by a factor of 3, and (3) mapping mode profiles of newly fabricated waveguides.

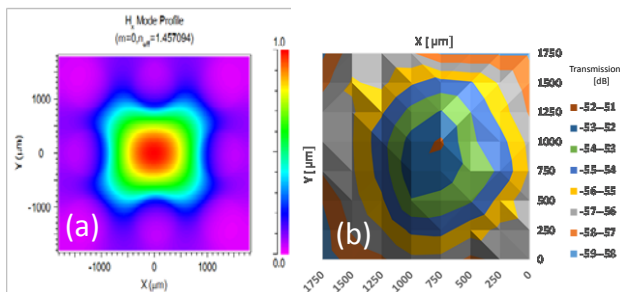


Figure 1: (a) FDTD simulation of an 8-hole square fiber (b) mapped mode profile of a fabricated waveguide using VNA

In Figure 1(a) is shown a FDTD simulation for the single mode in a square holey waveguide at 360 GHz (1480 microns). Figure 1(b) is the measured mode profile supported by a newly fabricated waveguide. In Figure 2 is shown the improved waveguide fabrication platform.

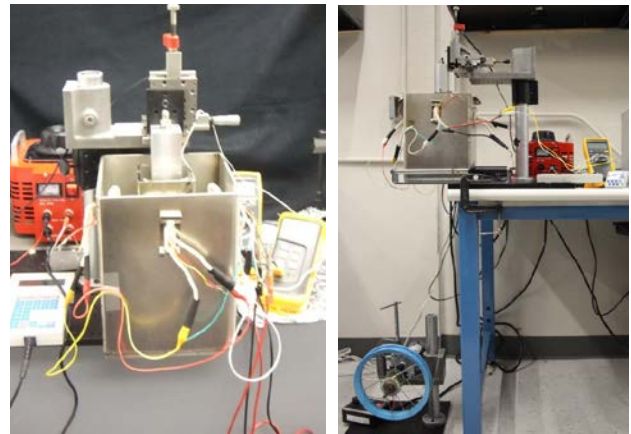


Figure 2: The developed third generation fabrication platform

In Figure 3 is shown recent results of an eight hole waveguide fabricated using the improved platform.

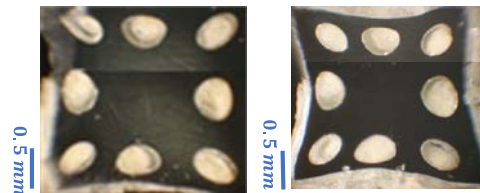


Figure 3: Optical micrograph of a drawn eight hole waveguide based on the design in Fig. 1 and using the improved fabrication platform in Fig. 2

In Year 3 the researchers will (1) functionally test the improved waveguides; (2) fabricate the transition between waveguide and electronic chips which includes development of a parabolic horn- reflector antenna.

**Keywords:** THz, interconnects, holey waveguides

## INDUSTRY INTERACTIONS

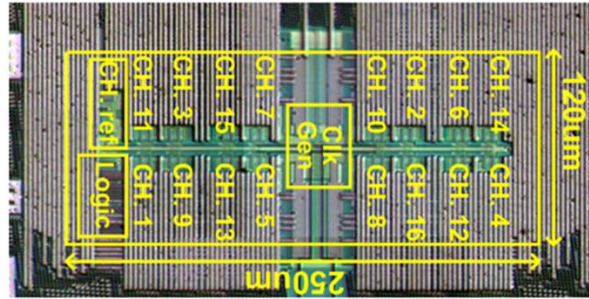
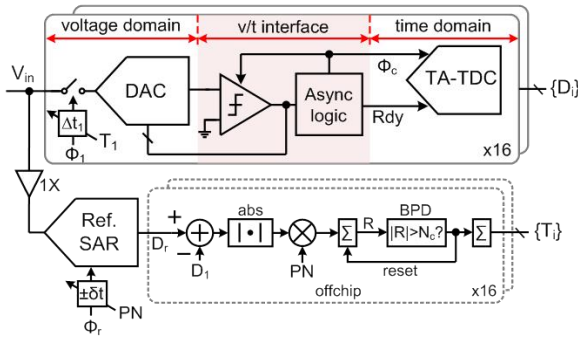
Texas Instruments

## MAJOR PAPERS/PATENTS

[1] N. Aflakian, N. Yang, T. LaFave Jr, R. M. Henderson, K. K. O, and D. L. MacFarlane “Square dielectric THz waveguides,” *Opt. Exp.* manuscript submitted.



# Fundamental Analog Thrust



Category	Accomplishment
Fundamental Analog (Circuits)	A charge-injection SAR (ciSAR), based on a charge injection DAC is demonstrated. The ADC achieves GHz sampling speed from a single SAR ADC and reduces area by more than half by leveraging two unique features of ciSAR: (i) interrupted settling and (ii) reusability of charge-injection cells. The prototype in 40-nm CMOS, occupies 0.00058mm <sup>2</sup> and consumes 1.26mW. The measured ENOB is above 5.46b sampled at 1GS/s. The area is 52% of the closest competitor and the Walden FOM is 28.7fj/conv-step. (1836.125, PI: M. Flynn, U. of Michigan)
Fundamental Analog (Test)	A novel Bayesian learning technique, relevance vector and feature machine (RVFM), for characterizing analog circuits with sparse statistical regression models is proposed. RVFM produces accurate models learned from a moderate amount of data, and computes a probabilistically inferred weighting factor quantifying the criticality of each parameter, hence offering an enabler for variability modeling, failure diagnosis, and test development. The effectiveness is demonstrated in the statistical variability modeling of various circuits. (1836.128, PI: P. Li, TAMU)
Fundamental Analog (Circuits)	Dynamic voltage and frequency scaling (DVFS) and rapid on/off (ROO) approaches along with robust supply voltage generation and regulation techniques are combined to achieve excellent energy efficiency across a wide range of data rates. A prototype source synchronous transceiver is implemented in 65-nm CMOS and is packaged in a 10mm×10mm QFN package. It achieves less than 14ns wake-up time with 14.1-5.9pJ/b energy efficiency for the effective data rates varying from 16Mb/s to 8Gb/s. (1836.129, PI: P. Hanumolu, UIUC)
Fundamental Analog (Circuits)	A power- and area-efficient 24GS/s, 6b, 16-way time-interleaved ADC array, featuring a voltage-time (v/t) hybrid two-step structure for high-speed and low-power operation, a crosstalk-free SAR DAC topology and a non-hierarchical sampling frontend obviating reference and input buffers, respectively, for power and area savings is demonstrated. Fabricated in 28-nm CMOS, a prototype consumes 23mW at 24GS/s and measures an SNDR/SFDR of 35/54dB for a low-frequency input and 29/41dB for a Nyquist input. The core area of the ADC is 0.03mm <sup>2</sup> . (1836.148, PI: Y. Chiu, UT Dallas)



# TASK 1836.087, A HIGH-SPEED LOW-POWER CLOCK DATA RECOVERY (CDR)

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## SIGNIFICANCE AND OBJECTIVES

We propose a low-voltage low-power 25Gb/s serial link receiver in 65nm CMOS technology. Novel circuit techniques are proposed to enable the receiver to operate under 0.6V (nominal supply voltage of 1.2V) for low power consumption with a power efficiency of <math><2\text{mW}/\text{Gb/s}</math>.

## TECHNICAL APPROACH

Novel circuit techniques are proposed to enable low-voltage and low-power operation of a 25Gb/s serial link receiver. At the center of the receiver is a low-phase-noise VCO employing a two-tank transformer-feedback technique to achieve large signal swing under  $V_{DD}$  of 0.6V. The proposed two-tank VCO improves the quality factor and lowers the phase noise with an ultra-low-supply voltage. Gate-biasing techniques are utilized in the varactors and capacitor array to ensure a wide tuning range of the VCO. A forward-body-biasing technique is proposed in the bang-bang phase detector to achieve a large signal swing under  $V_{DD}=0.6\text{V}$  for low BER.

## SUMMARY OF RESULTS

We implemented a 25Gb/s serial link receiver using 65nm CMOS with the proposed circuit techniques so that the entire receiver can be operated at  $V_{DD}=0.6\text{V}$  for low power operation and for compatibility with digital circuitry with decreasing  $V_{DD}$ . The receiver including the Continuous-Time Linear Equalizer (CTLE) consumes 55mW at 25Gbps, achieving a power efficiency of <math><2\text{mW}/\text{Gb/s}</math>.

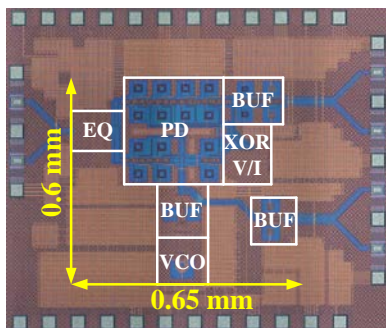


Figure 1: Chip microphotograph of the 25Gb/s serial link receiver

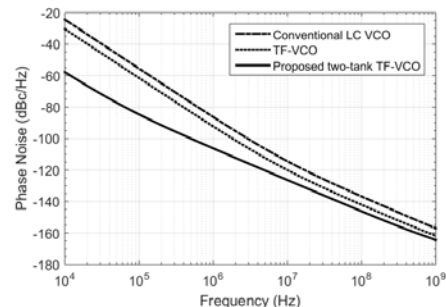


Figure 2: Simulated phase noise of the proposed two-tank VCO in comparison to that of the conventional VCO and Transformer-Feedback VCO

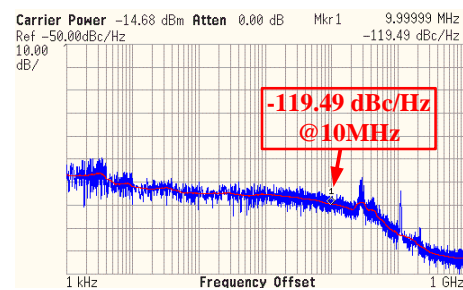


Figure 3: Measured phase noise of the VCO at 25GHz

<b>Data Rate</b>	24.12 Gb/s – 26.07 Gb/s
<b>Supply Voltage Vdd</b>	0.6V (Nominal 1.2V)
<b>Power Consumption</b>	48.8mW
<b>Recovered Clock Jitter</b>	0.23 ps, rms; 4.62 ps, pp
<b>Recovered Data Jitter</b>	0.91 ps, rms; 7.62 ps, pp
<b>Area</b>	0.6 x 0.65 (mm <sup>2</sup> )
<b>Technology</b>	65nm CMOS

TABLE 1: MEASUREMENT PERFORMANCE SUMMARY

**Keywords:** VCO, Clock Data Recovery (CDR), Low voltage, low power, serial link receiver

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] S. Guo, et. al., "A Low-Voltage Low-Power 25 Gb/s Clock and Data Recovery with Equalizer in 65 nm CMOS," IEEE RFIC 2015.

[2] T. Xi, S. et. al., "Low-Phase-Noise 54GHz Quadrature VCO and 76GHz/90GHz VCOs in 65nm CMOS Process," IEEE T-MTT, Volume 64, Iss. 7, 2016.

# TASK 1836.095, TEST GENERATION FOR MIXED-SIGNAL DESIGN VERIFICATION AND POST-SILICON

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## SIGNIFICANCE AND OBJECTIVES

We propose a novel methodology for maximizing DC current in digitally-assisted analog circuits. This is important in reducing the duration of burn-in test, where large current is driven through selected metal wires to screen open/short faults and EM failures during High Volume Manufacturing (HVM) Tests.

## TECHNICAL APPROACH

The proposed methodology identifies a set of analog bias voltages and digital mode selection signals that maximizes the DC current through either a particular wire segment or the power/ground bus. First, a channel-connected graph is built from a mixed signal transistor circuit, then the current activation condition is formulated as satisfiability constraints annotated in the channel-connected graph. This results in a conditional maximum flow problem or weighted constraint satisfaction problem (WCSP) formulation. We applied the proposed methodology to a representative mixed-signal block, which is a self-balanced feedback charge pump.

## SUMMARY OF RESULTS

An EDA flow is developed to automatically identify the activation condition for the channel-connected components (CCC) through localized circuit simulation. The current value and the activation condition of each channel-connected component are used to formulate the WCS problem, which is solved by a Satisfiability Modulo Theory (SMT) engine. Our method is capable of handling both analog voltage bias and digital mode selection signals.

We define the maximum current that can be achieved in localized DC simulation of a CCC to be unconstrained maximum current of the CCC. Algorithm 1 is a bisection method that identifies the input/bias condition that maximizes the DC current through a wire segment.  $I_U$  is initialized to be the unconstrained maximum current of the CCC. The `check_satisfiability()` subroutine checks if there is a input bias condition that respects all the constraints of the CCC, and yields a DC current through the CCC in the range  $[I_U, I_L]$ .

The DC current through the power/ground bus equals to the summation of the DC current through all the CCCs in the circuit. We define activation condition of a CCC, to be the range of analog bias voltage and values of digital

mode selection signals that will yield more than 90% of the unconstrained maximum DC current in a CCC.

**Algorithm 1** Maximize current through selected metal wire using bisection method

```

 $I_U \leftarrow I_{largest}$ 
 $I_L \leftarrow 0$ 
while  $I_U - I_L > \epsilon$  do
     $I_M \leftarrow \frac{I_U + I_L}{2}$ 
     $S \leftarrow \text{check\_satisfiability}(I_U, I_L)$ 
    if  $S$  is True then
         $I_L \leftarrow I_M$ 
    else
         $I_U \leftarrow I_M$ 
    end if
end while

```

Solving a WCSP in which (1) each clause corresponds to the activation condition of a CCC, and (2) the weight of a clause is the unconstrained maximum current of the corresponding CCC, yields an approximated maximum current through the power/ground bus.

Constraint	Weight
$0 \leq VB1, VB2, Vdiff1, Vdiff2, VG \leq VDD$	Hard
$Vdiff1 == \min(0.9464 \cdot VB1 + 0.7965, 1.8)$	Hard
$Vdiff2 == \min(0.9464 \cdot VB2 + 0.7965, 1.8)$	Hard
$VG == 1.66 - 1/(1 + 10^{-0.007 - 2.64 \cdot (Vdiff1 - 0.8 \cdot Vdiff2)})$	Hard
$(VG < 0.2) \wedge \neg D1 \wedge D2 \wedge (VB2 > 0.2)$	400
$(VB1 < 0.8) \wedge (VB2 < 0.8)$	20
$(Vdiff1 > 1) \vee (Vdiff2 > 1)$	20
$(VG < 0.2) \wedge (VB1 > 0.2)$	400

Table 1: Clauses with weight in the formulated WCSP of the numerical example

**Keywords:** channel-connected graph, weighted constraint satisfaction problem, current maximization, burn-in test

## INDUSTRY INTERACTIONS

Texas Instruments, Intel

## MAJOR PAPERS/PATENTS

[1] Chong Li, Suriyaprakash Natarajan, C.J. Richard Shi "Identifying DC Bias Conditions for Maximum DC Current in Digitally-assisted Analog Design", IEEE International Conference on Electronics, Circuits, and Systems, Dec 2015, Egypt.

[2] Chong Li, "Test generation for maximum instantaneous current in analog and mixed-signal circuit", SRC TECHCON, Sep 2015, Austin, TX.

# TASK 1836.096, MIXED-SIGNAL DESIGN CENTERING IN DEEPLY-SCALED TECHNOLOGIES

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## SIGNIFICANCE AND OBJECTIVES

A design methodology for robust design of high-performance analog circuit blocks in highly-scaled technologies is being investigated, to enable rapid yield ramp-up in scaled technologies.

## TECHNICAL APPROACH

We are developing a methodology that enables centering with respect to technology variability of high-performance mixed-signal signal designs in as few as one design iteration. It is based on the components, which are developed simultaneously:

- Instrumenting critical design components to accurately monitor impact of process variability on their performance.
- Creating a dedicated set of representative circuit primitives for their full variability characterization.
- Extracting a variability model from the test structures; building simplified Spice models to predict the distribution spread of critical components.

These components enable centering of critical analog blocks, such as clock and data recovery loops and high-performance data converters.

## SUMMARY OF RESULTS

We have developed an algorithm based on backward propagation of variability to improve yield prediction capability of existent models. The algorithm uses the equation below, where  $e_i$  is the measurement data and  $p_j$  the parameter values, to update the parameter variation values, including parameter correlations in the model.

$$\sigma_{\Delta e_k}^2 = \sum_{k=1}^n \left( \frac{\partial e_i}{\partial p_k} \right)^2 \sigma_{\Delta p_k}^2 + 2 \sum_{(u,v)} \frac{\partial e_i}{\partial p_u} \frac{\partial e_i}{\partial p_v} \text{cov}(\Delta p_u, \Delta p_v)$$

This underdetermined system is solved using a constrained LMS method to limit the solution space.

We have applied this methodology on a design of high-performance comparators for application in analog-to-digital converters, focal plane arrays, high-speed serial links and memory. Among studied topologies, double-tail latch, Figure 1, emerges with favorable tradeoffs among speed, power, offset and variability tolerance.

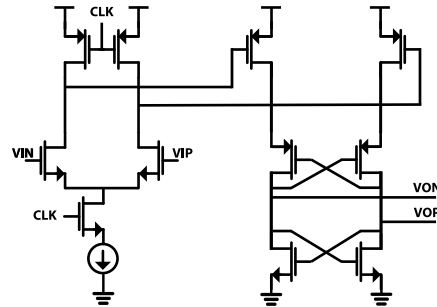


Figure 1: Double-tail latch comparator

These structures target characterizing offset and impulse sensitivity functions, which are then related to variability measured by I-V data of individual devices.

Two test chips have been designed. One test chip has been sent out for fabrication in 28nm FDSOI process which contains large comparator arrays for measuring distributions of offsets, impulse sensitivity functions and transistor I-V characteristics (Figure 2), and is presently being packaged. The second test chip, designed in 28nm HPM technology contains a set of SRAM sense amplifiers.

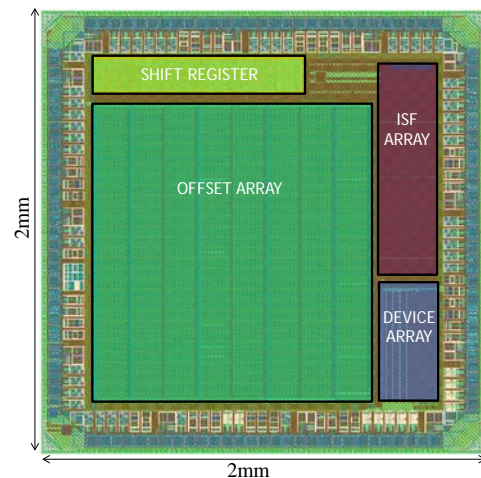


Figure 2: Layout of the 28nm test chip

**Keywords:** CMOS, variability, yield, design optimization, clock and data recovery

## INDUSTRY INTERACTIONS

Intel

## MAJOR PAPERS/PATENTS



# TASK 1836.109, NEW PARADIGMS FOR HIGH-PERFORMANCE AMPLIFICATION

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## SIGNIFICANCE AND OBJECTIVES

Amplifiers are increasingly power hungry and difficult to build in nanoscale CMOS. This has created a crisis that affects us all, particularly in the era of SoCs. The techniques presented in this summary offer new paradigms for high-performance amplification in a variety of applications as a scalable solution.

## TECHNICAL APPROACH

In recent years the ring amplifier (RAMP) emerged as a scalable amplifier for switched capacitor circuits. Its three-stage architecture lends itself to high gain, while a dynamic gain-bandwidth product during amplification eliminates the need for compensation. Despite all the work done in RAMPs, their noise performance is uncharacterized in literature. This work seeks to fill the gap in design knowledge with simulations and noise-characterization of a pipeline ADC.

## SUMMARY OF RESULTS

Estimating the noise performance of a RAMP is not as straight-forward as an OpAmp. For amplifiers, determining their noise performance is done by calculating the integrated noise power. To compute this, both the noise spectral density and bandwidth must be known. In OpAmps, these two characteristics are both primarily determined by input transconductance ( $g_{mi}$ ). Because of the virtual ground,  $g_{mi}$  is accurately predicted with a small-signal analysis.

For a RAMP, the concept of integrated noise remains, but estimating the parameters with a small-signal analysis becomes inaccurate. The bandwidth of a ring amplifier is not as easily understood. This is because during amplification it is variable. The bandwidth goes from high to low with amplification. The major defining feature of the ring amplifier is its deadzone. It is also one of the most important parameters for a designer to control. Therefore, the noise of a ring amplifier was investigated with respect to its deadzone. Figure 1 shows the simulated transient noise of the first amplifier in a 15b Pipelined ADC. The overall SNR is the combined noise of both the first amplifier and the estimated noise resulting from sampling circuits in the ADC. These results from transient noise simulations do not include other noise sources such as those from the following stages in the in the amplifier or reference noise.

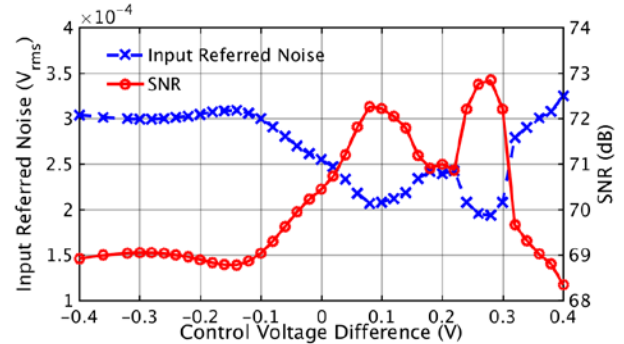


Figure 1: Simulated noise of 15b Pipelined ADC

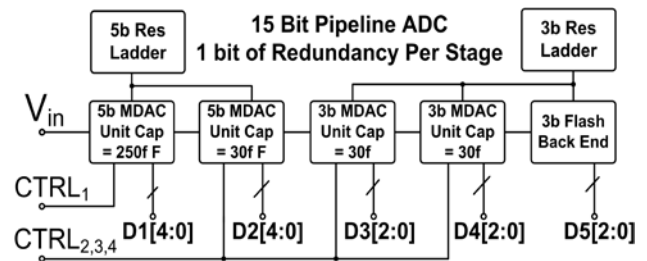


Figure 2: 15b Pipelined ADC Structure

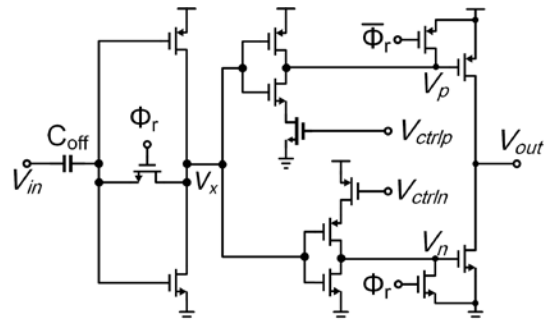


Figure 3: Current-starved Inverter Ring Amplifier

The overall structure of the ADC is shown in Figure 2. The higher resolution in the first stages allows for isolation of the noise performance. The structure of the Ring Amplifiers used in this design is shown in Figure 3.

**Keywords:** ring amplifier, noise performance, high resolution, scalable amplification

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS



# TASK 1836.111, ADVANCED ADC-BASED SERIAL LINK RECEIVER ARCHITECTURES

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 SEBASTIAN HOYOS, TEXAS A&M UNIVERSITY

## SIGNIFICANCE AND OBJECTIVES

While CMOS technology scaling allows for the efficient implementation of powerful on-chip DSP algorithms for equalization and symbol detection, ADC-based receivers are generally more complex and consume higher power. The proposed ADC-based serial link techniques aim to significantly improve interconnect bandwidth density in an energy-efficient manner.

## TECHNICAL APPROACH

In order to investigate design trade-offs, a novel statistical-modeling framework for advanced ADC-based serial links will be developed. This tool will be used to guide the design of a new hybrid ADC-based receiver architecture which combines in a power optimum manner equalization embedded in the ADC and dynamically power-gated digital equalization based on threshold detection, with an ultimate target data rate in excess of 25Gb/s. The statistical modeling framework and receiver prototypes will be leveraged to investigate the performance of the hybrid ADC architecture with multi-level modulation schemes (duobinary, PAM4, PAM8, etc.) and error correction coding.

## SUMMARY OF RESULTS

In order to relax ADC-based RX power and complexity, partial equalization can be embedded inside the ADC and not be limited by the ADC resolution. While this provides improved BER, additional eq. is generally required to support channels with loss >30dB. This is addressed in an

energy-efficient manner with a new hybrid ADC-based RX architecture which combines embedded ADC equalization and dynamically-enabled digital eq. based on threshold detection [1]. A 10Gb/s RX prototype with a 3-tap analog FFE embedded inside a 6-bit asyn. SAR ADC and a dynamically-enabled digital 4-tap FFE and 3-tap DFE was fabricated in GP 65nm CMOS (Figure 1). The RX compensates for up to 36.4dB loss with 30mW savings in the digital eq. power and an overall power <90mW.

In order to support data rates at or above 50Gb/s, energy-efficient ADC designs with moderate resolution and very high sampling rates are required. This is addressed in a 25GS/s 6b 8-way time-interleaved binary search ADC that employs a novel soft-decision selection algorithm to relax track-and-hold (T/H) settling requirements and improve ADC metastability tolerance (Figure 2) [2]. Fabricated in GP 65nm CMOS, the ADC

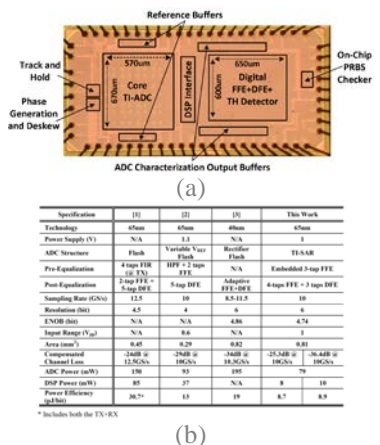
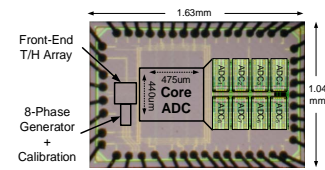


Figure 1: 10Gb/s hybrid ADC-based receiver: (a) GP 65nm CMOS prototype, (b) performance summary



(a)

TABLE I. PERFORMANCE SUMMARY

Specification	[5]	[4]	This Work
Technology	65nm	32nm SOI	65nm
Power Supply	1.5V	0.9V	1V
ADC Structure	TI-Flash	TI-Flash	TI-BS
Sampling Rate	16 GS/s	20 GS/s	25 GS/s
Resolution	6 bits	6 bits	6 bits
ENOB @ Nyquist	4.36 bits	4.84 bits	4.62 bits
Area	1.47 mm <sup>2</sup>	0.25 mm <sup>2</sup>	0.24 mm <sup>2</sup>
Power	435 mW	69.5 mW	88 mW
FOM ( $P_{2^{ENOB}}/A$ )	1325 fJ/c-6	124 fJ/c-6	143 fJ/c-6

(b)

Figure 2: 25GS/s 6b TI binary search ADC: (a) GP 65nm CMOS prototype, (b) performance summary

occupies 0.24mm<sup>2</sup> total area, achieves 29.6dB SNDR at Nyquist while consuming 88mW from a 1V supply, translating into a figure-of-merit (FoM) of 143 fJ/conv.

**Keywords:** analog-to-digital converter, ADC-based receiver, embedded equalization, energy efficient

## INDUSTRY INTERACTIONS

Freescal, Intel, Texas Instruments

## MAJOR PAPERS/PATENTS

- [1] A. Shafik et al., "A 10Gb/s Hybrid ADC-Based Receiver with Embedded Analog and Per-Symbol Dynamically-Enabled Digital Equalization," IEEE JSSC, Mar. 2016.
- [2] S. Cai et al., "A 25GS/s 6b TI Binary Search ADC with Soft-Decision Selection in 65nm CMOS," IEEE VLSI Symp., June 2015.

# TASK 1836.113, SYNTHESIZED CELL-BASED ADPLL IMPLEMENTATION FOR ACCELERATED DESIGN

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## SIGNIFICANCE AND OBJECTIVES

This program focuses on developing “cell-based” all-digital PLLs that can be synthesized from a cell library, implemented using existing automatic place and route (APR) tools, and then digitally calibrated. The end result will be a set of PLL architectures described in HDL which can be adapted to a wide range of performance requirements.

## TECHNICAL APPROACH

All-Digital Phase-locked loops (ADPLLs) are widely used as clock generators in advanced digital systems, eliminating several of the downsides of traditional PLLs. Previous work has demonstrated that integer-N ADPLLs can be implemented using digital synthesis and automatic place-and-route (APR) tools, resulting in a simplified and easily customizable design flow. Our next goal is the development of fractional-N frequency synthesizers which leverage novel architectural and implementation improvements. These new designs will be synthesizable using standard CAD tools, and will be prototyped in a series of test chips in advanced CMOS processes.

## SUMMARY OF RESULTS

Existing work has largely focused of clock generators targeting processor cores, an application this approach is well suited towards. A large number of PLLs in modern systems is targeted towards various high speed serial I/O standards. In order to explore the possibilities of synthesized PLLs for serial-link applications we are designing a clock generator targeting a 5 Gb/s serial transceiver. In addition, a synthesized clock and data recovery (CDR) system is generated alongside the main clock generator.

The PLL uses a phase domain architecture, as shown in Fig. 1. In this architecture, the digitally controlled oscillator (DCO) output signal is not divided down to the reference frequency. Instead, the integer and fractional number of DCO cycles occurring during a reference cycle are counted and compared to the expected value during each reference cycle. The integer and fractional parts of the DCO cycle count are measured by a digital cycle counter and an embedded time-to-digital converter (TDC). The embedded TDC works by sampling the internal phase signals of the ring oscillator in order to determine the overall state of the oscillator, and hence what fraction of a cycle it has completed. In order to improve the resolution of the embedded TDC, a phase

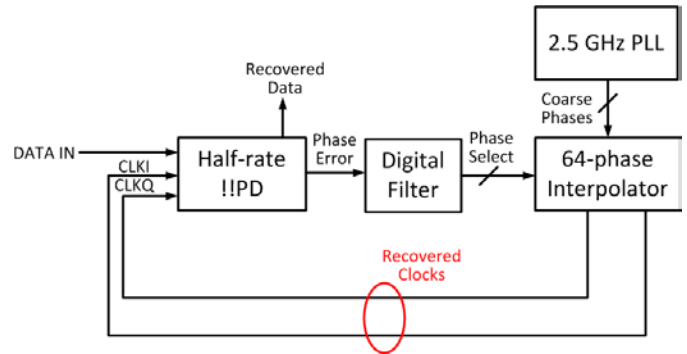


Figure 1: CDR block diagram

interpolation circuit is used. In addition, the ADPLL supports Spread Spectrum Clocking (SSC) by means of modulating the frequency control word. This reduces peak emission power, which is required by many serial link standards.

A system level phase noise simulation using estimated block level specs was done, with a phase jitter level of 1.23 ps. The spectrum with spread spectrum modulation enabled is shown in Fig. 2. This corresponds with the spreading requirements for most SSC SERDES applications.

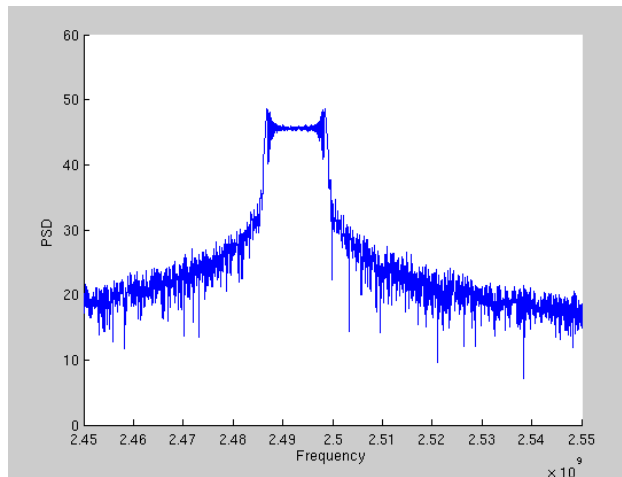


Figure 2: SSC output

**Keywords:** VLSA (Very Large Scale Analog), ADPLL, CMOS, frequency synthesizer, fractional-N

## INDUSTRY INTERACTIONS

Texas Instruments, Intel, Freescale

## MAJOR PAPERS/PATENTS

# TASK 1836.117, PERFORMANCE AND RELIABILITY ENHANCEMENT OF EMBEDDED ADCS WITH VALUE-ADDED BIST

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DEGANG CHEN, IOWA STATE UNIVERSITY

## SIGNIFICANCE AND OBJECTIVES

The objectives are to develop procedures for implementing parametric BIST of ADCs with minimal area overhead, to use on-chip test results to enhance performance by digitally calibrating the ADC, and to experimentally demonstrate the BIST and BIST-based calibration on an ADC internal to a microcontroller.

## TECHNICAL APPROACH

The Functionally Related Excitation (FRE) approach to testing using a Stimulus Error Identification and Removal (SEIR) algorithm will be adapted to a BIST solution. The FRE/SEIR approach was developed in conjunction on a previous SRC project. On-chip FRE signal generators using the shift operator will be developed for test signal generation and existing on-chip computation resources will be utilized to minimize the area overhead required to implement the SEIR algorithm. Target area overhead is at most 10% of the area of the existing uncalibrated ADC that is currently in high-volume production.

## SUMMARY OF RESULTS

A block diagram showing the BIST capability and the BIST-based calibration is shown in Fig. 1 with a target 12-bit ADC. Two additional bits of resolution have been added to the SAR ADC to allow for a 2-bit improvement in linearity with the BIST-based calibration. The final output is then decimated back to 12 bits after calibration.

The signal generator will be a current ramp based integrator comprised of the output from a simple regulated cascode current source charging a nonlinear capacitor. With the FRE/SEIR approach, linearity of the ramp is of little concern. To manage the size of the integration capacitor, a series of faster-rising ramps will be used instead of a single ramp. A second-generation level-spreading ramp generator using a dithered integration starting voltage was developed to maintain approximately uniform density of the input signal throughout the input range of the ADC. A critical component is the shift generator which must have a constant shift. The second-generation shift generator in Fig. 2 that provides rail-to-rail output using correlated level shifting (CLS) and that provides the constancy needed for testing 14-bit ADCs has been designed.

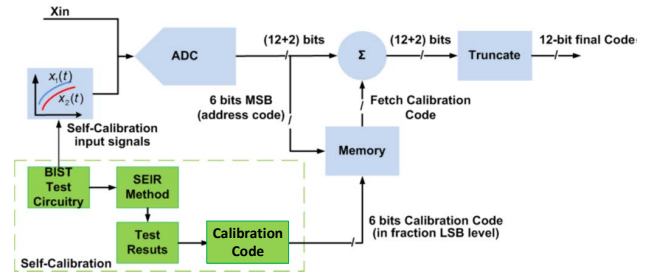


Figure 1: Block Diagram of ADC with BIST-Based Calibration and Value-Added BIST

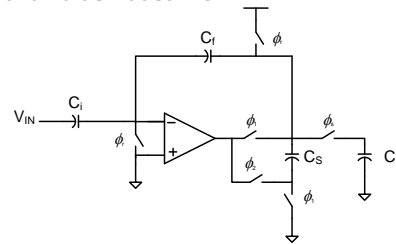


Figure 2: FRE shift generator using correlated level shifting for rail-to-rail outputs

**Keywords:** ADC BIST, self-calibration, analog testing, FRE signal generators, SEIR testing

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

In this custom-funding project, details about the ADC used for experimental verification are proprietary property of TI thus precluding publication of key technical details of the project. Two publications that discuss principles used in this research follow.

[1] X. Zhang et. al., "A Calibration Technique for SAR Analog-to-Digital Converter Based on INL Testing with Quantization Bits and Redundant Bit," 2015 IEEE Int. Symp. on Circuits and Systems (ISCAS), pp. 3024-3027, May, 2015.

[2] H. Meng et al., "A Simple Ramp Generator with Level Spreading for SEIR based ADC BIST Circuit," IEEE Midwest Symp. On Circuits and Systems (MWSCAS), pp. 53-56, Aug., 2015.

# TASK 1836.125, 10GS/S+ RESOLUTION-SCALABLE (4-7BITS) ADCS

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## SIGNIFICANCE AND OBJECTIVES

This research is developing and demonstrating new approaches to high speed ADC design. The new techniques enable energy efficient, very-high-speed (>10GS/s) moderate resolution analog to digital conversions (4-7b) in 28nm or 32nm CMOS technology.

## TECHNICAL APPROACH

To support growing data bandwidths, high-speed moderate resolution ADCs are vital for high-speed data links. Interleaved SAR ADCs achieve high sampling speeds and good energy efficiency. However, a challenge is that these ADCs are large and therefore suffer from interleaving artifacts related to size. Compact, efficient SAR ADCs are needed to address this problem. As an alternative, multiple-bit-per-cycle SAR ADCs deliver high speed from a single SAR ADC, but at the cost of significant added complexity (i.e. extra quantizers and capacitor DACs) and die area. This work addresses the need for a fast, compact SAR ADC, with a 1GS/s SAR ADC that has the best Walden FoM and the smallest area among 5~6.3bit ADCs.

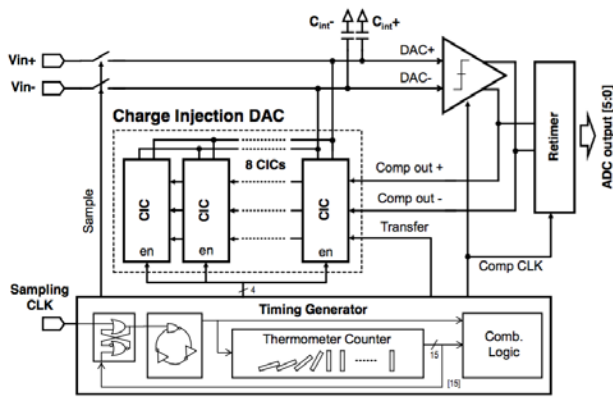


Figure 1: Block diagram of CIC-SAR 6-bit ADC

## SUMMARY OF RESULTS

We introduce the *charge injection SAR* (or ciSAR), which is based on a charge injection DAC structure. ciSAR achieves GHz sampling speed from a single SAR ADC and reduces area by more than half. The proposed ADC achieves the best Walden FoM and the smallest area by leveraging two unique features of ciSAR: (i) interrupted settling and (ii) reusability of charge injection cells.

ciSAR, thanks to interrupted settling, is faster, simpler and more linear for high-speed applications. This is because ciSAR avoids the significant distortion suffered

by conventional fast SAR ADCs due to insufficient DAC settling time. This distortion is caused by residual settling from earlier SAR conversion steps while the present DAC settling step is taking place.

In addition to interrupted settling, another important advantage of ciSAR is that CIC cells can be reused multiple times in a SAR conversion. Since CICs are only active during a short time, they can utilize the rest of the time (i.e. waiting for a comparator decision) to get ready for another transfer. By reusing the CICs for the subsequent transfer cycles, the DAC area of ciSAR can be reduced at least by half or even more, since the charge transfer process can be spread out over multiple transfer cycles to reach the desired level of transfers.

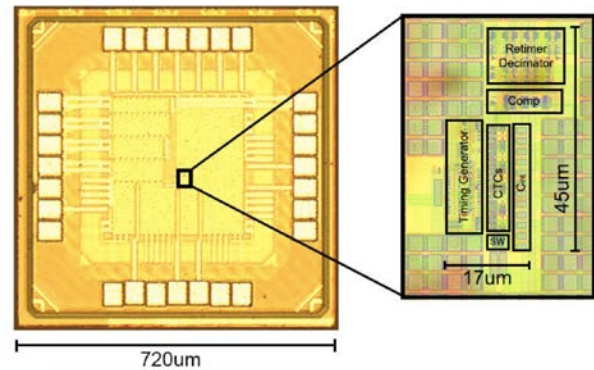


Figure 2: Die plot of 40nm CMOS 6-bit ADC

The ADC input range is 300mVpk-pk (600mVdiffpk-pk). The integration caps are each 200fF. The integration capacitors are implemented as M1-M7 MOM capacitors and occupy only 66um<sup>2</sup>. This compact layout scheme is possible since mismatch between the two caps only introduces a small offset.

The prototype, fabricated in 40nm CMOS, occupies 0.00058mm<sup>2</sup> and consumes 1.26 mW from a 1V supply. The measured ENOB is above 5.46b across input frequencies spanning from 30MHz to 500MHz, sampled at 1GS/s. The area is 52% of the closest competitor and the Walden FoM is measured at 28.6fJ/conv-step.

**Keywords:** ADC, flash, two-step, CMOS

## INDUSTRY INTERACTIONS

Texas Instruments, IBM

## MAJOR PAPERS/PATENTS

[1] K. Choo, J. Bell and M.P. Flynn, "Area-efficient 1GSps 6b SAR ADC with Charge-Injection Cell Based DAC," ISSCC 2016.



# TASK 1836.127, PRECISION TEST WITHOUT PRECISION INSTRUMENTS

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 RANDY GEIGER, IOWA STATE UNIVERSITY

## SIGNIFICANCE AND OBJECTIVES

Accurate spectral analysis is widely needed in IC characterization and final test. Ideal IEEE standard test requires accurate instruments and accurate test control, resulting in expensive equipment, complex test setup, demanding maintenance, TTM delays, and high test cost. The objective of this research is to develop new spectral test algorithms to remove IEEE standard requirements, deliver accurate full spectrum test results, and greatly reduce test equipment cost, TTM delays, and test time.

## TECHNICAL APPROACH

Mixed-signal spectral testing is re-cast as an identification problem of weakly nonlinear signal & systems. Statistical signal processing techniques are incorporated to develop algorithms for accurately separating and extracting all distortion, jitter and noise information out of a relatively small data set, with accuracy near theoretical limits. An innovative iterative time-frequency domain processing technique is utilized to achieve the best accuracy and time efficiency trade-off, in which all spectral spurs (input, distortions, periodic jitter, etc.) are identified in frequency domain while residue error construction and noise/jitter characterization (“flat” in spectrum) are done in time domain. This dual domain approach enables high time efficiency and high dynamic range detection, allowing accurate estimation of small error components from various sources of distortion under test.

## SUMMARY OF RESULTS

The final goal of the project is the elimination of all the stringent requirements in the ideal IEEE standard spectral testing. These requirements include: perfectly coherent sampling, accurate amplitude control, high purity sine wave stimulus, and jitter-free sampling clock signal. During the first two years, we published three journal papers and 9 conference papers. We introduced 1) FIRE method for removing non-coherency, 2) the FERARI method for both non-coherency and amplitude clipping, 3) a jitter and noise separation method for accurate SNR testing, 4) a comparative study of state of the art methods for dealing with non-coherent sampling, 5) an algorithm for both nonlinear signal source and non-coherent sampling, 6) algorithms for simultaneous AC and DC test with dramatic test time reduction; 7) an algorithm for accurate SNR test in the presence of clock jitter, 8) a method for clock jitter separation and

characterization; and 9) a method for generating ultra-pure sine wave signals for high resolution ADC testing.

During the year May 2015 – April 2016, we published two journal papers and 6 conference papers. We introduced a test method for accurate linearity testing with an impure sinusoidal stimulus robust against flicker noise. We also developed an algorithm for accurate spectral testing with non-coherent sampling and large distortion to noise ratios. Furthermore, we presented a new test solution for accurate spectral testing of analog-to-digital converters with frequency drift using phase correction and averaging. To handle clock jitter, we introduced an accurate and cost-effective technique for jitter and noise separation. Building upon this, we presented a low-cost test method for jitter separation and characterization. Many of the proposed test algorithms have been validated at SRC member companies.

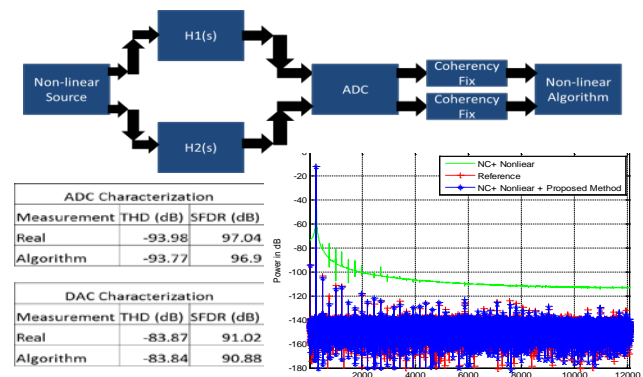


Figure 1: A proposed test algorithm allows the use of a nonlinear DAC as an approximate sine wave generator for testing a highly accurate ADC, also allowing noncoherent sampling. The algorithm produces simultaneously accurate test results for both the ADC and the DAC, as can be seen from both the spectrum and the table

**Keywords:** AC test, spectral test, nonlinear source, non-coherent sampling, amplitude clipping, jitter, noise

## INDUSTRY INTERACTIONS

Texas Instruments, Freescale

## MAJOR PAPERS/PATENTS

- [1] Wu, et al, Elect letters'15.
- [2] Wu, et al, IEICE Elect Exp'15.
- [3] Zhuang, et al, VTS'16.
- [4] Zhuang, et al, VTS'16.
- [5] Zhuang, et al, MWSCAS'15.
- [6] Duan, et al, ISCAS'15.
- [7] Xu, et al, ISCAS'15.
- [8] Xu, et al, ISCAS'15.



# TASK 1836.128, STATISTICAL ANALOG DESIGN PROPERTY CHECKING

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## SIGNIFICANCE AND OBJECTIVES

Aiding design, verification and test optimization of analog circuits requires accurate models that can reliably capture complex dependencies of circuit performances on essential circuit and device parameters, and test signatures. We seek to develop a novel Bayesian learning based approach for accurate modeling.

## TECHNICAL APPROACH

We propose a new machine learning technique, namely, relevance vector and feature machine (RVFM), for characterizing analog circuits with sparse statistical regression models [3]. RVFM not only produces accurate models learned from a moderate amount of simulation or measurement data, but also computes a probabilistically inferred weighting factor quantifying the criticality of each parameter as part of the overall learning framework, hence offering a powerful enabler for variability modeling, failure diagnosis, and test development.

## SUMMARY OF RESULTS

Compared to other popular learning-based techniques, the RVFM produces more accurate models, requires less training data, and extracts more reliable parametric ranking. The effectiveness of RVFM has been demonstrated in terms of the statistical variability modeling of a low-dropout regulator (LDO) and the built-in self-test (BIST) development and optimization of a charge-pump phase-locked loop (PLL).

For example, RVFM has been applied to characterize the LDO shown in Fig. 1. Fig. 2 shows the extracted weights (or significances) of 20 channel length variations regarding the load regulation performance. Fig. 3 shows more comprehensively the learning-based characterization of three LDO performances: quiescent current (QC), undershoot (UDS), and load regulation (LR).

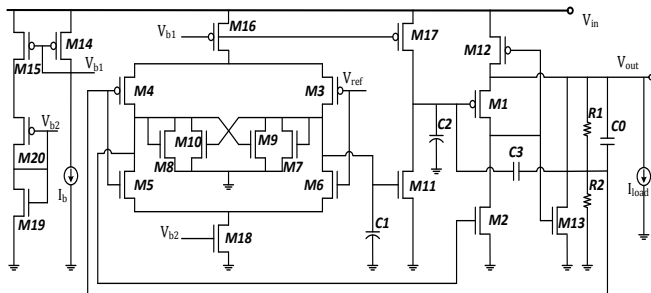


Figure 1: LDO with multiple regulation loops

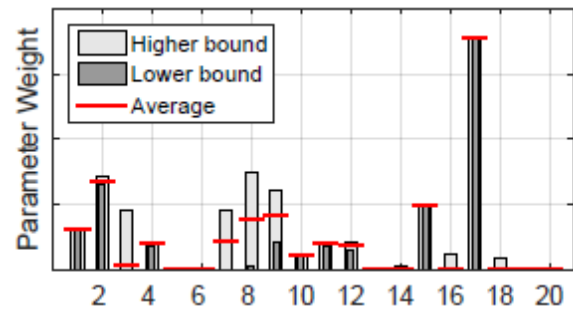


Figure 2: Parameter weights of 20 transistor channel length variables for load regulation

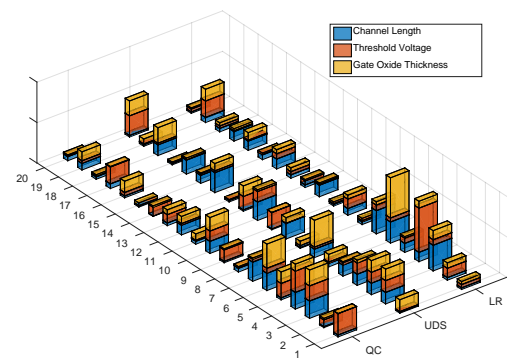


Figure 3: Parameter weights of 60 transistor-level variation (i.e. channel length, threshold voltage, gate-oxide thickness) parameters for three performances

The extracted RVFM performance models can be used for design and verification; and the extracted weights may provide critical design insights and enable diagnosis and test developments.

**Keywords:** machine learning, Bayesian learning, analog verification, analog characterization, BIST

## INDUSTRY INTERACTIONS

Texas Instruments, Intel

## MAJOR PAPERS/PATENTS

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- [2] Lin and Li, "Circuit Performance classification with active learning guided sampling for support vector machines," IEEE Trans. CAD, Sep. 2015.
- [3] Lin and Li, "Relevance vector and feature machine for statistical analog circuit characterization and built-in self-test optimization," IEEE/ACM DAC, Jun. 2016.

# TASK 1836.129, ENERGY PROPORTIONAL TRANSCEIVER WITH RAPID ON/OFF AND DVFS

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## SIGNIFICANCE AND OBJECTIVES

Proposed research sets out to explore energy proportion links combining rapid on/off (ROO) and dynamic voltage and frequency scaling (DVFS) to cut the power wastage so as to improve the energy efficiency at the system level. The solutions for fast response link power management and the characterization of burst-mode transceiver were proposed and evaluated.

## TECHNICAL APPROACH

A source synchronous architecture is adopted for the link transceivers (Fig.1). The power management consists of a hysteretic DC-DC converter and source follower-based low dropout voltage regulator (LDO). Multiply delay locked loop (MDLL) is adopted as the fast on/off clock multiplier. A programmable divider is proposed inside MDLL to suppress the supply voltage ripple and help MDLL settle within one reference cycle.

## SUMMARY OF RESULTS

This work demonstrate the first energy proportional transceiver that combines ROO and DVFS, and wake-up in less than 14ns for 6Gb/s operation (Fig. 2). The transceiver power scales almost linearly with average data rate or utilization level (Fig.3a). For 128-byte data bursts, the transceiver operating at a peak data rate of 8Gb/s in the ROO mode achieves 500x effective data rate scaling (8Gb/s–16Mb/s) while scaling the power by 84x (46.8–0.56mW) and energy efficiency by 6x (6.2–37pJ/b). With DVFS, energy efficiency varies by only 2.2x (6.2–14.1pJ/b) for 500x effective data rate scaling and 220x (46.8-0.21mW) power scaling (Fig.3b). ROO by itself can provide data rate scaling of only 100x for 2x variation in efficiency. Thanks to the combination of DVFS and ROO, the proposed link extends data rate scaling beyond 100x and achieves the largest energy proportional range of 500x with only 2x energy efficiency variation.

## INDUSTRY INTERACTIONS

Texas Instruments, Intel, AMD

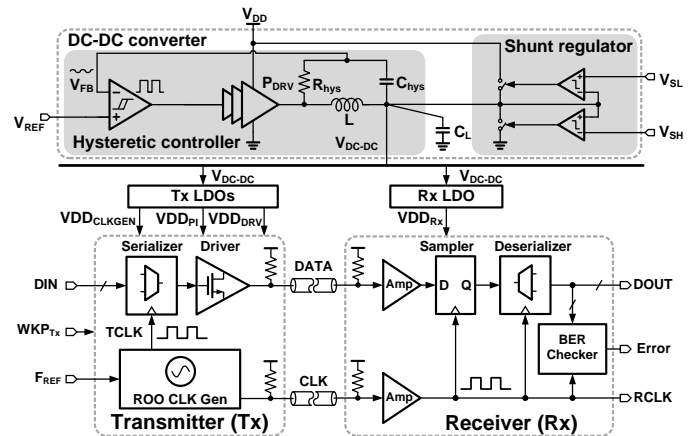


Figure 1: Block diagram of proposed link transceiver

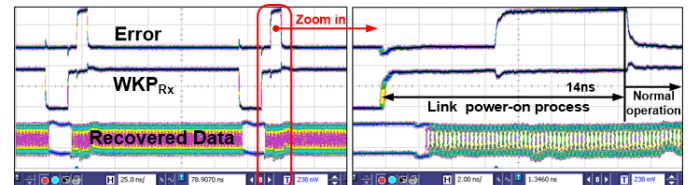


Figure 2: Measured transceiver power-on/off transient at 6Gb/s

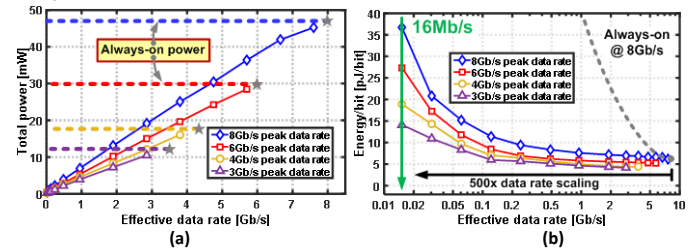


Figure 3: (a) Measured transceiver power versus effective data rate. (b) Measured transceiver energy-per-bit versus effective data rate

**Keywords:** energy proportional links, dynamic power management

## MAJOR PAPERS/PATENTS

[1] G. Shu, W. Choi, S. Saxena, S. Kim, M. Talegaonkar, R. Nandwana, A. Elkholy, D. Wei, T. Nandi, and P. Hanumolu, "A 16 Mb/s-8 Gb/s, 14.1-5.9 pJ/bit source synchronous transceiver using DVFS and rapid on/off in 65nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Jan. 2016, pp. 398-399.

# TASK 1836.132, FAULT-COVERAGE ANALYSIS OF ANALOG/MIXED-SIGNAL TESTS BASED ON STATISTICAL DISSIMILARITY

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## SIGNIFICANCE AND OBJECTIVES

The number of mixed-signal ICs escaping production screening is sharply rising due to the increasing use of digital circuits within analog systems. This task aims to develop a systematic way to quantitatively measure the fault coverage of a given analog/mixed-signal circuit test. This is a key pre-requisite to the automatic generation of efficient analog/mixed-signal test suites or patterns that can achieve high defect coverage and short testing time.

## TECHNICAL APPROACH

This task explores ways of quantitatively measuring the fault coverage of an analog/mixed-signal test suite leveraging various statistical discrimination methods.

For instance, a test is said to cover a fault when the fault causes large enough difference in the test's response that can be distinguished from the normal statistical variations of the circuit due to global process, voltage, and temperature (PVT) variations and local transistor-to-transistor mismatches.

In addition, the correlations among the test responses can be utilized in various ways, for instance, to enhance the effective coverage of a given test suite and to estimate the statistical distributions with a small number of Monte-Carlo samples.

## SUMMARY OF RESULTS

An initial study has been conducted that quantifies the test coverage of some representative analog/mixed-signal circuits over basic catastrophic stuck-short/open faults. Despite the simplistic assumptions made, the results demonstrate that the fault coverage analysis based on statistical discrimination can be an effective way to measure the fault coverage of a given test suite and guide the composition of an efficient test suite. For instance, the analysis shows that all the stuck-open/short faults in an 8-bit digitally-controlled phase interpolator can be covered with only 5 different delay measurement tests. The analysis can also identify redundant components in the circuit.

This year, an incremental, min-max search algorithm is devised to find a minimal set of tests that achieves the desired algorithm. This algorithm accounts for the cross-correlation among the tests and is more efficient than an exhaustive, combinatorial search algorithm.

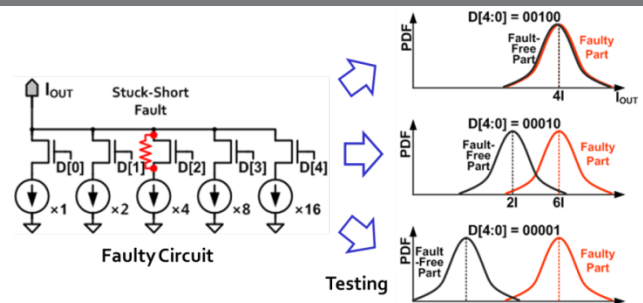


Figure 1: Determining fault coverage based on variability distribution

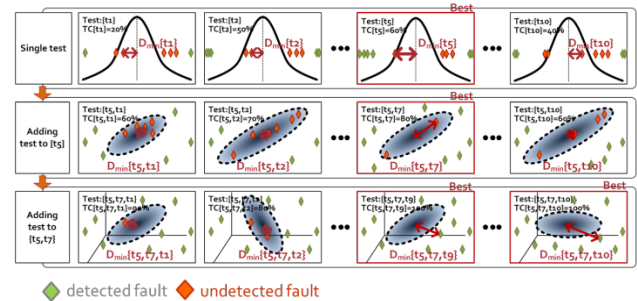


Figure 2: Efficient test compaction algorithm that finds the minimal set of tests with the desired coverage

**Keywords:** analog/mixed-signal circuits, production tests, fault coverage analysis, test compaction, automatic test pattern generation

## INDUSTRY INTERACTIONS

Texas Instruments, Intel, GlobalFoundries

## MAJOR PAPERS/PATENTS

- [1] S. Youn, C. Gu, and J. Kim, "Probabilistic Bug Localization for Analog/Mixed-Signal Circuits using Probabilistic Graphical Models," Design Automation Conf. (DAC), June 2014.
- [2] S. Jung, J. Lee, and J. Kim, "Variability-Aware, Discrete Optimization for Analog Circuits," Trans. on Computer-Aided Design, 2014.
- [3] S. Jung, J. Lee, and J. Kim, "Yield-Aware Pareto-Front Extraction for Discrete, Hierarchical Optimization of Analog Circuits," Trans. on Computer-Aided Design, 2014.
- [4] J. Kim, et al., "Discretization and Discrimination Methods for Design, Verification, and Testing of Analog/Mixed-Signal Circuits," Custom Integrated Circuits Conf., 2013.

# TASK 1836.134, HYBRID TWO-STEP PLLS FOR DIGITAL SOCS IN NANOSCALE CMOS

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## SIGNIFICANCE AND OBJECTIVES

PLLs are a critical part of today's communication systems. Their performance optimization is essential for modern SOCs. The objective of this project is to replace the bulky on-chip inductors used in low-jitter PLLs with compact ring oscillators, while still preserving the performance. This calls for development of a hybrid two-step PLL.

## TECHNICAL APPROACH

The overall frequency conversion is divided into two cascaded stages (Fig.1). The first stage, employing noise cancellation, generates a high quality, high frequency reference for the second stage. A novel noise cancellation technique is employed to achieve low noise, high ratio frequency multiplication. The wide loop bandwidth allows the usage of compact ring oscillators. The second stage, a fractional-N PLL, provides the required fine resolution. Due to the low-ratio multiplication, it has much reduced noise impact.

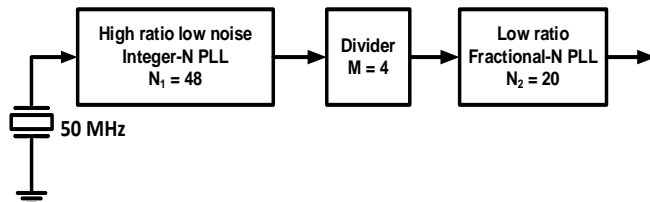


Figure 1: The block diagram of the proposed two step PLL

## SUMMARY OF RESULTS

The usage of large bandwidth (>1MHz) in the two-step PLLs architecture (Fig. 1) reduces the noise impact of the VCOs. This enables the usage of compact ring oscillators in spite of their poorer performance in comparison to large-size LC oscillators. The large BW also helps in shrinking the loop filter area, further reducing the area of the PLL.

We have currently focused on the first-stage ring-oscillator PLL architecture and circuit design. It has an input frequency of 50MHz and an output frequency of 2.4 GHz. The PLL uses a phase-detector based auxiliary PLL loop with a dead zone to keep the bias of the ring VCO aligned. The main loop uses a high-gain, low-noise sampling phase detector that maintains the phase lock between the VCO and reference frequency. The PLL has a high loop bandwidth of 2.5 MHz.

A key innovation we are prototyping for the first-stage ring-oscillator PLL is the use of a feed-forward phase-

noise-cancellation stage following the output of the PLL. The cancellation is implemented with a variable delay that receives its control information from noise-detection circuits embedded in the PLL.

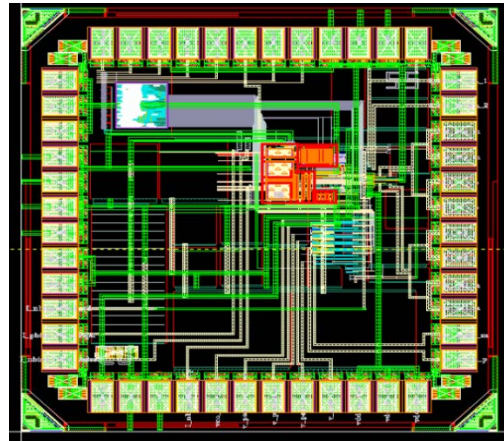


Figure 2 Layout of the ring-oscillator PLL prototype with feed-forward noise cancellation

We taped out a PLL prototype in 65nm CMOS (Fig. 2) in May 2016. The phase noise simulation results for the first-stage PLL before and after cancellation are shown in Fig.3. The RMS jitter reduces by 1.6 times from 0.8ps to 0.5ps.

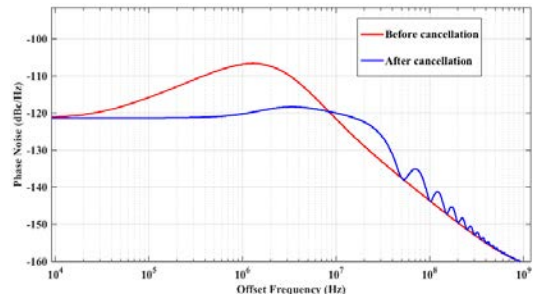


Figure 3: Simulated Phase noise of the first-stage PLL prototype, before and after noise cancellation

**Keywords:** two-step PLLs, sub-sampling phase detectors, ring oscillators, wide-band phase noise cancellation

## INDUSTRY INTERACTIONS

Intel, Texas Instruments, GlobalFoundries

## MAJOR PAPERS/PATENTS



# TASK 1836.136, INJECTION-LOCKED RING OSCILLATORS FOR CLOCK DISTRIBUTION IN MANYCORE PROCESSORS

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## SIGNIFICANCE AND OBJECTIVES

Technology scaling has enabled integration of many independent processing elements on a single die or in a same module. Energy-efficient circuit design for synchronization of manycore processors, based on both traditional techniques and injection-locked ring oscillators is the objective of this work.

## TECHNICAL APPROACH

We are developing a low-overhead global clock distribution scheme for manycore processors and heterogeneous SoCs based on ring oscillators and injection-locked ring oscillators (ILROs). A hard-coupled ILRO can multiply its output frequency, reducing the power overhead of the global clock distribution network.

## SUMMARY OF RESULTS

We have developed two designs for clock generation in manycore processors, based on a delay-locked loop (DLL) and on a phase-picking clock generator in Fig. 1 [1-2]. In the first approach, a ~2GHz reference clock is distributed to DLLs, which generate 16 uniformly-distributed clock phases. Phase-picking clock generator picks the appropriate phase for each clock cycle, based on information from the timing replica path.

The design, implemented in 28nm ultra-thin body and BOX fully-depleted silicon-on-insulator (UTBB FDSOI) technology is fully functional and occupies  $32\mu\text{m} \times 30\mu\text{m}$  (Fig. 1). Generated clock frequency is in the range 550-2260MHz at 1V and 100-625MHz at 0.5V.

The second clock generation scheme is self-timed. Figure 2 shows the schematic of the adaptive clock generator. The delay units are composed of four tunable delay banks, each of which uses a different cell for its delay element and can be tuned independently. Instead of using the delay line outputs for selecting DLL phases, in this approach we simply asynchronously toggle a standard flip-flop through its set/reset inputs. This design was also implemented in 28nm UTBB FDSOI process and achieved similar performance with much lower complexity.

In addition, the main clock in the test chip is generated by using a bang-bang ring-oscillator based PLL with pseudorandom dithering to eliminate spurs. This is also implemented in the 28nm test chip.

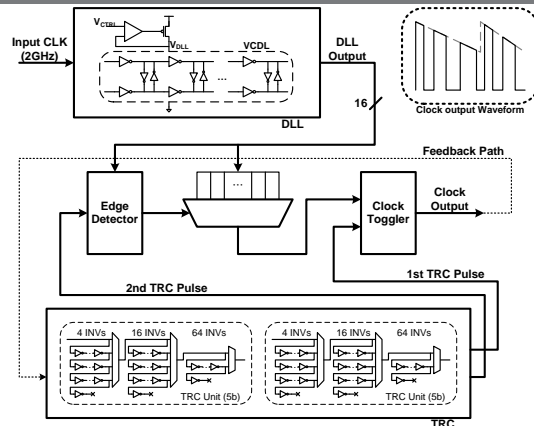


Figure 1: DLL-based clock generation

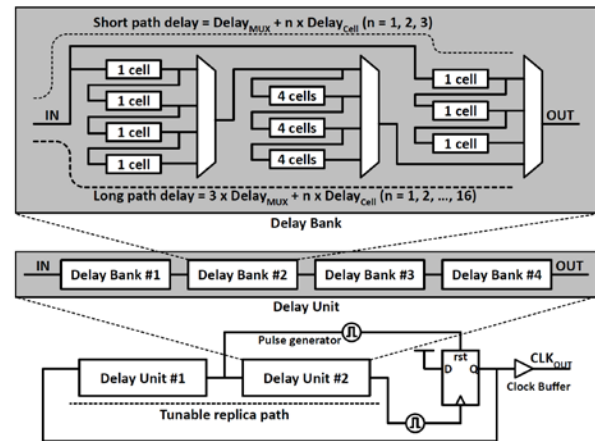


Figure 2: Self-timed clock generation

**Keywords:** CMOS, clock, manycore, DLL, PLL

## INDUSTRY INTERACTIONS

Intel, AMD, Freescale, GlobalFoundries

## MAJOR PAPERS/PATENTS

- [1] B. Zimmer, *et al*, "A RISC-V vector processor with simultaneous-switching switched-capacitor DC-DC converters in 28nm FDSOI," *IEEE Journal of Solid-State Circuits*, 2016, vol. 51, no. 4, pp. 930-942, Apr. 2016.
- [2] J. Kwak, B. Nikolić, "A 550-2260MHz Self-Adjustable Clock Generator in 28nm FDSOI," *Proc. A-SSCC*, Xiamen, Fujian, China, November 9-11, 2015.
- [3] B. Keller, *et al*, "Sub-microsecond adaptive voltage scaling in a 28nm FD-SOI processor SoC," to be presented at *ESSCIRC'16*, Lausanne, Switzerland, Sept. 12-15, 2016.



# TASK 1836.137, 50 GS/S AND BEYOND FREQUENCY-INTERLEAVED ENERGY-EFFICIENT ADCS

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## SIGNIFICANCE AND OBJECTIVES

This research explores a novel ADC technique referred to as frequency-interleaved analog-to-digital conversion (FI-ADC) for improving the performance of very high-speed ADCs. Performance of conventional high-speed ADCs is ultimately limited by jitter and we aim to determine if and how the FI-ADC can mitigate the jitter sensitivity of high-speed ADCs.

## TECHNICAL APPROACH

One of the key areas of focus of this work was to develop a comprehensive model for comparing the FI-ADC to the time-interleaved ADC (TI-ADC). A quantitative analysis was performed in addition to system-level simulations that compare the two architectures. The simulations support the theoretical findings and additionally provide further insight into the conditions under which the FI-ADC outperforms the TI-ADC. The second focus of this research was the development of a fully integrated FI-ADC system with 25GHz of bandwidth (50 GS/s) and 6b of resolution. For the first phase, a 25 GHz channelizing front-end was taped out. The front-end performs channelization, down-conversion, filtering and LO generation/distribution.

## SUMMARY OF RESULTS

Previous research has asserted that the FI-ADC has reduced jitter sensitivity due to the reduction in bandwidth presented to the sampling network, but fell short of providing a complete analysis of the impact of phase noise introduced during the down-conversion. Quantitative analysis shows that the phase noise present in the LO chain used for down conversion plays a critical role in determining if the FI-ADC outperforms the more traditional TI-ADC architecture. In general, the FI-ADC has great potential to improve performance for high input frequencies but sacrifices performance at lower frequencies. While SNR degradation due to jitter for a high frequency input signal will occur predominantly in one channel, other sources of errors, such as quantization noise, will manifest themselves in all channels, getting multiplied by number of channels effectively.

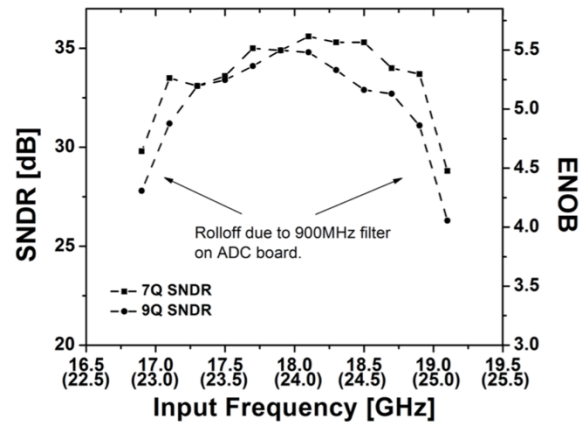


Figure 1: Measurement results for FI-ADC prototype front-end

Figure 1 shows SNR and equivalent ENOB for first prototype in a 65nm CMOS process. The analog front end (AFE) is responsible for channelizing and down-converting the wideband signal before presenting it to the baseband sub-ADCs assigned to each channel. In addition, the AFE must generate the multiple LO signals needed for mixing. By utilizing a front-end distributed amplifier and high-frequency harmonic rejection mixers, the AFE is capable of distributing and channelizing a 25 GHz signal with sufficient SNR and linearity for a 5-6b system. The AFE achieves an IIP3 of +5dBm and peak output SNDR of 34 dB for a 25 GHz input signal, which equates to 5.3b ENOB.

In future work, a new version of the AFE will be designed and fabricated using a 28nm process, utilizing a new architecture for channelization and a new LO distribution network. Optimization of the LO generation/distribution is crucial for FI-ADC to outperform TI-ADC in terms of power efficiency.

**Keywords:** high-speed ADCs, frequency-interleaved analog-to-digital conversion (FIADC)

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] BWRC retreat and poster presentations.

# TASK 1836.141, IC DESIGN FOR RESILIENCE AGAINST SYTSEM-LEVEL ESD

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## SIGNIFICANCE AND OBJECTIVES

ESD-induced soft failures in systems originate as hardware faults. This project seeks to develop integrated circuit designs that are resilient to power-on ESD. It also contributes to development of behavioral models of an IC's response to ESD that can be used for system design with ESD robustness.

## TECHNICAL APPROACH

Custom-designed CMOS test chips are subjected to IEC 61000-4-2 system-level ESD testing. The test chips are designed such that a variety of soft failures can be detected: bit flips in logic, glitches at input pins, supply noise, and latch-up. With a better understanding of soft failure mechanisms and vulnerable circuits, ESD failures can be minimized using a two-pronged approach: (i) ESD-robust IC design; (ii) system design for ESD noise reduction. System design for ESD robustness will be aided by ESD-models of the system components. Thus, behavioral modeling approaches for capturing component ESD susceptibility are investigated.

## SUMMARY OF RESULTS

The widely-used active rail clamp circuit was developed (in 1993) to provide component-level ESD protection. We have demonstrated several design modifications to the trigger circuit that lower the clamp's turn-on voltage during power-on ESD, potentially enabling it to provide system-level ESD protection. Previously, we presented a theoretical analysis of active rail clamp stability under power-on ESD conditions. This year, experimental proof of the analysis was obtained using wafer-level test structures fabricated in 65-nm CMOS. Depending on the number and relative values of the poles in the trigger circuit, oscillations were induced on the supply (Fig. 1).

A second threat to on-chip power integrity during system-level ESD was identified. Direct discharge to an electronic system may result in some of the ESD current entering the signal pin of an IC. The current return path from the IC to the board is through the multiplicity of power and ground pins. If there is non-negligible inductance separating the board-level and chip-level power nets, as is the case for wirebonded packages, the large time-derivative of the ESD current waveform ( $di/dt$ ) can result in the temporary discharging of the on-chip supply (Fig. 2).

Our experimental studies have established that mobile and tethered systems have similar soft failure

susceptibility. Soft failures originate from magnetic coupling between traces (input glitches), on-chip supply noise, substrate current injection, and radiated fields from the ESD gun.

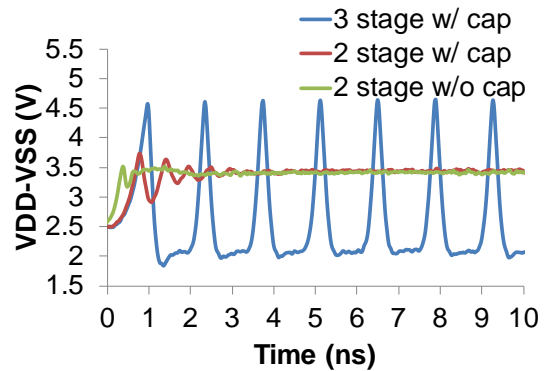


Figure 1: Response of a 2.5 V on-chip power supply to 0.6A ESD current injection. The trigger circuit for the active rail clamp test circuits has either 2 or 3 stages; the 3-stage design becomes unstable in response to power-on ESD. The on-chip supply decoupling capacitance was left off from one test structure to ascertain its effect

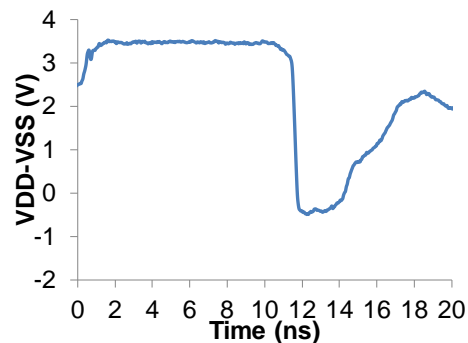


Figure 2: Supply collapse is observed at the tail-end of a 10ns ESD current pulse. Measurement result

**Keywords:** ESD, soft failures, behavioral models

## INDUSTRY INTERACTIONS

Texas Instruments, Intel, NXP, GlobalFoundries

## MAJOR PAPERS/PATENTS

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# TASK 1836.145, RF AND MIXED SIGNAL QUANTUM CMOS DEVICES AND CIRCUITS

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## SIGNIFICANCE AND OBJECTIVES

This project pioneers a path towards explicit quantum mechanical operation in industrial CMOS by demonstrating a new class of quantum MOS devices and circuits. This work will develop understanding of quantum MOS device physics and incorporation of such devices into RF and mixed-signal circuits operating at or near room temperature.

## TECHNICAL APPROACH

This project introduces quantum well (QW) NMOS transistors showing quantum transport characteristics in the form of negative differential transconductances (NDTCs). A main focus is to understand the device physics and how to make QW NMOS devices useful in circuits designed to exploit the NDTCs. In the past year, full temperature and gate length dependencies have been measured on a set of QW NMOS fabricated by Texas Instruments using a 45nm process. A prototype folding amplifier frequency multiplier circuit using the quantum NDTC has been designed and demonstrated.

## SUMMARY OF RESULTS

Over the second year of this project we completed full temperature ( $T$ ) and gate length ( $L$ ) dependence measurements on the NDTC transfer characteristic of a set of QW NMOS devices fabricated in a TI 45nm technology. The systematics of  $L$  dependence showed that QW NMOS devices with  $L = 35, 40,$  and  $45$  nm typically showed 3, 2, and 1 NDTC regime(s), respectively, consistent with the interpretation that the NDTCs arise from transport through quantum bound states in QWs of different lengths. The  $T$  dependence is summarized in Fig. 1, where it is seen that the drain-source current  $I_{DS}$  decreases and the NDTC strength, as measured by the current peak-to-valley ratio (PVR), increases in a thermally activated manner from room temperature down to  $\sim 125$  K. Below 125 K both  $I_{DS}$  and PVR saturate, consistent with a quantum tunneling transport mechanism.

We also designed and built a folding amplifier frequency multiplier circuit using a QW NMOS to generate a folded current-voltage transfer function via its NDTC. Time domain data shows frequency doubling in the kHz range at room temperature, as shown in Fig. 2. Fourier analysis confirms that the output is dominated by the second harmonic of the input. De-embedding the circuit para-

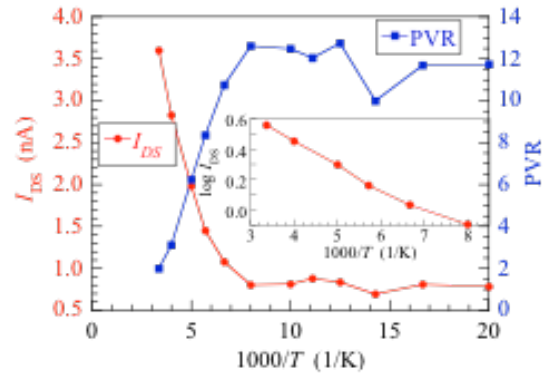


Figure 1: Temperature dependencies of  $I_{DS}$  and the NDTC strength as measured by PVR

-sitic impedances suggests that the doubling bandwidth could approach 10 GHz in an integrated circuit. This work is the first example of a silicon QW device fabricated by mainstream - CMOS technology being used in a circuit application and establishes the feasibility of scalable CMOS integrated circuits that exploit explicit quantum transport.

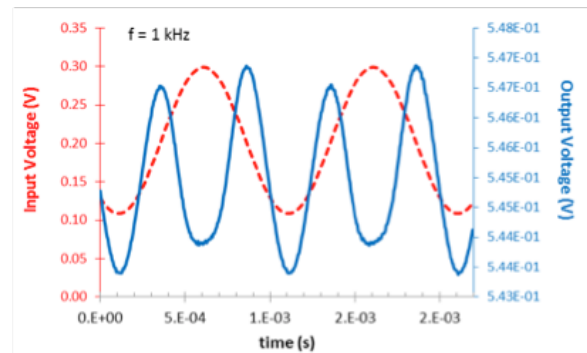


Figure 2: Plots of input (red, dashed line) and output (blue line) voltages vs. time showing frequency doubling at 1 kHz

**Keywords:** quantum devices, quantum circuits, negative differential conductance, quantum well, quantum CMOS

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

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# TASK 1836.148, 50GSPS+ TI HYBRID SAR ADC ARRAY WITH COMPREHENSIVE DDI CALIBRATION

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## SIGNIFICANCE AND OBJECTIVES

Time interleaving is an effective way to increase analog-to-digital conversion (ADC) speed. A low-power, high-speed sub-ADC is needed to reduce the interleaving complexity and power consumption. This work introduces a V-T hybrid two-step SAR ADC to meet both the speed and the efficiency target. Also, a reference dither based skew calibration is introduced to calibrate the timing mismatch of the interleaving array.

## TECHNICAL APPROACH

A comparator's resolving time is roughly inversely proportional to its input voltage magnitude. In this work the comparator resolving time of residue voltage on the summing node of a SAR ADC is quantized by the second-stage time-to-digital converter (TDC), resulting in an efficient two-step quantization structure. A slow-but-accurate reference ADC with precise timing is introduced and used as timing reference of the array. The ref. ADC clock is modulated by a 1b pseudorandom signal and the skew information is extracted by correlating the PN signal with the output difference between the ref. ADC and the sub-ADCs.

## SUMMARY OF RESULTS

A 16-way interleaved ADC prototype is implemented in a 28nm CMOS technology. The proposed skew calibration technique can suppress the timing spurs below 50dB with a Nyquist input. And the total power consumption is only 23mW, thanks to the hybrid SAR approach. We essentially achieved an FoM of 42fj/step, which is the best among recent state-of-the-art works.

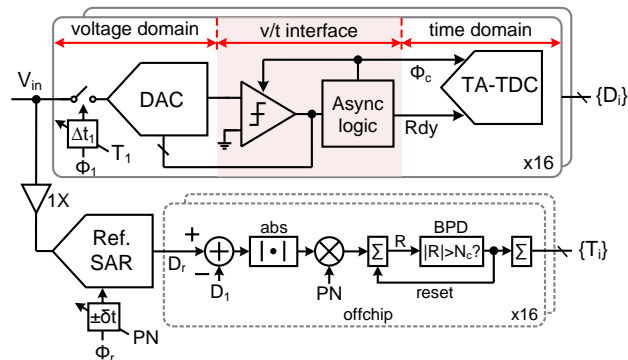


Figure 1: Proposed TI-ADC system with skew mismatch calibration

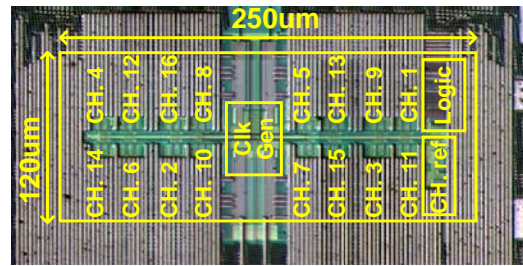


Figure 2: Prototype die photo (28nm CMOS)

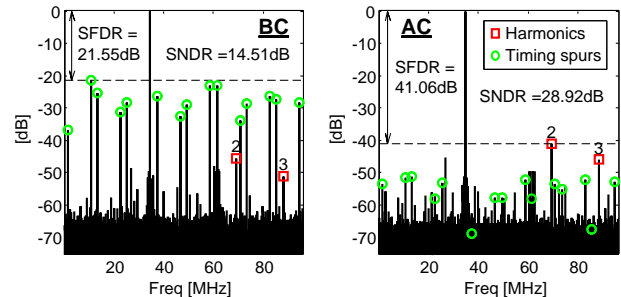


Figure 3: Output FFT before and after skew calibration with 11.9GHz sine wave input at 24GS/s

	Ours	VLSI13-IBM	ASSCC14-IBM	VLSI15-TAMU	ISSCC14-CMU
Tech	28nm	32nm SOI	32nm SOI	65nm	32nm SOI
Fs(GS/s)	24	8.8	36	25	20
SNDR(dB)	29	38.5	31.6	29.7	30.1
Power (mW)	23	35	110	88	69.5
Area (mm <sup>2</sup> )	0.06	0.025	0.048	0.24	0.25
FoM	42	58	98	143	124

Table 1: Performance Comparison (projected)

**Keywords:** TI-ADC, calibration, hybrid SAR, reference-ADC equalization, direct derivative information

## INDUSTRY INTERACTIONS

Texas Instruments, Intel

## MAJOR PAPERS/PATENTS

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