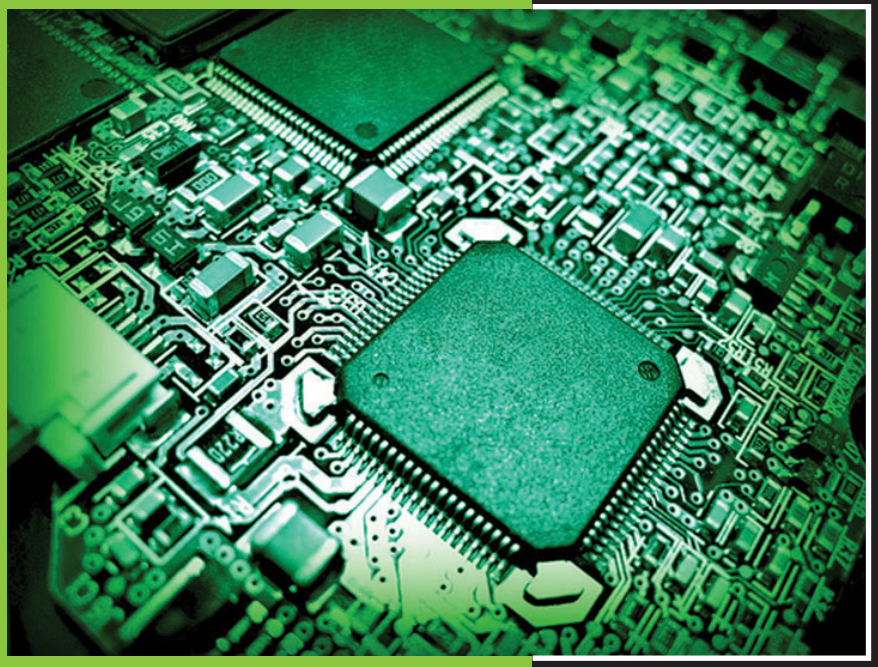
# TEXAS ANALOG CENTER OF EXCELLENCE

## ANNUAL REPORT 2011-2012



SRC

TxACE
TEXAS ANALOG
CENTER OF EXCELLENCE

# OUR MISSION

***The Texas Analog Center of Excellence seeks to create fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, healthcare, public safety and security.***

# OUR RESEARCH THRUSTS

- **Safety & Security**
- **Healthcare**
- **Energy Efficiency**
- **Fundamental Analog Circuits Research**

# TxACE 2011-2012 ANNUAL REPORT

The Texas Analog Center of Excellence (TxACE) located at the University of Texas at Dallas is the largest analog research center based in an academic institution. It is also a global center. Analog and mixed signal integrated circuits engineering is both a major opportunity and challenge. The increasing importance of analog integrated circuits in electronic systems and the emergence of new applications are providing an exciting opportunity. However, the inherent difficulty of the art makes it challenging. Creation of advanced wireless technology and sophisticated sensing and imaging devices depends on the availability of engineering talent for analog research and development. TxACE was established to help translate these opportunities into economic benefits by overcoming the challenge and meeting the need. Support for TxACE has been provided through a collaboration of the state of Texas, Texas Instruments, the Semiconductor Research Corporation, the University of Texas System, and the University of Texas at Dallas. Figure 1 shows the location of member institutions, including four international members.

The research tasks are organized into four research thrust areas: Health Care, Safety and Security, Energy Efficiency and Fundamental Analog. The scope of investigation extends from circuits operating at dc through terahertz, data converters that sample at a few samples/sec to 10s of giga-samples/sec, ac-to-dc and dc-to-dc converters working at μW to Watts, energy harvesting circuits, protein and DNA sensors and many more. Significant improvement on existing mixed signal systems and new applications based on this circuit research are anticipated. Students who have been exposed to hands-on innovative research are forming the leading edge of analog talent flow into industry. Close collaboration with and responsiveness to industry needs provide focus to the educational experience.

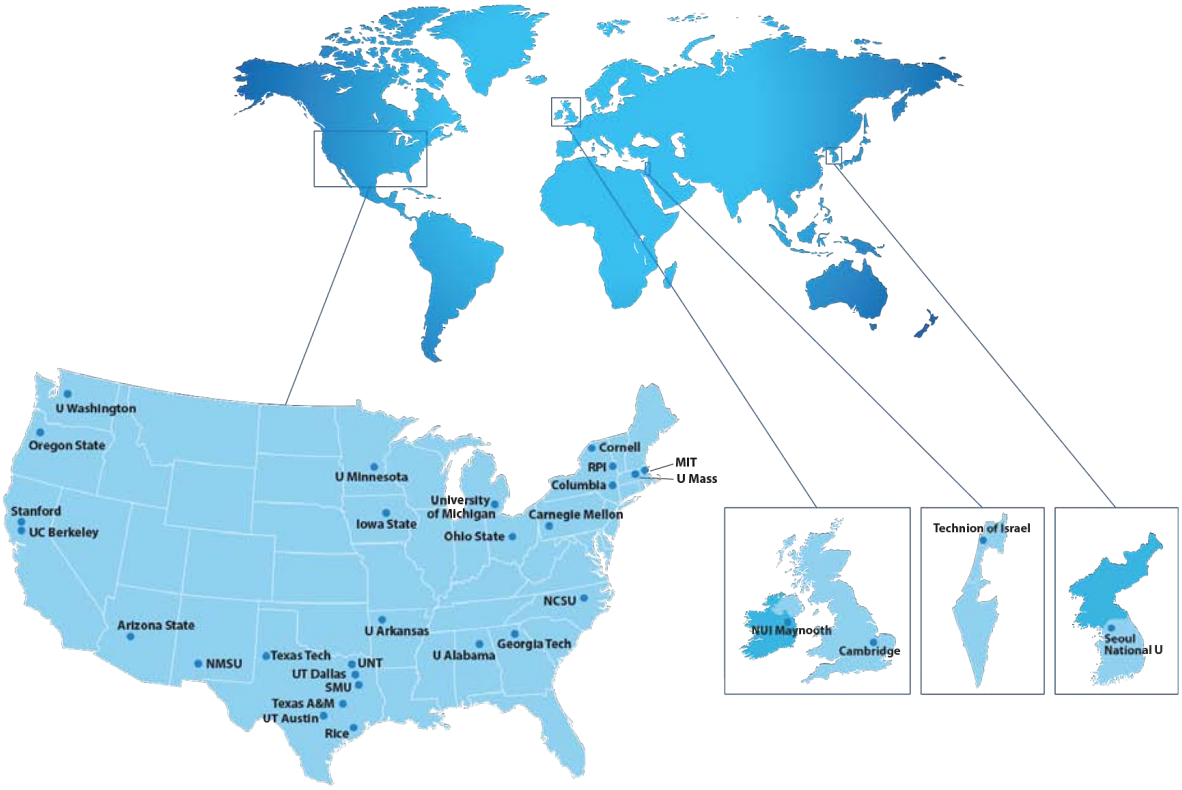



**Figure 1: Member institutions of Texas Analog Center of Excellence**

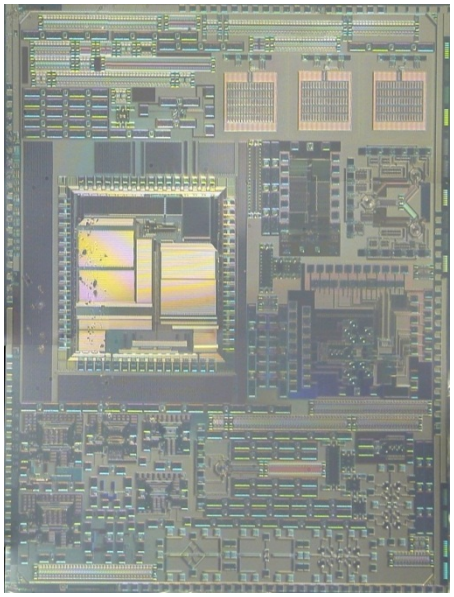


**Figure 2: Integrated circuit in TI 65-nm CMOS aggregated by TxACE (Participating Institutions: RPI, UT Austin, UT Dallas)**

## DIRECTOR'S MESSAGE

The Texas Analog Center of Excellence (TxACE) is leading analog research and education that creates new economic opportunities. Last year, TxACE researchers published 24 journal and 94 conference papers. They also made four invention disclosures and filed one patent application. One patent has been granted. Twenty-six PhD and 17 MS students of TxACE have graduated.

TxACE is the largest center based in an academic institution for analog research in the world (68 principle investigators from 31 academic institutions). We added one more international member, Technion of Israel, increasing the number of international members to four. Seven universities (Rice, SMU, Texas A&M, Texas Tech, UNT, UT Austin, UT Dallas) are from the state of Texas. During the last year, the Center supported 107 graduate students.

TxACE laboratories and design facilities are fully functional. They form probably the best laboratory for electronic circuits research. The TxACE high frequency circuit characterization tools are helping to lower a critical barrier for advancing millimeter and sub-millimeter wave integrated circuit technology. Laboratory use by researchers outside of UT Dallas is increasing. These capabilities are a global asset.

This year TxACE, with the support of Semiconductor Research Corp. and Texas Instruments Inc., started a new program to improve fabrication access. TxACE researchers now can fabricate circuits at a significant discount. I thank Dr. David Yeh of SRC and Prof. Yun Chiu of UT Dallas for leading this effort. The first run using UMC 130-nm CMOS was taped out in July. TxACE has also aggregated two chips for fabrication using a TI 65-nm process (Figure 2). We plan additional and more frequent runs at the 130 and 65-nm nodes.

I am happy to report that SRC, TI and UT Dallas have finalized the renewal of the Center for another three years. The Center is continuing to work with the State for additional research support. Looking back the last three years, we were more than successful in establishing the Center due to the hard work of principal investigators and students, and the generous support of the state of Texas, UT Dallas, the University of Texas System, TI, and SRC. I thank the TxACE team.

For the Center to be successful the next three years, the impact of our research and education programs should be evident. I look forward to work with the TxACE team to make this happen.

**Kenneth K. O, Director TxACE**
**Texas Instruments Distinguished Chair**
**The University of Texas at Dallas**

## BACKGROUND & VISION

For many years semiconductor electronics was driven by digital logic. This led to the digital revolution that we are all familiar with; impacting things from computational power to high definition digital television. For the next 20 years, analog and mixed signal semiconductor technology is expected to drive progress as electronics continues to bridge the gap between the analog real world and the digital information infrastructure. High performance analog technology is a unique segment of the semiconductor electronics business. It requires special skills in both design and process that reside predominantly in the United States.

To lead this change, in particular to lead analog technology education, research, commercialization, manufacturing, and job creation, the Texas Analog Center of Excellence was formally announced by Texas Governor Rick Perry in October 2008 as a collaboration of the Semiconductor Research Corporation, the state of Texas through its Texas Emerging Technology Fund, Texas Instruments Inc., the University of Texas system and the University of Texas at Dallas (see Figure 3). The center seeks to accomplish these objectives by creating fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, healthcare, and public safety and security.

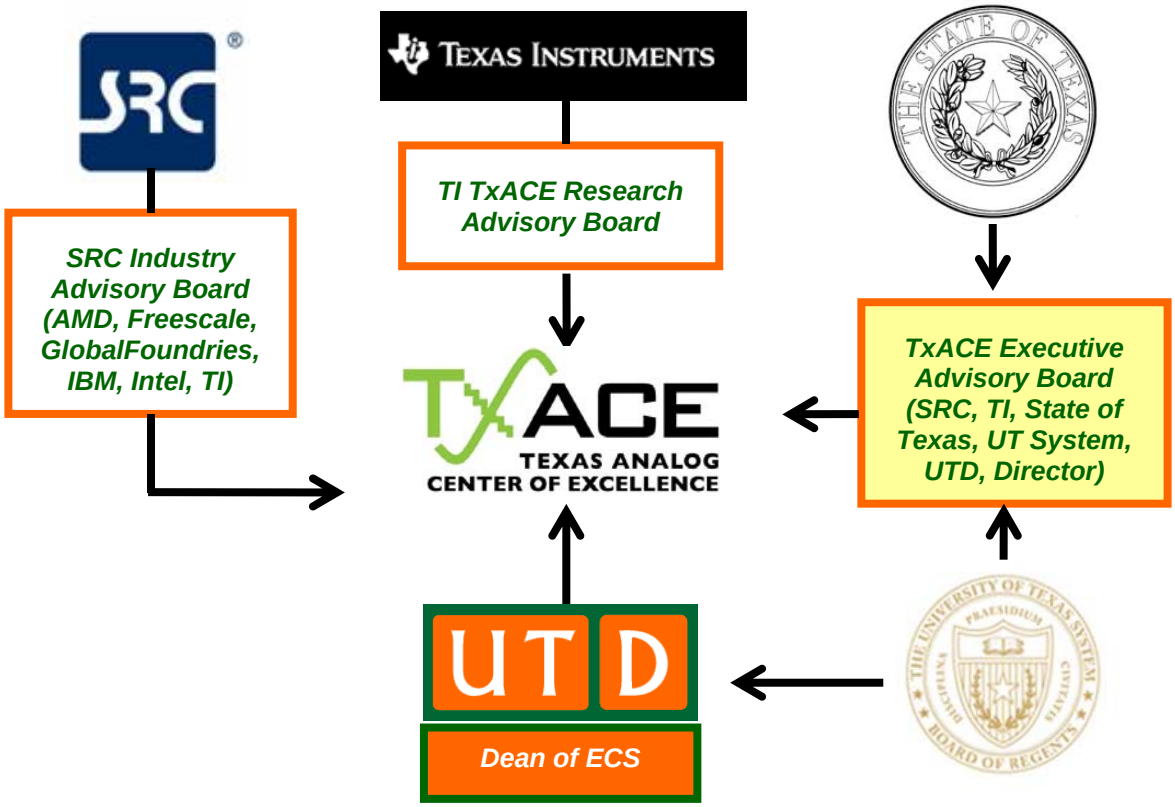



**Figure 3: TxACE organization relative to the sponsoring collaboration**

## CENTER ORGANIZATION

The Texas Analog Center of Excellence is guided by agreements established with the Center sponsors. Members of the industrial advisory boards identify the research needs and select research tasks in consultation with Center leadership. Figure 3 diagrams the relationship of TxACE to the members of the sponsoring collaboration.

Figure 4 identifies the elements of the organization. TxACE Director is Professor Kenneth K. O. The research is arranged into four thrusts that comply with the mission of the Center: Safety and Security, Health Care, Energy Efficiency and Fundamental Analog Research. The fourth thrust consists of vital research that cuts across more than one of the first three research thrusts. The thrust leaders are Prof. Brian A. Floyd of North Carolina State University for safety and security, Prof. Ramesh Harjani of the University of Minnesota for the health care, Prof. D. Ma of the UT Dallas for energy efficiency, and Prof. D. Allstot of the University of Washington for fundamental analog research. The thrust leaders and Prof. Yun Chiu of the UT Dallas form the executive committee. The committee, along with the director, form the leadership team that works to improve the research productivity of center by increasing collaboration, better leveraging the diverse capabilities of principle investigators of the center, and lowering research barriers. The leadership team also identifies new research opportunities for consideration by the industrial advisory boards members.

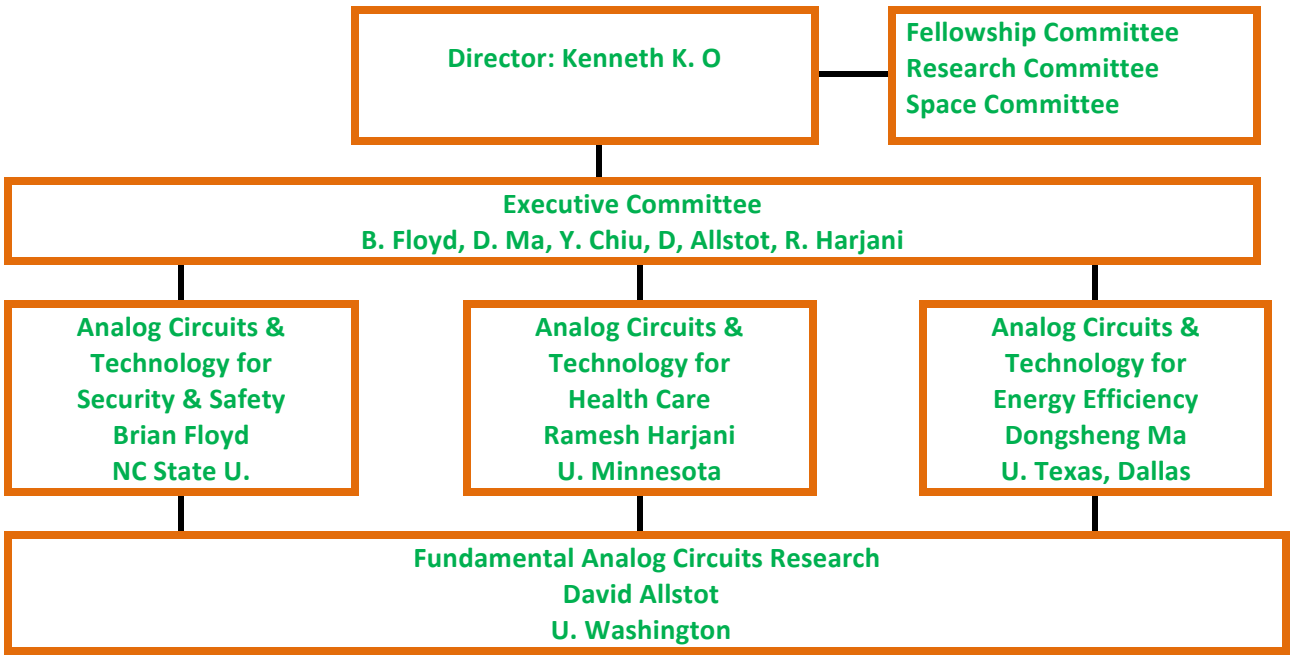



**Figure 4: TxACE organization for management of research**

## PUBLIC SAFETY AND SECURITY

(Thrust leader: Brian Floyd, NC State University)

TxACE has awarded nearly $3 million to researchers to develop analog technology that enhances public safety and security. The projects are intended to: 1) Enable a new generation of devices that can scan for harmful substances by researching 200-300-GHz silicon ICs for use

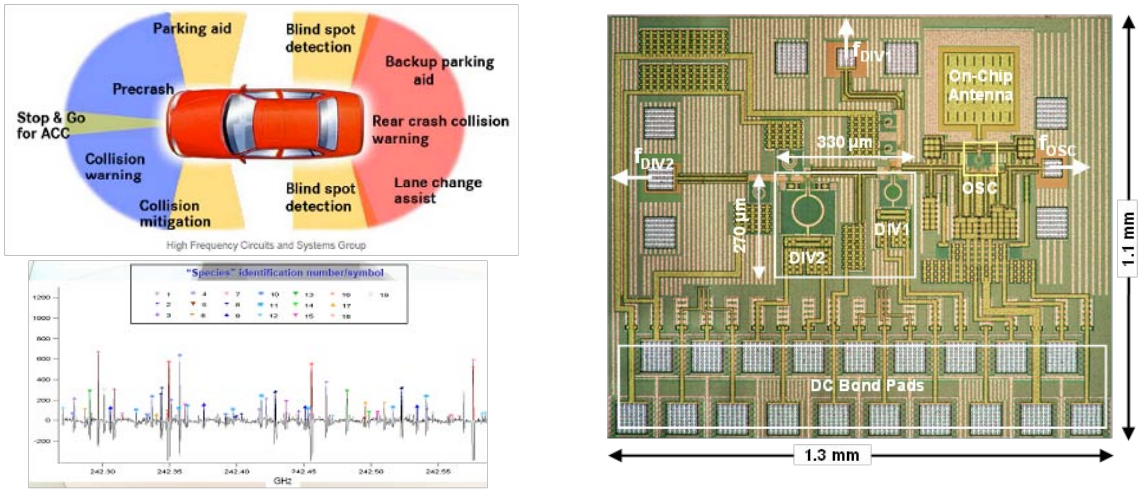


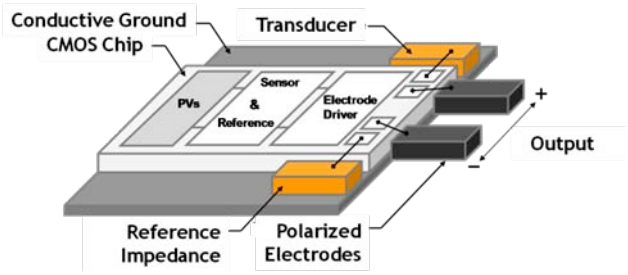

**Figure 5: Millimeter wave radar to improve automobile safety and rotational spectrum around 300 GHz. 400-GHz phase locking circuit in 45-nm CMOS (O, UT Dallas).**

in spectrometers and 2) Significantly reduce the cost of on-vehicle radar technology to improve automotive safety by researching circuit techniques that can improve manufacturing and lower test and packaging costs.

## HEALTH CARE

(Thrust leader: Ramesh Harjani, University of Minnesota)

Analog and RF integrated circuit technology is the essential interface enabling the power, speed and miniaturization of modern digital microelectronics to be brought to bear on an array of medical issues, including medical imaging, patient monitoring, laboratory analyses, bio-sensing and new therapeutic devices. TxACE is working to identify and support analog circuit research challenges that have the potential to enable important health-related applications. As part of this, TxACE has started a new effort to address the contact problem of EEG.



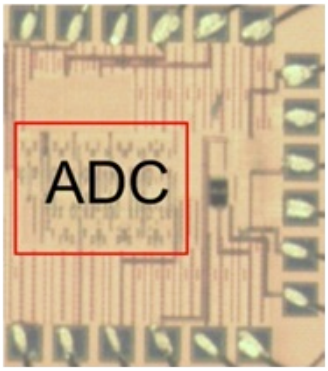
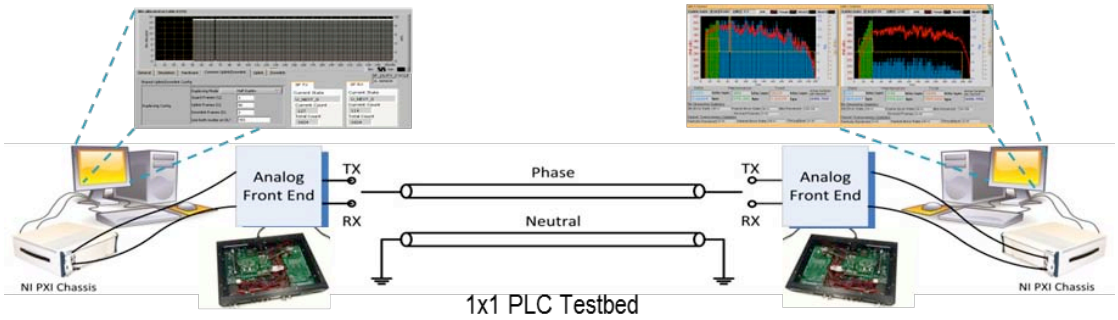




**Figure 6: (Left) Electronics and signal processing for EEG (R. Jafari, UT Dallas), (Right top) Photo-voltaic powered implantable medical sensor compatible to MRI (A. Hassibi, UT Austin) and (Right bottom) 8-bit 2ksamples/sec analog-to-digital converter for implantable sensor applications that consumes 101 nW (D. Lie, Texas Tech.).**

## ENERGY EFFICIENCY

(Thrust leader: Dongsheng Brian Ma, UT Dallas)

TxACE is committed to alleviate the global energy problem by improving the energy efficiency of electronic systems as well as by developing analog technologies that can make energy generation more efficient. The Center is also working to energize and power long-lasting in-situ microscale devices such as wireless microsensors, biomedical implants, and portable microelectronics.



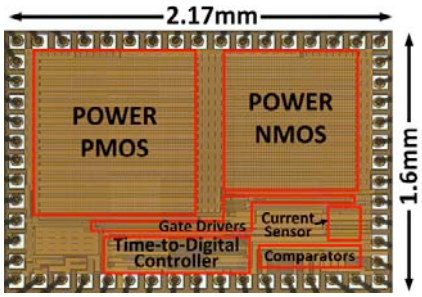




**Figure 7: (Top) Single transmitter and single receiver testbed for studying power line communication (PLC). Cyclostationary noise model for narrow band PLC has been accepted to IEEE P1901.2 standard. (B. Evans, UT, Austin). (Left) LED driver integrated circuit (H. Lee, UT Dallas) for enabling a large scale deployment of LED lighting which can reduce the US electricity demand by more than 20%**

## FUNDAMENTAL ANALOG CIRCUITS RESEARCH

(Thrust leader: David Allstot, University of Washington)

Research in this thrust focuses on cross-cutting areas in Analog Circuits which impact all of the TxACE application areas (Energy Efficiency, Health Care, Public Safety and Security). Fundamental analog circuits' research is crucial for the design of analog-to-digital converters and communication links, the development of CAD tools, and testing of high speed circuits.

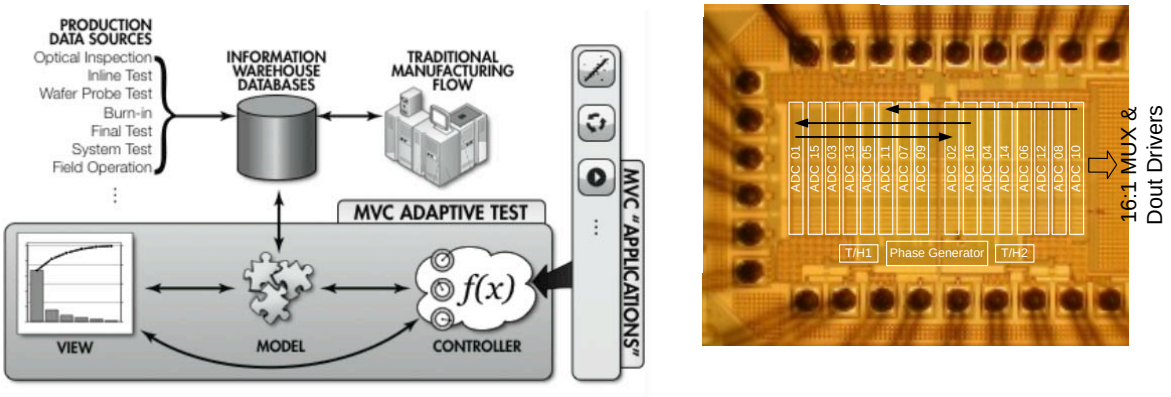



**Figure 8: (Left) Model view controller platform with integrated statistical learning theory controllers for adaptive testing that can reduce test time by an order of magnitude (Y. Makris, UT Dallas. (Right) 6b 1.6GS/s SAR ADC with embedded 1-tap DFE was implemented in an LP 90nm CMOS process and achieved 4.75b ENOB at 0.46pJ/conv. (S. Palermo, TAMU)**

## TXACE ANALOG RESEARCH FACILITY

The University of Texas at Dallas (UT Dallas) has renovated a ~8,000 $ft^2$ area on the third floor of the Engineering and Computer Science North Building to form an enhanced centralized group of laboratories dedicated to analog engineering research and research training. (Appendix I) The facility includes RF and THz, Integrated System Design, Embedded Signal Processing, and Analog & Mixed Signal laboratories, as well as a CAD/Design laboratory structured to promote collaborative research**.** The unique instrumentation capability includes network analysis and linearity measurements up to 325 GHz, spectrum analysis up to 20 THz, cryo-measurements down to $2^oK$, and multiple harmonic load pull measurements up to 48 GHz for the third order harmonic. The close proximity of researchers in an open layout enables natural interaction and compels sharing of knowledge and instrumentation among the students and faculty. The TxACE analog research facility is one of the best equipped university based electronics laboratories. The laboratory is available for use by TxACE researchers all over the world.

## RESEARCH PROJECTS AND INVESTIGATORS

The Texas Analog Center of Excellence (TxACE) is the largest university analog technology center in the world. Table 1 lists the names of the 68 principal investigators from 31 academic institutions with directed research tasks funded by TxACE. Seven schools (Rice, SMU, Texas A&M, Texas Tech, UNT, UT Austin, UT Dallas) are from the state of Texas. Twenty four are from outside of Texas. Four (Seoul National University, Korea; University of Cambridge, United Kingdom; National University of Ireland, Maynooth; and Technion – Israel Institute of Technology) are from outside of the US. Of the 68 investigators, 30 are from Texas. During the past year the Center supported 105 PhD and 2 MS students, and 26 PhD and 17 MS degrees were awarded to the TxACE students.

**Table 1: Principal and Co-Principal Investigators (September 2011 through August 2012)**

| Investigator | Institution | Investigator | Institution | Investigator | Institution |
|---|---|---|---|---|---|
| D. Allstot | U Washington | P. Hanumolu | Oregon State U | R. McMahon | Cambridge U |
| E. Alon | U Cal-Berkeley | R. Harjani | U. Minnesota | S. Mohanty | U North TX |
| D. Akinwande | UT Austin | A. Hassibi | UT Austin | U.-K. Moon | Oregon State U |
| A. Apsel | Cornell | M. Hella | RPI | B. Murmann | Stanford U |
| B. Banerjee | UT Dallas | R. Henderson | UT Dallas | S. Mukhopadhyay | Georgia Tech. |
| D. Blaauw | UT Dallas | R. Jafari | UT Dallas | B. Nikolic | U Cal-Berkeley |
| L. Bieris | UT Dallas | A. Karsilayan | Texas A&M U | K. O | UT Dallas |
| A. Blanchard | UT Dallas | B. Kim | U Alabama | V. Oklobdzija | NM State U. |
| S. Blanton | CMU | C. Kim | U Minnesota | S. Ozev | Arizona State |
| W. Burleson | U Mass | J. Kim | Seoul Nat. U | S. Palermo | Texas A&M U |
| A. Chatterjee | Georgia Tech | P. Kinget | Columbia U | J. Ringwood | Nui Maymooth |
| D. Chen | Iowa State U | E. Kougianos | U North Texas | J. Roychowdhury | U Cal-Berkeley |
| Y. Chiu | UT Dallas | F. Koushanfar | Rice University | M. Saquib | UT Dallas |
| F. De Lucia | Ohio State U | H. Lee | UT Dallas | R. Shi | U. Washington |
| J. Di | U Arkansas, Fayet. | C. Li | Texas Tech U | M. Shur | RPI |
| Y. Eldar | Technion | D. Lie | Texas Tech U | J. Silva-Martinez | Texas A&M U |
| K. Entesari | TAMU | P. Li | Texas A&M U | V. Stojanovic | MIT |
| B. Evans | UT Austin | X. Li | CMU | M. Torlak | UT Dallas |
| B. Fahimi | UT Dallas | S. Lim | GTech | E. Vogel | Georgia Tech. |
| B. Floyd | NC State U | J. Liu | UT Dallas | D. Wentzloff | U. Michigan |
| R. Geiger | Iowa State U | D. Ma | U Arizona | X.-C. Zhang | RPI |
| R. Gharpurey | UT- Austin | H.A. Mantooth | U Arkansas | D. Zhou | UT Dallas |
| P. Gui | SMU | Y. Makris | UT Dallas | | |

## SUMMARIES OF RESEARCH PROJECTS

The 88 research projects funded through TxACE during 2011-2012 are listed in Table 2 below by Semiconductor Research Corporation task identification number.

**Table 2: Funded research projects at TxACE by SRC task identification number (FA: Fundamental Analog, EE: Energy Efficiency, HC: Healthcare, S&S: Safety and Security)**

| # | Task | Thrust | Task Title | PI | Institution |
|---|---|---|---|---|---|
| 1 | 1836.004 | FA | Robust Design of Low Power Small Area Data Converters in Low Voltage Digital Processes | Geiger, Randall | Iowa St |
| 2 | 1836.006 | FA | Multi-Core and Distributed Parallel Simulation for Design and Verification of Custom Digital and Analog ICs | Li, Peng | Texas A&M University |
| 3 | 1836.010 | S&S | Digital Assisted Millimeter-Wave CMOS Circuits | O, Kenneth | UT Dallas |
| 4 | 1836.013 | FA | Wideband Receiver Architectures in Digital Deep Submicron CMOS | Hoyos, Sebastian | Texas A&M University |
| 5 | 1836.017 | EE | Performance-Oriented DVS-Compatible Single-Inductor Multiple-Output Power Converters | Ma, Brian | UT Dallas |
| 6 | 1836.019 | FA | Digitally-Enhanced Energy-Efficient High-Speed I/O Links | Shanbhag, Naresh | U of Illinois Urbana-Champaign |
| 7 | 1836.020 | FA | Low-Complexity High-Performance Analog-to-Digital Converters in Submicron CMOS | Moon, Un-Ku | Oregon St |
| 8 | 1836.021 | FA | CAD Algorithms and Tools for Fast and Accurate PLL Design in the Presence of Variability | Roychowdhury, Jaijeet | U of California-Berkeley |
| 9 | 1836.022 | FA | High-Speed MIMO Signaling Techniques for Single-Ended Parallel I/O | Harjani, Ramesh | U of Minnesota |
| 10 | 1836.030 | FA | Fast PVT-Tolerant Physical Design of RF IC Components | Mohanty, Saraju | U North Texas |
| 11 | 1836.031 | FA | Variation Tolerant Analog Design based on Generalized Kharitonov/Lyapunov Theory | Zhou, Dian | UT Dallas |
| 12 | 1836.032 | S&S | Millimeter Wave Phase-Locked Loop Design with Enhanced Tolerance to Process and Temperature Variation | Gharpurey, Ranjit | UT Austin |
| 13 | 1836.033 | S&S | MIMO Radar for Pixel Reduction in mm-Wave Imaging | Saquib, Mohammad | UT Dallas |
| 14 | 1836.034 | S&S | 77-81 GHz CMOS Transceiver with Built-In Self Test and Healing | Banerjee, Bhaskar | UT Dallas |
| 15 | 1836.035 | S&S | Development of CMOS Sub-Terahertz Receivers for Spectrometers | Banerjee, Bhaskar | UT Dallas |
| 16 | 1836.036 | S&S | Signal Generation for 200-300 GHz Spectrometer | O, Kenneth | UT Dallas |
| 17 | 1836.037 | S&S | Development of Antenna and Chip Interface Systems for Millimeter Wave and Sub-Millimeter Wave Applications | Henderson, Rashaunda | UT Dallas |
| 18 | 1836.038 | FA | A Hybrid 14-bit Analog-to-Digital Converter for Broadband Applications | Silva-Martinez, Jose | Texas A&M University |
| 19 | 1836.039 | S&S | UxIDs: Unclonable Mixed-Signal Integrated Circuits Identification | Koushanfar, Farinaz | Rice University |
| 20 | 1836.040 | FA | Energy-Efficient CMOS 10GS/s 6-bit ADC with Embedded Equalization | Palermo, Sam | Texas A&M University |

## Table 2: continued

| # | Task | Thrust | Task Title | PI | Institution |
|---|---|---|---|---|---|
| 21 | 1836.041 | EE | A High-Efficiency Single-Inductor Multiple-Input Multiple-Output Integrated DC/DC Converter for Energy-Harvesting Applications | Lee, Hoi | UT Dallas |
| 22 | 1836.042 | HC | Adaptive Data Prediction Based Receiver for Power-Efficient High-Resolution Ultrasound Imaging Systems | Ma, Brian | UT Dallas |
| 23 | 1836.043 | HC | High-Voltage Amplifier Technology | Gui, Ping | Southern Methodist |
| 24 | 1836.044 | FA | Statistical Models and Methods for Design and Test of Non-Digital Components | Li, Xin | Carnegie Mellon |
| 25 | 1836.046 | FA | Reconfigurable Antenna Interface for Low-Power Wireless Sensor Nodes | Allstot, David | U of Washington |
| 26 | 1836.047 | S&S | Integration of Millimeter Wave Antennas Using System in Package Techniques | Henderson, Rashaunda | UT Dallas |
| 27 | 1836.048 | S&S | Millimeter and Submillimeter Gas Sensors: System Architectures for CMOS Devices | De Lucia, Frank | Ohio State |
| 28 | 1836.052 | HC | An Ultra-low Power Signal Processing with Smart Analog-enabled Pre-Conditioning Stage for Inertial Sensing Applications | Jafari, Roozbeh | UT Dallas |
| 29 | 1836.053 | EE | High-Efficiency Highly-Integrated LED Driver Systems for Solid-State Lighting Applications | Lee, Hoi & Zhou, Dian | UT Dallas |
| 30 | 1836.054 | S&S | Silicon Based Beamforming Arrays for Millimeter Wave Systems | Torlak, Murat | UT Dallas |
| 31 | 1836.055 | HC | SPICE Models and Analog Circuits for Nanoscale Silicon Chemical- and Biological-Sensors | Vogel, Eric | UT Dallas |
| 32 | 1836.057 | FA | High Accuracy All-CMOS Temperature Sensor with Low-Voltage Low-Power Subthreshold MOSFETs Front-End and Performance-Enhancement Techniques | Li, Changzhi | Texas Tech University |
| 33 | 1836.058 | FA | Hierarchical Model Checking for practical Analog/Mixed-Signal Design Verification | Li, Peng | Texas A&M University |
| 34 | 1836.059 | FA | Power-Efficient 10-20GS/s ADCs for High-Speed Communications | Liu, Jin | UT-Dallas |
| 35 | 1836.060 | EE | Design Techniques for Scalable, Sub-1mW/Gbps Serial I/O Transceivers | Palermo, Sam | Texas A&M University |
| 36 | 1836.061 | HC | Analog Computing in Human Cells | Bleris, Leonidas | UT Dallas |
| 37 | 1836.062 | EE | System-Level Models and Design of Power Delivery networks with On-Chip Voltage Regulators | Li, Peng | Texas A&M University |
| 38 | 1836.063 | EE | Power line Communications for Enabling Smart Grid Applications | Evans, Brian | UT Austin |
| 39 | 1836.064 | HC | Ultra-Low-Power Analog Front-End IC Design for Implantable Cardioverter Defibrillator | Lie, Donald | Texas Tech University |
| 40 | 1836.065 | EE | Energy Efficient Comparator Elements for A/D Converters and High-Speed I/Os | Stajanovic, Vladmir | MIT |
| 41 | 1836.066 | HC | A Fully-Integrated CMOS Platform for Microwave-Based Label-Free DNA Sensing | Entesari, Kamran | Texas A&M University |
| 42 | 1836.067 | S&S | Characterization of CMOS Basic Building Blocks for Sub-THz Wideband Transmitters | Hella, Mona | Rensselaer Polytechnic |
| 43 | 1836.068 | EE | Global Convergence Analysis of Mixed-Signal Systems | Kim, Jaeha | Seoul National University |
| 44 | 1836.069 | EE | Electronic Systems for Small-Scale Wind Turbines | McMahon, Richard | Cambridge University |

## Table 2: continued

| # | Task | Thrust | Task Title | PI | Institution |
|---|---|---|---|---|---|
| 45 | 1836.070 | EE | Optimum Control of Power converters | Ringwood, John | National U of Ireland Naymooth |
| 46 | 1836.071 | HC | Design of Photovoltaic (PV) Power Harvesting CMOS ICs | Hassibi, Arjang | UT Austin |
| 47 | 1836.072 | S&S | Low Cost Test of High Speed Signals | Chatterjee, Abhijit | GA Tech |
| 48 | 1836.074 | S&S | Sub-45nm Circuits for True Random Number Generation and Chip Identification | Burleson | U Mass |
| 49 | 1836.075 | FA | Design of 3D Integrated Heterogeneous Systems | Mukhopadhyay, S. | GA Tech |
| 50 | 1836.076 | EE | Ultra-Low Power Delay-Insensitive Asynchronous Circuits | Di, Jia | U Arkansas/ Fayet |
| 51 | 1836.077 | FA | Statistical Characterization of Circuit Aging | Kim, Chris | U Minnesota |
| 52 | 1836.078 | FA | High-Resolution, Charge-Based A/D Converters for Nano-CMOS Technologies | Murmann, Boris | Stanford |
| 53 | 1836.079 | S&S | CMOS THz Generation and Detection | Hella, Mona | RPI |
| 54 | 1836.080 | FA | Variation-Tolerant Noise-Shaping ADCs With Embedded Digital Bias and V(DD) Scalable from 0.5V to 1.2V for Nanoscale CMOS | Kinget, Peter | Columbia |
| 55 | 1836.081 | EE | Combined Inductive/Capacitive DC-DC Converter for Efficient Dynamic Voltage Scaling | Harjani, Ramesh | U Minnesota |
| 56 | 1836.082 | S&S | Low-Cost Energy-Efficient 60GHz Transceivers with Built-In Test (BIST) | Alon, Elod | U Cal-Berkeley |
| 57 | 1836.083 | S&S | Built-In Test for Millimeter-Wave Phased Arrays | Floyd, Brian | NCSU |
| 58 | 1836.084 | S&S | Analog, Mixed-Signal and RF/High Speed Test | Ozev, Sule | Ariz. SU |
| 59 | 1836.085 | EE | CMOS Switched-Capacitor Power Amplifier Techniques | Allstot, David | U Washington |
| 60 | 1836.086 | FA | Variation Tolerant Calibration Circuits for High Performance I/O | Apsel, A. | Cornell |
| 61 | 1836.087 | FA | An Anyrate Reference-less Digital Clock-Data-Recover (CDR) with Decoupled Jitter Transfer and Jitter Tolerance Bandwidths | Gui, Ping | SMU |
| 62 | 1836.088 | EE | Efficient Digital-Intensive Wireless Transmitters Utilizing Switching Mode PAs | Gharpurey, Ranjit | UT Austin |
| 63 | 1836.089 | EE | Energy Efficient Comparator Elements for A/D Converters and High-Speed I/Os | Oklobdjiza, Vojin | NM SU |
| 64 | 1836.090 | EE | Digitally-Enhanced Clocking Strategies to Improve Energy-Efficiency of Serial Links | Hanumolu, Pavan | Oregon SU |
| 65 | 1836.091 | S&S | High-Data Rate Low-Cost Dielectric Waveguide Interconnects on Flexible Plastic Substrates | Akinwande, Deji | UT Austin |
| 66 | 1836.092 | S&S | A Model-View-Controller (MVC) Platform for Adaptive Test | Makris, Yiorgos | UT Dallas |
| 67 | 1836.093 | FA | Variability-Aware, Discrete Optimization for Analog Circuits | Kim, Jeha | Seoul National University |
| 68 | 1836.094 | S&S | Accurate FSM Approximation of Analog/RF Systems for Debugging Mixed Signal Designs | Roychowdhury, J. | UC Berkeley |
| 69 | 1836.095 | FA | Test Generation for Mixed-Signal Design Verification and Post-Silicon Debugging | Shi, Richard | U. Washington |
| 70 | 1836.096 | FA | Mixed Signal Design Centering in Deeply Scaled Technologies | Nikolic, B. | UC Berkeley |
| 71 | 1836.097 | FA | Dual-Domain SAR ADCs Incorporating Both Voltage and Time Information | Moon, U.-K. | Oregon State |
| 72 | 1836.098 | HC | Sub mW Wireless Transceiver Frontends for Body Area Networks | Harjani, Ramesh | U. Minnesota |

**Table 2: continued**

| 4 | Task | Thrust | Task Title | PI | Institution |
|---|---|---|---|---|---|
| 73 | 1836.099 | EE | Modeling of Analog and Switching Circuits | Mantooth, Alan | U. Arkansas |
| 74 | 1836.100 | EE | Test Techniques and Fault Modeling for High Voltage Devices and Boards | Kim, Bruce | U. Alabama |
| 75 | 1836.101 | S&S | Sparse 2D MIMO Radar Transceiver Design and Prototyping for 3D Millimeter-Wave Imaging | Mohammad, Saquib | UT Dallas |
| 76 | 1836.102 | S&S | Superresolution Techniques for 3D Millimeter Wave Radars | Torlak, Murat | UT Dallas |
| 77 | 1836.103 | HC | Reconfigurable Brain Computer Interface | Jafari, Roozbeh | UT Dallas |
| 78 | 1836.104 | EE | Fault Tolerant Drive Module for Double Stator Switched Reluctance Motor Drive (DSSRM) | Fahimi, Babak | UT Dallas |
| 79 | 1836.105 | EE | Cross-Regulation-Free Single-Inductor Multiple-Output DC-DC Power Converters with Nano-Second Load Transient Response | Ma, Dongsheng | UT Dallas |
| 80 | 1836.106 | EE | IF Sampling CMOS ADC Front-End with 100-dB Linearity | Chiu, Yun | UT Dallas |
| 81 | 1836.107 | FA | Verification of Multi-State Vulnerable AMS Circuits | Geiger, R., Chen, D. | Iowa State |
| 82 | 1836.108 | EE | Performance-Oriented DVS-Compatible Single-Inductor Multiple-Output Power Converters | Ma, Dongsheng | UT Dallas |
| 83 | 1836.109 | FA | New Paradigms for High-Performance Amplification | Moon, U.-K. | Oregon SU |
| 84 | 1836.110 | EE | Distributed Power Delivery Architecture for 2D and 3D Integrated Circuits | Mukhopadhyay, S. | GA Tech |
| 85 | 1836.111 | FA | Advanced ADC-Based Serial Link Receiver Architectures | Palermo, S. | TAMU |
| 86 | 1836.112 | EE | Shortstop: Fast Power Supply Boosting for Energy-Efficient, High-Performance Processors | Blaauw, D. | U. Michigan |
| 87 | 1836.113 | FA | Synthesized Cell-Based ADPLL Implementation for Accelerated Design | Wentzloff, D. | U. Michigan |
| 88 | 1836.114 | FA | Frequency Shapeable Multichannel ADCs | Eldar | Technion |

## ACCOMPLISHMENTS

TxACE has made significant research progress. Table 3 lists the major research accomplishments for the center during September 1st of 2011 to August 31st of 2012, while Table 4 summarizes the number of publications and inventions resulting from the TxACE research during the period. The TxACE researchers have published 94 conference papers and 24 journal papers. They have also made 4 invention disclosures and filed 1 patent application. One patent was granted. The list of publications is included as Appendix II. Following the tabulation, brief summaries of each project are provided.

**Table 3: Major TxACE Research Accomplishments (September 2011 through August 2012)**

| Category | Accomplishment |
|---|---|
| Circuits (Fund. Analog) | Demonstrated power combining techniques to achieve ~1W output power with an average efficiency >40% for OFDM signals at 2.4GHz and sufficient linearity to obviate digital predistortion in deep-sub-micron CMOS technologies (65-nm). Scaling-friendly switched-capacitor circuits are used in class-G CMOS digital power amplifiers to achieve high power, average efficiency and linearity. (1836.085, PI: D. Allstot, University of Washington) |
| Circuits (Fund. Analog) | Demonstrated analog-to-digital converters that exploit both voltage and time domain information to provide additional resolution without increasing power. The residue shaping, allowing a multi-stage ADC with half-bit redundancy to achieve a 6dB higher SQNR has been analyzed and simulated. Achieved low power (75uW at 8MHz) with overall measured FoM of 10fJ/conv. step. (1836.097, PI: U. Moon, Oregon State University) |
| Circuits (Fund. Analog) | Proposed a non-invasive methodology that keeps the stress interrupts for measurements within a few microseconds, preventing unwanted BTI recovery, while providing a parallel stress-measure capability on a large-scale memory array. An IEDM 2012 paper demonstrated for the first time an SRAM reliability macro capable of monitoring bit cell failures due to NBTI and PBTI. (1836.085, PI: C. Kim, University of Minnesota) |
| Circuits (Health Care) | Demonstrated a capacitive sensing technique in a VCO of a PLL for measurement of organic liquid fraction. The technique is utilized to measure fractional volume of an ethanol and methanol mixture with an accuracy of 1%. (1836.066, PI: K. Entesari, Texas A&M University) |
| Circuits (Safety & Security) | A fully-integrated 260-GHz transceiver has been demonstrated in 65-nm CMOS with an on-chip 4-element leaky-wave antenna array, showing transmission and reception at 10 Gb/s and 4cm range. Also, a 60GHz pulsed-oscillator transmitter has been demonstrated in 65-nm CMOS which consumes 21mW and can generate 10Gb/s data. (1836.082, PI: E. Alon, A. Niknejad, Univ. California, Berkeley) |
| Circuits (Safety & Security) | Low loss and high tuning range variable reactance elements are needed at millimeter-wave frequencies to enable high-performance oscillators, phase shifters, and tunable resonators. A transformer based variable inductor has been demonstrated, where an accumulation-mode MOS varactor is transformed into a higher Q effective variable inductance, achieving a measured Q > 10 and tuning range of 1.2:1 at 77GHz. (1836.036, PI: K. O, UT Dallas) |
| Circuits (Safety & Security) | A Phased Array Imaging Toolbox has been developed in Matlab, based on detailed mathematical derivations for near-field antennas, and it can be used to verify mathematical and simulation models for on-chip phased arrays of mm-wave imaging systems. The system simulator has been used to investigate performance of a 77GHz imaging system. (1836.054, PI: M. Torlak, UT Dallas) |

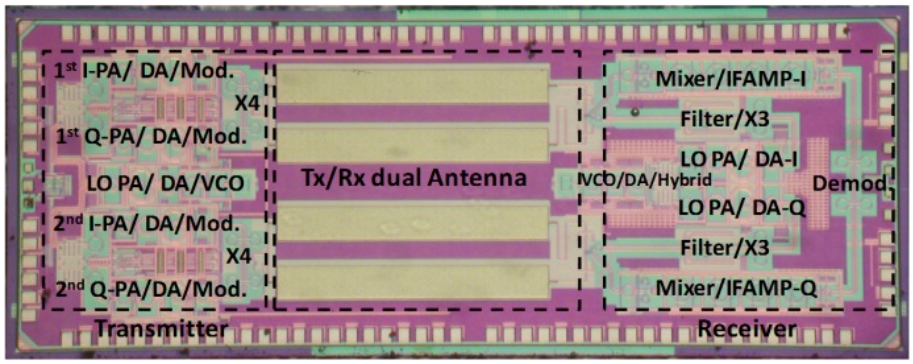
| | |
|---|---|
| Test (Safety & Security) | Developed a model view controller platform with integrated statistical learning theory controllers for adaptive testing that can reduce test time by an order of magnitude (1836.092, Y. Makris, UT Dallas) |
| Circuits (Energy Efficiency) | This project developed a high frequency model of a flyback transformer, using a time domain system identification method. The model can accurately predict the frequency response of transformer from 500Hz – 15MHz. This model can be used to estimate the output voltage in both continuous conduction mode and discontinuous conduction mode operation based on a primary-side sensing scheme for flyback converters. (1836.070, PI: J. Ringwood, National University of Ireland-Maynooth) |
| Circuits (Energy Efficiency) | A fully integrated combined inductive/capacitive converter was designed. This research pioneers the study of a compensated voltage regulation jointly achieved by an inductive switching converter and a SC power converter. The fully on-chip integration of both converters makes its form factor extremely attractive. (1836.081, PI: R. Harjani, University of Minnesota) |
| CAD (Energy Efficiency) | An entropy-based analysis method has been developed to reduce the number of reset circuits required to eliminate the global convergence problem. For a PLL, the number of reset circuits was reduced from 81 to 6. (1836.068, PI: J. Kim, Seoul National University) |

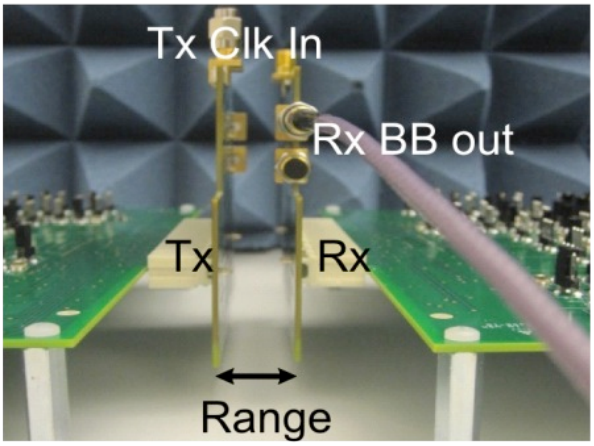
**Table 4: TxACE number of publications (September 2011 through August 2012)**

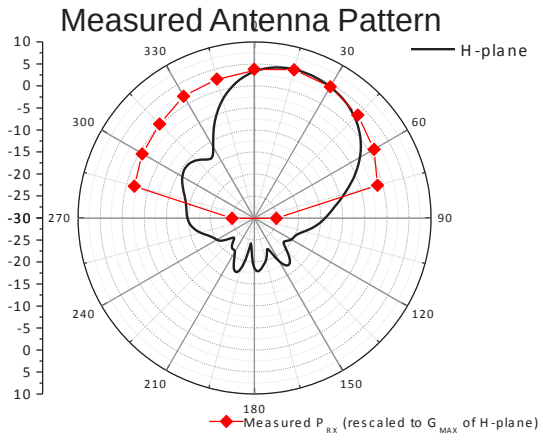
| Conference Papers | Journal Papers | Invention Disclosures | Patents Filed | Patents Granted |
|---|---|---|---|---|
| 91 | 23 | 4 | 1 | 1 |

# Safety and Security Thrust

4-element 260GHz transceiver array with on-chip antennas




## Summary of Accomplishments

| Category | Accomplishment |
|---|---|
| Security and Safety | A fully-integrated 260GHz transceiver has been demonstrated in 65nm CMOS with an on-chip 4-element leaky-wave antenna array, showing transmission and reception at 10 Gb/s and 4cm range. Also, a 60GHz pulsed-oscillator transmitter has been demonstrated in 65nm CMOS which consumes 21mW and can generate 10Gb/s data.<br><br>Publications: (1) J. D. Park et al., "A 260GHz Fully Integrated CMOS Transceiver for Wireless Chip-to-Chip Communication," IEEE Symposium on VLSI Circuits, Jun. 2012.<br>(2) L. Kong and E. Aon, "A 21.5mW 10+gb/s mm-Wave Phased-Array Transmitter in 65nm CMOS," IEEE Symposium on VLSI Circuits, June 2012.<br><br>(1836.082, PI: E. Alon, A. Niknejad, Univ. California, Berkeley) |

| | |
|---|---|
| Security and Safety | Low loss and high tuning range variable reactance elements are needed at millimeter-wave frequencies to enable high-performance oscillators, phase shifters, and tunable resonators. A transformer based variable inductor has been demonstrated, where an accumulation-mode MOS varactor is transformed into a higher Q effective variable inductance, achieving a measured Q > 10 and tuning range of 1.2:1 at 77GHz.<br><br>Publications: (1) Y.-H. Yun, T.-Y. J. Kao, and K. K. O, "Variable inductors in CMOS for millimeter wave applications," submitted for publication .<br><br>(1836.036, PI: K. O, UT Dallas) |
| Security and Safety | A Phased Array Imaging Toolbox has been developed in Matlab, based on detailed mathematical derivations for near-field antennas, and the toolbox can be used to verify mathematical and simulation models for on-chip phased arrays in millimeter-wave imaging systems. The system simulator has been used to investigate performance of a 77GHz imaging system.<br><br>Publications: (1) S. Patole and M. Torlak, "Two-dimensional millimeter-wave array imaging with beam-steered data," IEEE Trans. Antennas and Propagation, in preparation.<br><br>(1836.054, PI: M. Torlak, UT Dallas) |

# TASK 1836.09-11 DIGITAL ASSISTED MILLIMETER-WAVE CMOS CIRCUITS

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KENNETH K. O, THE UNIVERSITY OF TEXAS AT DALLAS

## SIGNIFICANCE AND OBJECTIVES

To improve yield and shorten time to market of millimeter wave CMOS circuits, this task is Investigating the feasibility of incorporating digitally-controlled built-in tuning in millimeter wave circuits that mitigates the impact of process variations, modeling uncertainty of passive and active components.

## TECHNICAL APPROACH

Detectors placed at the input and output of front-end amplifiers and mixer outputs of an RF transceiver can be used for measurements needed for tuning/calibrating the receiver and transmitter. The key challenges for realizing a digital assisted system operating at millimeter wave frequencies are (1) inexpensively injecting test signals, (2) incorporating tuning elements which do not add significant parasitics and degrade circuit performance, and (3) realizing high impedance broadband detectors with sufficient dynamic range. This effort will understand these challenges, and the limitations in the context of a 77-GHz reconfigurable low noise and power amplifiers fabricated in 45-nm CMOS.

## SUMMARY OF RESULTS

A tunable millimeter wave low noise amplifier in Figure 1 has been fabricated. The four stage amplifier includes four tunable inductors that can tune the inter-stage matching. In simulations, the gain center frequency can be tuned from 76 to 82 GHz. In measurements, the amplifier is tuned around 60 GHz. Because of the limited inductor tuning range, the center frequency can be tuned only between 58 and 61 GHz. The peak gain is ~10 dB.

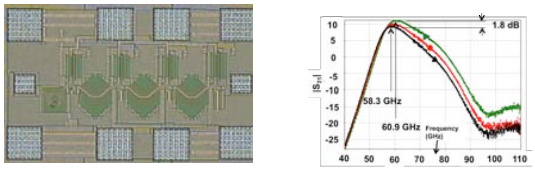


**Figure 1: Tunable amplifier layout and measurements**

Transformer based variable inductors usable up to ~77GHz are demonstrated and shown in Fig. 2. Measured inductance of two variable inductors can be tuned from 56.5 to 67pH and from 55.7 to 61.9pH at 77GHz. The bandwidth Q is greater than 10 at 77GHz. This is higher than that of typical Q of ~4 for MOS Varactors. This indicates that variable inductors with useful tuning range and sufficiently high Q can be realized in CMOS for use in millimeter wave circuits.

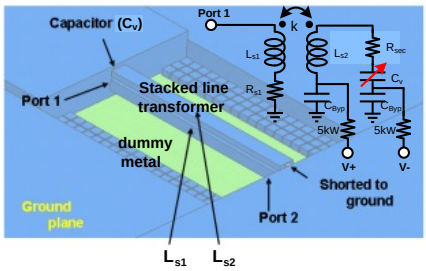


**Figure 2: Variable inductor structure and equivalent circuit model. The secondary resistance, $R_{sec}$ is the series resistance of secondary inductor $R_{s2}$ + the varactor resistance, $R_v$.**

In addition, a root mean square Schottky diode detector for estimating millimeter-wave (80 GHz to 110 GHz) signal voltage using DC or low frequency measurements is demonstrated. The detector is realized in a 45-nm CMOS process without any process modifications. The detector gain at 30-$mV_{rms}$ input voltage is 11 $V^{-1}$. The insertion loss is less than 0.2 dB and the flatness of the detector gain over 80 to 110 GHz is ±15 %. The input dynamic range is greater than 29 dB and the size of detector including the filter capacitor is 340 $\mu m^2$.

**Keywords:** tunable, mm-wave, variable inductor, Schottky diode detector

## INDUSTRY INTERACTIONS

Texas Instruments, Freescale, IBM

## MAJOR PAPERS/PATENTS

[1] N. Zhang et al., "W-Band Pulsed Radar Receiver in Low Cost CMOS," CICC, Sep., 2010, San Jose, Calif.

[2] C. Mao et al., "Diodes in CMOS for MM and Sub-MM Wave Circuits," **(Invited)** Intl. Sym. on VLSI Tech., Systs and Apps, April 2010, Hsinchu, Taiwan.

[3] C. Mao et al., "65/130 GHz diode freq. doubler in 0.13-µm CMO," IEEE JSSC, vol. 44, no. 5, pp. 1531-1538, May 2009.

[4] Y.-H. Yun et al., "Variable Inductors in CMOS for MM-Wave Applications," IEEE ED Letters (accepted).

[5] C. Li et al., "Broadband Root Mean Square Detector in CMOS for On-chip Measurements of MM-Wave Voltages," IEEE ED Letters (accepted).

# TASK 1836.030 FAST PVT-TOLERANT PHYSICAL DESIGN OF RF IC COMPONENTS

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## SIGNIFICANCE AND OBJECTIVES

PVT variability makes it hard to achieve "safe" designs in nanoscale CMOS technologies and also reduces yield. However, no major attempts have been made to address these for RFICs due to increased complexity and bottlenecks of analog simulation. We investigate fast physical design and optimization techniques for RF ICs such that the resulting designs are PVT tolerant.

## TECHNICAL APPROACH

To have a process-variation robust design accounting for parasitics, power, and temperature, we investigate a new "PVT tolerant RF IC design flow". In a standard RF IC design flow, multiple iterations between the front-end circuit design and back-end layout are required to achieve parasitic closure. Such a manual approach requires X number of iterations. The proposed design flow reduces the number of manual iterations to 1, by performing the X number of iterations on a parasitic parameterized netlist or layout-accurate metamodels instead of the layout. Hence, **this novel flow reduces the X number of manual iterations required for parasitic closure, to 1 manual iteration** with ultra-fast automatic iterations over the metamodels. Layout-accurate metamodeling and optimization algorithms are investigated for ultra-fast physical-design optimization.

## SUMMARY OF RESULTS

The effects of PVT variation on the performance of PLL components are analyzed. The physical design of the PLL is performed using a 180*nm* CMOS PDK. The simulations were performed on the full-blown (RLCK) parasitic-extracted netlist of the PLL. The statistical distribution of the center frequency proved its Gaussian nature for correlated variations. Statistical sampling techniques are compared for speed and accuracy, and polynomial metamodels are obtained for a ring oscillator and LC-VCO. Experiments show that LHS sampling is best for both PLL component circuits, followed by MLHS, MC and DOE. An ultra-fast design-flow that combines polynomial metamodels and bee-colony optimization algorithms is investigated which achieved approximately 90% power and 52% jitter reduction. An ultra-fast design flow that uses memetic-based optimization algorithms over neural-network metamodels for design-space exploration is explored which further increases the accuracy by 56% over the polynomial metamodels.

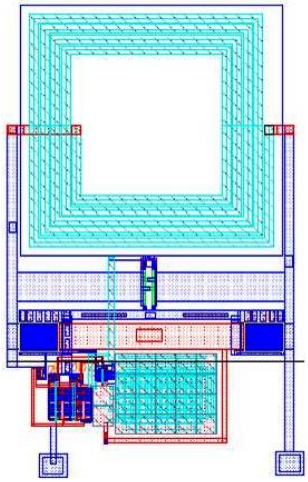

**Figure 1: P4VT Optimal Dual-Threshold VCO Layout.**

**Table 1: Experimental Results for 180nm PLL**

| Metric | Before Optimization | After Optimization | Improvement |
|---|---|---|---|
| Power | 9.29 mW | 0.87 mW | 90.6% |
| Jitter Vertical | 168.35$\mu$V | 3.28 nV | ~100% |
| Jitter Horizontal | 189 ps | 180 ps | 4.8% |

**Keywords:** process variation, parasitic effects, metamodeling, optimization, nano-CMOS, RF Circuits

## INDUSTRY INTERACTIONS

Intel

## MAJOR PAPERS/PATENTS

[1] O. Garitselov, et al., "A Comparative Study of Metamodels for Fast and Accurate Simulation of Nano-CMOS Circuits," IEEE Trans. Semiconductor Manufacturing, vol. 25, no. 1, pp. 26-36. 2012.

[2] O. Garitselov, et al., "Metamodel-Assisted Ultra-Fast Memetic Optimization of a PLL for WiMax and MMDS Applications," in *Proc. 13th* IEEE International Sympo. Quality Electronic Design, pp. 580-585, 2012.

[3] O. Garitselov, et al., "Fast Optimization of Nano-CMOS Mixed-Signal Circuits Through Accurate Metamodeling," in Proc. 12th Intl Sympo. Quality Electronic Design, pp. 405--410, 2011.

[4] S. P. Mohanty, D. Ghai, and E. Kougianos, "A P4VT (Power-Performance-Process-Parasitic-Voltage-Temperature) Aware Dual-$V_{Th}$ Nano-CMOS VCO," in Proc. 23rd Intl. Conf. VLSI Design, pp. 99--104, 2010.

# TASK 1836.032 MILLIMETER-WAVE PHASE-LOCKED LOOP DESIGN WITH ENHANCED TOLERANCE TO PROCESS AND TEMPERATURE VARIATION

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## SIGNIFICANCE AND OBJECTIVES

A key challenge to the manufacturability and robustness of designs at mm-wave frequencies arises from process and temperature (P&T) induced variations. This research focuses on the design of a phase-locked loop (PLL) based mm-wave frequency synthesizer for 77 GHz RADAR applications that is robust to such variations.

## TECHNICAL APPROACH

The impact of process and temperature (P&T) variations on PLL circuits has been investigated and several critical sensitivities have been identified through simulation. Circuit and architectural solutions to minimize changes in performance metrics, and prevent catastrophic failures due to such variations have been designed in a 65nm process. The approach is based on the use of broadband circuit techniques. A dual-mode VCO that reuses an LC tank to generate two distinct frequencies, with varactor-based fine frequency control has been designed. A broadband injection locked frequency divider is also implemented. Gain and amplitude response of critical circuits is controlled through bias setting, which has also been found to be effective for controlling temperature induced performance variation.

## SUMMARY OF RESULTS

An integer N PLL has been designed and implemented in a 65nm process. The circuit blocks that have the greatest impact on PLL performance due to P&T variations are those operating at the highest frequencies, namely the VCO and the first divider in the PLL.

In order to span a specific range of frequencies, the VCO needs to be designed with sufficient margin to accommodate the above variations. Typically, this introduces a design challenge, since oscillators exhibit an inherent trade-off between phase noise and tunability. To alleviate this trade-off, a dual-mode VCO has been proposed [1, 2] and designed. The design relies on active core reconfiguration around an LC resonator, as opposed to switching passive elements within the resonator. This allows for two modes of operation, with minimal change in the inductance-to-resistance ratio of the resonator. This in turn reduces phase noise variation for a given tuning range.

A circuit based on this approach has been designed with nearly 25% tuning range at 64GHz in a 65nm process. Since two distinct frequencies are achieved from the topology, without a change to layout, the sensitivity to layout variations is expected to be smaller in this approach, as compared to using two independent VCOs to span the same frequency range. Resonators based on transmission lines and LC tanks have both been investigated.

The impact of temperature variation has also been studied and described previously. This variation mechanism is seen to degrade tunability by approximately 2% due to change in varactor capacitance and $C_{gs}$ of the cross-coupled devices of the VCO. We have investigated the use of PTAT back gate compensation in an inversion mode varactor to compensate frequency shift arising from this mechanism. Temperature variation is seen to have a significant impact on phase noise. A key source of degradation at high temperatures arises from the resistance of the inductor metal, which has a positive temperature coefficient. A decrease in the quality factor with temperature degrades the swing, and in turn the phase noise. This degradation will be compensated through bias current control.

In mm-wave applications, injection locked frequency dividers (ILFDs) are often employed in the first divider stage. These designs can operate at much higher frequencies, since they use resonant tanks unlike static CML dividers. However these suffer from limited locking range. A low-power wide tuning range ILFD has been implemented as part of the PLL in the 65nm process. By using a larger Vgs on the input device of the divider compared to the devices connected to the LC tank of the ILFD, a locking range in excess of 20% is achieved.

**Keywords:** Frequency synthesis, phase-locked loop, variability, voltage-controlled oscillator, mm-wave design

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] R. Gharpurey *et al.*, A Single-Tank Dual-Band Reconfigurable Oscillator, VLSI Symp. pp. 176-177, 2006.

[2] S. Agarwal *et al.*, A Dual-mode Wide-band CMOS Oscillator, IEEE DCAS Workshop, 64-66, 2009.

# TASK 1836.033 MIMO RADAR FOR PIXEL REDUCTION IN MM-WAVE IMAGING

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## SIGNIFICANCE AND OBJECTIVES

The mm-wave radar imaging system is well-suited for many safety and security applications. It consists of antennas, analog-to-digital converters (ADC), digital signal processor (DSP), analog circuitry and so forth. We propose system design schemes that use less elements and less complex hardware to reduce cost of production.

## TECHNICAL APPROACH

We employ space-time block codes (STBC) to eliminate the cross-correlation effects among parallelly transmitted probing signals of a multiple-input-multiple-output (MIMO) radar imaging system to exploit the transmit diversity and reduce the hardware requirement. It is also desirable to utilize fewer bit ADCs from cost and power perspectives. However, fewer bit ADCs generate higher quantization error and degrade the performance. We analyze the effects of ADC quantization noise on radar imaging in order to design cost-effective systems. Due to quantization process, estimated target reflectivity coefficients become random variables, and their probability density function is derived through a statistical approach.

## SUMMARY OF RESULTS

In this section, we first compare the performance of an MIMO radar imaging system with the traditional one, and then demonstrate the further improvements achieved through the deployment of the proposed TR-STBC technique through numerical analysis. We consider a concealed weapon (revolver) as our test target as shown in Figure 1(a).

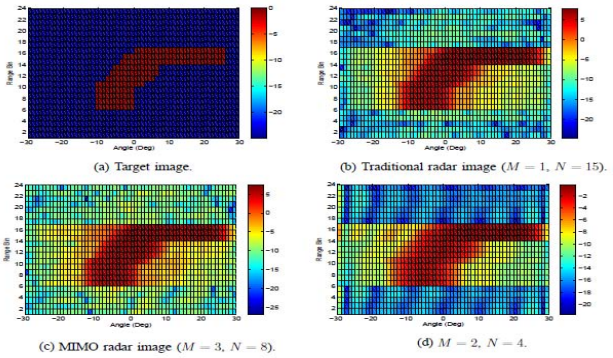


**Figure 1: (a) Target image, (b) traditional radar image, (c) MIMO radar image & (d) MIMO radar image with TR-STBC**

The images obtained using traditional, MIMO and MIMO with STBC, are shown in Figures 1(b), (c) and (d), respectively. The numbers of antennas used are 16, 11 and 6, respectively, which demonstrates a 60% reduction in transceiver antennas.

In the target image shown in Figure 2, 'U' has a reflectivity coefficient of 1 and 'T' has 0.5. The estimated targets are shown for two different values of the receiver tuning parameter λ. The respective distributions of the reflectivity coefficients for the two letters are shown on the right side. Note that there are three averaged PDFs in each subfigure; the solid curve, dashed curve and dash-dot curve represent 'U' area, 'T' area, and non-target area, respectively. The PDF of the non-target area is always closest to the vertical axis. These PDF illustrations can help choose the best suite of parameter values for the system that yields images of desired resolutions.

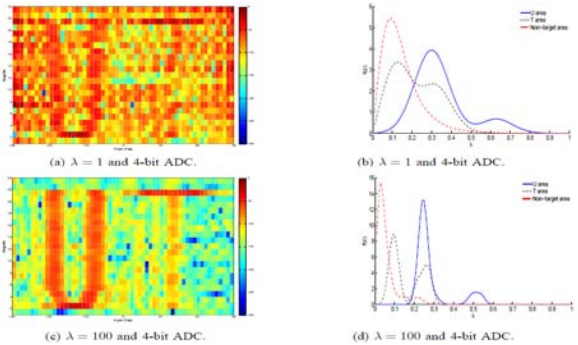


**Figure 2: Letter targets and corresponding distributions of reflectivity coefficients with different tuning parameters.**

In this project, we have also designed a MIMO radar configuration for sensor network localization in wide-area surveillance applications.

**Keywords:** MIMO Radar, millimeter wave, space-time-block-code, reflectivity coefficient, transmit diversity

## INDUSTRY INTERACTIONS

Texas Instruments, Intel

## MAJOR PAPERS/PATENTS

[1] T. Ali et al., "MIMO Radar Imaging for Target Detection and Localization in Sensor Networks," IEEE Systems Journal: Special Issue on Sensor Networks for Advanced Localization Systems (submitted), May 2011.

[2] J. Sung et al., "Effects of ADC Quantization Noise on MIMO Radar Imaging," IEEE Transactions on Signal Processing (submitted), Dec. 2011.

[3] A. Sadeque et al., "Space-Time Block Codes for MIMO Radar Imaging," IEEE Transactions on Aerospace and Electronic Systems (submitted), April 2012.

# TASK 1836.034 77-81 GHZ CMOS TRANSCEIVER WITH BUILT-IN SELF-TEST AND HEALING

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BHASKAR.BANERJEE@UTDALLAS.EDU

## SIGNIFICANCE AND OBJECTIVES

This work focuses on developing Built-in Self-Test (BIST) techniques for millimeter-wave (mmW) CMOS integrated transceivers for 77 GHz automotive radar applications. Testing is one of the key factors raising the cost of manufacturing mmW ICs. This research focuses on understanding the architectural trade-offs and testing algorithms, and developing circuits that can enable loopback based BIST techniques for mmW transceivers in standard CMOS technologies.

## TECHNICAL APPROACH

In order to perform BIST on a mmW CMOS transceiver, we need to enable a 'loopback' path between the transmitter and the receiver (if they are integrated on the same IC). Fig. 1 below represents the concept.

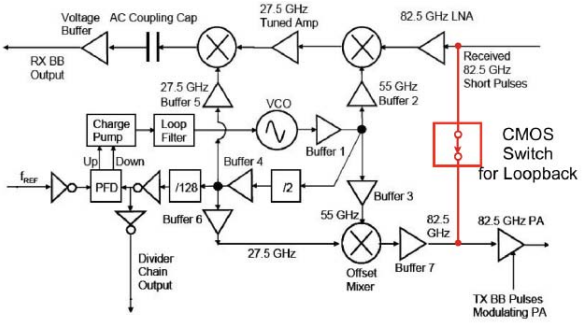


**Figure 1: Schematic of the 77 GHz transceiver with 'loopback' bath between the receiver and the transmitter to enable BIST.**

The key challenges to this approach are: (a) the isolation in the switch (between ON and OFF states) needs to be very high to be able to discern between actual loopback signal and the leakage signal through the silicon substrate, (b) The switch should be transparent to the transceiver, offering high impedance when open and low impedance when closed; and (c) developing an algorithm to be able to systematically test the whole chain for correct functionality.

## SUMMARY OF RESULTS

We have designed and fabricated a high isolation single-pole-single-throw (SPST) CMOS switch in a 45 nm technology. The schematic concept and the die photograph is shown in Fig. 2.

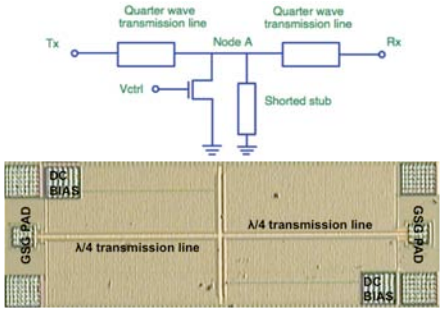


**Figure 2: Schematic of the SPST switch and its die photograph.**

The measured results show that the switch has a loss of about 10 dB at 77 GHz while having an isolation of better than 30 dB when in the OFF state. The measured results are shown in Fig. 3 below.

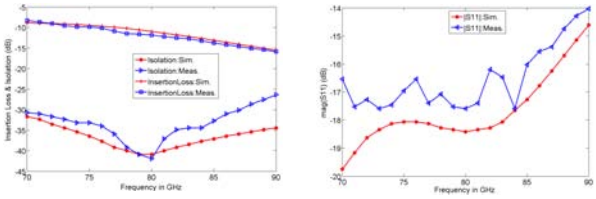

**Figure 3: Measured results for the insertion loss, isolation and matching for the switch. The switch provides an isolation > 40 dB between the ON and OFF states.**

In the last six months, the project will focus on extending the designs to smaller and better switches (high off-impedance, and low on-impedance) and also to develop a systematic testing plan to complete the BIST scheme.

**Keywords:** BIST, millimeter-wave, CMOS

## INDUSTRY INTERACTIONS

Texas Instruments, Freescale

## MAJOR PAPERS/PATENTS

[1] T. Mahzabeen, et. al., "A High Isolation 70-90 GHz CMOS Switch for Built-In-Self-Test ", under review, IEEE SiRF 2013.

[2] T. Mahzabeen, et. al., "77-81 GHz CMOS Transceiver with Built-in Self Test and Healing," SRC TECHCON 2012.

# TASK 1836.035 DEVELOPMENT OF CMOS SUB-THZ RECEIVERS FOR SPECTROMETERS

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## SIGNIFICANCE AND OBJECTIVES

This work focuses on developing CMOS integrated receivers for spectrometer covering 180GHz-300GHz frequency band. Wireless spectroscopy can be used to identify different chemicals in a gas sample, which respond uniquely to electromagnetic waves, undergoing rotational and vibrational transitions at different frequencies. Wireless detection of some chemicals can find widespread use in safety and security as well as health care applications.

## TECHNICAL APPROACH

As shown below in Fig.1, the 'sample-under-test' is excited with signals at a series of electromagnetic frequencies, and the transmitted waveform is down-converted and analyzed to determine the chemical contents in a sample. To cover the entire spectrometer band of 180-300 GHz we proposed that the receiver will be split-up into six sub-bands, covering 20GHz bands each so in all we have six receivers. In order to optimize the overall system performance, multiple architectures are analyzed and explored. Preliminary system level results indicate that the system Noise Figure achieved is < 18dB for an input RF power of -50dBm for direct down conversion receiver.

The key building block for the receiver is the front-end mixer. With current CMOS technology it is not possible to design active mixers using transistors at these frequencies. However, the high cut-off frequencies of Schottky Barrier Diodes (SBDs) in standard CMOS technology allow us to design anti-parallel-diode-pair (APDP) based subharmonic passive mixers covering the 180-300 GHz bands. An anti-parallel diode pair (APDP) based mixer has been designed in a UMC 130nm CMOS process. The measured results show a conversion loss of about -24 dB for a 200GHz RF signal down-converted to an IF of 15 MHz.

## SUMMARY OF RESULTS

A 180-200 GHz APDP diode pair has been designed and fabricated in a UMC 130 nm CMOS technology (Fig. 1). The mixer downconverts a 200 GHz RF signal to an IF of 15 MHz using the second harmonic of the LO signal (100 GHz).

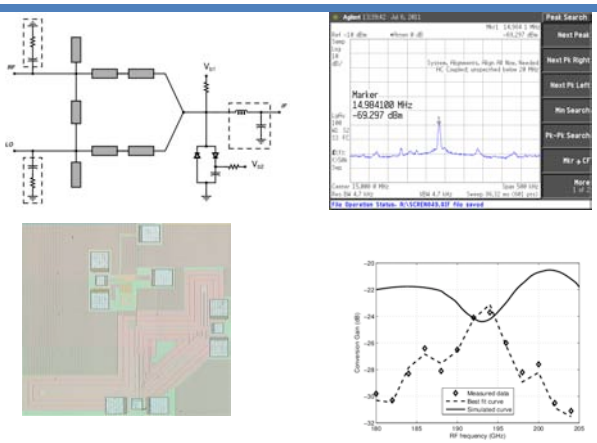

**Figure 1: 200 GHz APDP Mixer schematic, die photo, and measurement results.**

Fig. 2 shows the schematic and the simulated conversion gain of an improved APDP mixer. This mixer provides a voltage gain of about 1 dB at 200 GHz RF.

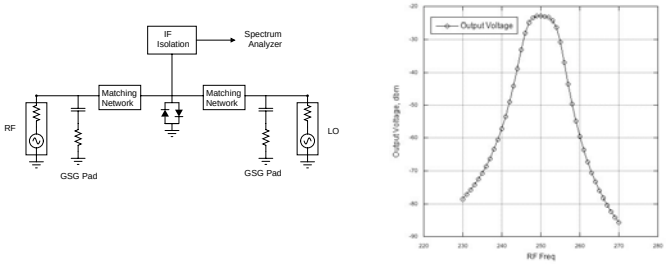


**Figure 2. Schematic and conversion gain for an improved APDP mixer at 200 GHz.**

In the next six months, the project will focus on measuring the improved mixer and finalizing the receiver architecture.

**Keywords:** THz CMOS, spectroscopy, APDP Mixer.

## INDUSTRY INTERACTIONS

Texas Instruments, Intel, IBM Research.

## MAJOR PAPERS/PATENTS

[1] M. F. Hanif, et. al., "Development of CMOS Sub-THz Receivers for Spectrometer," SRC TECHCON 2011, 2012.

[2] M. F. Hanif, et. al., "200 GHz CMOS APDP Mixer," IEEE MWCL (under review).

# TASK 1836.036 SIGNAL GENERATION FOR 200-300 GHZ SPECTROMETERS

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## SIGNIFICANCE AND OBJECTIVES

As part of the effort to help open up high millimeter and sub-millimeter wave frequency range for moderate volume and cost applications, this task is studying the feasibility of realizing a transmitter in CMOS for a rotational spectrometer that detects harmful molecules and can be used to analyzes breath.

## TECHNICAL APPROACH

This task will study the feasibility of realizing a transmitter for a rotational spectrometer in CMOS. The transmitted power should be ~10-100 µW. The main challenge is increasing the output frequency range, power, and frequency for phase locked signals. To realize a fast scan rate with a 10-kHz step, use of a fractional-N synthesizer is being investigated. The oscillator will operate at lower frequency than the output. The output signal is generated using a combination of an N-push technique and non-linear effects. This task will help generate the LO signal for the receiver.

## SUMMARY OF RESULTS

To examine the feasibility of phase locking 300-GHz signal, a 195-GHz frequency divide four circuit driven by a 195-GHz oscillator with a 390-GHz push-push (2-push) output is fabricated in TI 45-nm CMOS.

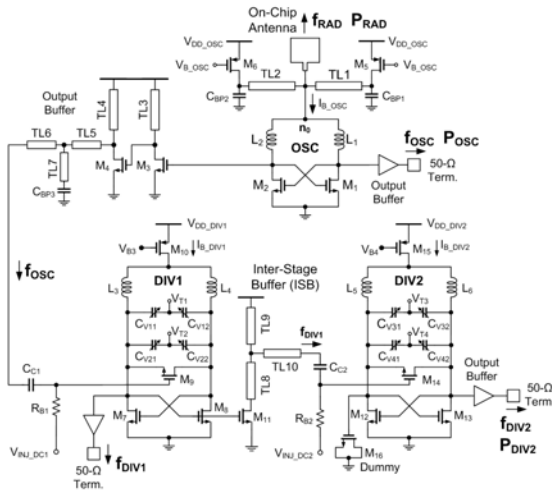


**Figure 1: Block diagram (a) and circuit schematic (b) of component chain for 390-GHz phase locked loop.**

Figure 1 shows the schematic. The divider successfully locked to 192.2-195.5 GHz indicating that it is possible to phase lock 390 GHz signal in CMOS. The measured radiated output power was also increased to 2.2 µW at 385GHz. The phase noise at 390 GHz is estimated to be lower than -68 dBc/Hz at 1MHz offset. Figure 2 shows the die photograph of the component chain for phase locking a 390-GHz signal.

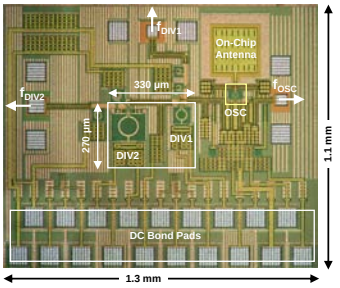


**Figure 2: Die photograph of the component chain for phase locking a 390-GHz signal.**

The output power and locking range of 390-GHz oscillators are too low for the spectrometer. To sufficiently increase these, the oscillator should operate at lower frequency. The work to generate 556-GHz signal using a 4-push oscillator and other new simulation results indicate that operation at four times below the output frequency in combination with frequency doubling should allow generation of sufficient output power and tuning range as well as phase locking for a single transmitter to cover the 180-300 GHz output range. A test structure for a wide tuning range quadrature voltage controlled oscillator has been submitted for fabrication using a 65-nm CMOS process. Additionally, test structures for a wide tuning range VCO and a fractional-N synthesizer that achieve a fast scan rate (~ 1GHz/sec) with a step size of 10 KHz have been fabricated and being prepared for measurements.

**Keywords:** rotational spectrometer, transmitter, CMOS, millimeter-wave.

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] D. Shim et al., "Components for Generation and Phase Locking 390-GHz Signal in 45-nm CMOS," IEEE VLSI Symposium on Circuits (accepted), 2012.

[2] K. K. O, "Silicon IC's for Sub-millimeter Wave Frequencies and Beyond," **Jack Kilby Lecture**, GOMAC Technology Conference, 2012.

[3] D. Shim et al., "553-GHz Signal Generation in CMOS Using a Quad.-Push Osc.," Symp. on VLSI Circuits, 2011.

[4] E.-Y. Seok et al., "Paths to THz CMOS IC's," IEEE JSSC, vol. 45, no. 8, pp. 1554 -1564, Aug. 2010.

# TASK 1836.037 DEVELOPMENT OF ANTENNA AND CHIP INTERFACE SYSTEMS FOR MILLIMETER WAVE AND SUB-MILLIMETER WAVE APPLICATIONS

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## SIGNIFICANCE AND OBJECTIVES

Feasibility study to develop techniques for designing and integrating high performance passive and RF matching components in the millimeter and sub-millimeter wave band. Techniques to improve radiation characteristics for antennas integrated into a CMOS processing strategy. This work is significant to developing cost-effective packaging for millimeter wave CMOS systems.

## TECHNICAL APPROACH

The technical approach is to improve performance of planar antennas by using novel broadband geometries as compared to microstrip patches. The antennas will be integrated with CMOS ICs using a post-CMOS fabrication process utilizing photo-definable dielectric layers and gold metallization. Multiple transmission lines will be studied in simulation (HFSS) and measurement for optimizing CMOS integration. These results will lead to affordable mm-wave CMOS electronics for automotive radar and spectrometers for harmful molecule detection.

## SUMMARY OF RESULTS

Fig. 1 shows the top view of three transmission lines (CPW, microstrip, GCPW) fabricated using the post-CMOS process. 8 - 56 µm of benzocyclobutene (BCB) polymer ($\varepsilon_r$ = 2.65) has been deposited onto 10 Ω-cm silicon wafers and 1 µm of Au is electroplated on the dielectric. The lines are measured using Agilent VNAs and Oleson extension modules working from 10 MHz to 110 GHz, 140 to 220 GHz and 240 to 325 GHz. LRRM calibration is used for the banded measurements. Table 1 shows measured loss up to 300 GHz. Fig. 2 shows attenuation across the 3 bands for BCB of 8 µm.

**Table 1: Attenuation and geometry of transmission lines.**

| TLs $\alpha$ (dB/mm) | Width (µm) | Gap (µm) | 60 GHz | 100 GHz | 220 GHz | 300 GHz |
|---|---|---|---|---|---|---|
| Microstrip | 16.5 | | 0.7 | 0.9 | 1.31 | 1.4 |
| CBCPW | 20 | 8 | 0.6 | 0.9 | 1.7 | 2.0 |
| CPW | 60 | 8 | 1.0 | 1.4 | 3.1 | 5.0 |
| CPW(56µmBCB) | 60 | 8 | 0.33 | - | 2.1 | 3.1 |
| GCPW | 18 | 10 | 0.6 | 0.8 | 1.3 | 1.6 |

This is the first time where lines fabricated on BCB/Si-CMOS have been characterized up to 300 GHz.

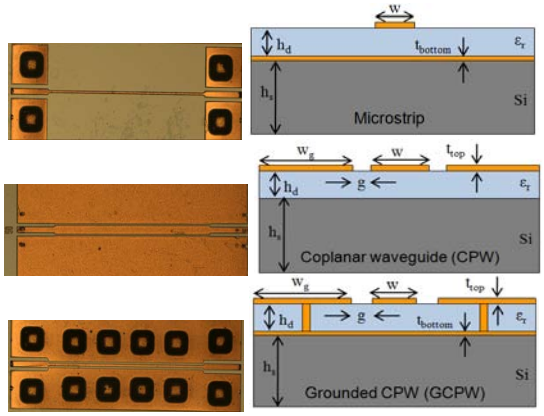


**Figure 1: Post-CMOS transmission lines.**

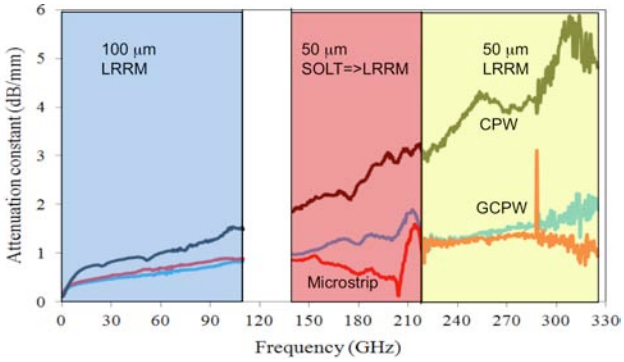


**Figure 2: Measured attenuation up to 325 GHz.**

**Keywords:** aperture antennas, broadband, benzocyclobutene, post-CMOS integration

## INDUSTRY INTERACTIONS

Intel, Texas Instruments

## MAJOR PAPERS/PATENTS

[1] R. Islam et al., "Performance of Coplanar Interconnects for Millimeter-Wave Applications," submitted to IEEE SiRF, 2012.

[2] R. Pierce, et al., "Broadband Planar Modified Aperture Bowtie Antenna," submitted to IEEE AWPL, July 2012.

[3] R. Islam, et al., "Millimeter-wave Loss of Coplanar Waveguide with BCB," submitted to IET, Aug. 2012.

# TASK 1836.046 RECONFIGURABLE ANTENNA INTERFACES FOR SENSOR NETWORKS

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## SIGNIFICANCE AND OBJECTIVES

Transmitters for ultra-low-power sensor networks are continuously evolving to transmit low output power in a highly efficient manner. To this end, various architectures have been introduced that trade off distinct advantages and disadvantages. A comparison of several recent transmitter architectures is presented in terms of power efficiency.

## TECHNICAL APPROACH

Transmitters for ultra-low-power sensor networks are evolving to transmit low output power efficiently.

The power budget of a transmitter is critically dependent on the design of the Power Amplifier (PA). Different applications require widely varying values for the Effective Isotropic Radiated Power from as low as -20 dBm for Body Area Networks to as high as 30 dBm for cellular communications. Substantial energy is saved with proper design. A class-C PA for operation as an antenna interface in body sensor network applications for both the MICS and Zigbee Standards has been developed.

## SUMMARY OF RESULTS

In a direct modulation transmitter (Fig. 1), a PA stage provides a buffer interface between the oscillator and the antenna. In a typical implementation, the oscillator is a digitally-controlled oscillator (DCO) operating with an NMOS (or CMOS) cross-coupled transistor pair(s).

A schematic of the class-C PA with mode control and the die photo are shown in Fig. 2. Reconfigurability is needed because of power, frequency and modulation differences between the MICS and ZigBee standards. MICS uses FSK modulation with an EIRP of 25uW in the 400-MHz band. ZigBee uses BPSK, PSSS or O-QPSK, and EIRP up to 1-mW, at either 800 MHz or 2.4 GHz. The PA will operate in a non-linear mode (e.g., class-D, class-E) for the MICS standard.

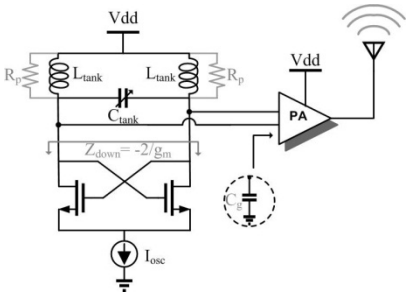


**Figure 1: A direct modulation transmitter with a digitally-controlled oscillator driving the PA.**

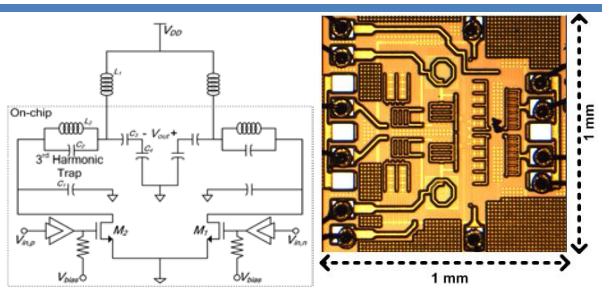


**Figure 2: Class-C PA with mode control; die photo in 0.13um CMOS.**

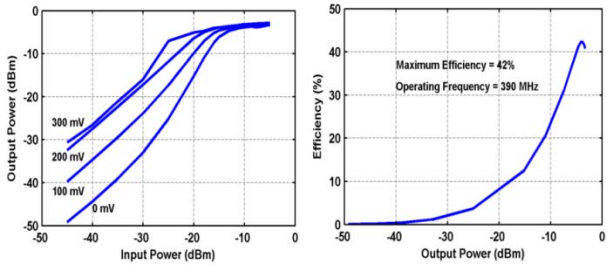


**Figure 3: Measured power characteristic vs. bias level and power output efficiency.**

The PA is fabricated in a 0.13 µm RF CMOS process for operation in the 400 MHz MedRadio band. The PA is driven by a pre-amplifier gain tunable in ~5dB steps.

This design realizes a truly reconfigurable power amplifier with digitally tuned output power. It achieves a measured peak output power and drain efficiency of -4 dBm and 43%, respectively, as shown in Fig. 3.

**Keywords:** Power amplifiers, antenna interface, class-C PA, body sensor networks, MedRadio

## INDUSTRY INTERACTIONS

Texas Instruments, Intel

## MAJOR PAPERS/PATENTS

[1] K. Natarajan, et al., "A Class-C Power Amplifier/Antenna Interface for Wireless Sensor Applications," IEEE Radio Frequency IC Symp., pp. 549-552, June 2011.

[2] K. Natarajan, et al., "Towards greener wireless transmission: Efficient power amplifier design," IEEE Intl. Green Computing Conf. (invited), pp. 1-4, July 2011.

[3] K. Natarajan, et al., "Transmitters for body sensor networks: A comparative study," IEEE Biomedical Circuits and Systems Conf., pp. 185-188, Nov. 2011.

# TASK 1836.047 INTEGRATION OF MILLIMETER WAVE ANTENNAS USING SYSTEM IN PACKAGE TECHNIQUES

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## SIGNIFICANCE AND OBJECTIVES

Feasibility study to develop new techniques for the integration of broadband, high performance antennas with state-of-the-art millimeter wave CMOS circuits. Support the development of low cost automotive radar and spectrometer applications. This work is significant to achieving packaged performance metrics while being affordable.

## TECHNICAL APPROACH

The technical approach is to optimize performance of foundry CMOS silicon circuits with broadband antennas integrated onto a low-cost package substrate. Flip-chip assembly and high performance transmission line feeds will be used to attach the IC to the substrate. EM simulation predicts loss tangent influence and fabricated lines are measured to confirm the results.

## SUMMARY OF RESULTS

50 Ω coplanar waveguide (CPW), grounded CPW and microstrip transmission lines have been simulated and fabricated on a multilayer FR4 core substrate fabricated by Ibiden. Fig. 1 shows the top view of the lines fabricated along with the 7cm x 7cm test coupon. From the attenuation in Fig. 2, we have determined that loss in the CPW lines is minimized by the way fields penetrate through the anisotropic FR4 material. Most of the fields are confined in the air and thick metal, whereas microstrip and GCPW have fields penetrating through the lossy FR4. These results are comparable to more commonly used substrates including LTCC and liquid crystal polymer (LCP) as shown in Table 2. This is the first time where lines have been fabricated and measured up to millimeter-wave frequencies showing that FR4 is a good candidate for substrates.

**Table 1: Attenuation of coplanar lines using SIP substrates.**

| Substrate | LTCC (CBCPW) | LCP (CPW) | FR4(CPW) |
|---|---|---|---|
| 60 GHz | 0.145 | 0.11 | 0.17 |

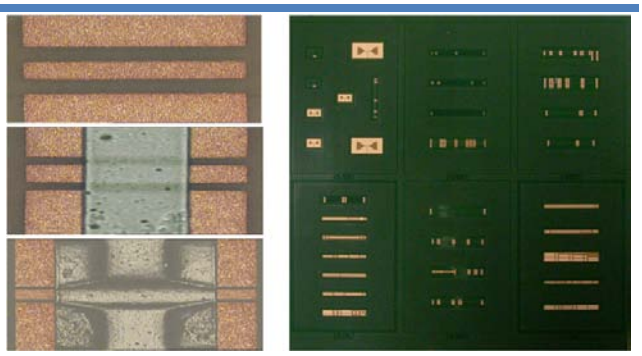

**Figure 1: Photograph of TLs fabricated by Ibiden.**

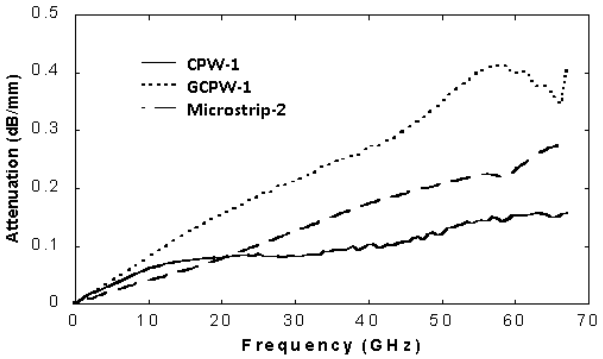


**Figure 2: Measured attenuation of TLs.**

**Keywords:** antenna in package, FR4, millimeter wave CMOS.

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] S. Aroor, et al., "Loss Performance of Planar Interconnects on FR-4 up to 67 GHz," submitted to IEEE Trans. On CPMT, July 2012.

[2] S. R. Aroor, et al., "Millimeter-wave Coplanar Interconnects and Radiators on FR-4 Laminates," submitted to IEEE EPEPS Conf., July 2012.

[3] S. Aroor et. al., "Millimeter-wave Frequency Performance of Conductor-Backed Coplanar Waveguide on FR408 Packaging Material," submitted to IMAPS – JMEP, March 2012.

# TASK 1836.048 MILLIMETER AND SUBMILLIMETER GAS SENSORS: SYSTEM ARCHITECTURES FOR CMOS DEVICES

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## SIGNIFICANCE AND OBJECTIVES

The objective of this project is to develop approaches to compact and inexpensive gas sensors based on millimeter and submillimeter (mm/submm) spectroscopy and implemented in CMOS technology. The dramatic cost, size, and power savings of CMOS will make this attractive sensor competitive in the mass market.

## TECHNICAL APPROACH

We have demonstrated that powerful and unique sensors in the mm/submm spectral region are now practical. This task (coordinated with other tasks that will provide the necessary CMOS antennas, receivers, and transmitters) seeks to develop and demonstrate architectures appropriate for the mass market. This will be accomplished by an iterative interaction between our sensor design background, the development of an intermediate approach based on mass-market technology, and the CMOS design teams. New applications will be developed and demonstrated.

## SUMMARY OF RESULTS

This project is designed to interface with and provide system guidance to three CMOS development projects at UT Dallas. These projects are to develop a probe source for the gas sensor, a sensitive heterodyne receiver, and antennas to transmit the microwave power from the source, through the gas interaction region, and onto the detector.

Last year, with our CMOS collaborators, we arrived at a specification targets for each of the three subsystems. Our end-to-end system analysis of the dynamic range and sensitivity of this design is in general agreement with those of the detailed CMOS designs of our collaborators.

In parallel with this CMOS system effort we are developing mm/submm systems and demonstrating new applications for CMOS based systems.

One of these is a gas sensor based on an integrated BiCMOS Rx/Tx system from IBM. Figure 1 shows a spectroscopic result from this system. We are finishing an end-to-end analysis of this system operating in a spectrometer mode and are discussing with IBM personnel spectroscopically desirable features for their next generation systems.

We also continue our work with TI as they develop in-house mm/submm systems related to our other work.

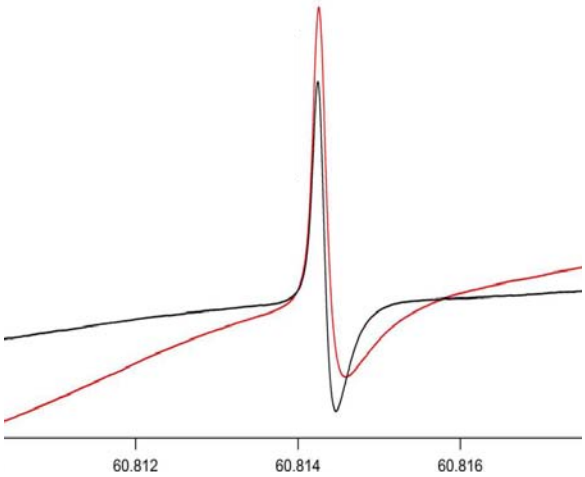


Figure 1. Output of IBM Tx/Rx based spectrometer for a line of OCS near 60 GHz.

We are planning a trip in the near term to help them optimize their systems and to consider the adaptation of a TI synthesizer for both of our use.

Additionally, for a demonstration of mm/submm diagnostics and process control on a commercial unit, Applied Materials has built for us a semiconductor plasma reactor with appropriate ports for a mm/submm probe. We expect this unit to ship in ~1 week. OSU has in place appropriate vacuum and pumping and a spectrometer so that we can rapidly demonstrate the utility of this approach for diagnostics and process control in semiconductor reactor plasmas.

**Keywords:** compact submillimeter spectroscopic gas sensor

## INDUSTRY INTERACTIONS

Texas Instruments, IBM, Applied Materials

## MAJOR PAPER

[1] Medvedev, Neese, De Lucia, and Plummer, Applied Optics 50, 3028, 2011.

# TASK 1836.054 SILICON BASED BEAMFORMING ARRAYS FOR MILLIMETER WAVE SYSTEMS

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## SIGNIFICANCE AND OBJECTIVES

In our current research task, we have developed phase array imaging software toolbox to verify mathematical models for the proposed imaging system without lens. Our mathematical models do not make the Fresnel zone approximation which requires quadratic phase terms. The coherent data can be mathematically constructed to form a focused image of the target without need for lens.

## TECHNICAL APPROACH

There are many challenges and opportunities for integration of antenna arrays into silicon substrate for millimeter imaging systems. Two dimensional target imaging requires reflected wave data to be collected by transceivers over two dimensions. Here, the reflected wave data is collected over different beam steering angles and different spatial level of transceiver array. Resolution of reconstructed image is a function of several parameters including number of transceivers, antenna spacing and the frequency of imaging system. We will incorporate this 2D beamforming array into silicon on chip with the aid of our industrial and TXACE collaborators.

## SUMMARY OF RESULTS

The main goal of the project is to build an imaging system that deploys the beamforming algorithm instead of mechanical scanning in the millimeter wave range. The antenna array and the receiver channels as well as the required phase shifters have been implemented in a phased array imaging simulator as a package of MATLAB toolbox. Particularly, we have developed a phased array imaging simulator to enable the user to model an end-to-end phased array imaging system. Imaging toolbox provides algorithms and tools for the design, simulation, and analysis of phased array signal processing systems. With aid of the toolbox, it will be easier to analyze algorithms for image reconstruction under varying antenna array parameters, size, spacing, coupling, antenna element pattern, and calibration errors. Highly functional graphical user interface (GUI) as shown in Fig. 1 allows designers to quickly define and verify required array size and resolution limits for imaging reconstruction algorithms. With the help of the toolbox, designers can accurately verify the limits of high-resolution signal processing algorithms before integrating them into silicon substrate.

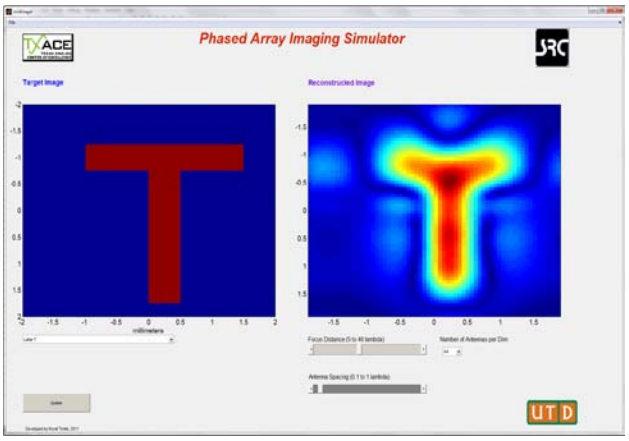


**Figure 1: Phased Array Imaging Simulator**

We can analyze different array geometries and beamforming weights, evaluate impact of phase and amplitude errors, mutual coupling between antenna elements, and impedance matching on the image resolution and target identification. Fully functional version of phase array imaging toolbox will allow rapid analysis of on-chip 2D antenna arrays in mmWave frequencies, comprising on-chip antenna elements such as patch, dipole, or user supplied element pattern.

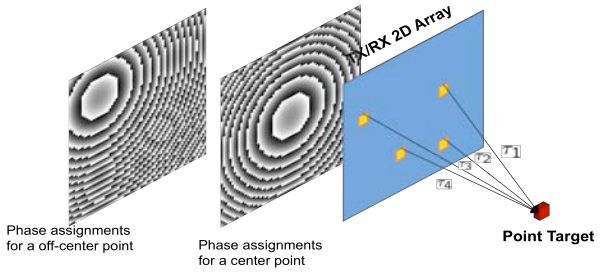


**Figure 2: 2D Imaging System needs phase assignments determined based on the location of the point target.**

**Keywords:** millimeter waves, imaging, beamforming, silicon antennas, antenna array

## INDUSTRY INTERACTIONS

Texas Instruments, IBM

## MAJOR PAPERS/PATENTS

[1] S. Patole and M. Torlak, "Two-Dimensional Millimeter-Wave Array Imaging with Beam-Steered Data," *IEEE Trans. On Antennas and Propagation*, in preparation.

# TASK 1836.067 CHARACTERIZATION OF CMOS BASIC BUILDING BLOCKS FOR SUB-THZ WIDEBAND TRANSMITTERS

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## SIGNIFICANCE AND OBJECTIVES

As the electronic industry continues to make progress, higher operating frequencies are desired to meet larger bandwidth communication, higher imaging resolution, and facilitate antenna integration with on-chip transceivers. The objective of this proposal is to develop an optimum design procedure for efficient wide band transmitters in the WR5 (140-220GHz) range, and bench mark the resulting transmitter architectures against existing discrete sub THz systems.

## TECHNICAL APPROACH

To increase the output power of CMOS sub THz sources, active combining using power amplifier stages will be incorporated in harmonic based N-push oscillators. This technique will be compared against the amplification at lower frequency and using frequency multipiers. Spatial combining and traditional on-chip combiners such as Wilkinson and transformer combiners will also be considered. In the mm-wave and sub-THz regions, the quality factor of the varactors in any oscillator dominates the tank losses. Achieving wide tuning range would require other techniques for frequency tuning. This will be done using magnetic tuning or tuning based on changing the properties of the active devices in the oscillator core.

## SUMMARY OF RESULTS

Signal generation is a challenge at sub THz frequencies due to the limitation of fmax of the CMOS process and the low quality factor of passive components due to substrate losses. Our approach is based on using a triple push oscillator with active combining network where three coupled fundamental oscillators generate identical signals which are $2\pi/3$ apart in phase as shown in Fig. 1. Advantages of N-push oscillators include better tuning range and lower phase noise. The core oscillator is designed at 71GHz using Colpitts topology. The third harmonic is combined at the output to produce a signal at 213GHz. The tuning range of the oscillator has been increased to 15 GHz using digitally controlled artificial dielectric. Table 1 summarizes the results.

Design of power amplifiers at sub-terahertz frequencies is severely limited by $f_t$ of the CMOS process and the lossy metal stack. State of the art work has reported an output power of 6dBm at 150GHz. We use a cascaded dissimilar distributive amplifier approach shown in Fig.2 to realize the PA. The advantages of such a configuration include higher bandwidth and ease of design. The gate voltage in a cascaded DA is doubled after each stage hence increasing gain. A dissimilar last stage (scaled) increases output power by increasing drain current. 8dBm of output power at 160GHz was achieved with a bandwidth of above 80 GHz. Power combining techniques were also investigated and a 0.8dB loss Wilkinson Power combiner was achieved at 200GHz for 2 way combining.

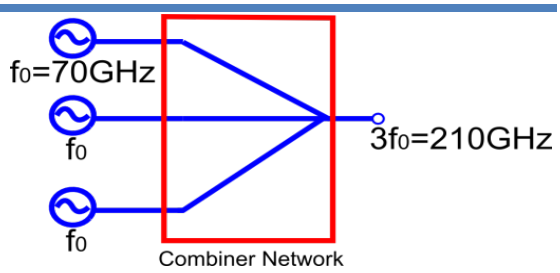


Figure 1: Triple push oscillator configuration.

Table 1: Simulation Results of TPO

| Tech. | $f_0$ | Tuning Range | Output Power | DC Power |
|---|---|---|---|---|
| 65nm CMOS | 215GHz | 213-228GHz | -18dBm | 19mW |

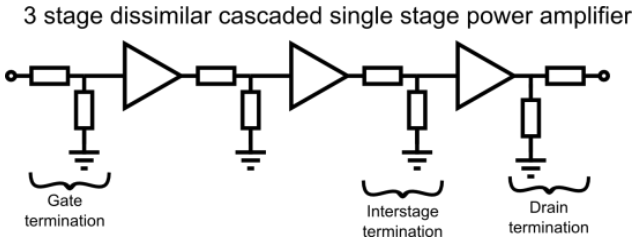


Figure 2: Power amplifier for 160GHz.

**Keywords:** N-push operation, on-chip power combiners, CMOS THz generation, VCOs, power amplifiers

## INDUSTRY INTERACTIONS

Texas Instruments, Intel.

## MAJOR PAPERS/PATENTS

[1] Sriram Muralidharan, Mona Hella, "A 213GHz - 228GHz, -91dB/Hz Phase Noise Triple Push Oscillator in 65nm CMOS", IEEE International Symposium on Circuits and Systems (ISCAS), 2012.

# TASK 1836.074 SUB-45NM CIRCUIT DESIGN FOR TRUE RANDOM NUMBER GENERATION AND CHIP IDENTIFICATION

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## SIGNIFICANCE AND OBJECTIVES

Cryptographic functions are increasingly needed in integrated circuits. Fortunately process variations and noise can be used to provide chip identifiers and true random number generation. This project explores novel techniques and metrics for these functions in CMOS technologies below 45nm.

## TECHNICAL APPROACH

A combination of circuit analysis, simulation and prototyping are used to develop novel circuits and protocols for chip identification and true random number generation (TRNG). Specifically, we develop arbiter-based physically unclonable functions (PUF) and metastability-based TRNGs. We also explore the use of existing SRAM for both of these functions. Statistical metrics that link CMOS behavior with cryptographic functionality are developed. SPICE simulations using predictive technology models down to 7nm allow speculation about technology trends. Prototyping in 32nm custom test chips and off-the-shelf FPGAs allow realistic measurements of actual noise and process variations to validate the SPICE results.

## SUMMARY OF RESULTS

This project consists of two types of functions: 1) PUFs and 2) TRNGs, and two perspectives of each: A) circuit design, and B) statistical metrics and protocols. Four PhD and several MS students have worked on the project.

Vikram Suresh has done internships at both AMD and Intel in the last year working on SRAM design and cryptography accelerators respectively. In [2], he developed new TRNG circuit techniques with a modified pre-charge that shows improved performance in the presence of process variation induced bias. In the coming year, he will be developing stochastic characterizations which directly translate process variation and noise statistics to the resulting random numbers, focusing on thermal noise that is the physical source of randomness in these circuits.

In [3], Lang Lin et al reported on our 45nm PUF test chip which showed good uniqueness and reliability metrics arbiter-based PUFs. Lang has since finished his PhD and is now working at Intel on I/O circuit design.

Burleson is collaborating with Dan Holcomb and others in developing PUF circuits based on the data retention voltage of SRAM [1]. This improves upon our previous highly cited work on power-up state of SRAM (Figure 1).

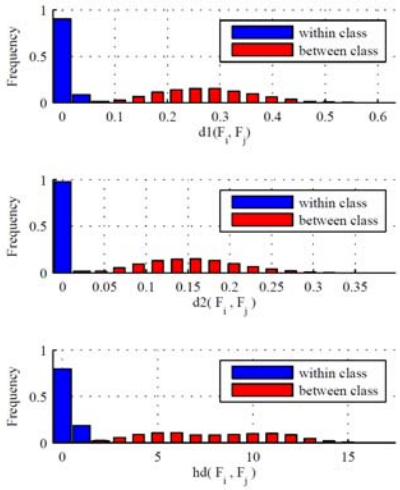


**Figure 1: Chip Identification results comparing the new DRV metrics vs. power-up state metrics. A clear improvement in delineation between within class and between class is shown in the top 2 plots vs. the bottom one (to appear RFIDSec 2012).**

New PhD students, Xiaolin Xu and Raghavan Kumar are exploring novel PUF schemes using FPGAs and are designing a 32nm test chip with several PUFs and TRNGs.

Burleson and Paar are collaborating with EPFL, Swiss on using PUFs in an implantable medical device [4] .

**Keywords:** PUF, TRNG, process variation, noise, cryptography

## INDUSTRY INTERACTIONS

Intel, AMD, IBM

## MAJOR PAPERS/PATENTS

[1] D. Holcomb et al "DRV-Fingerprinting: Using Data Retention Voltage of SRAM Cells for Chip Identification", RFIDSec (to appear), 2012.

[2] V. Suresh, W. Burleson, "Robust Metastability-based TRNG Design in Nanometer CMOS with Sub-Vdd Pre-charge and Hybrid Self-calibration," ISQED 2012.

[3] L. Lin, et al, "Design and Validation of arbiter-Based PUFs for Sub-45nm LowPower Security Applications," IEEE Trans. Info. Forensics & Security (to appear), 2012.

[4] W. Burleson et al. "Design Challenges in Secure Implantable Medical Devices," DAC 2012

# TASK 1836.079 CMOS THZ DETECTION

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## SIGNIFICANCE AND OBJECTIVES

This task investigates both plasmonic devices and super regenerative receiver based THz detector building blocks in 65 nm CMOS technology. The main focus is to realize a low cost, low power THz detector array with high responsivity and sensitivity for security, nondestructive industrial quality control, and medical-diagnosis.

## TECHNICAL APPROACH

Systematic modeling of the silicon FETs as THz detector is essential to understand the effect of different circuit parameters. In this regard, Spice modeling based on distributed channel and Medici Software has been used to quantify the plasma effect. On chip patch antenna is included to increase the coupling and therefore increase the responsivity. Another detector topology based on super regenerative receiver is also being investigated. This low power, area efficient topology provides exponential gain to the incoming radiation, but suffers from poor frequency selectivity. Optimum quenching signal and use of band limited negative resistance tank can improve the selectivity.

## SUMMARY OF RESULTS

To characterize the 65 nm device as terahertz detector for both the open drain and dc biased condition and validate the analytical and TI kit bsim4 model with the experimental data, three detectors with different configurations have been sent for fabrication. Each detector block consists of an on-chip patch antenna and MOS devices in single, series, parallel connection. Each detector has the same equivalent width and length to compare their responses in different configurations.

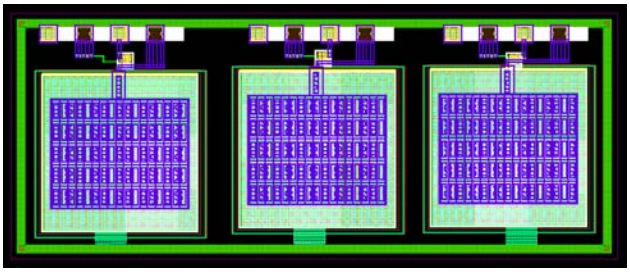

**Figure 1: Submitted Chip with device W/L ratio from left to right as 1.8µ/.14µ, 1.8µ/.07µ (two devices in series), 0.9µ/0.14µ (two devices in parallel).**

Recently, super regenerative receiver (SRR) has been introduced as a potential terahertz detector. With its exponential gain, low power consumption and low form factor, this topology can be an optimum solution as long as the received signal can be detected non-coherently. SRR topology depends on the change of start-up time of an oscillator. With the increasing incoming signal close to the oscillator resonant frequency, the start-up time decreases and by detecting the startup time information, presence of the incoming signal can be detected. The major drawback of a SRR is its low frequency selectivity. Arbitrary shape quenching signal and the use of band limited negative resistance are being investigated to address this issue.

Plasmonic device based detector offers high operating frequency (much much greater than the device cut off frequency) at the cost of a lower responsivity, therefore, to compete with these detectors, some topology based on inter-modulation has been reported. This can also be done with super harmonic injection locked oscillator. These topologies will also be explored. A new THz SPICE model capable of simulating FETs in a plasmonic mode of operation at frequencies far above the device cutoff frequency has also been demonstrated. The model uses a distributed RC or RLC network and is validated by comparison of the simulation results with our analytical model of the plasmonic detector and with measured results. It allows the determination of the operation regimes, where conventional SPICE models are still applicable. The applicability of this model for THz sensing applications is demonstrated by simulating the plasmonic THz FET sensor with on-chip amplifier.

**Keywords:** THz detection, on chip patch antenna, THz imaging, super regenerative receiver

## INDUSTRY INTERACTIONS

Texas Instruments, Intel

## MAJOR PAPERS/PATENTS

[1] A. Gutin, et al. “High Responsivity Terahertz Plasmonic Detector with On-Chip Amplifier,” IEEE Sensors, 2012.

# TASK 1836.082 LOW-COST ENERGY-EFFICIENT 60GHZ TRANSCEIVERS WITH BUILT-IN SELF-TEST (BIST)

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ALI NIKNEJAD, UC BERKELEY

## SIGNIFICANCE AND OBJECTIVES

Although CMOS-based 60GHz transceivers have entered commercial production, the cost and power consumption of these designs must be reduced substantially to enable broad adoption. This project will therefore explore techniques to both drastically improve 60GHz transceiver energy-efficiency and to eliminate the need for expensive mm-wave packaging and external testing.

## TECHNICAL APPROACH

The cost of mm-wave transceivers is often dominated by packaging and testing considerations. A key thrust of this project is therefore to explore efficient and compact on-chip mm-wave antenna arrays in order to enable the use of inexpensive packaging as well as built-in self-testing of the entire signaling path. Furthermore, aggressive power reduction is being pursued through optimized design of both the mm-wave and baseband CMOS circuits. Specifically, high-impedance and low-overhead circuitry phase-array elements are critical to reducing the power of the mm-wave circuitry, and a mixed-signal processing approach appears promising in achieving drastic reductions in baseband power.

## SUMMARY OF RESULTS

Most mm-wave wireless communication systems target relatively short distances (3-5m) and utilize relatively large phased-arrays for improved SNR and to mitigate interference. As a result, the per-element output power of each TX element in the array is typically quite low (~0dBm). In this regime, the efficiency of traditional TX elements is dominated by the fixed power overheads of blocks such as modulators and phase shifters.

In order to eliminate these overheads and improve mm-wave TX element efficiency, a newly proposed TX design utilizing a pulsed-oscillator was developed (Fig. 1). The TX is based on the observation that the phase of the oscillator can be determined by the start-up instant of the oscillator relative to a baseband clock. Thus, stopping and then re-starting the oscillator at a new phase at the beginning of each baseband symbol enables both phase-modulation (e.g., QPSK) as well as phase shifting (for phased-array functionality). The proposed design was fabricated in a 65nm CMOS process, and achieves 4.65% efficiency at 10Gb/s and 0dBm average output power – representing an improvement ~1.8X in efficiency over the best previous design.

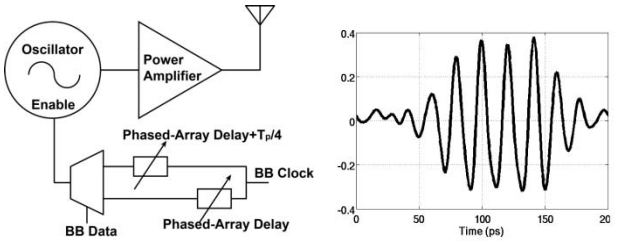


**Figure 1: Proposed low-power mm-wave TX element and its measured output waveform from a 65nm CMOS design.**

This project's second main thrust of recent progress is in exploring efficient on-chip antennas. For conventional standing-wave antennas such as patch, the limited thickness of the inter-metal dielectric (IMD) layers in standard CMOS processes directly limits both the efficiency and the bandwidth of the antenna. This project has therefore pursued microstrip leaky-wave antennas utilizing the first higher mode ($EH_1$) for improved efficiency and higher bandwidth (due to the traveling wave characteristic). An array of 4 of these on-chip antenna designs was prototyped as part of a 65nm 260GHz transceiver, and the measured radiation pattern is reasonably well-matched to simulations (Fig. 2).

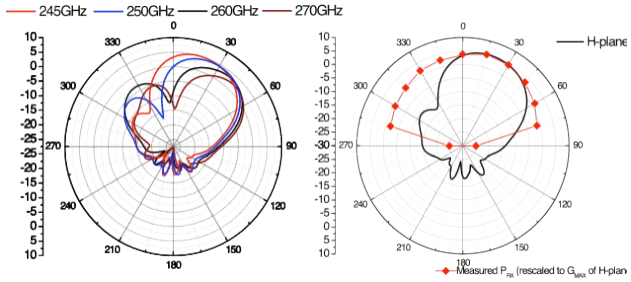


**Figure 2: a) Simulated and b) measured radiation pattern of the 260GHz microstrip leaky-wave antenna.**

**Keywords:** mm-wave, antennas, low-power, mixed-signal

## INDUSTRY INTERACTIONS

Texas Instruments, Intel, IBM

## MAJOR PAPERS/PATENTS

[1] J. D. Park et al., "A 260GHz Fully Integrated CMOS Transceiver for Wireless Chip-to-Chip Communication," IEEE Symposium on VLSI Circuits, June 2012.

[2] L. Kong and E. Aon, "A 21.5mW 10+gb/s mm-Wave Phased-Array Transmitter in 65nm CMOS," IEEE Symposium on VLSI Circuits, June 2012.

# TASK 1836.083 BUILT-IN TEST FOR POWER-EFFICIENT MILLIMETER-WAVE ARRAYS

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## SIGNIFICANCE AND OBJECTIVES

This program will develop orthogonal code-based built-in-test techniques for millimeter-wave arrays which will allow for simultaneous testing of all elements in the array at either circuit or package level, reducing the time and cost of test. Power-efficient 60GHz transmitter structures with BIST will be demonstrated.

## TECHNICAL APPROACH

A low-power 60GHz phased-array transmitter prototype with built-in-self-test will be developed in 0.12µm SiGe BiCMOS technology and then scalable test techniques will be developed for this demonstration platform. These test techniques will exploit code-division multiple-access techniques to allow for simultaneous or parallel testing of all array elements. CDMA-based test techniques will be compared to both external test and traditional BIST techniques. A single transmit chain will be developed followed by a four-element 60-GHz phased-array prototype.

## SUMMARY OF RESULTS

In the previous year, we have designed and taped-out our first-generation 60-GHz transmitter circuits in IBM 0.12µm SiGe BiCMOS technology. A two-stage class-AB power amplifier (PA) was developed which achieved 27dB gain, 8.1dBm output-referred $P_{1dB}$ and 18% peak power-added efficiency (PAE) in simulations. Second, a passive reflection-type phase shifter was developed which employed a dual-resonant reflective load topology to achieve a full 360° phase shift in a single stage. Unfortunately, the limited tuning range and quality factor of the varactors increases insertion loss to >15dB which is too high for use in the array. Finally, a millimeter-wave power detector was developed for built-in power monitoring through the array. All three of these circuits were taped out in Aug. 2011 and the hardware has been received. Measurements will be completed in 3Q-2012.

Second, we have developed second-generation 60GHz transmitter circuits working to increase power efficiency of the PA and improve the performance of the phase shifter. The new PA employs 2nd and 3rd harmonic termination to "square up" the output voltage waveform and reduce current/voltage overlap. This 2nd generation PA achieves a simulated peak PAE of 32% at 59GHz and an output $P_{1dB}$ of 14dBm. A stand-alone version of this PA was taped out in July 2012 to demonstrate this state-of-the-art PA performance. Our second-generation phase shifter was completely redesigned moving to a vector interpolator topology to achieve flat amplitude versus phase response. According to simulations, the interpolator achieves 6-7dB gain and 11-12dB noise figure. A four-bit design was implemented with <2° RMS phase error across 57-66GHz. This phase shifter will be taped out along with the PA in 4Q-2012.

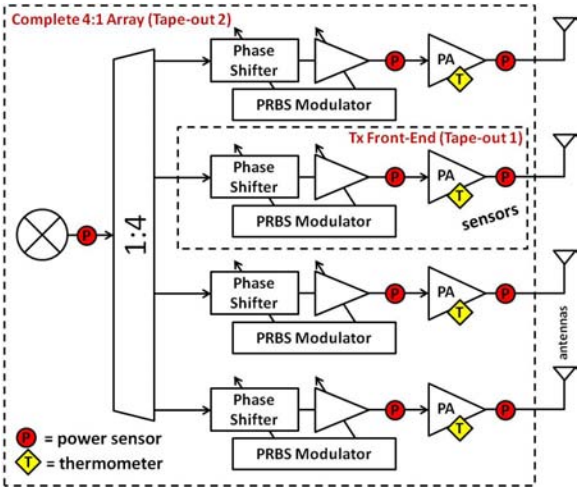


**Figure 1: Block diagram of proposed 60-GHz phased-array prototype with built-in-test capabilities.**

Finally, in the previous year we have developed behavioral models for Code-Modulated built-in Test (CMT), with architecture similar to that shown in Fig. 1. Using ADS, we have demonstrated CMT using simple Walsh codes showing the ability to simultaneously measure output power from each element in the array.

In the upcoming year, we will measure the 1st and 2nd generation circuits. We also plan to develop a multi-element phased array prototype with built-in test and submit for fabrication. Finally, we will extend our behavioral investigations of CMT beyond simple power measurement to include other needed transmitter performance metrics.

**Keywords:** millimeter-wave, phased-arrays, built-in test, 60GHz, CDMA

## INDUSTRY INTERACTIONS

Intel

## MAJOR PAPERS/PATENTS

[1] A. Sarkar and B. Floyd, "Power-efficient power amplifiers for 60GHz phased-array transmitters," accepted to 2012 SRC TECHCON, Sept. 2012.

# TASK 1836.091 INTERCONNECTS ON FLEXIBLE PLASTIC SUBSTRATES

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## SIGNIFICANCE AND OBJECTIVES

Interconnects which operate in the sub-THz range can perform over very large bandwidths and are well suited for high data-rate communication systems. This task is investigating dielectric waveguides that support low loss, low distortion, low crosstalk, and strong radiation confinement.

## TECHNICAL APPROACH

This task focuses on the design/simulation of candidate waveguides in CST Microwave Studio. The classic mechanism for guiding in dielectrics is total internal reflection where radiation is confined in a region of high-refractive index cladded by a low-index region. This task has focused on exploring alternatives and improvements to this technique with photonic crystals and photonic band gap (PBG) structures. It is our hope that these designs can serve as viable standalone devices or that they may augment and improve conventional index guiding designs for THz/sub-THz interconnects by reducing signal attenuation and reducing bending leakage and crosstalk.

## SUMMARY OF RESULTS

The first interconnect design is based on the well-known 1D Bragg reflector, which consists of a stack of alternating high and low refractive index regions. The presented design will be fabricated with of low-loss polypropylene and a polypropylene/$TiO_2$ nanopowder composite.

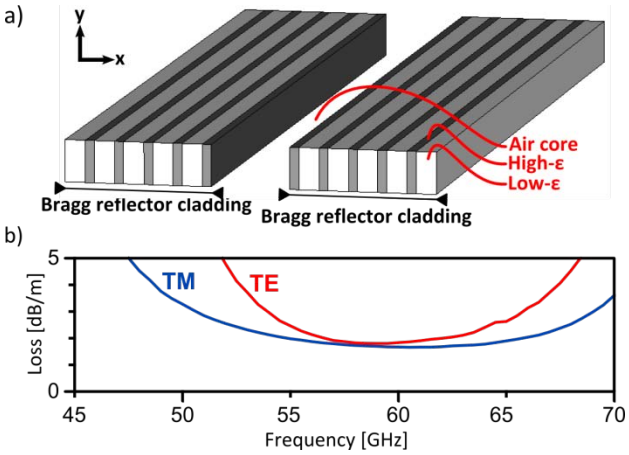


**Figure 1: Depiction of 1D Bragg reflector interconnect with air core (a) and simulated absorption/leakage losses for TE/TM polarized modes.**

This structure acts as a reflector over a range of frequencies and a waveguide channel can be formed as depicted in Figure 1(a). Unlike total internal reflection, the 1D Bragg reflector can confine radiation to a low refractive index region, such as air. Simulations indicate that the 1D Bragg reflector interconnect is able to support very low leakage/absorption losses over a 20% - 33% bandwidth.

The second interconnect design being investigated consists of a slab of polypropylene/$TiO_2$ nanopowder composite that is perforated by a hexagonal lattice of air holes. A schematic of the design is shown in Figure 2(a) and although this design supports a much narrower operating bandwidth and higher attenuation, it has a very strong E-field confinement as shown in the field pattern plot. This design would be well suited for a parallel and densely spaced interconnect architecture. Table 1 summarizes the projected performance of the investigated designs.

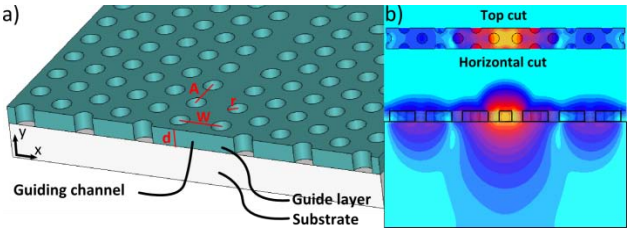


**Figure 2: Depiction of 2D Air-hole pattern interconnect (a) and E-field magnitude of fundamental mode (b)**

The designs investigated here show promise for supporting low signal attenuation, large bandwidths, and strong radiation confinement for future high speed chip to chip and board to board interconnects. Fabrication efforts will begin in late summer 2012 at the Microelectronics Research Center.

**Table 1: Projected performance of PBG interconnects**

| | 1D Bragg | 2D Hole Pattern |
|---|---|---|
| Attenuation | < 5 dB/m | 12 - 20 dB/m |
| Bandwidth | 20% - 33% | ~ 3.6% |
| E-field leakage | ~ 15dB at $1\lambda_0$ | ~ 30dB at $1\lambda_0$ |

**Keywords:** interconnects, waveguides, THz, dielectric, flexible

## INDUSTRY INTERACTIONS

Texas Instruments

# TASK 1836.101, SPARSE 2D MIMO RADAR TRANSCEIVER DESIGN AND PROTOTYPING FOR 3D MILLIMETER-WAVE IMAGING

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## SIGNIFICANCE AND OBJECTIVES

Millimeter wave (*mm*-wave) radar technology can be used for many safety, health care and commercial applications. In an effort to achieve a higher level of precision and affordability of such systems, sparse multiple-input-multiple-output (MIMO) radar technologies are explored within the mm-wave framework in this project.

## TECHNICAL APPROACH

The transceiver design for the MIMO radar *mm*-wave imaging system involves waveform design, antenna array design, and image processing techniques. In this project, three dimensional *mm*-wave imagers will be designed in order to obtain images of objects placed behind obstacles or inside closed boxes. A two-dimensional sparse MIMO transceiver array will be designed to help reduce the number of transceivers. In addition, sparse two-dimensional arrangements of the transceiver arrays will be designed in order to attain further spatial diversity. Finally, a prototype system will be built to test the algorithms designed in this project.

## SUMMARY OF RESULTS

In PI's previous work [2], the performance of an MIMO radar imaging system was compared with the traditional one, and it was demonstrated that the deployment of space-time block–codes in the transmit waveforms had the capability to yield further improvements. In this work, we make use of multiple such MIMO radar imaging systems to obtain three dimensional images.

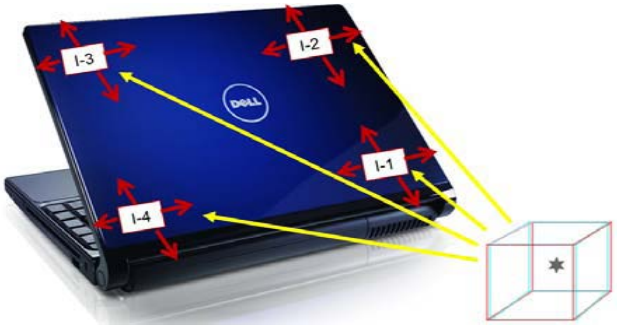


**Figure 1: Illustration of the placement of four mm-wave imaging systems used to capture a 3D image**

The idea originated from another work of the PI's [1] where the use of multiple imaging systems in sensor network target localization was proposed for the purpose of surveillance. Multiple mm-wave imaging systems were placed at different locations, which capture the target image in different angle bins depending on their positions relative to the target. These angular directions are then interpolated to obtain the target's position. A similar approach will be explored in the proposed project in a smaller scale in order to identify a target in a close range. While the 2D sparse array has a separation in the order of half the wavelength inside an imaging system, several of these "imaging systems" will be placed in the order of several inches apart to obtain localization that will lead to 3D images (Fig. 1).

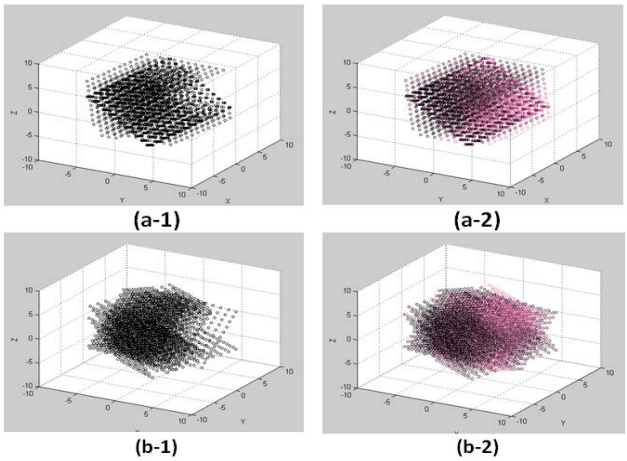


**Figure 2: (a-1) and (b-1) are targets from two different angles; (a-2) and (b-2) are the respective 3D images.**

The initial numerical results are demonstrated in Fig. 2, where the 3D target object (dark black region) and the estimated target image are shown from two different angles. Further research is in progress to enhance this system to make it more versatile and realistic.

**Keywords:** MIMO Radar; millimeter wave; 3D imaging; reflectivity coefficient; transmit diversity.

## INDUSTRY INTERACTIONS

Texas Instruments, Intel

## MAJOR PAPERS/PATENTS

[1] T. Ali et al., "MIMO Radar Imaging for Target Detection and Localization in Sensor Networks," IEEE Systems Journal: Special Issue on Sensor Networks for Advanced Localization Systems (submitted), May 2011.

[2] A. Sadeque et al., "Space-Time Block Codes for MIMO Radar Imaging," IEEE Transactions on Aerospace and Electronic Systems (submitted), April 2012.

# 1836.102 SUPERRESOLUTION TECHNIQUES FOR 3D MILLIMETER WAVE RADARS

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## SIGNIFICANCE AND OBJECTIVES

We propose to develop novel three dimensional millimeter wave signal processing techniques and millimeter propagation channel models to fully reconstruct three-dimensional (3-D) image from data gathered over a 2-D aperture. Aperture will consist of wideband transmitters and receivers implemented by industrial collaborators in silicon technology.

## TECHNICAL APPROACH

There are many challenges and opportunities for integration of antenna arrays into silicon substrate for millimeter imaging systems. Two dimensional target imaging requires reflected wave data to be collected by transceivers over two dimensions. Here, the reflected wave data is collected over different beam steering angles and different spatial level of transceiver array. Resolution of reconstructed image is a function of several parameters including number of transceivers, antenna spacing and the frequency of imaging system. We will incorporate this 2D beamforming array into silicon on chip with the aid of our industrial and TxACE collaborators.

## SUMMARY OF RESULTS

Analytical model of an active imaging system depends on accurate representation of the source/target interaction. For our implementation, we have considered three candidate imaging modalities: (i) Bistatic imaging, (ii) monostatic imaging, and (iii) transmission imaging. In this proposal, we will focus on three-dimensional (3D) monostatic echo imaging. In our previous research task (Task 1836.054), we have developed mathematical models implemented into phase array imaging software toolbox. Our mathematical models do not make any far field assumptions (Fresnel zone approximation requires quadratic phase terms). The coherent data can be mathematically constructed to form a focused image of the target without need for lens. Our goal is to develop a target localization system with high sensitivity and resolution. We have studied various physical challenges to address the limitations of existing systems. Based on our study, we will assess the potential performance of various sub-mm wave imaging techniques to determine the most promising three dimensional millimeter wave radar architecture and design. Our initial assessment will include determining antenna configuration, bandwidth of the waveforms, center frequency, signal resolution, target features, target illumination, scattering characteristics, and transmitter and receiver performance.

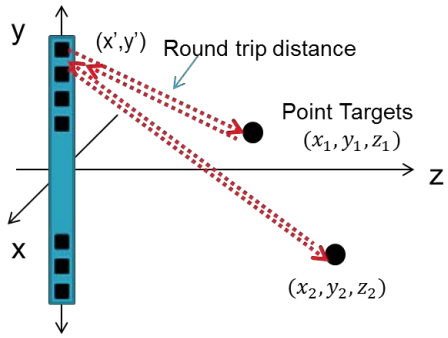
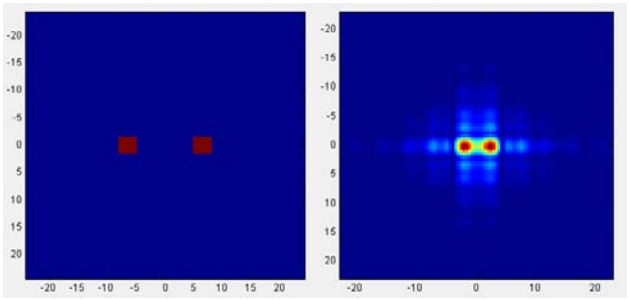



**Figure 1 Localization of 3D near-field targets.**

Conventional approaches rely on triangulation, beamforming, or time delay estimation. To improve the resolution performance, we have developed a subspace technique for the localization of near-field targets in three dimensional geometry (i.e., Figure 1). We have also expanded our previously built Phased Array Imaging Simulator Toolbox to demonstrate capabilities our proposed approach for closed space near-field sources as shown in Fig. 2.



**Keywords:** superresolution signal processing, millimeter radars, beamforming, silicon antennas, antenna array

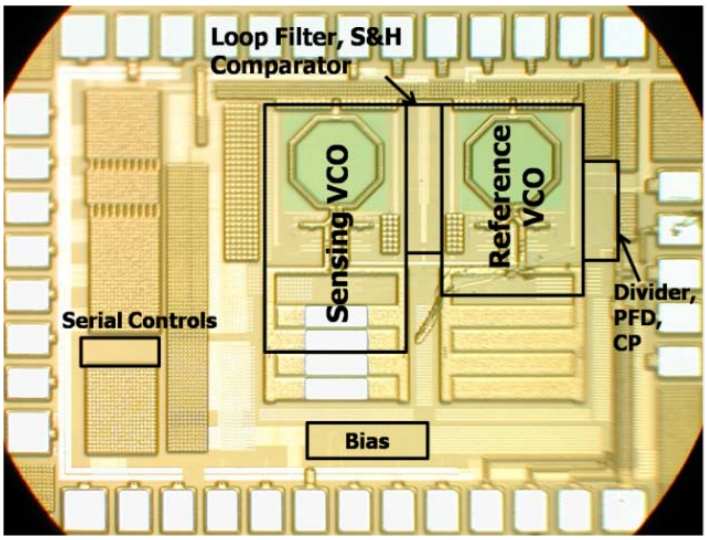
## INDUSTRY INTERACTIONS

Texas Instruments, IBM

## MAJOR PAPERS/PATENTS

[1] S. Patole and M. Torlak, "Two-Dimensional Millimeter-Wave Array Imaging with Beam-Steered Data," IEEE Trans. On Antennas and Propagation, (to be submitted).

# Health Care Thrust




Chemical fraction sensing chip fabricated in 90-nm CMOS (PI: K. Entesari)

## Summary of Accomplishments

| Category | Accomplishment |
|---|---|
| Health Care | Demonstrated a capacitive sensing technique in a VCO inside a PLL for measurement of organic liquid fraction. A reference VCO is used along with the sensing VCO to track the frequency changes due to non-systematic drifts. The output is the frequency difference between the two oscillators. A comparator compares the control voltages of the two VCOs to adjust the frequency division value and equate the two control voltages. The frequency shift due to the deposited material is proportional to the difference in division values. The technique is utilized to measure fractional volume of an ethanol and methanol mixture with an accuracy of 1%.<br><br>(1836.066, PI: K. Entesari, Texas A&M University) |

# TASK 1836.042 ADAPTIVE DATA PREDICTION BASED RECEIVER FOR POWER-EFFICIENT HIGH-RESOLUTION ULTRASOUND IMAGING SYSTEMS

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## SIGNIFICANCE AND OBJECTIVES

Traditional ultrasound receivers require power hungry circuits such as time-gain amplifiers (TGC) to accommodate the large dynamic range of the received signals. Although there has been a trend towards low power system with modern ICs, as semiconductor technologies reach device-level limits of operating voltage, saturation in the power reduction rates has been observed. An adaptive-data-prediction-based architecture is proposed in this project to enhance the receiver resolution without extra power cost. With a DSP signal filter and eliminating the TGC circuitry, a 76.3dB DR is achieved in real-time experiments.

## TECHNICAL APPROACH

The proposed adaptive-data-prediction-based receiver contains an amplifier, a mid-resolution ADC, a digital attenuator, an adaptive linear predictor, and a high-resolution DAC. The adaptive linear predictor estimates the coarse amplitude of the next sampled ultrasonic signal, which is converted into an analog format by the high-resolution DAC. A fine error signal is then generated by comparing the input signal and the predicted signal. An amplifier is employed to amplify the error signal to accommodate the dynamic range of ADC, who converts the error signal to the digital signal. Following that, a digital attenuator is needed to scale the amplified digital signal to the original level. Then, a high-resolution output signal is obtained in the digital domain by combining the prediction signal and digitalized error signal.

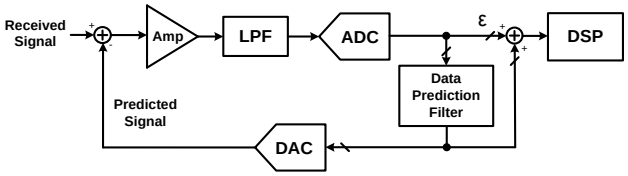


**Figure 1: Block diagram of the ADPB ultrasound imaging receiver.**

The ADPB receiver employs synthetic signal recreation techniques, where the future receiver outputs are estimated as a linear function of the past outputs and the present and past inputs. Design challenge is the implementation of real-time optimization of the DSP filter coefficients such that the synthetic signal closely matches the actual received signal. Therefore, in the project a least-mean-squares (LMS) criterion is proposed to accommodate fast and accurate signal estimation.

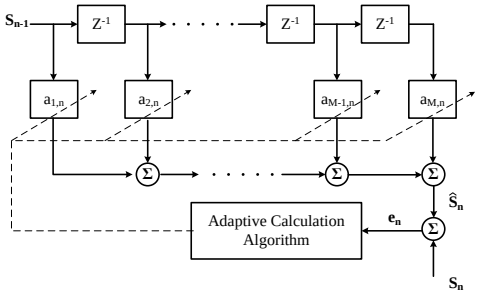


**Figure 2: The DSP filter design with least-mean-square algorithm.**

## SUMMARY OF RESULTS

For the first prototype hardware implementation, an Altera FPGA board and an AD/DA daughter card are employed to demonstrate the proposed ultrasound-imaging receiver architecture. The measurement results are shown in Fig. 3. With an 80.39-dB input DR signal, the output signal DR is 79.97 dB.

| | |
|---|---|
| Input FS Signal | 14-bit |
| Input DR | 80.39 dB |
| DAC Resolution | 14 Bits |
| ADC Resolution | 10 Bits |
| DSP Resolution | 16 Bits |
| Output Signal DR | 79.97 dB |

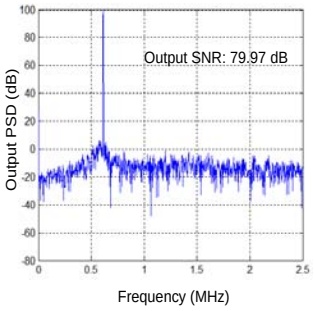


**Figure 3: (a) Performance summary of the proposed receiver and (b) measured receiver output signal-to-noise ratio.**

**Keywords:** Adaptive data prediction, LMS Algorithm.

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] Y. Wang and Dongsheng Ma, *Advanced Research Institute for Biomedical Imaging Workshop*, Oct. 2009.
[2] Y. Wang, M. Koen and Dongsheng Ma, *IEEE Transactions on Circuit and Systems*-II. pp. 26-30, Vol. 58, No. 1, Jan. 2011.
[3] Y. Wang and Dongsheng Ma, *SRC TECHCON,* accepted for publication, Sept. 2012.

# TASK ID# 1836.043, HIGH VOLTAGE LINEAR AMPLIFIER TECHNOLOGY

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## SIGNIFICANCE AND OBJECTIVES

Existing ultrasound transmitters use integrated high-voltage (HV) pulsers to excite the transducer, which suffer from limited usages in enhanced ultrasonic imaging. This project seeks to design a monolithically integrated HV *linear* power amplifier for enhanced ultrasonic imaging quality.

## TECHNICAL APPROACH

Advanced ultrasonic transmitter requires large signal swing (up to 180V), high slew rate (on the order of V/ns), large bandwidth (1-20 MHz), and low second harmonic distortions (HD2) (below -45dB) for enhanced imaging quality. We explore different circuit architectures and circuit design techniques to achieve the above design goals. Both fully differential circuit architecture and single-ended totem-pole topologies are explored. Novel circuit blocks such as current-feedback amplifiers and dynamic current biasing are designed to increase the bandwidth of the HV amplifier and its power efficiency. On the system level, digital pre-distortion (DPD) technique is designed to further improve on the linearity, and power efficiency.

## SUMMARY OF RESULTS

In this project, we have successfully designed, implemented, and demonstrated two generations of HV linear power amplifiers. The first generation is a fully differential HV linear amplifier implemented using TI's 0.7 µm LBCSOI 120 V technology. It is capable of generating a signal swing of 180 V with extremely low HD2 ( < - 58 dB). The results achieved outperform TI's existing TX517 HV pulser. One limitation is that the fully differential structure requires an off-chip transformer to combine the differential signals into a single-ended one, which increases the system area and cost. In the second-generation linear power amplifier, we use a 200V SOI CMOS technology to implement a single-ended linear power amplifier, eliminating the need for the off-chip transformer. In addition, we explore current-feedback techniques to improve the amplifier slew-rate and the bandwidth. In order to suppress the increased signal harmonic distortions associated with the single-ended design, a digital pre-distortion (DPD) technique is designed. Moreover, a dynamic biasing technique is used to further improve the power efficiency. Measurement results show that the HV power amplifiers is capable of producing a signal swing of 180Vpp with an HD2 of -45dB, and a frequency bandwidth that is almost twice that of the first generation. Figure 1 depicts the system block diagram of the HV power amplifier with current feedback with the DPD scheme. Figure 2(a) shows the schematic of the current-feedback linear amplifier, and 2(b) is the measured frequency spectrum (8.5MHz) with low HD2 achieved using the DPD technique.

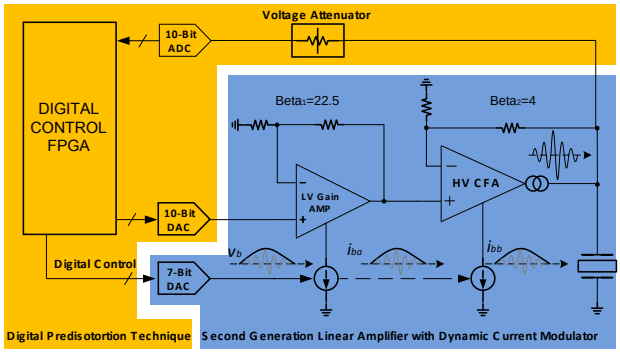
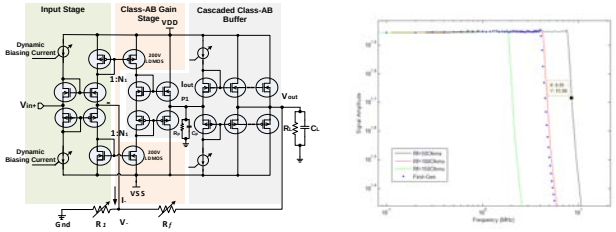



Figure 1: The HV current feedback linear amplifier with cascaded class-AB output and digital pre-distortion scheme.




(a) (b)

Figure 2: (a) Current-feedback amplifier with cascaded class-AB buffer. (b) Measured frequency response show the improved bandwidth by using current-feedback Technique.

**Keywords:** high-voltage, linear amplifier, current-feedback, power efficiency, pre-distortion, ultrasound

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] Z. Gao and P. Gui, "A Look-up-Table Digital Pre-distortion Technique for High-Voltage Power Amplifiers in Ultrasonic Applications" IEEE Transactions on UFFC vol. 59, issue 7, pp. 1550-1557.

[2] Z. Gao, P. Gui, and et al., "An High Voltage Linear Amplifier for Ultrasound Transmitter" SRC TECHON, Sept. 2010, Austin, Texas.

[3] Z. Gao and P. Gui, "A Digital-Feedback Pre-distortion Technique for Integrated High-Voltage Ultrasound Transmitting Power Amplifiers" Proceedings of IEEE International Ultrasonic Symposium, 2011.

[4]Gao and P. Gui, "A Digital Predistortion Technique for High-Voltage Power Amplifiers in Ultrasonic Transmitting applications," U.S. Patent application filed.

[5] Z. Gao, P. Gui, and et al., "An Integrated High-Voltage Low-Distortion Current-Feedback Linear Power Amplifier for Ultrasound Transmitters using Digital Predistortion and Dynamic Current Biasing Techniques" IEEE Transaction on Biomedical Circuits (under review).

# TASK 1836.052 AN ULTRA-LOW POWER SIGNAL PROCESSING WITH SMART ANALOG-ENABLED PRE-CONDITIONING STAGE FOR INERTIAL SENSING APPLICATIONS

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## SIGNIFICANCE AND OBJECTIVES

The proposed research explores the first of a kind ultra-low power programmable signal processing architectures for wearable computers. Our proposed system will enable the next generation of self-powered wearable computers that can operate with approximately tens of µW harvested through piezo-electric and thermo-electric devices. This research is also enabling the first of a kind sub-threshold digital logic and memory units operating at approximately 200mV. The advantage of the proposed circuits lies in extremely low leakage power, an essential feature in many biomedical circuits and applications.

## TECHNICAL APPROACH

We reduce the power consumption of the processing architecture by the notion of granular decision making or tiered signal processing. That is, we initially perform signal processing at a lower resolution, and hence at a lower power. If the incoming event significantly deviates from the event of interest, we identify this at a lower resolution, removing the event from the signal processing chain and keeping the remaining (higher resolution) signal processing modules inactive. If the incoming signal appears to be of interest, we gradually increase the resolution (and the power) until we identify the event of interest with sufficient confidence. The proposed architecture, compared to the state-of-the-art low-power microcontrollers, can reduce the power consumption by orders of magnitude. We further investigate ultra-low voltage circuits for the proposed processing and explore design techniques enabling digital logic and SRAM architectures operating at 175 to 200mV.

## SUMMARY OF RESULTS

We implemented several signal processing techniques including dynamic time warping (DTW) for detecting transitional movements (e.g., sit to stands) and discrete wavelet decomposition (DWT) for periodic activities (e.g., walking at a specific speed). We developed algorithmic methodologies to compose the signal processing architecture. For our proposed signal processing architecture, we considered several tunable parameters to adjust the resolution and the power. For example for DTW, the tunable parameters include bit resolution, sampling frequency and the threshold for accepting the incoming signals. We implemented DTW blocks using high-$V_{th}$ CMOS 45nm standard cell libraries.

We created an optimization methodology to determine the optimal set of parameters for DTW signal processing blocks. The power consumption of a 3-tier granular decision making module was measured at 1.23µW compared to the full resolution 1-tier at 6.29µW, achieving approximately an 80% power reduction. Similar signal processing modules were developed for periodic activities using DWT, with the power consumption of 3.82µW compared to 14µW at full resolution, achieving over 80% power reduction. We further created several sub-threshold logic and SRAM modules operating at approximately 175-200mV.

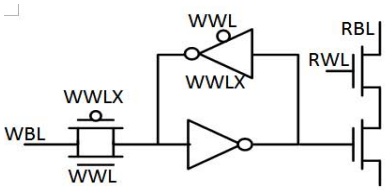


**Figure 1: Our proposed 10T SRAM**

The schematic for the proposed 10T bitcell is shown in Figure 1. We focused on making the basic feedback loop robust. The proposed 10T SRAM has completely isolated bitline for read and write. Therefore there is no constraint to access one row for read and another row for write simultaneously. Our proposed 24-kb SRAM consumes 700nW@50kHz, providing larger than 2X power saving compare to previously proposed subthreshold 6T SRAM. We further synthesized using 45nm TI (GS70) standard cell library. The power consumption of the 12-bit DTW block operating at 14.9 KHz was measured at 0.63nW and 84.91nW for dynamic and leakage, respectively.

**Keywords:** Biomedical Applications, Wearable Computers, Ultra-low Power Signal Processing, Self-powered Processing Architecture, Subthreshold Design

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] Roozbeh Jafari, Reza Lotfian, "A Low Power Wake-up Circuitry Based on Dynamic Time Warping for Body Sensor Networks," International Conference on Body Sensor Networks (BSN), 2011, Dallas, TX.

[2] Hassan Ghasemzadeh, Roozbeh Jafari, "Ultra Low Power Granular Decision Making using Cross Correlation: Optimizing Bit Resolution for Template Matching," IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), (Best Paper Award), 2011, Chicago, IL.

# TASK 1836.055 SPICE MODELS AND ANALOG CIRCUITS FOR NANOSCALE SILICON CHEMICAL- AND BIOLOGICAL-SENSORS

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## SIGNIFICANCE AND OBJECTIVES

Nanoscale chemical and biological sensors have been demonstrated, but little attention has been given to SPICE models and support circuitry. This project will develop physically realistic SPICE models for the sensor device. SPICE model creation will be followed by design of suitable support circuitry for a complete system.

## TECHNICAL APPROACH

The design of circuits to support the biological sensor will require a suitable SPICE model which comprehends the unique properties of this device. Generating such a SPICE model in turn requires a thorough understanding of the physics of the sensor and its operating environment. To improve the understanding of the biosensor device physics and generate the necessary data for a suitable SPICE model, a combination of theoretical analysis and TCAD modeling is being utilized. With a SPICE model available, reference support circuits are being developed.

## SUMMARY OF RESULTS

An example of the sensor element under study is shown in Fig. 1. Studies during the first year of this project provided understanding of the device physics of the biosensor configuration. In the second year, an initial SPICE model was developed.

In this final year, *the first ever SPICE model for these types of sensors was refined and published [1].* Figure 2 shows the pH response obtained using biosensor SPICE model. The model is fitted to pH sensing data obtained for a dual-gated sensor with coupling of back-gate voltage to electrically floating solutions on the top side of sensor. Very good agreement is demonstrated between the model and experimental results.

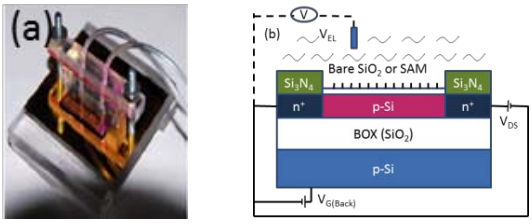


**Figure 1: (a) Photograph of sensor chip mounted on microfluidic delivery system (b) Sensor cross-section with measurement circuit.**

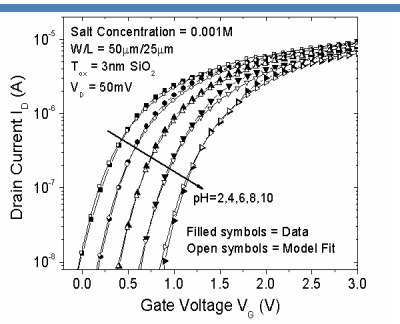


**Figure 2: pH response obtained using the newly refined biosensor SPICE model.**

*A novel transient simulation methodology was developed to simulate the effect of sensor noise on a differential pair amplifier detection circuit [2].* A noise signal was applied to the back gate and reference electrode of a nanoribbon BioFET sensor simulation. The output signal was time-averaged to obtain the noise rms amplitude. The ability to distinguish the sensor signal from the noise was examined for various amounts of noise power and integration (Figure 3). At concentrations below the arrow, the output voltage is dominated by noise.

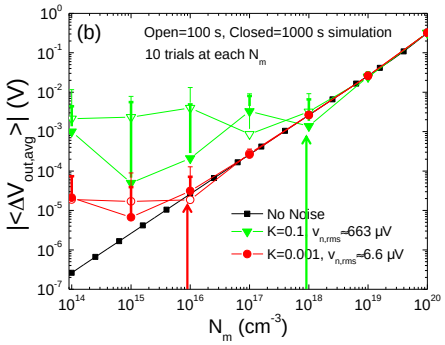


**Figure 3: Output voltage of a differential amplification circuit for various amounts of noise as a function of molecule conc.**

**Keywords:** chemical, biological, sensor, SPICE, model.

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] P. G. Fernandes et al., "SPICE Macromodel of Silicon-on-Insulator-Field-Effect-Transistor-Based Bio Sensors," Sensors and Actuators B **161**, pp. 163-170, 2012.

[2] K. D. Cantley et al., "Noise Effects in FET Biological Detection Circuits," IEEE MWCAS, 2012.

# TASK 1836.061 ANALOG COMPUTING IN HUMAN CELLS

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## SIGNIFICANCE AND OBJECTIVES

The objective of this project is the implementation of molecular circuits capable of responding to specific cellular disease-related signals and producing outputs accordingly that can be quantified using biologically modified field-effect transistors.

## TECHNICAL APPROACH

We are working on providing a framework for bridging endogenous cellular to extracellular information in a "universal" bioFET, programmable by reagents that are prepared according to the tissue type and disease. Our multi-component RNA- and protein- based biosensor circuits will be able to: (a) detect complex conditions related to abnormal expression of a number of molecular signals in mammalian cells, and (b) upon detection release biologically active modules in order to transduce the information to external devices.

## SUMMARY OF RESULTS

Complex combinations of abnormally expressed microRNAs are an excellent indicator of cell state. A system capable to detect these conditions may be used as a highly selective tool for diagnosis and treatment.

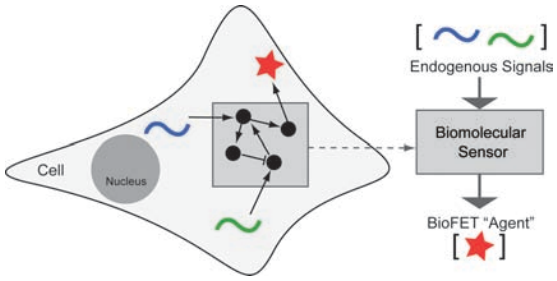


**Figure 1: The biomolecular sensor responding to endogenous signals and producing an output for a bioFET.**

Experimentally, we have been constructing proteins that can transduce endogenous information outside of a cell. We engineered recombinant proteins that "carry" tags that can be identified or bind to a bioFET. Examples include the following: a secreted P53-GFP output designed to interact with a femtomolar P53 biosensor (Hu Lab), which uses silicon nanowires coated with anti-P53 antibodies; and an experiment with a sensor that measures impedance (Prasad Lab), in this case, our gene output is an apoptosis driver, and the proper input leads to reduced impedance due to low cell viability. In addition, we are considering expressing the cell surface proteins with tags that can help attach to appropriately coated impedance measurement device.

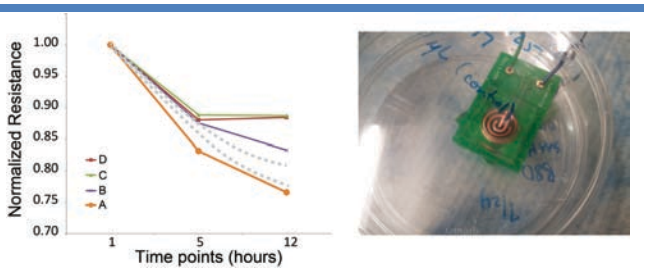


**Figure 2: Resistance measurements. A is the control and B-D are different concentrations of cells. The objective is that the endogenous reading will be along the dashed line.**

MicroRNAs (miRNAs) are involved in critical processes such as growth, differentiation, and apoptosis, therefore the loss or overexpression of critical microRNAs in a given cell type has major implications on cell fate. Our sensors for endogenous microRNA use four fully complementary target sites located in the 3' untranslated region (UTR) of a protein. Since microRNAs repress mRNA activity, for a direct sensor the fluorescent signal is high when the miRNA of interest is absent. An example is included in Fig. 3.

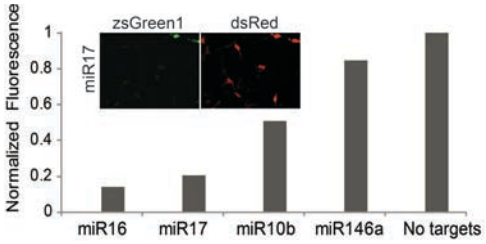


**Figure 3: A direct sensor for different microRNAs. The cells express both red and green, and green has microRNA targets. The results show that mir16 and 17 are the most abundant.**

We have implemented inverter sensors with microRNA targets on a repressor protein, which targets the output. In this case, the signal is high only when the miRNA of interest is present. Both the direct and inverter sensors have restriction enzyme sites within the 3'UTR on either side of the miRNA targets to allow ease in changing the target sites to the miRNA under study. Finally, we are currently designing and testing a toggle-switch based sensor and a fault-tolerant system, both for accurate and robust miRNA sensing.

## MAJOR PAPERS/PATENTS

[1] Taek Kang, Jacob White, Eduardo Sontag and Leonidas Bleris, "Validation of Network Reverse Engineering Using a Benchmark Synthetic Gene Circuit," The Fourth International Workshop on Bio-Design Automation (IWBDA) at DAC, June 2012.

# TASK 1836.064 ULTRA-LOW-POWER ANALOG FRONT-END IC DESIGN FOR IMPLANTABLE CARDIOVERTER DEFIBRILLATOR (ICD) DEVICES

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## SIGNIFICANCE AND OBJECTIVES

The aim of the project is to design ultra-low-power analog front-end (AFE) integrated circuits (ICs) for an implantable cardioverter defibrillator (ICD) device, which can also be used for other implantable devices or low-power biosensor systems. Emphasis is put on exploring system-level and circuit-level techniques to reduce power consumption for battery life extension with robust device reliability.

## TECHNICAL APPROACH

The proposed AFE IC architecture has a differential instrumentation amplifier (INA), a differential band-pass filter (BPF), a differential-to-single-end variable gain amplifier (VGA), and a single-ended successive approximation register (SAR) ADC. The IC allocates the total gain into the two amplifiers (i.e., INA and VGA) and has a high-order BPF sandwiched between them. The relatively complex IC architecture is adopted for good signal-conditioning. The power consumption is reduced by designing low-power blocks on the circuit level, and by combining two channels on the system level.

## SUMMARY OF RESULTS

Fig. 1 shows the proposed AFE IC that combines both the Brady and Tachy channels for the ICD/pacemaker applications; the two channels share one buffer and one ADC to save power.

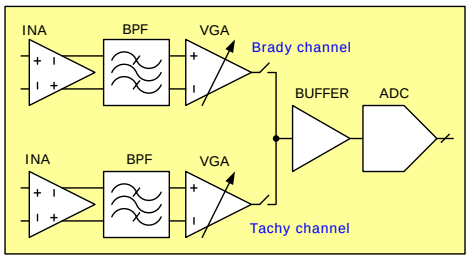


**Figure 1: A system diagram of our proposed AFE IC, with two channels sharing the same buffer and ADC to reduce power.**

Fig. 2 shows the single-ended 8-bit SAR ADC with a reference voltage equal to $V_{REF}/2$ and a novel switching method in the DAC [1]; however, it can digitize input signals within [0, $V_{REF}$]. The ADC achieved a resolution of 7.8 bits at 2 kS/s with only 101 nW in a TI 0.35-$\mu$m process [2]. Figure 3 shows the micrograph of the $G_m$–C filter and the proposed low-power wide-linear-range transconductor schematics. Using the $G_m$ cell as a linear source degeneration resistor, the transconductance value is attenuated by 91% [2] and therefore we could reduce the on-chip capacitor size of the proposed $G_m$–C filter for low frequency biosensor applications.

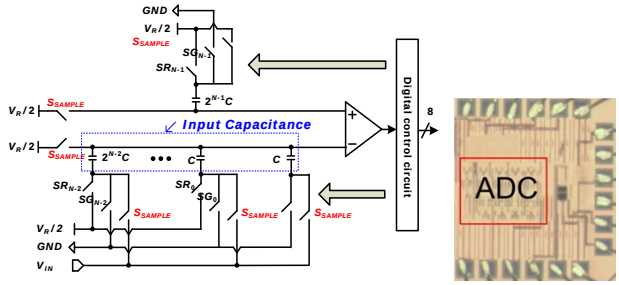


**Figure 2: The schematics (left) and the die micrograph (right) of our proposed SAR ADC with the new switching method.**

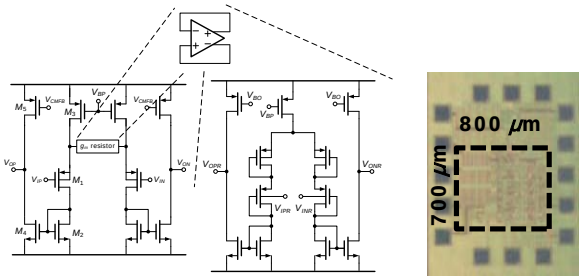


**Figure 3: Left: the schematics of our proposed transconductor with gate-driven input and the bulk-driven $G_m$ cell as the degeneration resistor. Right: the die micrograph of the $G_m$–C filter that utilizes the transconductor shown at left.**

In the 3rd year, the focus will be on improving the integration of the entire AFE IC channel and setting up of the proper test bench for AFE IC characterization. Moreover, the INA is being improved to achieve lower noise, and other circuit blocks such as a switch-capacitor filter is under development for accurate signal-filtering.

**Keywords:** implantable cardioverter defibrillator (ICD), analog front-end (AFE), ultra-low-power sensor.

## INDUSTRY INTERACTIONS

Texas Instruments and IBM

## MAJOR PAPERS/PATENTS

[1] W. Hu *et al.*, "An 8-bit Single-Ended Ultra-Low-Power SAR ADC with a Novel DAC Switching Method," in *Proc. IEEE ISCAS*, pp. 2349-2352, 2012.

[2] Y.-T. Liu *et al.*, "An Ultra-Low-Power CMOS Transconductor Design with Wide Input Linear Range for Biomedical Applications," in *Proc. IEEE ISCAS*, pp. 2211-2214, 2012.

# TASK 1836.066 A FULLY-INTEGRATED CMOS PLATFORM FOR MICROWAVE-BASED LABEL-FREE DNA SENSING

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SAMUEL PALERMO, TEXAS A & M UNIVERSITY

## SIGNIFICANCE AND OBJECTIVES

There are three reasons for sensing chemicals/ biochemicals at microwave frequencies: (1) understanding the effect of wireless signals on human body, food and drugs, (2) Frequency dispersion properties of many materials occur at microwave frequencies, and (3) detecting the static permittivity is possible by extrapolating the measured permittivities at microwave frequencies.

## TECHNICAL APPROACH

The proposed integrated self-sustained sensor is based on capacitive sensing technique in a VCO inside a PLL with considerable improvement in sensitivity. The proposed system eliminates any ADC to enhance the sensitivity. A reference VCO is used along with the sensing VCO to track the frequency changes due to non-systematic drifts. The output is the frequency difference between the two oscillators. A comparator compares the control voltages of the two VCOs to adjust the frequency division value and equate the two control voltages. The frequency shift due to the deposited material is proportional to the difference in division values.

## SUMMARY OF RESULTS

The sensor is fabricated in 90 nm CMOS technology, the microphotograph of the chip is shown in Fig 1.

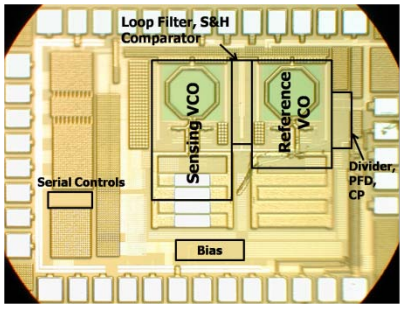


**Figure 1: Microphotograph of the sensing chip.**

The chip consumes around 22mW and the active chip area is around 0.8×0.75 mm$^2$. The sensing VCO frequency range is between 9.65 and 10.21 GHz, and the measured VCO gain is around 650 MHz/V. The PLL locking range in this case is 564 MHz. The reference VCO frequency range is between 10.4 to 11.03 GHz, and the measured VCO gain is around 760 MHz/V. The PLL locking range in this case is 630 MHz. Phase noise measurements of the sensing VCO, measured at the output of the divide by 8 CML dividers is around -110 dBc/Hz at 1 MHz offset. The system noise is measured, by varying the division value and measuring the average comparator output voltage. The curve is then fitted to a cumulative density function, and the value of the variance representing the system noise is extracted to be 15ppm. The sensing platform, including the sensor chip and off-chip peripherals, is then used for chemical sensing of organic liquids and binary mixtures. A plastic tube fixed on top of the sensor chip is used to deposit liquids under test for characterization. The sensing system is calibrated using reference liquids. Sensor's characteristics relating the frequency shift of the synthesizer to the permittivity is extracted. Ethanol-Methanol mixtures with fractional volumes $q$ $(0 \leq q \leq 100\%)$ are applied to the sensor. The frequency shift for each mixture is measured and mapped to a value of permittivity using the sensor's characteristics. Fig. 2 shows the detected value of permittivity of Ethanol-Methanol mixture compared to the theoretical value. A fractional volume accuracy of 1% has been demonstrated.

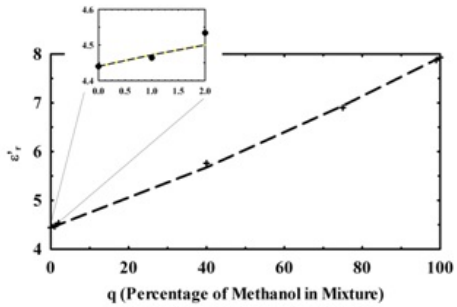


**Figure 2: Permittivity of Ethanol-Methanol mixture vs. fractional volume compared to theoretical values.**

**Keywords:** biosensor, chemical sensor, frequency synthesizer

## INDUSTRY INTERACTIONS

Intel

## MAJOR PAPERS/PATENTS

[1] "A Highly Sensitive Integrated Microwave ChemicalSensor Using a Fractional-N Frequency Synthesizer", IEEE Transactions on Microwave Theory and Techniques (under preparation).

# TASK 1836.071 DESIGN OF PHOTOVOLTAIC (PV) POWER HARVESTING CMOS ICS

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## SIGNIFICANCE AND OBJECTIVES

Energy autonomous ICs that can harvest energy from the environment are an enabling technology for autonomous sensors. The existing integrated energy harvesting systems generally require off-chip transducer elements that cannot be monolithically integrated using CMOS. We plan to create Standard CMOS-embedded photovoltaic (PV) cells, as energy harvesters, and demonstrate their applicability in biomedical implantable sensor devices.

## TECHNICAL APPROACH

To create CMOS PV energy harvesting system, we take advantage of the existing photodiodes of the CMOS process. P+/Nwell diodes are the optimal choice, since they have floating anodes and cathodes. Initially, we designed, fabricated and characterized the CMOS PV cells and evaluate their capabilities and limitations. Currently, we are working on PV cell stacking to increase the voltage as well as PV-riven CMOS sensor design. The ultimate goal is to use these results and enable a fully-integrated PV-driven implantable sensor.

## SUMMARY OF RESULTS

Initially, we designed, fabricated and measured the performance of CMOS PV cells in a 0.18 µm TSMC process. Based on the results shown in Fig. 1 (the responsivity and the I-V characteristics), we concluded that 10's of µW of power can be harvested in ambient light conditions (indoor light) per $mm^2$. This amount of power is quite sufficient for many low power ICs applications. Furthermore, we implemented the CMOS PV cells in an implantable sensor system. As shown in Fig. 2, in this 2.5mm x 2.5mm sub-µW integrated system, an unknown capacitive or resistive parameter is first measured by using a sub-threshold ring oscillator-based sensor, the acquired data is then modulated into a FSK signal, and finally transmitted neuromorphically to the skin surface by using a pair of polarized electrodes. The total area for diode is this is approximately 3.5 $mm^2$. The results of this research have been published [1-2].

**Keywords:** photovoltaic, implanted devices, sensor, CMOS, energy harvesting

## INDUSTRY INTERACTIONS

Texas Instruments, Freescale Semiconductor

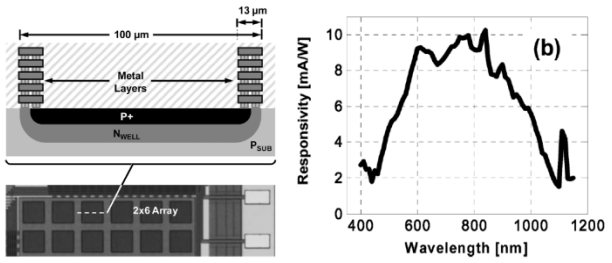


**Figure 1: CMOS PV Cell structure and responsivity.**

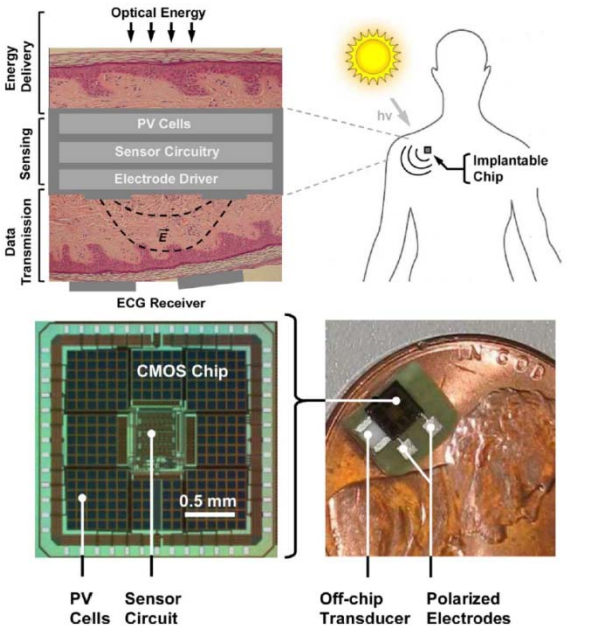


**Figure 2: A photovoltaic-driven energy-autonomous CMOS implantable sensor.**

## MAJOR PAPERS/PATENTS

[1] S. Ayazian, V. A. Akhvan, E. Soenen, and A. Hassibi, "A Photovoltaic-Driven and Energy-Autonomous CMOS Implantable Sensor," IEEE Transactions on Biomedical Circuits and Systems (BIOCAS), 6-4, pp. 336-343, 2012.

[2] S. Ayazian and A. Hassibi, "Delivering Optical Power to Subcutaneous Implanted Devices," International Conference of IEEE Engineering in Medicine and Biology (EMBS), pp. 2874-2877, 2011.

[3] S. Ayazian, E. Soenen, and A. Hassibi, "A Photovoltaic-Driven Energy-Autonomous CMOS Implantable Sensor," IEEE Symposium of VLSI Circuits, pp. 148-149, 2011.

# TASK 1836.103 RECONFIGURABLE BRAIN COMPUTER INTERFACE

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COLLABORATOR: MIKE CHI, UC-SAN DIEGO & COGNIONICS

## SIGNIFICANCE AND OBJECTIVES

The proposed task focuses on creating the next generation dry-contact and non-contact EEG systems for applications of brain computer interface (BCI). We focus on improving the reliability, convenience and wearability of BCI systems. We take a holistic system exploration approach considering the co-design of electrodes, analog front-end and low power DSPs. Our proposed EEG system is capable of self-reconfiguring itself in real-time to maximize the SNR of EEG signals and assuring exceptional reliability for numerous BCI applications.

## TECHNICAL APPROACH

In line with our ultimate objective on enhancing the reliability, convenience and wearability of BCI systems, we focus on 1) electrode design, 2) analog front-end capable of characterizing the coupling between the electrodes and the skin in real-time to improve the CMR and 3) power-optimized signal processing algorithms for applications of BCI to reduce the size of the battery and the overall form-factor of the system. We explore several configurations of electrodes, including dry-contact and non-contact electrodes. We investigate the effects of pin-contact and pin-density on the quality of signals. We test several hypotheses in the terms of the characterizing the skin-coupling using a reference signal injected via the driven right leg (DRL) circuitry. We further implement several BCI algorithms in C and study their memory usage and computational requirements.

## SUMMARY OF RESULTS

We created a base platform for our experimental study using TI ADS1299 (with 8 EEG channels), ARM Cortex-M4, and a laptop. We initialize ADS1299 using I2C via ARM Cortex-M4. Cortex-M4 reads EEG samples (250Hz, 24 bits per sample, gain of one) from ADS1299 and forwards them to the PC via UART. Our next prototype will be wireless incorporating two ADS1299's (16 EEG channels), MSP430 and Bluetooth with a wearable form factor.

We created several configurations of spring-loaded dry-contact electrodes, as shown in Fig. 1. We placed the electrodes on a 10-20 EEG cap and verified the setup in the context of several applications including P300 spell checker and capturing alpha waveforms when eyes are closed. For the sake of brevity, we only report the following finding. Our investigation, as indicated in Fig. 1, shows as the number of pins increases to 20, the quality of (alpha) brain signals degrades. This is due to the less than ideal skin-coupling of some pins. Our future research plans include monitoring the signal quality on pins in real-time and removing less-ideal pins.

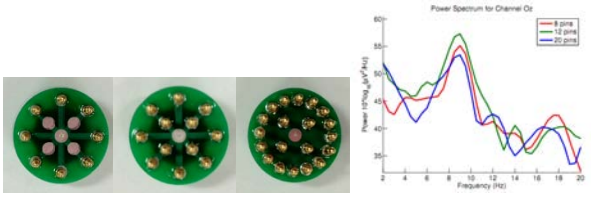



**Figure 1: Spring-loaded dry-contact electrodes with 8, 12 and 20 pins (left to right) and the power amplitude of the brain alpha waves (approx. 8 Hz) captured from Oz location with the electrodes.**

We designed a circuit that injects a reference signal over the DRL, with active feedback loop to the reference electrode. Our proposed circuit incorporates several single-ended positive electrodes, intended for capturing EEG signals. The injected reference signal will not appear on any positive electrodes if the skin-coupling of the reference and the positive electrodes are matching. However, in case of a mismatch, we will observe the reference signal on positive electrodes. The amplitude and the frequency of reference signal will provide cues to characterize the skin-coupling, remove the electrodes (or contacts) with poor skin-coupling and normalize the signals in DSP prior to signal processing. Fig. 2 shows ECG signals for good and loose contacts when the reference signal is present. The jitter on the right diagram corresponds to the injected reference signal.

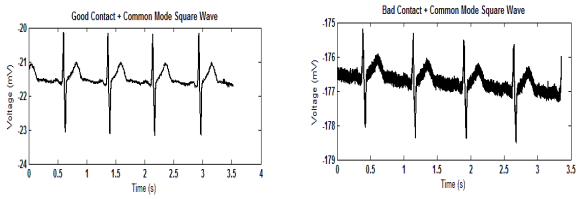



**Figure 2: Measured ECG signals with our reference signal injected over DRL for good (left) and loose (right) contacts.**

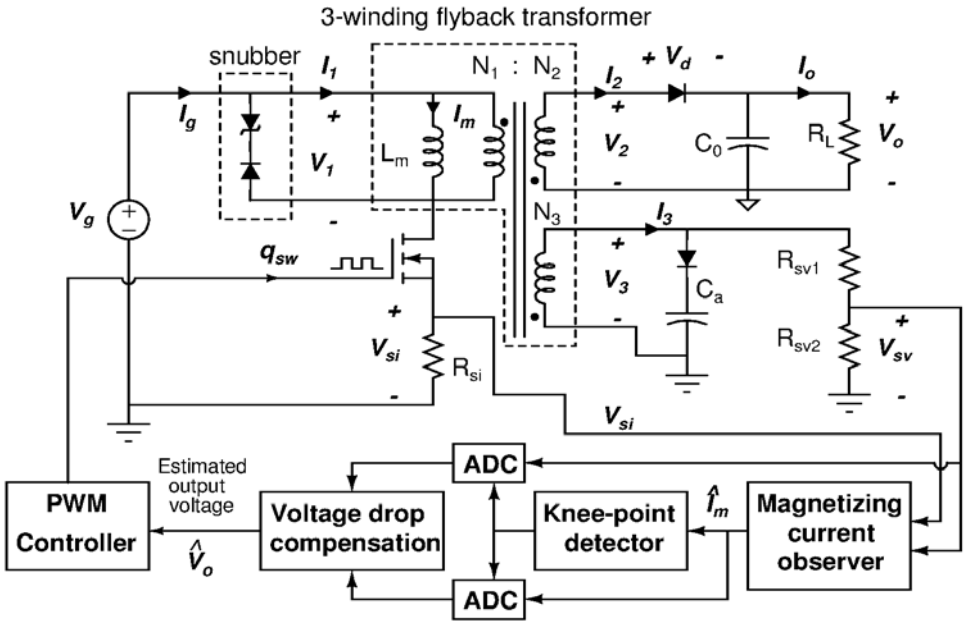
We implemented an extensive set of BCI signal processing algorithms in C and tested their performance on several architectures using SimpleScalar. We are exploring the memory usage and the computational requirements of the algorithms that can be used to design low-power DSPs for BCI.

**Keywords:** brain computer interface, bio-potentials, EEG, low-power processing, dry-contact electrodes

## INDUSTRY INTERACTIONS

Texas Instruments, Intel

# Energy Efficiency Thrust




## Summary of Accomplishments

| Category | Accomplishment |
|---|---|
| Energy Efficiency | Given the advantages of the primary-side sensing control for flyback converters in discontinuous conduction mode, this project is aimed at demonstrating a unified primary-side sensing solution that can work smoothly in both continuous and discontinuous conduction modes (CCM and DCM). The proposed method is highly reliant on the transformer model. The project developed a high frequency model of a flyback transformer, using a time domain system identification method. The transformer model can accurately predict the high frequency response from 500Hz – 15MHz.<br><br>Publications: (1) T. T. Vu, S. O'Driscol, and J. V. Ringwood, "3-winding flyback transformer model extraction using time-domain system identification", Proc. IEEE SPEEDAM, Italy, June 2012. (2) T. T. Vu, S. O'Driscol, and J. V. Ringwood, "Primary-side sensing for a flyback converter in both continuous and discontinuous conduction mode", Proc. Irish Signal and System conference, Maynooth, June 2012.<br><br>(1836.070, PI: J. Ringwood, National University of Ireland-MayNooth) |

| | |
|---|---|
| Energy Efficiency | A fully integrated combined inductive/capacitive converter was designed. The switched inductive converter utilizes a fixed frequency digital PWM controller. The switch size of the PMOS and NMOS power switch can be manually varied depending on the required load current and the frequency of operation of the ADC and the accumulator can also be varied to reduce wasteful power. The capacitive converter is a single mode (IPO-OPG) 2-phase interleaved design with a single mode hysteretic controller. A state machine depending on the reference voltage selects the appropriate converter by gating off the clock to the other converter. This research pioneers the study of a compensated voltage regulation jointly achieved by an inductive switching converter and a SC power converter. The fully on-chip integration of both converters makes its form factor extremely attractive.<br><br>Publications: (1) S. S. Kudva and R. Harjani, "Fully integrated on-chip DC-DC converter with a 450x output range," IEEE Custom Integrated Circuits Conference, September 2010. (2) S. S. Kudva and R. Harjani, "Fully integrated on-chip DC-DC converter with a 450x output range," (Invited) IEEE Journal of Solid-State Circuits, August 2011. (3) S. S. Kudva and R. Harjani, "Fully integrated capacitive converter with all digital ripple mitigation," IEEE Custom Integrated Circuits Conference, September 2012.<br><br>(1836.081, PI: R. Harjani, University of Minnesota) |
| Energy Efficiency | An entropy-based analysis method has been developed to reduce the number of reset circuits required to eliminate the global convergence problem. For a PLL, the number of reset circuits was reduced from 81 to 6.<br><br>Publications: (1) S. Youn, J. Kim, M. Horowitz, "Global Convergence Analysis of Mixed-Signal Systems," ACM/IEEE Design Automation Conference (DAC), June 2011. (2) S. Youn, J. Kim, M. Horowitz, "Preventing Global Convergence Failures in Mixed-Signal Systems by Eliminating Indeterminate States," Frontiers in Analog Circuit Synthesis and Verification (FAC), July 2011. (3) S. Youn, J. Kim, "Preventing Global Convergence Failures in Mixed-Signal Systems via Indeterminate State ('X') Elimination," in review, IEEE Trans. Circuits and Systems-I, 2012.<br><br>(1836.068, PI: J. Kim, Seoul National University) |

# TASK 1836.019 DIGITALLY ENHANCED ENERGY-EFFICIENT HIGH-SPEED I/O LINKS

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## SIGNIFICANCE AND OBJECTIVES

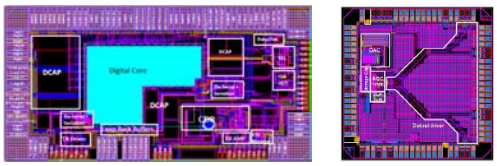
Design of high-speed and low-power analog mixed-signal circuits in nanoscale CMOS is made challenging due to a number of issues such as reduced supply voltage. These problems are exemplified in multi-Gb/s I/O links, whose prevalence in modern electronic systems motivates us to seek cost-effective solutions.

## TECHNICAL APPROACH

The goal of this project is to exploit the capability of DSP and ECC to reduce power and enhance ESD resiliency in high-speed I/O links. I/O link specific ECC will be explored in terms of BER, latency, encoder and decoder architectures. BER-optimal rather than SFDR-optimal ADC architectures will be developed. An ESD-protected multi-Gb/s I/O link embodying some of these ideas will be implemented.

## SUMMARY OF RESULTS

We have demonstrated the benefits of our systems-assisted approach via both analytical studies and two IC prototypes (see Fig. 1), demonstrating the energy benefits of ECC and BER-optimal ADCs, respectively, in I/O links. Over the past year, we have completed the testing of the ECC-based 4Gb/s I/O link (Fig. 1(a)), and are presently testing the 4 GS/s, 4b BER optimal ADC (Fig. 1(b)).



(a) (b)

**Figure 1: Prototype ICs all in 90nm: (a) 4 Gb/s ECC-based I/O trans. [1], and (b) 4Gb/s 4b BER-opt. ADC.**

The ECC-based I/O transceiver was tested over two channels, a high loss channel with 18.2 dB loss at Nyquist, and a channel with a sub-Nyquist notch was studied. The 4 Gb/s line rate transceiver in 90nm CMOS [1] is designed with short block length BCH codes. Measurement results demonstrate that FEC is beneficial by improving reliability for low signal swings, increasing maximum achievable information rate, or reducing inner transceiver energy consumption. Across the high loss channel, ECC shows a 45× reduction in the BER (see Fig. 2).

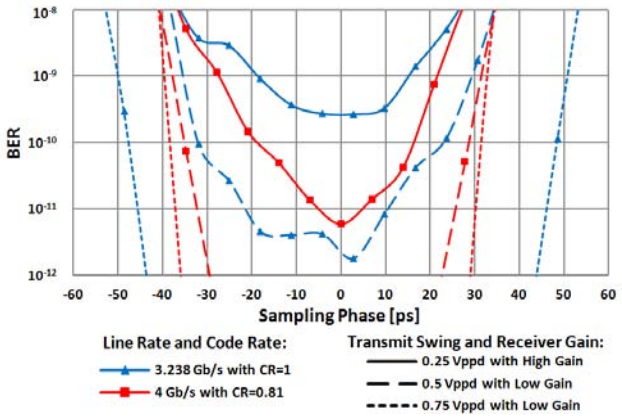



**Figure 2: Measured BER for a fixed information rate of 3.238 Gb/s.**

Across the sub-Nyquist notch channel, ECC is shown to increase the maximum achievable information rate by 27% while reducing the inner transceiver and codec energy consumption by 20%.

For ADC-based high-speed I/O links, we have shown via simulations in a 20-in FR4 10-Gb/s link: 1) the ADC shaping gain is > 30dB at a BER=$10^{-15}$ for a 3-b ADC, and 2) a 3-b BER optimal ADC gives $10^6$X reduction in BER over a 4-b conventional ADC at an SNR of 32 dB. This corresponds to a power savings of 50% in the ADC. A 4b, 4GS/s ADC prototype IC in 90nm was taped-out in June 2011. We will report the complete test results of a 4-b BER-aware ADC for a 4 Gb/s I/O link in a 90nm CMOS process (Fig. 1(b)) later in the year.

**Keywords:** high-speed I/O, DSP, ESD, ECC, low-power

## INDUSTRY INTERACTIONS

Texas Instruments, Intel, AMD, IBM.

## MAJOR PAPERS/PATENTS

[1] A. C. Faust, R. L. Narasimha, K. Bhatia, A. Srivastava, C. Kong, H.-M. Bae, E. Rosenbaum, and N. Shanbhag, "FEC-based 4 Gb/s Backplane Transceiver in 90nm CMOS," IEEE Custom Integrated Circuits Conference (CICC), Sept. 9-12, 2012, San Jose, Calif.

# TASK 1836.053 HIGH-EFFICIENCY HIGHLY-INTEGRATED LED DRIVER SYSTEMS FOR SOLID-STATE LIGHTING APPLICATIONS

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## SIGNIFICANCE AND OBJECTIVES

Solid-state lighting using LEDs are attractive for general lighting due to benefits of longer lifetime, higher efficiency and higher luminous efficacy over the conventional incandescent, halogen and fluorescent lamps. However, the ultimate hurdle of using LED lighting is the cost factor and an essential part of the cost is related to the LED driver system. This project aims to investigate effective methods to miniaturize the LED driver system for low cost consideration, as well as to improve the current accuracy and power efficiency of the LED driver under different conditions.

## TECHNICAL APPROACH

In order to preserve high accuracy of the LED current without using a large-value electrolytic output capacitor, a time-to-digital controller (TDC) is developed to minimize the current error under large variations of input and output voltages. The TDC does not require calibration, thus enabling the LED current to achieve fast settling time.

Without using the large-value electrolytic capacitor, both the reliability and the board size of the LED driver are significantly improved.

A low-power gate driver is developed. The proposed gate driver enables the use of synchronous rectification power stage under high input voltage condition. This addresses the issue of large conduction power loss caused by the low-side power diode. The power efficiency of the LED driver can thus be significantly increased.

## SUMMARY OF RESULTS

The proposed LED driver was implemented in a high-voltage 0.35-µm CMOS for performance verifications. Fig. 1 shows the micrograph of the proposed driver and its chip area is 3.5 $mm^2$ including pads. Our measurement results show that the proposed driver can drive 1 – 10 series-connected LEDs with small LED current variation of <±2% when delivering an average LED current of 350 mA. The proposed LED driver can achieve a peak power efficiency of >90% with the switching frequency of around 1 MHz. Since the proposed TDC does not require any calibration time, fast settling time (10.7 µs) of the LED current is achieved in the proposed LED driver as shown in Fig. 2. The settling time has over 10x improvement over that of state-of-the-art LED drivers.

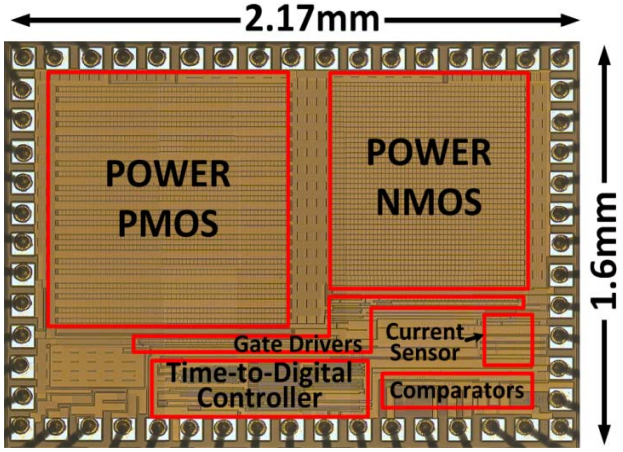


**Figure 1: Micrograph of the proposed LED driver realized by a high-voltage 0.35-µm CMOS.**

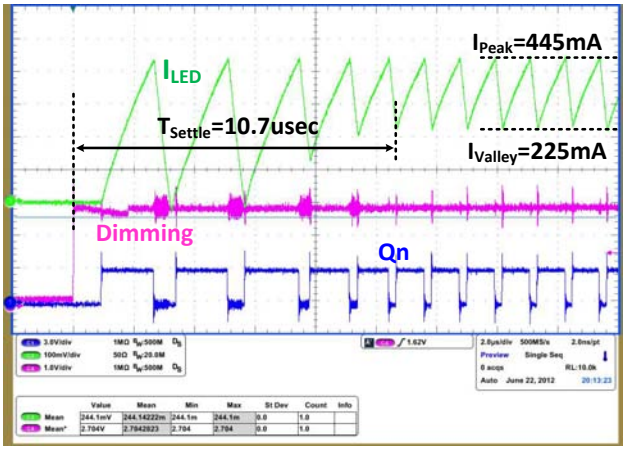


**Figure 2: Measured LED current and gate voltage of power transistor during startup. (Load: 5 series-connected LEDs)**

**Keywords:** LED Driver, solid-state lighting time-to-digital control

## INDUSTRY INTERACTIONS

Texas Instruments and Freescale

## MAJOR PAPERS/PATENTS

[1] D. Park and H. Lee, "A High-efficiency output-capacitor-less integrated LED driver with time-to-digital control for solid-state lighting applications," *SRC TECHCON*, Sept. 2012, Austin, Texas.

[2] D. Park and H. Lee, "Floating buck LED driver with timing difference compensation scheme," *UTD Invention Disclosure.*

# TASK 1836.060 DESIGN TECHNIQUES FOR SCALABLE, SUB-1MW/GBPS SERIAL I/O TRANSCEIVERS

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PATRICK CHIANG, OREGON STATE UNIVERSITY

## SIGNIFICANCE AND OBJECTIVES

Interface architectures which allow for high data rates at improved power efficiency levels are required to satisfy the growing I/O bandwidth in power-constrained environments. This project aims to improve the power efficiency of serial I/O transceivers to sub 1mW/Gbps for data rates ranging from 5-10Gbps.

## TECHNICAL APPROACH

The project utilizes a source-synchronous architecture with ultra-low-power driver, receiver, and clocking circuits that operate over a wide range of supply voltages. The key design techniques developed in this work include:

- Supply-scalable circuits to enable dynamic power management
- A hybrid voltage-mode driver with low-complexity, high-resolution current-mode equalization
- High multiplexing factor transmitter and receiver architectures capable of "near-threshold" operation
- Novel injection-locked ring oscillator de-skew with low bandwidth CDR for compensation of thermal drift and multi-phase static timing offsets.

## SUMMARY OF RESULTS

Fig. 1 shows a schematic of a hybrid driver developed in this work which combines the low output current levels of a voltage-mode driver to implement the main tap and a parallel current-mode driver to implement the post-cursor tap with minimal pre-driver complexity [1]. This implementation improves driver energy efficiency by eliminating any voltage-mode driver segmentation, as the equalization coefficient is set via the current-mode driver tail current DAC setting.

The transmitter was fabricated in an LP 90nm CMOS process, with a total active area of 250µm x 140µm. The transmitter transient performance at 4.8Gb/s data rate is verified in the $2^{15}$-1 PRBS eye diagrams with operation over a channel with 6dB loss at 2.4GHz, shown in Fig. 2(b). Improvement is achieved in both eye height, 87mV to 146mV, and eye width, 123ps to 150ps.

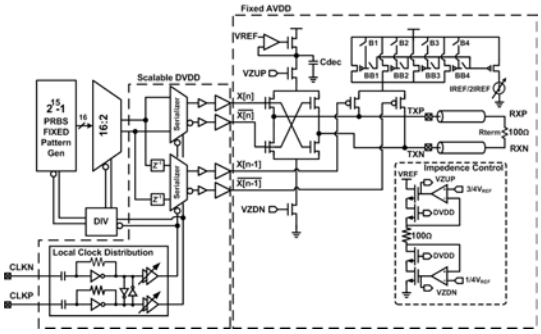
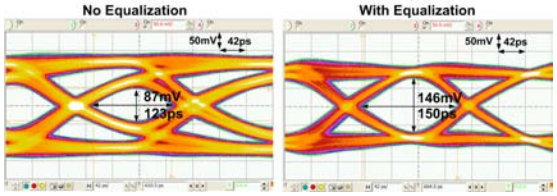



Figure 1: Voltage-mode TX with current-mode equalization [1].




(b)

Figure 2: 4.8Gb/s TX eye diagrams [1].

A source-synchronous link architecture [2] which utilizes supply scaling and high multiplexing factor transmitter and receiver architectures for near-threshold operation has also been implemented in a GP 65nm process. A 1:10 input de-multiplexing version of the receiver, which utilized super-harmonic injection-locking de-skew and operated at 0.6V, achieved 8Gb/s at 0.16-0.25pJ/bit [3, 4]. A full transceiver has been implemented with a 4:1 output multiplexing voltage-mode transmitter and a 1:8 input de-multiplexing receiver which achieves 0.47-0.66pJ/bit from 4.8-8Gb/s [5].

**Keywords:** High-speed I/O, injection-locked oscillator, transmit equalization, voltage-mode driver.

## INDUSTRY INTERACTIONS

IBM, Intel, Texas Instruments

## MAJOR PAPERS/PATENTS

[1] Y.-H. Song and S. Palermo, "A 6Gb/s Hybrid Voltage-Mode Transmitter with Current-Mode Equalization in 90nm CMOS," Accepted in IEEE TCAS-II.

[2] A. Ragab et. al., "Receiver Jitter Tracking Characteristics in High-Speed Source Synchronous Links," Journal of Electrical and Computer Engineering, 2011.

[3] K. Hu et. al., "Low-Power 8Gb/s Near-Threshold Serial Link Receivers Using Super-Harmonic Injection Locking in 65nm CMOS," IEEE CICC, Sept. 2011.

[4] K. Hu et. al., "0.16-0.25pJ/bit, 8Gb/s Near-Threshold Serial Link Receiver With Super-Harmonic Injection-Locking," IEEE JSSC, Aug. 2012.

[5] Y.-H. Song et. al., "A Near-Threshold, 0.47-0.66pJ/bit, 4.8-8Gb/s I/O Transceiver in 65nm-CMOS," submitted to IEEE Journal of Solid-State Circuits.

# TASK 1836.062 SYSTEM-LEVEL MODELS AND DESIGN OF POWER DELIVERY NETWORKS WITH ON-CHIP VOLTAGE REGULATORS

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## SIGNIFICANCE AND OBJECTIVES

The design of power delivery networks (PDNs) is a key avenue and a challenge for achieving power efficiency. We develop simulation tools, models and holistic system design strategies to achieve the optimal system performance trade-offs, and facilitate joint design optimization of active voltage regulators, converters, and passive on-die power grids.

## TECHNICAL APPROACH

One of the key focuses of this work is to optimize power delivery by identifying, analyzing and leveraging opportunities that involve with joint optimization of active regulator/converter circuits and passive distribution sub-networks. We are building simulation capability, system-oriented design models, and optimization-based design methodologies to enable efficient design space exploration for large PDNs with multiple integrated voltage regulators. This holistic design approach will shed new insights on interactions between key components of modern power delivery networks and help achieve the best system-level design tradeoffs between supply noise, power efficiency, area overhead and stability.

## SUMMARY OF RESULTS

A good understanding of complex interactions between various components of a PDN such as on-chip power grids, linear low-dropout voltage regulators (LDOs) and switching converters is essential for optimizing power supply noise, power efficiency, area overhead, stability and the tradeoffs thereof. Through design analysis, several important joint-design opportunities have been identified, which have been subsequently reflected in a simulation-driven optimization based design methodology. The methodology leverages the fast GPU-based simulation engine we developed and is able to perform system design optimization for PDNs with tens of millions of nodes and hundreds of active regulator components. Decap-only, LDO-only, joint decap and LDO as well as joint decap, LDO and buck converter optimizations are contrasted for a large PDN in Fig. 1 and Fig. 2. It can be seen that joint optimizations offer significant improvements on area, power efficiency and ground (quiescent) power, signifying the benefits of holistic system design.

A set of design-oriented implied symbolic models have also been initially investigated. These models may allow the designers to perform early-stage design exploration. In addition, a theoretically rigorous stability checking technique has been proposed to allow feasible localized stability assurance of PDNs with multiple active regulators.

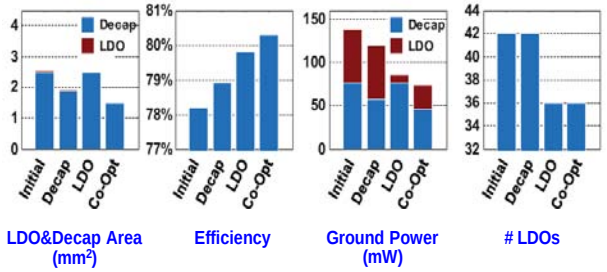


**Figure 1: PDN system optimization: decap-only optimization, LDO-only optimization, LDO/decap co-optimization.**

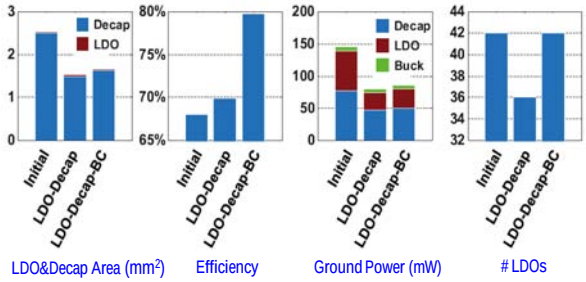


**Figure 2: PDN system optimization: LDO/decap co-optimization vs. LDO/decap/bulk converter co-optimization.**

In the coming year, we will continue our work on localized stability assurance for large PDNs with multiple active voltage regulators. We will also perform system-level modeling and design tradeoff analysis for PDN designs with aggressive power management.

**Keywords:** power delivery, on-chip voltage regulation, power supply noise, power efficiency, co-optimization

## INDUSTRY INTERACTIONS

Freescale, Intel, AMD, IBM

## MAJOR PAPERS/PATENTS

[1] S. Lai, B. Yan, P. Li, "Stability assurance and design optimization of large PDNs with multiple on-chip LDOs," Accepted to IEEE/ACM ICCAD, 2012 (SRC disclosure).

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# TASK 1836.063 POWERLINE COMMUNICATIONS FOR ENABLING SMART GRID APPLICATIONS

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## SIGNIFICANCE AND OBJECTIVES

Within a smart grid, we seek to enable higher data rate monitoring and controlling applications for making homes and small businesses more efficient in their use of energy. We focus on narrowband powerline communication systems operating in 3-500 kHz band delivering data rates up to 800 kHz over medium-voltage and low-voltage power lines.

## TECHNICAL APPROACH

Non-Gaussian noise and interference are among the primary impairments that limit the performance of narrowband PLC systems. Based on field measurement, we propose statistical models for two dominant categories of powerline noise: cyclostationary noise and impulsive noise. We propose learning-based algorithms to mitigate cyclostationary noise and impulsive noise in Orthogonal Frequency-Division Multiplexing (OFDM) PLC systems. To evaluate the proposed algorithms in performance vs. complexity tradeoffs, we implemented a single-transmitter single-receiver PLC testbed. The methods and prototype is currently being extended to a two-transmitter two-receiver system, exploiting the diversity from three phases on low-voltage lines and three copper wires in the inhome power systems.

## SUMMARY OF RESULTS

We propose a novel cyclostationary noise model that captures the periodic variation of noise statistics in both time and frequency domain (Figure 1). The model has been accepted into IEEE P1901.2 narrowband PLC standard.

We derive statistical-physical models for impulsive noise in PLC. We apply sparse Bayesian learning nonparametric techniques to estimate and mitigate impulsive noise in OFDM PLC systems without the need for training. In our simulations, the estimators achieve 5dB and 10dB SNR gains in communication performance respectively, compared to conventional OFDM receivers.

We implement a single-transmitter single-receiver (1x1) OFDM PLC testbed. It includes a software package running transceiver algorithms on National Instruments (NI) embedded computers, and an analog front-end (AFE) interface connecting the NI hardware with Texas Instruments PLC AFE. We are currently migrating the 1x1 system into a 2x2 MIMO PLC testbed.

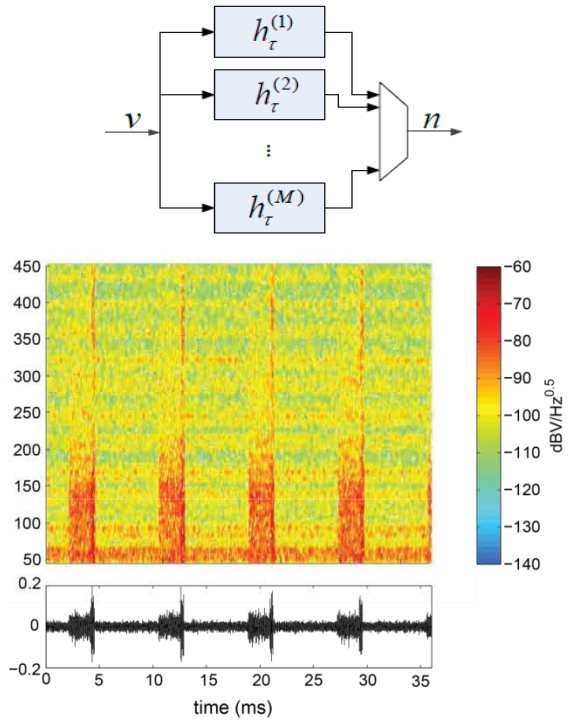


**Figure 1: Proposed cyclostationary noise model for narrowband PLC and the synthesized noise trace.**

**Keywords:** powerline communications, smart grid, cyclostationary noise, impulsive noise, testbed

## INDUSTRY INTERACTIONS

Texas Instruments, Freescale, IBM

## MAJOR PAPERS/PATENTS

[1] M. Nassar et al., "Local Utility Powerline Communications in the 3-500 kHz Band: Channel Impairments, Noise, and Standards", IEEE Sig. Proc. Magazine, 2012.

[2] M. Nassar et al., "Cyclostationary Noise Modeling In Narrowband Powerline Communication For Smart Grid Applications", IEEE ICASSP 2012.

[3] M. Nassar et al., "Statistical Modeling of Asynchronous Impulsive Noise in Powerline Communication Networks", IEEE Globecom 2011.

[4] J. Lin et al., "Non-Parametric Impulsive Noise Mitigation in OFDM Systems Using Sparse Bayesian Learning", IEEE Globecom 2011.

# TASK 1836.068 GLOBAL CONVERGENCE ANALYSIS OF MIXED-SIGNAL SYSTEMS

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## SIGNIFICANCE AND OBJECTIVES

Today, many modern mixed-signal systems including oscillators, phase-locked loops, and DC-DC converters suffer from fatal start-up failures due to ill-defined initial states, yet their existence is extremely difficult to detect using brute-force simulation approaches. This task aims to find practical tools and methodologies to prevent such global convergence failures.

## TECHNICAL APPROACH

This task seeks practical methods or tools rather than a rigorous mathematic proofing tool to establish the global convergence of a general, large-scale mixed-signal system.

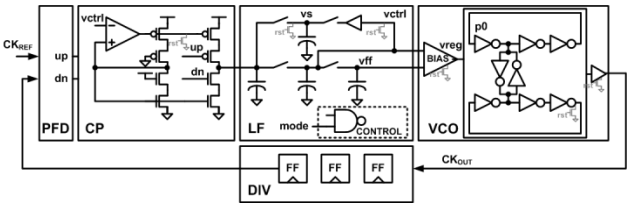
So far, the task has addressed the problem mainly in two directions: (1) a simulation-based analysis that can detect the existence of global convergence failures; and (2) a methodology or design flow that can effectively prevent the occurrence of these failures. For instance, the cluster split detection algorithm looks for an initial state that can lead to a false convergence [1] and the indeterminate state ('X') elimination algorithm guides the designers where to add resets by extending the notion of 'X' in digital to analog circuits [1-3]. One of the key objectives is to minimize the computational costs of these algorithms, especially when handling large-scale mixed-signal systems.

## SUMMARY OF RESULTS

The initial 'X' elimination algorithm developed in the first year had a problem of reporting too many X's in the system and hence requiring too many reset circuits. Among them, quite a few are unnecessary as they are resetting floating but isolated nodes that never influence the circuit's operation or the nodes that are strongly driven by other nodes.

The more elaborate entropy-based analysis method has been developed to identify the former type of nodes as *isolated X*'s while the latter as *dependent X*'s. And using this information, the revised 'X' elimination algorithm does not suggest the addition of reset circuits to these nodes.

Figure 1 illustrates the effectiveness of the revised algorithm with a phase-locked loop example that has a global convergence failure (that is, it does not reach the correct lock when initialized improperly). Compared to 81 resets suggested by the initial algorithm, the revised algorithm suggests that only 6 resets are enough to suppress the global convergence failures.




| After 1st iteration | | | After 2nd iteration | | |
|---|---|---|---|---|---|
| Nodes | $H(A_t\|A_0)/H(A_t)$ | H(A) | Nodes | $H(A_t\|A_0)/H(A_t)$ | H(A) |
| vctrl | 0.27 | 2.7 | vs | 0.11 | 1.8 |
| vs | 0.38 | 2.2 | nodes in VCO | 0.56~1.0 | 0.56~2.8 |
| nodes in CP | 0.66~0.97 | 0.33~1.7 | nodes in CP | 0.58~0.99 | 0.38~1.6 |
| nodes in PFD | 0.71~0.91 | 0.41~2.0 | other nodes in LF | 0.66~0.99 | 0.74~2.1 |
| other nodes in LF | 0.75~0.98 | 1.4~2.6 | nodes in PFD | 0.84~0.94 | 0.74~2.0 |
| nodes in DIV | 0.84~0.89 | 1.4~2.5 | nodes in DIV | 0.85~0.95 | 1.2~2.0 |
| nodes in VCO | 0.87~1.0 | 0.98~2.9 | | | |

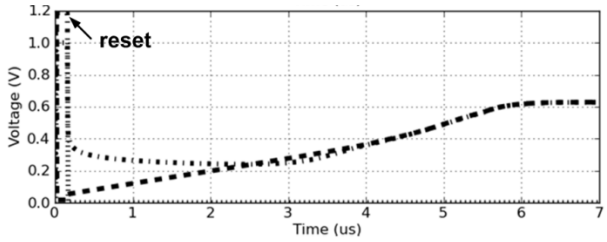



**Figure 1: An example phase-locked loop (PLL) with a global convergence failure (top), the entropy analysis identifying independent X's, isolated X's and dependent X's (middle) and the simulation trajectories with different initial states after adding the reset circuits suggested by the algorithm (bottom); the global convergence failure is prevented.**

**Keywords:** global convergence, start-up failures, mixed-signal systems, circuit simulation, formal analysis.

## INDUSTRY INTERACTIONS

Texas Instruments, Inc. and Intel Corp.

## MAJOR PAPERS/PATENTS

[1] S. Youn, J. Kim, M. Horowitz, "Global Convergence Analysis of Mixed-Signal Systems," ACM/IEEE Design Automation Conference (DAC), June 2011.

[2] S. Youn, J. Kim, M. Horowitz, "Preventing Global Convergence Failures in Mixed-Signal Systems by Eliminating Indeterminate States," Frontiers in Analog Circuit Synthesis and Verification (FAC), July 2011.

[3] S. Youn, J. Kim, "Preventing Global Convergence Failures in Mixed-Signal Systems via Indeterminate State ('X') Elimination," in review, IEEE Trans. Circuits and Systems-I, 2012.

# TASK 1836.069 ELECTRONIC SYSTEMS FOR SMALL-SCALE WIND TURBINES

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## SIGNIFICANCE AND OBJECTIVES

Wind power is an attractive renewable energy resource. This project focuses on improving the performance of domestic-scale wind turbines. A wind turbine emulator rig has been established to simulate static and dynamic situation of wind turbines under different wind speed conditions.

## TECHNICAL APPROACH

Based on the emulator system established last year, encoder-less control algorithm has been devised to achieve maximum power extraction. The estimation of generator speed was realized by measuring the current and voltage of the generator. By comparing the change in rotor speed and power, the generator was controlled to operate at the speed where maximum power is extracted at different wind speed conditions. A single phase full bridge inverter converted the DC voltage into a single phase sinusoidal voltage with constant amplitude and constant frequency for the load.

## SUMMARY OF RESULTS

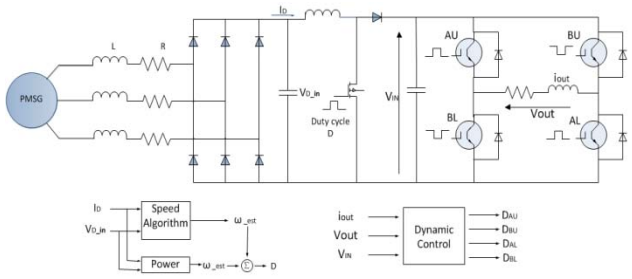



**Figure 1: Power conversion system and control strategy.**

Figure 1 shows the power conversion system and the control strategy used to control the permanent magnet synchronous generator (PMSG).

The rotor speed is estimated by measuring the output current and voltage of the rectifier. The generator is controlled to operate at optimal speed so that most wind power can be extracted. As shown in Figure 2, comparing the change in speed and power, further change in speed can be decided and it is realized by controlling the state of the switch in boost converter. The voltage is then converted to single phase AC to the load.

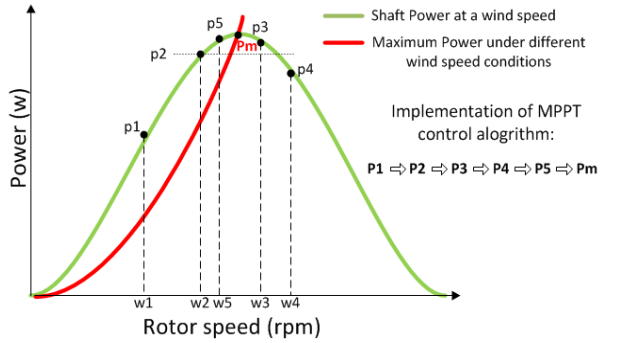
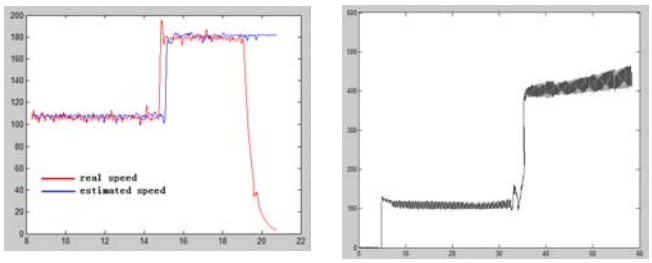



**Figure 2: Rotor speed vs. shaft power and maximum power track.**




(a) (b)

**Figure 3: (a) Real and estimated speed, (b) Extracted power.**

The experiment result in Figure 2(a) demonstrates comparison of real speed and the estimated speed (rpm) obtained from algorithm. Figure 2(b) illustrated the extracted power (watt) with change in wind speed.

In the third year of the project, the investigation of grid integration will be added into the encoder-less control algorithm. Moreover, system commercialization for TI will be investigated.

**Keywords:** renewable, encoderless, MPPT, PMSG, small wind

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] R.Esmaili, L. Xu, *"A New Method of Permanent Magnet Generator for Maximum Power Tracking in Wind Turbine Application,"* 2005, IEEE.

[2] A. Samosir, A.Yatim, *"Dynamic Evolution Controller for Single Phase Inverter Application."* 2009, IEEE Symposium on Industrial Electronics and Applications.

# TASK 1836.070 OPTIMUM CONTROL OF POWER CONVERTERS

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## SIGNIFICANCE AND OBJECTIVES

Given the advantages of the primary-side sensing control for flyback converters in discontinuous conduction mode, this project is aimed at proposing a unified primary-side sensing solution that can work smoothly in both continuous and discontinuous conduction mode (CCM and DCM). The proposed method is highly reliant on the transformer model.

## TECHNICAL APPROACH

The accuracy of primary-side sensing largely depends on the voltage drop at the transformer secondary side, which is a function of parasictic components and the secondary current. To achieve precise output voltage regulation under different working modes, an observer method is proposed to estimate the secondary current and predict the winding voltage drop based on the transformer model. To guarantee an accurate voltage drop prediction, a model of a real flyback transformer is obtained using a system identication technique. The proposed sensing technique is verified by simulation.

## SUMMARY OF RESULTS

For low frequency applications, transformer model extraction has been widely investigated using both time and frequency domain data. However, the studies for high frequency transformers have been carried out in the frequency domain only. The study in [1] presents a methodology to obtain a high frequency transformer model, as shown in Fig. 1, using a time-domain system identification technique. As demonstrating in the paper, the time domain approach can provide a winding model at least as accurate as obtained with the frequency response data.

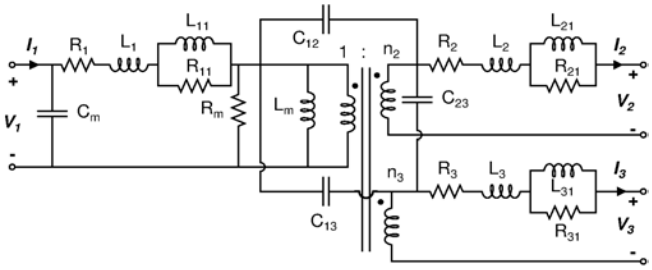


**Figure 1: A full model of a flyback transformer taking into account the frequency dependent effect of leakage inductance.**

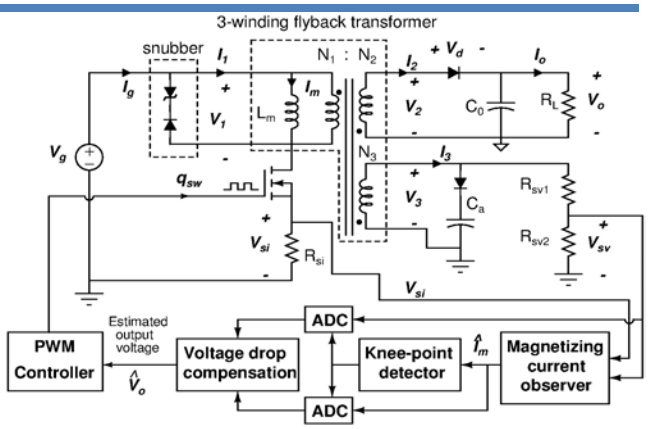


**Figure 2: Circuit diagram of a flyback converter with the proposed primary-side sensing control working in both conduction modes.**

Primary-side sensing for flyback converters in DCM has been widely investigated, however no research has been put into extending this strategy for both CCM and DCM. By considering the possibility to predict the winding voltage drop using the magnetizing current and the transformer model, the study in [2] introduces a unified sensing solution, as depicted in Fig. 2. As shown in the paper, the proposed sensing technique can accurately estimate the output voltage in both CCM and DCM. The sensing algorithm is simple and can be implemented by an analog or digital integrator.

Future work consists of adding a nonlinear core model for the transformer in [1] and performing experimental verifications for the proposed solution in [2].

**Keywords:** Primary-side sensing technique, flyback converter, transformer model, system identification.

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] T. T. Vu, S. O'Driscol, and J. V. Ringwood, "3-winding flyback transformer model extraction using time-domain system identification", Proc. IEEE SPEEDAM, Italy, June 2012.

[2] T. T. Vu, S. O'Driscol, and J. V. Ringwood, "Primary-side sensing for a flyback converter in both continuous and discontinuous conduction mode", Proc. Irish Signal and System conference, Maynooth, June 2012.

# TASK 1836.076 ULTRA-LOW POWER DELAY-INSENSITIVE ASYNCHRONOUS CIRCUITS

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DRS. SCOTT C. SMITH AND H. ALAN MANTOOTH

## SIGNIFICANCE AND OBJECTIVES

Leakage power has become a critical factor for deep submicron digital CMOS ICs. This project will evaluate the integration of MTCMOS power gating with delay-insensitive asynchronous logic for reducing leakage in both active and standby modes, as well as explore the ultra-low voltage asynchronous circuit design opportunity.

## TECHNICAL APPROACH

Since the spacer cycle of a dual-rail delay-insensitive asynchronous component is equivalent to gating the power of this component and forcing the output to logic 0, these circuits can enter sleep mode after every data cycle, while the circuit is in operation, and the handshaking signals between registers can be used as sleep control signals to control the power gating transistors. This approach has several merits: 1) limiting leakage in both active and sleep modes; 2) alleviating the effort and complexity of designing the sleep signal generation mechanism; 3) reducing the area overhead; and 4) facilitating the tool flow development.

## SUMMARY OF RESULTS

Delay-insensitive asynchronous logic like the NULL Convention Logic (NCL) utilizes dual-rail encoding to achieve delay-insensitivity. A NCL system consists of delay-insensitive combinational logic sandwiched between NCL registers, which use handshaking signals to coordinate circuit behavior. NCL circuits are comprised of 27 threshold gates and MTCMOS power gating structure is implemented inside each threshold gate. In order to maintain delay-insensitivity and maximize leakage saving, a series of innovations including early-completion detection, sleep-enabled register and completion detection unit design, have been applied. Incorporating MTCMOS power gating mechanism in NCL (denoted as MTNCL) has the potential to result in significant savings in energy consumption without large overhead in area.

An automated design flow for MTNCL circuits has been developed, as shown in Figure 1. Starting from Boolean RTL code, the design can be synthesized to MTNCL, optimized for performance, verified by commercial tools, and imported into physical-level EDA tools for chip integration.

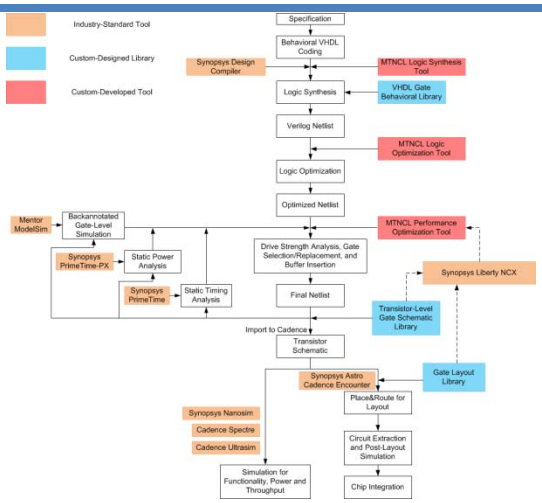


**Figure 1: Automated MTNCL Design Flow.**

Another aspect of the project is to explore the design of asynchronous circuits capable of operating at ultra-low voltages. Figure 2 shows a NCL threshold gate design with Schmitt-trigger structure using IBM 8RF process, which is able to operate reliably at 70mV.

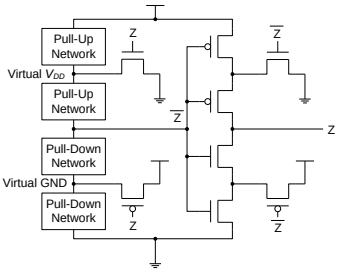


**Figure 2: NCL Threshold Gate Design Incorporating Schmitt-Trigger Structure for Ultra-Low Voltage Operation.**

**Keywords:** MTCMOS, delay-insensitive, asynchronous, ultra-low power, CAD tool

## INDUSTRY INTERACTIONS

Texas Instruments, Intel, IBM

## MAJOR PAPERS/PATENTS

[1] R. Thian, L. Caley, A. Arthurs, B. Hollosi, and J. Di, "An Automated Design Flow Framework for Delay-Insensitive Asynchronous Circuits," 2012 IEEE SoutheastCon, March 2012.

[2] A. Arthurs, J. Roark, and J. Di, "A Comparative Study of Ultra-Low Voltage Digital Circuit Design," International Journal of VLSI Design & Communication Systems, Vol. 3, No. 3, June 2012.

# 1836.081 - COMBINED INDUCTIVE/CAPACITIVE DC-DC CONVERTER

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## SIGNIFICANCE AND OBJECTIVES

This research aims to build highly efficient converters which can support very wide output power range. The main application of such a converter is to power multiple power domains with DVS, demanding fully integrated implementation. Hence, reduction of area occupied by the converter is another goal of this project.

## TECHNICAL APPROACH

A fully integrated combined inductive/capacitive converter was designed. The switched inductive converter utilizes a fixed frequency digital PWM controller. The switch size of the PMOS and NMOS power switch can be manually varied depending on the required load current and the frequency of operation of the ADC and the accumulator can also be varied to reduce wasteful power. The capacitive converter is a single mode (IPO-OPG) 2-phase interleaved design with a single mode hysteretic controller. A state machine depending on the reference voltage selects the appropriate converter by gating off the clock to the other converter.

## SUMMARY OF RESULTS

We have already demonstrated switching inductive fully integrated converter and fully integrated capacitive converter [1][2][3].

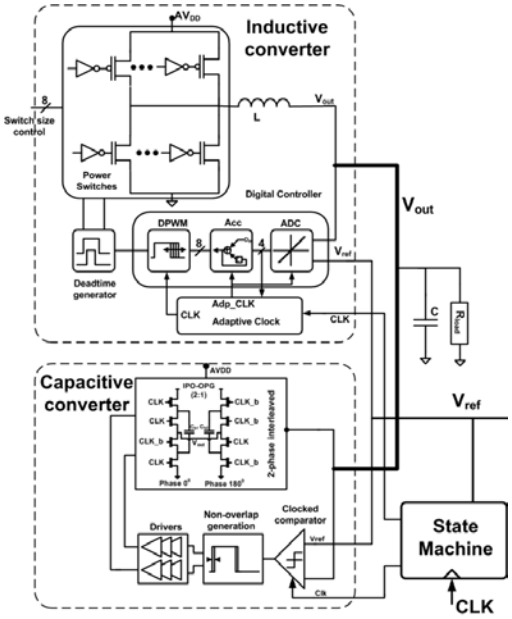


Figure 1: Parallel converter architecture

In this phase of project we have taped out a combined inductive/capacitive converter shown in fig. 1 in IBM 32nm SOI process. The passives both inductor and filter capacitor are integrated on-chip. The inductor is a stacked planar spiral inductor implemented in top two metal layers and achieves an inductance of 2nH with a series resistance of 485mΩ. The filter capacitor was implemented using high density deep trench capacitors to implement a total capacitance of 6.6nF. The layout of the combined converter occupies a total area of 524µmX822µm achieving a power density of 0.7W/mm$^{2.}$

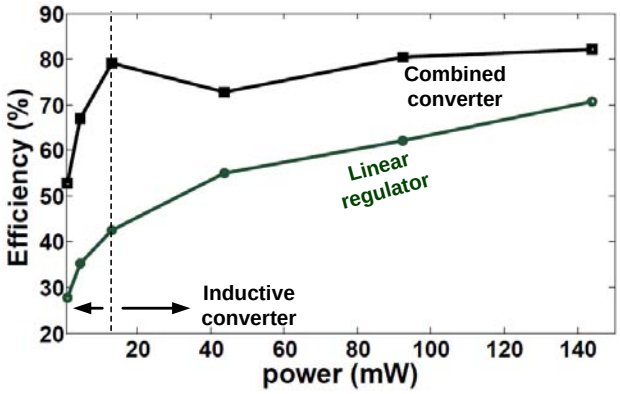


Figure 2: Simulated efficiency of the combined converter architecture

A maximum efficiency of 85.5% is achieved by the inductive converter and 79% by the capacitive converter. Fig. 2 shows the efficiency of the converter for a RO based load with DVS applied. The converter achieves higher efficiency linear regulator at all operating conditions. The efficiency at lower powers can be further improved by implementing additional capacitive converter modes.

**Keywords:** combined converter, switching inductive converter, capacitive converter

## INDUSTRY INTERACTIONS

Intel, IBM, Freescale

## MAJOR PAPERS/PATENTS

[1] S. S. Kudva and R. Harjani, "Fully integrated on-chip DC-DC converter with a 450x output range," IEEE Custom Integrated Circuits Conference, Sept. 2010.

[2] S. S. Kudva and R. Harjani, "Fully integrated on-chip DC-DC converter with a 450x output range," (Invited) IEEE Journal of Solid-State Circuits, Aug. 2011.

[3] S. S. Kudva and R. Harjani, "Fully integrated capacitive converter with all digital ripple mitigation," IEEE Custom Integrated Circuits Conference, Sept. 2012.

# TASK 1836.090 DIGITALLY-ENHANCED CLOCKING STRATEGIES TO IMPROVE ENERGY-EFFICIENCY OF SERIAL LINKS

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## SIGNIFICANCE AND OBJECTIVES

The goal of the proposed research is to explore and invent techniques to improve the energy efficiency of serial links by an order of magnitude. Specifically, this research will focus on co-designing system-level power management schemes with digitally-enhanced clocking circuit architectures to simultaneously achieve low-power operation and robustness to process variability, leakage, and low supply voltage.

## TECHNICAL APPROACH

The technical approach is based on operating the link at an energy-efficient supply voltage and leveraging the link inactivity periods to reduce the power consumption. The specific focus of this effort would be the design of fast locking clock generation circuits. To this end, we seek to employ highly digital circuit architectures that leverage self-calibration to speed up the lock time. In one possible approach the oscillator tuning characteristic is determined and upon power up, appropriate control word is loaded into the oscillator, thus acquiring instantaneous frequency lock.

## SUMMARY OF RESULTS

Phase acquisition time of a phase-locked loop (PLL) is limited by their loop bandwidth which in turn is typically restricted to one-tenth of the reference frequency. For faster phase locking, an injection locked oscillator (ILO) can be utilized (Fig. 1). Phase settling characteristics of ILO are analyzed and simulated (Fig. 2). Due to its limited locking range, an ILO requires a frequency locking loop (FLL) for initial frequency setting. Traditionally in an FLL a delta sigma modulator (DSM) digital to analog converter (DAC) followed by a filter is used to set frequency accurately. However, the settling time of filter becomes the bottleneck in fast frequency acquisition. A FLL loop without DSM DAC filter is proposed. Effect of various design parameters of DSM DAC on the phase noise and jitter are presented (see Fig. 3).

In the following year we seek to further investigate fast-locking clock generator including digital phase- and delay-locked loops and strive to implement a prototype test chip in a deep sub-micron CMOS process.

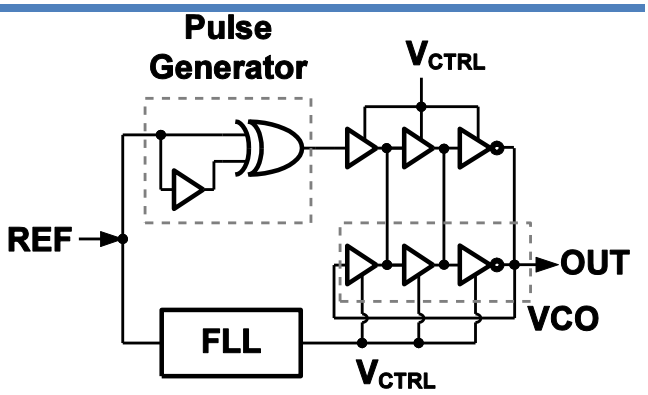


Figure 1: Injection-locked oscillator

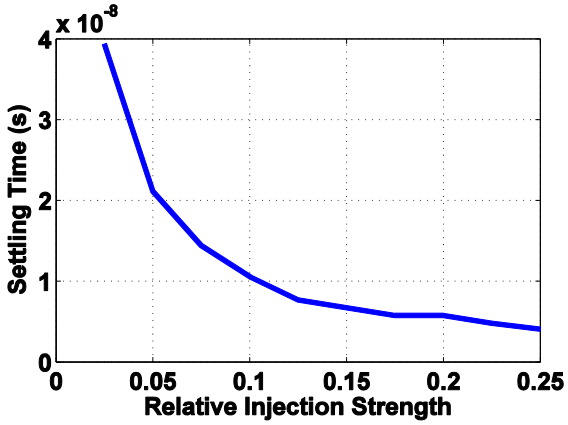


Figure 2: Settling time vs. injection strength of an ILO

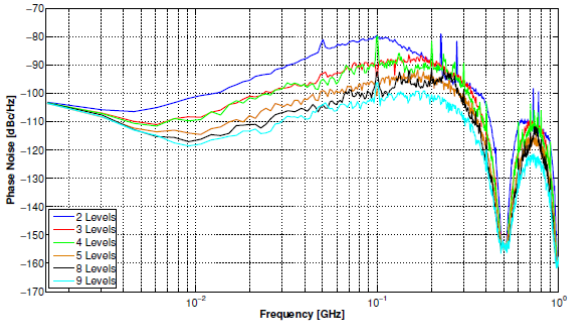


Figure 3: Impact of DSM levels on ILO phase noise

**Keywords:** fast frequency locking, ILO, PLL, FLL

## INDUSTRY INTERACTIONS

IBM, Texas Instruments, Intel

# 1836.104, FAULT TOLERANT INVERTER MODULE FOR DSSRM DRIVE

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## SIGNIFICANCE AND OBJECTIVES

Successful implementation of this technology will allow for satisfactory operation of the double stator switched reluctance motor (DSSRM) in the event of multiple failures in its power semiconductor devices. This will then allow for effective application of this technology in high impact applications such as automotive and military products.

## TECHNICAL APPROACH

Given the fact that fifty percent of the available power switches in DSSRM are not in operation at any given time, this project aims to multiplex the idle parts of the power converter in the event of a fault. This fallback strategy needs to be done concisely and according to the conduction bands of each phase. An electromechanical/mechanical system will physically alter the connections of each phase leg to the desired motor terminals. This needs to be done carefully so there are no residual charges in the power devices at the time of commutation.

## SUMMARY OF RESULTS

The team of investigators has considered two different implementations for this project. In the first approach, a micro-electromechanical actuator is being designed for commutation of the converter phases among various motor terminals. In this approach accurate assessment of timing and the required torque at various speeds have been taken into account. Figure 1 illustrates the general configuration of the system.

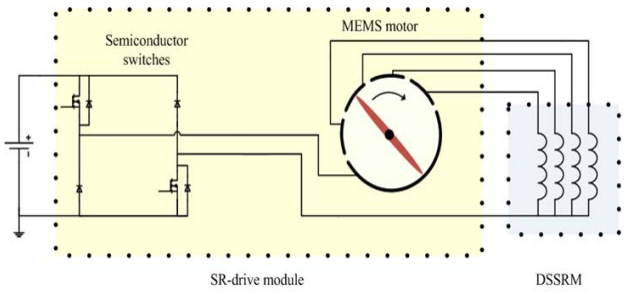


**Figure 1: The architecture for the converter multi-plexer**

In the second approach a mechanical system driven by the shaft of the machine is directly used to accommodate the mechanical commutation of the phases. This system takes advantage of the synchronous nature of the DSSRM drive and can effectively alter the mechanical connections between the inverter and motor terminals. However, the challenge remains on safe commutation by avoiding an interrupt of current. Figure 2 shows the architecture used for the second approach.

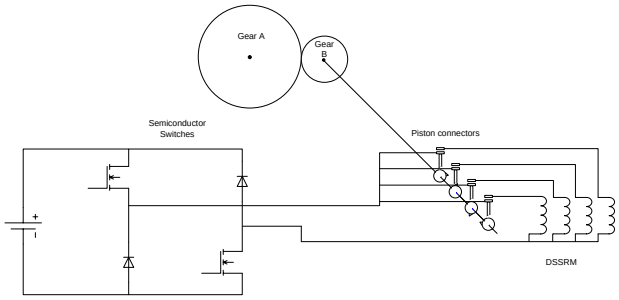


**Figure 2: Mechanical commutation of the phase using DSSRM torque**

These architectures have been conceptually analyzed and circuit models incorporating the analytical model of the DSSRM have been developed to evaluate their capability and potential shortcomings. An experimental prototype of the proposed concepts will be developed in the second year of the project to validate the operation of the system. Details of the system as well as potential applications of the proposed concept in multi-port power electronic interface is being investigated.

**Keywords:** DSSRM, fault tolerance, power converter, high torque, transportation

## INDUSTRY INTERACTIONS

Texas Instruments

# TASK 1836.105 CR-FREE SIMO DC-DC POWER CONVERTERS WITH NANO-SECOND LOAD TRANSIENT RESPONSE

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## SIGNIFICANCE AND OBJECTIVES

The output voltage ripple of modern switching power converters is desired to be low in high-performance systems. Meanwhile, the load transient response and dynamic voltage scaling (DVS) tracking speed are expected to be fast. A switching converter with both improved steady-state and dynamic performances is highly demanded.

## TECHNICAL APPROACH

By using dynamic current compensation (DCC) technique, both the load transient response and DVS tracking speed of switching power converter can be significantly improved without increasing the switching frequency or reducing the filtering inductance. The proposed quasi-single-current-band (quasi-SCB) control method obviates large ESR for filtering capacitor. Therefore, the low output voltage ripple can be achieved simultaneously. The switching frequency is also stabilized to avoid generating randomized switching noise spectrum. Moreover, the high power efficiency is maintained since the load current is dominated by the output current of switching converter in steady state.

## SUMMARY OF RESULTS

A switching power converter with low output voltage ripples and fast load/DVS transient response is proposed, as illustrated in Fig. 1. In the power stage, MOSFET transistors $M_{P1}$ and $M_{N1}$ operate as power switches to charge/discharge the inductor L, thereby delivering the inductor current ($I_L$) to the load. Large inductance is chosen to reduce the current ripples in $I_L$. As the slow transient response and large damping behavior are primarily caused by the instantaneous mismatch between $I_L$ and $I_{load}$, power transistors $M_{P2}$ and $M_{N2}$ are added to provide a dynamic compensation current $I_{DCC}$, together with the proposed dynamic current compensation (DCC) controller. Since $I_{DCC}$ accounts for only a small portion of the total load current (the current ripple of $I_L$), the sizes and power losses associated with $M_{P2}$ and $M_{N2}$ are much smaller than those of $M_{P1}$ and $M_{N1}$. Hence, the degradation on efficiency and silicon penalty are very limited. In addition to the DCC controller, a sensor-free quasi-SCB controller is employed to implement current mode hysteretic control with low ESR. In addition, switching frequency stabilization blocks are adopted to maintain a constant switching frequency, thereby avoiding randomized switching noise spectrum.

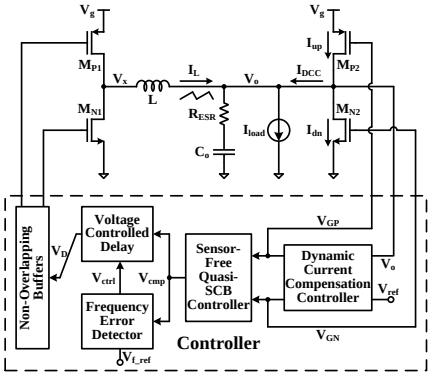


**Figure 1: Block diagram of the proposed switching converter.**

The proposed converter is designed with a TSMC 0.35µm CMOS process. The input voltage can range from 2.7 to 3.3V, while the output voltage can be regulated at any level between 0.5 to 1.8V with a nominal value of 1.5V. The maximum load current is 500mA. The maximum efficiency is 93.73%, measured at a load power of 525mW. It stays above 81.55% over the entire 750mW load range. When $I_{load}$ changes between 50mA and 500mA, the output voltage is recovered within 286.7ns with an overshoot/undershoot voltage less than 23.8mV, which are 153 and 46 times improvement compared with the conventional counterpart. Similarly, for the DVS tracking performance, a 2.672µs/V reference tracking speed is achieved, which is about 15 times improvement compared with conventional counterpart under the same testing condition. The proposed system architecture and control also benefit the steady-state operation. The steady-state output voltage ripple is well limited in different load conditions. The peak-to-peak output voltage ripple is reduced from 33.3 mV to 3.1 mV compared with the conventional counterpart, due to the joint effort of dynamic current compensation and quasi-SCB hysteretic control, which allow the use of low-ESR filtering capacitor.

**Keywords:** dynamic current compensation, quasi-single-current-band hysteretic control, frequency stabilization, low ripple, fast transient.

## INDUSTRY INTERACTIONS

Texas Instruments, Intel, AMD

## MAJOR PAPERS/PATENTS

[1] Y. Zhang and D. Ma, “Integrated Low-Ripple Fast-Transient Switching Power Converter with Dynamic Current Compensation and Sensor-Free Quasi-SCB Hysteretic Control,” APEC 2013 (submitted).

# TASK 1836.106 IF-SAMPLING CMOS ADC FRONT-END WITH 100-DB LINEARITY

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## SIGNIFICANCE AND OBJECTIVES

In order to take advantage of IF-sampling, ADC needs to have larger acquisition bandwidth and high linearity. For IF-sampling application, the front-end buffer/sampler is traditionally designed with bipolar transistors and higher supply voltage, which make the integration of the front-end circuits and the ADC core a challenging task in scaled CMOS technologies with low supply voltage. We propose a digital background calibration technique to linearize the front-end circuits of IF-sampling ADCs.

## TECHNICAL APPROACH

The problem is solved in two steps. First, a simple power series model is used to eliminate the static nonlinearity with the split-ADC architecture and the LMS algorithm for background learning. Secondly, a derivative error model is developed to address the dynamic nonlinearity of the front-end circuits.

## SUMMARY OF RESULTS

Static nonlinearity is independent of the input frequency. Our linearization scheme is derived from a technique termed offset double conversion (ODC).

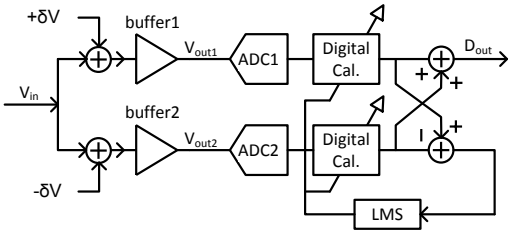



**Figure 1: ODC-based nonlinear calibration of ADC buffer**

As shown in Fig. 1, two dynamic offset signals are applied to the input of two conversion paths in the split-ADC architecture. The buffer transfer function is assumed to be nonlinear and static. When the system nonlinearity is successfully calibrated, the output difference between the two conversion paths should be a fixed offset which is identical to the offset injected at the input. A MATLAB simulation result shows that the proposed technique can potentially improve the SFDR performance by more than 40 dB.

Dynamic nonlinearity is dominant at higher frequencies, which is due to nonlinear switch resistance. The switch resistance of the traditional bootstrap architecture is

$$R_{on} = 1/\mu C_{ox}\frac{W}{L}\left(V_{DD} - V_{th} - \frac{1}{2}V_{DS}\right) \quad (1)$$

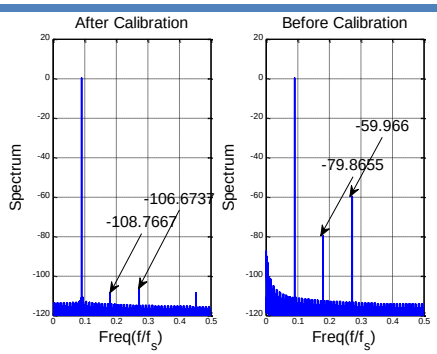



**Figure 2: Static nonlinearity calibration**

where Vds is proportional to the current flowing through the switch, which is frequency dependent. On the other side, the Vth variation is governed by the body effect, which depends mostly on input amplitude rather than input frequency. It is reasonable to assume that the Vds variation is dominant at higher frequencies. Based on this assumption, we propose a dynamic nonlinearity model capturing Vds variation effect as

$$V_{in} = V_{out} + \left(\tau_0 + \tau_1\left|\frac{dV_{out}}{dt}\right|\right)\frac{dV_{out}}{dt} \quad (2)$$

A S/H circuit using 65nm technology is simulated and calibrated with the proposed model. The input frequency is as high as 450 MHz and the SFDR is by approximately 40 dB. The sample rate is 100 MHz.

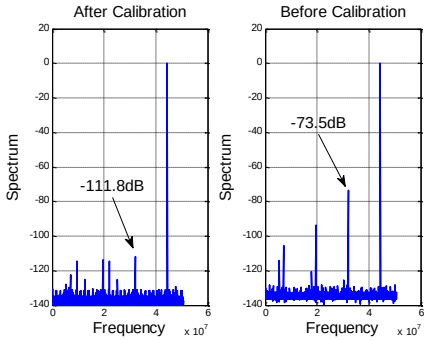



**Figure 3: Dynamic nonlinearity calibration**

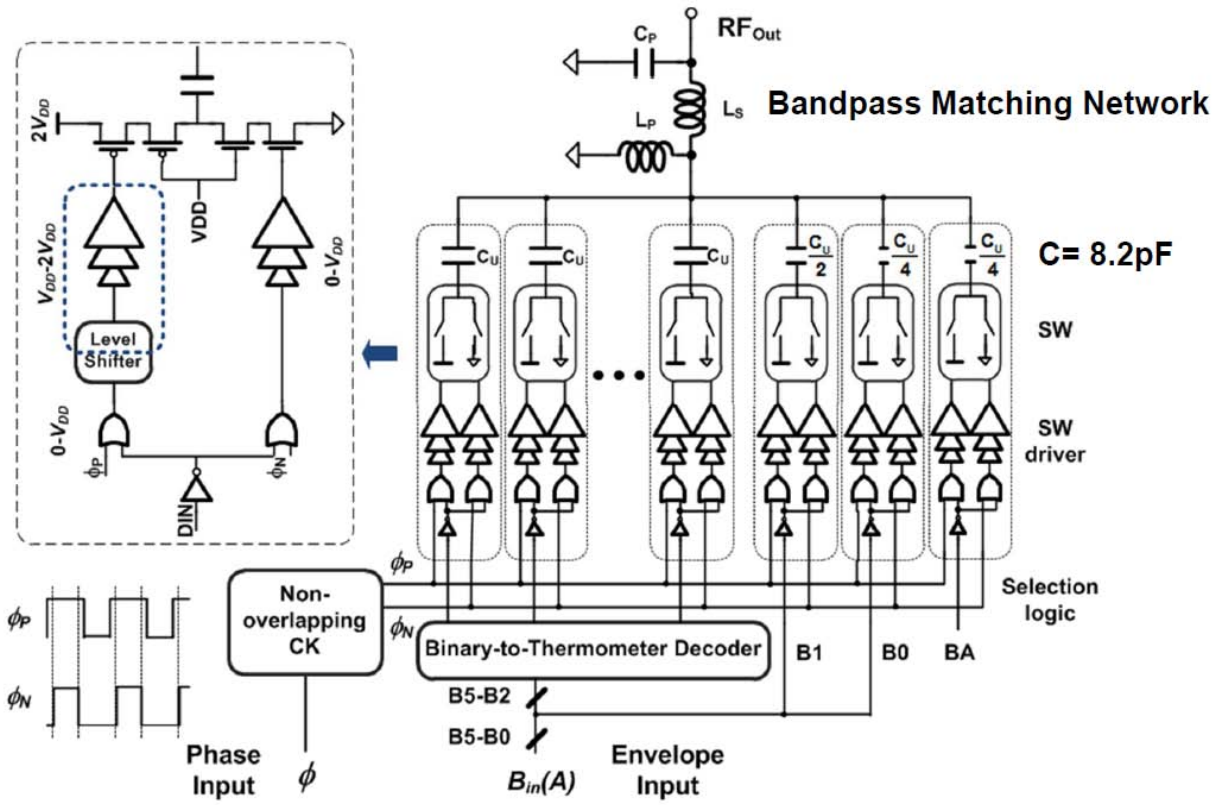
In the following year, we will investigate the validity of the proposed technique further with transistor circuits and design test structures to verify our assumptions and the potential effectiveness of the technique.

**Keywords**: IF-sampling, digital calibration, sample-and-hold, input buffer, split-ADC, offset double conversion

## INDUSTRY INTERACTIONS

Texas Instruments

# Fundamental Analog Thrust




## Summary of Accomplishments

| Category | Accomplishment |
|---|---|
| Fundamental Analog | Power combining techniques to achieve ~1W output power with an average efficiency >40% for OFDM signals at 2.4GHz and sufficient linearity to obviate digital predistortion in deep-sub-micron CMOS technologies. Scaling-friendly switched-capacitor circuits are used in CMOS digital power amplifiers to achieve high power, average efficiency and linearity. A class-G SCPA in 65nm CMOS with high average efficiency and high linearity.<br><br>Publications: (1) "A Switched-Capacitor PA for EER/Polar Transmitters," *IEEE ISSCC,* 2011. (2) "A Power-Combined Switched-Capacitor Power Amplifier in 90nm CMOS," *IEEE RFIC*, June 2011. (3) "A Switched-Capacitor RF Power Amplifier," *IEEE JSSC*, vol. 46, Dec. 2011. (4) "A Class-G Dual-Supply Switched-Capacitor Power Amplifier in 65nm CMOS," *IEEE RFIC*, June 2012. (5) "A Class-G Switched-Capacitor Power Amplifier," *IEEE JSSC*, vol. 48, May 2013.<br><br>(1836.085, PI: D. Allstot, University of Washington) |

| | |
|---|---|
| Fundamental Analog | ADCs that exploit both voltage and time domain information to provide additional resolution without increasing power. The action of residue shaping, allowing a multi-stage ADC with half-bit redundancy to achieve a 6dB higher SQNR has been analyzed and simulated. Optimization of binary SAR ADCs that use three-level DACs, but are not able to feature ternary quantizers, has been simulated resulting in energy and linearity improvements.<br><br>Publications: (1) “A 10b Ternary SAR ADC with Decision Time Quantization Based Redundancy,” *Proc. IEEE ASSCC.,* Nov. 2011. (2) “The Analysis and Application of Redundant Multi-Stage ADC Resolution Improvements through PDF Residue Shaping," Circuits and Systems I: Regular Papers, IEEE Transactions on, Early Access, 2012. (3) "Enhanced SAR ADC Energy Efficiency from the Early Reset Merged Capacitor Switching Algorithm," IEEE Int. Symp. Circuits Syst., pp. 2361-2364, May 2012.<br><br>(1836.097, PI: U. Moon, Oregon State University) |
| Fundamental Analog | Non-invasive methodology that keeps the stress interrupts for measurements within a few microseconds, preventing unwanted BTI recovery, while providing a parallel stress-measure capability on a large-scale memory array. An IEDM 2012 paper demonstrated for the first time an SRAM reliability macro capable of monitoring bit cell failures due to NBTI and PBTI.<br><br>Publications: (1) “Impact of Interconnect Length on BTI and HCI Induced Frequency Degradation,” IRPS, [Invited] 2012. (2) "On-Chip Silicon Odometers and their Potential Use in Medical Electronics,” IRPS, 2012. (3) "An Array-Based Chip Lifetime Predictor Macro for Gate Dielectric Failures in Core and IO FETs,” ESSDERC, Sept. 2012. (4) "A 32nm SRAM Reliability Macro for Recovery Free Evaluation of NBTI and PBTI,” IEDM, Dec. 2012.<br><br>(1836.085, PI: C. Kim, University of Minnesota) |

# TASK 1836.013 WIDEBAND RECEIVER ARCHITECTURES IN DIGITAL DEEP SUBMICRON CMOS

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## SIGNIFICANCE AND OBJECTIVES

Provide innovative solutions to achieve high performance and low power consumption required in continuous-time (CT) ΔΣ analog-to-digital converters (ADCs) for multi-standard receivers. Apply the proposed system and circuit-level techniques to the design of a low power CT ΔΣ ADC. Implementation of a CMOS chip prototype for the ADC and obtain experimental measurements to demonstrate the potential of the proposed solutions.

## TECHNICAL APPROACH

The main approach is to achieve the required flexibility in multi-standard RF receivers by exploiting the enormous momentum in digital signal processors. Particularly, the incoming signal at the receiver input is to be digitized as early as possible while filtering operations and channel selection are performed in the digital domain. In this context, CT ΔΣ modulators show up as an attractive option. There are two main challenges for that ADC to achieve the required performance within a multi-standard receiver:

1. Pulse width jitter associated with the clock of the feedback digital-to-analog converters (DACs).
2. Tolerance to OOB blockers in terms of loop filter linearity and noise folding.

Solutions to these two critical problems are being addressed by the ongoing research effort in this project.

## SUMMARY OF RESULTS

The block diagram in Fig. 1 illustrates the proposed hybrid DAC with jitter tolerance solution that is based on high-pass shaping the noise generated by pulse-width jitter in the feedback DAC. A second-order single-bit ΔΣ modulator is used as a test vehicle to demonstrate the performance of the adopted jitter suppression solution.

The plots in Fig. 2 show that the proposed solution can achieve jitter tolerance that can be as large as 20 dB over non-returning-to-zero (NRZ) DACs and comparable to switched-capacitor-resistor (SCR) DAC implementations. The proposed hybrid DAC solution doesn't entail any extra requirements on the slew-rate or gain-bandwidth of the op-amp in the load integrator.

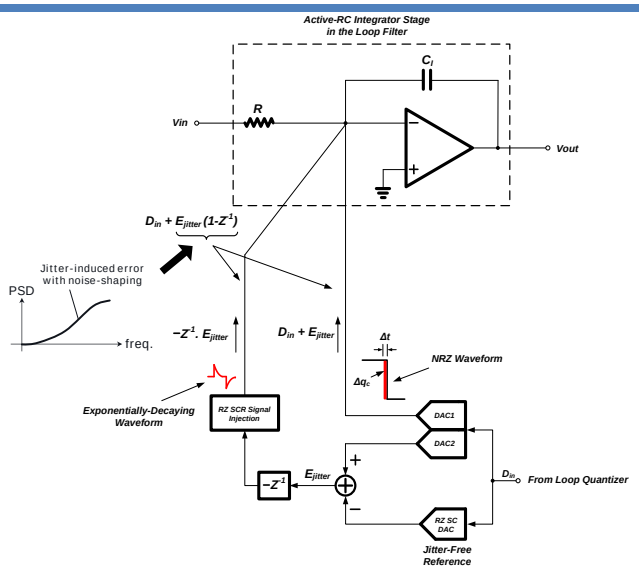


**Figure 1: Proposed Hybrid-DAC based on spectral shaping of jitter induced errors.**

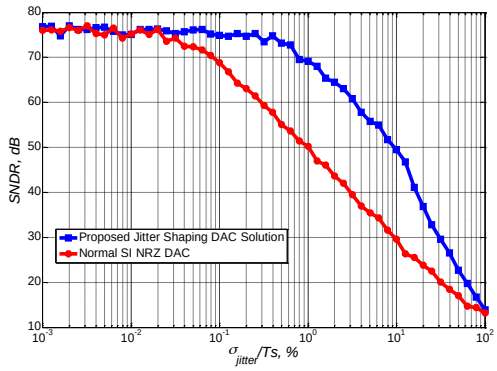


**Figure 2: Jitter tolerance performance of proposed DAC solution vs NRZ DAC.**

## INDUSTRIAL LIAISONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] R. Saad and S. Hoyos, "Feed-Forward Spectral Shaping Technique for Clock-Jitter Induced Errors in Digital-to-Analog Converters," IET Electronics Letters, vol. 47, no. 3, pp. 171–172, Feb. 2011.

[2] R. Saad, S. Hoyos, and J. Silva-Martinez, "Clock Jitter Shaping Technique for Continuous-Time Analog-to-Digital Converters," Patent No.: US 8164500, April 24, 2012.

# TASK 1836.022 HIGH-SPEED MIMO SIGNALING TECHNIQUES FOR SINGLE-ENDED PARALLEL I/O

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## SIGNIFICANCE AND OBJECTIVES

Processor-memory I/O bandwidth is often the bottleneck in high-speed computing. The goal of this task is to develop efficient adaptive techniques to improve multi-Gbps NRZ signaling by reducing crosstalk noise. This allows serial links to be placed closer together while operating at higher speeds for higher data throughput.

## TECHNICAL APPROACH

Our adaptive crosstalk cancellation (XTC) and automatic gain control (AGC) and decision feedback (DFE) loop cope with variations in channel inter-symbol interference (ISI) and crosstalk strengths. We are able to integrate and independently optimize ISI and XTC as the peak of the crosstalk amplitude occurs half a UI away from the cursor timing. The detection circuits used for adaptive XTC can be shared with the clock recovery loop to further reduce overall system power.

## SUMMARY OF RESULTS

Fig. 1 shows the circuit diagram for the adaptive XTC loop. The single-to-differential converter (SDC) has unity gain. XTC gain is adjusted via the signal addition ratio of the adder. After the XTC operation within the adder, the amplitude of resultant signal can vary depending on the value of addition. This variation of signal amplitude level is compensated for by the combination of the AGC (VGA) and adaptive DFE that follow so as to maintain a constant peak amplitude at the output of equalization stage.

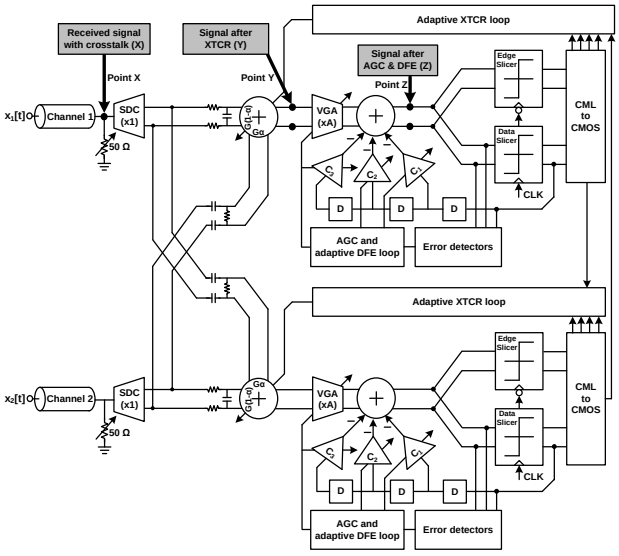


Figure 1: Complete adaptive XTCR and DFE architecture.

A data slicer that is triggered by the recovered clock makes decisions on the equalized signal. In parallel, an edge slicer samples the data signal at the transition timing and detects if the crosstalk is likely to produce a positive or negative impact. The detected digital signals are used to feed an adaptive XTC loop. CML-to-CMOS circuits convert differential signals at the slicer outputs into digital ones. A combinational logic block generates the 'UP' or 'DN' pulses depending on the sign of the crosstalk. An integrator updates the XTC gain by integrating these pulses. The digital delay block and combinational logic are similar to the phase detectors in a clock recovery block and can be shared to save power.

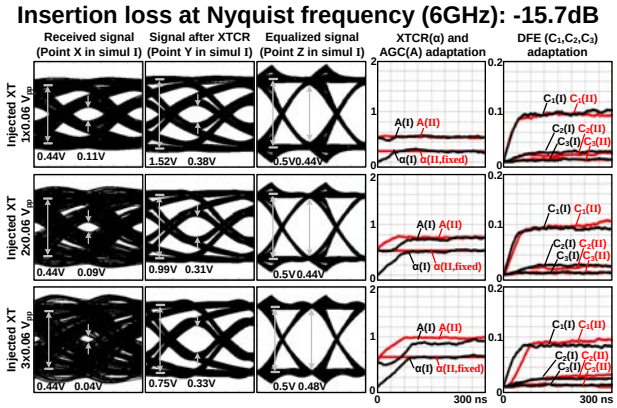


Fig. 2 presents simulation results for a 12 Gb/s adaptive XTC and AGC & DFE system. The channel has insertion loss of 15.7 dB with three crosstalk strengths of 60, 120 and 180 $mV_{pp}$. The eye-diagrams on the nodes at point X, Y and Z in Fig. 1 are observed and shown in the first three columns. The fourth column shows the converging values of the AGC gain (A) and the XTCR addition ratio (α) w/(black) and w/o (red) reutilized crosstalk.

**Keywords:** adaptive, crosstalk, cancellation, AGC, DFE

## INDUSTRY INTERACTIONS

Intel, AMD

## MAJOR PAPERS/PATENTS

[1] T. Oh and R. Harjani, "5 Gb/s 2x2 MIMO Crosstalk Cancellation Scheme," IEEE CICC, Sept. 2010.

[2] T. Oh and R. Harjani, "6 Gb/s MIMO Crosstalk Cancellation Scheme," (Invited) IEEE JSSC, Aug. 2011.

[3] T. Oh and R. Harjani, Analog-IIR Crosstalk Cancellation and Reutilization Receiver," IEEE VLSI, June 2012.

# TASK 1836.031 VARIATION TOLERANCE ANALOG DESIGN BASED ON GENERALIZED KHARITONOV/LYAPUNOV THEORY

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## SIGNIFICANCE AND OBJECTIVES

Process variations affect almost every circuit's performance. We have developed an approach to evaluate the interested circuit performance accounting for process variations. The interested circuit performance under process variations is firstly formulated as a constrained Nonlinear Programming (NLP) problem, and then the NLP problem is solved by Multi-Start Global Optimization (MGO) algorithm.

## TECHNICAL APPROACH

For evaluating the interested circuit performance under process variations, the following constrained NLP problem can be formulated as:

$$\text{Min}\backslash\text{Max } \mathrm{F} = f(\boldsymbol{P}) \qquad (1)$$

$$\boldsymbol{s.t.} \qquad \boldsymbol{P} = \{\boldsymbol{P}: P_i^- \le P_i \le P_i^+, i = 1,2,\dots n\} \qquad (2)$$

where $p_i$ is the *i*th process parameter and assumed to vary within its variation range $[p_i^-, p_i^+]$. $\boldsymbol{P}$ is an n dimensional process parameter variational space.

MGO algorithm is developed to solve the NLP problem. The basic flow of MGO is summarized (taking maximization procedure for example):

Initialize *i*=1

**While** (stopping criteria are not satisfied)

{ **Step 1.** Generate a start point $\boldsymbol{s}_i$ in $\boldsymbol{P}$ using Sobol quasi-random sequence generation method

**Step 2.** Apply a local NLP solver to obtain a local optimum $\boldsymbol{F}_i$ from $\boldsymbol{s}_i$

**Step 3.** If ! ($\boldsymbol{F}_i \in \boldsymbol{F}$) Update $\boldsymbol{F}_i$ into list $\boldsymbol{F}$

**Step 4.** *i=i+1*}

Return the largest one in $\boldsymbol{F}$ as final result

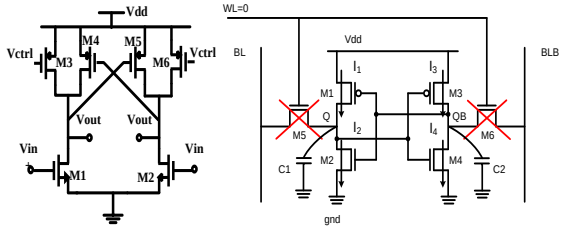
## SUMMARY OF RESULTS

A. Example of Worst Case Oscillator Phase Noise

Take a three stage ring oscillator, which is designed with Maneatis (Fig.1(a)) delay cell in 0.18µm technology. The worst case phase noise at 600 kHz is of interest. Five different methods are compared based on the total number of SPICE simulation runs (Table 1).

B. Example of DRV of SRAM cells

The Data Retention Voltage (DRV) of the SRAM cells (Fig.1(b)) is of interest. The SRAM cell is designed with 90nm technology. Three different methods are compared based on the total SPICE simulation runs.




(a) (b)

**Figure 1: (a) Maneatis Delay Cell (b) SRAM Cell**

**Table 1: Comparison Results for Oscillator Phase Noise**

| | *Accuracy* | *# of Samplings* | *Speed up* |
|---|---|---|---|
| **Process Corner** | 39% | 4 | 13451x |
| **Monte Carlo** | <0.1% | 53805 | 1x |
| **Quasi Monte Carlo** | <0.1% | 46877 | 1.1x |
| **Simulated Annealing** | <0.1% | 41086 | 1.3x |
| **Our method** | | 1760 | 31x |

**Table 2: Comparison Results for DRV of SRAM cells**

| | **Importance Sampling** | **Monte Carlo** | **Our Method** |
|---|---|---|---|
| **Computed DRV (6σ)** | 0.29 V | 0.29 V | 0.29 V |
| **# of Samplings** | $6\times10^5$ | $3\times10^7$ | < 70 |
| **Speed Up** | 8572x | 428572x | |

Besides the evaluations of circuit performance under process variations, this developed method can be extended to circuit performance optimizations. What is more, some parallel computing techniques can be employed to further speed up the developed approach.

**Keywords:** process variations, circuit performance evaluations, optimization method.

## INDUSTRY INTERACTIONS

Texas Instruments, Intel

## MAJOR PAPERS/PATENTS

[1] G. Huang et al.,"An Efficient optimization Based Method to Evaluate the DRV of SRAM Cells," IEEE Trans on Circuits and Systems I (submitted).

[2] L. Qian et al, "Oscillator Phase Noise verification Accounting for Process Variations," IEEE Trans on Circuits and Systems II (submitted).

# TASK 1836.038 A HYBRID 14-BIT ANALOG-TO-DIGITAL CONVERTER FOR BROADBAND APPLICATIONS

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AYDIN ILKER KARSILAYAN, TEXAS A&M UNIVERSITY

## SIGNIFICANCE AND OBJECTIVES

Recent developments in wireless communications have led to a strong need for low power, high resolution analog-to-digital conversion solutions. The performance of these must be immune to the presence of strong out of band blockers. This project will develop a low power, high resolution ADC robust against strong interferers.

## TECHNICAL APPROACH

To prevent saturation and overload in the presence of strong interferers, detectors are utilized to sense loop filter overloading in a continuous-time low-pass SD ADC topology. These activate a programmable attenuator that permits guaranteeing loop stability at the expense of reducing SNR. Then, since blockers and out-of-band quantization noise convolve with the noise of the clock, filtering the latter reduces the power of the aliased noise in-band. Hence, a 2nd-order HPF is included in the clock path to limit the effects of jitter. As result, robustness against loop saturation due to blockers and reduced sensitivity to clock jitter-induced noise are achieved.

## SUMMARY OF RESULTS

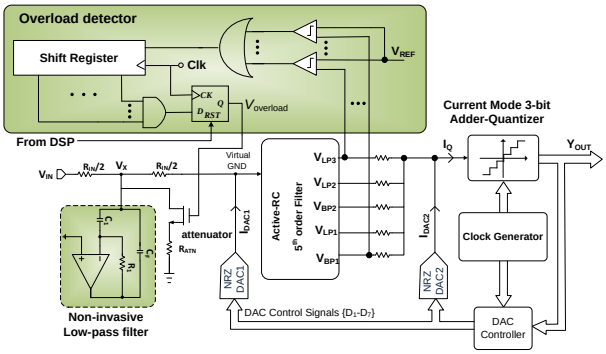


**Figure 1: 5th order feed-forward ΔΣ ADC with overload detector monitoring and non-invasive filtering.**

Fig. 2 shows the blocker filtering by non-invasive filter. First order filtering (Amplifier OFF trace) improves blocker tolerance by 4dB or more after 50MHz while the 2nd order non-invasive filter increases jitter tolerance by more than 10 dB for the same frequency range.

**Table 1: Summary of measured performance from ADC.**

| $F_s$ (MHz) | BW (MHz) | SNDR (dB) | DR (dB) | Blocker filtering | Power (mW) |
|---|---|---|---|---|---|
| 500 | 20 | 60 | 63 | 19 dB | 25 |

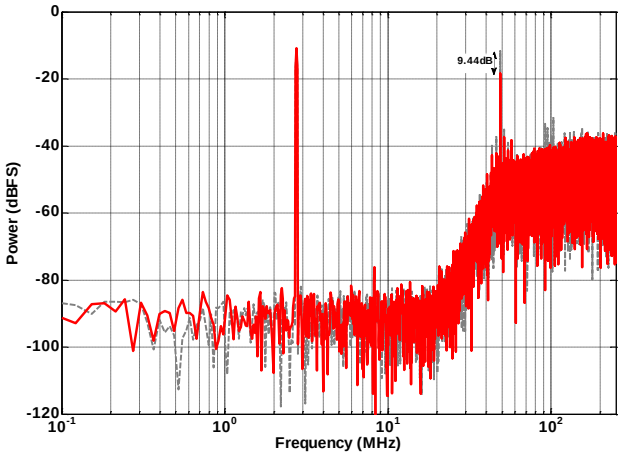


**Figure 2: Blocker tolerance with the amplifier ON and OFF in presence of an in band -11.5dBFS signal at 2.744 MHz**

**Keywords:** 5th–order CT LP SD ADC, Blocker, Input non-invasive Filter, Jitter, Filtering

## INDUSTRY INTERACTIONS

Texas Instruments, Intel, Freescale Semiconductor

## MAJOR PAPERS/PATENTS

[1] H. M. Geddada, et. al.," A Blocker Tolerant Analog-to-Digital converter for broadband applications," IEEE JSSC, to be submitted.
[2] J. Kim, et. al., "Wideband Inductor-less Balun-LNA employing feedback with noise and distortion cancelling," IEEE Trans on MTT, accepted, Sept. 2012.
[3] H. M. Geddada, et. al., "Fully Balanced Low-Noise Transconductance Amplifiers with P1dB > 0dBm in 45nm CMOS," IEEE European Solid-State Circuits Conference, Sept. 2011.
[4] H. M. Geddada, et. Al., "Inductorless Wideband CMOS LNAs with Nonlinearity Cancellation," IEEE Midwest Symposium on Circuits and Systems, Best Student Paper Award, Aug. 2011.
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# TASK 1836.039 UXIDS: UNCLONABLE MIXED-SIGNAL INTEGRATED CIRCUITS IDENTIFICATION

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## SIGNIFICANCE AND OBJECTIVES

We introduce the design and implementation of UxID, a novel class of Strong Physical Unclonable Functions (PUFs). UxID utilizes the uncertainty in CMOS leakage currents operating in the subthreshold region to create a unique fingerprint for each chip instance. A new authentication system is created for ultra-low overhead, robust operation of UxIDs.

## TECHNICAL APPROACH

We designed and implemented the first architecture for a novel current-based Strong PUF, which converts the analog variations in CMOS leakage currents to a unique digital quantity at a high speed and low power.

To ensure security and robustness of UxID in presence of inherent error instabilities and reverse-engineering, the novel low overhead Slender PUF protocol and system are created. Slender PUF enables a Prover with physical access to UxID to authenticate itself to a Verifier. Verifier shares a compact secret model characterizing the UxID challenge-response relationships, but Slender PUF fully hides the model from third-parties while being robust to errors and modeling attacks.

## SUMMARY OF RESULTS

Our UxID design (shown in Fig. 1) delivers ultra-low power consumption by operating on sub-threshold leakage currents and employing an automatic cut-off mechanism to stop the current flow after response evolution.

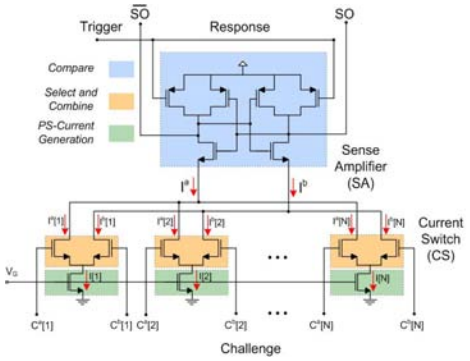


**Figure 1: PUF architecture with current generators, current switches, and a latch based sense amplifier.**

We have investigated the optimal operational parameters to achieve the highest level of robustness in presence of extreme variations in external conditions such as temperature and supply voltage. In doing so, we have targeted the Strong PUF class of operation and have investigated our circuit operation for temperatures ranging from -55°C to 125°C and 20% fluctuations in supply voltage. Our UxID design exhibits an error rate as low as 3% under extreme temperature variation, and 8% with the supply voltage fluctuations.

A chip containing 35 PUF strings has been custom designed and fabricated in IBM CMOS 90nm technology. Based on the challenge inputs, each PUF selects and combines a subset of currents generated by 128 random current generators. The combined quantities are then compared and the digital response is generated by two sense amplifiers. In order to reduce the number of pins, the challenges and responses are fed through two scan chains in a serial manner.

To address the issues pertaining to security in the presence of errors and modeling attacks, we devised the novel lightweight and low power Slender PUF system protocol. Slender PUF can be used with any Strong PUFs including UxIDs to automatically provide robustness against inherent noise in the PUF responses without requiring externally added and costly traditional error correction modules. Our Slender PUF implementation requires a few simple modules, excluding the need for expensive cryptographic functions and classic error correction techniques. Furthermore, we have performed a thorough analysis of the protocol's resiliency to various attacks. We have demonstrated that by careful selection of parameters our Slender PUF is resilient against all known Strong PUF machine learning attacks.

**Keywords:** Current PUF, Authentication, Low Power.

## INDUSTRY INTERACTIONS

IBM, Texas Instruments

## MAJOR PAPERS/PATENTS

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# TASK 1836.040 ENERGY-EFFICIENT CMOS 10GS/S 6-BIT ADC WITH EMBEDDED EQUALIZATION

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## SIGNIFICANCE AND OBJECTIVES

The proposed ADC system aims to significantly improve the energy efficiency of Nyquist-rate ADC-based receivers in high-speed applications through partial equalization embedded in the ADC. Techniques are developed to efficiently implement embedded equalization in a time-interleaved successive-approximation-register (SAR) ADC.

## TECHNICAL APPROACH

SAR ADC architectures have the potential to achieve excellent energy efficiency for medium resolution ADCs in sub-100nm CMOS technologies. In order to achieve the required conversion rate, a time-interleaved structure is used. The target design is a 6-bit 10GS/s ADC with figure of merit (FOM) better than 0.3pJ/conversion-step. To further relax the digital processing and achieve better efficiency for the whole receiver, especially for high-speed link applications, ADC with embedded partial equalization is considered.

## SUMMARY OF RESULTS

In order to relax ADC-based receiver power and complexity trade-offs, partial equalization can be embedded inside the ADC and not be limited by the ADC resolution. A statistical BER modeling tool was developed in this work that includes the effects of channel ISI, quantization noise, thermal noise, and receiver jitter. Utilizing this modeling tool, it was shown that 2-taps of embedded FFE allows for ADC resolution savings of 1-2bits for high-loss channels and embedded DFE allows for BER improvement for a given channel [1]. In order to explore this technique, two CMOS ADC prototypes with embedded equalization were implemented.

A 6-bit 1.6GS/s SAR ADC with an embedded 1-tap DFE (Fig. 1) was implemented in an LP 90nm CMOS process and achieved 4.75b ENOB at 0.46pJ/conv [2]. As shown in Fig. 2, in order to verify the functionality of the embedded 1-tap DFE, a transmitter module generates a 1.6Gb/s $2^{23}$-1 PRBS that is passed through a two-tap FIR filter and then applied to the ADC input. As evident by the ADC output codes, the distorted input data eye is dramatically improved from 3 LSB with the embedded DFE disabled to 27 LSB with the DFE enabled.

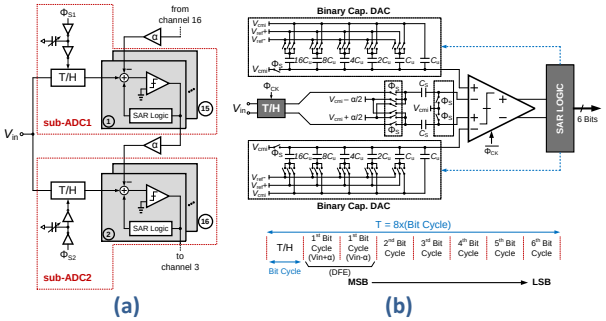


**Figure 2: SAR ADC with embedded 1-tap DFE: (a) block diagram, and (b) unit SAR ADC schematic.**

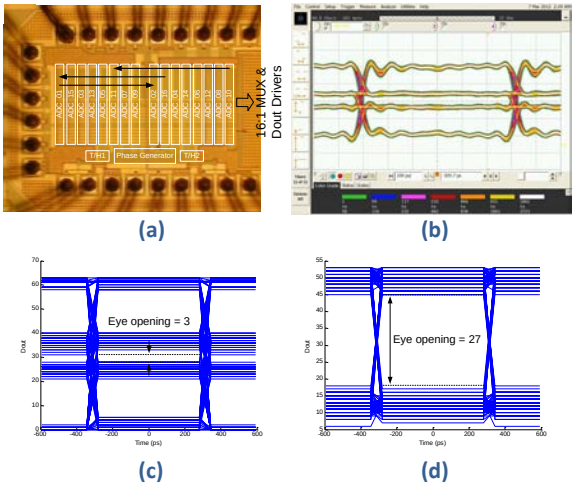


**Figure 1: 6-bit, 1.6GS/s ADC with embedded DFE experimental results: (a) 90nm CMOS prototype (b) 1.6Gb/s pre-distorted input signal (c) ADC output code with embedded DFE disabled (d) ADC output code with embedded DFE enabled.**

A 6-bit 10GS/s SAR ADC with embedded 2-tap FFE and 1-tap DFE was recently taped out in a GP 65nm process. Testing is currently underway for this prototype, with post-layout simulations predicting ENOB=5.1bits and the ADC FOM=0.25pj/conv.

**Keywords:** Analog-to-digital converter, embedded equalization, energy efficient, successive approximation register (SAR), time interleaved

## INDUSTRY INTERACTIONS

Intel, Texas Instruments

## MAJOR PAPERS/PATENTS

[1] A. Shafik et al., "Embedded Equalization for ADC-Based Serial I/O Receivers," IEEE EPEPS, Oct. 2011.

[2] E. Zhian Tabasy et al., "A 6b 1.6GS/s ADC with Redundant Cycle 1-Tap Embedded DFE in 90nm CMOS," IEEE CICC (accepted), Sept. 2012.

# TASK 1836.044 STATISTICAL MODELS AND METHODS FOR DESIGN AND TEST OF NON-DIGITAL COMPONENTS

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SHAWN BLANTON AND LAWRENCE PILEGGI, CARNEGIE MELLON UNIVERSITY

## SIGNIFICANCE AND OBJECTIVES

Develop, implement, and validate through experiment the statistical models and methods for the design of SRAM bit cells and their surrounding analog periphery circuits with user-provided constraints on performance, yield and quality.

## TECHNICAL APPROACH

A unified statistical analysis engine is developed to predict SRAM performance, yield, reliability and testability by fast Monte Carlo method. The proposed engine adapts the recent advance of Gibbs sampling from the statistics community to adaptively search the variation space and speed up the convergence of Monte Carlo analysis. Our experimental results demonstrate that the proposed Gibbs sampling method achieves 3~10× runtime speedup over other state-of-the-art techniques without surrendering any accuracy.

## SUMMARY OF RESULTS

SRAM bit cells are generally designed with minimum-size devices, and can be significantly affected by large-scale process variations posed by nanoscale manufacturing technology. It becomes increasingly critical to evaluate the statistical behavior of SRAM bit cells both efficiently and accurately. Since bit cells typically have extremely small failure probability, a simple Monte Carlo method suffers from slow convergence rate as only few random samples will fall into the failure region. To improve the sampling efficiency, importance sampling has been proposed to directly sample the failure region based on a distorted probability density function (PDF), instead of the original PDF of process variations.

Applying importance sampling to SRAM analysis, however, is not trivial. Ideally, in order to maximize prediction accuracy, we should sample the failure region that is most likely to occur. Such a goal, however, is extremely difficult to achieve, since we never know the exact failure region in practice. Motivated by this observation, a novel Gibbs sampling method is developed to improve the efficiency of importance sampling. Unlike the traditional Monte Carlo algorithm that samples a given PDF, the proposed Gibbs sampling approach does not need to know the sampling PDF explicitly. Instead, it adaptively searches the failure region and then generates random samples in it. From this point of view, Gibbs sampling can be conceptually viewed as a unique Monte Carlo method with an integrated optimization engine which allows us to efficiently explore the failure region.

The statistical analysis engine developed in this project facilitates us to efficiently explore the SRAM performance trade-offs at multiple levels of design hierarchy, including both the bit cells and their peripheral circuits. As a demonstration example, we study the robustness of an industrial 6-T 45nm SRAM cell under extremely low supply voltages. Fig. 1 shows the bit cell failure rate as a function of the supply voltage with different error-correcting schemes. It explores the design trade-offs between the robustness of the bit cell and the complexity of the error-correcting scheme.

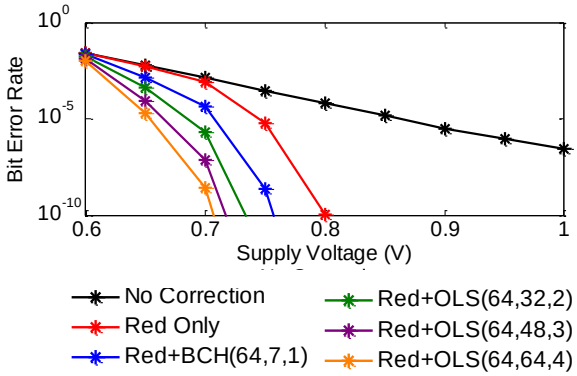


**Figure 1: Bit cell failure rate is shown as a function of supply voltage with different error-correcting schemes: redundancy (Red), Bose-Chaudhuri-Hocquenghem code (BCH) and orthogonal Latin square code (OLS).**

**Keywords:** memory, parametric yield, statistical analysis

## INDUSTRY INTERACTIONS

Texas Instruments, Freescale, Intel, IBM

## MAJOR PAPERS/PATENTS

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[2] C. Dong and X. Li, "Efficient SRAM failure rate prediction via Gibbs sampling," IEEE DAC, 2011.

[3] S. Sun, Y. Feng, C. Dong and X. Li, "Efficient SRAM failure rate prediction via Gibbs sampling," IEEE Trans. CAD (submitted), 2011.

# TASK 1836.057 HIGH ACCURACY ALL-CMOS TEMPERATURE SENSOR WITH LOW-VOLTAGE LOW-POWER SUBTHRESHOLD MOSFETs FRONT-END AND PERFORMANCE-ENHANCEMENT TECHNIQUES

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## SIGNIFICANCE AND OBJECTIVES

This project investigates temperature sensors based on subthreshold-MOSFETs and Schottky barrier diodes for on-chip thermal management, aiming to achieve low supply voltage, low power, small chip size and improved accuracy.

## TECHNICAL APPROACH

In order to achieve low supply voltage, subthreshold MOSFETs and Schottky barrier diodes are used to replace the traditional BJT devices in the temperature sensor. Bulk-driven technique is adopted in amplifiers to further reduce the supply voltage. Dynamic element matching (DEM), dynamic offset cancellation (DOC), gain boosting, etc, are applied to the sensor so as to minimize device mismatch induced errors. One-point low cost digital calibration methods are studied to further improve the accuracy performance of the sensor. Furthermore, scattered thermal monitors with small sensing diodes distributed across the chip featuring high accuracy of relative temperature measurement are proposed for multi-core thermal management solution.

## SUMMARY OF RESULTS

Subthreshold MOSFETs have been used as temperature-sensing devices for low voltage purpose. The error correction amplifier adopts bulk-driven inputs and further reduces the supply voltage. Measurements demonstrated sub-1-V/0.4-V operations in 0.5-µm/130-nm processes. Since the bulk-driven amplifier exhibits a lower gain than its gate-driven counterpart, a gain boosting mechanism has been demonstrated. In addition, advanced DEM and DOC are implemented to further minimize error [1].

In the multi-core era, multi-location thermal monitoring is desirable for load balancing. A MOSFETs-based temperature sensor front-end with scattered sensor nodes has been developed as shown in Fig. 1. The relative accuracy among different sensor nodes is improved by DEM and careful layout. Since the area close to the on-chip hot spots is expensive, one of the targets is to achieve small size for the sensing diodes. Besides, small sensing diodes can be deployed closer to the hot spots so as to sense the "real" temperature of interest. Experimental results demonstrated the multi-location thermal monitoring [2].

The Schottky barrier diode (SBD) is also a good candidate

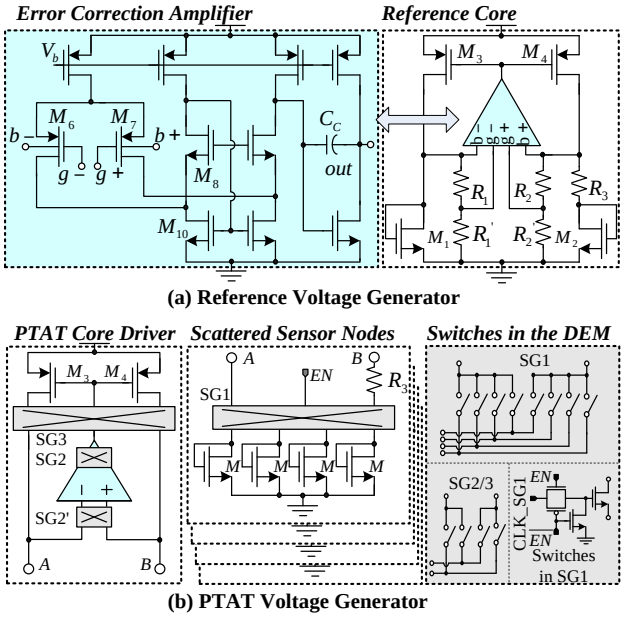


**Figure 1: Schematic of the proposed scattered thermal monitor.**

for low voltage applications. Another advantage of SBDs is that the device size is smaller. SBD devices have been characterized and an accurate model was developed for temperature sensor design. The zero-temperature-coefficient (ZTC) point has been demonstrated, which is much lower compared with subthreshold MOSFETs. This indicates promising low voltage applications in reference and temperature sensor design [3].

Furthermore, SBD-based multi-location thermal monitors have been designed. A special one-point low cost digital calibration method was proposed.

**Keywords:** Subthreshold MOSFETs, Schottky barrier diode, temperature sensor, low voltage, multi-location thermal monitoring

## INDUSTRY INTERACTIONS

Intel, IBM, Freescale, GLOBALFOUNDRIES.

## MAJOR PAPERS/PATENTS

[1] L. Lu, et al., "An all-CMOS low supply voltage temperature sensor front-end with error correction techniques," ISCAS, May 2012, Seoul, Korea.

[2] L. Lu et al., "An all-CMOS low supply voltage scattered thermal monitoring front-end," vol. 48, no. 16, 2012.

[3] Y. Li et al., "Temperature characteristics of Schottky barrier diodes for low voltage sensing applications," IET Electronics Letters, vol. 48, no. 7, pp. 406-408, 2012.

# TASK 1836.058 HIERARCHICAL MODEL CHECKING FOR PRACTICAL ANALOG/MIXED-SIGNAL DESIGN VERIFICATION

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## SIGNIFICANCE AND OBJECTIVES

Analog/mixed-signal (AMS) verification is a significant challenge to date and is confronted by complex dynamics and switching activities of AMS circuits. This project aims to develop practical AMS verification methodologies by leveraging hierarchical analog behavioral model equivalence checking, formal and semi-formal methods and machine learning techniques.

## TECHNICAL APPROACH

The inherent computational complexity associated with the verification of analog and mixed-signal circuits has rendered many formal methods non-scalable and hence calls for practical methodologies that can be applied to large designs. To this end, we aim to develop a framework that integrates analog behavioral model equivalence checking, which builds a bridging abstraction layer for verifying large AMS designs, and efficient formal approaches, which can be efficiently applied to the checked behavioral models. This framework allows one to combine the benefits of both formal and semi-formal verification techniques to tackle the grand challenge of verifying large AMS designs.

## SUMMARY OF RESULTS

Following up our earlier work on optimization-based analog behavioral model equivalence checking, recently we have developed a simulation-assisted reachability analysis approach. This reachability analysis intelligently introduces simulation acceleration into the process of reachability analysis while retaining the conservativeness of verification. This approach has been shown to be efficient for a class of nonlinear analog/mixed-signal circuits with complex continuous and discrete switching dynamics.

The proposed reachability analysis is used to verify the startup of a tunneling diode oscillator and locking of a charge-pump PLL starting from an uncertain initial condition. Fig. 1 illustrates the complex continuous dynamics and discrete state transitions in a charge-pump PLL. Locking of the PLL starting from uncertain initial conditions is verified using the proposed reachability analysis, which computes conservative approximations of the PLL state trajectories (Fig. 2). The conservativeness of the verification is confirmed by running Monte-Carlo simulation of the PLL starting from the targeted initial condition intervals. These results indicate that locking can be achieved in 2.1us.

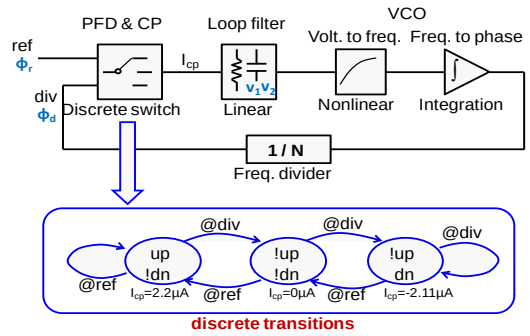


**Figure 1: Continuous dynamics and discrete state transitions in a charge-pump PLL.**

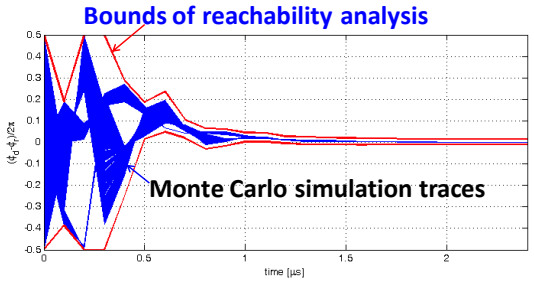


**Figure 2: The phase error trajectories of the PLL under uncertain initial conditions computed by the proposed reachability analysis.**

In the future, we will investigate on a coverage metric for behavioral model equivalence checking. This metric will provide a level of confidence for analog equivalence checking. We will also develop statistical machine learning techniques to complement our verification methodologies for further improvement on scalability.

**Keywords:** Analog/mixed-signal verification, behavioral modeling equivalence checking, formal and semi-formal methods, reachability analysis, machine learning

## INDUSTRY INTERACTIONS

Intel, Freescale, Texas Instruments

## MAJOR PAPERS/PATENTS

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# TASK 1836.059 POWER-EFFICIENT 10-20GS/S ADCs FOR HIGH-SPEED COMMUNICATIONS

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## SIGNIFICANCE AND OBJECTIVES

Next generation high-speed communication systems demand wide-bandwidth ADCs with sampling rate beyond 10GS/s. In serial links, wide-bandwidth ADCs followed by DSPs allow sophisticated equalization to correct fiber impairments and enhance channel spectral efficiency. Additionally, emerging wireless applications of the 10GHz UWB and newly unlicensed millimeter-wave-bands also demand such high-speed ADCs.

## TECHNICAL APPROACH

The current state of the art ADC around 10-20GS/s achieves 24GS/s sample rate in 90nm CMOS. However, its power consumption is quite high at 1.2W (5pJ/conversion-step FOM, 5ENOB @ low frequencies). Yet, this is the best compared with previous ADCs around 10-20GS/s in CMOS, SiGe, and InP HBT technologies in terms of power and FOM. Another design uses two interleaved flash ADCs to achieve 12.5GS/s rate with 4.5-bit resolution. This research will investigate techniques for power-efficient 10-20GS/s ADCs with a FOM<0.1pJ/conversion-step and 5ENOB.

## SUMMARY OF RESULTS

This research investigates using time-interleaved flash converters to achieve 10-20GS/s sampling rates. The accuracy of a flash ADC in CMOS is dominated by random offsets of comparators due to device mismatches. To improve the accuracy, large devices are needed to minimize device mismatches. However, this presents more parasitic capacitance to reduce the speed. To maintain a certain speed, larger current, therefore, larger power is required. Using offset calibration, smaller devices can be used to achieve the desired accuracy. Therefore, the speed is improved and the power consumption can be smaller, leading to better FOM.

Two new digitally controlled trimming offset calibration techniques have been proposed to calibrate preamplifier and comparator offsets and to minimize the loading of the calibration devices on the critical signal path to enhance ADC bandwidth.

We have studied the trade-offs related to sub-ADC speed and time-interleaving factor. In this design, we will use 65nm CMOS process for 10GS/s ADC due to consideration of fabrication cost. In the existing publication literature, the fastest published ADC in 65nm CMOS without interleaving is 5GS/s. Higher than 5GS/s operation might be possible to design but power efficiency would degrade increasingly faster as the speed approaches the technology limit. Therefore, the minimum possible interleaving factor for 65nm CMOS is 2 to achieve good power-efficiency. On the other hand, if the time-interleaving factor is too much, there would be a large strain on the amount of timing skew calibration. Complicated background calibration algorithm would be needed to achieve such a calibration which inturn would consume a large amount of digital resources. Overall, in our design, we make a design trade-off and make the interleaving factor to be 4 with each sub-ADC running at 2.5GS/s. The architecture of the sub-ADC is a two-step structure in lieu of a full-flash structure to achieve better power efficiency, which is one of the main objectives of our proposed research. We also propose a simplified foreground timing skew calibration which makes the interleaving clock timing calibration much easier. Figure 1 shows the overall simulation result of our time-interleaved ADC at 10GS/s. The SFDR is above 45dB over all frequency while the SNDR has a bandwidth of 7GHz, which is limited by the input network bandwidth.

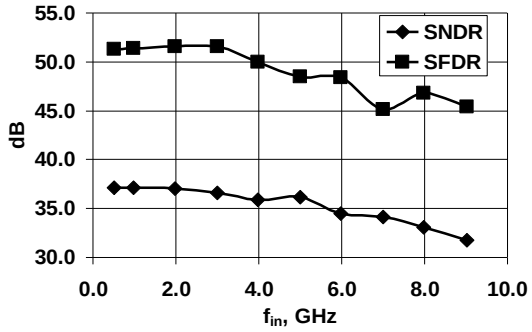


**Figure 1: Post-layout simulation on the time-interleaved ADC at 10GS/s in 65nm CMOS**

**Keywords:** Time interleaved ADC, Flash ADC, ADC calibration, power efficiency

## INDUSTRY INTERACTIONS

Texas Instruments, Intel, Freescale, IBM

## MAJOR PAPERS/PATENTS

[1] J. Yao and J. Liu, *CICC*, Sept. 2011

[2] X. Yang and J. Liu, *CICC*, Sept. 2011

# TASK 1836.072 LOW COST TEST OF HIGH SPEED SYSTEMS

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## SIGNIFICANCE AND OBJECTIVES

With ever increasing speed of communication systems, the cost of testing high speed devices (10 GHz – sub THz) for noise and distortion is becoming prohibitive. In addition, acquisition of high speed signals poses significant challenges. In this task, low cost scalable solutions for future high speed test and characterization are developed.

## TECHNICAL APPROACH

The cost of high speed signal measurement is dominated by the costs of synchronized high-speed data acquisition and capture. In this task, through use of intelligent back-end signal processing algorithms along with (incoherent) time and frequency sampling techniques, the cost and complexity issues of high speed signal capture and reconstruction are significantly alleviated.

The two major techniques that are developed in this project are based on jitter expansion and incoherent under sampling of data. While jitter expansion provides a simple solution to the problem of sub pico-second jitter measurement, waveforms reconstructed from incoherently under-sampled data can be used for system performance characterization at extremely high speeds without the use of a waveform-synchronous trigger.

## SUMMARY OF RESULTS

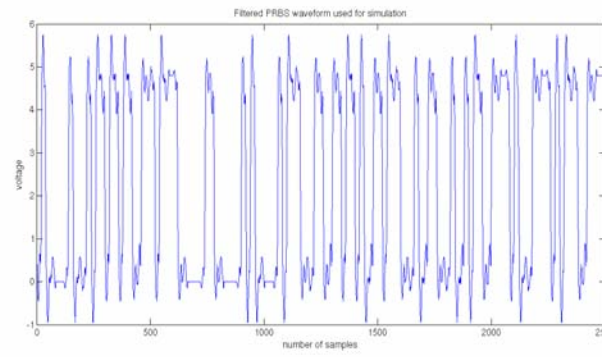


**Figure 1: Reconstructed 2^7 -1 PRBS waveform using incoherent under-sampling.**

Low cost scalable and accurate solutions for high frequency test signal acquisition have been demonstrated that are robust to variations in signal phase and do not require precise phase synchronization at high frequencies. The incorporation of asynchronous under-sampling allows one to reduce the cost of the data acquisition system without precise knowledge of the signal clock. It is possible to reconstruct, with high accuracy, complex periodic signal waveforms ranging from multi-tone signals to pseudo random bit sequences (PRBSs). In Fig. 1 we show the reconstructed eye for a 127 bit PRBS waveform. Reconstruction is performed using time domain analysis methods that give O(log(N)) improvement per iteration over Fourier domain reconstruction (N= no of samples) using significantly fewer number of data samples.

Even when the data waveform is not periodic we were able to reconstruct the eye diagram as shown in Fig. 2.

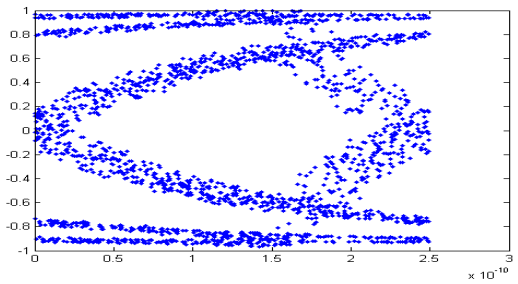

**Figure 2: Reconstructed eye for random bit stream using incoherent under-sampling.**

From the reconstructed waveform we were able to measure and separate out the various jitter components and precisely estimate path delay mismatch in various circuit traces.

**Keywords:** High speed test, waveform acquisition, under-sampling, jitter measurement, eye monitoring.

## INDUSTRY INTERACTIONS

Texas Instruments, Intel

## MAJOR PAPERS/PATENTS

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# TASK 1836.075 DESIGN OF 3D INTEGRATED HETEROGENEOUS SYSTEM

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## SIGNIFICANCE AND OBJECTIVES

The objective of this research is to address the challenges to 3D integration of highly different circuits/systems with varying technology, power profiles, operating voltage, and clock domains through the 3D technology using Through-Silicon-Via (TSV).

## TECHNICAL APPROACH

The performance, power, and reliability of a 3D-Integrated Heterogeneous System (3D-IHS) depend on the functionality, power profile, and frequency of individual dies; the non-uniformity in their physical environments; die-to-die coupling; and die-to-package coupling. This research will develop design methods for the 3D-IHS and transform them into design tools and silicon prototype. This project will develop design methods and tools for power/clock delivery, signal integrity, and die-to-die communication in 3D integrated heterogeneous systems. The technical approach integrates modeling, circuit techniques, and physical design to deliver design tools and silicon prototype.

## SUMMARY OF RESULTS

The primary results include design methods for 3D integrated heterogeneous systems (3D-IHS) and their application to example high-performance and embedded systems. The major observations are:

- *TSVs and Signal Integrity:* We have first developed an on-chip test and signal recovery circuit to detect TSV defects and recover signal [1]. Next, we have modeled the TSV-to-TSV coupling in 3D ICs and studied its impact on full-chip signal integrity [2]. Finally, we have analyzed the interactions 3D Via potential and electrical behavior of neighboring transistors for FDSOI devices [3].
- Clock-Delivery in 3D ICS: We have presented 3D clock delivery methods that optimize the number of TSVs and buffers, and their placements to design robust 3D clock trees [4].
- Thermal Effects in 3D IC: We have studied the effect of thermal coupling a core and SRAM stack. We have observed that due to thermal coupling the power dissipation in cores strongly modulates the performance and robustness of 3D SRAM [5]. Also, 3D IC placement methods have been developed that exploit the thermal coupling in the stack [6]. TSVs and logic cells are spread intelligently on each die to reduce the local power density and increase the thermal conductivity of different tiers to the heat sink to improve overall thermal behavior.
- Power Deliver in 3D ICS: We have analyzed the bias and frequency dependent capacitance of the P/G TSVs and its impact on the high-frequency noise in the power delivery network (PDN) of a 3D stack [7]. Next, we have modeled the current density distribution within a P/G TSVs considering DC current crowding and used the models for chip-scale power grid analysis [8]. Finally, we have shown that due to the tier-to-tier supply coupling, PDN noise generated by cores (aggressor) can degrade the robustness of SRAMs (victims) in a 3D stack [9].
- Post-silicon-Tuning for 3D ICs: We have developed tier-adaptive-voltage-scaling (TAVS) as a post-silicon tuning methodology for improving parametric yield of 3D integrated circuits considering die-to-die and within-die process variations [10].

**Keywords:** 3D integration, heterogeneous system, signal integrity, die-to-die coupling, Through-Silicon-Vias

## INDUSTRY INTERACTIONS

Global Foundries, IBM, and Intel Corp,

## MAJOR PAPERS/PATENTS

[1] M. Cho, et. al. *IEEE TCPMT, Nov. 2011*.

[2] C. Liu, et. al., DAC, 2011.

[3] A. Trivedi et. al. *IEEE EDL,* pp. 1020-1022, *Aug. 2011*.

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[5] S. Chatterjee, et. al. "Impact of Die-to-Die Thermal Coupling on the Electrical Characteristics of 3D Stacked SRAM Cache," IEEE Semi-Therm, Feb. 2012.

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[8] X. Zhao, et. al. "Analysis of DC Current Crowding in Through-Silicon-Vias and Its Impact on Power Integrity in 3D ICs", ACM Design Automation Conference, 2012.

[9] K. Chae et. al, "Tier-Adaptive-Voltage-Scaling (TAVS): A Methodology for Post-Silicon Tuning of 3D ICs," ASP-DAC, Jan. 2012.

[10] W. Yueh, et. al, "On the Parameteric Failures of SRAM in a 3D-die Stack considering Tier-to-Tier Supply Cross-talk," IEEE VTS, 2012.

# TASK 1836.077 STATISTICAL CHARACTERIZATION OF CIRCUTI AGING

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## SIGNIFICANCE AND OBJECTIVES

We perform a recovery free evaluation of the impact of Negative and Positive Bias Temperature Instability (NBTI, PBTI) on read/write operation in a 32kb SRAM macro implemented in a 32nm high-κ/metal-gate silicon-on-insulator process. A novel non-invasive methodology keeps the stress interrupts for measurements within a few microseconds, preventing unwanted BTI recovery from corrupting the test data, while providing a parallel stress-measure (SMS) capability on large scale arrays.

## TECHNICAL APPROACH

A 32kb SRAM was implemented in a manner identical to a product sub-array. The complexity of the test was transferred to the finite state machine (FSM) to administer the SMS timing sequence. The measure window was kept short by doing a pseudo-read operation, to store the flip data internally in the memory array. The full readout and slow scan operation is deferred to the stress cycle. The FSM timing sequence for conventional approach and proposed approach are shown in Fig. 1. Compared to conventional approach of fully reading out flip information for each cell during measurement window, we get a several order improvement in measure time, reducing error due to unwanted BTI recovery.

## SUMMARY OF RESULTS

**Read Failure Measurements:** Fig. 2(a) shows read bit failure rate (BFR) with stress time at different measurement interrupts ($T_{MEAS}$) showing expected degradation trends. Over a period of 2000s stress time, BFR degrades roughly ten times. The right column shows BFR captured after $T_{STRESS}$=10s at different $T_{MEAS}$. Over $T_{STRESS}$=2000s, with $T_{MEAS}$ kept at 3µs, the BFR rises by around 10 times. Without using the proposed timing technique, $T_{MEAS}$ is more than few milliseconds, causing errors of as much as 10-100X in terms of BFR. We can also look at how Read $V_{MIN}$ evolves over the stress time. By ensuring an at-least three decade smaller $T_{MEAS}$, the proposed method alleviates 35mV error from the conventional methods.

**Write Failure Measurements:** Fig. 2(b) shows the BFR evolution for write case. As expected, there is an improvement seen in BFR. The sensitivity to $T_{MEAS}$ was found to be much greater than the read, and BFR is seen to drop sharply below 3.6µs. At 85°C for $T_{STRESS}$=2000s, the BFR drops 2x, pointing to lower sensitivity overall to BTI stress, compared to read case. Overall, a 100X error in BFR is obtained from the conventional methods due to the smaller $T_{MEAS}$.

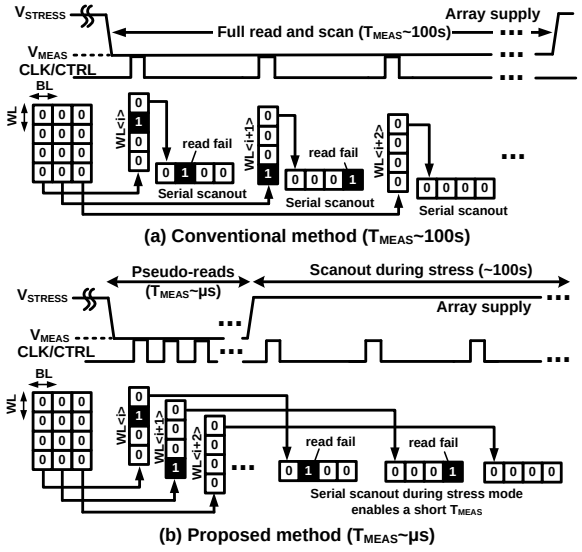


Figure 1: (a) Conventional method (b) Proposed method

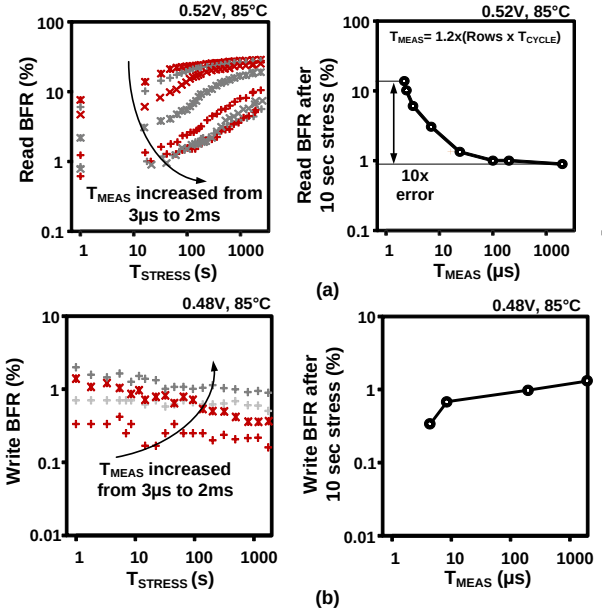


Figure 2: (a) Read and (b) Write bit failure rates change with stress time measured from a 32nm HKMG SOI test chip.

**Keywords:** SRAM reliability, NBTI, PBTI, recovery

## INDUSTRY INTERACTIONS

Texas Instruments, Intel, IBM, GLOBALFOUNDRIES

## MAJOR PAPERS/PATENTS

in preparation

# TASK 1836.078 HIGH-RESOLUTION, CHARGE-BASED A/D CONVERTERS FOR NANO-CMOS TECHNOLOGIES

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## SIGNIFICANCE AND OBJECTIVES

The successive approximation register (SAR) ADC architecture is attractive for integration in aggressively scaled CMOS, primarily since it does not rely on linear amplification blocks. This project aims to push the performance of SAR ADCs to the next level achieving both high resolution (~12bits) and high speed (>150MHz) in 65nm CMOS technology. These specifications are required e.g. in wireless base station receivers.

## TECHNICAL APPROACH

Aggressive scaling of unit capacitances in a SAR ADC allows the designer to set the input capacitance according to the thermal noise limit, resulting in lower switching energy and faster conversion speed. Silicon measurements of an innovative test structure designed to measure the mismatch characteristics of small unit caps (0.5f – 1fF) will commence shortly. In addition, chip measurements of an 8 bit, 400-MS/s SAR A-D converter that uses the idea of time constant matching (TCM) are currently in progress. Learnings from these measurement results will be used to design the final SAR ADC targeting 12 bits, and $f_s$ = 200MHz.

## SUMMARY OF RESULTS

The top level block diagram of the 8-bit SAR ADC is shown in Fig. 1. It consists of a binary weighted capacitive DAC, a fast comparator and digital SAR logic. A metal-on-metal (MOM) fringe capacitance of 0.75fF is used as the unit cap in the capacitive DAC. Time constant matching is used to speed up the DAC settling, which is a major bottleneck in improving the conversion speed. Asynchronous timing in the SAR logic obviates the need of a fast external clock, increases the conversion speed and improves the metastability probability. The conversion speed of a SAR ADC is inversely proportional to the SAR loop delay, which can be expressed as $T_{loop} = T_C + T_D + T_{DAC}$; where $T_C$ is the comparator decision time, $T_D$ is the digital delay through the SAR logic and $T_{DAC}$ is the DAC settling time. A fast comparator with small regeneration time constant decreases $T_C$. TCM reduces $T_{DAC}$ by appropriate matching of the pull up and pull down paths in the capacitive DAC. Making the pull down path faster (larger switch) does not reduce $T_{DAC}$ substantially but increases $T_D$ as the bigger switch presents a larger capacitive load to the SAR logic. This has a detrimental effect on the ADC conversion frequency. Optimum switch sizing as per TCM provides a design point that reduces $T_C + T_D$, thus increasing the conversion speed of the ADC. The chip layout is shown in Fig. 2. Preliminary chip measurements show promising performance.

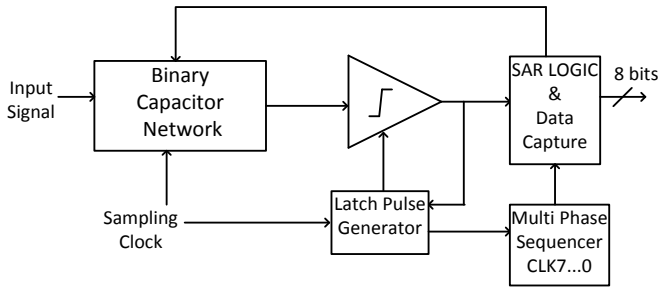


**Figure 1: Top level block diagram of the 8-bit SAR ADC.**

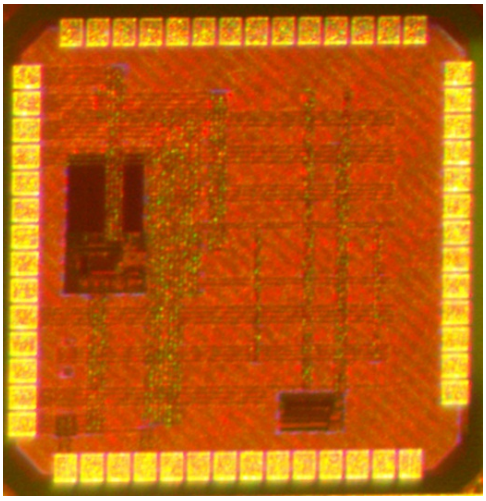

**Figure 2: Die photo of the 8-bit, 400-MS/s SAR ADC.**

**Keywords**: Capacitor matching, time constant matching, CMOS, Successive approximation, ADC

## INDUSTRY INTERACTIONS

Texas Instruments, Freescale, Intel

# TASK 1836.080 VARIATION-TOLERANT NOISE-SHAPING ADCs WITH EMBEDDED DIGITAL BIAS AND VDD SCALABLE FROM 0.5V TO 1.2V FOR NANOSCALE CMOS

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## SIGNIFICANCE AND OBJECTIVES

We have demonstrated different design techniques and architectures for analog circuits down to 0.5V in earlier work. However, with the advance of technologies, it is necessary to develop high performance circuits in flexible supply applications. This project proposes to investigate the supply scalable analog interfaces on nano-scale CMOS process.

## TECHNICAL APPROACH

A continuous-time sigma-delta modulator with embedded digital biasing will be designed and fabricated to address the flexibility of supply scalable operation. This project chooses the sigma delta modulator with a continuous-time implementation because of the relaxed sampling network requirement and no need for signal-path switches that are not suitable for low supply voltage applications. A cascaded 2-1 architecture has been selected to overcome the stability challenges when changing the supply voltage. In addition, the pulse-controlled common-mode biasing is proposed for scalable supply operation and to avoid the use of large area of passive components and thus provide substantial area savings.

## SUMMARY OF RESULTS

The architecture of a cascaded 2-1 continuous-time (CT) sigma delta modulator (SDM) with digital noise cancellation filters is shown in Fig. 1. The sub-ADCs and sub-DACs are chosen to be four bits to reduce quantization error and the clock jitter sensitivity. A four-input sub-ADC is implemented in the first stage of the modulator to remove the need of a summing amplifier.

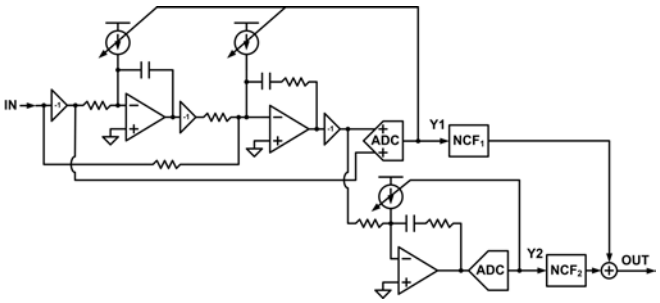


**Figure 1: Architecture of a cascaded 2-1 CT SDM.**

By using the system level simulation, the design requirements to performance limitations have been studied, including the unity-gain bandwidth and DC gain of the amplifiers, loop filter component value (RC) variation, and clock jitter.

The impact of the supply voltage scaling from 0.6 to 1.2V on the figure-of-merit of the sigma-delta modulator is being modeled and studied for the different sub-blocks.

The proposed pulse-controlled common-mode feedback (CMFB) shown in Fig. 2 is a digital biasing technique. By using this technique, there is no need for large passive components for common mode sensing while enabling large output swings compared to active solutions. The disturbance on the amplifier outputs is significantly smaller than for switched capacitor solutions.

A proof-of-principle prototype to demonstrate the pulse controlled common-mode feedback as well as the voltage scalable architecture (0.6 – 1.2V) is being designed, simulated and laid-out with a tape-out target at the end of August 2012. The prototype will also help to validate the performance models used to evaluate the FOM supply dependence.

**Keywords:** Supply scalable amplifier, continuous-time sigma delta modulator, digital biasing

## INDUSTRY INTERACTIONS

Texas Instruments, Freescale

# TASK 1836.084 SINGLE SET-UP DETAILED TESTING OF WIRELESS TRANSCEIVERS FRONT-ENDS USING DIGITAL PROCESSING

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## SIGNIFICANCE AND OBJECTIVES

This project aims at development of system-level characterization approaches for the most important parameters of RF front-ends through a digital interface and using a single test set-up. A secondary objective of the project is the derivation of analytical models to compute top-level parameters, such as EVM, from extracted system-level parameters.

## TECHNICAL APPROACH

The generic technique that is used in this project is based on (a) mathematical modeling of the overall circuit behavior including all desired parameters of interest and additional parameters that may affect circuit response and (b) development of excitation signals that will decouple the various parameters of interest from the observed response. The venue has been selected as RF transceivers but the technique can generally work with any analog circuit that can be mathematically modeled.

## SUMMARY OF RESULTS

The modeling technique has been implemented for a full transceiver architecture as well as a transmitter followed by an envelope detector that is used as the Built-in-test circuit. The parameters of interest for the modeling include linear domain parameters, such as gain, IQ gain imbalance, IQ phase imbalance, DC offsets, time skews, and non-linear domain parameters such as the third order input intercept of the transmitter and the receiver. The envelope detector is modeled as self-mixer followed by a low-pass filter with unknown gain/attenuation. Using specialized test signals, it is possible to determine the parameters in a step-by step fashion. It should be noted that all these parameters have been determined with only one test set-up.

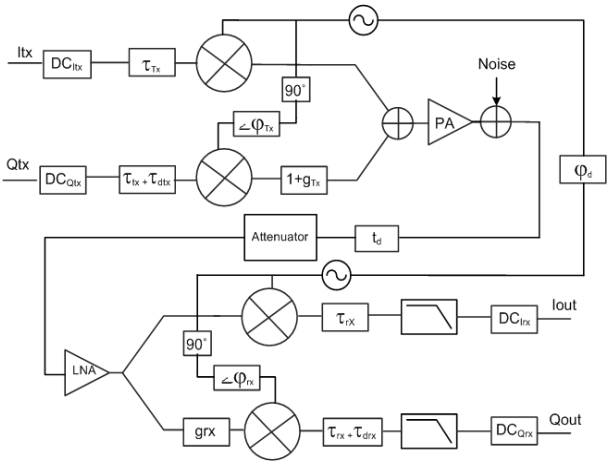


**Figure 2: Loop-back configuration including the parameters that need to be measured.**

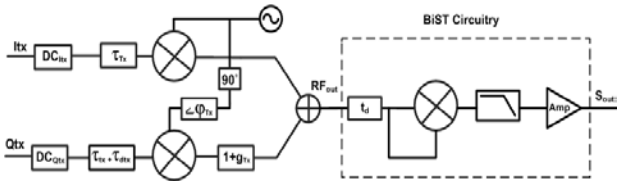


**Figure 1: Transmitter model with envelope detector.**

Figure 1 shows the overall model including the parameters of interest for the loop-back configuration, and Figure 2 shows the model for the transmitter followed by the envelope detector configuration. The measurement approach has been verified using hardware experiments that follow the architectural configurations of Figures 1 and 2. Tables I and II show the accuracy of measurements using these two configurations.

**Table 1: Hardware measurement results in loop-back mode.**

| Parameter | Actual | Computed | Error |
|---|---|---|---|
| TX Phase MM | 4° | 5.87° | 1.87° |
| RX Phase MM | 2° | 1.25° | 0.75° |
| TX Gain MM | 25% | 25% | 0% |
| RX Gain MM | 15% | 16% | 1% |
| Irx-Dcoffset | -20mV | -18mV | 2mV |
| Qrx-Dcoffset | 10mV | 9.4mV | 0.6mV |

**Table 2: Hardware measurement results for the transmitter with envelope detector.**

| | Actual | Computed | Error |
|---|---|---|---|
| **Gain MM** | -5% | -5.1% | 0.1% |
| **Phase MM** | 1° | 1.1° | 0.1° |
| **DC Itx** | 10mV | 12.6mV | 2.6mV |
| **DC Qtx** | 10mV | 10.6mV | 0.6mv |
| **IIP3** | 5.8dBm | 5.1dBm | 0.7dB |

**Keywords:** transceiver testing, built-in test

## INDUSTRY INTERACTIONS

Texas Instruments, Intel

## MAJOR PAPERS/PATENTS

[1] A. Nassery, O. E. Erol, S. Ozev, and M. Verhelst, "Signal Development and Analysis for OFDM Systems RF Front-End Parameter Extraction," IEEE TCAD.

# TASK 1836.085 CMOS SWITCHED-CAPACITOR POWER AMPLIFIER TECHNIQUES

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## SIGNIFICANCE AND OBJECTIVES

A digitally-controlled switched-capacitor RF power amplifier (SCPA) uses a dual-supply, class-G architecture and is implemented in 65nm CMOS. It implements signal envelope digital-to-analog conversion using switching functions controlled by digital logic to achieve superior efficiency and high linearity at output power backoff to eliminate the need for digital predistortion.

## TECHNICAL APPROACH

A class-G SCPA improves the average efficiency for signals with large peak-to-average power ratios. It operates from either of two power supply voltages depending on the amplitude of the signal. Operation close to saturation for more than just the near-peak signal levels is achieved by digitally selecting the optimal supply voltage based on a digital code word representation of the envelope $A(t)$. For small (large) $A(t)$ values, selected capacitors are switched between $V_{DD}$ and $V_{gnd}$ ($V_{DD2}$ ($2\times V_{DD}$) and $V_{gnd}$). An optimal switching arrangement is used in the design to maximize efficiency.

## SUMMARY OF RESULTS

A class-G SCPA is shown in Fig. 1 (the fabricated circuit is fully differential). It utilizes a digital EER technique to achieve high linearity from a high-efficiency switching configuration. First, the non-CE modulated baseband signal is transformed from a Cartesian representation to an equivalent polar form. The resulting time-varying amplitude signal, $A(t)$, is input as a digital code word, $B_{IN}(A)$, to combinatorial decoding logic that enables switching of the bottom plates of selected capacitors between $V_{DD}$ and $V_{gnd}$ or $V_{DD2}$ and $V_{gnd}$. After up-conversion to the RF carrier frequency, the time-varying phase signal, $\phi(t)$, serves as the clock input to the combinatorial logic that drives the capacitor array.

The un-switched top plates are connected to a band-pass matching network that provides low impedance to the array at the desired frequency, enables high power output, and filters harmonics associated with switching.

For the conventional switching sequence (Fig. 1), the efficiency decreases as the normalized output voltage changes from 1.0 to 0.5 V. This drawback is overcome using a switching sequence that uses both $V_{DD}$ and $V_{DD2}$ (Fig. 1). The SCPA delivers a peak (average) output power of 24.3 (16.8) dBm with a peak (average) PAE of 44% (33%) for an *IEEE 802.11g* signal with an EVM of 2.9 % at 2.4 GHz as shown in Fig. 2.

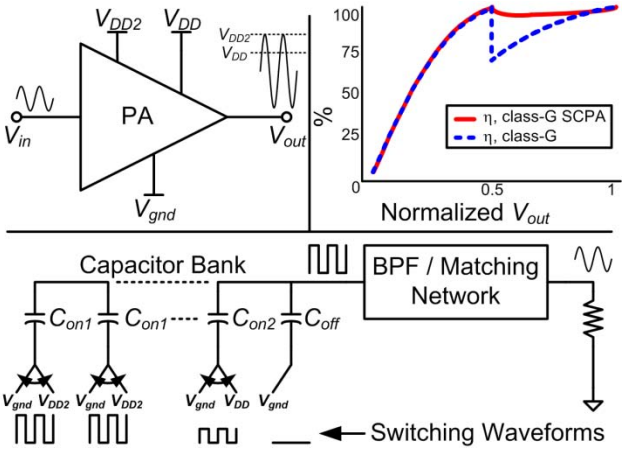


**Figure 1: Class-G SCPA with two supply voltages. Clockwise from top left: Conceptual class-G PA, comparison of ideal efficiencies for the conventional and SCPA versions, and an ideal implementation with ideal switches and capacitors.**

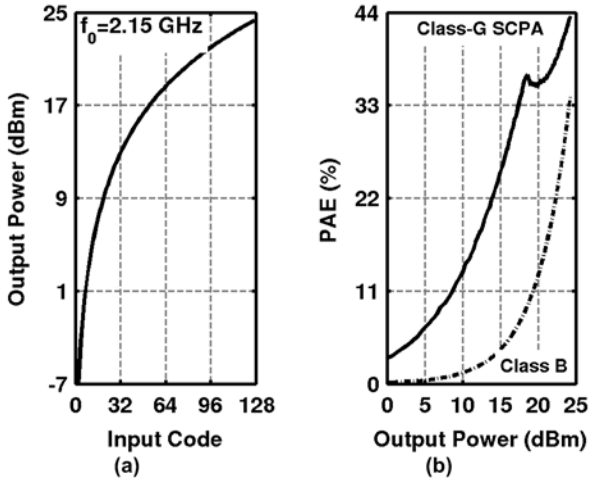


**Figure 2: (a) Measured output power vs. input code and (b) PAE vs. output power.**

**Keywords:** Power amplifiers, polar transmitters, EER, switched-capacitor circuits, power combining circuits

## INDUSTRY INTERACTIONS

Texas Instruments, Intel

## MAJOR PAPERS/PATENTS

[1] S. Sehajpal, et al., "Impact of switching glitches on class-G power amplifiers," IEEE Microwave and Wireless Components Letters, vol. 22, pp. 282-284, May 2012.

[2] S. Yoo, et al., "A class-G dual-supply switched-capacitor power amplifier in 65nm CMOS," *IEEE Radio Frequency Integrated Circuits Symp.*, pp. 233-236, 2012.

# TASK 1836.086 VARIATION TOLERANT CALIBRATION CIRCUITS FOR HIGH PERFORMANCE I/O

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## SIGNIFICANCE AND OBJECTIVES

Process variation degrades operation of analog subsystems and high performance I/O. While sources of process variation are well understood, methods to combat its effects are ad-hoc with power and area costs. This project explores circuit techniques to improve calibration of high performance I/O blocks at a reduced cost.

## TECHNICAL APPROACH

The first focus of this project is I-mode calibration DAC's with improved linearity. Two methods are demonstrated: adding redundant cells to reduce DNL and "ordered" cell selection to reduce INL. Low variation monitor circuits to measure and sort currents and a smaller second generation DAC cell are also developed. Finally, theoretical expressions are derived from ordered statistics to characterize each approach.

The second focus of this project is PI monitors. A novel time to digital converter using a stochastic source is explored in simulation. Next year the DAC will be completed and focus will move to design of PI monitor.

## SUMMARY OF RESULTS

A first generation 8 bit thermometer DAC was designed and tested to demonstrate the concepts of redundancy and reordering. The DAC cell contains an embedded memory cell to store a configuration bit, indicating if the current source in the cell is an "outlier" to be eliminated. An addressing scheme and decoder allow elimination of 2 cells per row. Measurement of currents in each cell and sorting is done off chip. Reordering of rows to reduce INL is also done off chip. Measured results for a set of first generation DAC's in a 65nm CMOS process indicate a baseline current variation of 18% and roughly 40% average improvement in INL and DNL over a simple DAC using the two techniques.

The DAC has since been redesigned to reduce area overhead and include measurement and sorting circuits. Cell redesign reduces the total area by ~85% from the first version. However, there is still a 3X area overhead required to store the configuration bit in the cell and enable addressing and sorting. This area could be used for a larger current source with lower variation. Figure 1 shows the DNL reduction that would result from a larger current source. The red star indicates the simulated DNL for the new DAC with two redundant cells per row. 40% improvement is still achieved considering equal area.

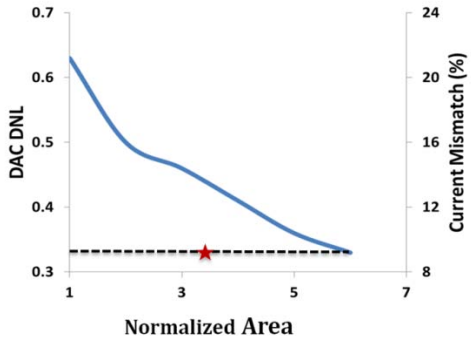


**Figure 1: DAC DNL for various sizes of PMOS I-source. The star indicates area of new DAC with two bits of redundancy per row.**

Current sorting and selection circuits have been designed and sent for fabrication. Sorting is done by selecting the median cell and comparing it via a high precision current comparator. Simulation indicates a good approximation to a mean comparison, with less than 4% error. Circuits have been sent for fab and will be tested upon return.

New theory has been developed to characterize the effect of redundancy and reordering on INL and DNL. Variances for the redundant DAC are calculated based on a truncated probability distribution and include the effects of row-wise sorting and selection. The reordering technique is characterized using ordered statistics. INL and DNL are calculated based on these variances. A paper has been submitted with these results.

Work has also begun on a novel PI monitor circuit based on a stochastic time-to-digital conversion technique. In the next year, circuits to demonstrate the concept will be designed, fabricated and tested.

**Keywords:** variation, DAC, INL, DNL, phase interpolator

## INDUSTRY INTERACTIONS

Intel, IBM

## MAJOR PAPERS/PATENTS

[1] M. Mukadam, I. Mukhopadhyay, R. Narayanan, F. O'Mahony, and A. B. Apsel, "Statistical Techniques to Reduce Non-linearity errors in Thermometer DACs," Electronics Letters (submitted).

# TASK ID# 1836.087, AN ANY-DATA-RATE REFERENCE-LESS DIGITAL CLOCK DATA RECOVERY WITH DECOUPLED JITTER TRANSFER AND JITTER TOLERANCE

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## SIGNIFICANCE AND OBJECTIVES

Clock-Date-Recovery (CDR) circuits are typically analog intensive, power consuming, occupying large silicon area, and requiring a reference clock. The objective of this project is to design a truly-digital reference-less CDR that can handle any data rate up to 16 Gb/s with small silicon area, low power and superior jitter performance.

## TECHNICAL APPROACH

Our CDR architecture employs a novel digital scheme where frequency acquisition and phase detection are performed in lower-speed digital domain, resulting in very low power dissipation and small silicon area. Using a wide-band DCO and wide-band phase interpolator (PI) along with a frequency locking loop (FLL), the architecture can accommodate data rate from hundreds of MHz to 16 GHz, and automatically detect and acquire the new data rate without the need for an external reference clock. In addition, the DPLL architecture can achieve superior jitter performance by decoupling jitter transfer from jitter tolerance without introducing jitter peaking.

## SUMMARY OF RESULTS

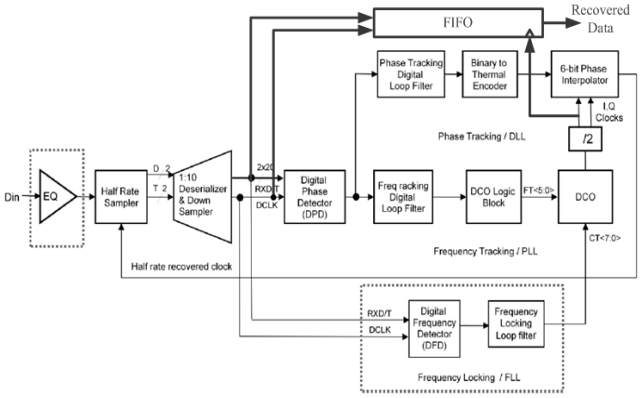
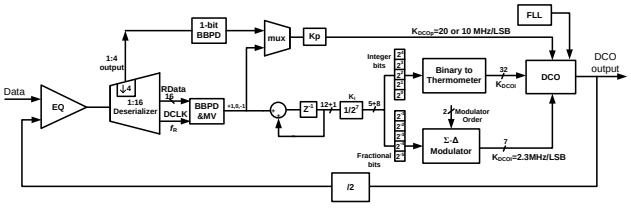
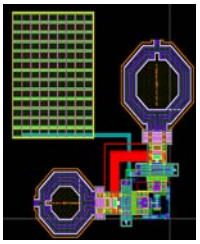


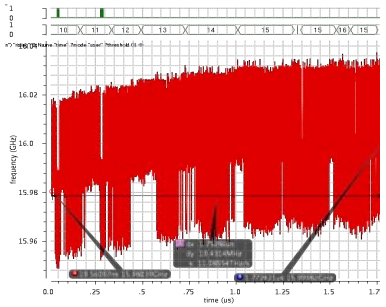

Figure 1: The DPLL-PI-based reference-less digital CDR.

Fig. 1 shows the PI-DPLL-based reference-less CDR architecture. It combines a digital PLL and a PI-based digital DLL for jitter tracking. The digital PLL is responsible for clock generation and slow jitter tracking while the DLL is used to track the high frequency jitter, and the JTRAN and JTOL bandwidths can be decoupled. Since March 2011 when the project started, we have completed the following: a) architecture study of the low-jitter any-data-rate digital CDR, b) schematic and layout of a 8-16 GHZ digital controlled oscillator (DCO) and a 4-8 GHz phase interpolator, c) development of a digital DCO-based PLL system with a reference-less FLL, and d) development of a PI-based DLL system. The silicon implementation using 65nm technology is ready for tape-out in Oct. 2012. Fig. 2 (a) depicts the DCO-based digital PLL subsystem and Fig. 2(b) the layout of the DCO with mutual-coupling inductive tuning for extended tuning range. Two inductive cores are employed to cover the frequency range of 8-16GHz. Fig. 2(c) shows the simulated CDR locking process for this simulation with an input data rate of 16 Gb/s and the applied input sinusoidal jitter of 0.8 UIpp @ 4MHz compared to the requirement of 0.15 UIpp @ 4 MHz (OC-192). The first waveform is the bit-error-rate (BER) detector output. When the output is zero, it means no error is detected. The middle waveform in Fig. 2(c) is the PLL integral path output. The PLL integral path determines the DCO average output frequency. As can be seen in the DCO output frequency (in red), it is approaching the input data rate.




(a)






(b) (c)

Figure 2: (a) Digital PLL architecture. b) DCO layout. (c) Simulated CDR locking process

**Keywords:** reference-less CDR, DCO, phase interpolation, jitter transfer, jitter tolerance

## INDUSTRY INTERACTIONS

Texas Instruments

# TASK 1836.088 EFFICIENT SWITCHING MODE DIGITAL-INTENSIVE WIRELESS TRANSMITTERS UTILIZING SWITCHING MODE PAS

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## SIGNIFICANCE AND OBJECTIVES

The efficiency of radio frequency transmitters and power amplifiers (PA) continues to pose a significant challenge in the design of battery-operated wireless communication systems as well as in base station applications. In this work we will investigate the use of switching power amplifiers and suitable modulation schemes for enhancing efficiency.

## TECHNICAL APPROACH

Two-level modulation schemes such as PWM are well suited for use with efficient switching power amplifiers. These schemes are inherently digital friendly and therefore can be implemented in low-cost CMOS technologies. A PWM based approach that relaxes the requirement for high quality reference signal generation will be employed as part of this work. High-speed Class-D switching PAs in CMOS will be utilized for enhancing efficiency. Minimization of in-band spurs is a key design goal. A passive external band-pass filter will be employed to reduce out-of-band spurs.

## SUMMARY OF RESULTS

A classical PWM generates its output by comparing the input to a ramp signal. This approach becomes progressively challenging as the bandwidth increases, as the ramp rate needs to be orders of magnitude higher than the signal bandwidth in order to ensure linearity. A modified feedback based PWM generator is utilized to achieve adequate bandwidth (Fig. 1).

A key issue in the use of switching modulation schemes for wireless applications arises from the high spurious content in these waveforms. When used in wireless applications, it is critical that the spurious products not corrupt the in-band signal. Based on simulations of the PWM generator and the digital upconverter, we have implemented a spectral planning scheme to avoid the appearance of in-band spurs. The approach relies on the proper selection of the PWM clock and the upconversion LO. In the time domain, this can lead to narrow pulses, when digitally up-converting the PWM signal due to asynchronous LO and PWM waveforms. This can degrade the noise floor and distortion performance, which can be recovered through the use of narrower channel length technologies.

Critical design challenges at the circuit level include the design of the upconversion mixer. This design needs to be sufficiently high speed to accommodate the sharp pulse edges generated by the modulation scheme. Another design that has been addressed is the IQ combiner at the outputs of the switching PAs. This design is required to combine two quadrature high-speed digital streams at the PA outputs. Critical requirements include quadrature accuracy of the combiner and its bandwidth. An LC network has been designed for this purpose.

The design has been simulated in a standard 130 nm CMOS process. With an LO frequency of 900MHz, and PWM switching frequency of 1.28GHz the peak efficiency reaches 35%. The driver amplifier (DA) is responsible for 41% of total power dissipation due to the fast switching and relatively large geometry of transistors. Fig. 2 shows the spectrum of a WCDMA signal at 9 dBm output power.

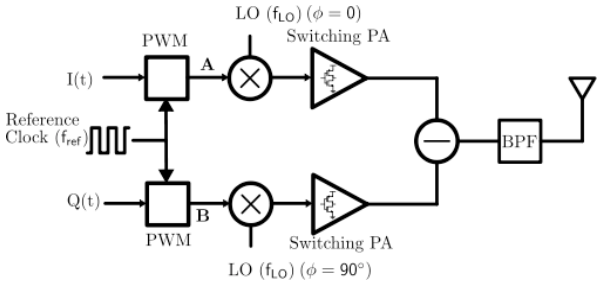


Figure 1: Architecture

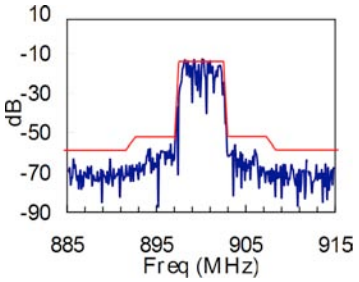


Figure 2: CDMA output spectrum

**Keywords:** PWM, digital modulation, wireless transmitters, switching mode PAs.

## INDUSTRY INTERACTIONS

Texas Instruments

# TASK 1836.089 ENERGY EFFICIENT COMPARATOR ELEMENTS FOR A/D CONVERTERS AND HIGH-SPEED I/Os

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VLADIMIR M. STOJANOVIC, MIT

## SIGNIFICANCE AND OBJECTIVES

This work addresses the problem of excess power dissipation in ADCs. We focus on the comparator as one of the key elements that needs to be optimized in order to achieve energy-efficient A/D conversion. Several factors influence power consumption of a comparator, such as supply voltage, input common-mode, input overdrive, and transistor sizing.

## TECHNICAL APPROACH

In order to optimize power of a comparator we have performed a series of characterizations. We have examined the effects of supply voltage, clock slope, transistor sizing, common-mode voltage, and input overdrive on comparator power, performance, and impulse sensitivity function (ISF) using HSPICE simulations. Power is linked to the two dimensional graphs characterizing speed of a comparator circuit for input common mode, overdrive, and supply voltage scaling. This helps to determine appropriate trade-offs in power while delivering specified performance level. A new set of equations for computing the effect of non-zero sampling aperture of a comparator on ADC resolution (ENOB) are derived.

## SUMMARY OF RESULTS

Sense-amplifier-based clocked comparators, namely Strong-Arm (SA), modified Strong-Arm (mSA), and the double tail sense amplifier (Schinkel), are characterized. The characterization framework is developed in HSPICE. The TT setting of IBM 45nm SOI technology is used in simulations. The nominal settings of the characterization environment are: $V_{dd}$=1V, Temp=25C, $V_{cm}$=0.75V, $\Delta V_{in}$= 50mV, $C_{load}$=10fF. The sampling clock frequency is 1GHz.

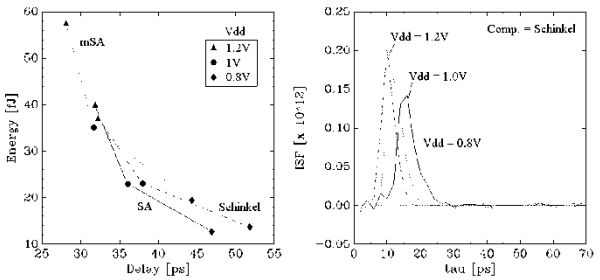


**Figure 1: Effect of supply voltage ($V_{dd}$) scaling on comparator energy, delay, and ISF.**

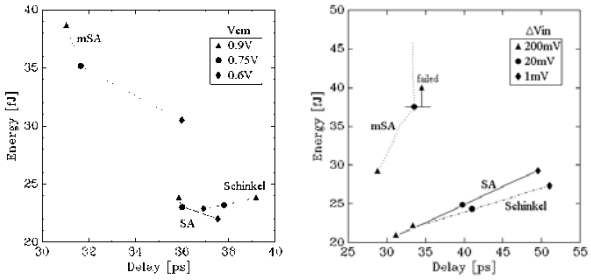


**Figure 2: Effects of common-mode voltage ($V_{cm}$) and input overdrive ($\Delta V_{in}$) scaling on comparator energy and delay.**

Transistors in the comparator circuits are sized to achieve minimal EDP for the nominal settings. The optimal selection of the comparator depends on the operating voltage. Similarly, both energy and delay increase when overdrive voltage is decreased.

Non-ideal sampling in an ADC is caused by comparator aperture and clock jitter. The aperture model takes into account the fact that the sampling pulse is not an ideal Dirac delta of zero width, rather a non-zero time resolution window. Clock jitter appears when the sampling pulses have uneven interspacing. We have derived equations for the calculation of ENOB for a given sampling aperture and rms jitter. ENOB vs. sampling aperture and clock jitter for sampling frequencies of 1GHz and 5GHz obtained using derived equations are shown in Fig. 3.

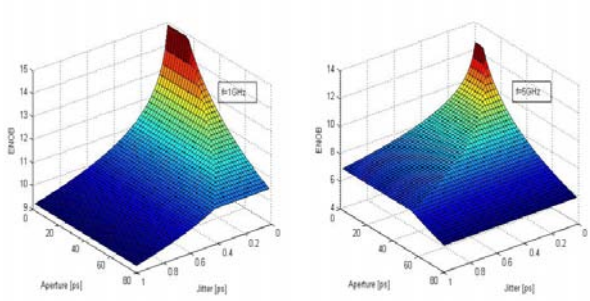


**Figure 3: ENOB vs. sampling aperture width and clock jitter for sampling frequencies of 1GHz and 5GHz.**

**Keywords:** ADC, low power design, clocked comparator

## INDUSTRY INTERACTIONS

IBM, Texas Instruments, Intel

# TASK 1836.092 A MODEL-VIEW-CONTROLLER (MVC) PLATFORM FOR ADAPTIVE TEST

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## SIGNIFICANCE AND OBJECTIVES

Adaptive test is an emerging approach to dynamically modify the test plan for RF devices with high specificity: per wafer or per device. This project will develop a model view controller (MVC) framework and statistical learning theory/machine learning methods necessary to support industrial adaptive test.

## TECHNICAL APPROACH

We are architecting an adaptive test MVC framework with: (i) Models, which will serve as abstractions of existing industry production databases, (ii) Views, which will provide test engineers feedback on adaptive test algorithms, and (iii) Controllers, which will contain modular adaptive test components to be employed at each stage of testing. We anticipate treating these adaptive test components as "applications", which consist of algorithms for each stage of data collection and processing (inline/kerf, wafer final test, module final test, field returns, etc.). By standardizing the controller platform we can encourage the emergence of an adaptive test "application ecosystem", simplifying deployment.

## SUMMARY OF RESULTS

There is growing industrial interest in deploying so-called “adaptive test”, or dynamically modifying the test plan. Adaptive test is particularly challenging for analog and RF testing, where testing is already a complicated and expensive endeavor. In this project, we posit that achieving meaningful results for adaptive test in the analog and RF test domain will require statistical models that are at parity of sophistication with the complexity of the test problem. To address this, we develop a model-view-controller architecture that responds to the challenges of adaptive test for analog and RF devices with an elegant and modular solution, enabling rapid deployment of novel statistical methods as they become available, while keeping test engineers informed about the inner workings of the deployed adaptive test system.

Within this MVC framework, we have developed a Gaussian process model-based methodology for generating spatial estimates of sparsely sampled e-test and probe parameters across the surface of wafers, as depicted in Figure 1. The highly accurate estimates generated by our Gaussian process models enable extraction of per-die estimates of these parameters.

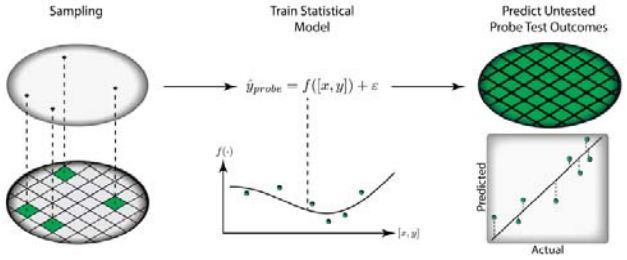


**Figure 1: Spatial Estimation Methodology**

For e-test parameters, our Gaussian process model is able to generate extremely accurate predictions in an experiment involving more than 8,000 HVM wafers. For 90% of the parameters, the Gaussian process model-based methodology demonstrates less than 4% error, and for the majority of the parameters the prediction error is much lower. Additionally, our Gaussian process model-based approach consistently outperforms Virtual Probe, on average by 0.5%, and in certain cases, by a significant margin of almost 5%, while requiring an order of magnitude less runtime to evaluate on each wafer.

Similar results are obtained for probe test parameter predictions, enabling dramatically reduced probe test cost for RF devices. By sparsely sampling probe tests and extrapolating to untested die locations, our proposed methodology avoids dense application of costly probe tests. As demonstrated on more than 3,000 HVM manufacturing wafers, the proposed methodology requires only a very small sample (on the order of 1%) of die on each wafer to construct highly accurate spatial interpolation models. Despite this sparse sampling, a mean prediction error of less than 2% is achieved, an order of magnitude lower than the state-of-the-art.

**Keywords:** analog/RF, adaptive test, test metric estimation, machine learning, spatial correlation models

## INDUSTRY INTERACTIONS

Texas Instruments, IBM

## MAJOR PAPERS/PATENTS

[1] N. Kupp et. al. “Spatial Correlation Modeling for Probe Test Cost Reduction in RF Devices,” ICCAD, 2012.

[2] N. Kupp et. al. “Spatial Estimation of Wafer Measurement Parameters Using Gaussian Process Models,” ITC, 2012.

[3] N. Kupp et al, “Applying the Model-View-Controller Paradigm to Adaptive Test,” IEEE Design and Test of Computers, vol. 29, no. 1, pp. 28-35, 2012.

# TASK 1836.093 VARIABILITY-AWARE, DISCRETE OPTIMIZATION FOR ANALOG CIRCUITS

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## SIGNIFICANCE AND OBJECTIVES

While analog circuit optimizers that can automatically size transistors in a circuit according to a prescribed performance metric can be an effective productivity tool for analog, the reality is that their adoption into the mainstream flows has been rather slow. Exploiting the inherent uncertainty in the IC process, this task aims to explore the use of discrete optimization techniques for realizing a fast, deterministic optimizer that can perform quick, incremental 'what-if' analysis.

## TECHNICAL APPROACH

While analog design parameters are typically of continuous values, we assert that such a continuous design space can be effectively covered with a set of finite, coarsely-spaced, discrete points by exploiting the inherent variability in the IC technology. Our expectation is that a discrete optimizer can solve many of the problems faced with the existing, continuous optimizers for analog circuits.

In particular, the task is focused on three aspects of applying the discrete optimization to analog circuit synthesis: discretizing a continuous design space, searching for better design candidates, and comparing the statistical quality (e.g. yield) between the design candidates.

## SUMMARY OF RESULTS

The feasibility and effectiveness of a discrete optimizer for sizing analog circuits has been demonstrated with the first prototype tool. The use of discrete grids to cover the continuous design space in presence of variability has been justified by a formal analysis and new algorithms to address three aspects of a discrete optimization tool for analog circuits have been developed.

First, an isotropic discrete grid named "Polka-Dot" is proposed that places the discrete points with equal distances to the nearest neighbors. The number of nearest neighbors also midly scales with the dimension.

Second, when performing the local search, only a randomly selected candidate among the nearest neighbors is examined for performance improvement rather than the whole neighbors, saving computational costs while still reaching convergence.

Third, when comparing two design candidates, the Monte-Carlo samples for statistical analysis are added in an incremental fashion to minimize the computational cost of yield-aware optimization.

The feasibility of the proposed optimization algorithm has been demonstrated on a digitally-controlled oscillator (DCO) example. The optimal solution that finds the balance between the resolution, linearity, phase noise, and power dissipation was found with low computation costs.

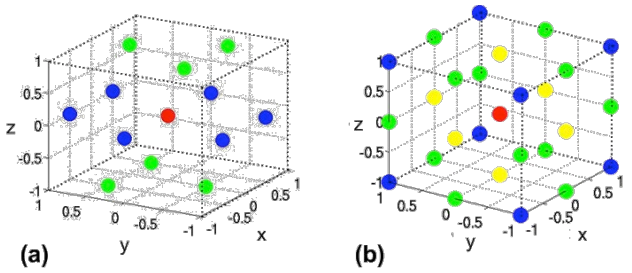


**Figure 1: (a) The proposed isotropic grid named "Polka-Dot" in comparison with (b) the classical Cartesian grid.**

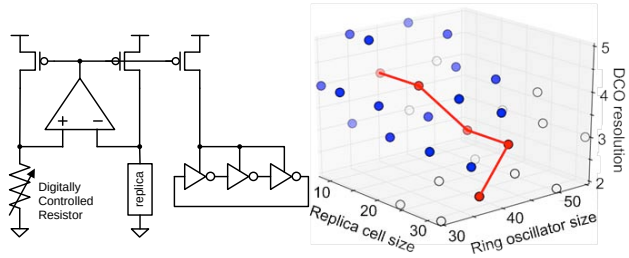


**Figure 2: Optimization of a digitally-controlled oscillator (DCO) using the proposed algorithm. The yield-aware optimum is found after 250 Monte-Carlo sample runs, which is only 20 runs in average for each design point.**

**Keywords:** analog circuit synthesis, circuit optimization, discrete optimization, yield-aware optimization, statistical comparison.

## INDUSTRY INTERACTIONS

Texas Instruments, Intel

## MAJOR PAPERS/PATENTS

[1] S. Jung, S. Youn, J. Kim, "Analysis on Performance Controllability under Process Variability: A Step Towards Grid-Based Analog Circuit Optimizers," Frontiers in Analog Circuit Synthesis and Verification (FAC), July 2011.

[2] S. Jung, Y. Choi, J. Kim, "Variability-Aware, Discrete Optimization for Analog Circuits," ACM/IEEE Design Automation Conference (DAC), June 2012.

# TASK 1836.094 ACCURATE FSM APPROXIMATIONS OF ANALOG/RF SYSTEMS FOR DEBUGGING MIXED-SIGNAL DESIGNS

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ROBERT BRAYTON, UC BERKELEY

## SIGNIFICANCE AND OBJECTIVES

This project aims to develop tools, techniques, and algorithms to automatically produce discrete-time logical abstractions (Finite State Machines, or FSMs) that accurately capture the SPICE-level I/O behavior of continuous-time analog/mixed-signal circuits. Such abstractions will enable efficient analysis, simulation, design, validation, and debugging of analog/mixed-signal systems, using the powerful, FSM-based framework that has already been developed for digital design.

## TECHNICAL APPROACH

Our core technique for FSM abstraction of continuous systems, dubbed DAE2FSM, is based on Angluin's algorithm from computational learning theory. We have adapted this algorithm to learn Mealy machine representations of SPICE-level circuits, with the goal to faithfully mimic the I/O trajectories of the underlying continuous system. One of our key technical contributions is to extend the approach to learn FSMs with arbitrary input and output alphabets, which enables us to finely discretize the circuit's underlying waveforms, and also to handle multi-input, multi-output circuits. We are also working to develop algorithmic refinements of this technique for composing individual FSMs to realize functional abstractions of larger designs. The approaches we are investigating include multi-level discretized hierarchical FSM construction, branch and bound state space pruning and exploration, lookup table based FSM generation, and others.

## SUMMARY OF RESULTS

We have applied the DAE2FSM technique to SPICE-level deep sub-micron (i.e., 22nm) digital building blocks like latches, flip-flops, and circuits constructed from them. The FSMs so generated are able to capture not only the intended digital functionality of such systems, but also the underlying analog dynamics responsible for circuit failures and deviations from ideal functionality.

For example, Fig. 1 illustrates the application of DAE2FSM to 22nm D flip-flops exhibiting different failure modes when clocked aggressively. In the first mode (top half of the figure), the flip-flop is unable to register the bit "1" applied as a single pulse, but registers the bit when two or more consecutive "1"s are applied (as seen from the SPICE-simulated blue output waveform corresponding to the green input signal). This behavior is captured by the auto-generated binary FSM produced by our technique for this circuit. The second failure mode (bottom half of Fig. 1) results in intermediate levels in the SPICE-simulated output, which are captured by the multi-level FSM abstraction produced by our technique.

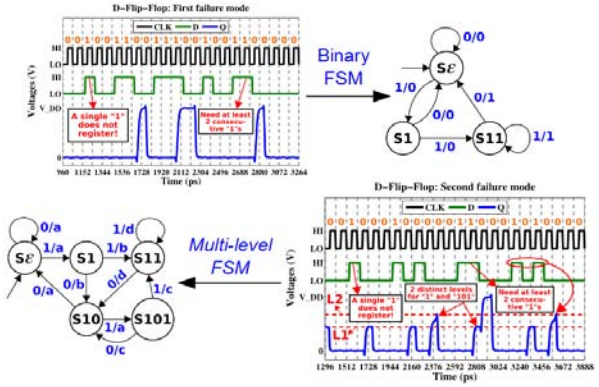


**Figure 1: Automatically generated binary and multi-level FSMs that capture failure modes in D flip-flops.**

In the coming year, we expect to refine and extend our algorithm to produce inter-composable FSM abstractions representing the SPICE-level I/O behavior of much larger designs - digital, analog, and mixed-signal. We also anticipate the development of new techniques for representing lookup table I/O data in FSM form, which will in turn enable formal methods of analysis for circuit-level validation, property checking, and debugging.

**Keywords:** finite state machines, analog/mixed-signal design, continuous behavioral modeling, SPICE-accurate simulation, circuit analysis, validation, debugging

## INDUSTRY INTERACTIONS

Intel, Freescale Semiconductor, Texas Instruments

## MAJOR PAPERS/PATENTS

[1] Aadithya and Roychowdhury, "Automatic Generation of Accurate Discrete-Time Logical Abstractions of Continuous-Time Circuit Dynamics," DAC, June 2012, San Francisco, Calif.

[2] Aadithya et al., "A Fully Automatic Technique for Constructing FSM Abstractions of Non-Ideal Latches in Communication Systems", ICASSP, March 2012, Kyoto, Japan.

[3] Gu and Roychowdhury, "FSM Model Abstraction of Analog/Mixed-Signal Circuits by Learning from I/O Trajectories," ASP-DAC, Yokohama, Japan, Jan. 2011.

# TASK 1836.096 MIXED-SIGNAL DESIGN CENTERING IN DEEPLY-SCALED TECHNOLOGIES

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## SIGNIFICANCE AND OBJECTIVES

A design methodology for robust design of high-performance analog circuit blocks in highly-scaled technologies is being investigated that will enable rapid yield ramp-up.

## TECHNICAL APPROACH

We are developing a methodology that enables centering with respect to technology variability of high-performance mixed-signal signal designs in as few as one design iteration. It is based on the components, which are developed simultaneously:

- Instrumenting critical design components to accurately monitor impact of process variability on their performance.
- Creating a dedicated set of representative circuit primitives for their full variability characterization.
- Extracting a variability model from the test structures; building simplified Spice models to predict the distribution spread of critical components.

These components enable centering of critical analog blocks, such as clock and data recovery loops and high-performance data converters.

## SUMMARY OF RESULTS

We are developing a design methodology that addresses variability at all levels. This is being accomplished by developing yield-aware optimization tools targeting critical analog circuit designs, and by relying on extraction and modeling of manufacturability requirements specific to the target design.

The methodology is based on variability characterization by using representative test structures and building blocks to hierarchically capture variability and propagate distributions from devices, via components to systems. The approach involves selection of representative critical analog components, the design of transistor and component arrays in a characterization run, and backward propagation of performance data and its variability across the levels of hierarchy.

The approach is illustrated on a yield optimization of a high-performance clock-and-data-recovery (CDR) loop, Fig. 1.a, to achieve high datarates. Comparator is a key component in the loop, which we are characterizing using impulse-sensitivity function (ISF), Fig. 1.b.

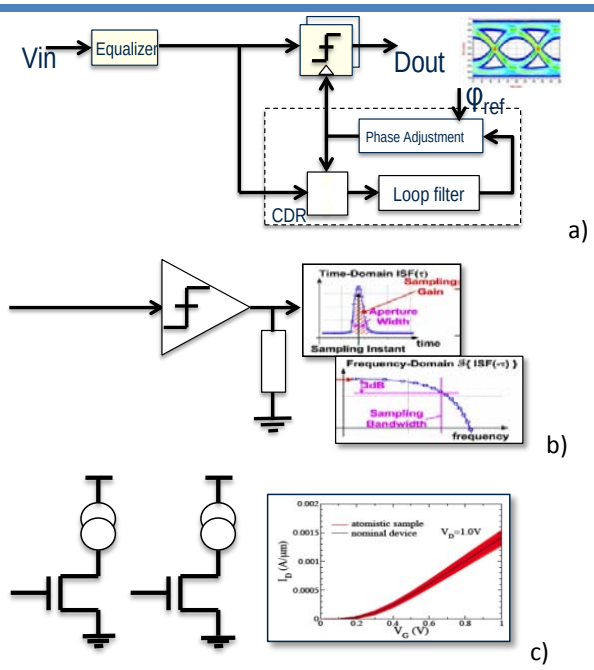


**Figure 1: Illustration of the characterization approach a) Block diagram of a CDR b) Impulse-sensitivity function of a comparator c) device-level I-V characteristics**

Measured variability in ISF is being related to the variability measured by I-V sweeps of individual devices, Fig. 1.c, via backward variability propagation.

A preliminary simulation of variability of the ISF of a comparator, in response to +/-1% and +/-5% variation is flat-band voltage is shown in Fig. 2.

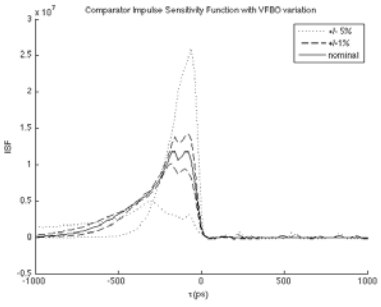


**Figure 2: Variation of ISF in response to the variation in flat-band voltage.**

**Keywords:** CMOS, variability, yield, design optimization, clock and data recovery

## INDUSTRY INTERACTIONS

Intel

# 1836.097 DUAL-DOMAIN SAR ADCS INCORPORATING BOTH VOLTAGE AND TIME INFORMATION

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## SIGNIFICANCE AND OBJECTIVES

Typical SAR ADCs only utilize quantizer binary digital outputs to switch the DAC and change state, limiting the optimal efficiency of the structures. The techniques presented in this summary offer ways to improve efficiency and resolution by utilizing time and statistical information.

## TECHNICAL APPROACH

The resolution and efficiency improving techniques are implemented in a prototype Ternary SAR (TSAR) IC. The TSAR structure examines the time delay of the voltage comparator used to give the input polarity and uses that information to create an optimized switching algorithm, half-bit redundancy, and speed improvements. Residue shaping is also investigated which is the ability to extract extra resolution from a given stage redundant ADC due to the changing statistics of each stage and is present in the TSAR structure.

## SUMMARY OF RESULTS

The TSAR ADC has been implemented by placing a time comparator after the typical voltage comparator block [1]. Since the delay of the voltage comparator varies linearly with the given input voltage, the delay gives information about the magnitude of the input and a third level can be determined for small signals in addition to the positive and negative codes present in the binary SAR.

The three level quantizer allows for an optimized switching algorithm and reduced DAC driver activity due to the presence of a no switching region. Also, redundancy and residue shaping are present with no additional stages or sub-radix arrays. Finally, the conversion speed and number of average SAR cycles are improved due to the reduction of early stage comparator delays and TSAR stage skipping. The fabricated prototype in 0.13uM CMOS achieves a figure of merit (FOM) of 10fJ/CS at 8 MHZ and 10b accuracy. The architecture is shown to reduce DAC switching and driver power by about 60% and comparator power by 20%. Also, a 10b operation can be implemented with a max of 9 cycles and an average of 8.02 cycles. Further research includes looking at multi-stage feedback in TSAR structures to further optimize efficiency and optimizing the efficiency of SARs with three-level DACs, but only binary quantizers.

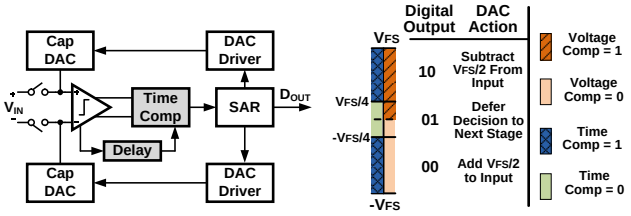


Figure 1: The Ternary SAR (TSAR) structure and stage output

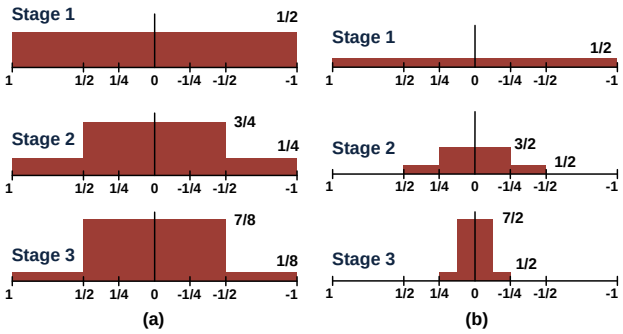


Figure 2: Residue shaping for an (a) pipeline and (b) TSAR ADC

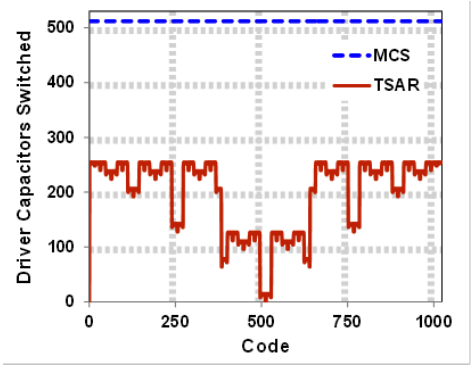


Figure 3: TSAR DAC driver activity compared to the MCS SAR

Table 1: Performance Summary

| | VDD | ENOB | BW | Power | Area |
|---|---|---|---|---|---|
| TSAR | 0.8V | 9.87b | 8MHz | 75uW | .056mm$^2$ |

**Keywords:** Ternary SAR, residue shaping, time comparator, SAR energy, SAR ADC

## INDUSTRY INTERACTIONS

Texas Instruments, Intel

## MAJOR PAPERS/PATENTS

[1] J. Guerber, M. Gande, H. Venkatram, A. Waters, and U. Moon, "A 10b ternary SAR ADC with decision time quantization based redundancy," *ASSCC,* Nov. 2011.

# TASK 1836.099 MODELING OF ANALOG AND SWITCHING CIRCUITS

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## SIGNIFICANCE AND OBJECTIVES

Current methods of simulating analog and switching circuits together are time consuming, and faster modeling methods are required. The objective of this project is to create a method of model creation that reduces modeling efforts to only a few hours or less and simulation time from days to minutes.

## TECHNICAL APPROACH

Switching circuits, such as many common power converter topologies, can take a long time for Spice-like tools to simulate due to the near instantaneous changes introduced by the switches. An *averaged* modeling method is being investigated where the switching element is averaged over time and thereby linearized. Simulations proceed much more quickly (seconds/minutes versus hours). Novelty in this work will arise from a new duty cycle expression synthesis enabling time and frequency domain simulations. Model generation will be automated such that it can be easily generated from a data sheet, measured data or netlist in a reasonable amount of time.

## SUMMARY OF RESULTS

While averaged modeling is not a new technique, the proposed method introduces two novel aspects to make the approach more viable and accurate. First, the proposed method models the feedback paths from the output to the switching element using small-signal transfer functions in addition to the large-signal expressions commonly used to derive PWM relations. Second, the approach is designed to be *automated* such that the model can be generated from a datasheet, measured data or a circuit netlist. This approach will reduce the amount of effort required to produce the model by orders of magnitude as compared to state-of-the-art approaches. To reach this goal, the initial period of the research has focused in two areas: exploration of existing modeling approaches for modeling the feedback paths in switching converters, and design of the overall automated technique to be subsequently implemented.

There are many approaches to reduced-order models of complex linear and switching circuits, including behavioral modeling (top-down modeling) and purely mathematical model order reduction approaches (symbolic modeling, state-space averaging). For switching converters, these approaches have been previously applied successfully; however each suffers from at least one major drawback. Mathematical approaches quickly become intractable when modeled by hand, and are difficult to automate with limited gains in simulation performance. Behavioral modeling, particularly when hand-coded, can give an order of magnitude gain in simulation time, but often at a high cost in modeling effort. In switching circuits, the problem is compounded further as the circuits are also truly mixed-signal in behavior. Averaging methods including discrete time averaging (DTA) and PWM switch averaging (PSA) move the problem wholly into either the discrete or continuous domain. As the target for a switching converter model is in an analog simulator, the method proposed is based upon the PSA method.

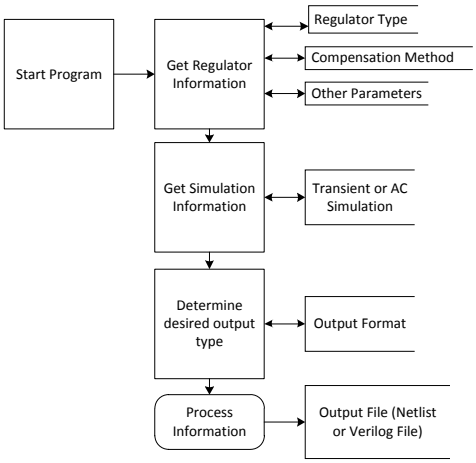


**Figure 1: PWM switch model generation tool flow chart.**

The flow of the tool developed is given in Fig. 1. The tool operates on various inputs that can be collected from data sheets, measurements, or circuit simulations of a transistor-level netlist. Using the given data, the tool uses a template-based approach to identify the proper feedback and compensation techniques to employ and generates an averaged model in either PSpice or Verilog-A format. This facilitates both system-level and chip-level design and verification tasks.

**Students/Post-docs:** Rui Mao, Michael Leonard, Matt Francis (Post-Doc) **Keywords:** behavioral modeling, averaged modeling, automated modeling

## INDUSTRY INTERACTIONS

Texas Instruments, Intel

# TASK 1836.100 TEST TECHNIQUES AND FAULT MODELING FOR HIGH VOLTAGE DEVICES AND BOARDS

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## SIGNIFICANCE AND OBJECTIVES

High-Voltage testing is expensive and test measurements are extremely difficult due to low magnitude of output response subdued by power supply and tester noise. To overcome these test challenges we will develop fault models, modify existing load boards to accommodate HV discharge problems and provide low-cost test techniques for HV-LDMOS.

## TECHNICAL APPROACH

Lateral DMOS transistors are used as output drivers in numerous applications from smart phones to motor drives. We will develop fault models of high-voltage devices for defects by starting with electrical modeling of LDMOS, induce physical defects in it, and incorporate it in a low-cost fault model based test technique. Our approach is to use the fault models we develop to perform test simulation where the results will be stored in a fault dictionary and compare with ATE test results. Finally, we automate the entire test procedure using previously developed RADPro tool and perform component-level diagnostics in high-voltage DIBs.

## SUMMARY OF RESULTS

High-Voltage (HV) production automated test equipment (ATE) is expensive and it provides multisite testing for high throughput. However, the test throughput could be dramatically reduced due to long charging or discharging effects of the ATE, DIB and the DUT resulting in high test cost. To overcome some of the limitations we have developed a novel fault model based test technique which limits the test suit to a couple of HV measurements and still have fairly sufficient test coverage. Using the statistical data obtained from production floor testing the most commonly found structural defects are gate-FOX short, post-breakdown thermal stress, and drain-leakage. We developed fault models for these structural defects by inducing its physical behavior as parasitic elements in the hybrid MOS-pi model of HV-LDMOS. HV-LDMOS testing involves conventional breakdown and leakage tests. In HV-LDMOS the test measurements are of extremely low magnitude. Coupled with the large charging and discharging time of the ATE and power supply noise it is very difficult to make accurate test measurements. We developed a novel test technique where in the dc stimulus is chopped to a relatively higher frequency using the ATE clock pulse and provided to the DUT. The DUT response is processed using a lock-in amplifier on a software platform for demodulating the response and retrieving the dc value of the test measurement.

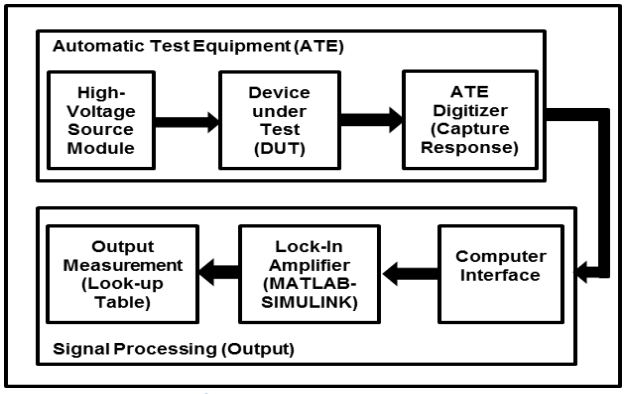


**Figure 1: Test setup for high-voltage LDMOS.**

Test simulation was performed for a 700 V driver IC and the results are shown in Table 1.

**Table 1: Test simulation results for high-voltage LDMOS**

| Test Condition | DUT Specifications | Gain |
|---|---|---|
| Fault Free | 5 mA (10 V, 200 V) | -6.521 |
| Soft-Breakdown | 2 nA (17 V, 0 V) | -1.861 |
| Hard-Breakdown | 2 nA (20 V, 0 V) | -0.537 |
| Thermal Stress (120 $^0$C) | 5 mA (10 V, 200 V) | -4.167 |
| Drain Leakage ($I_{dl}$ = 5 nA) | 5 nA (0 V, 200 V) | -9.784 u |

As part of future work we will develop a prototype test board for implementing this test technique and also work on alternate test techniques for testing high-voltage LDMOS using low-voltage signals.

**Keywords:** Lateral DMOS, Quasi-saturation Effect, RESURF Effect, Structural Defects, Fault Modeling.

## INDUSTRY INTERACTIONS

Texas Instruments Inc.

## MAJOR PAPERS/PATENTS

[1] S. Kannan et al., "Development of Scalable Electrical Model for High-Voltage LDMOS," IEEE IPEMC-ECCE, 2012.
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# TASK 1836.107 VERIFICATION OF MULTI-STATE VULNERABLE AMS CIRCUITS

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DEGANG CHEN, IOWA STATE UNIVERSITY

## SIGNIFICANCE AND OBJECTIVES

Many basic analog circuits inherently possess undesired (Trojan) stable equilibrium points. The objective is to develop a systematic procedure that detects presence or absence of multiple equilibrium points in basic AMS circuits and to develop a verification process that verifies a designer's Trojan removal circuits are effective over PVT variations.

## TECHNICAL APPROACH

Initially, in conjunction with SRC member companies, a class of basic single loop (single-input/single-output (SISO)) circuits that are known to possess multiple stable equilibrium points will be identified. These circuits will serve as a first benchmark. In parallel, a computationally practical contraction algorithm from the nonlinear controls community in conjunction with homotopy/continuation methods will be adapted to determine the presence or absence of multiple stable equilibrium points in SISO circuits. In the next phase, the same approach will be followed for identifying and eliminating Trojan states in circuits with multiple-inputs/multiple-outputs (MMO) when the loop is broken.

## SUMMARY OF RESULTS

Basic bias generators, voltage and current references, and temperature sensors often have Trojan equilibrium states. Trojan State Elimination (TSE) circuits, often termed "start-up" circuits, are used to eliminate the undesired Trojan states. But, on occasion, the Trojan operating states are missed through the design and verification process or the TSE circuit is ineffective under certain conditions thereby causing failure of the circuit. A systematic method for pre-silicon verification that neither happens is necessary to eliminate these two scenarios.

One of the many such circuits that serves as both a bias generator and a temperature sensor is the inverse-Widlar structure shown in Fig. 1. By breaking the loop at the gate of $M_5$, the circuit is recognized as the cascade of two inverters with operating points on the $V_{OUT}$=$V_{IN}$ line. The transfer characteristics of the open-loop structure are shown in Fig. 2 along with a stable Trojan operating point. The TSE circuit must be designed so that the Trojan Operating Point is removed over PVT variations. Transient simulations are often used to verify effectiveness of "start-up" circuits but do not guarantee Trojan states have been eliminated. The open-loop continuation/homotopy method can be used to verify that a TSE circuit is effective at removing Trojan operating points over PVT variations.

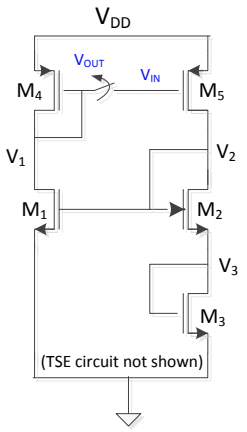


**Figure 1: Basic inverse-Widlar temperature sensor.**

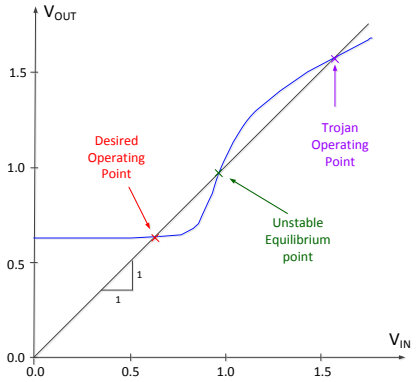


**Figure 2: Transfer characteristics of open-loop structure.**

A detailed discussion of how robustness of TSE circuits to PVT variations is achieved with the open-loop homotopy method is presented in [1]. Simulation results for a temperature sensor designed in a 0.18µm CMOS process show a TSE circuit is effective at eliminating Trojan states over PVT variations.

**Keywords**: analog verification, start-up circuits, Trojan states, homotopy, bias generators

## INDUSTRY INTERACTIONS

Intel, Texas Instruments, Freescale, AMD

## MAJOR PAPERS/PATENTS

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## APPENDIX I, TEXAS ANALOG CENTER OF EXCELLENCE FACILITY

The University of Texas at Dallas (UT Dallas) has prepared a ~8,000 $ft^2$ area on the third floor of the Engineering and Computer Science North Building to form an enhanced centralized group of laboratories dedicated to analog engineering research and research training. Figure I.1 is a 3D sketch of the facility. The facility includes RF and THz, Integrated System Design, Embedded Signal Processing, and Analog & Mixed Signal laboratories, as well as a CAD/Design laboratory structured to promote collaborative research**.** Figure I.2 presents the facility floor plan showing the dimensions of each laboratory.

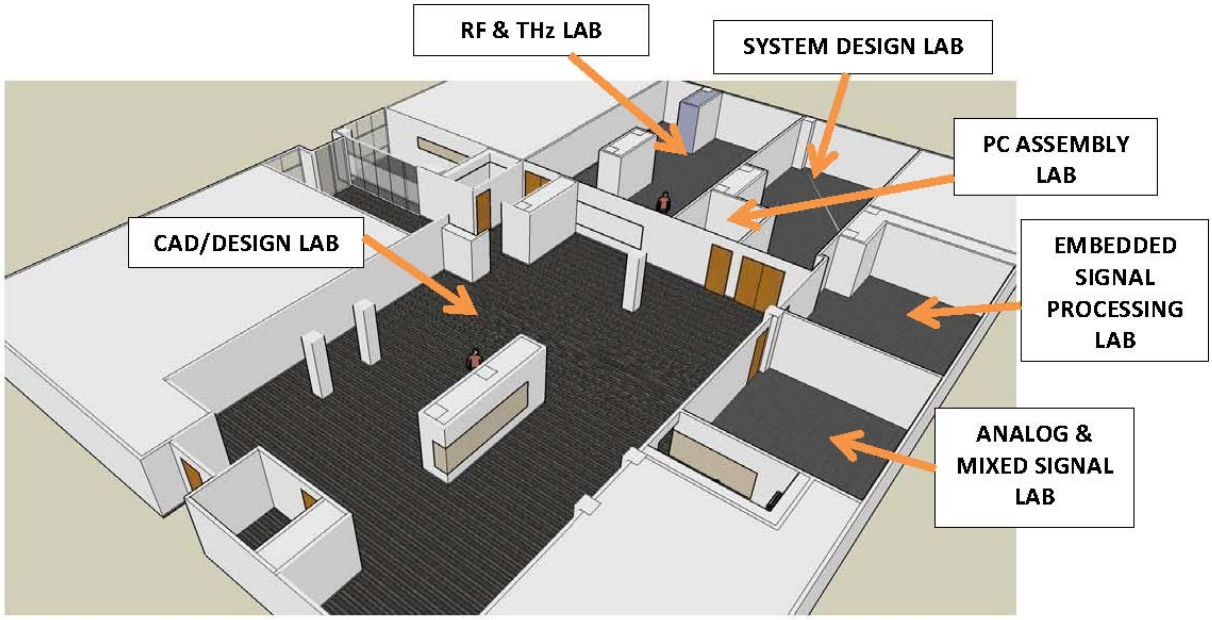


**Figure I.1: TxACE Analog Research Facility Sketch**

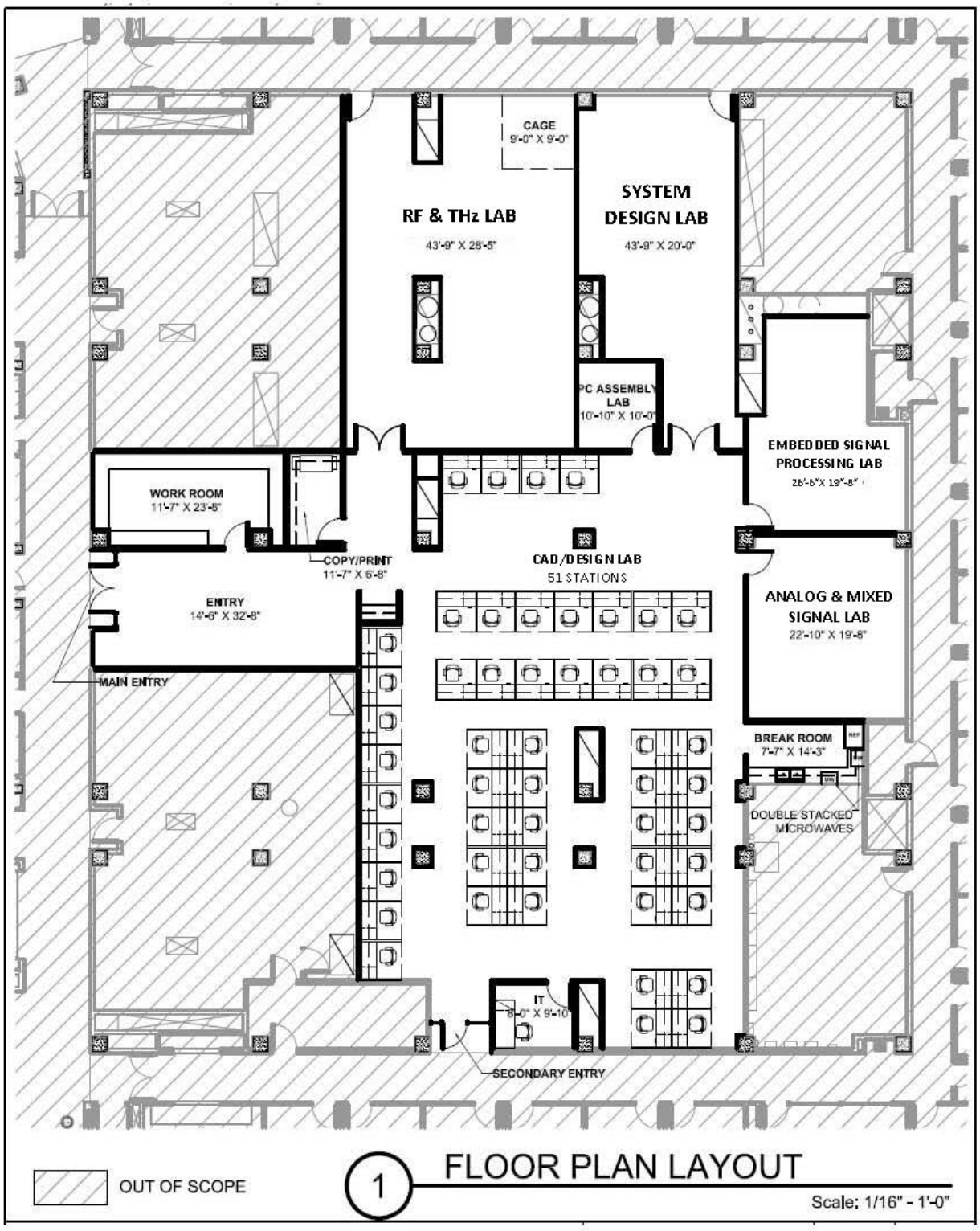


**Figure I.2: TxACE Analog Research Facility Floor Plan**

## APPENDIX II, PUBLICATIONS OF TXACE RESEARCHERS

### Conference Publications

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