TEXAS ANALOG CENTER OF EXCELLENCE

ERIK JONSSON SCHOOL OF ENGINEERING AND COMPUTER SCIENCE

Annual Report 2019 – 2020

SRC®

TxACE TEXAS ANALOG CENTER OF EXCELLENCE

UT DALLAS The University of Texas at Dallas

TxACE MISSION

The Texas Analog Center of Excellence seeks to create fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, health care, and public safety and security.

TxACE THRUSTS

- *Safety, Security and Health Care*
- *Energy Efficiency*
- *Fundamental Analog Circuits*

TxACE 2019–2020 ANNUAL REPORT

The Texas Analog Center of Excellence (TxACE), located at the University of Texas at Dallas is the largest analog research center based in an academic institution. Analog and mixed signal integrated circuits engineering is both a major opportunity and challenge. Analog circuitry is a critical component of the majority of products for the $400+ billion per year integrated circuits industry, as a part of sensing, actuation, communication, power management and others. Digital integrated circuits such as microprocessors, logic circuits and memories are now integrating analog functions such as input/output circuits, phase locked loops, temperature sensors and power management circuits. It is also common to find microcontrollers with multiple analog-to-digital and digital-to-analog converters. These circuitries impact almost all aspect of modern life: safety security, health care, transportation, energy, entertainment and others.

Creation of advanced analog and mixed signal circuits and systems depends on the availability of engineering talent for analog research and development. TxACE was established to help translate the opportunity into economic benefits by overcoming the challenge and meeting the need. TxACE was established through a collaboration of the state of Texas, Texas Instruments, the Semiconductor Research Corporation, the University of Texas System, and The University of Texas at Dallas.

The research tasks are organized into three research thrust areas: Safety, Security and Health Care, Energy Efficiency and Fundamental Analog. The scope of investigation extends from circuits operating at dc through terahertz, data converters that sample at a few samples/sec to 10's of Giga-samples/sec, AC-to-DC and DC-to-AC converters working at µW to Watts, energy harvesting circuits, sensors and many more. Significant improvements to existing mixed signal systems and new applications have been made and continued to be anticipated. Students who have been exposed to hands-on innovative research are forming the leading edge of analog talent flow into the industry. Close collaboration with and responsiveness to industry needs provide focus to the educational experience.

DIRECTOR'S MESSAGE

The Texas Analog Center of Excellence (TxACE) is leading analog research and education. During this year of COVID-19, it has become evident how important the efforts of the Center are. Can you imagine, what our life would have been like, if the pandemic happened 10 years ago? The technologies that the center has helped to create have become the necessary means for saving the civilization during this time. We are privileged to be able to contribute toward this.

It is my pleasure to report that the Center despite the disruption is making excellent progress toward accomplishing our mission. The Center funded 74 research tasks led by 63 principal investigators at 31 institutions, including four international universities. The Center supported 203 graduate and undergraduate students.

Over the past year, TxACE researchers published 29 journal and 48 conference papers. We also filed 5 patent applications and 2 invention disclosures, and were granted 2 patents. Twenty-three Ph.D., five M.S. and one B.S. students have completed their degree program.

There are always too many research accomplishments to list all here. A selected list includes improving energy efficiency of CMOS imagers by >20x by employing a compressive sensing coding scheme utilizing a mixed-signal switched capacitor matrix multiplier, demonstrating that selecting ESD protection devices based on an eye diagram analysis reduces circuit performance degradation, improving energy density by 2x using a hybrid resonant switched capacitor converter with an integrated LC resonator while increasing efficiency, and demonstration of a 10-Gbps 315 GHz MSK receiver with 5X higher data rate than that for the state of art at 5X higher carrier frequency.

The TxACE laboratory is continuing to help advance integrated circuit research by making its instruments and expertise available to researchers and our industrial partners all over the world.

I would like to thank the students, principal investigators and staff for their efforts, and UT Dallas, the University of Texas System, TI, and SRC, as well as many friends of TxACE all over the world for their generous support. I look forward to another year of working with the TxACE team to make our way of life better, safer and healthier through our research, education and innovation.

Most importantly, I wish everybody health and safety.

Kenneth K. O, Director TxACE
Texas Instruments Distinguished
University Chair Professor
The University of Texas at Dallas

BACKGROUND & VISION

The $400+ billion per year integrated circuits industry is evolving into an analog/digital mixed signal industry. Analog circuits are providing or supporting critical functions such as sensing, actuation, communication, power management and others. These circuits impact almost all aspect of modern life including safety, security, health care, transportation, energy, and entertainment. To lead this change, in particular to lead analog and mixed signal technology education, research, commercialization, manufacturing, and job creation, the Texas Analog Center of Excellence was announced by Texas Governor Rick Perry in October 2008 as a collaboration of the Semiconductor Research Corporation, state of Texas through its Texas Emerging Technology Fund, Texas Instruments Inc., University of Texas system and University of Texas at Dallas. The Center seeks to accomplish the objectives by creating fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, healthcare, and public safety and security as well as by improving the research and educational infrastructure.

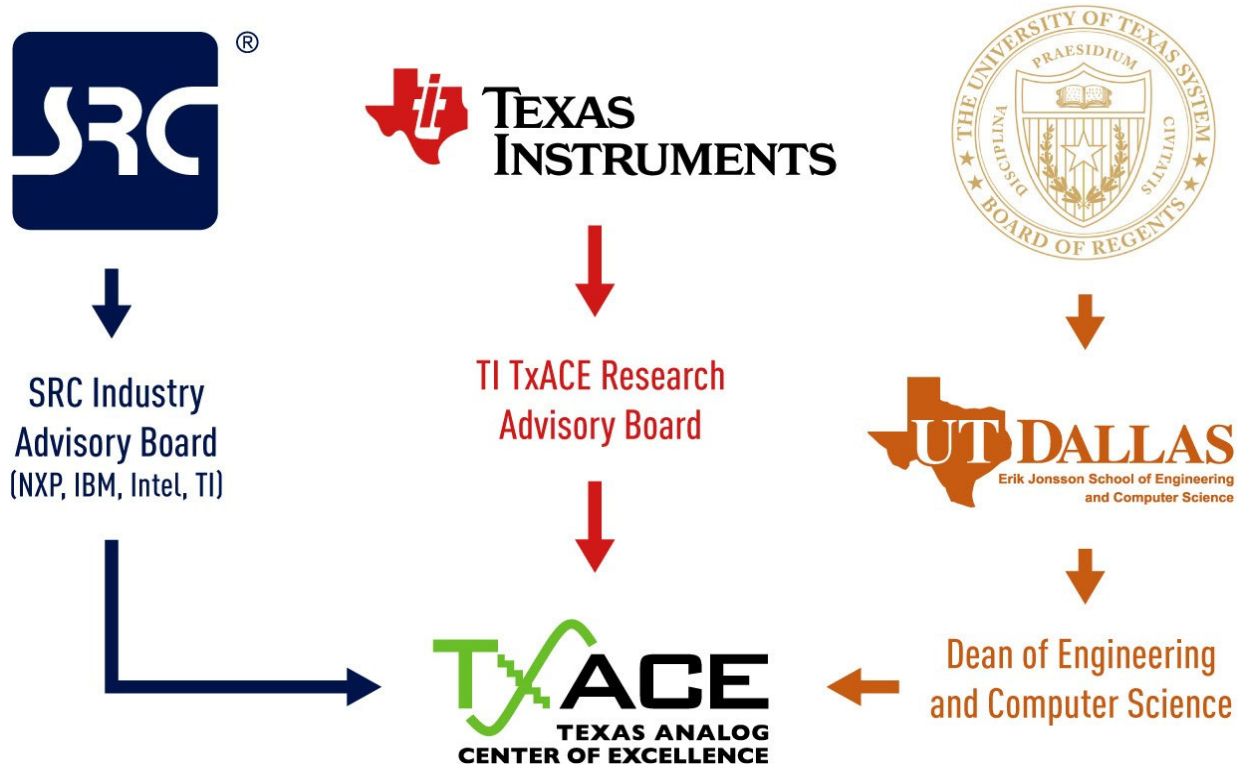


Figure 1. TxACE organization relative to the sponsoring collaboration (2019-2020).

CENTER ORGANIZATION

The Texas Analog Center of Excellence is guided by agreements established with the Center sponsors. Members of the industrial advisory boards identify the research needs and select research tasks in consultation with the Center leadership. Figure 1 diagrams the relationship of TxACE to the members of the sponsoring collaboration.

The internal organization of the Center is structured to flexibly perform the research mission while fully embracing the educational missions of the Universities.

Figure 2 shows the center management structure. The TxACE Director is Professor Kenneth O. The research is arranged into three thrusts that comply with the center mission: Safety, Security and Health Care, Energy Efficiency and Fundamental Analog Research. The third thrust consists of vital research that cuts across the first two research thrusts. The thrust leaders are Prof. Yiorgos Makris of the University of Texas at Dallas for safety, security and health care, and Prof. Ali Niknejad of the University of California, Berkeley for energy efficiency. The leader for fundamental analog is Prof. Pavan Hanumolu of University of Illinois, Urbana-Champaign. The thrust leaders along with Professor Dongsheng Ma of the The University of Texas at Dallas form the executive committee. The committee, along with the director, forms the leadership team that works to improve the research productivity by increasing collaboration, better leveraging the diverse capabilities of principle investigators of the Center, and lowering research barriers. The leadership team also identifies new research opportunities for consideration by the Industrial Advisory Boards.

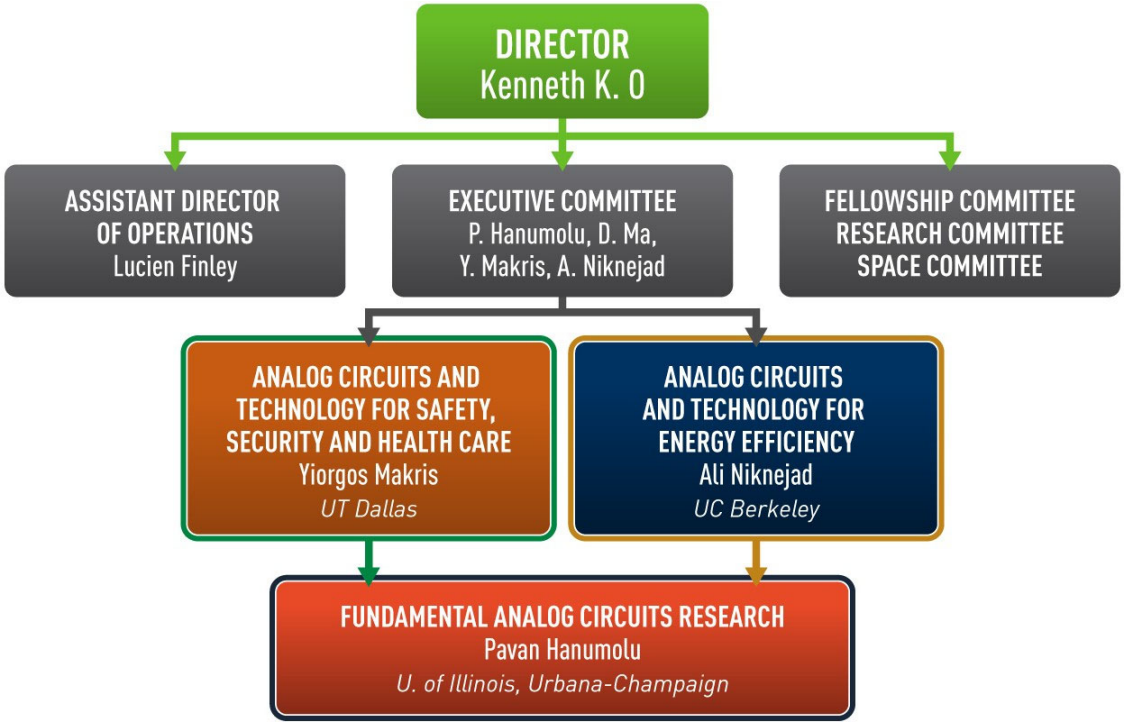


Figure 2. TxACE organization for management of research

SAFETY, SECURITY & HEALTH CARE

(Thrust leader: Yiorgos Makris, University of Texas at Dallas)

TxACE is developing analog technologies that enhance public safety and security, and health care. This thrust is working to improve safety by mitigating various reliability threats in analog/RF devices, including ESD, supply noise, temperature stress/strain and electro-migration, as well as by developing effective machine learning-based design, verification and self-test solutions. This thrust also seeks to reduce the cost of millimeter wave imaging and on-vehicle radar technology for automotive safety by researching signal processing techniques that reduce system complexity and transmitter architecture that can efficiently adapt to changing antenna characteristics, as well as sensor fusion techniques that can enable monitoring behaviors of a driver in an automobile. Furthermore, this thrust is investigating methods for remote attestation of IoT edge devices, security protocols for energy harvesting IoT nodes and security aware dynamic power management. Additionally, this thrust includes research towards designing efficient wearable IoT devices through 3D printing of distributed silicon circuits and sensors, as well as vital sign detection through millimeter wave radar.

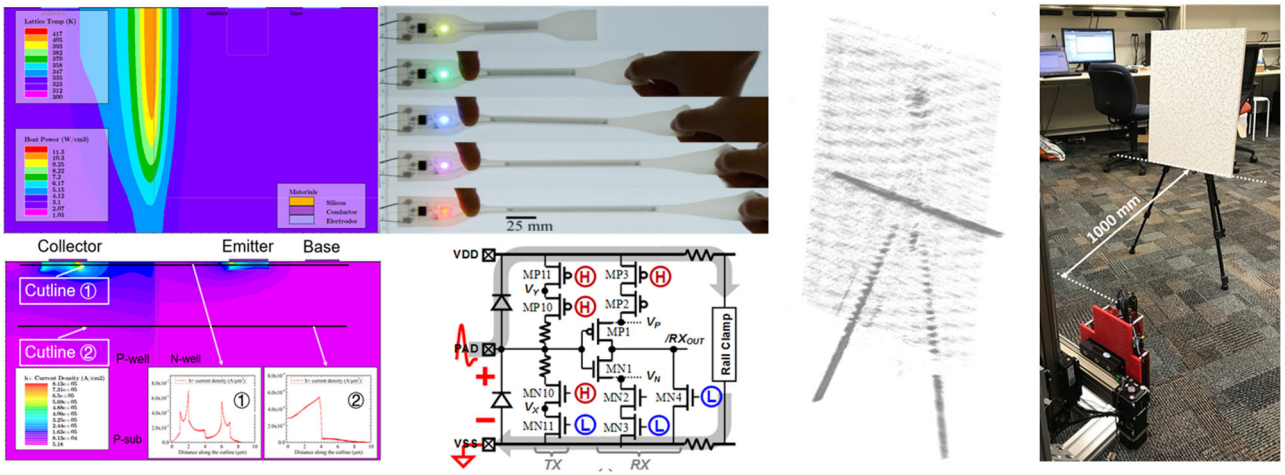


Figure 3. (Left) Holes current density distribution after parasitic substrate PNP triggers, with the current flow and crowding observable near the surface of the structure and the overall temperature distribution of the device @ I =300mA (Z. Chen, University of Arkansas), (Top center) Multi-layer printed LMP interconnects enable simple stretchable circuits using discrete components and embedded battery (M. Johnston & Y. Mengüc, Oregon State University), (Bottom center) Energy of the ESD pulse used to activate bias control circuitry that maximizes the transceiver robustness against the ESD-induced over-voltage stress at the IO pad (E. Rosenbaum, University of Illinois Urbana Champaign), (Right) Photograph of the small metal strip concealed behind a drywall located at a distance of 1000 mm, and reconstructed image in 3-D volumetric view (M. Torlak, UT Dallas).

ENERGY EFFICIENCY

(Thrust leader: Ali Niknejad, UC Berkeley)

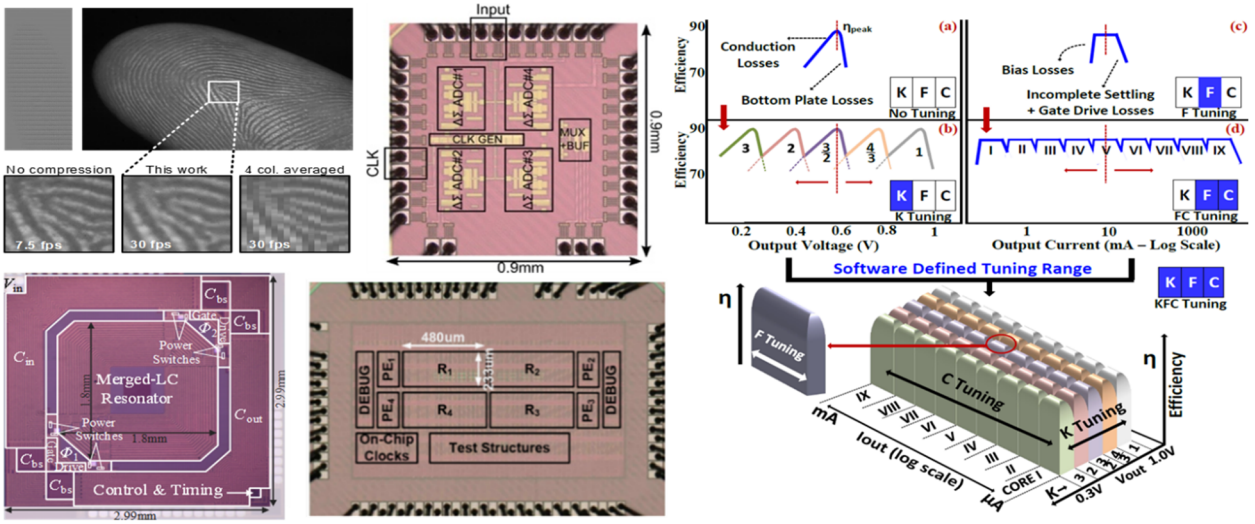


Figure 4. (Top left) Images captured using a compressive sensing coding scheme for a CMOS imager with a switched capacitor mixed-signal matrix multiplier improves the state-of-art energy efficiency by >20x. (N. Sun, UT Austin), (Top center) A VCO-based Bandpass-ADC by 4x time-interleaving our prior second-order LP-ADC that achieves a record-breaking band-pass Walden FoM of 57fJ/step. (A. Sanyal, U. of Buffalo), (Right) Efficiency profile of a capacitive converter and 3D-plot showing KFC (conversion ratio frequency capacitance) tuning for a direct battery-to-silicon DC-DC converter in CMOS using a multi-resonant coupled-inductor with 80% efficiency over a wide conversion range (0.2 – 0.8). (R. Harjani, U. of Minnesota), (Bottom left) Merged LC resonant switched capacitor for 2:1 step down with regulation @ 45 MHz. (J. Stauth, Dartmouth), (Bottom center) Metastability error detection and correction integrated circuit (MEDAC) consisting of 4 routers and PEs each having its own V/F domain (M. Seok, Columbia U.).

TxACE is committed to alleviate the global energy problem by improving the energy efficiency of electronic systems as well as by developing analog technologies that can make energy generation, distribution and utilization more efficient. The Center is also working to energize and power long-lasting in-situ microscale devices such as wireless microsensors, biomedical implants, and portable microelectronics. The research in this thrust includes power converters, co-optimization of converters and regulators with systems powered by them, I/O with power consumption that scales with the data rate, optimization of TSV placement for thermal management, efficient drivers for a power stage with reduced EMI, ultra low-power analog to digital converters, ultra-capacitors formed using carbon nano-tubes, a fast start-up crystal oscillator with reduced power consumption, built-in self-test for power management IC's, System-In-Package energy harvester and others. Many of the solutions employ mixed-signal techniques, exploiting digital trends and utilize novel scaling friendly analog architectures in order to improve the control and expand the flexibility of the overall system

FUNDAMENTAL ANALOG CIRCUITS RESEARCH

(Thrust leader: Pavan Hanumolu, U. of Illinois Urbana-Champaign)

Research in this thrust focuses on cross-cutting areas in analog and mixed signal circuits which impact all of the TxACE application areas (Energy Efficiency, Public Safety and Security, Health Care). The list of research includes design of a wide variety of analog-to-digital converters, communication links, low-power crystal oscillators, I/O circuits, noise reduction techniques, new amplifier topologies suitable for use in nano-scale CMOS, development of CAD tools and testing of integrated circuits.

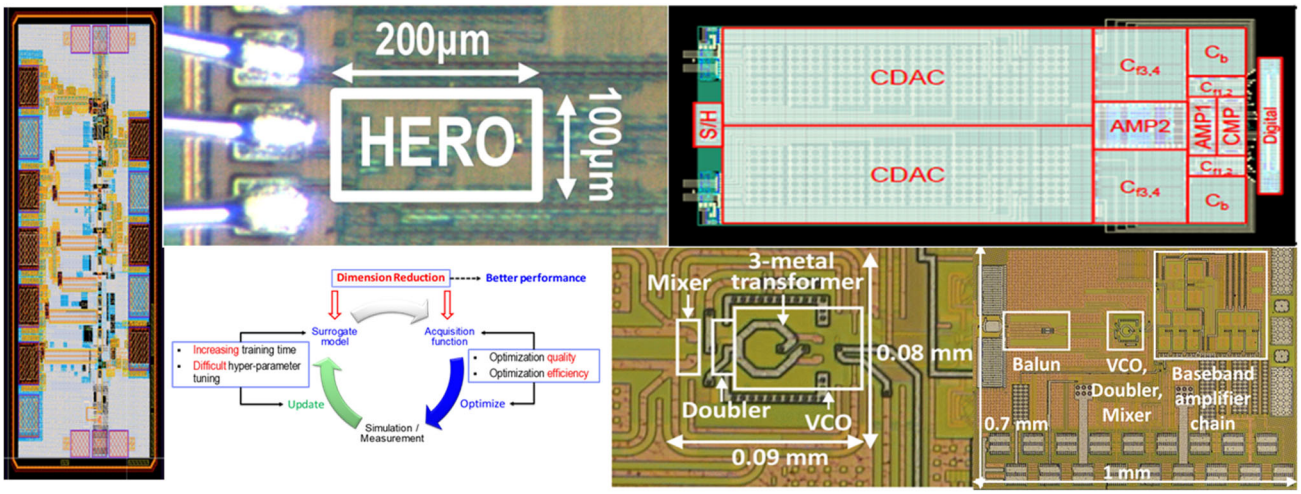


Figure 5. (Left) 170 - 260 GHz wideband LNA (A. Babakhani, UCLA), (Top cneter) Ultra-low-power crystal oscillator (D. Sylvester, University of Michigan), (Top right) Fourth-order noise shaping SAR ADC (M. Flynn, University of Michigan), (Bottom center) Bayesian optimization based rare failure detection for analog and mixed-signal circuits (P. Li, UC Santa Barbara), (Bottom right) 315 GHz minimum shift keying receiver (K. O, UT Dallas).

TXACE ANALOG RESEARCH FACILITY

The centralized group of laboratories of the Texas Analog Center of Excellence dedicated to analog engineering research and training occupy a ~ 8000-ft2 area on the 3rd floor of the Engineering and Computer Science North building (Figure 6). The facility includes RF and THz, Integrated System Design, Embedded Signal Processing, and Analog & Mixed Signal laboratories as well as CAD/Design laboratory structured to promote collaborative research**.** The unique instrumentation capability includes network analyses and linearity measurements up to 325 GHz, spectrum analysis up to 120 THz, and cryo-measurements down to 2^{o}K. The Center also added a pulsed multiple harmonic load and source pull measurement set up (up to 60 GHz for the third harmonic) and a 325-GHz antenna measurement set up. The close proximity of researchers in an open layout enables natural interaction and compels sharing of knowledge and instrumentation among the students and faculty. The TxACE analog research facility is one of the best equipped electronics laboratories. The laboratory is available for use by TxACE researchers and industrial partners all over the world.

Figure 6. TxACE Analog Research Facility

RESEARCH PROJECTS AND INVESTIGATORS

The Texas Analog Center of Excellence (TxACE) is the largest university analog technology center in the world. Table 1 lists the current principal investigators of the 74 tasks from 31 academic institutions funded by TxACE. Four universities (SMU, Texas A&M, UT Austin, UT Dallas) are from the state of Texas. Twenty-three are from outside of Texas. Four (Delft University of Technology, University of Twente, Indian Institute of Tech. Kharagpur, and University of Toronto) (Figure 7) are from outside of the US. Of the 63 investigators, 18 are from Texas. During the past year, the Center supported 168 Ph.D., 23 M.S., and 12 B.S. students. 23 Ph.D., five M.S., and one B.S. degrees were awarded to the TxACE students.

Investigator	Institution	Investigator	Institution	Investigator	Institution
B. Akin	UT/Dallas	A. Hazra	Indian Institute of Tech. Kharagpur	S. Ozev	Arizona State
N. Al-Dhahir	UT/Dallas	R. Henderson	UT/Dallas	S. Palermo	TEES
A. Babakhani	UCLA	S. Hoyos	TEES	S. Pamarti	UCLA
N. Bagherzadeh	UC/Irvine	J. Hu	TEES	G. Rincon-Mora	Georgia Tech
B. Bakkaloglu	Arizona State	M. Johnston	Oregon State U.	R. Rohrer	SMU
S. Bhunia	U. of Florida	C. Kim	U. of Minnesota	E. Rosenbaum	UIUC
D. Blaauw	U. of Michigan	M. Kim	UT/Dallas	A. Sanyal	U. at Buffalo
C. Busso	UT/Dallas	G. Lee	UT/Dallas	V. Sathe	U. of Washington
A. Chatterjee	Georgia Tech	J. Lee	UC/Irvine	P. Schaumont	Virginia Tech
D. Chen	Iowa State U.	P. Li	UC/Santa Barbara	K. Sengupta	Princeton
Y. Chen	Duke University	D. B. Ma	UT/Dallas	M. Seok	Columbia
Z. Chen	U. Arkansas/ Fayetteville	N. Maghari	U. of Florida	H. Shichijo	UT/Dallas
P. Dasgupta	Indian Institute of Tech. Kharagpur	K. Makinwa	Delft University	J. Stauth	Dartmouth
W. Eisenstadt	U. of Florida	Y. Makris	UT/Dallas	N. Sun	UT/Austin
M. Flynn	U. of Michigan	Y. Menguc	Oregon State U.	M. Swaminathan	Georgia Tech
J. Friedman	UT/Dallas	U. Moon	Oregon State U.	D. Sylvester	U. of Michigan
R. Geiger	Iowa State U.	S. Mukhopadhyay	Georgia Tech	G. Temes	Oregon State U.
J. Gu	Northwestern U.	F. Najm	U. of Toronto	S. Thompson	U. of Florida
P. Gui	SMU	B. Nauta	U. of Twente	M. Torlak	UT/Dallas
P. Hanumolu	UIUC	A. Niknejad	UC/Berkeley	A. Trivedi	U. Illinois, Chicago
R. Harjani	U. of Minnesota	K. O	UT/Dallas	X. Zhang	Washington U.

Table 1. Principal Investigators (May 2019 through April 2020)

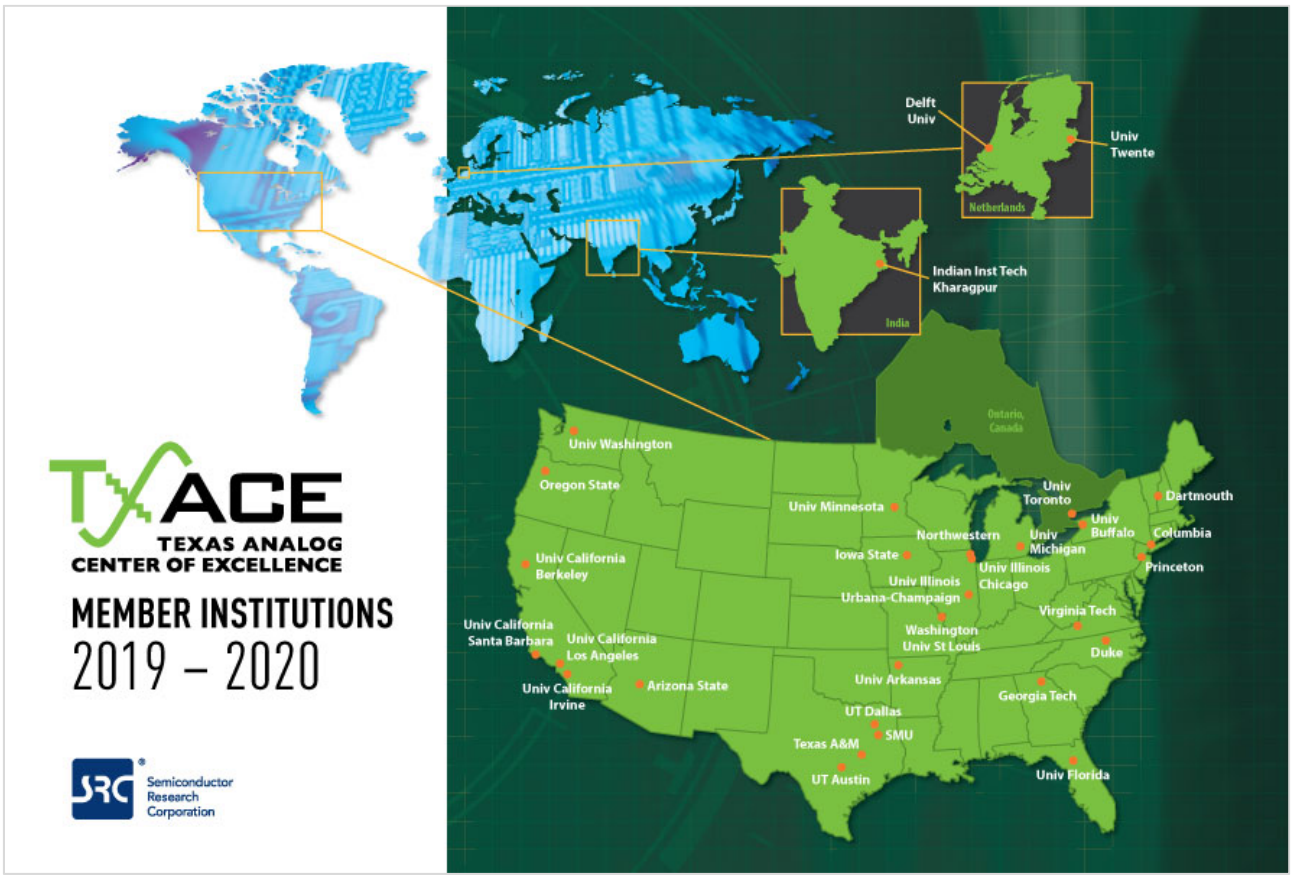


Figure 7. Member Institutions of Texas Analog Center of Excellence

SUMMARY OF RESEARCH PROJECTS

The 74 research projects funded through TxACE during 2019-2020 are listed in Table 2 below by the Semiconductor Research Corporation task identification number.

	Task	Thrust	Title	Task Leader	Institution
1	2712.002	EE/SS	On-line Self-Testing and Self-Tuning of Integrated Voltage Regulators	Mukhopadhyay, Saibal	Georgia Tech
2	2712.003	SS	Multi-Modal BIST Design and Test Metrics Evaluation for Analog/RF Circuits	Ozev, Sule	Arizona State
3	2712.005	FA	Automated Cross-Level Validation and Debug of Mixed-Signal Systems in Top-Down Design: From Pre-Silicon to Post-Silicon	Chatterjee, Abhijit	Georgia Tech
4	2712.006	EE	Robust, Efficient All-Digital SIMO Converters for Future SOC Domains	Sathe, Visvesh	Univ. of Washington
5	2712.007	EE	High-Resolution Low-Voltage Hybrid ADCs for Sensor Interfaces	Flynn, Michael	Univ. of Michigan
6	2712.008	EE	Direct-Battery-to-Silicon Power Transfer in Advanced Nanometer CMOS	Harjani, Ramesh	Univ. of Minnesota
7	2712.009	EE	Low Power Area Efficient Flexible-rate Energy Proportional Serial Link Transceivers	Hanumolu, Pavan Kumar	UIUC
8	2712.010	FA	Ringamp-assisted Circuits/Techniques and Next-generation Ringamps	Moon, Un-Ku	Oregon State Univ.
9	2712.011	FA	Robust Reliable and Practical High Performance References in Advanced Technologies	Geiger, Randall	Iowa St Univ.
10	2712.012	EE	EDAC and DCDC-Converter Co-Design for Addressing Robustness Challenges in Emerging Architectures	Seok, Mingoo	Columbia
11	2712.013	SS	Reconfigurable MM-Wave Tx Architecture and Antenna Interface with Active Impedance Synthesis in Multi-Port Node-Conjugated Combiner	Sengupta, Kaushik	Princeton
12	2712.014	FA	Leveraging CMOS Scaling in High Performance ADCS	Maghari, Nima	Univ. of Florida

	Task	Thrust	Title	Task Leader	Institution
13	2712.015	SS	Area-Efficient On-Chip System-Level IEC ESD Protection for High Speed Interface ICs	Chen, Zhong	U Arkansas/Fayetteville
14	2712.016	EE	3D IC Thermal Management Based on TSV Placement Optimization and Novel Materials	Lee, Jaeho	UC/Irvine
15	2712.017	SS	Mitigating Reliability Issues in Analog Circuits	Kim, Chris	Univ. of Minnesota
16	2712.018	SS/EE	Test Techniques to Approach Several Defect-per-billion for Power ICs	Eisenstadt, William	Univ. of Florida
17	2712.019	SS/EE	Pre-computed Security Protocols for Energy Harvested IoT	Schaumont, Patrick	Virginia Tech
18	2712.020	EE	Low-Power Mostly Digital Time-Domain Delta-Sigma ADCs for IoT	Sanyal, Arindam	Univ. at Buffalo
19	2712.021	SS	Distributed Silicon Circuits and Sensors in 3D-Printed Systems for Wearable IoT Sensors	Johnston, Matthew	Oregon State Univ.
20	2712.022	SS	Intrinsic Identifiers for Database-Free Remote Authentication of IoT Edge Devices	Bhunia, Swarup	Univ. of Florida and U. Illinois, Chicago
21	2712.023	EE	Ultra-Low-Power Compressive Sensing Techniques for IoT Applications	Sun, Nan	UT/Austin
22	2712.024	EE	A System-In-Package Platform for Energy Harvesting and Delivery for IoT Edge Devices	Mukhopadhyay, Saibal	Georgia Tech
23	2712.025	FA	Reduction of Low Frequency Noise Impact in Nano-Scale CMOS Circuits	O, Kenneth	UT/Dallas
24	2712.026	SS	Fault Characterization and Degradation Monitoring of SiC Devices	Akin, Bilal	UT/Dallas
25	2712.027	EE	Gate Driving Techniques and Circuits for Automotive-Use GaN Power Circuits	Ma, D. Brian	UT/Dallas
26	2712.028	EE	High Performance Micro-supercapacitor on a Chip Based on a Hierarchical Network of Nitrogen Doped Carbon Nanotube Sheets Supported MnO2 Nanoparticles	Lee, Gil	UT/Dallas

	Task	Thrust	Title	Task Leader	Institution
27	2712.029	SS	Novel Super-resolution and MIMO Techniques for Automotive and Emerging Radar Applications	Torlak, Murat	UT/Dallas
28	2712.031	FA	Adaptive Trimming and Testing of Analog/RF Integrated Circuits (ICs)	Makris, Yiorgos	UT/Dallas
29	2712.032	FA	Hierarchical Analog and Mixed-Signal Verification Using Hybrid Formal and Machine Learning Techniques	Li, Peng	UC/Santa Barbara
30	2810.002	SS/EE	Security-Aware Dynamic Power Management for System-on-Chips	Mukhopadhyay, Saibal	Georgia Tech
31	2810.003	EE	Integrated Voltage Regulator Management for System-on-Chip Architectures	Zhang, Xuan	Washington Univ.
32	2810.005	FA/SS	Circuit Design for ESD and Supply Noise Mitigation	Rosenbaum, Elyse	UIUC
33	2810.006	EE	Combating Unprecedented Efficiency, Noise and Frequency Challenges in Modern High Current Integrated Power Converters	Ma, D. Brian	UT/Dallas
34	2810.007	FA	Fully Integrated Phase Noise Cancellation Techniques	Niknejad, Ali	UC/Berkeley
35	2810.008	EE	Circuit Techniques for Fast Start-Up of Crystal Oscillators	Pamarti, Sudhakar	UCLA
36	2810.009	EE/FA	Mixed-Signal Building Blocks for Ultra-low Power Wireless Sensor Nodes	Sylvester, Dennis	Univ. of Michigan
37	2810.010	EE	GS/s ADC Based Cycle-to-Cycle Closed-Loop Adaptive Smart Driver for High-Performance SiC/GaN Power Devices	Gui, Ping	SMU
38	2810.011	EE	Micro-Power Analog-to-Digital Data Converters for Sensor Interfaces	Temes, Gabor	Oregon State Univ.
39	2810.012	EE	NPSense - Nano-Power Current Sensing	Makinwa, Kofi	Delft University
40	2810.013	FA	Frequency-Domain ADC-Based Serial Link Receiver Architectures for 100+Gb/s Serial Links	Palermo, Samuel	TEES

	Task	Thrust	Title	Task Leader	Institution
41	2810.014	SS	Deep Learning Solutions for ADAS: From Algorithms to Real-World Driving Evaluations	Busso, Carlos	UT/Dallas
42	2810.015	FA	Demonstration of 120-Gbps Dielectric Waveguide Communication Using Frequency Division Multiplexing (FDM) and Polarization Division Multiplexing (PDM)	O, Kenneth	UT/Dallas
43	2810.016	SS	Condition Monitoring of Industrial/Automotive Drive Components through Leakage Flux	Akin, Bilal	UT/Dallas
44	2810.017	SS	Reliability Study of E-mode GaN HEMT Devices	Kim, Moon	UT/Dallas
45	2810.018	FA	Transition Design for High Data Rate Links at Submillimeter Wave Frequencies	Henderson, Rashaunda	UT/Dallas
46	2810.019	FA	Design Automation for Coverage Management in Analog and Mixed-Signal SOCs	Dasgupta, Pallab	Indian Institute of Tech. Kharagpur (IITK)
47	2810.020	FA	Analog/Mixed-Signal RF Circuit Time Domain Sensitivity and Its Applications	Rohrer, Ronald	SMU
48	2810.021	SS	A Collaborative Machine Learning Approach to Fast and High-Fidelity Design Prediction	Hu, Jiang	TEES and Duke University
49	2810.022	SS	A Collaborative Machine Learning Approach to Fast and High-Fidelity Design Prediction	Chen, Yiran	Duke Univeristy and TEES
50	2810.023	SS	Machine Learning Driven Automatic Mixed-Signal Design Verification-Validation for Automotive Applications	Chatterjee, Abhijit	Georgia Tech
51	2810.025	SS	Machine Learning-Based Layout Analysis and Netlist Optimization for Defect Tolerance and Design Robustness to Process Imperfections and Variations	Makris, Yiorgos	UT/Dallas
52	2810.026	FA	Low Noise Balun Pre-Power Amplifier	Nauta, Bram	University of Twente
53	2810.027	SS	Measurement and Modeling of Stress/Strain on Analog Transistor and Circuit Parameters	Thompson, Scott	University of Florida
54	2810.028	FA	Robust ATE Multi-Site HW Design to Enable Effective Analog Performance Testing in Analog-Mixed-Signal (AMS) SoCs	Chen, Degang	Iowa State U.

	Task	Thrust	Title	Task Leader	Institution
55	2810.029	FA	170GHz – 260GHz Wideband PA and LNA Design in Silicon	Babakhani, Aydin	UCLA
56	2810.030	FA	Neural Network Recognition & On-Chip Online Learning with STT-MRAM	Friedman, Joseph	UT/ Dallas
57	2810.031	FA	Development and Asssessment of Machine Learning Based Analog and Mixed-Signal Verification	Li, Peng	UC/Santa Barbara
58	2810.032	EE	DRIVR: A Digital, Re-configurable, Unified Clock-Power (UniCaP) Fabric for Energy-Efficient SoCs	Sathe, Visvesh	U. of Washington
59	2810.033	FA	Interleaved Noise-Shaping SAR ADCs for High-Speed and High-Resolution	Flynn, Michael	U. of Michigan
60	2810.034	EE	Always-on Keyword Spotting based on Analog-Mixed-Signal Computing Hardware	Seok, Mingoo	Columbia
61	2810.035	EE	Computationally Controlled Integrated Voltage Regulators	Sathe, Visvesh	U. of Washington
62	2810.036	FA	Highly Stable Integrated Frequency References	Hanumolu, Pavan	UIUC
63	2810.037	FA	High-performance Ringamp-based ADCs	Moon, Un-Ku	Oregon State U.
64	2810.038	SS	Extreme Temperature Digital, Analog, and Mixed-Signal Circuits (ET-DAMS)	Kim, Chris	U. of Minnesota
65	2810.039	EE	Development of Compact and Low Cost Fully Integrated DC-DC Converter with Resonant Gate Drive and Intelligent Transient Response	Gu, Jie	Northwestern U.
66	2810.040	EE	Hybrid/Resonant Sc Converters With Integrated Lc Resonator For High-Density Monolithic Power Delivery	Stauth, Jason	Dartmouth
67	2810.041	SS	ESD Protection for IO Operating at 56 Gb/s and Beyond	Rosenbaum, Elyse	UIUC
68	2810.042	EE	Digitally Enhanced High Efficiency, Fast Settling Augmented DCDC Converters	Bakkaloglu, Bertan	Arizona State

	Task	Thrust	Title	Task Leader	Institution
69	2810.043	FA	Analog Optimization Hybridizing Designer's Intent and Machine Learning	Li, Peng	UC/Santa Barbara
70	2810.044	FA	Hierarchical Characterization and Calibration of RF/Analog Circuits Using Lightweight Built-in Sensors	Ozev, Sule	Arizona State
71	2810.046	SS	Generating Current Constraints for Electromigration Safety	Najm, Farid	U. of Toronto
72	2810.047	SS	Architecture and DfT methods for improving life time reliability and functional safety of electronic circuits and systems out of application context	Chen, Degang	Iowa State U.
73	2810.048	SS	Characterization and Mitigation of Electromigration Effects in Advanced Technology Nodes	Kim, Chris	U. of Minnesota
74	2810.049	EE	1-W Battery-Charging CMOS Buck Regulator	Rincon-Mora, Gabriel	Georgia Tech

Table 2: Funded research projects at TxACE by SRC task identification number (FA: Fundamental Analog, EE: Energy Efficiency, SS: Safety, Security and Health Care)

ACCOMPLISHMENTS

In the past year, TxACE has made significant research progress. Table 3 summarizes the number of publications and inventions resulting from the TxACE research during May 2019 to April 2020, while Table 4 lists the major research accomplishments for the Center during the period. The TxACE researchers have published 48 conference papers and 29 journal papers. They have also made 2 invention disclosure, filed 5 patent applications, and were granted 2 patents. The list of publications is included as Appendix I. Following the tabulation, brief summaries of each project are provided.

Table 3. TxACE number of publications (May 2019 through April 2020)

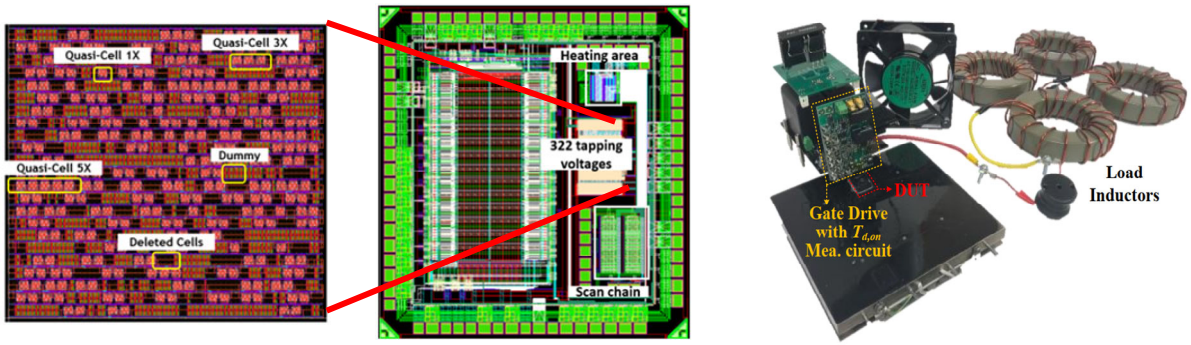
Conference Papers	Journal Papers	Invention Disclosures	Patents Filed	Patents Granted
48	29	2	5	2

Table 4. Major TxACE Research Accomplishments (May 2019 through April 2020)

Category	Accomplishment
Fundamental Analog (Circuits)	Ultra-low power crystal oscillators (XOs) are key components in wearable, IoT, and mobile applications. Using a frequency-divided high-energy-to-noise-ratio pulse injection allows the crystal to run freely for a longer time between injections, thus improving long-term frequency stability and reducing injection overheard. Fabricated in 40-nm CMOS, a prototype 32kHz XO consumes only 0.51nW and achieves 2ppb Allan deviation, which is 5x lower compared to that achieved by state-of-the-art nW-XOs. (2810.009, PI: D. Sylvester & D. Blaauw, U Michigan)
Fundamental Analog (Circuits)	Higher-order noise shaping in successive approximation register analog to digital converter (SAR ADC) is demonstrated using a cascaded-noise-shaping (CaNS) SAR architecture. By cascading two 2nd-order NS stages, a 4th-order noise-transfer function is realized while consuming similar power and area to a 2nd-order NS-SAR. Fabricated in 28-nm CMOS, the prototype CaNS-ADC occupying 0.02mm^2 achieves 88dB SNDR over a 100kHz bandwidth while consuming only 120µW. (2810.033, PI: M. Flynn, U Michigan)
Energy Efficiency (Circuits)	Power IC's from a battery involves several power conversion stages, usually requiring a high voltage buck converter and LDOs. A direct battery-to-silicon prototype demonstrates that DC-DC conversion can be accomplished in CMOS using a multi-resonant coupled-inductor with 80% efficiency over a wide conversion rage (0.2 – 0.8). The output voltage is then regulated using a digital LDO with zero steady-state output voltage ripple. (2712.008, PI: R. Harjani, U Minnesota)
Energy Efficiency (Circuits)	Ultra low-power compressive sensing techniques for IoT applications have the potential to greatly improve the energy efficiency of edge devices. A compressive sensing coding scheme for a CMOS imager uses a mixed-signal switched capacitor matrix multiplier. This is the first CMOS image sensor that achieves single-shot compressive sensing using Nyquist-rate ADCs, improving the state-of-art energy efficiency by >20x. (2717.023, PI: N. Sun, UT Austin)

Energy Efficiency (Circuits)	A hybrid resonant switched capacitor converter with an integrated LC resonator is demonstrated for high-density power delivery. A designed and tested merged LC resonator with on-chip spiral magnetics results in a factor of two improvement in power density with higher efficiency relative to comparable pure switched-capacitor implementations. (2810.040, PI: J. Stauth, Dartmouth)
Safety, Security and Health Care (Systems)	This project is developing a co-design methodology for ESD-protected front-end circuits in 56-Gbps receivers that employ PAM4 signaling. Defining a capacitance budget as a function only of the data-rate and the technology node is overly simplistic and may lead one to unnecessarily limit a component ESD reliability. Selecting ESD protection devices based on an eye diagram analysis reduces circuit performance degradation. (2810.041, PI: E. Rosenbaum, UIUC)
Safety, Security and Health Care (Systems)	This project investigates vital sign detection algorithms using mm-Wave frequency modulated continuous wave (FMCW) radar. To date, results have shown effective tracking of a heart rate across time, with mean squared heart rate errors of approximately 1 bpm for a static single subject when compared to a wearable chest strap. (2712.029, PI: M. Torlak, UT Dallas)

Safety, Security and Health Care Thrust



Category	Accomplishment
Safety, Security and Health Care (Systems)	This project is developing a co-design methodology for ESD-protected front-end circuits in-54 Gbps receivers. Initial work focused on a study of "ESD capacitance budgets," demonstrating that an eye diagram analysis is needed to determine when the ESD protection will unacceptably compromise the circuit performance. Case studies made apparent that defining a capacitance budget as a function only of the data-rate and the technology node may lead one to unnecessarily limit a component ESD reliability or, conversely, force the designer to unnecessarily increase the chip power or accept a reduced error rate. (2810.041, E. Rosenbaum, UIUC)
Safety, Security and Health Care (Systems)	As opposed to camera-based sensors, millimeter wave (mm-Wave) radar technology provides the ability to meet privacy requirements in addition to being unobtrusive and non-intrusive. This project investigates vital sign detection algorithms using mm-Wave frequency modulated continuous wave (FMCW) radars. To date, results have shown effective tracking of a heart rate across time, with mean squared heart rate errors of approximately 1 bpm for a static single subject when compared to a wearable chest strap. (2712.029, M. Torlak, UT Dallas)
Safety, Security and Health Care (Systems)	There is an emerging set of applications requiring stretchable, compliant electronics, including wearable devices, instrumented fabrics, and soft robots with distribute sensors and computation. Over the course of this project, progress has been made in printing multi-layer stretchable circuits using discrete components, in extended strain testing of liquid metal paste material, and in development of compact modeling frameworks for stretchable interconnects. (2712.021, M. Johnston & Y. Mengüc, Oregon State University)

TASK 2712.002, ON-LINE SELF-TESTING AND SELF-TUNING OF INTEGRATED VOLTAGE REGULATORS

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SIGNIFICANCE AND OBJECTIVES

The proposed research will develop low-complexity algorithms and low-overhead all-digital self-testing and self-tuning architecture for high-frequency IVRs. The proposal will focus on a digitally controlled fully integrated inductive VR (FIVR), digital low-dropout regulators (DLDO), and power delivery system with a FIVR and multiple distributed DLDOs.

TECHNICAL APPROACH

The challenge for testing/tuning of IVRs is the presence of high frequency closed-loop control. The proposed approach is based on the principle that in a system with an IVR and digital core(s), the testing/tuning should focus on system performance rather than the IVR in isolation. We propose to characterize the output voltage variation that ultimately determines the performance of the digital load. We consider large signal perturbations (load and reference steps) to excite the transient noise in the IVR's output, and tune the IVR's loop to minimize the noise. Finally, we explore co-tuning of IVR and processor.

SUMMARY OF RESULTS

A fully synthesized integrated inductive buck regulator with flexible precision variable frequency feedback loop implemented in 65-nm CMOS process using an automated design and GDSII generation flow is demonstrated. The design demonstrates 0.52V/µs output ramp and 200ns response time to 30mA/75ps load transient in a high precision mode with 120MHz switching frequency. The peak efficiency is 79.3% at 0.78V output and 43mA load current.

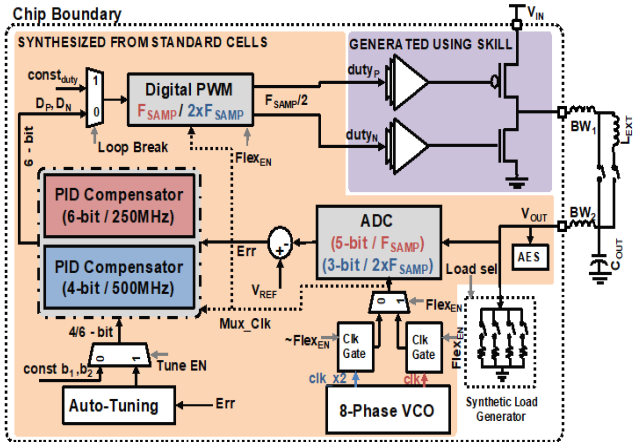
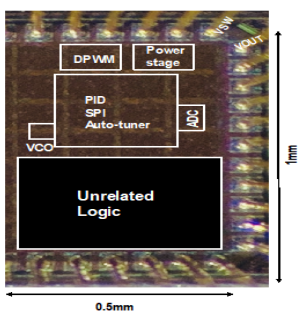


Figure 1. The architecture of full-synthesized architecture with on-line tuning.



Technology	65
Package	CLCC44
Control	Digital PWM Flexible Precision
Phase	1
V_{IN} (V)	0.9-1.2
V_{OUT} (V)	0.6-1.0
Maximum I_L (mA)	45
F_{SW}	80-120
F_{SAMP}	160-240 (High Precision) 320-480 (Low Precision)
L (nH)	62 (50+2xBW)
C (nF)	23 (20 + 1.5 mos + 1.5 mim)
Peak Efficiency (%)	79.3 @ (V_{OUT}=0.78V, I_L=43mA)
Synthesizable	Yes

Figure 2. The summary of the test-chip.

The degradation of the transient performance and power conversion efficiency of on-chip VRs due to NBTI have been investigated. The measurement show that NBTI induced shifts in the power stage resistance have much smaller effect on the IVR compared to DLDOs.

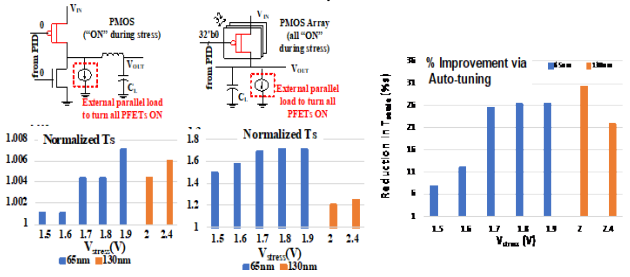


Figure 3. The measurement results showing impact of of aging on inductive VR and digital LDO.

Keywords: Integrated voltage regulator, self-testing,

INDUSTRY INTERACTIONS

Intel, NXP

MAJOR PAPERS/PATENTS

[1] A. Singh, et al., "A Digital Low-Dropout Regulator with Auto-Tuned PID Compensator and Dynamic Gain Control for Improved Transient Performance under Process Variations and Aging," IEEE TPEL, March 2020.

[2] V. Chekuri, et al., "Auto-tuning of Integrated Inductive Voltage Regulator using On-chip Delay Sensor to Tolerate Process and Passive Variations," IEEE TVLSI, Aug. 2019.

[3] V. Chekuri, et al., "A Fully Synthesized Integrated Buck Regulator with Auto-generated GDS-II in 65nm CMOS Process," IEEE CICC, March 2020.

[4] (Invited) V. Chekuri, et al., "Aging Challenges in On-chip Voltage Regulator Design," International Reliability Physics Symposium (IRPS), April 2020.

TASK 2712.003, MULTI-MODAL BIST DESIGN AND TEST METRICS EVALUATION FOR ANALOG/RF CIRCUITS

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SIGNIFICANCE AND OBJECTIVES

This project aims at (a) designing a library of BIST blocks that can be re-designed with minimal effort, (b) developing measurement techniques that do not rely on detailed knowledge of internal BIST parameters, and (c) developing a BIST advisor toolflow for system-level BIST insertion and evaluation.

TECHNICAL APPROACH

We have divided this problem into two parallel threads. First, we have developed a library of BIST components, including a gain measurement unit, a phase mismatch measurement unit, a PRBS injection unit, a cross correlator, and a programmable OPAMP-less ADC. Second, the BIST advisor toolflow takes into account multiple BIST options and evaluates them in terms of fault coverage and hardware cost to provide viable options for the designers.

SUMMARY OF RESULTS

During this project, we have developed a BIST insertion flow. Our BIST approach consists of two parts, first one is a target specific part where we develop a methodology to apply and observe PRBS in order to obtain a loop transfer function, second part is evaluation of different testing approaches in terms of fault coverage. The latter also considers the simulation shortcomings and includes the application of macro-modelling to shorten the simulation time which may be prohibitively high when a high number of potential faults could be inserted into circuits and also considering challenges of simulating circuits which take a very long time to simulate.

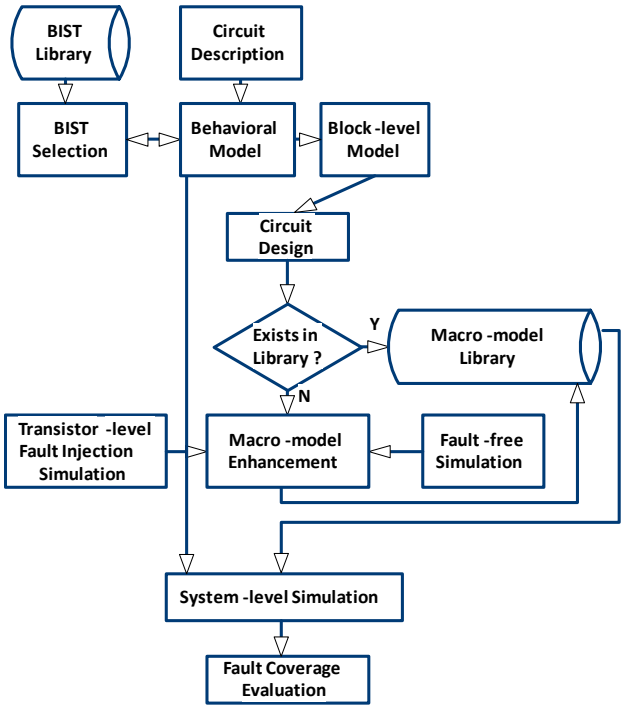

Figure 1. BIST insertion flow.

The flow of our testing approach, which is called BIST advisor is summarized in Figure 1. BIST library in the flow chart consists of blocks designed such as PRBS generation, digital cross correlator etc. For any target application there may be some different blocks needed. For example, PLL and LDO use the same 12-Bit PRBS generation and same digital cross correlator consisting of up/down counter, however since LDO output is analog it requires a 1-bit analog-to-digital converter. The first step in the process is to develop a methodology to apply and cross correlate PRBS signals, which is explained in depth in the previous sections. Next task is to decide whether circuit simulation could be done for fault evaluation considering the simulation time for the set of fault cases. We want to macro model faulty behavior of a circuit so that it can be simulated quickly. In order to do that first, non-faulty behavior should be modelled. Matlab or any other behavioral modelling tool can be used for this purpose. Block level simulations are very fast, thus it enables fast modelling. After non-faulty block in a loop is modelled, its features which effects the loop behavior is extracted. Then faults are inserted and model is extracted based upon these features.

Keywords: Analog BIST, Fault Simulation

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

[1] Ince, Mehmet, and Sule Ozev. "Digital Defect Based Built-in Self-Test for Low Dropout Voltage Regulators." In IEEE European Test Symposium (ETS), pp. 1-2. IEEE, 2020.

TASK 2712.013, RECONFIGURABLE MM-WAVE TX ARCHITECTURE AND ANTENNA INTERFACE WITH ACTIVE IMPEDANCE SYNTHESIS IN MULTI-PORT NODE-CONJUGATED COMBINER

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SIGNIFICANCE AND OBJECTIVES

We demonstrated a generalized broadband VSWR-reconfigurable PA architecture with a multi-port DAC based topology across 26-40 GHz. We also reported the first mm-Wave Load Modulated Balanced Amplifier (LMBA) that aims broadband and back-off efficiency in the 5G bands. The paper has been **is a Best student paper finalist at IMS 2020.**

TECHNICAL APPROACH

We proposed a generalized method of loadpulling to overcome VSWR in a reconfigurable fashion between 26-40 GHz. For the LMBA, we presented the first mmWave load modulated balanced PA architecture with adaptive biasing for enhanced linearity.

SUMMARY OF RESULTS

The VSWR-tolerant RF-in and RF-out PA is based on the proposed asymmetrical architecture to allow for broadband operation over the multiple bands at 28GHz, 37GHz, and 39GHz while allowing tolerance towards VSWR events up to 4:1. The initial results were published in [1], and we presented an entire analytical framework and theoretical limits and design techniques in the special issue paper in [2].

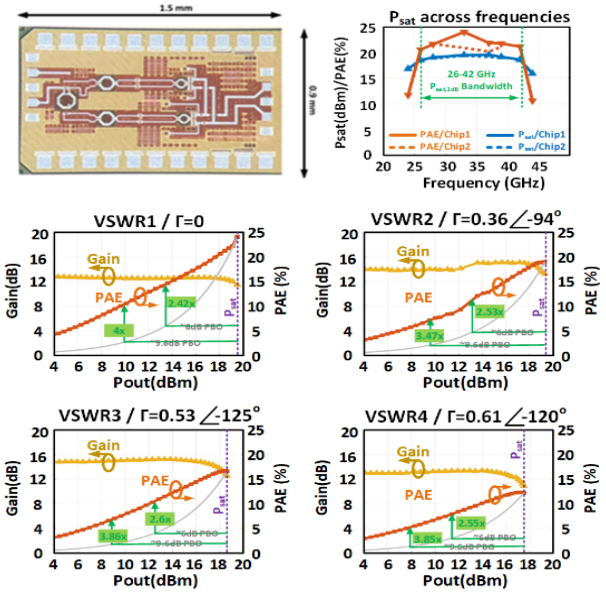

Figure 1. Schematic of the broadband VSWR-tolerant PA architecture in 65-nm CMOS operating across 26-40 GHz.

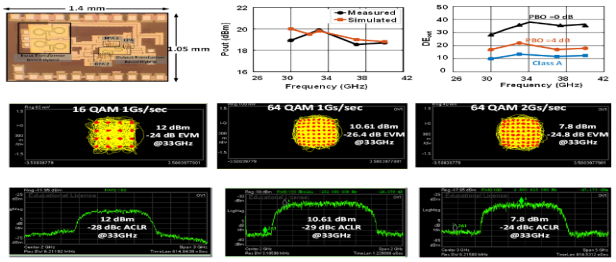

Figure 2. Continuous wave measurements of LMBA across 30-40 GHz along with drive ups at 33,36 and 40 GHz. EVM and ACLR vs average output power for a 16/64 QAM signal at 33 GHz. 16QAM and 64QAM constellations and spectrum.

The load modulated balanced amplifier chip micrograph is shown in Fig. 2. The architecture is implemented with a transformer-based hybrid at input and output to allow wideband power combining and achieve high isolation with a control PA for load-modulation and back-off efficiency enhancement across 30-40 GHz. For enhanced linearity, an integrated adaptive biasing is integrated on-chip allowing superior ACLR performance across 30-40 GHz. The PA achieves 18.5-20 dBm, output drain efficiency >30% across 30-40 GHz, and demonstrates EVM of -26.4 dB and ACLR of -29 dBc at an average output power of 10.6 dBm for 64-QAM at 1GS/s. To the best of the authors' knowledge, this is the first load-modulated balanced PA at mmWave in silicon.

Keywords: mmWave, PA, broadband, load modulation, 5G

INDUSTRY INTERACTIONS

Texas Instruments, Intel, NXP

MAJOR PAPERS/PATENTS

[1] C.R.Chappidi and K.Sengupta, "A 26-42 GHz Broadband, Back-off efficient and VSWR Tolerant CMOS Power Amplifier Architecture for 5G Applications," *VLSI 2019.*

[2] C.R.Chappidi, T.Sharma, Z.Lu and K.Sengupta, "Multiport-Active Load-pulling for mm-Wave 5G Power Amplifiers: Bandwidth, Back-off Efficiency and VSWR Tolerance," *IEEE TMTT* special Issue on mmw-PAs.

[3] C.R.Chappidi, T.Sharma, Z.Lu and K.Sengupta, "Load Modulated Balanced mm-Wave CMOS PA with Integrated Linearity Enhancement for 5G applications" *IMS 2020.*

[4] Kaushik Sengupta and Chandrakanth Chappidi, Load modulated balanced mm-Wave PA architecture, provisional patent filed.

TASK 2712.015, AREA-EFFICIENT ON-CHIP SYSTEM-LEVEL IEC ESD PROTECTION FOR HIGH SPEED INTERFACE IC'S

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SIGNIFICANCE AND OBJECTIVES

Area-efficient, low-capacitance, on-chip system-level IEC ESD protection solutions for high-speed interface ICs will be designed, fabricated and characterized. Device physics for substrate parasitic PNP structure in P^+/N-well diodes will be modeled.

TECHNICAL APPROACH

To reduce the total ESD device areas and reduce the parasitic capacitance, our approach is to utilize the inherent parasitic PNP structure in the high-side ESD diode as a parallel path to shunt the ESD discharge current. The key for this approach is to understand and adjust the characteristics of substrate PNP structures, such that the triggering and ESD clamping voltage of parasitic PNP structure is within the specific ESD protection window. Meanwhile, the clamping voltage of the primary ESD protection path needs to be higher than the triggering voltage of the parasitic PNP device.

SUMMARY OF RESULTS

First, ESD diodes with various layout designs were fabricated in the UMC 65-nm CMOS process. The objective is to evaluate which type of diodes can achieve better ESD performance (e.g., thermal failure current I_{t2}) within the same layout area for given I_{t2}/Area. Moreover, capacitance of these devices is investigated. Different metal routings were designed for different diode structures to compare the capacitance. The TLP I-V measurements show that the island-type diodes achieve higher I_{t2}/Area than the finger-type diodes, but also have higher capacitance. Thus, the figure-of-merit, I_{t2}/C is introduced to supplement the performance evaluation of the device.

Second, ESD characterization of dual-diode ESD protection with a primary ESD cell (2.5V PMOS and 2.5V NMOS were designed) was conducted. We expected that the parasitic substrate PNP should not be triggered before the turn-on of the primary ESD cell. However, the measurements indicate that parasitic substrate PNP triggers before the primary ESD due to higher triggering voltage of the primary ESD cell. The triggering voltage on this parasitic substrate PNP has been re-designed in a new tapeout.

Third, in the real applications of the dual-diode ESD protection, parasitic capacitance existing in the power supply or board might have some effects on ESD behaviors of the parasitic substrate PNP. The parasitic capacitance will introduce transient displacement current that will be injected into the forward-biased ESD diode. This transient current may affect the triggering of the parasitic substrate PNP. The testing configuration shown in Figure 1 is used to evaluate this effect. Through the direct comparison of the TLP I-V curves with and without the external capacitor, we can observe that the triggering point decreases with the external capacitor. A time domain extraction of a single TLP waveform has been performed to characterize the injected current level generated by the external capacitor. The actual I-V curve across the external capacitor can be extracted from the waveforms captured by the oscilloscope (Figure 1). More TLP measurements are going to be performed to evaluate the effects of current injection on the parasitic PNP triggering.

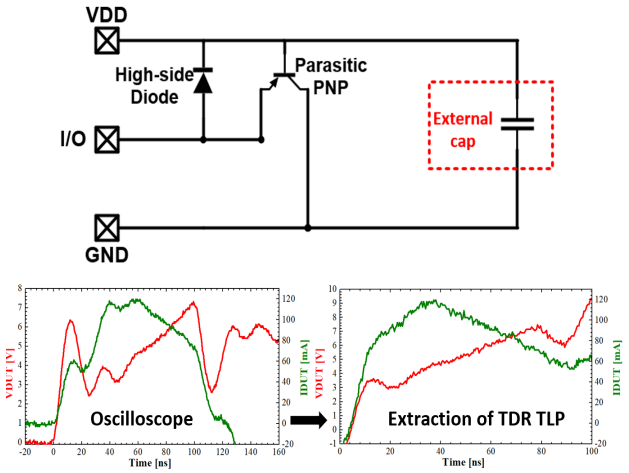

Figure 1. Current injection testing configuration with an external capacitor is used to analyze the effect of injected current on the parasitic PNP triggering behavior. Time domain extraction methodology is used to get the I-V curve across the capacitor.

Keywords: ESD, PNP, IEC, TCAD, Current injection

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Zhong Chen, Muhammad Ali, Hui Wang, "ESD Self-protection of Output Circuitry Using Substrate Bipolar Structure," Provisional patent filed.

[2] W. Hui, et al, "Area-efficient Dual-diode ESD Protection Based on Parasitic Bipolar Device for High-speed Interface ICs," Under revision for Journal of Electrostatics.

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SIGNIFICANCE AND OBJECTIVES

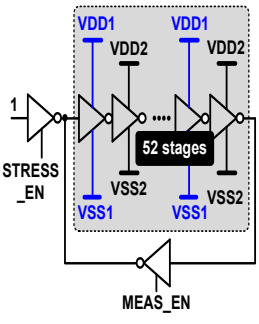
An on-chip reliability monitor capable of characterizing all four types of bias temperature instability (BTI) modes is proposed. Stressed ring oscillators with independent dual power rails are implemented for this purpose. Extensive BTI data was collected from a 65-nm ROSC array under different stress conditions.

TECHNICAL APPROACH

In this work, we demonstrate for the first time, an on-chip beat frequency based monitor circuit capable of characterizing frequency shifts caused by all four BTI modes. The main innovation is a ring oscillator (ROSC) circuit with dual power rails enabling different BTI stress modes. The beat frequency detection scheme offers a high frequency measurement precision (>0.01%) with minimal unwanted device recovery during measurements owing to the short stress interrupt time (>1µs).

SUMMARY OF RESULTS

The proposed ring oscillator circuit for separately measuring all four BTI induced shifts shown in Fig. 1 consists of two power rails, a 52-stage inverter chain, and two tri-state inverters. During stress mode, the ROSC is configured as an open loop inverter chain whose input is set to 0V. To apply different BTI stress modes to the inverter chain, two sets of power supplies are used; VDD1 and VSS1 for odd inverter stages and VDD2 and VSS2 for even inverter stages. In measurement mode, the inverter chain is configured into a ROSC and the power rail voltages are switched to the nominal VDD and VSS voltages.

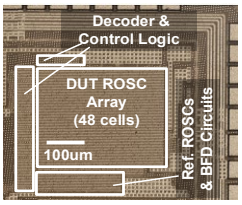


Mode 1	PMOS NBTI + NMOS PBTI
Mode 2	Mode1 + PMOS PBTI
Mode 3	Mode1 + NMOS NBTI
Mode 4	Mode1 + PMOS PBTI + NMOS NBTI

Power Supply Conditions				
Stress Mode	VDD1	VSS1	VDD2	VSS2
Mode 1	Vstress	0	Vstress	0
Mode 2	Vstress	0	0	0
Mode 3	Vstress	Vstress	Vstress	0
Mode 4	Vstress	Vstress	0	0
Meas. Mode	Vnom	0	Vnom	0

Figure 1. (left) Proposed dual power rail ROSC. (upper right) BTI stress modes. (lower right) Power supply configuration.

The test chip shown in Fig. 2 consists of a 48 ROSC array grouped into four 12 ROSC sub-arrays, 3 reference ROSCs, and 3 parallel beat frequency detection circuits. Each sub-array is assigned to one of the four different stress modes, and power switches control the two VDD and VSS pairs depending on the stress mode. Before applying stress, we measured the frequency distribution of fresh ROSCs. The frequencies of the three reference ROSCs were separated using on-chip trimming capacitors to cover the frequency range (~3%) of the ROSC array. During stress mode, one ROSC is selected at a time for frequency measurements using column and row decoders while the other ROSCs are kept in stress mode. The multiplexed output of the selected DUT is compared with the three reference ROSC frequencies using the beat frequency detection circuits.



Process	65nm GP
BTI Stress Modes	PMOS NBTI, NMOS PBTI, PMOS PBTI, NMOS NBTI
Core/IO Supply	1.0V / 2.5V
Stress Voltage	1.8V, 2.2V, 2.6V
Meas. Voltage	0.9V
DUT Device	Core Deivce
Area	425 x 360 µm^2

Figure 2. Die photo and chip specification summary.

Frequency shifts measured from the 65nm test chip are shown in Fig. 3. All 4 BTI components have a positive correlation with temperature while the power law exponent increases modestly with increasing temperatures. To extract the individual BTI components, we took the difference between the frequency shifts measured under different stress modes. Measured results show that PMOS NBTI is dominant followed by PMOS PBTI and NMOS NBTI.

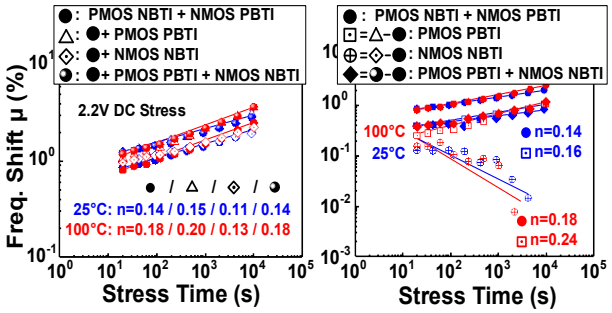


Figure 3. Test chip data showing combined (left) and individual (right) BTI induced shifts.

Keywords: bias temperature instability, analog reliability, ring oscillators, beat frequency, stress experiments

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

[1] G. Park et al., "An All BTI (PMOS NBTI, PMOS PBTI, NMOS NBTI, NMOS PBTI) Odometer based on a Dual Power Rail Ring Oscillator Array," (in preparation)

TASK 2712.018, TITLE TEST TECHNIQUES TO APPROACH SEVERAL DEFECT-PER-BILLION FOR POWER IC'S

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SIGNIFICANCE AND OBJECTIVES

This research designed, simulated and tested custom LDO and Buck Converter power ICs using additional bare-die test points to better anticipate part failures. The goal was to improve yield by culling power ICs with outlier subcircuit performance. Additional work characterized small-signal LDO control loop gain using IC external pins.

TECHNICAL APPROACH

Task researchers developed novel 65-mn CMOS LDOs and Buck Converter designs with internal IC test points for enhancing testing. Analyses and simulations of these designs were used to determine subcircuit performance inside the LDO and Buck Converter. Based on this work, a 65-nm CMOS LDO test IC and a Buck converter test IC were designed, fabricated and tested. The functional LDO Test IC was used to demostrate on-chip control loop gain and phase response measurements. Researchers also investigated methods to do control loop characterization quickly on ATE.

SUMMARY OF RESULTS

This year the project researchers 1) packaged a 65-nm CMOS Buck converter IC, made a custom test board for the converter and performed converter measurements, 2) developed a technique in collaboration with TI engineers to characterize LDO control-loop circuit elements from LDO measurements, and 3) developed test boards and performed small-signal control-loop measurements of an LDO test IC.

Also, researchers used measurements to identify outlier capacitors in the LDO control-loop from LDO IC pin measurements. This work was performed at TI Tucson, AZ.

The Buck converter IC testing strategy used extra probe points for DC and analog test on die. The researchers were guided by the SRC/TI program liaison engineers to develop a Buck converter test IC with an advanced Average Current Mode (ACM)-based control loop design. The researchers received 65-nm CMOS Buck converter ICs from Global Foundries in July 2019. These ICs were packaged and characterized.

Bench equipment measurements showed good Buck converter line regulation and overall performance. The Buck converter IC band-gap reference (BGR), the test MUXs, the control loop amplifiers and the regulation subcircuits performed well. The band-gap reference gave a supply independent reference voltage of 1.32 V, with the bias supply range of 2 V to 3.5 V. The Buck converter inner current control-loop and outer voltage control loop functioned as designed. The regulated output voltage was 1.65 V and output ripple was around ±10mV. The load current was regulated at 42 mA with a 40Ω internal load.

The task researchers developed methods for small-signal LDO control-loop characterization. These methods are important for determining LDO stability and reliability. The safety of automobile brake control systems can be compromised by unstable compensation in the LDO control-loop. Reseachers developed small-signal test boards for the LDO test IC that enabled switching out control loop elements (capacitors and resistors).

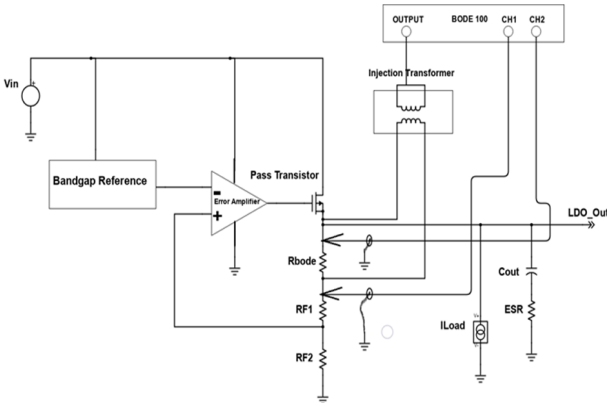

Figure 1. The LDO control loop measurement schematic.

Bode 100 analyzer probes were placed across R_{bode} to determine the control-loop small-signal performance. For PSRR measurement, a test signal was injected at V_{in} through an injection transformer. LDO control-loop cutoff frequency measurements showed the ability to determine outlier values of C_{out}, the critical compensation capacitor. Work is continuing to translate the servo-loop technique to a loadboard circuit for ATE-based testing.

Keywords: Test, Analog, Power, LDO, Buck Converter

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] A. Tulsiram, and W. Eisenstadt, "In Situ DC Loop Gain and Stability Measurement of LDOs using a Nulling Op-Amp Servo Loop," Fourth ART Workshop, Washington, D.C., USA, November 14-15, 2019.

TASK 2712.019, PRE-COMPUTED SECURITY PROTOCOLS FOR ENERGY HARVESTED IOT

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SIGNIFICANCE AND OBJECTIVES

We optimize the latency and energy-efficiency of Internet security protocols in energy-harvesting IoT. An energy-harvesting IoT device has a limited and leaky energy-storage capacity. The energy must be used as soon as possible after harvesting. With pre-computing techniques, cryptographic applications can instantly use the harvested energy. Pre-computed results are stored efficiently and reliably in non-volatile memory and are used to improve latency. We demonstrate precomputed random-number generation and cryptographic key-exchange, which are part of Internet security protocols.

TECHNICAL APPROACH

The feasibility and efficiency of the proposed techniques will be evaluated through an end-to-end demonstrator with an energy-efficient micro-controller and with a wireless communication front-end. We develop techniques to spread out computations over time by reformulating cryptographic algorithms as capable of generating coupons, which are precomputed portions of the algorithm. We propose techniques for coupon generation and their secure storage in non-volatile, possibly off-chip memories. We also consider and optimize the impact of precomputed security protocols on the communication cost and the storage cost. We validate the proposed approach by constructing a prototype implementation on an energy-harvesting oriented microcontroller-based platform.

SUMMARY OF RESULTS

When a computing platform temporarily loses power, it stores its current state in a checkpoint, such that it can recover and continue execution at the point just before storing the checkpoint. A checkpoint also holds pre-computed results (or coupons) to support the execution of a single cryptographic algorithm over multiple power-loss events. We performed a detailed security analysis of storing checkpoints in non-volatile memory. Also, a checkpoint also holds pre-computed results. We identify three possible scenarios that can threaten the security of the checkpointing process: a checkpoint may be snooped (eavesdropped upon), a checkpoint may be spoofed (tampered), and a checkpoint may be replayed. Each of these attacks can lead to loss of information security on the IoT device, or loss of control.

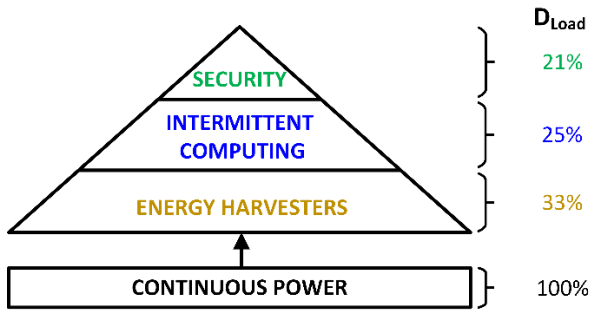

Figure 1. Performance Impact of Secure Intermittent Computing for ECDH.

We have evaluated the overhead of our proposed Secure Intermittent Computing protocol (SICP) for the case of cryptographic key exchange (ECDH). The prototype is constructed for a Texas Instruments MSP430FR5994 microcontroller that is performing key exchange under energy harvesting. The results are shown as a relative overhead compared to a continuously powered design. We measured the continuous ECDH operation to consume 6.3 mW and we assumed a 2 mW kinetic energy harvester, yielding a 33% duty cycle under intermittent operation. This duty cycle would imply key exchange takes 3 times as long under energy harvesting operation. The selected p160 curve for ECDH uses a 1211-byte checkpoint which must be stored and retrieved, and which reduces the duty cycle further to 25%. Implementing secure checkpoints, as enabled using SICP, adds additional overhead of encryption, and reduces the operation duty cycle to 21%. Hence, we conclude that the overhead of secure checkpointing on a realistic cryptographic protocol increases from 3x (only energy harvesting) to 5x (including secure checkpointing).

We have summarized out conclusions of the project in a forthcoming journal paper [1].

Keywords: cryptography, energy-harvesting, NVM applications, intermittent computing, MSP430

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] A. S. Krishnan, C. Suslowicz, P. Schaumont, "Secure and Stateful Power Transitions in Embedded Systems," IEEE Transactions on VLSI Systems, under review.

TASK 2712.021, DISTRIBUTED SILICON CIRCUITS AND SENSORS IN 3D-PRINTED SYSTEMS FOR WEARABLE IOT SENSORS

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YIĞIT MENGÜÇ, OREGON STATE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

There is an emerging set of applications that require stretchable, compliant electronics – including wearable devices, instrumented fabrics, and soft robots with distributed sensors and computation. In this project, we are working to demonstrate a fundamentally new method for the fabrication of stretchable, 3D-printed objects containing distributed sensors and silicon ICs.

TECHNICAL APPROACH

Developing stretchable electronics faces two primary challenges: integration of active semiconductor devices in elastic substrates and providing stretchable, conductive interconnects. In this project, we combine 3D printing of liquid metal materials and silicone rubber with PCB fabrication techniques to build solid 3D objects with electronic components distributed throughout. Silicon integrated circuits, used for computation, sensing, and actuation will be connected through liquid metal conductors confined to 3D microfluidic channels. Through additive, layer-by-layer construction, electronic devices can be inserted and connected throughout the 3D structure. We will also develop compact models for the interconnects, which will be used to design adaptable front-end circuits for stretchable interconnect interfaces.

SUMMARY OF RESULTS

Over the course of this project, we have demonstrated progress (Fig. 1) in printing multi-layer stretchable circuits using discrete components, extended strain testing of liquid metal paste material, and developed a compact modeling framework for stretchable interconnects. Specific outcomes have included:

- Demonstrated printing of sensors and analog and digital interconnects using discrete active and passive components [1,2].
- Extended testing of stretchable interconnects, demonstrating <5% change in resistance over 100,000 stretch cycles at 50% strain (1.5X) [4].
- Established a compact modeling framework for Cadence-compatible simulation of stretchable interconnects under static and dynamic strain [3].
- Printed antenna structures were developed, and a 2.4GHz liquid metal paste antenna structure was fabricated for future integration into stretchable circuits for wireless communication.

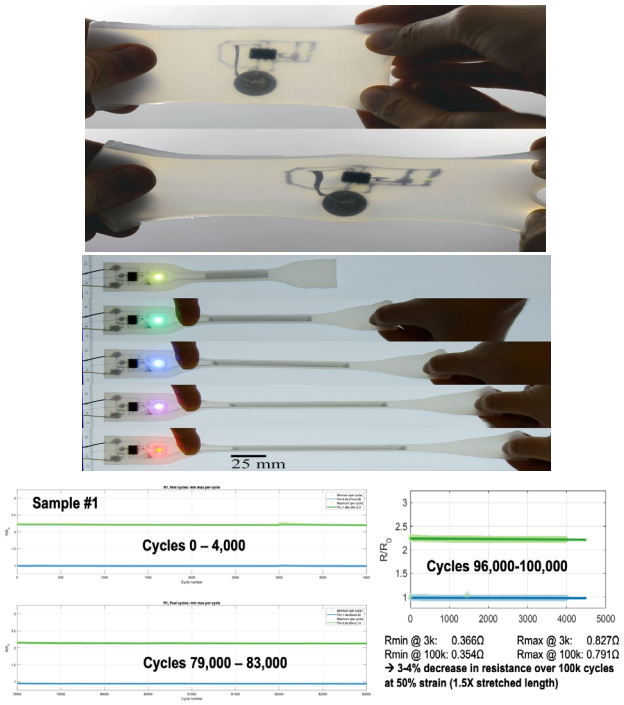

Figure 1. Printed stretchable circuits (top) with active and passive components [1]; 100,000 cycle strain data (bottom).

Keywords: Stretchable electronics; 3D printing; wearable devices; packaging; sensor interfaces

INDUSTRY INTERACTIONS

Texas Instruments, Intel, IBM

MAJOR PAPERS/PATENTS

[1] C. Votzke, U. Daalkhaijav, Y. Mengüç, and M.L. Johnston, "3D-printed liquid metal interconnects for stretchable electronics," *IEEE Sensors Journal*, vol. 19, no. 10, pp. 3832 - 3840, 2019.

[2] C. Votzke, U. Daalkhaijav, Y. Mengüç, and M.L. Johnston, "Highly-stretchable biomechanical strain sensor using printed liquid metal paste," 2018 BioCAS, Cleveland, OH, Oct. 2018.

[3] K. Clocker, C. Votzke, Y. Mengüç, and M.L. Johnston, "Compact modeling of stretchable printed liquid metal electrical interconnects," IEEE International Conference on Flexible and Printable Sensors and Systems, pp. 1-3, Jul. 2019.

[4] C. Votzke, K. Clocker, Y. Mengüç, and M.L. Johnston, "Electrical characterization of stretchable printed liquid metal interconnects under repeated cyclic loading," IEEE International Conference on Flexible and Printable Sensors and Systems, pp. 1-3, Jul. 2019.

TASK 2712.022, INTRINSIC IDENTIFIERS FOR DATABASE-FREE REMOTE AUTHENTICATION OF IOT EDGE DEVICES

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AMIT RANJAN TRIVEDI, UNIVERSITY OF ILLINOIS AT CHICAGO

SIGNIFICANCE AND OBJECTIVES

We present a novel low-power CMOS framework for nonparametric density estimation of time-series and anomaly detection. Anomalies in time-series data are detected samples with low-likelihood. We also introduce a current PUF based novel technique for concurrent IC and PCB integrity verification utilizing the onboard JTAG (Joint Test Action Group) structure. This approach can effectively protect ICs and PCBs from counterfeiting/cloning/in-field tampering attacks.

TECHNICAL APPROACH

Nonparametric density estimation is implemented using a kernel density estimation (KDE) methodology. KDE is realized using Gaussian kernel functions. Presented anomaly detection framework allows for programming parameters such as sliding-window length, kernel standard deviation, and likelihood threshold to ensure efficient detection. On the other hand, through physical measurements, we observe that the supply current in a PCB fluctuates primarily depending on the overall in-circuit switching activities in the boundary scan chain of the PCB, which is utilized to authenticate ICs, and PCBs concurrently, and detect in-field tampering.

SUMMARY OF RESULTS

Fig. 1 shows the overall architecture for unsupervised anomaly detection based on the nonparametric density estimation approach. Previously validated samples for KDE based PDF estimation are stored on the sample bank. An array of integrated current-steering DACs and hold-cells are used for the conversion of samples. A PDF learner estimates using pre-validated samples, and anomalies are detected by determining low-likelihood samples.

In the PCB verification technique, we deploy a custom hardware platform that consists of two chips (an FPGA and a microcontroller) in its boundary-scan architecture (BSA). Using the industry standard, we transmit test data into BSA, and meanwhile, perform hands-on current measurements at both chip level and PCB level over 20 boards to generate device-specific signatures that demonstrate high uniqueness, robustness, and randomness properties. The block diagram of the system level connection is depicted in Fig. 2. The experiments are run over 20 different PCBs of the same kind for five different supply voltage levels. Fig. 3(a) illustrates the percentage bit errors from every operating point, which demonstrates the robustness of the generated signatures. Finally, we conduct intentional alteration experiments by replacing the onboard FPGA to replicate the scenario of PCB tampering. The results (Figure 3(b)) indicate the successful detection of the intentional modifications introduced to the boundary scan chain of the PCB.

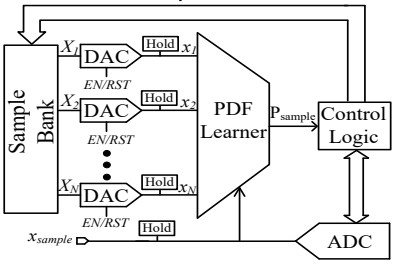


Figure 1. Overall architecture for anomaly detection.

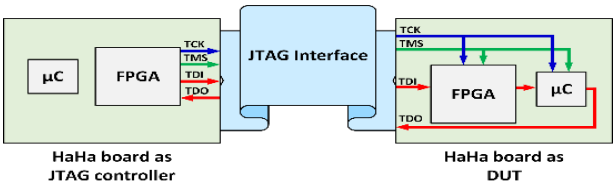
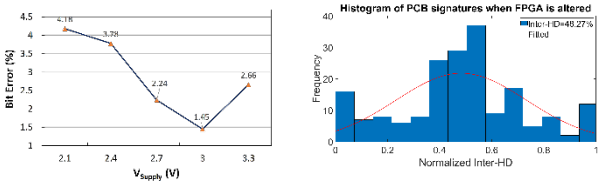


Figure 2. Block diagram of IC and PCB level connections.



(a) (b)

Figure 3. (a) V_{supply} variation results, (b) inter-Hamming distance results for intentional alteration experiments.

Keywords: Kernel density estimation, nonparametric, anomaly detection, authentication, Hamming, JTAG, PUF

INDUSTRY INTERACTIONS

Texas Instruments, Intel, IBM, NXP

MAJOR PAPERS/PATENTS

[1] A. R. Trivedi et. al., U.S. Provisional Patent, Jointly Filed with U. Illinois at Chicago, U. Florida/Under Process.
[2] S. Bhunia et. al., U.S. Provisional Patent, Filed with U. Florida/Under Process, 62/935,440.
[3] S.D. Paul et. al., "Systematic Integrity Verification of Printed Circuit Board Using JTAG Infrastructure," submitted to ACM JETC.

TASK 2712.026, FAULT CHARACTERIZATION AND DEGRADATION MONITORING OF SIC DEVICES

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SIGNIFICANCE AND OBJECTIVES

The long-term reliability of SiC MOSFETs is a concern limiting their wide application in industry. This research investigates the performance change of the SiC MOSFETs over aging, and develops condition monitoring methods to determine the state-of-health of the device in real applications.

TECHNICAL APPROACH

Utilizing the DC power cycling test setup designed previously, the loss change of the SiC MOSFETs due to aging is investigated with the aid of curve tracer and double pulse test bench. The parameter shifts are recorded over the power cycling process, and new aging precursors like on-resistance at different gate bias and body diode voltage drops are identified. Detection circuits are developed accordingly to measure these aging precursors, and the state-of-health condition monitoring is realized for SiC MOSFETs.

SUMMARY OF RESULTS

The impact of aging on the switching loss of SiC MOSFETs is being investigated. Due to the aging, the turn-on loss of the SiC MOSFETs is increased as indicated in Fig. 1. The loss change is more significant at the high-current and fast switching conditions. For instance, more than 36.8% increase of turn-on loss is observed at 600 V/20 A with 0-Ω gate resistance. The main reason for this loss change is caused by the package degradation of the device, and detailed reason is analyzed in this research work.

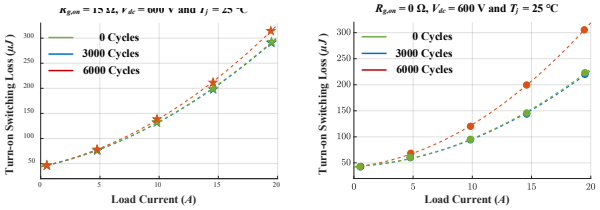

Figure 1. Turn-on loss change at different conditions.

In terms of the condition monitoring, the saturation and ohmic region drain-source resistances of the device are utilized as aging precursors for die and package, respectively. As shown in Fig. 2, the saturation current of the device decreases as the gate oxide starts to degrade. Therefore, a measurement circuit is proposed to sense the saturation-region resistance for gate oxide degradation monitoring. On the other hand, a sudden change of ohmic on-resistance is observed in Fig. 2, and it is caused by the package degradation. The ohmic resistance is also measured in the circuit to monitor the package degradation in SiC MOSFETs.

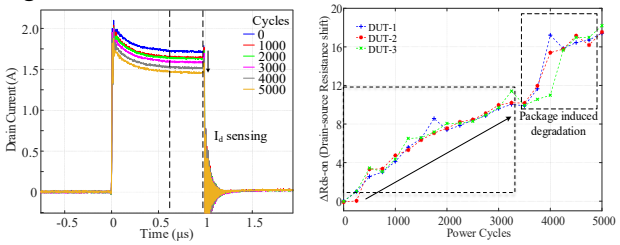

Figure 2. On-board measured saturation current and resistance change due to the gate oxide degradation.

Similarly, the body diode voltage V_{SD} is also a good aging precursor: the V_{SD} change at zero gate bias and low current can indicate the gate oxide degradation while the V_{SD} change at negative bias and large current (0.5 A) reflect the package degradation. A circuit is proposed as shown in Figure 3 to provide a complete condition monitoring of the gate oxide and package degradations in SiC MOSFETs.

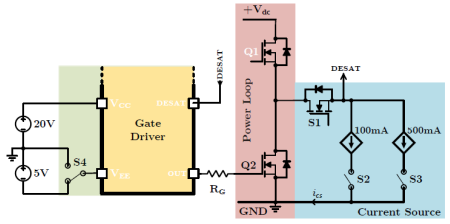

Figure 3. Body diode voltage measurement circuit for condition monitoring of SiC MOSFETs.

Keywords: SiC MOSFETs, aging precursor, performance degradation, condition monitoring, reliability

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] F. Yang, et al., "Investigation of Aging's Effect on the Conduction and Switching Loss in SiC MOSFETs," ECCE, Baltimore, MD, USA, 2019.

[2] S. Pu, et al., "A Practical On-board SiC MOSFET Condition Monitoring Technique for Aging Detection," Accepted to in *IEEE Trans. Ind. Appl.*

[3] E. Ugur, et al., "A New Complete Condition Monitoring Method for SiC Power MOSFETs," in *IEEE Trans. Ind. Electron*.

[4] Two UTD, SRC joint patents.

TASK 2712.029, NOVEL SUPER-RESOLUTION AND MIMO TECHNIQUES FOR AUTOMOTIVE AND EMERGING RADAR APPLICATIONS

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SIGNIFICANCE AND OBJECTIVES

As opposed to camera based sensors, millimiter wave (mmWave) radar technology provides the ability to meet privacy requirements in addition to being unobtrusive and non-intrusive, with its capability of detecting motion and vital signs from a distance, while maintaining accuracy. In this report, vital signs detection algorithms using mmWave frequency modulated continuous wave (FMCW) radar are presented.

TECHNICAL APPROACH

The resolution capabilities of mmWave FMCW radar sensors for range, Doppler and angle build the premise for various in-home applications. Here, in-home applications span vital signs monitoring of children, patients and elderly as well as non-intrusive fall detection of the elderly and security monitoring and others. On top of that, solutions to pre-existing problems in these application areas extend naturally to other outdoor applications such as driver monitoring and search and rescue operations.

Research for non-contact vital signs detection using radars spans various sensor technologies with its potential to measure and detect disorders in breathing and heart rate. Current availability and proliferation of low cost, high resolution and easily integrable radar sensors, operating in the mm-Wave region makes stand-off detection of cardio-pulmonary signals a highly promising application.

SUMMARY OF RESULTS

In regards to human vital signs monitoring, high range resolution of mm-Wave sensors gives us the ability to separate echoes from different body parts including torso and head. In addition, use of multiple transmit and receive antennas add the ability to resolve scatterers in angular domain. This becomes vitally important in real life applications where the subject is no longer in a controlled environment. This is because there are various problems that come with detecting heart rate signals, especially given that it is dominated by the much stronger respiration signal. The harmonics of the respiration signal, the intermodulation and cross product terms all cause erroneous detection of heart rate signals. Echoes from human subjects are intricate and hence the traditional spectral cleaning algorithms do not always give accurate estimation. We use a FMCW radar in MIMO configuration to spatially scan a human subject using transmit and receive beamforming methods in specific locations of the body. With physiological differences in subjects, scanning multiple points in the body provides a more reliable estimation technique for heart rate detection. In addition, diverging from a point reflector subject model, we introduce a strategy to incorporate Doppler signatures at multiple range bins as well as multiple angular bins to reduce the probability of erroneous heart rate estimation. The problems of heart rate detection is further compounded by small scale motions of the subject, such as talking and intermittent head movements. Our proposed strategy offers an improved detection of the heart rate even during instances of such small scale motion and does not rely on tracking of the peaks over time, where variations of heart rate may still cause erroneous detection.

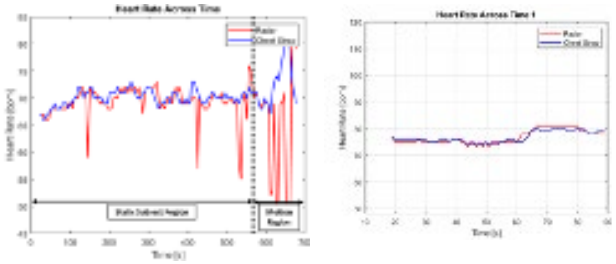

Figure 1. Heart rate monitoring. Left: Motion of the subject clearly creates estimation significant estimation errors with classical algorithms. Right: An example of heart-rate detection improvement obtained by means of motion compensation.

With respect to heart rate measurements, preliminary results have shown effective tracking of a subjects heart rate over time. An example is shown in Fig. 1. The mean squared heart rate errors are approximately 1 bpm for a static single subject when compared to a wearable chest strap. Our approach can be applied to various real life applications of vital sign monitoring.

Keywords: mm-Wave radar, FMCW, vital sign monitoring

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] M. E. Yanik, D. Wang, and M. Torlak, "3-D MIMO-SAR Imaging Using Multi-Chip Cascaded Millimeter-Wave Sensors," Proc. IEEE GlobalSip, Nov. 2019, Ottawa, Canada, pp. 1-6.

[2] A. Baral, B. Upadhyay, and M. Torlak, "Performance Comparison of Vital Signs Detection using 24 GHz and 77 GHz Radars," *SRC Techon*, Sept. 2019, Austin, TX.

TASK 2810.002, SECURITY-AWARE DYNAMIC POWER MANAGEMENT FOR SYSTEM-ON-CHIPS

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SIGNIFICANCE AND OBJECTIVES

The proposed research investigates the energy-security trade-offs associated with Dynamic Power Management (DPM). The proposed effort will develop methodology to characterize security implications of DPM in SoCs and design circuit/system techniques to co-optimize security and energy-efficiency of DPM.

TECHNICAL APPROACH

This effort will pursue a cross-layer approach to understand the energy-security trade-offs in Dynamic Voltage Frequency Scaling (DVFS). First, we will design power domains that are secure against power-/EM- side-channel analysis by leveraging the distributed integrated voltage regulators. Next we will investigate energy-security trade-off at the chip level by focusing on the DVFS controller and algorithm. Finally we will explore an integrated approach considering secure power domains and secure DVFS controllers.

SUMMARY OF RESULTS

Side-channel Analysis of PRINCE: We present a 65-nm test-chip of a dual-mode PRINCE encryption engine, configurable between pipelined and fully unrolled modes. Correlation Power and EM analyses on test-chip measurements show minimal exploitability of leakage from registers, implying that unrolled PRINCE can be pipelined without significantly hurting its side channel robustness. The overall system has a minimum MTD (Minimum Trace to Disclose) of 460K and a projected maximum throughput of 502 Mega encryptions per second.

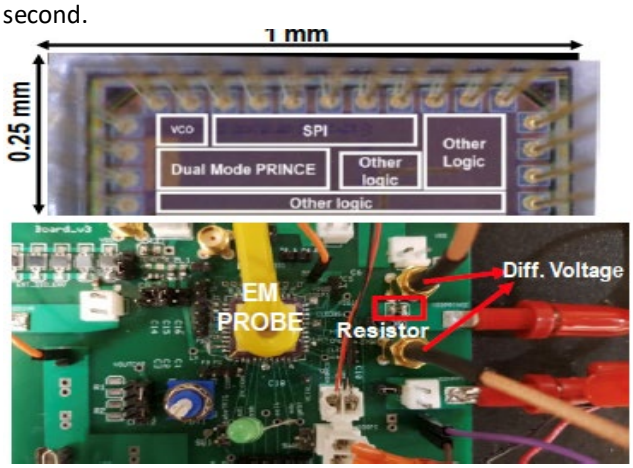

Figure 1. The architecture for digital LDO based power and electromagnetic emission based side channel security.

Metrics	Mode	
	Unrolled	Pipelined
Max Freq. (@ 1.1V)	102 MHz	496MHz
Encryption Latency	1 cycle	11 cycles
Projected Throughput	102 M enc/s	496 M enc/s
Power @ Max Freq.	1.76mW	8.04mW

	This work	ISSC '19 [5]	VLSI '16 [2]
Technology	65nm	130nm	28nm
Crypto Engine	Dual-Mode PRINCE	S-AES + P-AES	Unrolled PRINCE
Power	1.06mW @80MHz	10.9mW @ 80Mhz,	9.98mW @ 400 MHz
Gate count	9,301	N/A	N/A
Area	0.0774mm^2	‡0.062mm^2	0.0074 mm^2
MTD	460K @ 480 MHz**	< 10K* @ 86 MHz‡	N/A

Figure 2. Performance Summary of Test-chip.

DVFS based Application Inferencing and Malware Detection: We demonstrate Dynamic Voltage and Frequency Scaling (DVFS) states form a signature pertinent to an application, and its run-time variations comprises of features essential for securing IoT devices against malware attacks. We have demonstrated this proof of concept by performing experimental analysis on a Snapdragon 820 mobile processor, hosting Android operating system (OS). We developed a supervised machine learning model for application classification and malware identification by extracting features from the DVFS states time-series. The experimental results show >0.7 F1 score in classifying different android benchmarks and >0.88 in classifying benign and malware applications, when evaluated across different DVFS governors. We also performed power measurements under different governors to evaluate power-security aware governor. We have observed higher detection accuracy and lower power dissipation under settings of on-demand governor.

Keywords: Secure, Side-channel, Dynamic Power Management, Integrated Voltage Regulator, Dynamic Voltage Frequency Scaling

INDUSTRY INTERACTIONS

Intel, IBM

MAJOR PAPERS/PATENTS

[1] A. Singh, et al., "Enhanced Power & Electromagnetic SCA Resistance of Encryption Engines via a Security-Aware Integrated All-Digital LDO," IEEE Journal of Solid State Circuits (JSSC), vol. 55, no. 2 , Feb. 2020, pp. 478 – 493.

[2] N. M. Rahman, et al., "A Configurable Dual-Mode PRINCE Cipher with Security Aware Pipelining in 65nm for High Throughput Applications," IEEE Custom Integrated Circuit Conference (CICC), March 2020.

[3] N. Chawla, et al, "Application Inference using Machine Learning based Side Channel Analysis," IEEE International Joint Conference on Neural Network (IJCNN), 2019.

TASK 2810.005, CIRCUIT DESIGN FOR ESD AND SUPPLY NOISE MITIGATION

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SIGNIFICANCE AND OBJECTIVES

This project seeks to develop (1) IC-level power distribution networks that promote power integrity even in the presence of power-on ESD, and (2) understand and mitigate latch-up that occurs in response to power-on ESD.

TECHNICAL APPROACH

This work identifies ESD-induced reliability hazards, including latch-up, and evaluates solutions. There is a special emphasis on power-on ESD, such as that resulting from system-level discharges. Laboratory characterization of custom-designed test chips is the primary method used to investigate reliability hazards and evaluate proposed solutions. Some of the failures addressed in this work result from supply noise and an effort is made to accurately measure the on-chip noise; board-level measurements are generally unsuitable since the test chips are assembled in wire bonded packages and the package inductance decouples the noise signals at the board and chip levels. Therefore, the researchers develop and deploy on-chip noise sensors. Measurement results are interpreted with the aid of circuit simulation and electromagnetic (FDTD and FEM) simulation.

SUMMARY OF RESULTS

On the basis of test chip measurements and circuit simulation, we completed the analysis of system-level ESD-induced supply noise for ICs. The integrity of the power supply for the core logic circuits can be maintained by separating the ground nets of the IO and the core logic supplies or by eliminating the board-level decoupling capacitance on an internally-regulated core power supply. It must be noted that complete isolation of the various on-chip ground nets is not permitted due to component-level ESD requirements. ESD-induced soft errors in a microcontroller (MCU) were investigated [1]. A previously undocumented cause of latch-up in circuits with reverse body bias capability was identified. The latch-up is triggered by power-on ESD and the root cause is an induced forward-bias on the source-body diodes of the NMOS transistors. The forward-bias arises because the ESD current induces potential differences across the body bias net and, thanks to the RBB scheme, the source bias does not track those variations. It was demonstrated that circuit simulation may be used to assess the latch-up susceptibility of a given design (Fig. 1). In simulation and analysis, we have demonstrated that ESD protection circuits intended for system-level protection (i.e., power-on ESD) can reduce the amplitude of simultaneous switching noise (SSN) by several hundred millivolts. The test chip designed to validate the analysis is fully functional; however, precise measurement of the SSN has not yet been achieved due to extremely large current transients associated with the SSN induced noise on the PCB power nets. The PCB design is being re-executed with the aid of electromagnetic simulation.

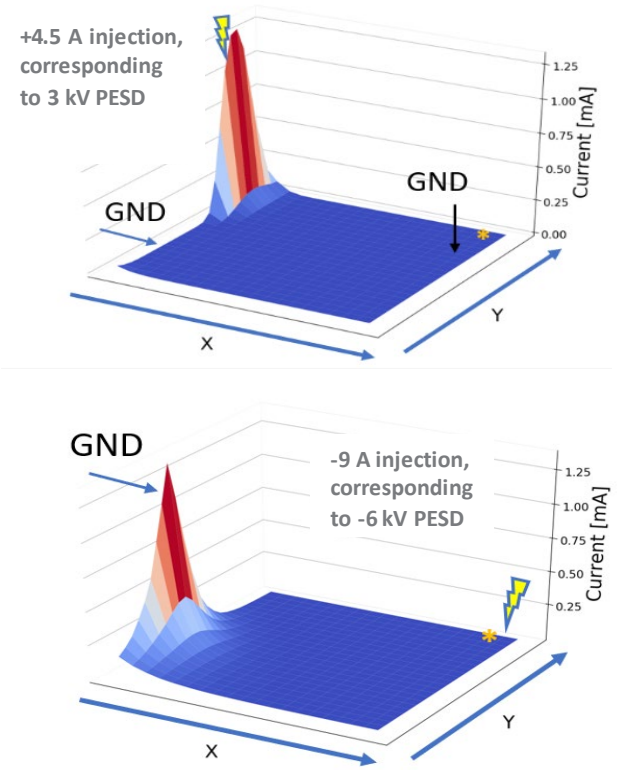

Figure 1. Circuit simulation of MCU with RBB. Current in the NMOS body diodes is plotted (base current for parasitic PNPN). PMC is located near the asterisk. Emission microscopy reveals that the simulation correctly predicts where latch-up occurs.

Keywords: ESD, latch-up, integrated voltage regulator, simultaneous switching noise, rail clamp

INDUSTRY INTERACTIONS

Texas Instruments, NXP, Intel

MAJOR PAPERS/PATENTS

[1] S. Vora and E. Rosenbaum, "Analysis of system-level ESD-induced soft failures in a CMOS microcontroller," *IEEE Transactions on Electromagnetic Compatability*, Early Access, doi: 10.1109/TEMC.2020.2986971.

TASK 2810.014, DEEP LEARNING SOLUTIONS FOR ADAS: FROM ALGORITHMS TO REAL-WORLD DRIVING EVALUATIONS

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NAOFAL AL-DHAHIR, THE UNIVERSITY OF TEXAS AT DALLAS

SIGNIFICANCE AND OBJECTIVES

Investigate deep-learning-based algorithms and evaluate their performance using fusion of sensing technologies (regular cameras, infrared lenses, RADAR) to estimate the driver's visual attention in real-world driving conditions. The project explores novel probabilistic models of visual attention, creating shared representation across multiple sensing technologies.

TECHNICAL APPROACH

We analyze alternative sensing technologies suitable for head pose estimation for in-vehicle applications, creating novel visual attention models (gaze). We perform real-world driving tests to evaluate alternative sensors that are appropriate for head pose estimation. We develop novel probabilistic models of the visual attention of the drivers describing confidence regions of the gaze given the position and orientations of the driver's head using deep learning. We propose multimodal deep learning frameworks to fuse sensors using shared layer representation between modalities, creating robust and accurate solutions regardless of the environment.

SUMMARY OF RESULTS

1) Data collection: We have collected the Multimodal Driver Monitoring Database, which has multiple sensors to study visual attention of the driver (four cameras, depth cameras, and CAN-Bus). The data has 60 drivers. The effort was interrupted by COVID-19 (target was 100 drivers).

2) Head Pose Estimation from Point-Cloud Data: Head pose estimation has been a key task in computer vision since a broad range of applications often requires accurate information about the orientation of the head. Achieving this goal with regular RGB cameras faces challenges in automotive applications due to occlusions, extreme head poses and sudden changes in illumination. We proposed a novel point-cloud based deep learning approach to estimate the driver's head pose from depth camera data (Fig. 1), addressing these challenges. The proposed algorithm is inspired by the PointNet++ framework, where points are sampled and grouped before extracting discriminative features. Our proposed approach achieves predictions that are almost always more reliable than the state-of-the-art head pose estimation methods based on regular cameras. It provides predictions even for extreme rotations, which is not the case for the other methods. This is the first study on head pose estimation using deep learning on point-cloud data.

Figure 1. algorithm for point-cloud head pose estimation.

3) Gaze estimation from regular cameras: We used regular RGB cameras to assess the visual attention of the driver, producing statistical estimations for the elevation and azimuth angles of the driver's gaze. The proposed gaze estimation algorithms can help in evaluating and analyzing driver distractions, and producing information to alarm the driver in case of distraction. In addition, they can play a key role in deciding whether to hand control to a human operator in level 3 and 4 autonomous vehicles. We detect both the face and the eyes of the driver to be able to observe subtle gaze features and feed them to our developed deep learning architecture that outputs customized estimations for each gaze angle. We produce high-accuracy and high-precision elevation and azimuth gaze angles estimations, demostrating the generalization capabilities of our gaze estimation algorithm.

Keywords: ADAS, head pose estimation, deep learning, visual attention, multimodal sensing

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] T. Hu, S. Jha, and C. Busso, "Robust driver head pose estimation in naturalistic conditions from point-cloud data," in IEEE Intelligent Vehicles Symposium (IV2020), Las Vegas, NV USA, June 2020.

[2] S. Jha and C. Busso. Estimation of driver's gaze region from head position and orientation using probabilistic confidence regions. IEEE Trans. on Intelligent Transportation, to be submitted, June 2020.

[3] S. Jha, M. Marzban, T. Hu, M.H Mahmoud, N. Al-Dhahir and C. Busso. Multimodal Driver Monitoring Database. IEEE Trans. on Intelligent Transportation, to be submitted, July 2020.

[4] M. Marzban, A. Seripali, S. Jha, C. Busso, N. Al-Dhahir, "A New Deep Learning Approach for Customized Gaze Regions Estimation in Naturalistic Driving Environments" to be submitted to IEEE Trans. on Intelligent Transportation, to be submitted July 2020.

TASK 2810.016, CONDITION MONITORING OF INDUSTRIAL/ AUTOMOTIVE DRIVE COMPONENTS THROUGH LEAKAGE FLUX

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SIGNIFICANCE AND OBJECTIVES

Condition monitoring of electrical motors are performed by using parameters like current, back emf, vibration etc. In this research, the stray magnetic field around the motor is used for detecting the inter-turn short circuit fault and temperature estimation of permanent magnets in permanent magnet synchronous motor (PMSM).

TECHNICAL APPROACH

Electromechanical energy conversion in electrical motors takes place via magnetic field. Any fault occurred in a motor is more likely to have fault signatures in its air gap magnetic field. Since it is not possible to measure the airgap magnetic field, the stray magnetic field around the motor reflects the variation in airgap magnetic field which makes it a promising condition monitoring tool.

SUMMARY OF RESULTS

Stator winding fault is one of the common faults in electric motors. Most of the winding faults are initiated as an inter-turn short circuit fault. In this research we have proposed that the third harmonic component of stray magnetic field can be used as a reliable signature to detect and locate the fault. The proposed method works through out the entire range of operation.

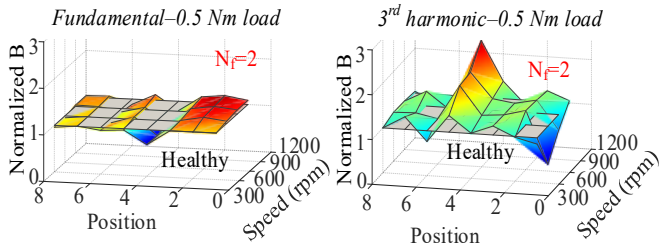


Figure 1. Fault signature in third harmonic component of stray magnetic field in PMSM.

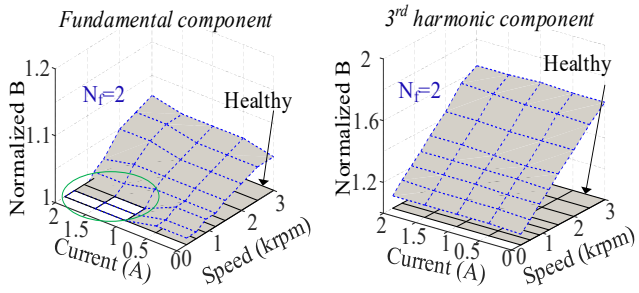
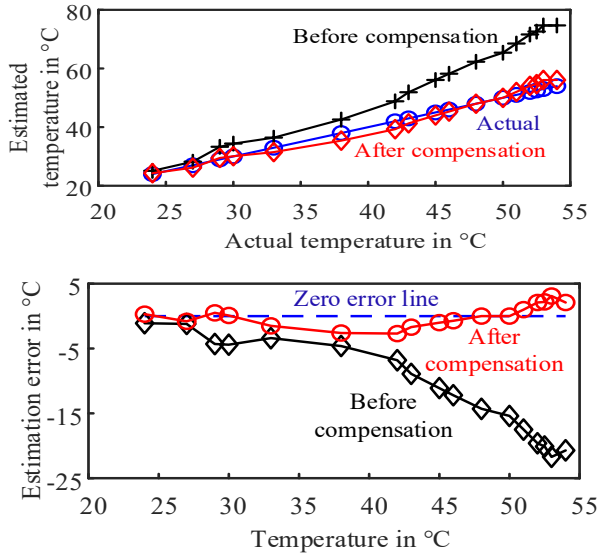


Figure 2. Stray magnetic field at the fault location.

Temperature monitoring of permanent magnets are essential since the magnets are susceptible to thermal demagnetization. In this research, we are proposing a method to estimate the temperatue of permanent magnets through the stray magnetic field.

The change in permanent magnet flux due to temperature affects the stray magnetic field around the motor. It is also affected by the permeability variation of steel due to temperature and the magnetic field due to the stator current. A compensation coefficient is introduced to isolate the stray magnetic field variation due to permanent magnet and temperature is estimated with an error less than 5°C.



Keywords: stray magnetic flux, PMSM, inter-turn short circuit fault, permanet magnet temperature estimation

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Y. Qi., M. Zafarani, V. Gurusamy and B. Akin, "Advanced Severity Monitoring of Inter Turn Short Circuit Faults in PMSMs," in IEEE Transactions on Transportation Electrification.doi: 10.1109/TTE.2019.2913357.

[2] V. Gurusamy, C., Li, B. Akin, "A Stray Magnetic Flux Based Robust Diagnosis Method for Detection and Location of Interturn Short Circuit Fault in PMSM" IEEE Transactions on Instrumentation & Measurement, under review.

TASK 2810.017, RELIABILITY STUDY OF E-MODE GAN HEMT DEVICES

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SIGNIFICANCE AND OBJECTIVES

AlGaN/GaN High Electron Mobility Transistors (HEMTs) are excellent candidates for high-voltage power switching applications. This work involves TDDB of commercial p-GaN gate E-mode HEMTs. Failed devices were inspected employing SEM/FIB to precisely locate the failure and HR TEM imaging to indentify the physical mechanism for failure.

TECHNICAL APPROACH

Commercially available AlGaN/GaN E-mode HEMTs were stressed at different gate voltage and temperature to understand the device behavior and time to fail variation under the same. Devices were tested until failure and were subjected to Failure Analysis. Furthermore, the failed area was precisely prepared using FIB and studied under HR TEM for microscopic changes occurring at the active device area to understand the physical nature of breakdown.

SUMMARY OF RESULTS

Stressing voltage and temperature play vital roles in device performance. Fig. 1 shows the TDDB of similar devices studied at the same stress voltage (7V) but different temperatures. Fig. 1(b) shows the device failure lifetime is very close for the devices at high temperature, whereas TTF for similar devices at room temperature is random. The occurrence and the magnitude of oscillation are less at high temperatures, which is one possible reason for the consistent lifetime of devices. Also, noise appears imposed on the I_G as the device life comes near to the end, which is not visible in Fig. 1 (a) due to excessive oscillations.

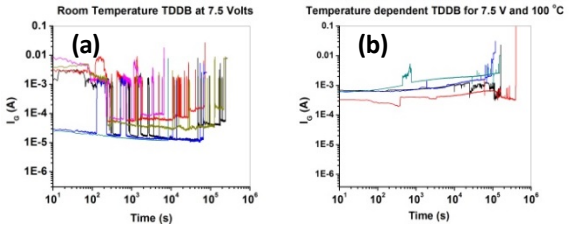

Figure 1. TDDB stress data at 7.5 V and 25/100 °C.

Fig. 2 shows gate stressing at 8V and 100 °C, and the device lifetime is almost one order of magnitude less. It shows a similar variation in TTF and the frequency of oscillation is lesser than at 7.5 V and 100 C. Fig. 2 (b) shows a Weibull plot for the devices for TTF for all the testing conditions. As seen in the Weibull plot, the device displays a narrow spread at 7.5 V and 100 C. At higher voltages, TTF varies a lot, and at room temperature, the oscillations make the device failure less consistent.

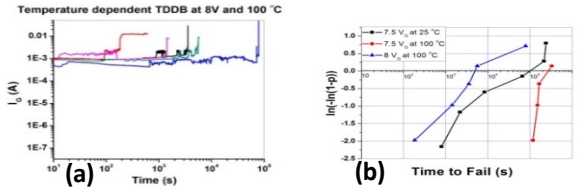

Figure 2. (a) TDDB stress data and (b) Weibull plot.

Fig. 3 shows SEM/HRTEM images of failures. The failed device shows damages at three locations; (i) AlGaN/GaN interface, (ii) gate fingers, and (iii) areas adjacent to the gate. In some devices, electric discharge lines were also observed. SEM images show extensive damage to gate fingers and localized deformation. Lift out samples from failure sites were characterized, and HRTEM images are shown in Figs. 3(c)-(e). Fig. 3(c) shows a vertical crack extending to the substrate because of residual stress relaxation resulting in delamination in the GaN layer. Fig. 3(d) shows severe plastic deformation on the gate as a result of the reverse piezoelectric effect. AlGaN/GaN heterostructure damage is seen in Fig. 3(e), and this damage is observed throughout the AlGaN/Gan interface because of lattice mismatch and heavy current density.

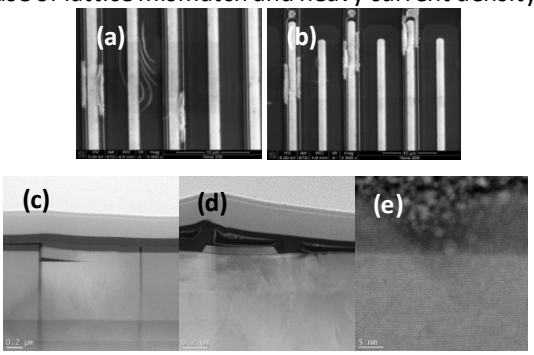

Figure 3. SEM and TEM images distinctive failure locations on active device area.

Work on pulse measurements and constant current stressing along with in-situ TEM biasing is in progress.

Keywords: E-mode GaN HEMT device, Reliability, Failure mechanism

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

TASK 2810.021 AND 2810.022, A COLLABORATIVE MACHINE LEARNING APPROACH TO FAST AND HIGH-FIDELITY DESIGN PREDICTION

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YIRAN CHEN, DUKE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

Synthesis parameter tuning is critical for circuit performance and power, yet, has long been a time consuming manual process. The objective of this work is to develop a machine learning approach for automating this process. The research result will facilitate fast chip design closure as well as accelerated time to market.

TECHNICAL APPROACH

We introduce FIST, a machine learning-based automatic parameter tuning methodology that aims to find the best design quality with a limited number of trials. Instead of merely plugging in machine learning engines, we develop clustering and approximate sampling techniques for improving tuning efficiency. The feature extraction in this method can reuse knowledge from prior designs. Furthermore, we leverage a state-of-the-art XGBoost model and propose a novel dynamic tree technique to overcome overfitting.

SUMMARY OF RESULTS

FIST learns previous knowledge from those already synthesized designs. The knowledge includes each parameter's impact (importance) on solution quality. We assume the samples with the same values on those important features result in similar final solution qualities.

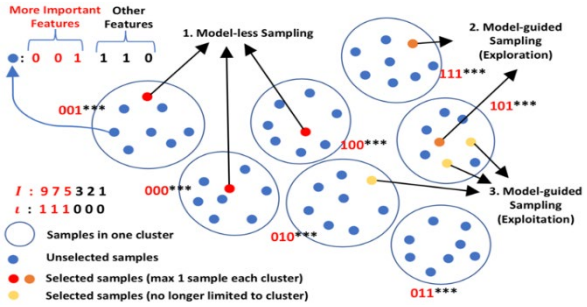

Figure 1. The three major sampling stages of FIST model.

An example of the proposed FIST model is depicted in Fig. 1. It consists of three major stages. 1. Calculate the important features according to previous data, then cluster the samples with the same values on these features. We assume the solution qualities of samples in the same cluster are the same. 2. Select one sample, get its solution quality, then put the whole cluster into the training set. Train an XGBoost machine learning model every time when the training set is updated. 3. Keep selecting by the whole cluster until we have accumulated enough samples.

Fig. 2 shows the result of FIST measured by the best solution rank with the same sampling cost. Compared to the baselines, FIST provides 53% better solution quality.

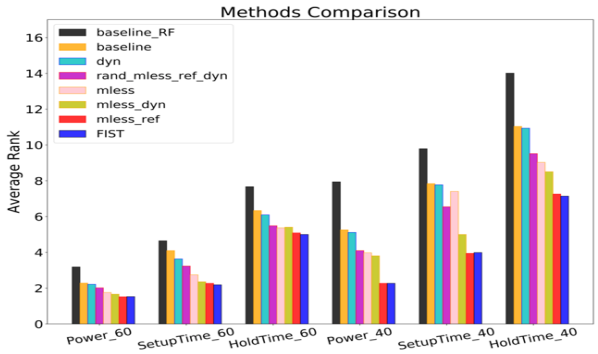

Figure 2. The best solution's rank with the same sampling cost.

Fig. 3 shows the parameter tuning results on an industrial design. The yellow points are the best design qualities achieved by FIST, considering the timing-area trade-off. The black points are hand-tuned solutions from experienced VLSI designers. The comparison shows that FIST outperforms the engineer's solution by ~2% in area.

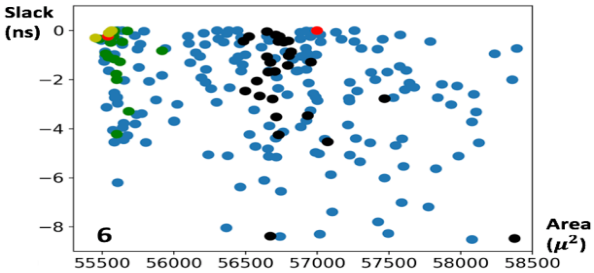

Figure 3. The design quality tuned by FIST on industrial design.

Keywords: design flow parameter tuning, search space exploration, machine learning, Random Forest, XGBoost

INDUSTRY INTERACTIONS

IBM, ARM, NXP, Mentor, A Siemens Business

MAJOR PAPERS/PATENTS

[1] Z. Xie, G.-Q. Gang, Y.-H. Huang, H. Ren, Y. Zhang, B. Khailany, S.-Y. Fang, J. Hu, Y. Chen, and E. C. Barboza, "FIST: A Feature-Importance Sampling and Tree-Based Method for Automatic Design Flow Parameter Tuning," *Asia and South Pacific Design Automation Conference*, 2020, Beijing, China.

TASK 2810.023, MACHINE LEARNING DRIVEN AUTOMATIC MIXED-SIGNAL DESIGN VERIFICATION-VALIDATION FOR AUTOMOTIVE APPLICATIONS

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SIGNIFICANCE AND OBJECTIVES

The research will develop the next generation of pre and post-silicon design model extraction and validation tools that will allow complex mixed-signal systems to be tested and debugged automatically 10X-100X more efficiently (speed, accuracy) than current techniques while providing diagnosis down to the physical level for quick design fixes.

TECHNICAL APPROACH

We develop behavioral circuit models automatically from netlist descriptions *using machine learning algorithms.* Machine learning kernels are inserted into circuit netlists to learn differential behaviors (between modeled vs. netlist) for design bug diagnosis with *a minimum number of circuit level simulations.* The goal is to speed up design bug detection and debug time (cost) by 10X-100X *using test stimulus generation techniques that collaborate closely with machine learning driven model generation algorithms.* A further objective is to automate the process of design debug, localize the debugging effort to the smallest possible region of the physical layout of the circuitry.

SUMMARY OF RESULTS

The proposed model synthesis and debug algorithms have been demonstrated on various circuits including linear low-dropout regulators, RF receivers, and analog-to-digital converters.

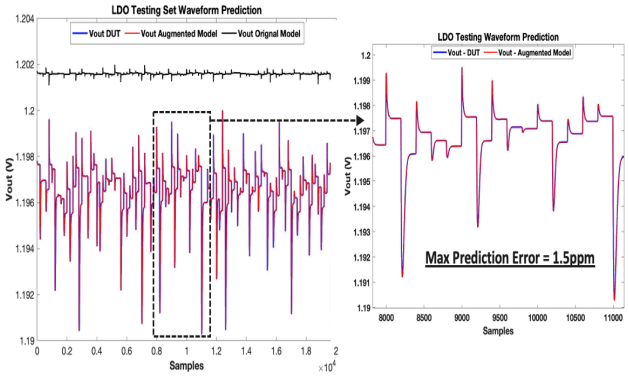

Figure 1. LDO model/circuit output after convergence.

Fig. 1 above shows a successful model generation for a low dropout regulator designed in 4-5nm technology. The trained synthesized model achieved a small residual error of 1.5ppm with a > 60x simulation speed improvement over SPICE-based simulator.

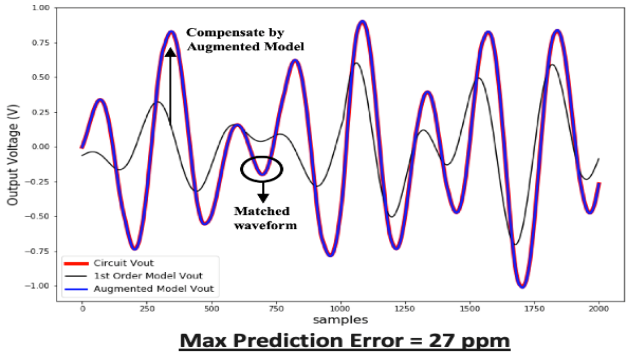

Figure 2. RF model/circuit output after convergence.

Fig. 2 shows the baseband response of a direct-down conversion RF receiver using the same model synthesis algorithm. A maximum residue error of only 27ppm is achieved with a > 200x simulation speedup. In addition to the model synthesis, an optimization-based design bug diagnosis algorithm is developed to detect and localize bugs within a sub-module of a system. The algorithm is fully integrated with a SPICE circuit simulator and is capable of modeling subcircuits within a feedback loop.

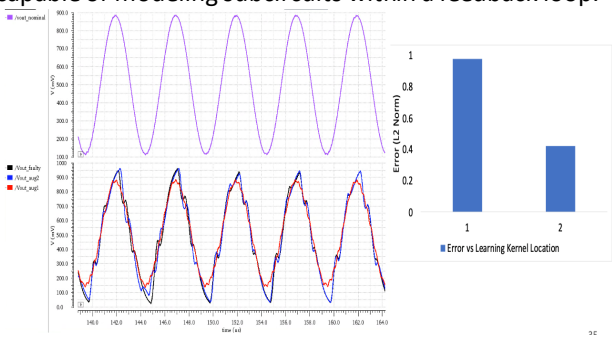

Figure 3. Diagnosis on a 2nd order sigma-delta modulator.

Fig. 3 demostrates the result of a successful debug of 2nd stage integrator design bug inside a 2nd order sigma delta modulator. The diagnosis algorithm also successfully localized a design bug in an RF receiver.

Keywords: Design validation, debug, test generation, machine learning

INDUSTRY INTERACTIONS

Texas Instruments, Intel, NXP

MAJOR PAPERS/PATENTS

[1] Iterative Testing and Learning Driven Mixed-Signal Design Validation and Diagnosis, Workshop Presentation, FMCAD2019.

TASK 2810.025, MACHINE LEARNING-BASED LAYOUT ANALYSIS AND NETLIST OPTIMIZATION FOR DEFECT TOLERANCE AND DESIGN ROBUSTNESS TO PROCESS IMPERFECTIONS AND VARIATIONS

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SIGNIFICANCE AND OBJECTIVES

This work focuses on using Machine Learning (ML) towards obtaining defect tolerant IC layouts and netlists. Currently, we focus on: (i) Developing coverage metrics and confidence estimation methods to enhance layout Design Space Exploration (DSE), (ii) Developing methods to characterize the effects of design-process interactions on timing, thereby, synthesizing defect tolerant netlists.

TECHNICAL APPROACH

Layout-level methods: We improve the robustness of layouts through ML-based lithographic hotspot detection. Performance of a hotspot detection model largely depends on the quality of the training dataset. Therefore, we seek to increase the information-theoretic content of the training dataset by synthetically generating all possible DRC-clean patterns for a given technology node.

Netlist-level methods: Our methods include characterization of the cell library database for delay defects, quantification of defect tolerance of netlists, and usage of defect characterization to drive the identification and rewiring/redesigning of netlists, to increase delay defect tolerance. An overview of the proposed netlist optimization procedure is shown in Fig. 1.

SUMMARY OF RESULTS

ML-based layout analysis: While our final goal is to improve hotspot detection through quantification / coverage estimation of the design space, in this phase of the project, we focused on performing a detailed study of the state-of-the-art and establishing a clear baseline. Consequently, we highlighted the common *fallacies* pervasive in the literature, identified several *pitfalls* in contemporary benchmarks, and offered *marching orders or best recommendations* towards improving the quality of hotspot detection. We also developed and publicly released a new set of benchmarks, which are now popularly known as *ICCAD'19 benchmarks*, to effectively evaluate ML-based hotspot detection methods. In the next phase of the project, we intend to tackle the challenging problem of exploring the entire DRC-clean design space. We are developing methods which identify sparsely populated areas of the design space, guide the synthetic pattern generation tools to target those areas and, thereby, continuously increase coverage.

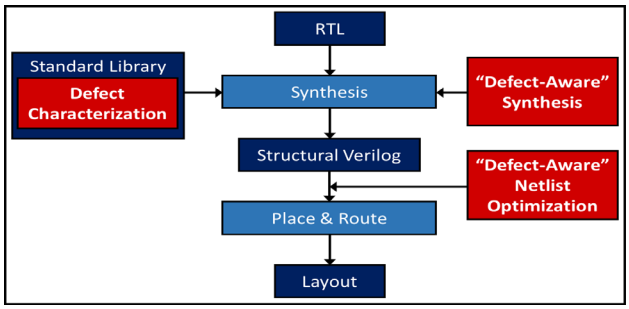

Figure 1. ML-Based Netlist Optimization for Delay Defects.

ML-based netlist optimization: Methods developed in this project are intended to identify vulnerable gates in the netlists and locally transform them to improve the defect tolerance of the entire netlist. To generate defect tolerant netlists, the synthesis tool must be supplied with models which characterize the defect responses of the cell library and a method to quantify the delay defect tolerance of a netlist. To this end, we characterized a 65-nm cell library, containing 60 cells, for its delay timings by injecting delay defects modelled as parasitic resistances/capacitances and performing SPICE simulations. The delay responses of these library cells were modelled into probability distributions and used to evaluate the netlist cell delays. To quantify delay defect tolerance, we queried the PrimeTime database for path delay information of netlist gates and the worst-case slack, compared it with the delay distributions obtained from library characterization and, therefore, identified the vulnerable cells in the netlist. Going forward, we plan to improve susceptible gate identification by introducing functional parameters into delay distribution information.

Keywords: Layout analysis, Coverage estimation, Benchmarks, Netlist optimization, Defect tolerance

INDUSTRY INTERACTIONS

Intel, Mentor

MAJOR PAPERS/PATENTS

[1] S. S. Thiagarajan, S. Natarajan, and Y. Makris, "Defect Tolerance Estimation and Netlist Optimization for Digital Designs," SRC TECHCON, 2020 (Under review).

[2] G. R. Reddy, K. Madkour, and Y. Makris, "Machine Learning Based Hotspot Detection: Fallacies, Pitfalls, and Marching orders," ICCAD, 2019.

TASK 2810.027, MEASUREMENT AND MODELING OF STRESS/STRAIN ON ANALOG TRANSISTOR AND CIRCUIT PARAMETERS

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SIGNIFICANCE AND OBJECTIVES

Packaging of electronic devices introduces compressive bixial stress and variable vertical stress due to silica particles in the epoxy. We show that due to non-linear nature of the intrinsic carrier concentration, compressive bizial stress (common type in most commercial packages) is disadvantgeous to bipolar device variability. Significantly improved matching could be obtained if transistors were packaged with tensile stress.

TECHNICAL APPROACH

BJT matching due to packaging stress is modeled using device simulation. The parameter shifts of BJT analog transistors will be measured using a 4-point bending flexure wafer bending jig. Measurents and modeling will be compared.

SUMMARY OF RESULTS

The goal is to develop a detailed understanding of packaging stress that results a voltage offset in a typical differential amplifier circuit (see Fig. 1).

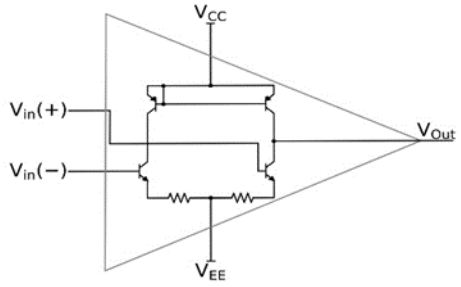


Figure 1. Example matching circuit.

The collector current change due to stress can be approximated by a summation due to the change in intrinsic carrier concentration and mobility:

$$I_s = \frac{k_B T}{q}\frac{A}{W}\sigma^{Minority} = \frac{k_B T}{q}\frac{A}{W} * \frac{q}{N_{Majority}} n_i^2 \mu \quad (1)$$

$$\frac{\Delta I_c}{I_c} = \frac{\Delta I_s}{I_s} = \frac{\Delta(n_i^2\mu)}{n_i^2\mu} \approx \frac{\Delta\mu}{\mu} + \frac{\Delta n_i^2}{n_i^2} \quad (2)$$

Device simulations are used to calculate change in collector current vs. biaxial stress and are shown below. Individual changes due to mobility and intrinsic carrier concentration are also shown. The data shows BJT collector current shifts more under compressive stress since the n_i and μ changes are additive. Next the sensitivity to bipolar collector current to vertical stress is calculated (typical stress caused by random silica particles in the epoxy).

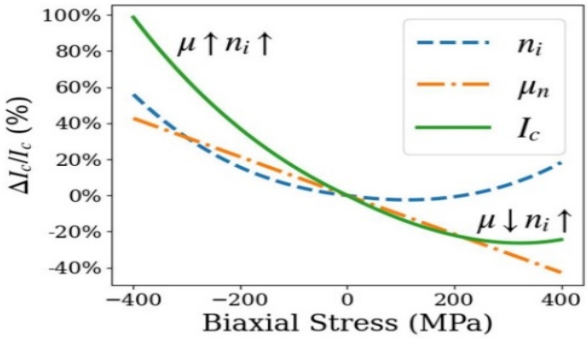


Figure 2. Change in collector current vs package stress.

Sensitivity is calculated by taking the slope of collector current change between -20PA and 20MPA. Different global package or process induced stress is considered (x-axis). Two points of insensitivity to vertical packaging stress are shown depending on the built in global stress: one for uniaxial stress and one for biaxial stress (x-axis).

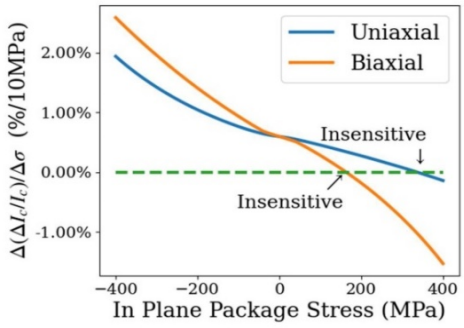
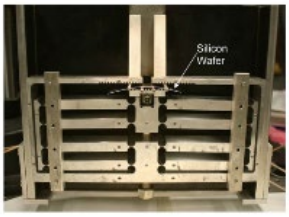
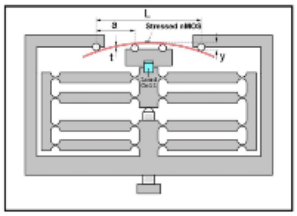


Figure 3. Sensitive of collector current vs stress.

Wafer bending experiments are next planned on commercially available BJTs to validate these results (setup shown below).





Keywords: strained Silicon, BJT matching, packaging stress

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] "Negative Impace of Compressie Biaxial Stress on High Percision Biploar Devices," submitted to EDL May 2020.

TASK 2810.038, EXTREME TEMPERATURE DIGITAL, ANALOG, AND MIXED-SIGNAL CIRCUITS (ET-DAMS)

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SIGNIFICANCE AND OBJECTIVES

Characterizing device and circuit performance is a key requirement for building reliable systems, especially those exposed to harsh operating temperatures. In year 1 of this project, we have designed a ring oscillator array test structure with on-chip heaters to collect massive frequency data at extreme operating temperatures.

TECHNICAL APPROACH

A test chip for characterizing the circuit performance at extreme temperatures was taped out in a 65-nm GP process. The chip consists of a 24×20=480 ring oscillator array with different threshold voltages, interconnect lengths, and interconnect layers. This allows for a statistically significant characterization under different voltage and temperature conditions. In addition, on-chip heaters using M7 metal layer were included to efficiently control the die temperature, from cryogenic to extremely high temperatures. Utilizing the on-chip heaters and a liquid nitrogen based test setup, we can cover a temperature range from 77K to 400K.

SUMMARY OF RESULTS

Fig. 1 shows the circuit diagram of the ring oscillator based test structure. Row select and column select signals are scanned in to read out the frequency of the selected ring oscillator. For a comprehensive analysis, we have implemented different types of ring oscillator circuits including different threshold voltages (LVT, SVT, HVT), different interconnect layers (M2, M6), and different interconnect lengths (0μm, 100 μm, 200 μm, 300 μm). The array based test structure can be scaled up to any size depending on the amount of data needed for necessary statistical confidence.

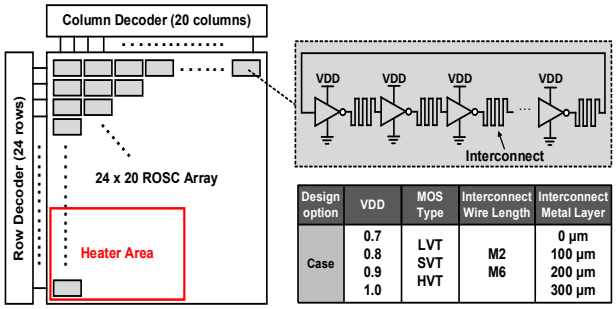

Figure 1. Ring oscillator array for circuit characterization at extreme temperatures.

For fast and accurate die temperature control, we have implemented three snake shaped heaters above the ring oscillator circuits on M7 metal layer. The layout of the heater is shown in Fig. 2 (upper). Temperature coefficient of resistance measured from the three different heaters show excellent linearity as shown in Fig. 2 (lower).

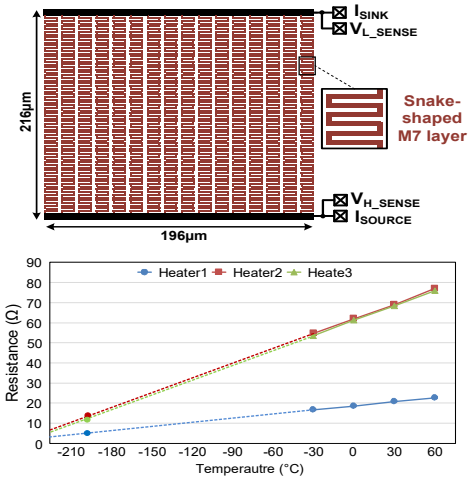

Figure 2. (Upper) On-chip heater for controlling die temperature. (Lower) Temperature coefficient of resistance measurement of on-chip heater.

Fig. 3 shows some early measurement results where the average ring oscillator frequency is plotted versus the die temperature for different interconnect lengths. A slight discrepancy between the on-chip heater results and the temperature chamber results, suggesting a temperature difference between the two method. We plan to investigate this issue through extensive measurements and data analysis.

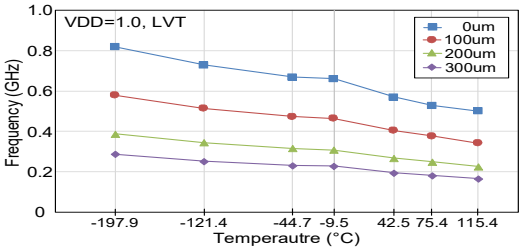

Figure 3. Early measurement results showing ring oscillator frequency at different temperatures, from -198C to 115C.

Keywords: extreme temperature electronics, ring oscillator, on-chip heater, cryogenic operation, temperature coefficient of resistance

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

TASK 2810.041, ESD PROTECTION FOR IO OPERATING AT 56 GB/S AND BEYOND

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SIGNIFICANCE AND OBJECTIVES

The project objective is to develop a co-design methodology for ESD-protected front-end circuits in receivers that employ PAM4 signaling. This will enable a designer to achieve adequate component-level ESD protection without increasing the required equalization.

TECHNICAL APPROACH

A four-pronged technical approach has been developed. First, ESD hazards arising from a variety of bandwidth extension technique are identified. The second step is to identify the V_{MAX} for each circuit topology under consideration, where V_{MAX} is the maximum tolerable voltage at the IO pin under ESD conditions. Generally, the designer has multiple receiver topologies to choose between. Third, the available protection devices are characterized (I_{fail}/Capacitance (mA/fF), V_{fail}, R_{on}*Capacitance). Finally, the performance and reliability of each candidate circuit are optimized through co-design. Much of the work is carried out using analysis and circuit simulation, but test chip fabrication and measurement will be used for proof of concept.

SUMMARY OF RESULTS

In the open literature, there are no prior ESD works that specifically focus on PAM4 systems, and thus the research topic has high novelty. The usual practice for ESD design is to work with a capacitance budget. Fig. 1, taken from JEDEC publication 157, *Recommended ESD-CDM Target Levels*, was derived assuming that a 10 Gb/s SerDes has an ESD-capacitance budget that is fixed at 200 fF; the protection levels listed in the figure are for 45-nm CMOS. Moving to a more advanced node without a change in the ESD design methodology will require either (1) an increase in the capacitance budget, or (2) a lowered specification for the ESD protection level. The first option is not feasible if the data rate is increased also.

Although the goal of this project is to change the ESD design methodology and introduce circuits that are, by construction, more resilient to ESD and therefore require reduced protection, the initial work on this project was a careful study of "ESD capacitance budgets." That work demonstrates that expressing the capacitance budget as a single number is not appropriate. For PAM4 systems in particular, one must perform an eye diagram analysis to determine when the ESD protection will unacceptably compromise the circuit performance. The eye opening is affected by the channel dispersion, the linearity of the ESD capacitance, and the presence of inductive elements in the package or on-chip. Case studies make apparent that defining a capacitance budget as a function only of the data-rate and the technology node is an overly simplistic approach that may lead one to unnecessarily limit a component's ESD reliability or, conversely, force the designer to unnecessarily increase the chip power or accept a reduced error rate.

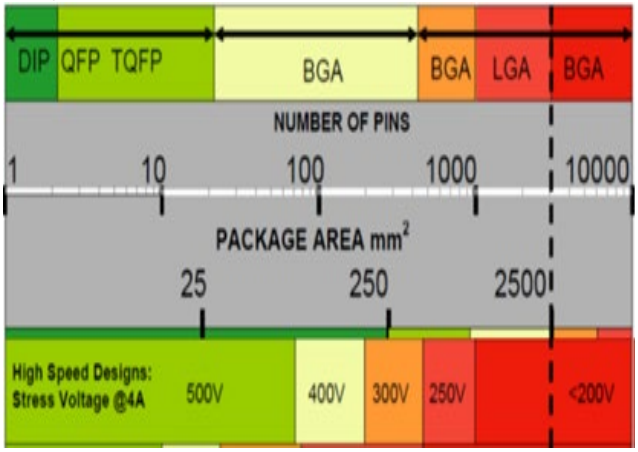

Figure 1. Industry Council's ESD roadmap (*JEP-157*) shows that increasing package sizes and pin counts will reduce the CDM-ESD protection level. The analysis was carried out for a 10 Gb/s data-rate, 45-nm CMOS, and SCR-based ESD protection with C_{ESD} = 200 fF. The initial work on this task suggests that the concept of a fixed ESD capacitance budget is not suitable for high-speed link design.

Keywords: Charged device model ESD, PAM4, SerDes, Receiver circuits

INDUSTRY INTERACTIONS

Intel, NXP, Texas Instruments

MAJOR PAPERS/PATENTS

TASK 2810.046, GENERATING CURRENT CONSTRAINTS FOR ELECTROMIGRATION SAFETY

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SIGNIFICANCE AND OBJECTIVES

We focus on electromigration (EM) failures of on-chip metal lines, and are developing tools to guarantee chip robustness in the face of EM degradation. Our goal is to provide techniques by which one can ensure EM reliability-by-design. The key advantage is improved accuracy and reduced conservatism.

TECHNICAL APPROACH

It is difficult to achieve EM sign-off on modern chip designs, due to the limitations of traditional empirical models that are built into existing tools. Modern physical EM models allow one to overcome these limitation, but are expensive to use, especially when doing EM simulation on large chip power grids. Instead of simulation, we will develop an "inverse approach": generate design-aware constraints on the circuit currents which, if guaranteed during chip design, would ensure EM safety for the desired lifetime. Since these constraints correspond to the specific design, this has the potential to improve accuracy and reduce pessimism.

SUMMARY OF RESULTS

Korhonen had provided in 1993 a physical model for EM that describes the evolution over time of the mechanical stress (built-up internal pressure) in a metal line, which is the cause of EM failures. We have built on this in our previous work, leading to a formulation of a linear (LTI) system for the stress vector as a function of line currents.

$$\dot{\sigma}(t) = A\sigma(t) + Bu(t)$$

The system matrix *A* has negative diagonal entries and is otherwise non-negative. It has zero row sums, so it is singular; it's also diagonally dominant and irreducible. We also reduced the matrix by one row/column using mass conservation, and the reduced matrix was found to be invertible in practice. This year, we were able to establish two useful theoretical results: 1) the original matrix is the negative of an M-matrix; this turns out to be useful for the next result, and 2) the reduced matrix is non-singular in general, which is a key result. Unfortunately, the reduced matrix is no longer an M-matrix (nor its negative) which is a complication, but not insurmountable, we think.

On another front, we have been looking at the steady-state stress at the nodes, which may be useful as a proxy for their dynamic (transient) stress; every node moves towards its steady-state stress (SSS) over time. There is some existing work on this, which we have built upon. We were able to establish two theoretical results. First, for every node in an interconnect tree, the deviation of its SSS from the tree-wide weighted-average stress, which we have shown is at all times equal to the initial stress in the tree, is proportional to the deviation of its voltage from the tree-wide weighted-average voltage. This is a very cheap algebraic way to immediately find the steady-state stresses from the voltages. It will be useful for analysis as well. Second, there is a straightforward linear matrix relationship between the vector of steady-state stresses and the vector of tree loading currents: $G\sigma \propto I$, which employs the familiar conductance matrix of the tree. As is, this system is not uniquely solvable because *G* is singlar. However, after enforcing a mass-conservation constraint, it becomes non-singular and the system uniquely solvable. This will be very useful for the inverse approach.

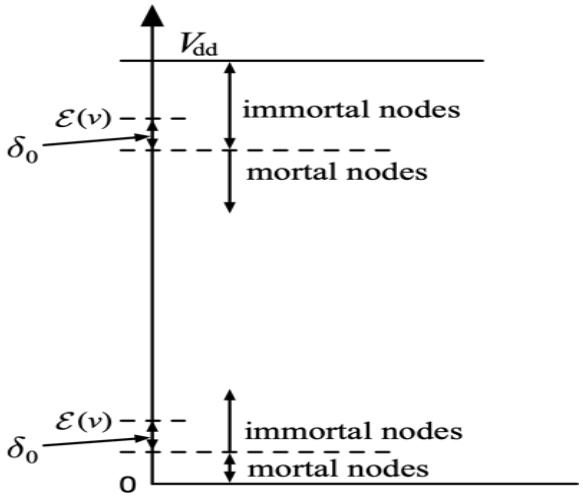

Figure 1. The steady-state voltages in the power/ground network identify whole groups of nodes as immortal.

Future work will follow the research plan in the original proposal. First, we will develop a "baby" inverse approach, based on the SSS. We will then develop the full theory for the inverse approach using dynamic stress. An initial implementation will then be developed, under DC inputs. This will then be extended to the full chip and will allow for multiple nucleations.

Keywords: integrated circuits, electromigration, stress, reliability, current constraints

INDUSTRY INTERACTIONS

Mentor,

MAJOR PAPERS/PATENTS

TASK 2810.047, ARCHITECTURE AND DFT METHODS FOR IMPROVING LIFE TIME RELIABILITY AND FUNCTIONAL SAFETY OF ELECTRONIC CIRCUITS AND SYSTEMS OUT OF APPLICATION CONTEXT

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SIGNIFICANCE AND OBJECTIVES

Increasingly more ICs are deployed in mission-critical applications to improve performance, reduce accidents, and save lives. Stringent requirements on lifetime reliability and functional safety (LRFS) are imposed but methodologies are significantly lagging for analog circuits. This project develops cost-effective DfT methods for greatly improving LRFS for analog and mixed-signal circuit.

TECHNICAL APPROACH

We will develop a DfT architecture and multilevel of monitoring and healing DfT solutions for ensuring lifetime reliability and functional safety. Digital DfT is assumed available to check our circuits. At power-on, we will use digital-like controls and detectors to verify all analog connectivity and topological correctness, which ensures functionality of basic analog components. With intrinsic process matching, we then perform accurate AMS BIST and calibration. After that, various health and ageing monitors will go online. A current sampling strategy will enable simultaneous measurements of many health and safety conditions, and will trigger recalibration and/or safety actions as necessary.

SUMMARY OF RESULTS

We have developed digital-like DfT tests for checking connectivity and functionality of a bandgap reference, a Widlar current reference, and a most widely used folded cascode + common source operational amplifier. We have also developed a digital-like strategy for checking all the components inside a SAR ADC with capacitor DAC. We have also developed preliminary online detectors that detect momentary excessive transients in a differential node pair or an excessive common mode glitch. We have also started developing an alternative solution to the analog test bus (ATB), that we call concurrent sampling, that will relax many of the pains associated with ATB, and that enable simultaneous measurement of many nodes under monitoring.

The progress on the connectivity and functionality check for operational amplifiers has been rich enough that a paper has been submitted to the 2020 International Test Conference. The amplifier with digital injection and digital detector circuits is shown in Fig. 1. The Injector is digitally activated to introduce a suitable amount of offset voltage. Digital inverters are used to monitor the op amp output, and two so-called window inverters are used to monitor the cascode transistor biasing. With these simple digital-like circuits, all connectivity faults except 3 are correctly detected. The three un-detected faults do not cause an electrical topology change and the op amp is still functional, equaling 100% functionality coverage.

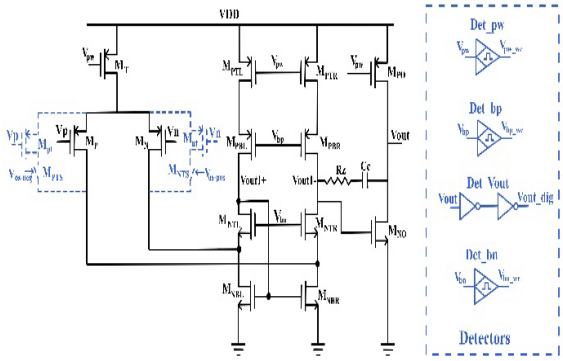

Figure 1. Operational Amplifier with Injection (Control) and Detector (Monitor). The injection circuit digitally activated, and the detector circuits are made of digital-like circuits and generate digital outputs.

Fault	M_T	M_P	M_N	M_{PTL}	M_{PTR}	M_{PBL}	M_{PBR}	M_{NTL}	M_{NTR}	M_{NBL}	M_{NBR}	M_{PO}	M_{NO}	Cover
D Open	D	D	D	D	D	D	D	D	D	D	D	U	D	92%
S Open	D	D	D	D	D	D	D	D	D	D	D	D	D	100%
G Open	D	D	D	D	D	D	D	D	D	D	D	D	D	100%
GD short	U	D	D	D*	D	D	D	D	D	D	D	D	D	92%
GS short	D	D	D	D	D	D	D	D	D	D	D	D	D	100%
DS short	U	D	D	D	D	D	D	D	D	D	D	D	D	92%
all														96%

Table 1. Fault coverage: operational amplifier (without compensation network).

Keywords: lifetime reliability and functional safety, power-on digital-like test for analog, built-in self-test and calibration for AMS, online health/ageing monitors, online concurrent sampling of many nodes

INDUSTRY INTERACTIONS

Texas Instruments, NXP, Intel

MAJOR PAPERS/PATENTS

[1] Marampally Saikiran, et al., "Robust DfT Techniques for…," in IEEE ITC, 2020 (Submitted).

TASK 2810.048, CHARACTERIZATION AND MITIGATION OF ELECTROMIGRATION EFFECTS IN ADVANCED TECHNOLOGY NODES

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SIGNIFICANCE AND OBJECTIVES

Electromigration is the primary back end of line reliability concern that is expected to worsen in future technologies due to higher current densities and self-heating effects. The goal of this work is to develop novel test structures and characterization methods for understanding EM effects in power grids and interconnect circuits.

TECHNICAL APPROACH

In year 1 of this project, we have developed a realistic power grid test structure where each individual standard cell is replaced with an equivalent gate poly resistor. These quasi load cells can withstand the high stress temperature (e.g. >300C) required for accelerated testing. The proposed gate replacement technique allows us to use any digital block for evaluating power grid electromigration effects.

SUMMARY OF RESULTS

Fig. 1 shows the conceptual diagram of the proposed power grid test structure. A realistic power grid layout with hundreds of voltage tapping points is used for EM characterization. Stress current or stress voltage is applied across the V_{DD} and GND terminals of the power grid. To raise the temperature of the device under stress without damaging the control circuitry and test board, we employ local on-chip heaters. A wide analog multiplexer implemented using IO devices is used to read out the various local voltages of the power grid. The scan chain and analog multiplexer are placed 100's of micrometers away from the power grid to protect them from high temperature stress.

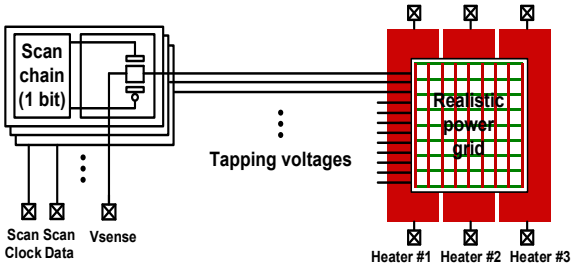


Figure 1. Conceptual diagram of a test structure for characterizing electromigration effects in power grids.

Fig. 2 describes the proposed gate replacement technique where large standard cells or a group of small standard cells are replaced with equivalent gate poly resistors. Unsolicited gates are used to match the load current. Small gates such as 1x inverter were simply ignored since the equivalent load resistance is too large to implement using poly resistors. The dimensions of the power grid is 124μm x 115μm. A script was written to automatically replace the cells with our custom designed quasi-load cells. Different load condition can be realized by changing the percentage of the cell that are being replaced by the script. This flexibility allows us to characterize EM for applications with different power consumption. Fig. 3 shows the full chip layout and a close-up view of the power grid test structure. We are currently preparing for the chip testing. In addition, we have been testing a circuit specifically designed to understand the impact of EM on signal line delay.

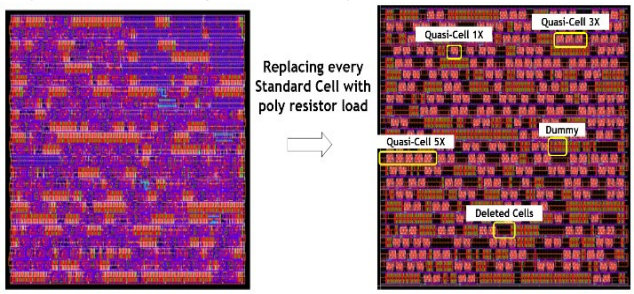


Figure 2. Gate replacement technique where each standard cell is replaced with a poly resistor load with the same equivalent resistance.

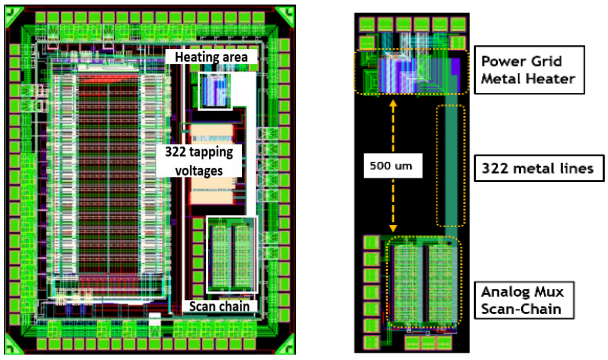


Figure 3. (left) Full chip layout. (right) Close up view of power grid test structure. The analog mux and scan-chain are located away from the power grid to prevent damage due to the high temperature stress.

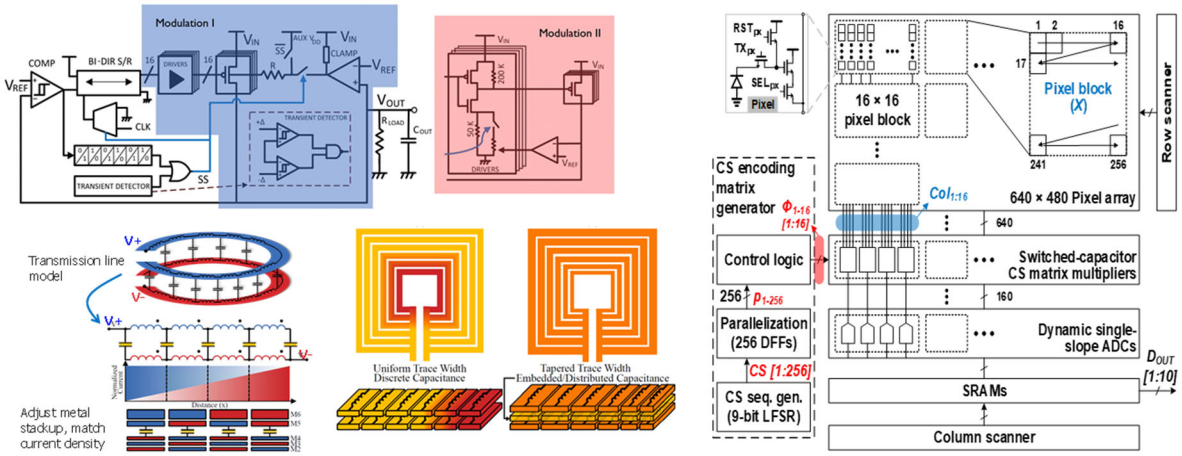
Keywords: electromigration, power grid, gate replacement technique, on-chip heater, voltage tapping

INDUSTRY INTERACTIONS

Intel, Mentor

MAJOR PAPERS/PATENTS

Energy Efficiency Thrust



Category	Accomplishment
Energy Efficiency (Systems)	Power IC's from a battery involves several power conversion stages, usually requiring a high voltage buck converter and LDOs. A direct battery-to-silicon prototype demonstrates that DC-DC conversion can be accomplished in CMOS using a multi-resonant coupled-inductor with 80% efficiency over a wide conversion rage (0.2 – 0.8). The output voltage is then regulated using a digital LDO with zero steady-state output voltage ripple. (2712.008, R. Harjani, U. Minnesota)
Energy Efficiency (Circuits)	Design of future ultra-low power processors operating near threshold (sub-mW operation SoCs) is hampered by maintaining sufficient margin in the supply to avoid errors. By creating an on-chip error detection and correction circuit, the margin can be significantly reduced and eliminated to allow true error-free operation near threshold. A 10-output single inductor multi-output DC-DC converter with integrated capacitors is demonstrated in 65-nm CMOS. (2717.012, M. Seok, Columbia)
Energy Efficiency (Circuits)	Ultra low-power compressive sensing techniques for IoT applications have the potential to greatly improve the energy efficiency of edge devices. A compressive sensing coding scheme for a CMOS imager uses a mixed-signal switched capacitor matrix multiplier. This is the first CMOS image sensor that achieves single-shot compressive sensing using Nyquist-rate ADCs, improving the state-of-art energy efficiency by >20x. (2717.023, N. Sun, UT Austin)
Energy Efficiency (Circuits)	A hybrid resonant switched capacitor converter with an integrated LC resonator is demonstrated for high-density power delivery. A designed and tested merged LC resonator with on-chip spiral magnetics results in a factor of two improvement in power density with higher efficiency relative to comparable pure switched-capacitor implementations. (2810.040, J. Stauth, Dartmouth)

TASK 2712.002, ON-LINE SELF-TESTING AND SELF-TUNING OF INTEGRATED VOLTAGE REGULATORS

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SIGNIFICANCE AND OBJECTIVES

The proposed research will develop low-complexity algorithms and low-overhead all-digital self-testing and self-tuning architecture for high-frequency IVRs. The proposal will focus on a digitally controlled fully integrated inductive VR (FIVR), digital low-dropout regulators (DLDO), and power delivery system with a FIVR and multiple distributed DLDOs.

TECHNICAL APPROACH

The challenge for testing/tuning of IVRs is the presence of high frequency closed-loop control. The proposed approach is based on the principle that in a system with an IVR and digital core(s), the testing/tuning should focus on system performance rather than the IVR in isolation. We propose to characterize the output voltage variation that ultimately determines the performance of the digital load. We consider large signal perturbations (load and reference steps) to excite the transient noise in the IVR's output, and tune the IVR's loop to minimize the noise. Finally, we explore co-tuning of IVR and processor.

SUMMARY OF RESULTS

A fully synthesized integrated inductive buck regulator with flexible precision variable frequency feedback loop implemented in 65-nm CMOS process using an automated design and GDSII generation flow is demonstrated. The design demonstrates 0.52V/µs output ramp and 200ns response time to 30mA/75ps load transient in a high precision mode with 120MHz switching frequency. The peak efficiency is 79.3% at 0.78V output and 43mA load current.

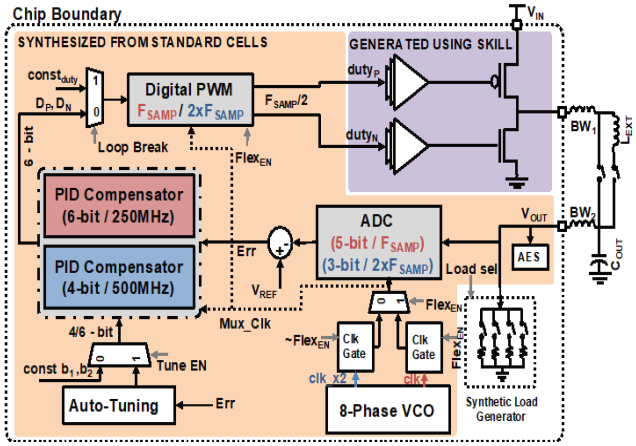
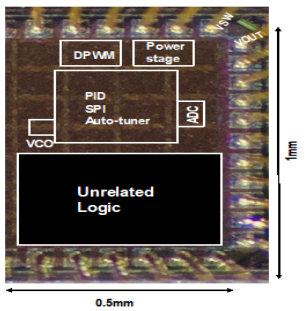


Figure 1. The architecture of full-synthesized architecture with on-line tuning.



Technology	65
Package	CLCC44
Control	Digital PWM Flexible Precision
Phase	1
V_{IN} (V)	0.9-1.2
V_{OUT} (V)	0.6-1.0
Maximum I_L (mA)	45
F_{SW}	80-120
F_{SAMP}	160-240 (High Precision) 320-480 (Low Precision)
L (nH)	62 (50+2xBW)
C (nF)	23 (20 + 1.5 mos + 1.5 mim)
Peak Efficiency (%)	79.3 @ (V_{OUT}=0.78V, I_L=43mA)
Synthesizable	Yes

Figure 2. The summary of the test-chip.

The degradation of the transient performance and power conversion efficiency of on-chip VRs due to NBTI have been investigated. The measurement show that NBTI induced shifts in the power stage resistance have much smaller effect on the IVR compared to DLDOs.

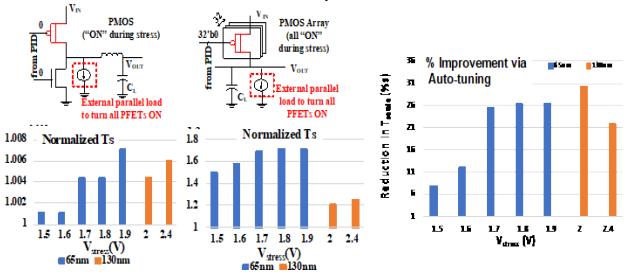


Figure 3. The measurement results showing impact of of aging on inductive VR and digital LDO.

Keywords: Integrated voltage regulator, self-testing,

INDUSTRY INTERACTIONS

Intel, NXP

MAJOR PAPERS/PATENTS

[1] A. Singh, et al., "A Digital Low-Dropout Regulator with Auto-Tuned PID Compensator and Dynamic Gain Control for Improved Transient Performance under Process Variations and Aging," IEEE TPEL, March 2020.

[2] V. Chekuri, et al., "Auto-tuning of Integrated Inductive Voltage Regulator using On-chip Delay Sensor to Tolerate Process and Passive Variations," IEEE TVLSI, Aug. 2019.

[3] V. Chekuri, et al., "A Fully Synthesized Integrated Buck Regulator with Auto-generated GDS-II in 65nm CMOS Process," IEEE CICC, March 2020.

[4] (Invited) V. Chekuri, et al., "Aging Challenges in On-chip Voltage Regulator Design," International Reliability Physics Symposium (IRPS), April 2020.

TASK 2712.006, ROBUST, EFFICIENT ALL-DIGITAL SIMO CONVERTERS FOR FUTURE SOC DOMAINS

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SIGNIFICANCE AND OBJECTIVES

As Integrated Voltage Regulated (IVR)-- enabled DVFS systems continue to be more aggressively adopted in SoC designs, their limited scalability poses a significant challenge. Single-Inductor Multiple Output converters offer a scalable solution, but face significant regulation challenges. The proposed effort seeks to provide (1) an all-digital voltage regulation system using a Single-inductor Multiple Output (SIMO) topology for digital SoC domains, and (2) a Unified Clock and Power (UnCaP) architecture[1] to enable robust regulation without prohibitive amounts of decoupling capacitance.

TECHNICAL APPROACH

Two central components that will determine the efficacy of the adopted technical approach are (1) understanding the impact of insertion delay on UniCaP performance; and (2) computationally enhancing SIMO control to aggressively reduce Vdd droop guardbands in multi-domain SoCs. We observed that SIMO converters offer poor load regulation, motivating the design of Unified Clock and Power (UniCaP) prototypes in 65-nm CMOS. To address this challenge, we propose two solutions: (1) SIMO control that allows for "droop balancing" across multiple domains and (2) computational control to devise a SIMO architecture that achieves rapid transient response, and whose transient response does not degrade linearly with the number of SIMO domains.

SUMMARY OF RESULTS

We leveraged the learning from our computational control LDO and buck test chips (Fig. 1) which were presented in 2019 (ISSCC) and 2020 (VLSI), into our proposed 4-domain integrated SIMO regulator. A successful outcome will yield the first SIMO demonstration of not only digital domains but those that are fully-integrated. Fig. 2(a) shows the proposed SIMO architecture, which has returned from fabrication and is currently in testing. Simulation waveforms of the "droop balancing" operation of the proposed system are shown in Fig. 2(b). A current step occuring on a single domain causes all domains to experience a voltage-droop in a shared fashion. Thus, cross-regulation is effectively embraced as not a phenomenon to be avoided, but one that is best engineered to achieve the best efficiency/droop in SIMO design.

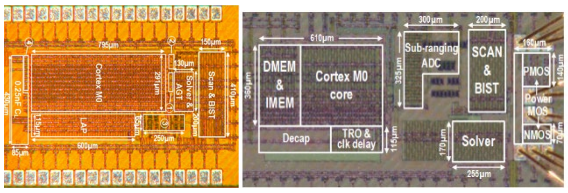

Figure 1. Test chips presented in 2019 and 2020 that demonstrate computational control, which has been applied into the proposed 4-phase SIMO regulator design.

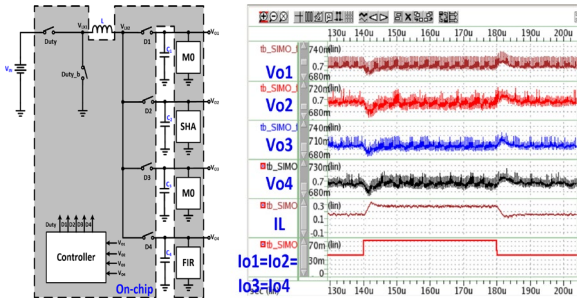

Figure 2. Proposed SIMO architecture (a) Block diagram of system implementation and (b) simulation waveforms of the proposed computational controller.

Meanwhile, a parallel test chip effort is also quantifying the impact of insertion delay on the ability of the UniCaP architecture to eliminate V_{dd} droop margins. In agreement with the Industry liaisons, it was decided that resonant drive was not going to be a subject that we would be able to pursue in the available timeframe and funding framework.

Keywords: SIMO, Unified Clock and Power, Voltage Regulation, Clock Stretching.

INDUSTRY INTERACTIONS

Intel, ARM, NXP

MAJOR PAPERS/PATENTS

[1] Sun, X et al. “A 0.6–1.1V Computationally Regulated Digital LDO with 2.79-cycle Mean Settling Time and Autonomous Runtime Gain Tracking in 65-nm CMOS" ISSCC 2019.

TASK 2712.007, HIGH-RESOLUTION LOW-VOLTAGE HYBRID ADCS FOR SENSOR INTERFACES

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SIGNIFICANCE AND OBJECTIVES

The goal of this research is to extend the state-of-the-art of high resolution sensor interface ADCs through research and development of a hybrid ADC architectures, that are also easy to drive.

TECHNICAL APPROACH

This new class of converters will facilitate and improve sensing and IoT applications. These needs are currently unmet since state-of-the-art low-power ADCs are difficult to drive (i.e. requiring filter and input buffer), and are limited in either resolution or power consumption. ADCs for sensors are often implemented as SAR or oversampling ADCs. SAR ADCs achieve excellent energy efficiency but are limited in resolution. Calibration adds complexity and may need to be adjusted with temperature and supply changes. Sigma-Delta ADCs and incremental converters can achieve higher resolution but are constrained by the requirements of the op-amps and switches.

SUMMARY OF RESULTS

High-resolution, sub-MHz bandwidth data converters are essential for audio and sensor applications and are conventionally implemented as Sigma-Delta (SD) converters. The dependence of SD ADCs on op-amps inherently results in difficulties for process scaling, power efficiency improvement, and area reduction. A promising alternative to SD ADCs is the emerging Noise-Shaping (NS) SAR ADC, which provides high resolution with high energy efficiency and compactness. For medium-high SNR applications, some NS-SAR ADCs already exhibit better performance than SD ADCs. However, currently lacking are NS-SARs for applications that require SNR >85 dB and hundreds of kHz of bandwidth. The SNR is limited because most recent NS-SAR ADCs are restricted to a low-order noise transfer function (NTF). Additionally, noise from the loop filter limits performance.

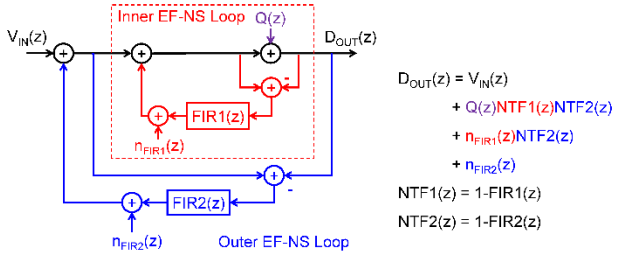

Figure 1. Cascaded-Noise-Shaping SAR architecture.

We propose a Cascaded-Noise-Shaping (CaNS) SAR architecture that cascades two 2nd-order error-feedback (EF) NS stages to provide a 4th-order NTF for high resolution, while consuming similar power and area to a 2nd-order NS-SAR. The zeros of the overall NTF are independently controlled by the two sub-NTFs. This makes the overall NTF less sensitive to the variation of coefficients.

Fabricated in 28-nm HPC+ CMOS, our prototype CaNS-SAR ADC occupies an active area of 0.02mm^2 and consumes 119.9µW power from a 1V supply at a 2MS/s sampling rate. A peak SNDR of 87.6dB is measured with a 10x over sampling ratio, resulting in a Schreier FoM of 176.8dB. Only 2dB change in SNR is observed between 5 devices, over a 0~70°C temperature range and for a ±10% amplifier supply variation, showing good PVT robustness.

This work enables the first 4th-order NTF and excellent SNR performance in single-channel NS-SAR ADCs, while preserving the energy efficiency of SAR architecture. The proposed ADC is a more compact and energy efficient alternative to SD ADCs for audio and sensing applications that require high SNDR in sub-MHz bandwidth.

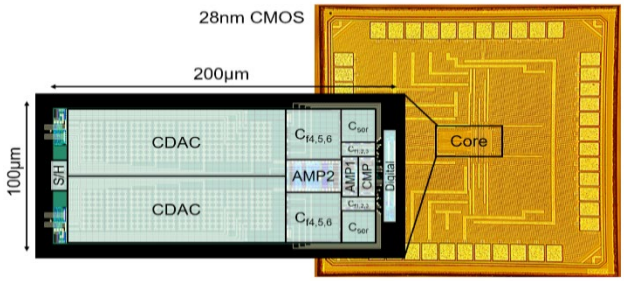

Figure 2. Protoype CaNS SAR ADC in 40nm CMOS.

Keywords: Sigma Delta, ADC, sensor, SAR, IoT

INDUSTRY INTERACTIONS

Texas Instruments, Intel, ARM, NXP

MAJOR PAPERS/PATENTS

[1] L. Jie, B. Zheng, H-W. Chen, R. Wang, M. P. Flynn, "A 4th-Order Cascaded-Noise-Shaping SAR ADC with 88dB SNDR Over 100 kHz Bandwidth," 2020 International Solid-State Circuits Conference, (ISSCC), February 2020.

[2] L. Jie, et al. "A Calibration-Free Time-Interleaved Fourth-Order Noise-Shaping SAR ADC," JSSC, vol.54, no. 12, pp 3386-3395, Dec. 2019.

[3] L. Jie, et al., "A 4th-Order Cascaded-Noise-Shaping SAR ADC with 88dB SNDR Over 100kHz Bandwidth," ISSCC, February, 2020, San Francisco.

TASK 2712.008, DIRECT-BATTERY-TO-SILICON POWER TRANSFER IN ADVANCED NANOMETER CMOS

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SIGNIFICANCE AND OBJECTIVES

The aim of the task is to facilitate direct-battery-to-silicon high-tension-power delivery in advanced CMOS processes to bring down delivery losses and area footprint. The key objective is to develop circuit techniques to handle the breakdown voltages and to implement fine-grain feedforward control for SOCs while making these solutions portable across technology and types of SOCs.

TECHNICAL APPROACH

Deep-submicron technologies have ~1V as the core MOS rated voltages and at-max 2.5V for thick-oxide I/O MOS devices. In order to handle 4+V battery voltage careful stacking/design of devices is required. During the course of the project, we focus our work on both capacitive and hybrid converters and lower dropout regulators.

SUMMARY OF RESULTS

1.Fully tunable software defined DC-DC converter

A software defined (SD) capacitive converter with five conversion ratios (K) and having both frequency (F) and capacitance (C) based output voltage modulation was presented. The efficiency profile of this SD-capacitive converter is shownin Fig. 1. Under K, F and C tuning, the system can support the largest load range while maintaining high efficiency.

2.Smart-Offset analog LDO

An analog solution for ultra low voltage LDOs using smart offset was proposed in [3]. Our SO-LDO uses smart negative offset topology and can sustain a load variation of 10-100mA with achieving a peak current efficiency of 99.1% at 100mA load.

3.Digital Low Dropout Regulators with Zero Steady-State Output Ripple

By exploiting body-bias and modulating the driver gate voltage, two zero-ripple D-LDO method were designed in [4]. Both techniques can handle a load range of 0.1-20mA (200X) with 99.4% current efficiency and zero output voltage ripple.

4.Multi-mode hybrid DC-DC converter

To accommondate a wide range DC-DC conversion ratio (K) (between 1 to 13), we implemented a direct battery to silicon multi-mode hybrid switching regulator system in 65-nm CMOS [2]. The proposed DC-DC converter has three modes of operations, buck (for K=5-13), resonant (K=1 & 2) and soft switching (for K=3 & 4). The peak efficiency 86.6% and a load range of 0.5-200mA at a peak power density of 0.3W/mm^2 are reported in [2].

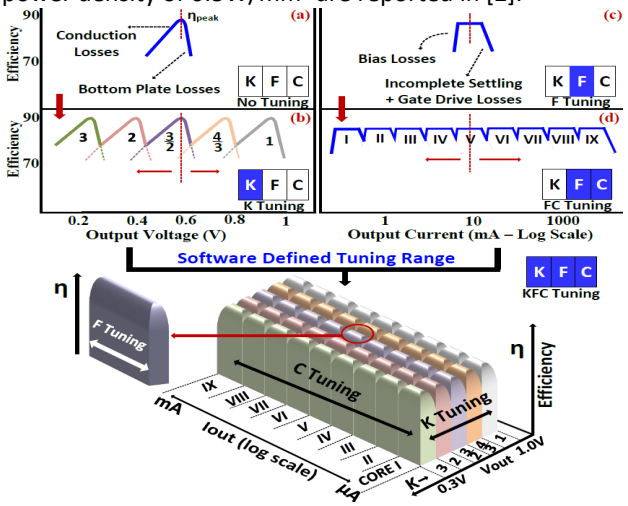

Figure 1. Efficiency profile of a capacitive converter; Bottom 3D-plot shows KFC tuning for the proposed SDCC.

5.Multi-mode hybrid DC-DC converter

A new hybrid DC-DC converter with multiple resonant operation points was designed to further increase the power efficiency around the whole range of VCR. The converter provides a 93% peak and 79% minimum power efficiency over 0.2-0.9 VCR range with 190mW/mm2 output power density.

Keywords: power mgmt, hybrid DC-DC, zero-ripple LDO

INDUSTRY INTERACTIONS

NXP, Intel

MAJOR PAPERS/PATENTS

[1] Chaubey, S. & Harjani, R., “Fully Tunable Software Defined DC-DC Converter with 3000X Output Current & 4X Output Voltage Range 2010", IEEE CICC 2017, Austin.

[2] Chaubey, S. & Harjani, R., “A Multi-Mode DC-DC Converter for Direct Battery-to-Silicon High Tension Power Delivery in 65nm CMOS”, IEEE CICC 2019, Austin.

[3] Chaubey, S & Harjani, R., " A Smart-Offset Analog LDO with 0.3V Minimum Input Voltage and 99.1% Current Efficiency", IEEE A-SSCC, Seoul, South Korea, Nov 2017.

[4] Chaubey, S & Harjani, R., “Design Techniques for Zero Steady-State Output Ripple in Digital Low Dropout Regulators”, IEEE MWSCAS, Dallas, August 2019.

[5] Harjani, et al., “Ultra High Density Integrated Composite Capacitor”, US patent # 9,812,457, Issued Nov 7, 2017 [Patent].

TASK 2712.009, LOW POWER AREA EFFICIENT FLEXIBLE-RATE ENERGY PROPORTIONAL SERIAL LINK TRANSCEIVERS

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SIGNIFICANCE AND OBJECTIVES

The objective of this research task is to develop techniques to achieve energy proportional operation in high speed links operating with high-loss channels. We proposed a baud-rate receiver architectures that can turn on/off rapidly while compensating a large channel loss and verified them using experimental results obtained from a prototype.

TECHNICAL APPROACH

The proposed half-rate receiver consists of a CTLE, 3-tap DFE, baud-rate CDR, and circuitry to support rapid on/off operation. The proposed phase detector (PD) uses a new timing function, f(t)=h0-h1, that enables baud-rate CDR operation. Compared to Mueller-Muller PD, the proposed PD requires only half the number of samplers and performs better when channel loss is high. The potential error propagation was avoided by adopting a duobinary encoding/decoding scheme. Phase sweeping is performed implicitly by digitally adding a frequency offset to the DCO and the CDR can find the optimal phase within 100UI.

SUMMARY OF RESULTS

The proposed receiver was fabricated in a 65-nm CMOS technology; the design's die photo is shown in Fig. 1. It occupies an active area of 0.45 mm^2 and achieves error-free operation (BER < 10^{-12}) when recovering 12Gb/s PRBS31 data. The receiver is characterized using a channel that has a measured insertion loss of 20dB at Nyquist frequency. The measured bathtub plots with and without DFE are shown in Fig. 2. DFE improves clock phase margin to about 0.18UI at a BER of < 10^{-11}. A phase noise plot of the 6-GHz recovered clock is shown in Fig. 2. Integrated jitter (10kHz to 100MHz) is 498 fsrms. Turn on behavior of the receiver is illustrated in Fig. 2. Error-free operation with PRBS 7 pattern is achieved after 18ns as indicated by the error signal going low. Because this time includes latency introduced by the de-serializer and the internal BER checker, the actual turn-on time of the receiver is smaller than 18ns. The error-free rapid-on behavior is validated with 12000 data pattern and 500 on-off cycles, which translates to BER < 10^{-6}. Data length and the number of on-off cycles used in this test were limited by our measurement setup.

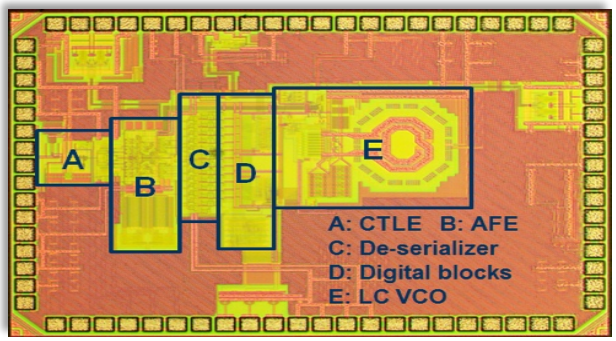

Figure 1. Proposed half-rate receiver architecture.

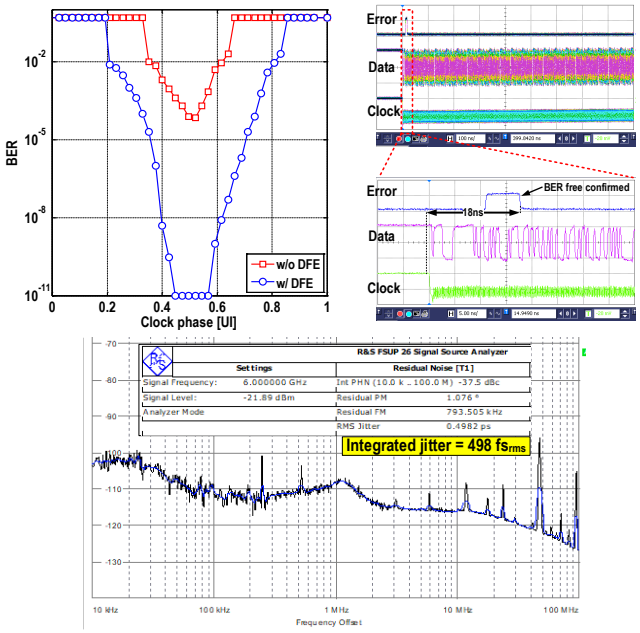

Figure 2. Measured turn-on behavior.

Keywords: CDR, Baud-rate, Rapid on/off, Burst-mode.

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] D. Kim et al., "A 12Gb/s 10ns turn-on time rapid on/off baud-rate DFE receiver in 65nm CMOS," Journal of Solid State Cirucits (to appear).

TASK 2712.012, EDAC AND DCDC-CONVERTER CO-DESIGN FOR ADDRESSING ROBUSTNESS CHALLENGES IN EMERGING ARCHITECTURES

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SIGNIFICANCE AND OBJECTIVES

The goal of this project is to develop techniques on EDAC and DCDC converter co-design for the post-Moore's law era when aggressive architectures and circuits must be explored to continue the performance and energy-efficiency scaling while ensuring robustness and reliability.

TECHNICAL APPROACH

We will devise the following techniques: (i) direct error regulation to make DVS energy-efficient and fully-digital while miniaturizing capacitor sizes in the integrated switched-capacitor converter; (ii) EDAC+Converter for non von-Neumann and parallel architecture, such as error correction scheme for super-Vt circuits performing no instruction replay, and techniques for in and around embedded memory; (iii) EDAC+DVS for clock domain crossing to simplify clock distribution and generation.

SUMMARY OF RESULTS

Last year, we have worked on mainly two projects [1,2]. In the first project, we have worked on a EDAC (Error Detection and Correction) based clock domain crossing (CDC) technique. There is a large body of the work on CDC and metastability, but little works have been done to develop the in-situ metastability condition detection and correction (MEDAC) for an NTV (Near Threshold Voltage) SoC where the frequencies, phases, and voltages are different among V/F domains.

In NoC (Network on Chip) design, the synchronizer has been an effective technique for CDC, but it neither guarantees the correctness of data nor provides long-term mitigation. We replace the conventional synchronizer with the proposed MEDAC unit. As shown in Fig. 1 top, it consists of a metastability detector and a corrector. The detector has the main and a shadow synchronizer. The main synchronizer receives Rx_clkd, which is the delayed version of the clock of the shadow synchronizer clock Rx_clk by the interval window (WI). If a signal arrives near either of the RX or TX clock edges, the output of the first flip-flop of the synchronizers may enter the metastability state. The MEDAC unit compares the output of the two synchronizers and flags this as the metastability condition.

Also, the proposed MEDAC takes a preventive action to reduce the probability of future metastability. Specifically, we have devised a scheme to optimally and dynamically adjust the phase that maximally extends the time to the next metastability. We designed the metastability corrector in the MEDAC unit. The mean-time-between-metastability (MTBM) timer counts the number of cycles between two adjacent metastability detections and estimates if the current ΔPnorm incurs too much metastability. If it does, the phase shifter modulates the three delay lines to change ΔPnorm to a better value.

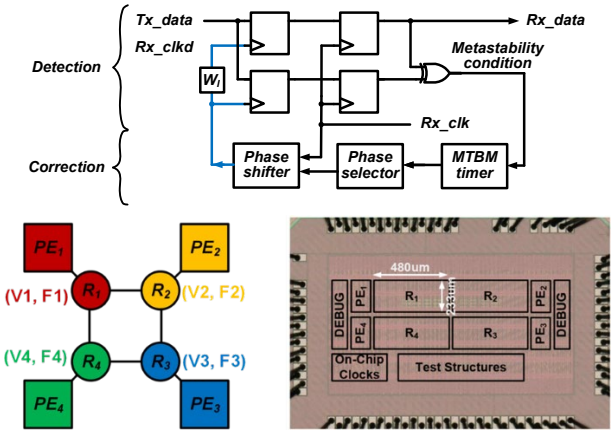

Figure 1. Proposed MEDAC circuits (top), the 2x2 NoC test chip architecture featuring the MEDAC technique (bottom left) and the die photo of the test chip in 65-nm CMOS (bottom right).

In the second project, we have designed and prototyped a single-inductor-multiple-output (SIMO) buck converter for a sub-milliwatt digital system-on-chip (SoC). The converter achieves better area efficiency and power conversion efficiency (PCE) over using multiple switched capacitor DC-DC converters and linear regulators. The proposed SIMO converter fully integrates all the output capacitors on a chip to minimize the off-chip component count.

Keywords: NTV, EDAC, clock domain crossing, metastability, SIMO DC-DC converter

INDUSTRY INTERACTIONS

Intel, Texas Instruments, IBM

MAJOR PAPERS/PATENTS

[1] Chuxiong Lin, et al., "A Near-Threshold-Voltage Network-on-Chip with a Metastability Error Detection and Correction Technique…," IEEE International Solid-State Circuits Conference (ISSCC), 2020.

[2] Dongkwun Kim, et al., "A 10-Output Single-Inductor-Multiple-Output DC-DC Buck Converter with Integrated Output Capacitors…," IEEE Asian Solid-State Circuits Conference (ASSCC), 2020, to be submitted.

`TASK 2712.016, 3D IC THERMAL MANAGEMENT BASED ON TSV PLACEMENT OPTIMIZATION AND NOVEL MATERIALS

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NADER BAGHERZADEH, UNIVERSITY OF CALIFORNIA, IRVINE

SIGNIFICANCE AND OBJECTIVES

3D integrated circuits (ICs) rely on through-silicon-vias (TSVs) for signal communications across stacked dies. The main objectives in this period were to investigate the trade-offs in thermal and electrical performance metrics of signal TSVs, to identify optimal TSV designs, and to evaluate novel TSV materials for future applications.

TECHNICAL APPROACH

A 3-D electromagnetic (EM) field solver and a heat transfer simulator were employed to model and analyze the electrical and thermal properties of TSVs with various configurations, dimensions, and materials. To find the optimal TSV design, a cost function was defined to consider the trade-offs in thermal and electrical performance. Materials with high thermal conductivities such as carbon nanotubes (CNTs) and Boron Arsenide (BAs) were evaluated for use in coaxial TSVs.

SUMMARY OF RESULTS

We modeled a 3D IC system that has 8 dies and each die is made of Si layer, BEOL, and bonding layer with 2 W power consumption. We assumed a 1% TSV insertion density ($A_{TSV\ unit\ cell}/A_{chip}$) for both signal-ground (S-G) and coaxial TSVs. Some of the simulation parameters including thermal conductivity (k) are listed below.

Table 1. Material properties and structure dimensions.

	k ($Wm^{-1}K^{-1}$)	Thickness (μm)
Si Die	100	40
Bond	0.15	10
BEOL	1.5	20
TSV	400	40

The EM simulations were performed using Ansys HFSS and the insertion loss (S_{21}) was used to evaluate the signal integrity. For S-G and coaxial TSVs, the TSV radius and height were fixed while the distance between signal and ground was varied. Coaxial TSVs provide better electrical performance compared to that of the S-G TSVs because the EM fields that carry its signal exist only between the inner conductor and ground shell, which mitigates the signal loss and coupling noise. However, coaxial TSVs are much difficult to manufacture. A cost function is defined as $Cost = aT_{normalized} + bS21_{normalized}$, where $T_{normalized} = \frac{T-T_{min}}{T_{max}-T_{min}}$ and $S_{normalized} = \frac{S21-S21_{max}}{S21_{min}-S21_{max}}$. The weight factors, a and b for temperature and signal integrity are assumed to be 1.

Figure 1 shows that for both TSV configurations. The normalized temperature increases while the normalized insertion loss decreases with the increase of signal and ground distance, which are caused by the reduced effective thermal conductivity and reduced coupling capacitance, respectively. An optimal TSV structure can be found that provides the best overall performance.

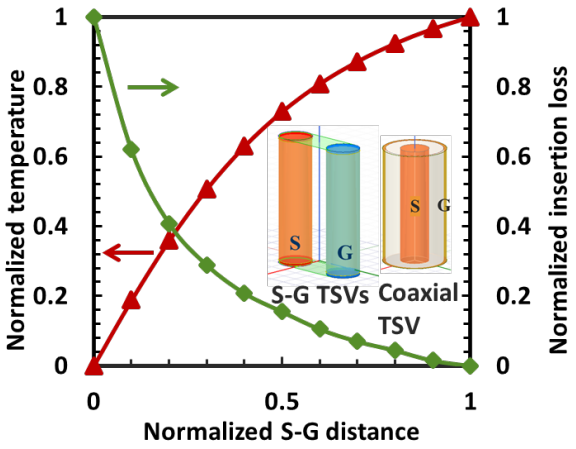

Figure 1. Temperature (left) and insertion loss (right) changes with respect to the distance between signal and ground TSVs.

While the peak temperature can be reduced by increasing the thermal conductivity, the insertion loss can be reduced by increasing the electrical conductivity or reducing the dielectric constant. If CNTs are used as signal TSVs, the peak temperature could reduce up to 24%. On the other hand, BAs are electrically insulating, and they can be used as thermal TSVs to reduce the peak temperature up to 25%. Furthermore, CNTs and BAs have similar coefficients of thermal expansion, compared to Si, which may minimize thermal stresses.

Keywords: 3D ICs, S-G TSVs, coaxial TSV, electro-thermal trade-off, optimal TSV design

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] Z. Ren et al., "Thermal TSV optimization and hierarchical floorplanning for 3D integrated circuits," IEEE Trans. Compon., Packag., Manuf. Technol., 10.4, 2020.
[2] Z. Ren et al., "Thermal analysis of 3D ICs with TSVs placement optimization," ASME InterPACK, 2019.

TASK 2712.018, TITLE TEST TECHNIQUES TO APPROACH SEVERAL DEFECT-PER-BILLION FOR POWER IC'S

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SIGNIFICANCE AND OBJECTIVES

This research designed, simulated and tested custom LDO and Buck Converter power ICs using additional bare-die test points to better anticipate part failures. The goal was to improve yield by culling power ICs with outlier subcircuit performance. Additional work characterized small-signal LDO control loop gain using IC external pins.

TECHNICAL APPROACH

Task researchers developed novel 65-mn CMOS LDOs and Buck Converter designs with internal IC test points for enhancing testing. Analyses and simulations of these designs were used to determine subcircuit performance inside the LDO and Buck Converter. Based on this work, a 65-nm CMOS LDO test IC and a Buck converter test IC were designed, fabricated and tested. The functional LDO Test IC was used to demostrate on-chip control loop gain and phase response measurements. Researchers also investigated methods to do control loop characterization quickly on ATE.

SUMMARY OF RESULTS

This year the project researchers 1) packaged a 65-nm CMOS Buck converter IC, made a custom test board for the converter and performed converter measurements, 2) developed a technique in collaboration with TI engineers to characterize LDO control-loop circuit elements from LDO measurements, and 3) developed test boards and performed small-signal control-loop measurements of an LDO test IC.

Also, researchers used measurements to identify outlier capacitors in the LDO control-loop from LDO IC pin measurements. This work was performed at TI Tucson, AZ.

The Buck converter IC testing strategy used extra probe points for DC and analog test on die. The researchers were guided by the SRC/TI program liaison engineers to develop a Buck converter test IC with an advanced Average Current Mode (ACM)-based control loop design. The researchers received 65-nm CMOS Buck converter ICs from Global Foundries in July 2019. These ICs were packaged and characterized.

Bench equipment measurements showed good Buck converter line regulation and overall performance. The Buck converter IC band-gap reference (BGR), the test MUXs, the control loop amplifiers and the regulation subcircuits performed well. The band-gap reference gave a supply independent reference voltage of 1.32 V, with the bias supply range of 2 V to 3.5 V. The Buck converter inner current control-loop and outer voltage control loop functioned as designed. The regulated output voltage was 1.65 V and output ripple was around ±10mV. The load current was regulated at 42 mA with a 40Ω internal load.

The task researchers developed methods for small-signal LDO control-loop characterization. These methods are important for determining LDO stability and reliability. The safety of automobile brake control systems can be compromised by unstable compensation in the LDO control-loop. Reseachers developed small-signal test boards for the LDO test IC that enabled switching out control loop elements (capacitors and resistors).

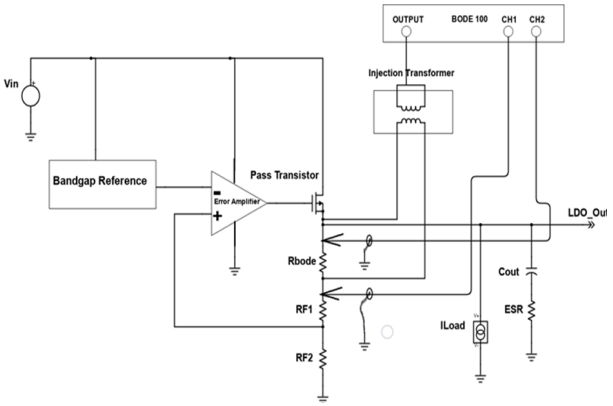

Figure 1. The LDO control loop measurement schematic.

Bode 100 analyzer probes were placed across R_{bode} to determine the control-loop small-signal performance. For PSRR measurement, a test signal was injected at V_{in} through an injection transformer. LDO control-loop cutoff frequency measurements showed the ability to determine outlier values of C_{out}, the critical compensation capacitor. Work is continuing to translate the servo-loop technique to a loadboard circuit for ATE-based testing.

Keywords: Test, Analog, Power, LDO, Buck Converter

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] A. Tulsiram, and W. Eisenstadt, "In Situ DC Loop Gain and Stability Measurement of LDOs using a Nulling Op-Amp Servo Loop," Fourth ART Workshop, Washington, D.C., USA, November 14-15, 2019.

TASK 2712.019, PRE-COMPUTED SECURITY PROTOCOLS FOR ENERGY HARVESTED IOT

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SIGNIFICANCE AND OBJECTIVES

We optimize the latency and energy-efficiency of Internet security protocols in energy-harvesting IoT. An energy-harvesting IoT device has a limited and leaky energy-storage capacity. The energy must be used as soon as possible after harvesting. With pre-computing techniques, cryptographic applications can instantly use the harvested energy. Pre-computed results are stored efficiently and reliably in non-volatile memory and are used to improve latency. We demonstrate precomputed random-number generation and cryptographic key-exchange, which are part of Internet security protocols.

TECHNICAL APPROACH

The feasibility and efficiency of the proposed techniques will be evaluated through an end-to-end demonstrator with an energy-efficient micro-controller and with a wireless communication front-end. We develop techniques to spread out computations over time by reformulating cryptographic algorithms as capable of generating coupons, which are precomputed portions of the algorithm. We propose techniques for coupon generation and their secure storage in non-volatile, possibly off-chip memories. We also consider and optimize the impact of precomputed security protocols on the communication cost and the storage cost. We validate the proposed approach by constructing a prototype implementation on an energy-harvesting oriented microcontroller-based platform.

SUMMARY OF RESULTS

When a computing platform temporarily loses power, it stores its current state in a checkpoint, such that it can recover and continue execution at the point just before storing the checkpoint. A checkpoint also holds pre-computed results (or coupons) to support the execution of a single cryptographic algorithm over multiple power-loss events. We performed a detailed security analysis of storing checkpoints in non-volatile memory. Also, a checkpoint also holds pre-computed results. We identify three possible scenarios that can threaten the security of the checkpointing process: a checkpoint may be snooped (eavesdropped upon), a checkpoint may be spoofed (tampered), and a checkpoint may be replayed. Each of these attacks can lead to loss of information security on the IoT device, or loss of control.

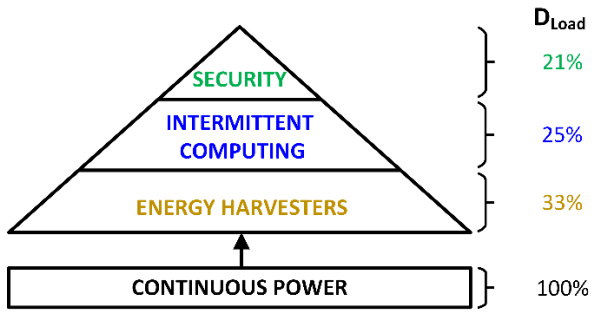

Figure 1. Performance Impact of Secure Intermittent Computing for ECDH.

We have evaluated the overhead of our proposed Secure Intermittent Computing protocol (SICP) for the case of cryptographic key exchange (ECDH). The prototype is constructed for a Texas Instruments MSP430FR5994 microcontroller that is performing key exchange under energy harvesting. The results are shown as a relative overhead compared to a continuously powered design. We measured the continuous ECDH operation to consume 6.3 mW and we assumed a 2 mW kinetic energy harvester, yielding a 33% duty cycle under intermittent operation. This duty cycle would imply key exchange takes 3 times as long under energy harvesting operation. The selected p160 curve for ECDH uses a 1211-byte checkpoint which must be stored and retrieved, and which reduces the duty cycle further to 25%. Implementing secure checkpoints, as enabled using SICP, adds additional overhead of encryption, and reduces the operation duty cycle to 21%. Hence, we conclude that the overhead of secure checkpointing on a realistic cryptographic protocol increases from 3x (only energy harvesting) to 5x (including secure checkpointing).

We have summarized out conclusions of the project in a forthcoming journal paper [1].

Keywords: cryptography, energy-harvesting, NVM applications, intermittent computing, MSP430

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] A. S. Krishnan, C. Suslowicz, P. Schaumont, “Secure and Stateful Power Transitions in Embedded Systems,” IEEE Transactions on VLSI Systems, under review.

TASK 2712.020, LOW-POWER MOSTLY DIGITAL TIME-DOMAIN DELTA-SIGMA ADCS FOR IOT

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SIGNIFICANCE AND OBJECTIVES

The aim of this project is to develop low-power, delta-sigma ADCs for IoT. A purely VCO-based highly digital architecture is investigated in this project. The target is to design high-order, digital delta-sigma ADC with power consumption less than 100μW.

TECHNICAL APPROACH

A modified digital phase-locked loop (DPLL) architecture is used for the proposed ADC design. The analog input perturbs the digitally controlled oscillator (DCO) phase and the DPLL changes the DCO control word to cancel out the phase perturbation. Thus, the DCO control word acts as a quantized representation of the analog input. Ring oscillators are used as DCO and DPLL loop filter, resulting in highly digital architecture and high-order quantization noise shaping. The merits of the proposed ADC are a) no nonlinearity calibration b) excess loop delay can be compensated without requiring auxiliary DAC and c) inherent DAC mismatch shaping.

SUMMARY OF RESULTS

We fabricated a 65-nm prototype VCO-based bandpass ADC by 4x time-interleaving our prior second-order LP-ADC [1]. *The prototype ADC achieves a band-pass walden FoM of only 57fJ/step which is the best reported so far.*

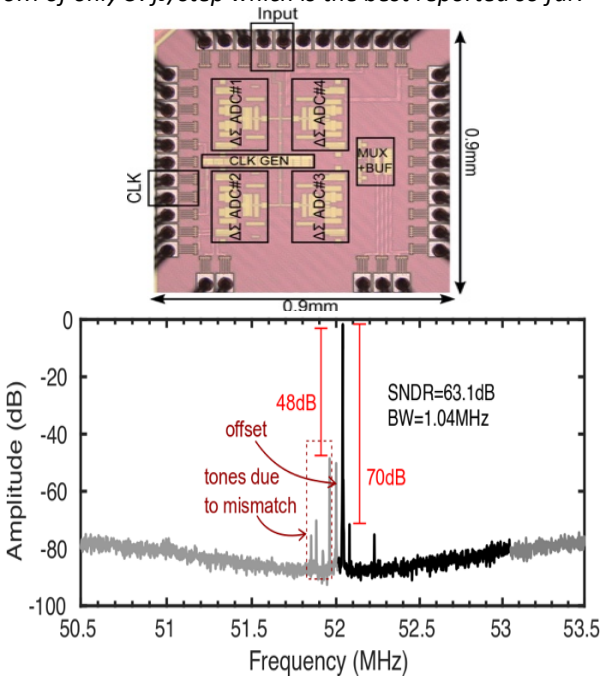

Figure 1. Prototype BP (bandpass) ADC and FFT plot.

While each sub-ADC has an NTF (Noise Transfer Function) proportional to $(1-z^{-1})^2$, the TI ADC has an NTF proportional to $(1-z^{-4})^2$ since the relationship between quantization error of adjacent samples in each sub-ADC is preserved even though the TI-ADC runs 4x faster. The BP ADC uses front-end passive-mixers to down-convert the input signal before feeding to the LP sub-ADCs. The sub-ADCs have intrinsic anti-aliasing that filters out replicas created due to mixing. After the sub-ADC outputs are sampled, only the signal at the input frequency is retained at the combined output while the replicas are canceled. In the presence of timing/gain mismatch between the sub-ADCs, the replicas are not perfectly canceled but fall out of band. Thus, the proposed BP ADC does not need calibration for mismatch errors. Use of passive-mixers reduce ADC SNR while maintaining CT operation. ADC SNR can be improved by sampling the input signal prior to quantization.

Fig. 1 shows a die photograph of our BP ADC as well as the measured FFT plot. The ADC has a dynamic range of 66dB at 1MHz bandwidth. Table 1 shows a performance summary of the prototype VCO based BP ADC.

Table 1. Performance summary.

Tech (nm)	Fs (MHz)	BW (MHz)	Power (mW)	SNDR (dB)	FoM_bp (fJ/step)
65	208	1	0.36	63	57

The future direction is to extend the order of noise-shaping by adding a noise-shaping SAR stage in front of the VCO ADC which will increase noise-shaping order and allow rail-to-rail input swing handling.

Keywords: ADC, VCO, DPLL, Delta-Sigma, Noise-shaping

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

[1] A. Jayaraj et al., "8.6fJ/step VCO-based CT 2nd-order delta-sigma ADC,'' IEEE A-SSCC, pp. 197-200, 2019.

TASK 2712.023, ULTRA-LOW-POWER COMPRESSIVE SENSING TECHNIQUES FOR IOT APPLICATIONS

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SIGNIFICANCE AND OBJECTIVES

For modern CMOS image sensor aiming for always-on IoT applications, achieving high energy efficiency is the key goal while maintaining substantial image quality. However, the increasing resolution makes the power consumption of pixel readouts continue to grow and further burdens the battery. Compressive sensing is capable of compressing the natural images in analog domain before digitization, which can greatly improve the energy efficiency of image sensors for IoT applications.

TECHNICAL APPROACH

Unlike the prior arts where compressive sensing (CS) was implemented with complex and power-hungry analog building blocks, a simple-but-effective CS framework for image capturing and an energy-efficient switched-capacitor matrix multiplier is proposed to implement the proposed CS image sensor. The proposed CS framework greatly reduces the number of pixels needed when generating each CS sample and introduced ±1 pseudo-random encoding as opposed to 0-1 binary encoding used in the prior arts. Moreover, the proposed switched-capacitor matrix multiplier works seamlessly with the dynamic source follower biasing for pixel readout and the dynamic single-slope ADC that digitizes the compressed result.

SUMMARY OF RESULTS

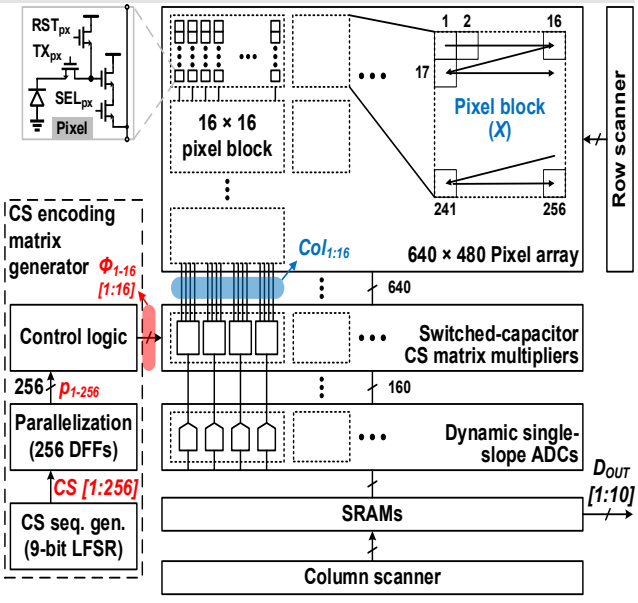

Figure 1. The architecture of the proposed CS image sensor.

The proposed CS image sensor architecture is shown in Fig. 1. The prototype is fabricated in a 110-nm CMOS process. Operating at 45 fps and 3.3/2.4/1.3-V pixel/analog/digital supply voltages, the image sensor consumes 0.7 mW, which results in an energy efficiency of 51 pJ/pixel. This energy efficiency is an over 20x improvement compared to the state-of-the-art CS imagers. Benefitting from both the CS encoder and ADC operating in a fully dynamic manner, the power scales with the sensor frame rate and the energy efficiency is maintained across different frame rates. It achieves a temporal noise of 0.90 LSB_{rms} and a low column FPN of 0.05 LSB_{rms}.

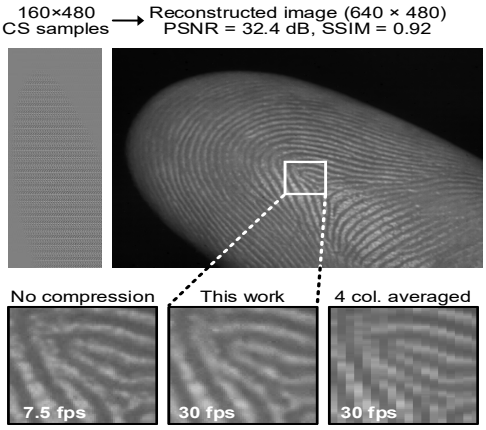

Figure 2. Sample image and comparisons.

Fig. 2 shows captured sample images. The sensor outputs a compressed image and the image is completely reconstructed into an image with full resolution via an L0 minimization algorithm. The chip supports not only CS mode, but also 2 other modes for comparison: i) no compression but with a 4x reduced frame rate, and ii) a simple average by averaging 4 adjacent pixels. Compared to the other modes, the proposed CS scheme retains the fine details without affecting the frame rate.

Keywords: compressive sensing, CMOS image sensor, switched-capacitor circuit, matrix multiplication, single-slope ADC

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] W. Zhao et al., "An Always-On 4x Compressive VGA CMOS Imager with 51pJ/pixel and >32dB PSNR," IEEE *Symposium on VLSI Circuits* (VLSI), Jun. 2020 (accepted).

TASK 2712.024, A SYSTEM-IN-PACKAGE PLATFORM FOR ENERGY HARVESTING AND DELIVERY FOR IOT EDGE DEVICES

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MADHAVAN SWAMINATHAN, GEORGIA INSTITUTE OF TECHNOLOGY

SIGNIFICANCE AND OBJECTIVES

The proposed research aims to design a System-In-Package (SIP) based energy delivery system for powering wireless sensor nodes and IoT edge devices.

TECHNICAL APPROACH

We will develop the architecture of the proposed system-in-package based energy harvesting and delivery system. We will design and fabricate the on-package inductor for the proposed energy delivery system. We will design, fabricate and test the power management unit of the proposed SiP.

SUMMARY OF RESULTS

PMU Test-chip: We have designed, taped out, and measured a test-chip in 65-nm CMOS for a self-powered system using on-chip or off-chip photodiodes. The design includes on-chip photodiodes for harvesting, a boost regulator with system based MPPT, and an encryption engine as a load. The IC is interrogated using optical power transfer via off-chip photodiodes and visible light based data transfer via on-chip CMOS diodes. Authentication is performed with a lightweight encryption engine PRINCE. The IC consumes 2.29µW standby power and achieves 53.8-kbps data rate.

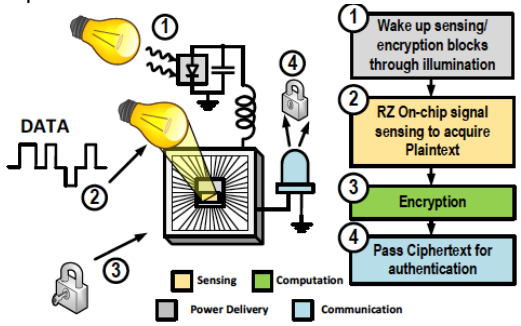
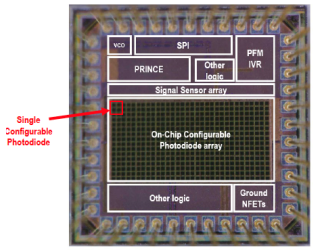


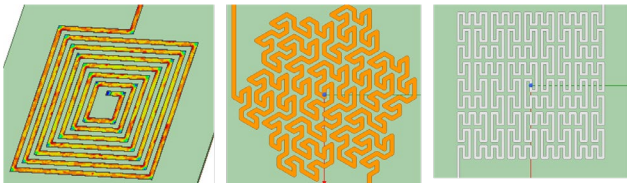
Figure 1. Overview of the self-powered authentication IC.



Technology	65nm CMOS
Package	CLCC44
Area	1mm x 1mm
Photodiode Area	720µm x 360µm
Photodiode FF	77%
VCO Max. Freq	500MHz
Encrypt. Eng Area	430µm x 180µm
IVR Area	15µm x 54 µm

Figure 2. Summary of the self-powered IC test-chip.

Fabrication of Inductors: The inductor works primarily focused on the performance impact of bending the inductor, especially when compared against the impact of bending a microstrip transmission line. Here, we found that the inductance and quality factor are significantly impacted by bending whereas bending a microstrip transmission line does not have a noticeable impact on its performance. This difference between the change in performance for the inductor compared to the microstrip occurs due to the accumulation of stress along the length of the inductor. When the inductor is bent, there is a larger accumulation of stress as more paths have an increase in stress due to the unequal distribution of stress along the length of the substrate. Since the inductor is centered on the substrate and the peak stress occurs at the center, the inductor experiences more total stress while bending increases. One method used to decrease the change in performance caused by bending is changing the inductor layout from a spiral shape to a fractal shape. The fractal shape decreases the total stress along the inductor's path. However, the disadvantage of these inductors is the overall decrease in the inductance and quality factor compared to the typical spiral inductor. This decrease in performance is caused by the length increase found on the fractal inductors compared to the spirals. Therefore, the spiral inductor was chosen as the final inductor architecture.



Keywords: Integrated voltage regulator, self-testing, and self-tuning

INDUSTRY INTERACTIONS

Intel

MAJOR PAPERS/PATENTS

[1] E. Lee, et al., "An Authentication IC with Visible Light Based Interrogation in 65nm CMOS," Custom Integrated Circuit Conference (CICC), 2019.
[2] S. Sivapurapu, et al., "Multi-Physics Modeling and Characterization of Components on Flexible Substrates," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 9, no. 9, pp. 1730-1740.

TASK 2712.027, GATE DRIVING TECHNIQUES AND CIRCUITS FOR AUTOMOTIVE-USE GAN POWER CIRCUITS

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SIGNIFICANCE AND OBJECTIVES

The double-step down (DSD) topology can support high switching frequency with high power density and high efficiency. However, because of the unique structure, the closed loop regulation for DSD topology should prevent the two sub-covnerters being turned on at the same time. Phase current balancing control is also necessary to avoid hot spots due to imbalanced phase currents.

TECHNICAL APPROACH

To achieve direct 48V/1V power conversion with a DSD topology, GaN HEMTs are used as power switches and a master slave adaptive ON-OFF time (AO2T) control is poposed. The elastic ON-time modulation leads to significant improvement on transient response and voltage droop performance, compared to prior arts. On-time (T_{ON}) overlap is also avoided to protect power switches from voltage breakdown. A master phase mirror enables adaptive master-slave phase synchronization and automatic phase current balancing for improved reliability.

SUMMARY OF RESULTS

The proposed GaN-based DSD power converter is shown in Fig. 1. There are one master sub-converter and one slave sub-converter in the DSD converter. To avoid the harmful ON-time (T_{ON}) overlap and current imbalance, a master-slave adaptive AO2T control is employed. In steady state, because load current I_O is constant, the elastic ON-time modulator (EOM) generates a fixed T_{ON} for both master and slave sub-converters. The feedback control for the master sub-converter is thus an adaptive-OFF time control, where T_{ON} is initialized at the trip point of V_{SEN} and V_{EA} in Fig. 2. M_{MH} in the master sub-conveter is on to charge L_M until T_{ON} expires. Meanwhile, a master phase mirror circuit records the instant switching period T_{SW} of the master sub-converter. After T_{ON} expires, M_{MH} is off and M_{ML} is on. The master sub-converter enters the discharge phase T_{OFF}, which is defined adaptively by I_O. At the instant of $T_{SW}/2$, the master phase mirror enables the slave sub-converter. M_{SH} is turned on to charge L_S for the same T_{ON}, followed by similar switching actions described in the master phase. During the dynamic transient, I_O changes. The EOM elastically adjusts T_{ON} to satisfy the new I_O, making the control an adaptive ON-time control. Similar switching actions described in steady state repeat. Combining the adaptive-OFF-time control in steady state and the adaptive ON-time control in dynamic transient, the converter thus accomplishes a truly adaptive-ON-OFF time control.

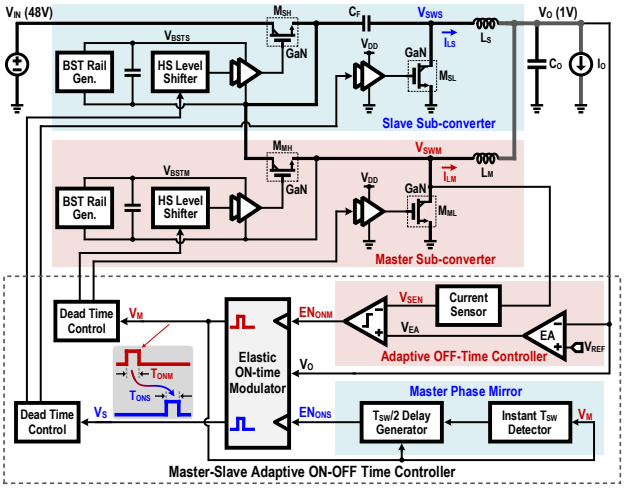

Figure 1. Block diagram of DSD GaN power converter.

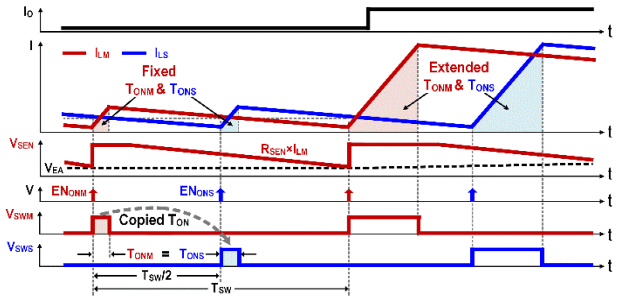

Figure 2. Operation scheme of DSD GaN power converter.

Keywords: GaN-based power converter, direct 48V/1V power conversion, double step-down architecture, adaptive ON- and OFF-time control, elastic ON-time modulation, master phase mirroring.

INDUSTRY INTERACTIONS

Texas Instruments, NXP, IBM

MAJOR PAPERS/PATENTS

[1] D. Yan, et al., "A Two-Phase 2MHz DSD GaN Power Converter with Master-Slave AO2T Control for Direct 48V/1V DC-DC Conversion," *2019 Symposium on VLSI Circuits*, Kyoto, Japan, 2019, pp. C170-C171.

[2] D. Yan, et al., "Direct 48-/1-V GaN-Based DC–DC Power Converter With Double Step-Down Architecture and Master–Slave AO2T Control," *in IEEE Journal of Solid-State Circuits*, vol. 55, no. 4, pp. 988-998, April 2020.

TASK 2712.028, HIGH PERFORMANCE MICRO-SUPERCAPACITOR ON A CHIP BASED ON A HIERARCHICAL NETWORK OF NITROGEN DOPED CARBON NANOTUBE SHEETS SUPPORTED MNO_2 NANOPARTICLES

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SIGNIFICANCE AND OBJECTIVES

This work is focused on improvement of electrochemical performance of microsupercapacitors using incorporation of metal oxide (manganese oxide nanoparticles) and changing the electrode interspacing. The effects of active material thickness and electrode interspacing were also studied.

TECHNICAL APPROACH

Different multi sheets of carbon nanotube were used to fabricate the devices. Manganese oxide nanoparticles were electroeposited on a CNT sheet using a three-electrode configuration at constant potential of 1.2 V for 10 s. Impact of resolution (gap) on the specific capacitance of the flexible devices was also investigated.

SUMMARY OF RESULTS

Pristine carbon nanotube based devices were used as the reference for each part of the experiments. In the first part, we studied how the electrode thickness would improve the specific capacitance, and energy and power density of the devices. Later we improved the electrochemical performance by decorating CNT sheets with manganese oxide nanoparticles.

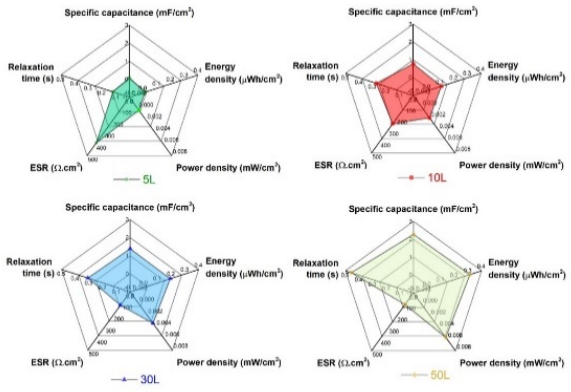

Figure 1. Specific capacitance, power and energy density, relaxation time, and equivalenet series resistance of microsupercapacitor as a function of thickness.

Fig. 1 shows the five important indices used to evaluate a supercapacitor device performance. As seen the highest specific capacitance of 2.5mF/cm^2 was obtained for microsupercapacitors with 50 layers of CNT sheets. High values of 0.3 μWh/cm^2 and 6 μW/cm^2 for power and energy densities, respectively were also obtained.

In the final phase we studied our microsupercapacitors on a flexible PET (Polyethylene terephthalate) substatrate. We investigated electrode interspacing (resolution) effect on improving the eletrochcemical performance through shortening the ion diffusion path.

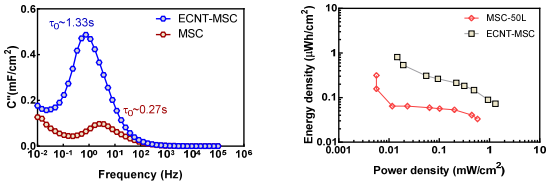

Figure 2. Left: frequency response of a microsupercapacitor device with 50 layers of CNT before and after Mn oxide incorporation. Right: energy and power density of the same device before and after oxide decoration on CNT sheets.

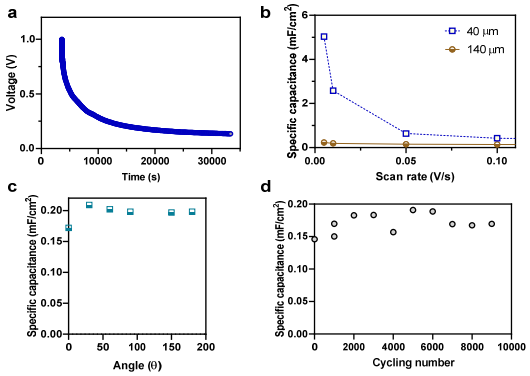

Figure 3. (a) self discharge of a microsupercapacitor device with 10 layers of CNT sheet on a flexible PET substrate, (b) specific capacitance versus sca rate at two resolution of 40 and 140 μm, (c) specific capacitance at different bending angle, (d) specific capacitance change with bending cycle.

Keywords: Carbon nanotube sheet, microsupercapacitor, metal oxide, micro-device, energy storage

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] B. Dousti, G. S. Lee, N. Geramifard, US Patent, Patent number. US 2020/0123009 A1, April 23, 2020

[2] B. Dousti, Y. Choi, S. Cogan, G. S. Lee, Ultrathin microsupercapacitors based on CNT, under review, ACS Nano, May 2020.

TASK 2810.002, SECURITY-AWARE DYNAMIC POWER MANAGEMENT FOR SYSTEM-ON-CHIPS

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SIGNIFICANCE AND OBJECTIVES

The proposed research investigates the energy-security trade-offs associated with Dynamic Power Management (DPM). The proposed effort will develop methodology to characterize security implications of DPM in SoCs and design circuit/system techniques to co-optimize security and energy-efficiency of DPM.

TECHNICAL APPROACH

This effort will pursue a cross-layer approach to understand the energy-security trade-offs in Dynamic Voltage Frequency Scaling (DVFS). First, we will design power domains that are secure against power-/EM- side-channel analysis by leveraging the distributed integrated voltage regulators. Next we will investigate energy-security trade-off at the chip level by focusing on the DVFS controller and algorithm. Finally we will explore an integrated approach considering secure power domains and secure DVFS controllers.

SUMMARY OF RESULTS

Side-channel Analysis of PRINCE: We present a 65-nm test-chip of a dual-mode PRINCE encryption engine, configurable between pipelined and fully unrolled modes. Correlation Power and EM analyses on test-chip measurements show minimal exploitability of leakage from registers, implying that unrolled PRINCE can be pipelined without significantly hurting its side channel robustness. The overall system has a minimum MTD (Minimum Trace to Disclose) of 460K and a projected maximum throughput of 502 Mega encryptions per second.

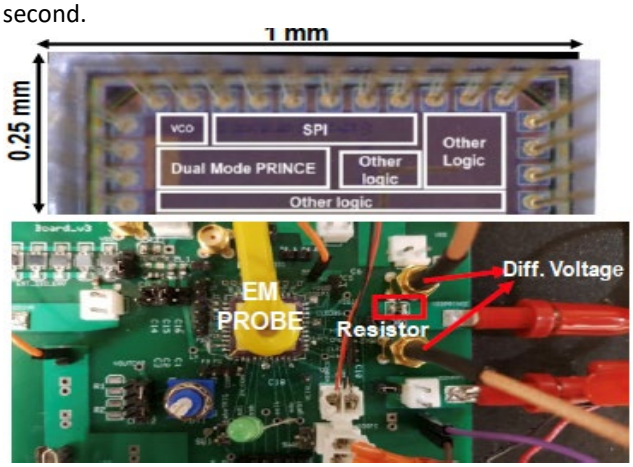

Figure 1. The architecture for digital LDO based power and electromagnetic emission based side channel security.

Metrics	Mode	
	Unrolled	Pipelined
Max Freq. (@ 1.1V)	102 MHz	496MHz
Encryption Latency	1 cycle	11 cycles
Projected Throughput	102 M enc/s	496 M enc/s
Power @ Max Freq.	1.76mW	8.04mW

	This work	ISSC '19 [5]	VLSI '16 [2]
Technology	65nm	130nm	28nm
Crypto Engine	Dual-Mode PRINCE	S-AES + P-AES	Unrolled PRINCE
Power	1.06mW @80MHz	10.9mW @ 80Mhz,	9.98mW @ 400 MHz
Gate count	9,301	N/A	N/A
Area	0.0774mm^2	‡0.062mm^2	0.0074 mm^2
MTD	460K @ 480 MHz**	< 10K* @ 86 MHz‡	N/A

Figure 2. Performance Summary of Test-chip.

DVFS based Application Inferencing and Malware Detection: We demonstrate Dynamic Voltage and Frequency Scaling (DVFS) states form a signature pertinent to an application, and its run-time variations comprises of features essential for securing IoT devices against malware attacks. We have demonstrated this proof of concept by performing experimental analysis on a Snapdragon 820 mobile processor, hosting Android operating system (OS). We developed a supervised machine learning model for application classification and malware identification by extracting features from the DVFS states time-series. The experimental results show >0.7 F1 score in classifying different android benchmarks and >0.88 in classifying benign and malware applications, when evaluated across different DVFS governors. We also performed power measurements under different governors to evaluate power-security aware governor. We have observed higher detection accuracy and lower power dissipation under settings of on-demand governor.

Keywords: Secure, Side-channel, Dynamic Power Management, Integrated Voltage Regulator, Dynamic Voltage Frequency Scaling

INDUSTRY INTERACTIONS

Intel, IBM

MAJOR PAPERS/PATENTS

[1] A. Singh, et al., "Enhanced Power & Electromagnetic SCA Resistance of Encryption Engines via a Security-Aware Integrated All-Digital LDO," IEEE Journal of Solid State Circuits (JSSC), vol. 55, no. 2 , Feb. 2020, pp. 478 – 493.

[2] N. M. Rahman, et al., "A Configurable Dual-Mode PRINCE Cipher with Security Aware Pipelining in 65nm for High Throughput Applications," IEEE Custom Integrated Circuit Conference (CICC), March 2020.

[3] N. Chawla, et al, "Application Inference using Machine Learning based Side Channel Analysis," IEEE International Joint Conference on Neural Network (IJCNN), 2019.

TASK 2810.003, INTEGRATED VOLTAGE REGULATOR MANAGEMENT FOR SYSTEM-ON-CHIP ARCHITECTURES

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SIGNIFICANCE AND OBJECTIVES

The modern sophisticated power delivery networks (PDNs) with integrated voltage regulators (IVRs) and advanced power management techniques (e.g., dynamic voltage freuqnecy scaling, DVFS) require system-level optimization and rigorous evaluation from the perspective of efficiency, stability, security, .etc.

TECHNICAL APPROACH

To systemically optimize and quantitatively evaluate the metrics of the IVR-enabled PDN configuration, we first propose two frameworks for IVRs: Ivory 2.0 [1], aiming at analytical modeling and system-level early-stage design space exploration; and PowerScout [2], focusing on side-channel vulnerabilities evaluation respectively. In Ivory, we introduce a fast, accurate, and validated static model and a novel method to derive the dynamic mode. In Power Scout, a wide spectrum of IVR topologies with a variety of metrics is covered to perform comprehensive design space exploration. IVR-enabled power delivery system opens the door for microsecond level fast power management. Then we propose HiFIVE [3]–a hierarchical fast power management framework to adaptively change V/F at the microsecond (μs) timescales.

SUMMARY OF RESULTS

Ivory's feasibility of exploring IVR-enabled PDN early-stage design space is demonstrated by optimizing the PDN configuration of SoC systems. A novel dynamic model [1] is proposed to analyze the transient responses of IVR based power delivery system (as shown in Figure 1). Ivory helps the designers achieve maximum efficiency while maintaining minimum voltage noise.

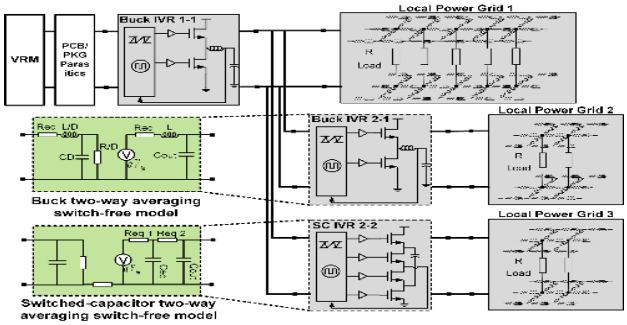

Figure 1. Hierarchical power delivery system with integrated voltage regulator (IVR) dynamic models.

In addition to high efficiency and low noise, another benefit of IVR-enabled PDN demonstrated by Ivory is that IVR enables fast dynamic voltage frequency scaling (DVFS). Compared to the native DVFS with conventional PDN configuration, the fast DVFS supported by IVR can reach finer granularity and save more energy. When equipped with per-core IVR, HiFIVE - the proposed hierarchical and fast power management framework could achieve significant energy savings (35.2%) across a broad range of workload benchmarks. Compared with existing state-of-the-art DVFS-based power management schemes that can only operate at millisecond timescales, it provides notable (up to 11%) Energy-Delay Product (EDP) improvements [3].

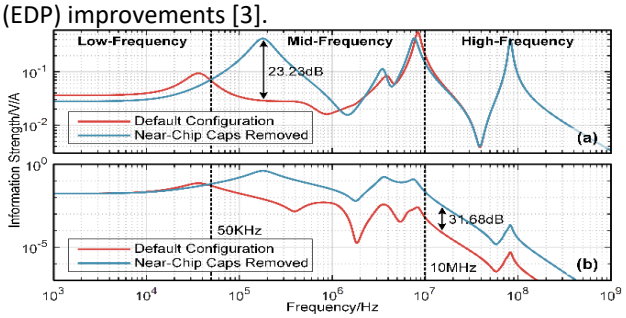

Figure 2. The information strength of (a) intra-chip and (b) inter-chip information leakage under two configurations.

For the security perspective of PDN, the results show that PowerScout can correctly predict the performance of the attack. With PowerScout, we revel that emoving near-chip capacitors can increase intra-chip information leakage by a maximum of 23.23dB at mid-frequency and inter-chip leakage by an average of 31.68dB at mid-and high-frequencies (as shown in Figure 2a). And for inter-chip information leakage, near-chip capacitors increase information strength at both mid and high frequencies by an average of 31.68dB (as shown in Figure 2b).

Keywords: Integrated voltage regulator,DVFS, security

INDUSTRY INTERACTIONS

Intel

MAJOR PAPERS/PATENTS

[1] A. Zou et al., "Ivory 2.0 System-Level Early Stage Modeling Framework for IVR-enable Power Delivery System," IEEE Trans. on CAD. (under review)

[2] H. Zhu et al., "PowerScout: A Security-Oriented Power Delivery Network ModelingFramework for Cross-Domain Side-Channel Analysis," 2020 ICCAD. (under review)

[3] K. Garimella et al., "HiFIVE: Hierarchical Fast Integrated Voltage and Frequency Scaling for Energy-Efficient Multi/Manycore Processors," 2020 ICCAD. (under review)

TASK 2810.006 COMBATING UNPRECEDENTED EFFICIENCY, NOISE AND FREQUENCY CHALLENGES IN MODERN HIGH CURRENT INTEGRATED POWER CONVERTERS

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SIGNIFICANCE AND OBJECTIVES

To deal with the EMI emissions in GaN power converters, a continuous random spread-spectrum-modulaiton (SSM) scheme is developed. It employs a Markov-chain-based random clock generator to modulate the switching frequency of the power converter in the analog domain. Thereby, the EMI spectra is spread uniformaly and continuously, attenuating the EMI noise.

TECHNICAL APPROACH

Based on a chaotic dynamic system, a Markov-chain-based random clock generator is built to implement the analog f_{SW} modulation within a sideband of Δf_C centered at f_{SW0}. Hence, it conducts SSM continuously and spreads the spurious noise at f_{SW0} and its harmonics uniformly, achieving desirable C-RSSM. Compared to conventional discrete RSSM (D-RSSM), it effectively overcomes the finite frequency resolution limitation, thus achieving a better EMI noise compression.

SUMMARY OF RESULTS

Spread-spectrum modulation (SSM) techniques are prevalent in industrial power products for EMI reduction. By distributing the switching frequency within a certain sideband, the EMI energy originally concentrated at the fundamental frequency and its harmonics is spread to a lower level. For effective EMI suppression, it is highly preferable to accomplish continuous RSSM (C-RSSM). For this purpose, a Markov-chain-based random clock generator is designed to realize random f_{SW} modulation in the analog domain. Beneficially, it conducts SSM continuously and spreads spurious noise uniformly. As illustrated in the spectrum plot of Fig. 1, although conventional D-RSSM could achieve similar peak EMI reduction (ΔEMI) with a wider modulation range, it elevates noise floor significantly due to spectral overlap. In the proposed Markov C-RSSM, the peak EMI and noise floor are both effectively attenuated with minimal die-area overhead.

The core of the proposed continuous RSSM technique is the Markov-chain-based random clock generator. It utilizes a random voltage sequence denoted as $\{V_{ran}\}$. Based on a chaotic dynamic system, the state transitions satisfy the Markov character.

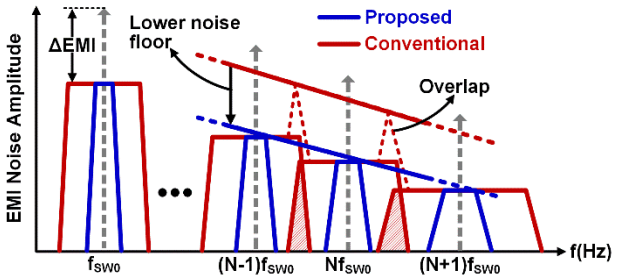

Figure 1. Spectral plot of the proposed C-RSSM scheme.

The circuit is designed as shown in Fig. 2. To compute the new state $V_{ran}[n+1]$, the present one $V_{ran}[n]$ is fed into a G_m-cell. The converted current I_{gm} is then driven into a summation node Σ. Meanwhile, $V_{ran}[n]$ is compared to a reference V_M. The result multiplies the current I_1 in binary to implement the Markov partition. Finally, a fixed current I_2 is subtracted from Σ to generate the random current I_{ran}, leading to $V_{ran}[n+1]=I_{ran}\times R_1$. Triggered by V_{CMP}, $V_{ran}[n+1]$ is sampled to adjust the VCO input and the clock frequency.

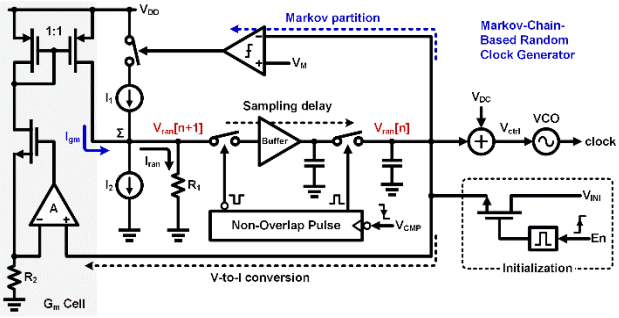

Figure 2. Schematic of the Markov-chain-based random clock.

Keywords: GaN, continuous RSSM, EMI noise

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Y. Chen and D. Ma, "EMI-regulated GaN-based switching power converter with Markov continuous random spread-spectrum modulation and one-cycle on-time rebalancing," IEEE J. Solid-State Circuits (JSSC), vol. 54, no. 12, pp. 3306-3315, Dec. 2019.

[2] Y. Chen and D. Ma, "An 8.3MHz GaN power converter using Markov continuous RSSM for 35dBμV conducted EMI attenuation and one-cycle T_{ON} rebalancing for 27.6dB V_O jittering suppression," ISSCC, Feb. 2019, pp. 250-251.

TASK 2810.008, CIRCUIT TECHNIQUES FOR FAST STARTUP OF CRYSTAL OSCILLATORS

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SIGNIFICANCE AND OBJECTIVES

High-Q crystal oscillators (XOs) are notorious for being extremely slow to start-up. Their long start-up time increases the average power consumption in duty-cycled systems such as Internet-of-Things. The objective of this work is to reduce the start-up time with minimal energy consumption.

TECHNICAL APPROACH

Previously, we demonstrated an XO start-up technique that pre-energizes a high-Q resonator close to its steady-state energy using a low-Q "injection" oscillator for a precisely-calculated, short, duration (~100cycles) [1]. The technique achieved 15x faster startup than prior art. The short injection duration, which amounts to wideband signal injection, together with a PTAT injection drive make it tolerate upto +/-6500ppm injection frequency errors from temperature and process variability. In this project, we are further enhancing our technique's tolerance to injection frequency errors and also extending it to other oscillator topologies such as ultra low power RTC XOs.

SUMMARY OF RESULTS

First, we have developed a technique that adjusts T_{inj}, based on a coarse temperature sensor. We developed a theory that identifies the precise T_{inj} for a given temperature (upto 10% inaccuracy in T_{inj} is tolerable) and verified the technique using our previous hardware demonstrating tolerance of up to +/-9000ppm injection frequency error without sacrificing our excellent startup time [2]. Second, we extended our startup technique to a new XO topology that employs DC-only sustaining amplifiers and series resonance operation. We achieved the lowest reported power consumption of 0.55nW for a 32kHz XO [3], and a patent has been filed jointly with SRC [4]. Third, we performed comparative theoretical analysis of injection strategies viz., single-tone, chirp and dithered frequency injection, and our precise energization [2] based on the premise that startup time, startup energy, and sensitivity to injection frequency mismatch depend strongly on the PSD of the injection signal. We showed that the wideband PSD of chirping and dithered injection signals renders them more tolerant of frequency injection errors but at a significant startup time and energy cost compared to our technique, as shown in Fig. 1 [2].

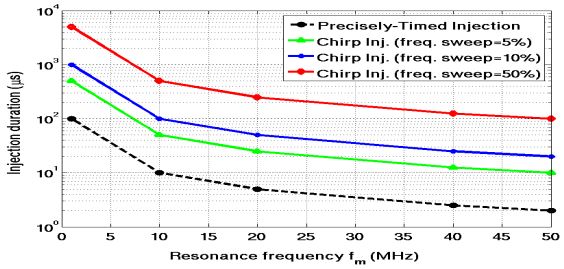

Figure 1. Optimal injection duration of precisely-timed injection technique compared to the chirp injection technique over different oscillation frequencies.

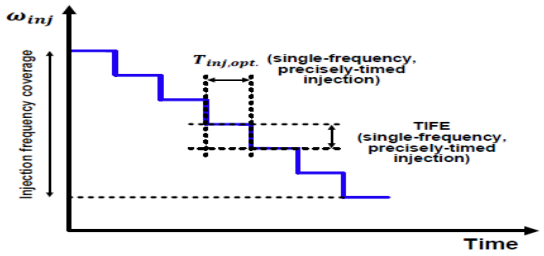

Figure 2. Proposed injection profile.

We are currently developing a prototype IC that will employ a proposed optimum "injection profile" (Fig. 2) derived from this analysis, to simultaneously reduce startup time (and hence, startup energy) and improve tolerance to injection frequency errors. As shown, the injection frequency is "chirped", but in discrete steps, and at each step, a very short, precise injection duration will be employed.

Keywords: Start-up time, crystal oscillators, low power, oscillator sustaining amplifiers, real time clocks

INDUSTRY INTERACTIONS

Intel

MAJOR PAPERS/PATENTS

[1] H. Esmaeelzadeh, "A Quick Startup Technique for High-Q Oscillators Using Precisely Timed Energy Injecton," JSSC 2018.

[2] H. Esmaeelzadeh, "Low-Energy Clock Generation for IoT Applications," Ph.D. Thesis, UCLA, 2019.

[3] H. Esmaeelzadeh, S. Pamarti, "A sub-nW 32-kHz Crystal Oscillator Architecture Based on a DC-Only Sustaining Amplifier," JSSC Dec 2019 (ISSC special issue).

[4] S. Pamarti et al., Ultra-low-power Oscillator with DC-Only Sustaining Amplifier, US 16/726,721 filed with SRC.

TASK 2810.009, MIXED-SIGNAL BUILDING BLOCKS FOR ULTRA-LOW POWER WIRELESS SENSOR NODES

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DAVID BLAAUW, UNIVERSITY OF MICHIGAN

SIGNIFICANCE AND OBJECTIVES

This project develops novel and state-of-art ultra-low power mixed-signal circuits, suitable for IoT systems. This includes timekeeping circuits, amplifiers, and CMOS-based sensors.

TECHNICAL APPROACH

The most challenging ultra-low power circuit components are mixed-signal circuits such as timers, clock sources, sensing and interface circuits (e.g., temperature sensors and low-noise amplifiers). Some of these cannot be duty cycled (e.g., timers), while others require both low noise and low power (e.g., amplifiers), which are traditionally mutually exclusive. This work proposes new ULP designs for: 1) crystal oscillator based real time clocks (RTCs), 2) temperature-compensated wakeup timers, 3) temperature sensors, and 4) front-end low-noise amplifiers.

SUMMARY OF RESULTS

We proposed a 32-kHz crystal oscillator (XO) with high energy-to-noise-ratio pulse injection. The design techniques we propose are: (1) NMOS-only pulsed driver; (2) frequency-divided (4kHz), high energy-to-noise-ratio pulse injections at peaks and valleys of the XO waveform; (3) a current reference with switched-capacitor resistance and ultra-low leakage switches to provide precise current in PVT variations; (4) a T/4-delay clock slicer to both convert the sinewave XO waveform to square wave and generate delay for timing of the energy injection. Fig. 1 shows the architecture of the proposed 32-kHz crystal oscillator.

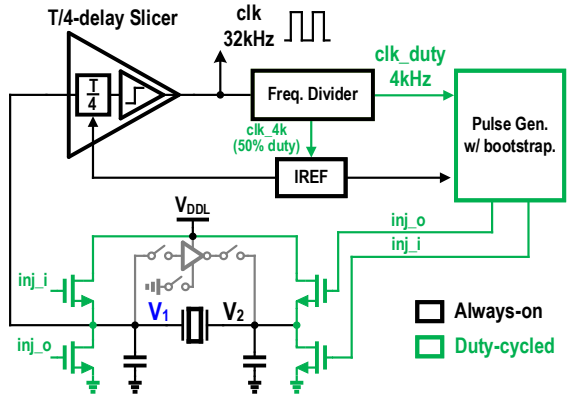

Figure 1. The architecture of the proposed crystal oscillator.

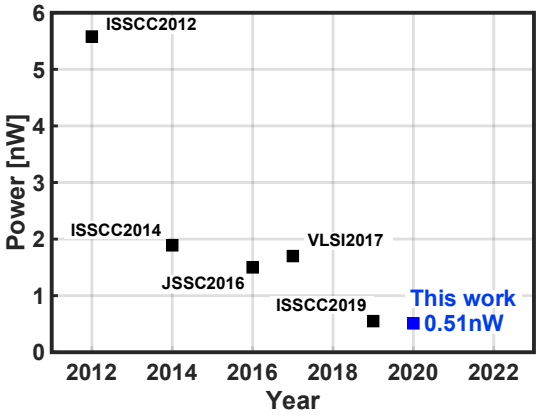

Figure 2. Power consumptions of nW XOs.

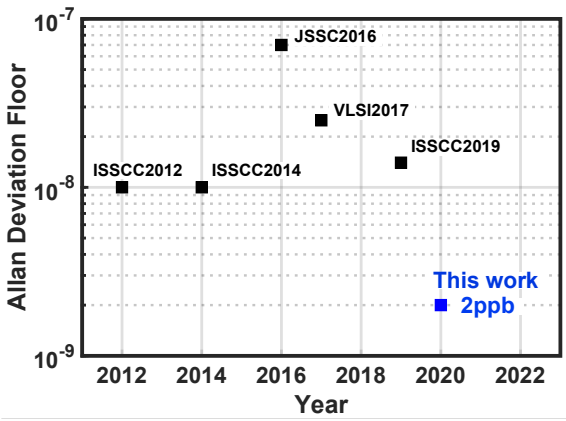

Figure 3. Allan deviation floor of nW XOs.

The proposed XO was fabricated in a 40-nm CMOS process and the layout area including the startup circuit is 0.02 mm^2. With two power supplies, 0.45V and 0.15V, ECS-2X6-FLX crystal, and a 135-mV oscillation amplitude across the crystal, the measured power consumption is 0.51nW at 25°C, which is the lowest among the reported 32-kHz crystal oscillators.

Keywords: CMOS, crystal oscillator, ultra-low power

INDUSTRY INTERACTIONS

NXP

MAJOR PAPERS/PATENTS

[1] L. Xu et al., "3.3 A 0.51nW 32kHz Crystal Oscillator Achieving 2ppb Allan Deviation Floor Using High-Energy-to-Noise-Ratio Pulse Injection," 2020 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2020, pp. 62-64.

TASK 2810.010, GS/S ADC BASED CYCLE-TO-CYCLE CLOSED-LOOP ADAPTIVE SMART DRIVER FOR HIGH-PERFORMANCE SIC/GAN POWER DEVICES

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SIGNIFICANCE AND OBJECTIVES

As the input/output voltage ratio increases, buck converters suffer from degraded power efficiency. The objective of this research is to demonstrate a 3-level buck converter using GaN switches that maximizes the power efficiency while utilizing a novel control algorithm based on machine learning (ML).

TECHNICAL APPROACH

We propose a 3-level buck converter capable of down-converting an input voltage (V_{IN}) at 48V to an output voltage (V_{OUT}) at 5V with high efficiency. Compared to a 2-level buck, the 3-level topology cuts the voltage stresses across the 4 GaN switches by half to significantly reduce the switching losses. Instead of employing conventional control loops using energy-costly error amplifiers, we propose an on-chip machine-learning-based control althrighm to deliever precise V_{OUT}. With these two approaches, the prototype chip can produce highly-precise V_{OUT} with high energy efficiency over a wide range of load current (I_{OUT}).

SUMMARY OF RESULTS

A. Overall Topology of the Proposed 3-level Buck Converter and Operational Principle

Fig. 1 depicts the architecture of the proposed 3-level buck converter. Four GaN switches controlled by PWM logic form a 3-level buck converter. Between the two gates of high-side GaN switches and the level shifters, 6-phase Gaussian gate drivers as illustrated in [1] are constructed. Using Gaussian regulation during the switching process, the electromagnetic interferences (EMI) levels are reduced by up to 49dB meanwhile maintaining a high power efficiency.

A novel machine-learning-based control algrithm is realized on-chip to replace the conventional error amplifiers to save the quiescent power consumption of the chip. During the buck operations with different I_{OUT} and V_{IN}, an on-chip PWM generator produces a 2MHz driving clock with a reconfigurable duty ratio to produce the desired PWM signals. The parameters of the PWM generator are obtained through training using a machine learning approach. The trained parameters are then stored on-chip to be used for the buck operations.

To further improve the power efficiency, a Zero-Voltag-Switching (ZVS) technique is implemented to reduce the I-V overlap when turning on each of the GaN switches.

B. Chip implementation and layout photo.

The proposed 48-to-5V 3-level buck converter is implemented using a 0.18-μm BCD process with a chip size of 2mm x 2mm as shown in Fig. 2. The design is currently being manufactured by TSMC.

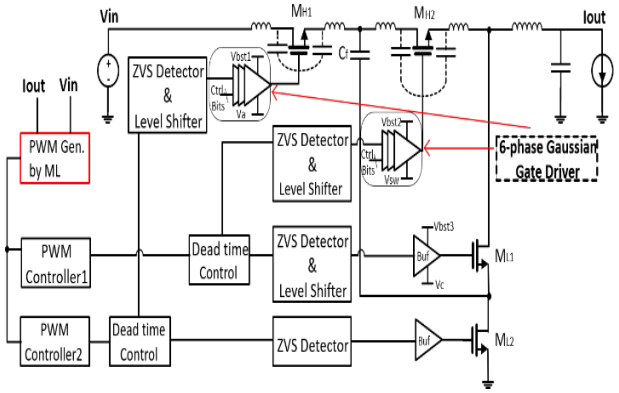

Figure 1. Architecture of the proposed 3-level buck converter with Gaussian regulation and machine learning techniques.

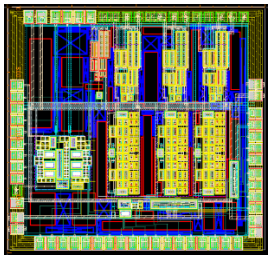

Figure 2. Layout photo of the proposed 3-level buck converter based on ML technique.

Keywords: GaN driver, Gaussian transition regulation, machine learning, smart driver, 3-level buck

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] C. Yang, P. Gui and et. al., "A 10MHz 40V VIN Slope-Reconfigurable Gaussian Gate Driven GaN DC-DC Converter with 49.1dB Conducted EMI Noise Reduction at 100MHz," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), 2020.

TASK 2810.011, MICRO-POWER ANALOG-TO-DIGITAL DATA CONVERTERS FOR SENSOR INTERFACES

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SIGNIFICANCE AND OBJECTIVES

MEMS-based sensor sytems have many applications in automotive electronics, Iot, and communication. Their interface circuits require data converters with high accuracy and power efficiency. This project has developed such an analog-to-digital converter. It is based on novel circuitry, and meets all of its specifications.

TECHNICAL APPROACH

We have developed a novel active noise-shaping SAR ADC. It is based on a two-capacitor DAC, embedded in a high-accuracy digitally corrected circuit. To mitigate the effects of non-idealities noise filtering, correlated double sampling and correlated level shifting are used. These techniques correct the non-idealities of the opamp used. Also, to cancel the effects of mismatches and parasitic capacitors, the complete circuit is calibrated using a novel bit-by-bit digital correction technique. This process accurately calculates the conversion error for each bit. These errors are then saved in a look-up table, and used to enhance the accuracy of the conversion.

SUMMARY OF RESULTS

The simplified circuit of the active noise-shaping SAR A/D converter is shown in Fig. 1. The circuit includes the two-capacitor DAC (C1 and C2), an amplifier with integrating capacitors (C3), correlated double sampling capacitors (C4) and correlated level shfting capacitors (CLS). Fig. 2 shows the die photo of the fabricated device, and Fig. 3 the measured output spectra.

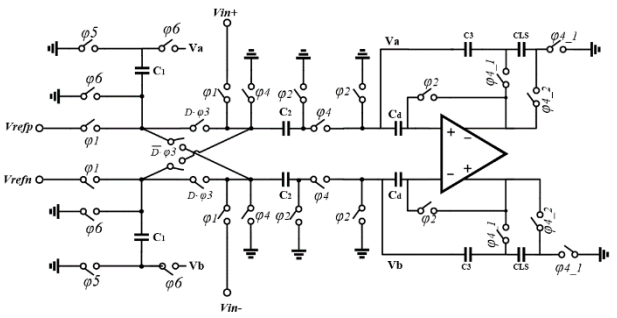

Figure 1. Simplified circuit diagram of the active noise-shaping SAR ADC.

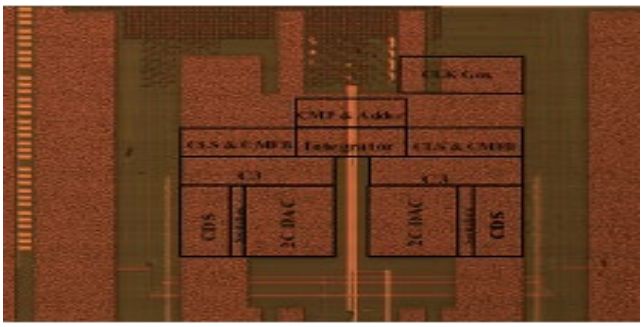

Figure 2. Die photo.

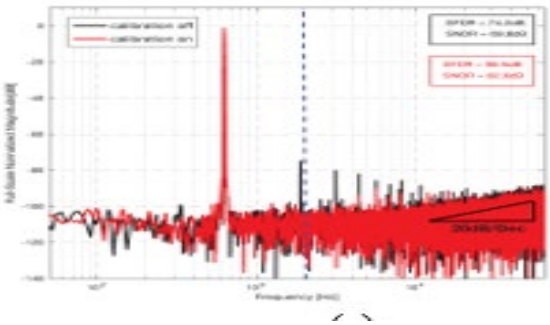

Figure 3. Measured output spectra. Black: without calibration; red: with calibration.

The ADC was fabricated in a 0.13-μm CMOS technology. It achieved 85.1 dB DR, 82.6 dB SNDR and 90.9 dB SFDR within a 2-kHz signal bandwidth for 32 oversampling ratio (OSR). It consumes 40.8 μW power using a 1.6 V power supply. Calibration added 13 bits to the SNDR.

Keywords: Active noise-shaping SAR ADCS; ADCs for MEMS; high-accuracy ADCs; sensor interfaces

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

[1] Shi, L., Zhang, Y. Wang, Y. Kareppagoudr and Temes, G.C., "A 13b ENOB Noise Shaping SAR ADC with a Two-Capacitor DAC," IEEE International Midwest Symposium on Circuits and Systems, Windsor, Ontario, Aug 5-8, 2018.
[2] Shakya, J. and Temes, G.C., "Predictive Noise-Shaping SAR ADC," IEEE Internat. Circuits and Systems Symp., Sapporo, Japan, 2019.

TASK 2810.012, NPSENSE – NANO-POWER CURRENT SENSING

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ROGER ZAMPARETTE, TU DELFT

SIGNIFICANCE AND OBJECTIVES

Battery fuel gauges usually employ a shunt-based Current-Sensing System (CSS). State-of-the-art CSSs consume µWs of power to achieve the required performance. However, many IoT or wearable applications require power consumption in the sub-µW range. This project aims to develop nano-power CSSs suitable for battery fuel gauges.

TECHNICAL APPROACH

Continuous-Time Delta-Sigma Modulators (CTΔ∑Ms) are a good choice for this task since they have relaxed settling requirements and thus dissipate less power than discrete-time ∑ΔMs. However, achieving sufficient accuracy, is quite challenging since resistor mismatch may then become the limiting factor. Further reductions in power consumption can be achieved by the use of aggressive duty-cycling at the circuit level e.g. in reference voltage generation and bias circuits.

SUMMARY OF RESULTS

This report presents the results of the first prototype towards nano-power CSSs. The proposed architecture (shown in the single-ended form in Fig. 1) uses a 1st-order CTΔ∑M to digitize the voltage drop across an integrated shunt resistor.

The choice of a 1st order modulator is motivated by the fact that its output can be decimated by a sinc filter. Such a filter has a uniform response, which means that short current pulses will be properly averaged by the CSS irrespective of when they occur.

A key feature of the modulator is that its summing node is implemented by a Capacitively-Coupled Instrumentation Amplifier (CCIA), which allows the handling of beyond-the-rail input common-mode voltages and improves energy-efficiency.

An 8-tap FIR-DAC was used in the modulator's feedback path. It reduces the signal error in the loop and allows the use of energy-efficient current-reuse amplifiers. A small drawback is the need for an extra compensation path to deal with the increased delay in the feedback path.

To deal with the large TCR (0.3%/K) of the integrated shunt, the modulator employs a temperature dependent reference voltage made by combining ΔV_{BE} and V_{BE}.

The circuit was taped-out in a 180-nm standard CMOS technology, occupies 1.95 mm^2, and draws 1.3 µA. The chip photograph is shown in Fig. 2.

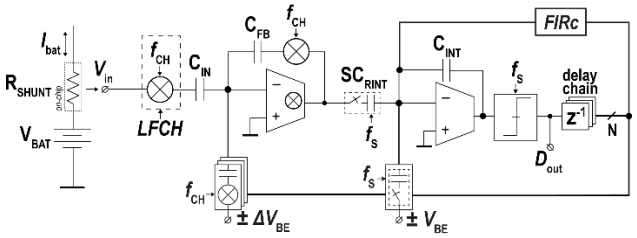

Figure 1. Simplified Single-Ended Circuit Architecture.

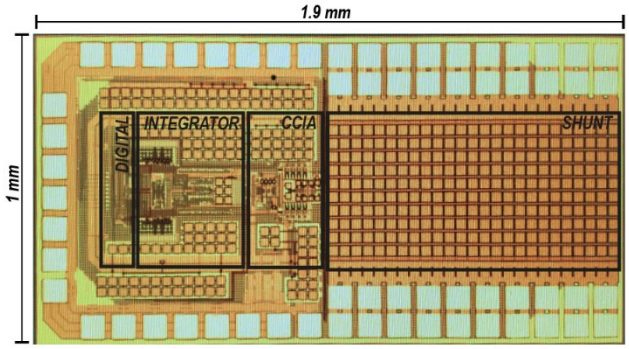

Figure 2. Chip photograph.

Since it is chopped, the CCIA was expected to have a low offset. However, as shown in Fig. 3, a large offset of 560 µV was observed. This was traced to two causes. One, the low off-impedance of a switch that resets the integration capacitor limited the modulator's loop gain, and hence its detection limit. Two, the mismatch of the two pseudo-resistors used to bias the CCIA's inputs. These issues will be fixed in a redesign which will be taped-out in June 2020.

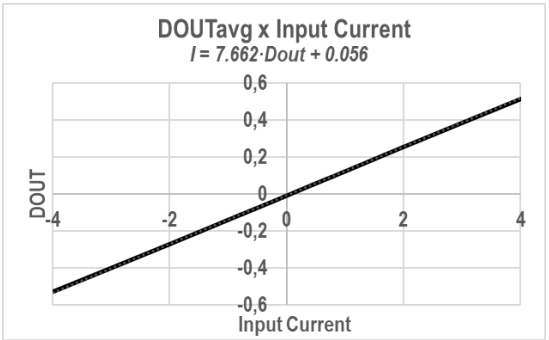

Figure 3. Sensor DC transfer function.

Keywords: current-sensing, continuous-time, shunt-based, capacitively-coupled, fir-dac

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

TASK 2810.032, DRIVR: A DIGITAL, RECONFIGURABLE, UNIFIED CLOCK-POWER (UNICAP) FABRIC FOR ENERGY EFFICIENT SOCS

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SIGNIFICANCE AND OBJECTIVES

Integrated Voltage Regulation (IVR) -- remains a critical technology for driving sustained efficiency in SoCs, offering buck converter efficiencies without additional bulky components. The objective of this effort is to devise a domain-scalable run-time programmable IVR fabric that drives and leverages advances in adaptive clocking and SIMO design (Fig. 1).

TECHNICAL APPROACH

The design effort is organized into four thrusts (1) analyzing the effectiveness of UniCaP in designs with a large insertion delay; (2) Demonstrate domain-scalable SIMO implementation, critical to providing the necessary flexibility required for a dynamically programmable IVR fabric; (3) Investigating optimal design-time allocation of cross-bar switches which connect modules to domains based on SoC usage profiles; and (4) Designing a tileable buck architecture that can be configured at run-time either as a single-buck, a phase in a multi-phase buck, or a SIMO converter. The goal of the effort is to implement a test chip demonstration that incorporates all 4 efforts.

SUMMARY OF RESULTS

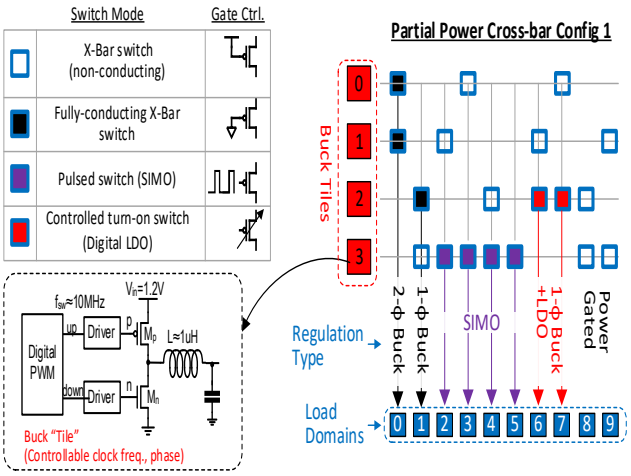

Figure 1. Proposed DRIVR fabric used to allow a limited number of buck-tile "resources" to service a larger number of active voltage domains.

At this time, we have performed analysis on the impact of insertion delay on uniCaP effectiveness, and corroborated the analysis with SIPICE simulations. A 65-nm test chip is being tested to provide the required silicon validation.

Early results indicate that the analytical model is very effective at predicting the functional inter-dependence of insertion delay, droop duration and V_{dd}-sensitivity mismatch between distribution and critical path. However, it has been found to be wanting in accurately predicting the extent of margin reduction degradation due to these effects. This model is currently at the center of our effort in tandem with test-chip measurements for Thrust 1. Fig. 2 shows early silicon measurements obtained from the test-chip, showing the impact of insertion delay, clock distribution-critical path sensitivity mismatch, and supply noise frequency on margin reduction.

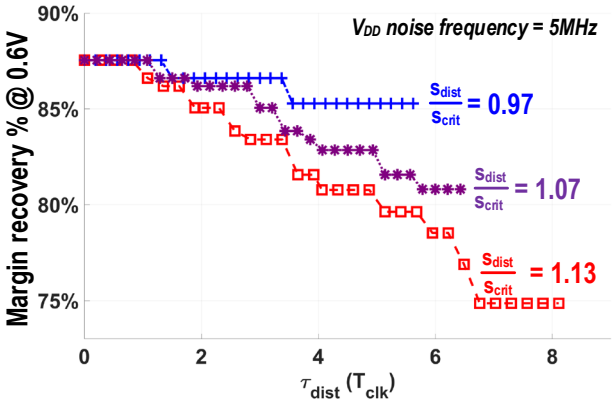

Figure 2. Margin recovery vs. insertion delay (units of Tclk) for different Vdd sensitivies between the clock distribution and the circuit critical path.

A parallel test chip effort is also underway on Thrust 2, exploring an architecture to address the linear degradation of V_{dd} droop as domain-counts scale.

Keywords: UniCaP, SIMO, Configurable Voltage Regulation

INDUSTRY INTERACTIONS

NXP, Intel, ARM

MAJOR PAPERS/PATENTS

TASK 2810.034, ALWAYS-ON KEYWORD SPOTTING BASED ON ANALOG-MIXED-SIGNAL COMPUTING HARDWARE

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SIGNIFICANCE AND OBJECTIVES

The primary goal of the project is to create hardware-design knowledge and techniques on analog-mixed-signal (AMS) hardware for artificial intelligence (AI) and machine-learning (ML) related computing. Specifically, we will create AMS hardware which can provide significant benefit in scaling power consumption in acoustic signal classification tasks.

TECHNICAL APPROACH

We will conduct the planned research as follow. (i) We will design *new feature extraction AMS hardware that uses non-linear circuits*. (ii) We will develop a compact model of the non-linear AMS hardware, and by using the model, we will develop *a training model that can effectively tolerate the variability of AMS computing hardware*. (iii) We will design a matching back-end *classifier based on deep neural network (DNN)*. We will develop the digital circuits to map the model at the minimal leakage/power consumption. By combining the developed architecture/techniques, we will prototype one test chip for the AMS front end and another for the end-to-end multi-keyword recognition systems.

SUMMARY OF RESULTS

During Jan 2020 - Apr 2020, we have worked on the AMS feature extraction front-end based on non-linear circuits. Our goal was to reduce the power consumption of the front-end by another 10X from our prior work [1,2]. To achieve this goal, we have explored three options. The first is to reduce the system bandwidth, the second option is to elevate noise floor, and the third option is to employ non-linear circuits. We found that the third option is the most promising. As shown in Fig. 1, the first two options can reduce power but at a non-negligible amount of classification accuracy degradation. The third option, relaxing linearity, has the potential to save power at no/little accuracy degradation.

Based on this idea of using non-linear circuits, as shown in Fig. 2, we have designed a new featue-extraction front-end. The low noise amplifier (LNA) adopts a single-ended input so do the bandpass filters, which improve the power efficiency by 2X. We employ asymmetric amplifiers followed by a half-wave rectifier. The asymmetric amplifier does not care about the clipping in the output voltage, which largely relaxes design complexity and reduces power dissipation. The rectifier is a very simple structure based on a single transistor biased in the sub-threshold region. The current output of the rectifier is integrated in a integrated and fire (IAF) neuron producing spike inputs to the digital DNN backend designed for keyword classification.

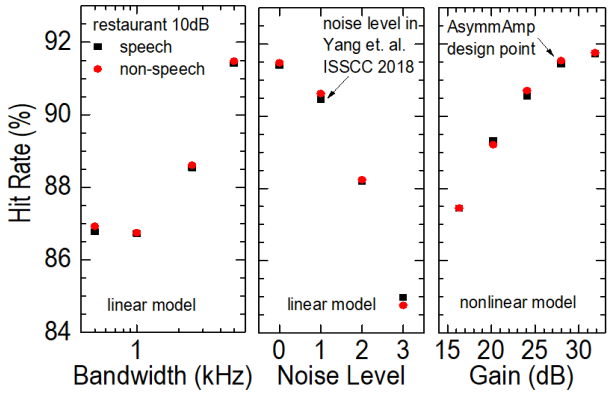

Figure 1. Three knobs to improve power-efficiency: bandwidth (left), noise (middle), and linearity (right).

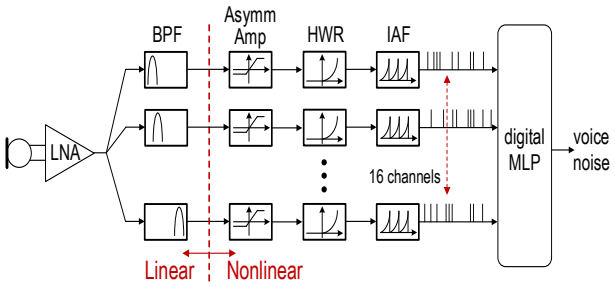

Figure 2. The proposed 16-channel AMS feature extraction front end based on non-linear circuits. In the test chip measurement, it consumes only 80 nW.

A test chip chip has been frabricated and the measurement has started. The entire front-end consumes only 60 nW, which is ~10X less than our prior work [1,2].

Keywords: Keyword spotting, speech command recognition, AMS computing hardware, signal to feature conversion, deep neural networks

INDUSTRY INTERACTIONS

Intel

MAJOR PAPERS/PATENTS

[1] M. Yang, et al., "A 1μW voice activity detector using analog feature extraction…," ISSCC, 2018.
[2] M. Yang, et al., "Design of an Always-On Deep Neural Network Based 1 μW Voice…"JSSC, 2019.

TASK 2810.035, COMPUTATIONALLY CONTROLLED INTEGRATED VOLTAGE REGULATORS

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SIGNIFICANCE AND OBJECTIVES

The enhanced spatio-temporal control afforded by increasingly Integrated Voltage Regulation (IVR) in modern SoCs is critical to achieving efficiency. This effort proposes to examine computationally intensive IVR control strategies for buck and LDO designs in particular, geared toward improving transient response in terms of peak droop and settling time.

TECHNICAL APPROACH

The design effort is organized into two key thrusts (1) Using "computational control" to achieve time-optimal transient response to random switching load current profiles typical of SoCs. (2) Addressing a key weakness in digital LDOs--their prohibitive Power Supply Rejection performance--to advance the state of the art in the transient response of digital LDOs. The main approach toward Thrust 1 will be to evaluate the use of Model Predictive Control (MPC) for rapid transient response. This effort seeks to demonstrate the effectiveness, and the limits of more advanced control strategies on regulator design using test-chip demonstrations in 65-nm CMOS.

SUMMARY OF RESULTS

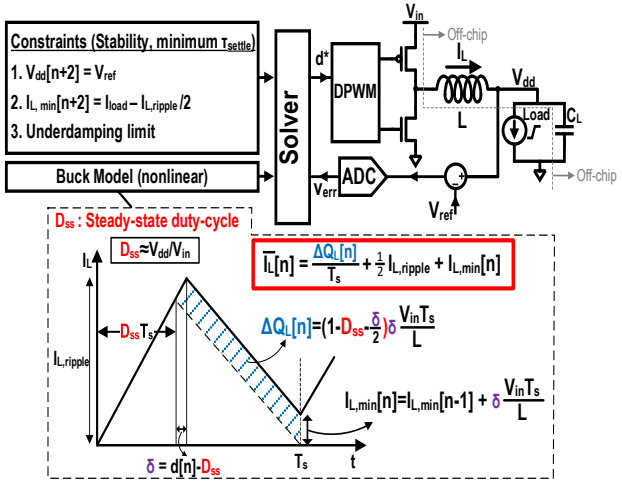

Figure 1. MPC-based buck converter control relies on a predictive model (and its periodic update using measurable state variables) to devise an optimal trajectory for the duty cycle that will achieve minimum settling time.

At this time, we have outlined an architecture for the proposed LDO and performed system simulations to verify our approach. We have also designed an initial buck-architecture (Fig. 1) that employs MPC for rapid transient response. The approach relies on accurate time-domain modeling of inductor charge delivery in a buck converter to build an accurate predictive model of the impact of duty-cycle on Inductor current and output voltage. Delay and power prohibitive run-time constrained optimization is avoided by relaxing the optimization problem to one of constraint satisfaction – settling V_{dd} droop in 2 cycles (Fig. 2).

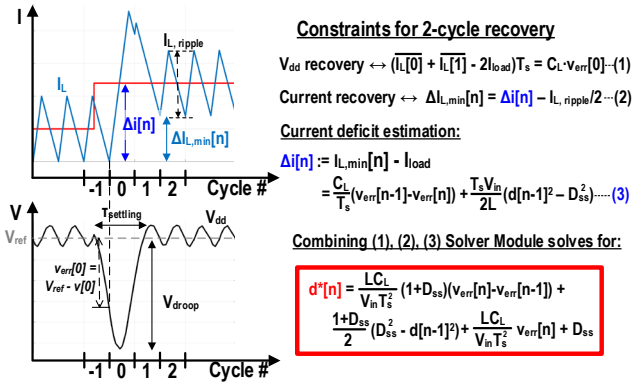

Figure 2. Simulation waveforms and computations performed by the MPC-based buck converter.

The worst-case droop scenario for a buck converter occurs in the context of duty-cycle saturation – when simple linear models for a buck converter break down. MPC works particularly effective in enabling time-optimal transient response under a random current loading scenario by effectively tracking the surplus charges that the system will deliver under duty cycle saturation conditions if the inductor current were to return to a steady-state condition.

A parallel test chip effort is also underway on Thrust 2, exploring an architecture to the PSR and transient response time challenges faced by digital LDOs.

Keywords: Model-predictive control, Voltage Regulation

INDUSTRY INTERACTIONS

Intel, NXP, ARM

MAJOR PAPERS/PATENTS

TASK 2810.039, DEVELOPMENT OF COMPACT AND LOW COST FULLY INTEGRATED DC-DC CONVERTER WITH RESONANT GATE DRIVE AND INTELLIGENT TRANSIENT RESPONSE

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SIGNIFICANCE AND OBJECTIVES

This project targets to build a compact and efficient fully integrated buck converter with substantial benefits such as low area cost, high current density, etc. Using developed techniques, we plan to show the state-of-art energy efficiency, area efficiency and intelligent transient response in a fully integrated DC-DC converters.

TECHNICAL APPROACH

This project will develop novel circuit techniques for fully integrated buck converters. At technology level, we will develop a methodology for optimal on-chip inductor design including topology, operating frequency and stacking solutions with other components. At circuit level, we will explore novel resonance based operation to reduce switching loss. At system level, we will leverage advanced machine learning or event driven operations to build an intelligient droop response module. Cross-layer optimizing these techniques, we plan to achieve state-of-art power and area efficiency with a well-developed design methodology. We will use Cadence Virtuoso for circuit design and EMX tools for electromagnetic simulation.

SUMMARY OF RESULTS

We have made initial progress towards our deliverable in the first year, which includes a methodology for on-chip inductor and capacitor design. We have experimented a few different inductor topology and explored efficiency and area tradeoff. The results are not conclusive yet. We also studied the components that contribute to the power efficiency loss in our existing fully integrated DC-DC converter.

Keywords: DC-DC converter, resonant switching, fast transient response, event based feedback control, machine learning techniques

INDUSTRY INTERACTIONS

IBM, Intel, Texas Instruments

MAJOR PAPERS/PATENTS

TASK 2810.040, HYBRID/RESONANT SC CONVERTERS WITH INTEGRATED LC RESONATOR FOR HIGH-DENSITY MONOLITHIC POWER DELIVERY

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SIGNIFICANCE AND OBJECTIVES

Fully-integrated power management is important for a variety of computing and communication applications but is difficult due to the limitations of on-chip passive components. This project explores a new direction using distributed LC-resonators in hybrid switched capacitor architectures to manage high-frequency losses and expand efficiency and power-density.

TECHNICAL APPROACH

This work involves co-optimization of high-frequency DC-DC converters based on hybrid-resonant switched capacitor architectures and distributed planar-spiral LC resonators. A variety of analytical and numerical methods is used to model skin- and proximity-effect losses in planar magnetics which use capacitive dielectrics to ballast and homogenize current density. Several circuit topologies are under study spaning nominal 2:1 resonant converters as well as higher conversion ratios using Series-Parallel and Dickson architectures. Circuit design is completed in Cadence with a tapeout expected in Q3-4 2020; electromagnetic simulation is completed in Sonnet and other tools.

SUMMARY OF RESULTS

This work builds on a related and recently published effort, [1]-[2] that first detailed the merged LC concept. The converter prototype used a 2-phase merged resonator with coupled magnetics as part of a nominal 2:1 step down resonant switched capacitor converter (Figs. 1 & 2). The design operates at ~45MHz with off-time modulation for fast voltage regulation and light-load efficiency enhancement.

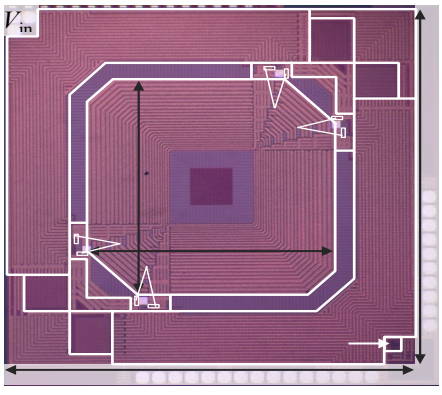

Figure 1. Merged LC resonant switched capacitor die-photo from [1]; nominal 2:1 step down with regulation @ 45 MHz.

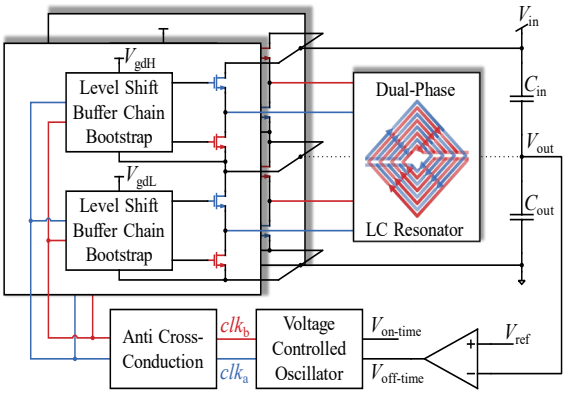

Figure 2. 2-phase coupled ReSC converter block diagram.

The use of coupled magnetics and multiphase interleaving combined with the merged resonator allowed the design, highlighted in Fig. 2, to achieve efficiency >85% at 0.47W, the highest efficiency@power for published designs with on-chip spiral magnetics.

Recently completed work includes an expansion of the modeling and simulation suite for spiral resonators including better ways to analyze, and use embedded capacitance and the full metal stackup. We are currently working on both electromagnetic simulation and Cadence IC design while exploring relevant topologies from among the switched capacitor base-class.

A next-generation design is in preparation for tapeout in Q3-4 of 2020. We are currently using a 180-nm SOI process which allows benefits including bottom plate parasitic reduction, access to high-density MIM capacitors, and switching devices capable of switching frequencies in the 10's of MHz. Next steps in circuit design activities include the design of high-speed integrated controllers and mode-switching regulation.

Keywords: Power Management, DC-DC Converters

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] P. H. McLaughlin, Z. Xia and J. T. Stauth, "11.2 A Fully Integrated Resonant Switched-Capacitor Converter with 85.5% Efficiency at 0.47W Using On-Chip Dual-Phase Merged-LC Resonator," ISSCC 2020.

[2] P.H. McLaughlin et al., "A Monolithic Resonant Switched-Capacitor Voltage Regulator with Dual-Phase Merged-LC Resonator," JSCC (invited, in review).

TASK 2810.042, DIGITALLY ENHANCED HIGH EFFICIENCY, FAST SETTLING AUGMENTED DC-DC CONVERTERS

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SIGNIFICANCE AND OBJECTIVES

State-of-the-art digital loads impose challenging requirements for power-supply regulators to provide fast-transient currents. Fast-transient response improvement techniques utilizing auxiliary circuits became pupular due to their enhanced efficiency and design-flexibility. Our goal is breaking the efficiency/dynamic-response/settling-time trade-off in conventional dc-dc converters, by developing high-speed, digitally controlled augmented power stages with optimal load current control and settling time.

TECHNICAL APPROACH

In the proposed augmented power converter topology, an auxiliary stage with a small inductor, and a high switching rate converter share the load capacitor with the main stage providing fast settling under fast-load-transients. We will develop observer-based load capacitor current estimator to control the auxiliary stage, having it work as a Current-Controlled-Current-Source. Given the specific supply-voltage regulation window, this system achieves a fully-integrated solution that requires a smaller (3~4x) external capacitor size, which is significantly compatible and adequate for low-cost mass-production. For design, characterization and validation of the proposed system, Arizon-State-University Connection-One-Research-Labs will be used, which provides all necessary CAD/EDA design softwares/tools (Matlab, Cadence/Virtuoso) and test equipments for characterization.

SUMMARY OF RESULTS

The initially planned tape-out date is beginning of May 2021. System-level design is ongoing. Different control schemes (PWM control, hysteretic control, Constant-On/Off-Time control) and control modes (voltage mode, current mode) for the main stage are being analyzed in terms of settling speed and stability. Digital nonlinear controls (single-cycle or multi-cycle correction) for the aux stage are included. VerilogAMS models are used to build the transient detector and control logics. We propose a novel fast-transient-current detection technique across the load capacitor with an arbitrary ESR as shown in Fig. 1. The timings for digital control are computed in an analog domain for high cost/energy efficiency.

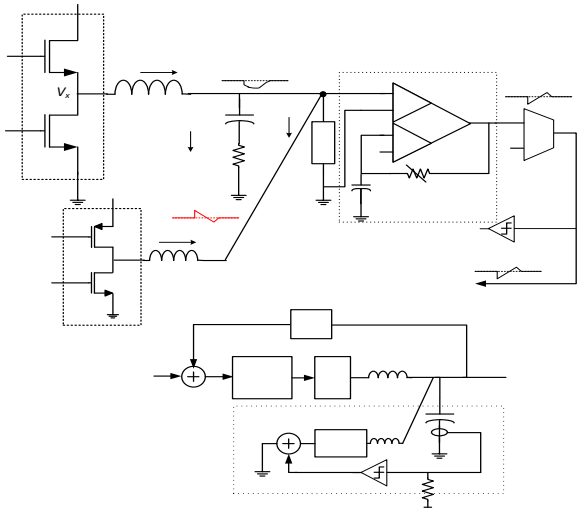

Figure 1. (a) Differential error-amplifier based load current detector (b) small-signal model of main/aux stage controller.

The target design specifications are summarized in Table1.

Table 1. Target Design Specifications of the Proposed Augmented Converter.

Parameter	Design Target
Technology node	TSMC180
Input Voltage (Vin)	5V +/-10%
Output Voltage (Vout)	0.5V – 0.8V
Switching Frequency Main Converter	500kHz
Switching Frequency Aux Converter	5-10MHz
Output Voltage Regulation Window	3-5% of Vout
Output capacitor reduction	3-4X
Main converter inductance	~1uH
Aux converter inductance	100nH~500nH
Aux converter average active current	500uA
Aux converter average standby current	150uA
Settling time	2uSecs

Keywords: augmented converter, fast transient detector, fast settling, high efficiency, digital nonlinear control

INDUSTRY INTERACTIONS

NXP, Intel

MAJOR PAPERS/PATENTS

TASK 2810.049, 1-W BATTERY-CHARGING CMOS BUCK REGULATOR

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SIGNIFICANCE AND OBJECTIVES

Charging batteries (in cell phones) with other batteries (like battery banks) is a new normal today. Volume and charge life are critical in this space. The objective of this research is to develop a small and power-efficient single-inductor voltage regulator that also charges and conditions a battery for maximum capacity (energy).

TECHNICAL APPROACH

Charging dynamics in Lithium-Ions are largely unexplored, so conventional chargers do not charge them to their highest possible levels. The first step in this research is to study, test, and develop charging methods that expand capacity. The second step is to develop an efficient power supply using one inductor that charges a battery and supplies a load. To preserve energy, power flow in all directions should be efficient: input–output, input–battery, and battery–output. The third step is to develop an efficient controller that supplies and regulates the output while charging and conditioning the battery for maximum capacity.

SUMMARY OF RESULTS

Important parameters to consider when selecting a battery are capacity, power density, cycle life, safety, and cost. Capacity is how much useful energy a battery can store. Power density is the amount of power a battery can output. Cycle life is the number of times a battery can charge and discharge fully. Safety refers to thermal stability: unlikelihood of thermal runway and gas venting.

Unfortunately, no single battery technology is the best in all respects. $LiCoO_2$, $LiNiMnCoO_2$, and $LiNiCoAlO_2$ in Table 1, for example, excel in capacity. $LiFePO_4$ is good for power and safety, but not for capacity. $LiMn_2O_4$ outputs the most power, but also cycles the least. $LiTiO_2$ can cycle the most, but also stores the least energy.

Table 1. Lithium-ion batteries.

Chemistry	Capacity [Wh/Kg]	Power [W/Kg]	Cycle Life [# Cycles]	Safety
$LiCoO_2$	150–250	740	500–1000	Low
$LiMn_2O_4$	100–150	1800	300–700	Moderate
$LiNiMnCoO_2$	150–220	1500	1200–1950	Moderate
$LiFePO_4$	90–120	1000	1000–2000	High
$LiNiCoAlO_2$	200–300	750	1000–1280	Moderate
Li_2TiO_2	50–80	–	3000–7000	Moderate

$LiNiMnCoO_2$ is popular in power tools and electronic bicycles because capacity, power density, and cycling are all important in those applications. $LiCoO_2$ is more popular in portable electronics like mobile phones, laptops, and tablets because size, energy, and cost are more constraining than power and cycling. Shrinking dimensions and increasing packing densities are largely to blame for this. Physical makeup, however, is not the only determinant factor – capacity is also sensitive to temperature and the charging process.

Chargers normally charge with low steady currents to maximize capacity. This way, more of the battery charges. The problem with this approach is long charge cycles. Pulse, ramp, sine, and super-imposed variants are unexplored methods that this research aims to study. Testing, adjusting, and evaluating measurements against a consistent constant-current baseline will reveal a method that packs the most energy into a battery.

The goal for the next year is to develop a CMOS switched inductor that can supply an output and charge a battery, like Fig. 1 shows. The key to this technology is the use of one inductor to transfer power in all directions with a high conversion efficiency. Conventional systems use two inductors or sacrifice efficiency or regulation for the sake of size.

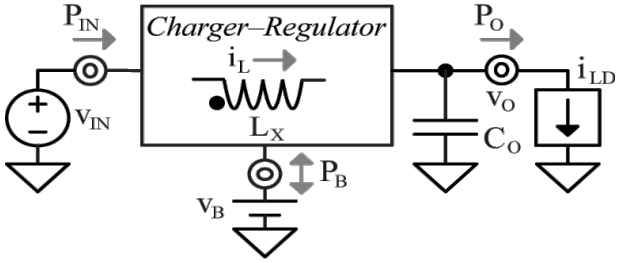


Figure 1. Battery-charging voltage regulator.

The goal for 2022 is to develop a CMOS controller for the switched inductor. The key here is to regulate the output and charge and condition a battery so capacity is at the highest possible level with the shortest possible charge time. In all, the fundamental advantages of this research will be higher capacity, higher efficiency, smaller footprint, and lower cost.

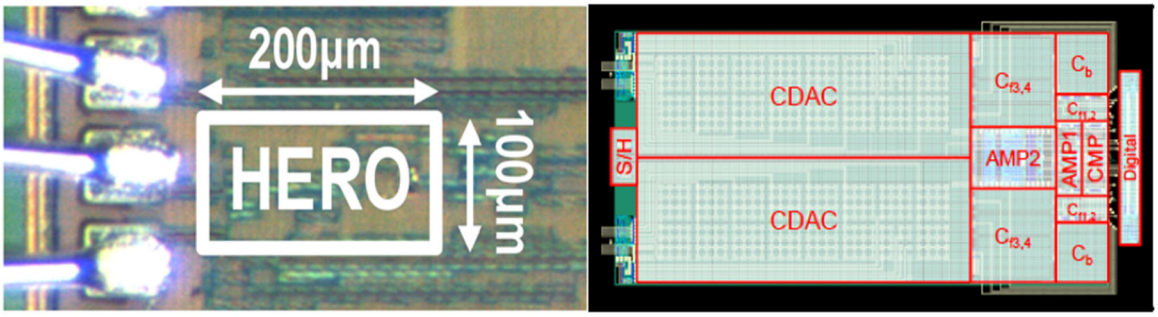
Keywords: Li-ion charger, voltage regulator, capacity

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

Fundamental Analog Thrust



Category	Accomplishment
Fundamental Analog (Circuits)	Ultra-low power crystal oscillators (XOs) are key components in wearable, IoT, and mobile applications. Using a frequency-divided high-energy-to-noise-ratio pulse injection allows the crystal to run freely for a longer time between injections, thus improving long-term frequency stability and reducing injection overheard. Fabricated in 40-nm CMOS, a prototype 32-kHz XO consumes only 0.51nW and achieves 2ppb Allan deviation, which is 5x lower compared to that achieved by state-of-the-art nW-XOs. (2810.009, D. Sylvester & D. Blaauw, U Michigan)
Fundamental Analog (Circuits)	Higher-order noise shaping in successive approximation register analog-to-digital converters (SAR ADCs) is demonstrated using a cascaded-noise-shaping (CaNS) SAR architecture. By cascading two 2^{nd}-order NS stages, a 4^{th}-order noise-transfer function is realized while consuming similar power and area to a 2^{nd}-order NS-SAR. Fabricated in 28-nm CMOS, the prototype CaNS-ADC occupying $0.02mm^2$ achieves 88dB SNDR over a 100kHz bandwidth while consuming only 120µW. (2810.033, M. Flynn, U Michigan)
Fundamental Analog (Circuits)	A 315-GHz self-synchronizing minimum shift keying (MSK) receiver outputs digital bits and is implemented using a frequency doubler in a PLL. Fabricated in a 65-nm CMOS process, the prototype receiver is used to form a 10-Gbps link with BER < 10^{-11} at an RF input power of -21-dBm without using separate frequency synchronization between the transmitter and receiver, and data equalization. The 315-GHz RF is the highest for PLL-based receivers and for MSK receivers. (2810.015, K. O, UT Dallas)

TASK 2712.005, AUTOMATED CROSS-LEVEL VALIDATION AND DEBUG OF MIXED-SIGNAL SYSTEMS IN TOP-DOWN DESIGN: FROM PRE-SILICON TO POST-SILICON

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SIGNIFICANCE AND OBJECTIVES

There are few automated tools for design debug of mixed-signal/RF circuits and systems. The goals are to develop algorithms and tools for modeling and debug of mixed-signal/RF systems. The approach combines iterative test generation and behavior learning to model and debug low level mixed-signal/RF behaviors.

TECHNICAL APPROACH

An adversarial stimulus generation vs. behavior learning algorithm is developed in which *a population of test stimuli is used to expose divergent behaviors between a high level model and its transistor level implementation while an underlying machine learner tries to minimize such divergence*. The stimuli and response data are used to train learning kernels that augment the high level behavioral model concerned in such a way as to *minimize the observed behavior divergence* until no further divergent behaviors can be exposed by stimulus generation. The end result of the procedure is an *automatically generated surrogate model of the netlist* that captures all of its input-output behaviors. A design bug diagnosis technique was also developed and demonstrated on pilot circuits.

SUMMARY OF RESULTS

The proposed approach was demonstrated on several circuits including ampliers, low dropout regulators and a PLL. Figure 1 below shows the accuracy with which hysteresis in an RF power amplifier was automatically modeled using the methodology. Figure 1 shows hysteresis measurements performed on hardware and Figure 2 shows the same extracted from automatically constructed models of device input-output behavior. High modeling accuracy is achieved. Automated diagnosis of design bugs was also demonstrated for a PLL and other circuits.

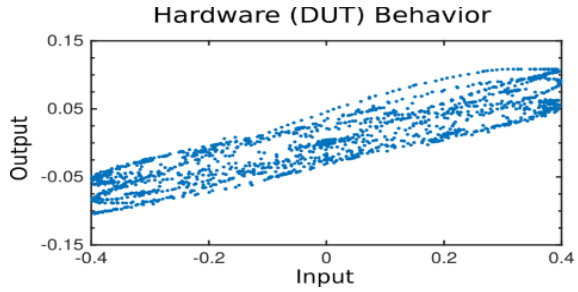

Figure 1. Hysteresis captured from hardware.

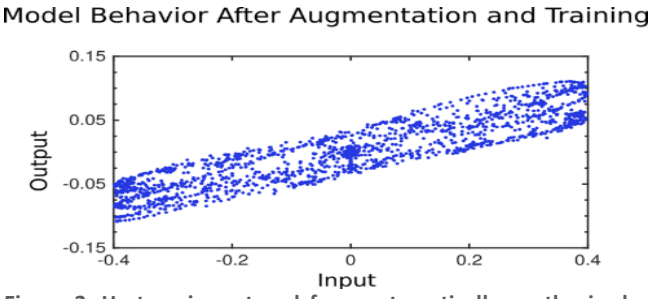

Figure 2. Hysteresis captured from automatically synthesized model.

Keywords: Design Validation, Test, Learning, Analog

INDUSTRY INTERACTIONS

Texas Instruments, Intel, NXP

MAJOR PAPERS/PATENTS

[1] B. Muldrey, S. Deyati and A. Chatterjee, "Post silicon validation: Automatic characterization of RF device nonidealities via iterative learning experiments on hardware," *VLSI Design Conference*, 2017.

[2] B. Muldrey, S. Deyati and A. Chatterjee, "DE-LOC: Design validation and debugging under limited observation and control, pre-and post-silicon for mixed-signal systems." *2016 IEEE International Test Conference (ITC)*. IEEE, 2016.

[3] B. Muldrey, S. Deyati and A. Chatterjee, "Mixed Signal Design Validation Using Reinforcement Learning Guided Stimulus Generation for Behavior Discovery." *2019 IEEE 37th VLSI Test Symposium (VTS)*. IEEE, 2019.

[4] John B. Muldrey, Algorithms for post-silicon validation and debug of RF, analog and mixed-signal circuits and systems, *Ph.D dissertation,* Georgia Institute of Technology, 2019.

TASK 2712.010, RINGAMP-ASSISTED CIRCUITS/TECHNIQUES AND NEXT-GENERATION RINGAMPS

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SIGNIFICANCE AND OBJECTIVES

Our research goal is to solidify ring amplifier as a dominant means of amplification in mixed-mode circuits through demonstration of performance improvements over traditional operational transconductance amplifiers. In this task, ring amplifier design addressing expressed interest in process-voltage-temperature stabilization techniques has been implemented and published.

TECHNICAL APPROACH

Two chips were prototyped in a 180-nm CMOS technology which demonstrated circuit design techniques for mitigation in process-voltage-temperature variation of ring amplifier-based systems. The prototypes include a low-dropout regulator and oversampling analog-to-digital converter.

SUMMARY OF RESULTS

This task builds on previous innovation in mixed-signal systems utilizing ring amplifier in two catagories. The first new innovation was an expansion of ring amplifier into other applications, namely the low-dropout regulator. Second, this task addresses member feedback on the need for tolerance to process-voltage-temperature variability.

The first prototype demonstrated the usage of ring amplifier in power regulation applications and was published at the 2019 Asian Solid-State Circuits Conference. By utilizing the ring amplifier in a continuous feedback loop, fast recovery to changing regulator load conditions can be maintained with low quiescent power consumption therefore demonstrating high-efficiency in linear regulation. The circuit schematic of the ring amplifier-based low-dropout regulator is shown in Figure 1.

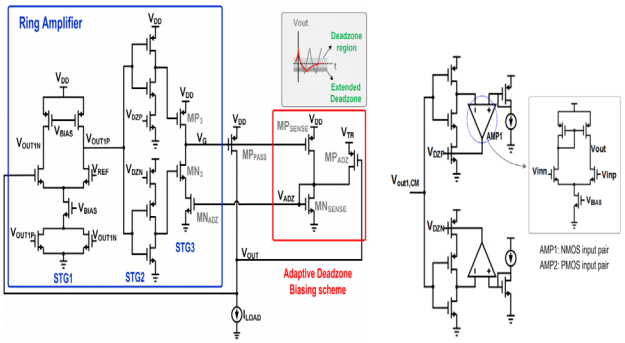

Figure 1. Architecture of ring amplifier-based low-dropout regulator with PVT regulation circuit.

PVT regulation is provided with a replica circuit and error feedback amplifiers as shown in [2]. A performance summary of the low-dropout regulator is given in Table 1.

Table 1. Low-dropout regulator performance summary.

V_{OUT}	Dropout	Max I_{Load}	Quies. Current	Settle Time	PSRR @1kHz
1.0V	90mV	80mA	6.5uA	432ns	-40dB

The second prototype demonstrated the use of ring amplifier with PVT regulation in a second-order Delta-Sigma modulator ADC. This project is still ongoing with performance enhancements expected in future results.

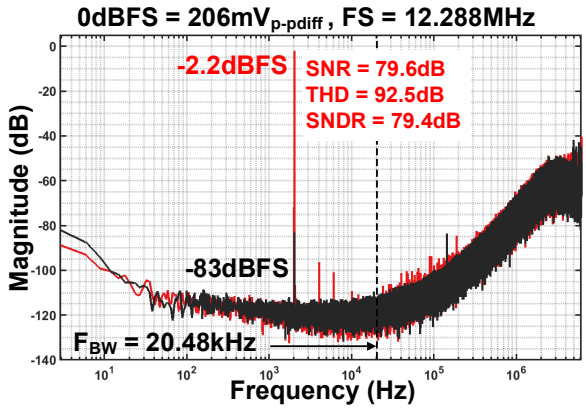

Figure 2. Dynamic performance of the second-order Delta-Sigma modulator ADC.

Keywords: analog-to-digital converter, low-dropout regulator, ring amplifier, process-voltage-temperature

INDUSTRY INTERACTIONS

Texas Instruments, NXP, Intel

MAJOR PAPERS/PATENTS

[1] B. Xiao *et al.*, "An 80mA capacitor-less LDO with 6.5uA quiescent current and no frequency compensation using adaptive-deadzone ring amplifier," *IEEE Asian Solid-State Circuits Conference (ASSCC)*, Nov. 2019.

[2] P. Venkatachala *et al.*, "Process invariant biasing of ring amplifiers using deadzone regulation circuit," *IEEE Int. Symp. on Circuits and Systems (ISCAS)*, May 2018.

TASK 2712.011, ROBUST RELIABLE AND PRACTICAL HIGH PERFORMANCE REFERENCES IN ADVANCED TECHNOLOGIES

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SIGNIFICANCE AND OBJECTIVES

Objective is to develop circuits that express the bandgap voltage at the output with a single electrical trim at standard test temperature and to adapt all-electrical trim to an on-demand run-time trim without requiring external test equipment. Significance is in development of references with lower temperature dependence.

TECHNICAL APPROACH

Our approach to the first objective is to revisit the issue of expressing the bandgap voltage at the output of a circuit directly rather than focusing on expressing the bandgap voltage only at an inflection temperature. Our approach to meet the second objective will be to identify what additional information can be obtained from correlated reconfiguration of a circuit in which the bandgap voltage and temperature are tightly intertwined in the device characteristics and design variables. Two test chips will be designed to obtain experimental verification of the performance of the new precision reference circuits.

SUMMARY OF RESULTS

Two new bandgap reference circuits have been developed that ideally express the bandgap voltage at the output. In contrast to existing approaches that provide curvature correction to partially correct for a nonlinear TlnT term that has been a nemesis for bandgap references for over 3 decades, these two new circuits are designed to eliminate the nonlinear TlnT term. These may be the first two circuits that actually express the bandgap voltage of silicon at the output.

One is based upon a dc current bootstrapping approach and the second is based upon a dc voltage bootstrapping approach. A patent was obtained for the current bootstrapping approach.

The current bootstrapping circuit was fabricated in a 130-nm CMOS process. A Fluke Microbath Thermometer Calibrator was used to make measurements. Initial measured results were disappointing with the temperature dependence of the offset voltage of the operational amplifiers and the limited digital trim range limiting performance. The measured TC over an 80°C window was 14 ppm/°C. Though performance with this approach to the sub 1 ppm/°C range should be achievable, resources for refabricating and retesting were not available so emphasis has been placed upon the voltage bootstrapping approach which should offer comparable performance.

The voltage bandgap expression circuit using a voltage bootstrap is shown in Fig. 1. The performance limitatins are believed to be dominantly associated with the diode-connected substrate pnp transistors so only this part of the reference was fabricated in a 65-nm CMOS process to allow clear experimental delineation between limitations associated with the pnp devices and the remaining components that can be readily added by experienced designers with the required level of performance. Layout of the pnp transistor array is shown in Fig. 2. Experimental results with 2 temp trim show 1.8 ppm/°C over 90°C range. A new test board with increased trim resolution has been fabricated; tests are ongoing. Sumulations suggest this should have sub 1ppm/°C performance.

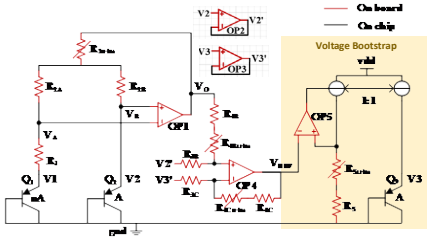

Figure 1. Current Bootstrapped Bandgap Extractor Reference.

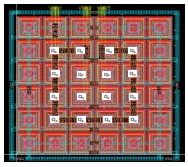

Figure 2. Voltage Bootstrapped Bandgap Extractor Reference.

Keywords: bandgap reference, diode model, curvature-compensation, voltage reference, bandgap separator

INDUSTRY INTERACTIONS

Texas Instruments, Intel, NXP

MAJOR PAPERS/PATENTS

[1] D. Chen and Z.Liu, US Pat. 10,359,801 "Voltage reference generator with linear and non-linear temperature dependency elimination," July 23, 2019.
[2] N. Liu, R.L. Geiger, and D. Chen, "Bandgap Voltage V_{GO} Extraction with Two-temperature trimming for designing Sub-ppm°/C Voltage References," ISCAS, May 2019.

TASK 2712.14, LEVERAGING CMOS SCALING IN HIGH PERFORMANCE ADCS

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SIGNIFICANCE AND OBJECTIVES

We have continued our efforts in debugging and optimizing the silicon measurement results. The final revisions of the designs have been sent out for fabrication. We will update our measurement results when we receive the prototypes.

TECHNICAL APPROACH

The goal is to leverage properties of scaled CMOS to improve the performance of ADCs. In this effort, we have proposed three gerenal solutions (1) Correlated Dual Loop (CDL) Delta-Sigma: A new variation on Sturdy-MASH modulators, which has been widely used. This new structure will eliminate the need for quantizer error extraction which is a critical limiting factor in continuous-time multi-loop delta-sigma ADCs. (2) Digital Correlated Level Shifting (D-CLS): targeting pipelined ADCs, this technique leverages the traditional CLS but removes the loading from the opamp and shifts it to digital domain by quantizing the next stage early. (3) 3-Step Quantizer: using time/phase frequency to quantize the signal in delta-sigma ADCs .

SUMMARY OF RESULTS

The two highlighted prototypes are shown in Fig. 1 (Digital Corelated Level Shifting) and Fig. 2 (CDL SMASH). The D-CLS pipelined ADC enhances the effective loop gain of the MDAC by the number of bits resolved in that stage. Unfortunately, due to a problem in the comparactor of the flash ADC, it was unstable to verify the full operation of the fabricated prototype. We have debugged and the updated prototype has been submitted for fabrication.

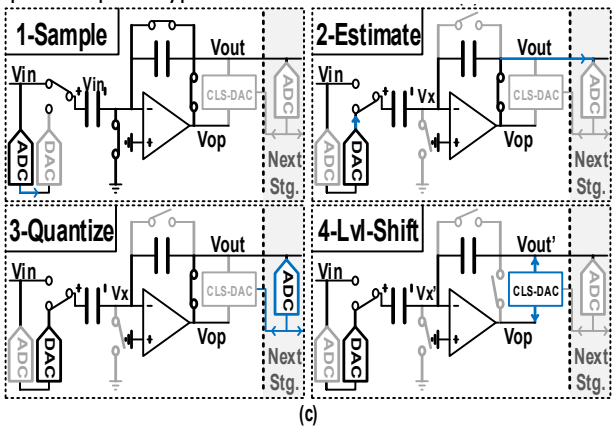

Figure 1. The proposed Digital CLS and its timing diagram.

The other prototype is targeted on CT Delta-Sigma ADC and uses a new form of Sturdy-MASH modualtors that eliminates the need for quantization error extraction. The fabricated prototype measurements in Fig. 2 show promise, however the noise floor was 12dB higher than the anticipated. After detailed post-layout simulation, we realized the the parasitics associated with the virtual ground of the first integrator couples with the DAC references which increased noise. We have fixed this issue and submitted the new design for fabrication. The last prototype including 3-step NSIQ is ready for testing.

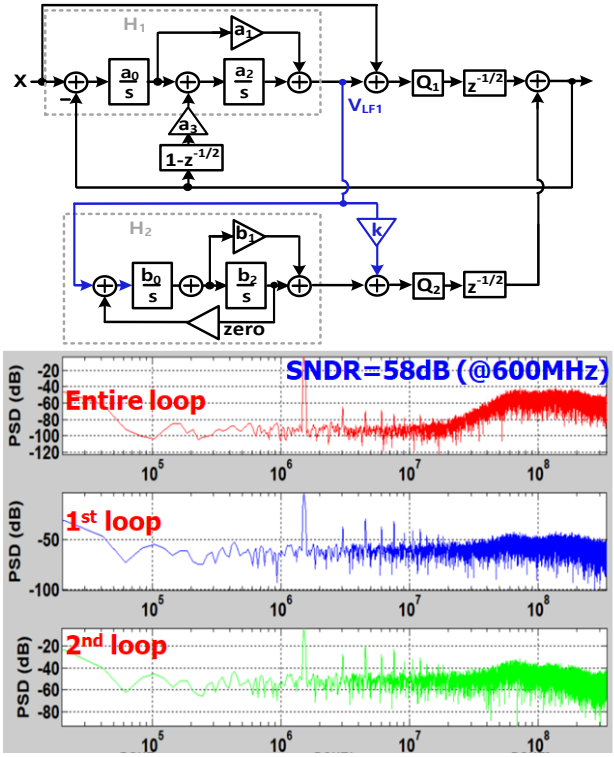

Figure 2. Architecture level of the under fabrication prototype CDL Delta-Sigma ADC.

Keywords: Quantization, Delta-Sigma, ADC, Pipelined

INDUSTRY INTERACTIONS

Texas Instruments, NXP, Intel

MAJOR PAPERS/PATENTS

TASK 2712.025, REDUCTION OF LOW FREQUENCY NOISE IMPACT IN NANO-SCALE CMOS CIRCUITS

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SIGNIFICANCE AND OBJECTIVES

This project is investigating approaches to incorporate an on-chip measurement capability and post-fabrication configurable minimum size transistor arrays to reduce the low frequency noise impact in RF and analog circuits. This approach may be more effective for reducing low frequency noise impact than increasing the transistor size.

TECHNICAL APPROACH

Using transistors with lower noise through post fabrication selection, and approaches for integrating a highly sensitive noise measurement circuit based on a frequency synthesizer commonly found in RF and millimeter wave transmitter and receiver will be investigated. Intelligent search algorithms will be applied to select the combinations with low frequency noise with the minimum number of measurements. Approaches to increase the operating frequency of VCO and the factors that limit the maximum operating frequency are being investigated. Lastly, feasibility to extend this technique to other circuits is being investigated.

SUMMARY OF RESULTS

The number of intended dopants and un-intended defects in a minimum sized device is reduced with technology scaling. One missing dopant or having an additional defect can dramatically increase or decrease the threshold voltage, current and noise. A 4.3-GHz voltage controlled oscillator (VCO) that embraces the variability of nano-scale transistors to reduce its phase noise by taking advantage of reduced low frequency noise of some minimum sized transistors with a fewer defects or traps through post-fabrication selection is reported [1].

The VCO fabricated in 65-nm CMOS (Fig. 1) uses a digitally addressable array of cross-coupled minimum-size NMOS transistor pairs for post-fabrication selection. An algorithm based on Hamming distance using the measurements of ~1,500 combinations was used to identify the combinations with the record phase noise of -130dBc/Hz at 1-MHz offset from a 4.3-GHz carrier.

To make this technique practical, an affordable and sufficiently rapid on-chip measurement technique for the phase noise that can resolve noise below -130dBc/Hz for a 4.3-GHz carrier is being researched. Fig. 1 also shows a phase locked loop (PLL) including the components for phase-noise measurements. Fig. 2 shows an automated set-up to measure the phase noise of VCO and PLL. Using this set-up, the algorithms for identification of low noise combinations are being imporved. An updated version of the PLL in 65-nm CMOS that has reduced phase noise and requires an ADC with a reduced dynamic range has been fabricated. Additionally, a down conversion mixer using this technique has been fabricated and being characterized. Applicablilty of this technique to other circuit elements as well as to that operating at higher frequencies are being investigated.

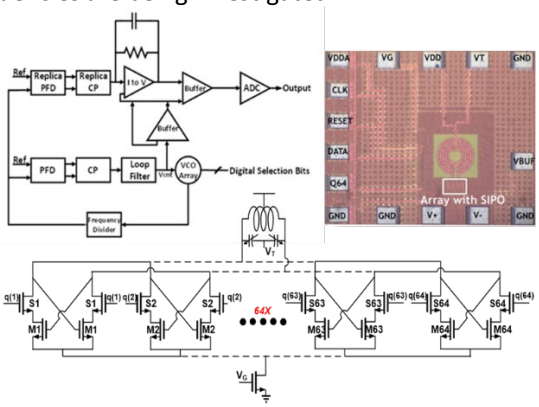

Figure 1. PLL incorporating a 4.3-GHz VCO (Top Right and Bottom) using an array of cross-coupled NMOS transistors and components for on-chip phase noise measurements.

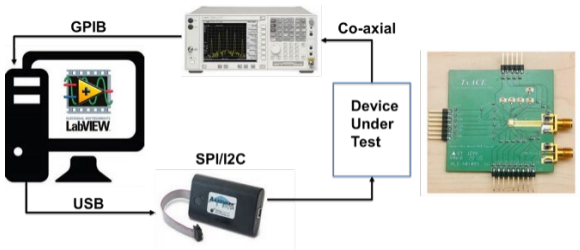

Figure 2. Automated set up for phase-noise measurements.

Keywords: low frequency noise, on-chip noise measurements, post-fabrication selection

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] A. Jha, et al., "-197dBc/Hz FOM 4.3-GHz VCO Using an Addressable Array of Minimum-Sized NMOS Cross-Coupled Transistor Pairs in 65-nm CMOS," *IEEE Symposium on VLSI Circuits*, pp. 214-215, June 2016, Honolulu, Hi.

TASK 2712.031,ADAPTIVE TRIMMING AND TESTING OF ANALOG/RF INTEGRATED CIRCUITS (ICs)

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SIGNIFICANCE AND OBJECTIVES

As part of the post-fabrication process, the optimum operating voltage (V_{min}) is searched in order to reduce the power consumption of each device. The device under study has four V_{min} values. The goal is to adaptively identify the V_{min} of one speed by taking advantage of the inter-V_{min} correlation.

TECHNICAL APPROACH

We propose an adaptive solution using machine learning by using the correlation between the four different V_{min} values. We experimented with the prediction of search seed for linear speed at the wafer and die-level. For the wafer-level solution, the features included V_{min} of only one of the speed to predict V_{min} of another speed. The same was repeated for other speeds too. For the die-level solution, the features included for the adaptive solution are e-tests, multiprobe measurements and V_{min} of one speed to predict V_{min} of another speed.

SUMMARY OF RESULTS

An industrial dataset of more than 700 wafers with more than 500 devices was provided by Texas Instruments Inc. The experiments seek to identify the cost savings and power consumption overhead for the linear search. This includes only the adjustment of the starting search seed (L1P) as well as both the adjustment of starting seed and highest possible search limit (L2P). From Fig. 1, we can observe that at a power consumption overhead of 7%, an overall test cost savings of 60% is achieved.

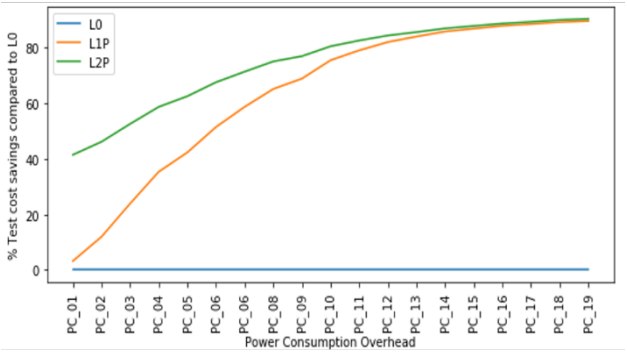

Figure 1. Wafer-level V_{min} Search Savings Compared to Current Approach L0.

For the L2P approach, where we predict the starting seed and the highest search limit shows a test cost savings of approximately 70% at a power consumption overhead of 6%.

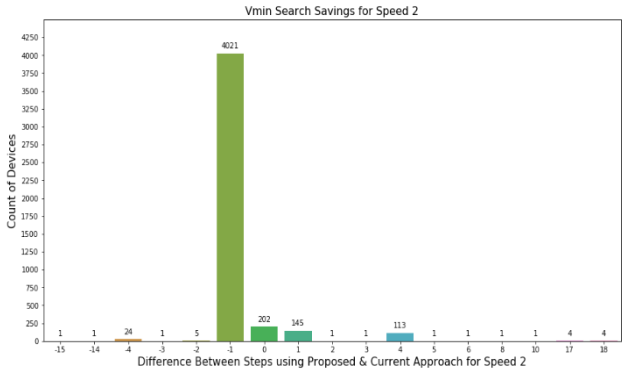

Figure 2. Die-Level Search Savings for Speed 2.

For the die-level approach, we only performed the adjustement for starting seed (L1P) experiment. We make use of the e-tests, multiprobe test measurements and V_{min} value corresponding to one speed level of the device to predict the starting point of the V_{min} search for another speed level associated with the device.

Figure 2 shows the count of devices by the difference between steps taken to reach desired V_{min} for Speed 2 using the proposed and current approach. Out of 4527 devices under test, 4053 devices achieved savings, 202 devices took the same amount of steps as the proposed approach and 272 devices needed more steps using the proposed approach compared to the compared approach. Overall, 3388 steps were saved compared to the current approach for the test set of devices. The same experiment was repeated for the remaining two speeds as well.

From the results, we were able to observe that there is still a room for improvement in achieving cost savings. We are currently exploring to see if additional die-level measurements can be used to achieve more savings.

Keywords: adaptive test, post-silicon calibration, machine learning, trimming

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] D. Neethirajan, C. Xanthopoulos, S. Boddikurapati, A. Nahar and Y. Makris, “Wafer-Level & Die-Level Adaptive Vmin Calibration Seed Forecasting using Inter-Vmin Correlation,” (IEEE T-CAD Journal In preparation).

TASK 2712.032, HIERARCHICAL ANALOG AND MIXED-SIGNAL VERIFICATION USING HYBRID FORMAL AND MACHINE LEARNING TECHNIQUES

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SIGNIFICANCE AND OBJECTIVES

Finding extremely-rare failures of a given analog/mixed-signal (AMS) design has been a long-lasting challenge. We propose to leverage the machine learning power of Bayesian optimization (BO) to address the challenging problem of verifying AMS circuits with stringent low failure requirements.

TECHNICAL APPROACH

While providing an attractive black-box solution applicable to AMS verification, a well-known limitation of Bayesian optimization (BO) is its limitation in dealing with high-dimensional problems. When the dimensionality of the black-box optimization problem increases, so does the dimensionality of the optimization of the acquisition function, which is typically non-convex, at each sequential sampling step. Solving high-dimensional optimization problems can be both computationally expensive and hard. The high run-time cost and degradation of optimization solution quality for high-dimensional problems severely limit the scalability of BO. We propose to employ random embedding to effectively reduce the effective dimensionality of the verification problem, as shown in Figure 1 [1].

SUMMARY OF RESULTS

This work aims to extend the applicability of BO to the challenging problem of rare failure detection of AMS circuits with large numbers of design uncertainties. Dimensionality reduction is possible for AMS circuits since under many practical situations variational parameters of a circuit do not have equal significance to a given design performance to be verified. Specific circuit topologies employed in practical circuits build constrained structures into the way different circuit/process parameters influence the given design performance. This gives rise to parameters that are statistically insignificant.

Random embedding provides a systematic way to explore hidden parametric redundancy. As such, parameter redundancy needs not to be specified by the designer a prior, which is very hard in general. Instead, it can be streamlined in the sequential statistical learning/black-box optimization framework of Bayesian optimization as shown in Figure 1. Our BO approach is further supported by a proposed random embedding dimension selection algorithm that estimates the effective dimension of a given AMS circuit using a small amount of training (simulation) data prior to the BO-based failure discovery process.

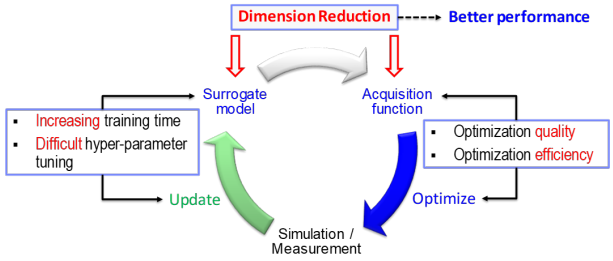

Figure 1. BO-based verification with dimension reduction.

Table 1 demonstrates the success of the proposed approach on detecting rare design failures w.r.t the quiescent current of an LDO under 60 process parameter variations which are completely missed by competitive smart sampling and BO techniques without dimension reduction.

Table 1. Failure detection of an LDO of 60 parameters. MC: Monte Carlo Sampling; SSS: scaled-sigma sampling; EI/PI/LCB: standard BO with the respective acquisition function; pBO: BO with multiple acquisition functions; HDBO: proposed BO approach. The number of simulations runs for finding the first failure and the worst quiescent current found are reported.

Method	# Sim Runs	Worst Case	1st Fail	Runtime
MC	649,000	11.6mA	-	160h25m12s
SSS	6,000	8.2mA	-	1h38m41s
EI	$50_{init}+350_{seq}$	7.0mA	-	6h46m13s
PI	$50_{init}+350_{seq}$	7.2mA	-	6h00m23s
LCB	$50_{init}+350_{seq}$	8.0mA	-	6h33m42s
pBO	$50_{init}+5*70_{batch}$	7.0mA	-	8h03m19s
HDBO	$50_{init}+5*50_{batch}$	12.7mA	231	1h57m05s (serial execution)

Keywords: Analog and mixed-signal, Verification, Formal Verification, Machine Learning, Dimension Reduction

INDUSTRY INTERACTIONS

TI, IBM, NXP

MAJOR PAPERS/PATENTS

[1] H. Hu et al., "Enabling High-Dimensional Bayesian Optimization for Efficient Failure Detection of Analog and Mixed-Signal Circui," IEEE/ACM DAC, June, 2019.

TASK 2810.005, CIRCUIT DESIGN FOR ESD AND SUPPLY NOISE MITIGATION

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SIGNIFICANCE AND OBJECTIVES

This project seeks to develop (1) IC-level power distribution networks that promote power integrity even in the presence of power-on ESD, and (2) understand and mitigate latch-up that occurs in response to power-on ESD.

TECHNICAL APPROACH

This work identifies ESD-induced reliability hazards, including latch-up, and evaluates solutions. There is a special emphasis on power-on ESD, such as that resulting from system-level discharges. Laboratory characterization of custom-designed test chips is the primary method used to investigate reliability hazards and evaluate proposed solutions. Some of the failures addressed in this work result from supply noise and an effort is made to accurately measure the on-chip noise; board-level measurements are generally unsuitable since the test chips are assembled in wire bonded packages and the package inductance decouples the noise signals at the board and chip levels. Therefore, the researchers develop and deploy on-chip noise sensors. Measurement results are interpreted with the aid of circuit simulation and electromagnetic (FDTD and FEM) simulation.

SUMMARY OF RESULTS

On the basis of test chip measurements and circuit simulation, we completed the analysis of system-level ESD-induced supply noise for ICs. The integrity of the power supply for the core logic circuits can be maintained by separating the ground nets of the IO and the core logic supplies or by eliminating the board-level decoupling capacitance on an internally-regulated core power supply. It must be noted that complete isolation of the various on-chip ground nets is not permitted due to component-level ESD requirements. ESD-induced soft errors in a microcontroller (MCU) were investigated [1]. A previously undocumented cause of latch-up in circuits with reverse body bias capability was identified. The latch-up is triggered by power-on ESD and the root cause is an induced forward-bias on the source-body diodes of the NMOS transistors. The forward-bias arises because the ESD current induces potential differences across the body bias net and, thanks to the RBB scheme, the source bias does not track those variations. It was demonstrated that circuit simulation may be used to assess the latch-up susceptibility of a given design (Fig. 1). In simulation and analysis, we have demonstrated that ESD protection circuits intended for system-level protection (i.e., power-on ESD) can reduce the amplitude of simultaneous switching noise (SSN) by several hundred millivolts. The test chip designed to validate the analysis is fully functional; however, precise measurement of the SSN has not yet been achieved due to extremely large current transients associated with the SSN induced noise on the PCB power nets. The PCB design is being re-executed with the aid of electromagnetic simulation.

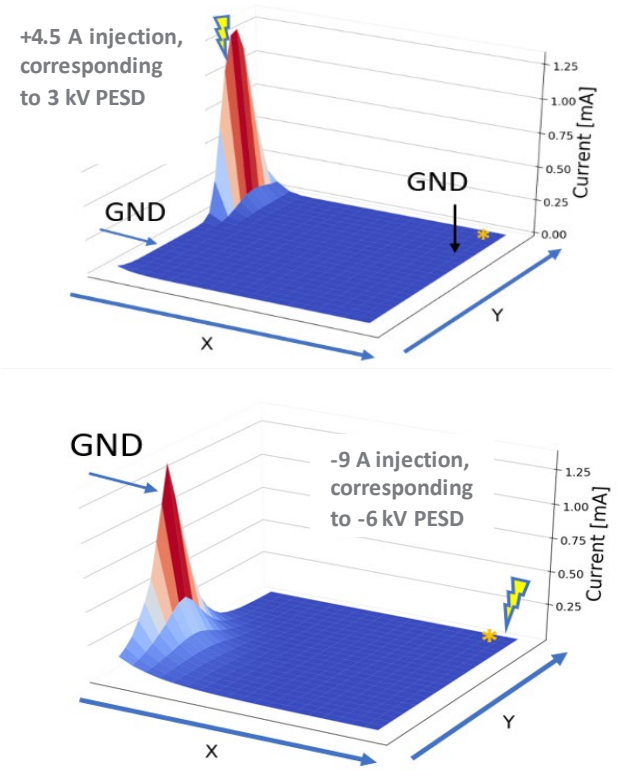

Figure 1. Circuit simulation of MCU with RBB. Current in the NMOS body diodes is plotted (base current for parasitic PNPN). PMC is located near the asterisk. Emission microscopy reveals that the simulation correctly predicts where latch-up occurs.

Keywords: ESD, latch-up, integrated voltage regulator, simultaneous switching noise, rail clamp

INDUSTRY INTERACTIONS

Texas Instruments, NXP, Intel

MAJOR PAPERS/PATENTS

[1] S. Vora and E. Rosenbaum, "Analysis of system-level ESD-induced soft failures in a CMOS microcontroller," *IEEE Transactions on Electromagnetic Compatability*, Early Access, doi: 10.1109/TEMC.2020.2986971.

TASK 2810.007, FULLY INTEGRATED PHASE NOISE CANCELLATION TECHNIQUES

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SIGNIFICANCE AND OBJECTIVES

This research will explore new architectures for frequency multiplication to reduce power consumption and to reduce phase noise. The frequency multipliers are compact, friendly to digital scaling, but suffer from high spurs and phase noise. To correct for these, a fully integrated digital phase noise calibration and a spur suppression are also realized and co-designed with the analog circuitry.

TECHNICAL APPROACH

In the previous reporting period, we proposed a low-jitter clock multiplier that is insensitive to frequency drift, and a digital spur calibration technique that effectively suppress the spurs, as shown in Fig. 1. In this period we have a further improved version, one that achieves lower power and supports a generalized multiplication ratio.

SUMMARY OF RESULTS

Fig. 1 shows a measured prototype in 28-nm CMOS demonstrating the validity of the proposed technique.

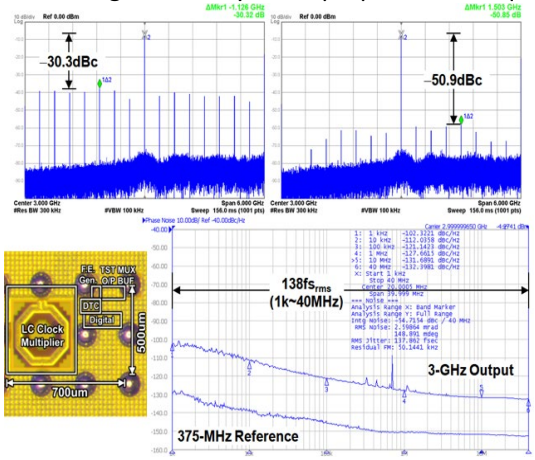

Figure 1. The architecture for the proposed clock multiplier, and the measurement results.

The intrinsic 3-GHz output clock contains substantial spurs at the offset of harmonics of 375-MHz with the highest spur level of -30.3dBc. After applying the calibration, the spurs can be suppressed considerably down to -50.9dBc. With the DTC modulated by calibrated coefficients, the 3-GHz output presents a phase noise of -127.7dBc/Hz at 1-MHz offset and the integrated jitter of 138fsrms (from 1k to 40MHz) that achieves a -249.1dB FoM with only 6.5mW.

In the 2nd version, we further improve the clock multiplier as follows:

1. Power Reduction:
   We can eliminate the spur-correcting DTC by direct-frequency-modulation of the LC tank. The power can be reduced from 6.5mW to 2.9mW, improvomg the FoM by 3dB (−249→ −252dB)
2. N-extension:
   In the previous designs, since the oscillation can sustain only for ~Q cycles between each injection pulse, the multiplication ratio (N) is low. In the 2nd version, we can have arbitray N by introducing feedback pulses to replenish the tank energy.
3. Fractional-N:
   We can achieve a fractional ratio by inserting a DTC between the refrence and the input of the multiplier. Controlled by the delay moudulator, the DTC can compensate the fractional q-noise. An LMS correlator is used to elstamate the gain for q-noise compensation.

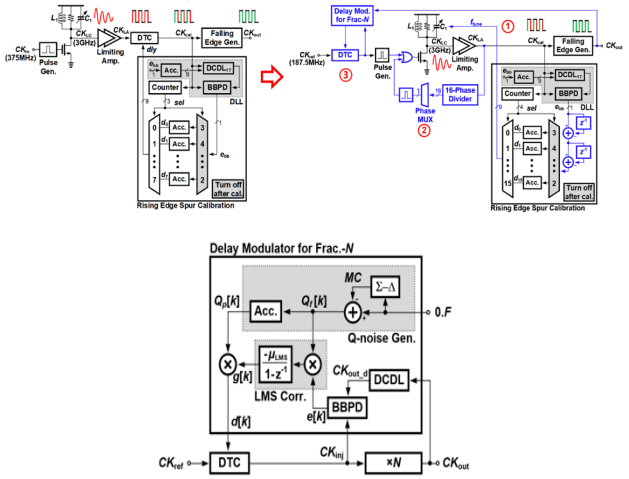

Figure 2. Top: 3 major improved for the 2nd version. Bottom: the delay modulator for fractional -N.

Keywords: Spur cancellation, injection-locked clock multiplier, clock multiplier, digital spur suppression

INDUSTRY INTERACTIONS

Intel

MAJOR PAPERS/PATENTS

[1] Y. Li et al., "A 138 fsrms-Integrated-Jitter and −249dB-FoM Clock Multiplier with −51dBc Spur Using A Digital Spur Calibration Technique in 28-nm CMOS," *Symposia on VLSI Technology and Circuits (VLSI)*, June 2019.

TASK 2810.009, MIXED-SIGNAL BUILDING BLOCKS FOR ULTRA-LOW POWER WIRELESS SENSOR NODES

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DAVID BLAAUW, UNIVERSITY OF MICHIGAN

SIGNIFICANCE AND OBJECTIVES

This project develops novel and state-of-art ultra-low power mixed-signal circuits, suitable for IoT systems. This includes timekeeping circuits, amplifiers, and CMOS-based sensors.

TECHNICAL APPROACH

The most challenging ultra-low power circuit components are mixed-signal circuits such as timers, clock sources, sensing and interface circuits (e.g., temperature sensors and low-noise amplifiers). Some of these cannot be duty cycled (e.g., timers), while others require both low noise and low power (e.g., amplifiers), which are traditionally mutually exclusive. This work proposes new ULP designs for: 1) crystal oscillator based real time clocks (RTCs), 2) temperature-compensated wakeup timers, 3) temperature sensors, and 4) front-end low-noise amplifiers.

SUMMARY OF RESULTS

We proposed a 32-kHz crystal oscillator (XO) with high energy-to-noise-ratio pulse injection. The design techniques we propose are: (1) NMOS-only pulsed driver; (2) frequency-divided (4kHz), high energy-to-noise-ratio pulse injections at peaks and valleys of the XO waveform; (3) a current reference with switched-capacitor resistance and ultra-low leakage switches to provide precise current in PVT variations; (4) a T/4-delay clock slicer to both convert the sinewave XO waveform to square wave and generate delay for timing of the energy injection. Fig. 1 shows the architecture of the proposed 32-kHz crystal oscillator.

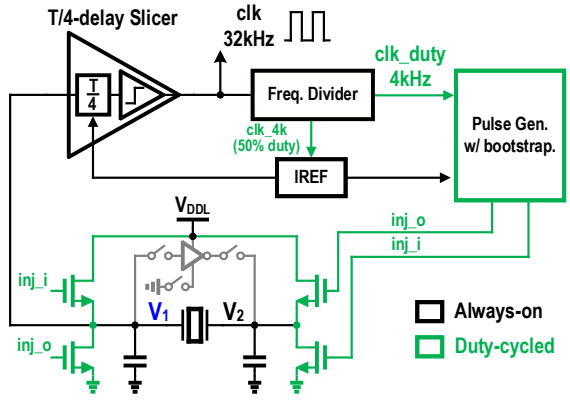

Figure 1. The architecture of the proposed crystal oscillator.

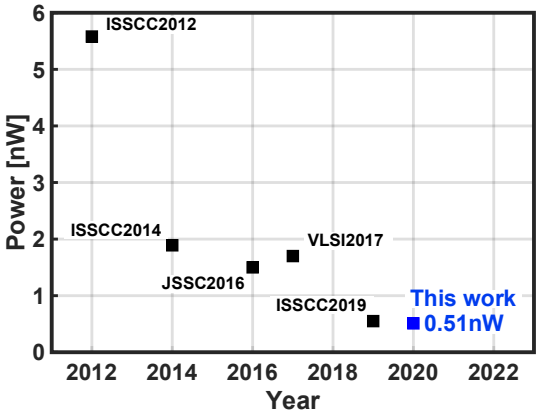

Figure 2. Power consumptions of nW XOs.

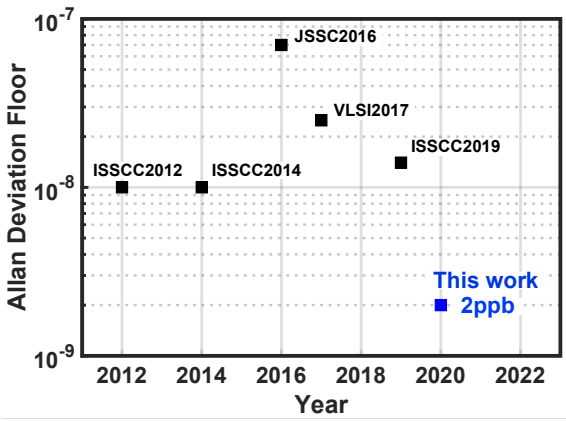

Figure 3. Allan deviation floor of nW XOs.

The proposed XO was fabricated in a 40-nm CMOS process and the layout area including the startup circuit is 0.02 mm^2. With two power supplies, 0.45V and 0.15V, ECS-2X6-FLX crystal, and a 135-mV oscillation amplitude across the crystal, the measured power consumption is 0.51nW at 25°C, which is the lowest among the reported 32-kHz crystal oscillators.

Keywords: CMOS, crystal oscillator, ultra-low power

INDUSTRY INTERACTIONS

NXP

MAJOR PAPERS/PATENTS

[1] L. Xu et al., "3.3 A 0.51nW 32kHz Crystal Oscillator Achieving 2ppb Allan Deviation Floor Using High-Energy-to-Noise-Ratio Pulse Injection," 2020 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2020, pp. 62-64.

TASK 2810.013, FREQUENCY-DOMAIN ADC-BASED SERIAL LINK RECEIVER ARCHITECTURES FOR 100+GB/S SERIAL LINKS

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SEBASTIAN HOYOS, TEXAS A&M UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

Clock jitter places fundamental performance limitations on common time-interleaved ADC architectures, necessitating clock generation and distribution circuitry that achieves rms jitter of a few hundred femtoseconds. The ADC-based high-speed serial link design techniques in this proposal aim to significantly improve jitter robustness and reduce ADC resolution and digital equalization complexity.

TECHNICAL APPROACH

A new configurable frequency-domain ADC-based receiver serial link architecture is in development that is capable of providing jitter robustness for baseband and coherent multi-tone modulation applications. The receiver utilizes ADCs with novel techniques to improve the configurable SAR sub-ADC speed and efficiency, including a design that utilizes reference pre-emphasis to enhance DAC settling and low-overhead reconfiguration logic to enable per-channel operation with a scalable resolution. Efficient digital reconstruction, equalization, and inter-channel interference filters for symbol detection are also in development.

SUMMARY OF RESULTS

Fig. 1 shows the proposed frequency-domain ADC-based receiver [1]. The input CTLE drives the front-end channels that have a mixer for down-conversion, a Bessel low-pass filter, and an ADC for sampling and digitization. These digitized samples are then processed by the FIR filters in the DSP and their outputs are combined to either perform symbol estimation in PAM-4 baseband mode or to perform both inter-channel interference (ICI) and ISI cancellation in multi-tone mode. This architecture

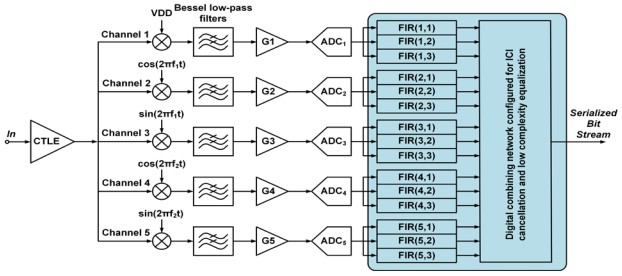

Figure 1. Configurable frequency-domain ADC-based receiver.

provides several benefits. First, the mixers perform self-equalization and provide some channel loss compensation, allowing for a reduction in digital equalization complexity. Second, high-frequency noise introduced by the mixers and CTLE is attenuated by the channel filters. Finally, the inclusion of digital receive-side ICI cancellation filters in the proposed 128Gb/s system allows for a 50% improvement in relative channel spacing when compared against a previous 10Gb/s mixed-signal implementation.

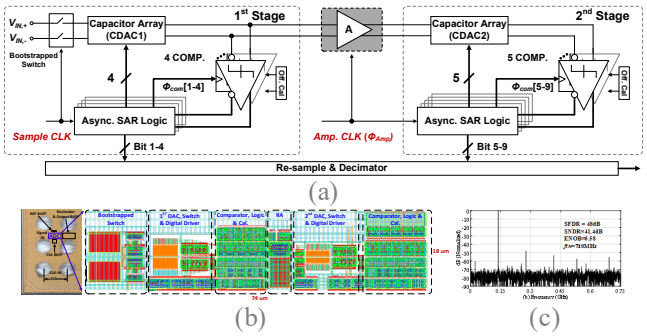

Figure 2. 1.5GS/s pipelined-SAR ADC: (a) block diagram, (b) prototype chip micrograph, and (c) measured output DFT with Nyquist input (Decimated by 18, 4096 FFT points).

The unit ADCs for the proposed frequency-domain ADC-based receiver are shown in Fig. 2 [2]. A single channel 1.5GS/s pipelined-SAR ADC utilizes a novel output level shifting (OLS) settling technique to reduce the power and enable low-voltage operation of the dynamic residue amplifier. Employing the OLS technique allows for an inter-stage gain of ~4 from the dynamic residue amplifier with a settling time that is only 28% of a conventional CML amplifier. Fabricated in a 14-nm FinFET technology, the ADC occupies 0.0013mm^2 core area and operates with a 0.8-V supply. 6.6-bit ENOB is achieved at Nyquist while consuming 2.4mW, resulting in an FOM of 16.7fJ/conv.-step.

Keywords: Analog-to-digital converter, frequency-interleaving, jitter, receiver, serial link

INDUSTRY INTERACTIONS

Intel, Texas Instruments

MAJOR PAPERS/PATENTS

[1] J. C. Gomez Diaz et al., "Jitter-Robust Multicarrier ADC-Based Serial Link Receiver Architecture," (Invited) 2019 MWSCAS, August, 2019, Dallas, TX.

[2] Y. Zhu et al., "A 1.5GS/s 8b Pipelined-SAR ADC with Output Level Shifting Settling Technique in 14nm," 2020 CICC, March, 2020, Virtual.

TASK 2810.015, DEMONSTRATION OF 120-GBPS DIELECTRIC WAVEGUIDE COMMUNICATION USING FREQUENCY DIVISION MULTIPLEXING AND POLARIZATION DIVISION MULTIPLEXING

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SIGNIFICANCE AND OBJECTIVES

This project in collaboration with the efforts on transitions and multiplexer/demultiplexer, and on low loss dielectric waveguides for operation at 100-400 GHz seeks to demonstrate 120-Gbps Polarization Division Multilexing and Frequency Division Multiplexing (45-GHz bands around 180 and 315 GHz) communication over a 1-m long dielectric waveguide using CMOS circuits.

TECHNICAL APPROACH

To excite waves at two different frequency bands with two different polarizations in a dielectric waveguide, transmitters for the 180 and 315-GHz bands will be used to drive a cross dipole. The receivers of two bands will be connected to one of the cross dipoles, while the second dipole will be terminated to reduce reflection. These receivers and transmitters will be used to demonstrate FDM operation. For PDM operation, the receiver will be rotated 90 degrees to pick up signals with the second polarization.

SUMMARY OF RESULTS

The dielectric waveguide communication system will eventually use five 45-GHz frequency bands spanning 157.5 to 382.5 GHz and supporting two polarization channels for a total of 10 30-Gbps channels for an aggregated data rate of 300 Gbps. This project in particular seeks to demonstrate 120-Gbps PDM and FDM electronic communication over a 1-m long dielectric waveguide using circuits fabricated in 65-nm CMOS. The 45-GHz bands around 180 and 315 GHz will be utilized for FDM. The transmitters and receivers connected through a diplexer or a combiner to a cross-dipole for the demonstration are shown in Fig. 1.

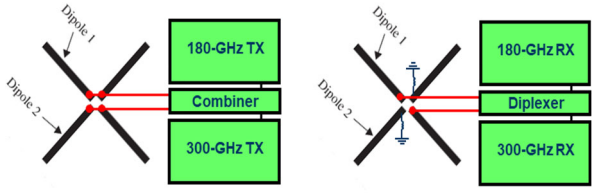

Figure 1. TX and RX chains for PDM and FDM operation with cross-dipoles.

Fig. 2 shows a block diagram of the 180-GHz receiver that utlizes a phase locked loop (PLL) receiver architecture to demodulate MSK modulated signals. A similar architecture is used also for the 315-GHz receiver. 180 and 315-GHz receiver and transmitter pairs with a diplexer and a cross-dipole have been fabricated. Fig. 3 shows measured eye diagrams of 10-Gbps MSK data stream generated and demodulated by the 180 and 315-GHz transmitters and receivers. The transmitters and receivers will be integrated with a multiplexer/demultiplexer, transitions and a low loss holey waveguide (8dB/m) for the multiple channel demonstration utilizing PDM and FDM.

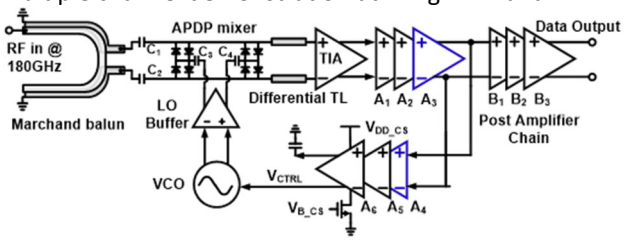

Figure 2. Block diagram of 180-GHz PLL MSK receiver.

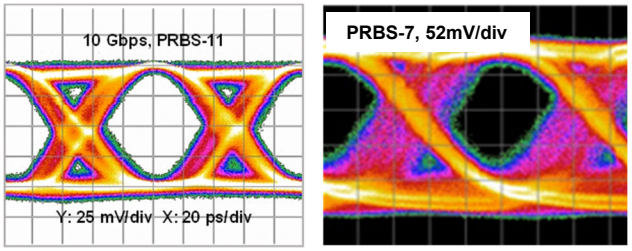

Figure 3. Eye diagrams for a 10-Gbps demodulated output of 180-GHz (Left) and 315-GHz (Right) receivers.

Keywords: dielectric, waveguide, commmunication, millimeter waves

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] Q. Zhong et al., "300-GHz CMOS QPSK Transmitter for 30-Gbps Dielectric Waveguide Communication," *IEEE CICC*, April 2018, San Diego, CA.

[2] Z. Chen et al., "Generation of High Data Rate MSK Modulated 180-GHz Signals," IEEE Microwave Wireless Comp. Letts., vol. 29, no. 11, pp. 757-760, Nov., 2019.

[3] I. Momson et al., "315-GHz Self-Synchronizing Minimum Shift Keying Receiver in 65-nm CMOS," *IEEE Symposium on VLSI Circuits*, June, 2020.

[4] S. Dong et al., "A Wideband 180-GHz Phase-Locked-Loop Based MSK Receiver," *IEEE Custom Integrated Circuits Conference*, March, 2020, Boston, MA.

TASK 2810.018, TRANSITION DESIGN FOR HIGH DATA RATE LINKS AT SUBMILLIMETER WAVE FREQUENCIES

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SIGNIFICANCE AND OBJECTIVES

This research investigates techniques to excite a broadband dielectric waveguide using an integrated on-chip dual-band cross-dipole antenna with a printed circuit board (PCB)-based quadruple ridge waveguide as the transition structure. The transition supports a two-channel communication operating at 180 and 315 GHz with 45-GHz bandwidths.

TECHNICAL APPROACH

The technical approach involves using ANSYS HFSS to design by simulation the individual front-end structures which include a dual-band cross-dipole antenna that serves as the feed for the RF signals on the integrated circuit. In addition, a broadband dielectric waveguide that is ideally 1 meter long is included with a metallic quadruple ridge waveguide that guides the energy between the antenna and dielectric waveguide. Upon completion of designing the individual elements, we performed an impedance and electromagnetic field matching optimization to improve the efficiency of the transitions.

SUMMARY OF RESULTS

Fig. 1 shows the simulated insertion loss of the integrated system from one antenna (transmit chip) to the other antenna (receive chip) with a metallic to dielectric waveguide transition that is 10 mm long on each side of the dielectric waveguide itself (10 mm long). Although not shown, the antennas are designed to operate at 180 and 315 GHz and have $|S_{11}|$ of at least -7 dB within the frequency bands.

The total between the antennas is 30 mm. The simulated $|S_{21}|$ across the frequency range of 100 to 400 GHz is plotted in the figure along with a comparison of the insertion loss when two antennas separated by a distance of 0.4 mm. The insertion loss for these cases are similar. The results show the total insertion loss is -30 dB at 180 GHz and -45 dB at 315 GHz. The transition loss can be calculated by dividing the $|S_{21}|$ by 2 after removing the loss of the dielectric waveguide.

The project officially concluded on 30 June 2020 although we are still completing the demonstration and comparison of results. This work is in collaboration with Dr. Ken O and will involve the measurement of the fabricated antennas standalone and then with the transmitter and receiver ICs to demonstrate for estimating the data rate and system performance.

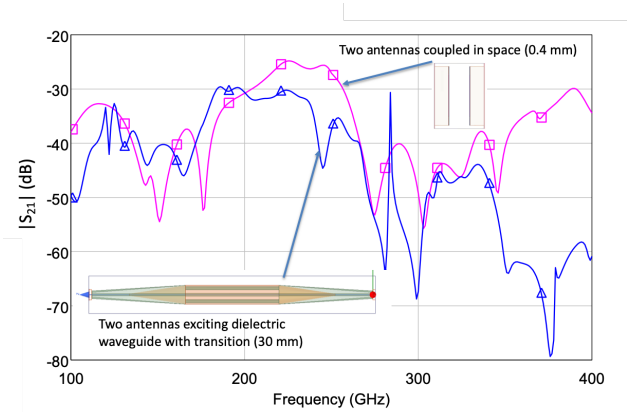

Figure 1. HFSS simulated $|S_{21}|$ when two dual band cross-dipole antennas are separated by the dielectric waveguide and transition (30 mm) and by free space (0.4 mm). Inset shows the HFSS designs.

Table 1. Table of insertion loss ($|S_{21}|$) between dual-band cross-dipole antennas.

Frequency (GHz)	Ant-dielectric-Ant distance	Ant-space-Ant distance
	30 mm	0.400 mm
180	-30 dB	-33 dB
315	-46 dB	-45 dB

Keywords: dual band dipole excitation, dielectric waveguide, transition, quadruple ridge waveguide

INDUSTRY INTERACTIONS

Texas Instruments, NXP, IBM

MAJOR PAPERS/PATENTS

[1] M. Mishra et al., "Waveguide excitation using on-chip antenna for wireline data links," *2019 IEEE International Conference on Microwaves, Antennas, Communications and Electronic Systems (COMCAS), Nov. 2019, Tel Aviv Israel.*

[2] N. Aflakian et al., "Low Loss Square Grid Dielectric Waveguide," IEEE Texas Symposium on Wireless & Microwave Circuits and Systems, May 2020, virtual presentation.

[3] N. M. Vijayakumar, R. Franklin, R. Henderson, "Multilayer Printed Circuit Board Square Waveguide in Ka Band," accepted for URSI GASS 2020, postponed to 2021.

TASK 2810.019, DESIGN AUTOMATION IN COVERAGE MANAGEMENT IN ANALOG AND MIXED SIGNAL SOCS

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ARITRA HAZRA, INDIAN INSTITUTE OF TECHNOLOGY KHARAGPUR

SIGNIFICANCE AND OBJECTIVES

The objective of this task is to design and implement CAD support for coverage management of AMS artifacts in mixed signal SoCs. Towards this goal, we are working closely with Texas Instruments in arriving at formal metrics for AMS coverage and developing mechanisms for computing such metrics over standard commercial simulators.

TECHNICAL APPROACH

We have proposed an extension to SystemVerilog coverage artifacts for defining AMS coverage *bins*. This includes the types: range (normal and deglitched), level, *ddt*, glitch, frequency and mode coverage [1]. We also support different monitoring types, such as cross-coverage, timed monitoring, conditional coverage monitoring, etc. We have designed a coverage specification language similar to the one present in SystemVerilog. A tool has been developed which interfaces with off-the-shelf AMS simulators with standard VPI-callbacks and does an online computation of the different coverage values. The tool also offers an offline mode of operation where it processes the waveform dumps to compute the coverage values. A graphical results visualizer has also been developed for displaying the coverage results.

SUMMARY OF RESULTS

We have obtained results on two test-cases, 1) LDO transistor level netlist circuit, 2) waveform dumps from an industrial SAR-ADC at Texas Instruments, and 3) SAR-ADC from AMS benchmark circuits from ITC 2017. On these test-cases we have computed different coverage types with our tool CoveRT (Coverage Reporting Tool), results of which are given in Table 1.

CoveRT has undergone some optimizations that have been reflected on the last two columns of Table 1. On comparing the results of these coverage types among simulations across different process corners and test benches, one can identify the coverage gaps present during the testing phase. A snapshot of the graphical visualizer from the results is shown in Fig. 1.

We have introduced the support for conditional coverage in AMS. This enables the verification engineer to place optional guard conditions on when a coverage monitor has to be activated. We have also proposed the notion of cross coverage for AMS designs [2].

Table 1. Runtime for Coverage Analysis using CoveRT.

Test-Case	Bin Granularity	Time taken by CoveRT	
		Earlier	Now
TI LDO	0.01	49s	20s
	0.001	1m 52s	23s
	0.0001	2m 41s	27s
TI SAR-ADC	0.01	49s	26s
	0.001	1m 04s	29s
	0.0001	1m 53s	34s
Benchmark SAR-ADC	0.01	1m 48s	28s
	0.001	2m 07s	35s
	0.0001	5m 36s	42s

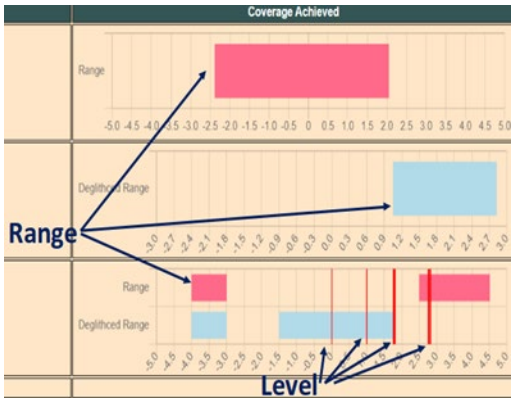

Figure 1. Graphical Visualizer for Coverage Results.

To summarize, we believe that our contribution is rooted at the needs of the verification engineer as we have shown through our results how different coverage types and monitoring types can be utilized to verify various functional attributes of AMS system.

Keywords: Analog and Mixed Signal, Coverage Management, AMS simulation, Conditional Coverage Cross-coverage, SystemVerilog

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] S. Sanyal et al., "CoveRT: A Coverage Reporting Tool for Analog Mixed-Signal Designs," VLSI Design 2020.
[2] S. Sanyal et al., "The Notion of Cross Coverage in AMS Design Verification," ASP-DAC 2020.

TASK 2810.020, ANALOG/MIXED-SIGNAL RF CIRCUIT TIME DOMAIN SENSITIVITY AND ITS APPLICATIONS

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SIGNIFICANCE AND OBJECTIVES

Traditionally, in order to address fault analysis, diagnosis, yield estimation; reliability analysis or performance optimization for an analog circuit, inordinate computer power is entailed to derive the outcomes due to parameter excursions. Time domain sensitivity analysis provides a reasonable accurate estimation of the above and, ideally, one simulation should suffice for all.

TECHNICAL APPROACH

An ultra-fast simulator which contains all the necessary transient information is first developed, with user-defined acceptable accuracy as the sole error control. Based on the transient simulation information from original and closely related adjoint circuit analyses, time domain sensitivity analysis is applied efficiently to estimate the effects of all incremental parameter variations using only the one simulation. Manifolds of acceptable behavior are generated with respect to the nominal response. From these a potential fault library is generated, which includes observability and observation points.

SUMMARY OF RESULTS

In terms of accuracy and efficiency, the ultra-fast transient simulator shows a great deal of improvement when compared to SPICE-derived simulators. The simulator takes step functions directly as input excitations. Furthermore, this novel transient simulator drives the circuit all the way from its initial state to its steady state, thereby providing an alternative approach to address the DC convergence problem.

As the nominal transient response is computed, the related adjoint circuit analysis proceeds concurrently in terms of the linearized model derived from the nominal response. Thereby, we are able to obtain all of the time domain parameter sensitivities. Parameter sensitivity provides the parameter deviation's first order approximation. Fig. 1 compares the results between actual 10% parameter deviation response and the deviation approximation for a simple RC-diode circuit.

Based on the time domain sensitivity information and all parameters' statistical models, the overall multi-manifold acceptability deviation range from the nominal response is established and is as shown in Fig. 2. Any responses that lie outside of the manifold become fault signatures and added to the fault library.

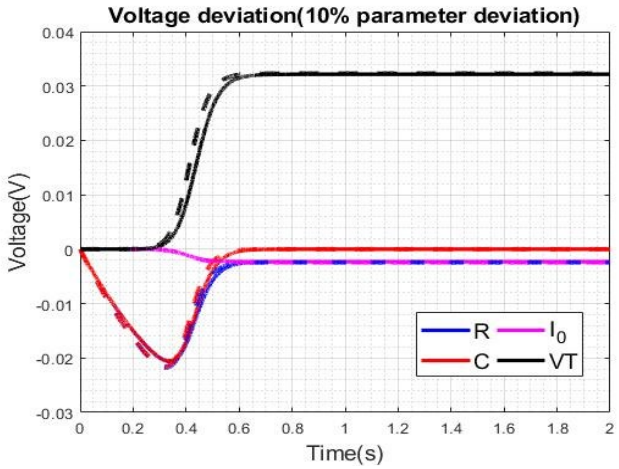

Figure 1. Comparison between 10% parameter deviation and the adjoint sensitivity derived deviation approximation.

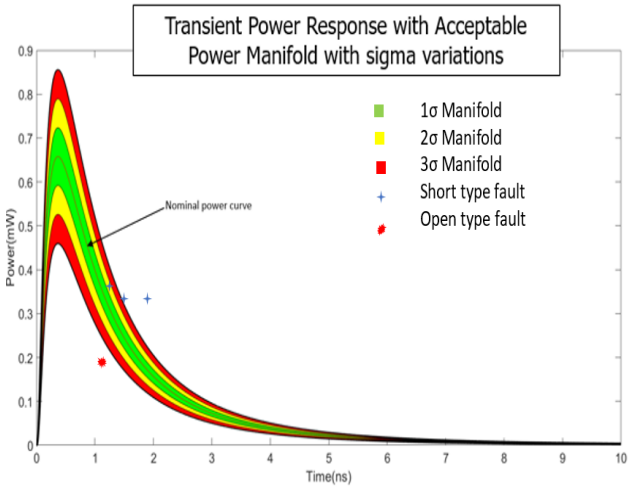

Figure 2. Statistical manifolds generation and fault locations.

In the future, such sensitivity analysis will be applied to more and more complicated circuits. Moreover, its applications to yield estimation, fault diagnosis and corner reconciliation (efficiently addressing historically established corners) will be explored.

Keywords: transient simulator, fault detection, fault diagnosis, parameter sensitivity, time domain and adjoint circuit analysis

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

TASK 2810.026, LOW NOISE BALUN PRE-POWER AMPLIFIER

BRAM NAUTA, UNIVERSITY OF TWENTE, B.NAUTA@UTWENTE.NL

SIGNIFICANCE AND OBJECTIVES

LNA and balun stages are common building blocks in RF receiver front-ends both in mobile and base station applications. Due to high linearity and bandwidth requirements, these blocks are generally discrete components, not only increasing the real estate of the system but also making the system costly. As a solution to this challenge, a CMOS based balun amplifier with high linearity and wide bandwidth is targeted in this work.

TECHNICAL APPROACH

A 22-nm CMOS technology is chosen to design a balun amplifier with high bandwidth. However, achieving high linearity comparable to that of discrete MMIC LNAs (made in HEMT, HBT etc) and passive baluns are challenging. The targeted balun amplifier also needs to achieve other functionalities such as matching at input and output, gain and phase balancing, moderate NF etc. This further increases the challenge to achieve high linearity as many of these functionalities limit the possible architecture and circuit techniques to increase linearity. In this work, attention is also given to explore linearity improvement techniques which are robust to PVT changes.

SUMMARY OF RESULTS

Fig. 1 shows the proposed balun amplifier architecture.

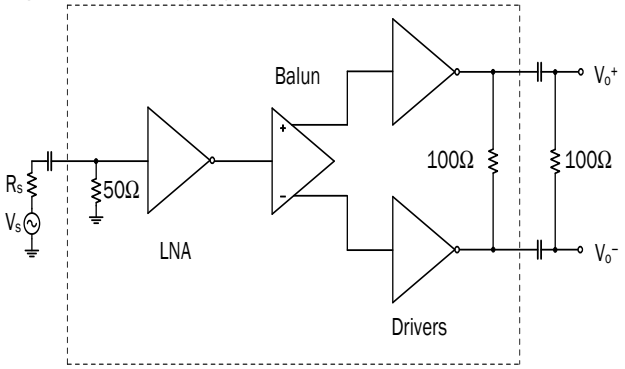

Figure 1. Proposed LNBPA architecture.

The proposed balun amplifier consists of three stages. The first stage is an LNA which reduces the effect of noise from the subsequent stages. Balun action is performed by the middle stage. The final stage consists of driver amplifiers to drive differentially matched loads. Thus different functionalities are distributed among different blocks to alleviate the various trade offs that exist between these functionalities.

Feedback is used to achieve PVT robust high linearity. However, this feedback needs to work at high speed as a wide bandwidth is targeted in this work. Source degeneration is one such high speed feedback technique used in this work. Cascode structures are used as cascoding reduces the capacitive loading due to Miller effect and also reduces the nonlinearity contribution by the output resistance by increasing the output resistance compared to the load resistance. Another linearization technique used in this work is to use complementary design in each stage. This not only reduces the nonlinearity due to the second order polynomial coefficient, but also increases the SNR due to current reuse.

Minimum length transistors are used to maximize the bandwidth. A gain peaking inductor is used in series with the input matching resistor to extend the matching bandwidth. Attention is given during layout to both routing inductance and capacitances. Package and measurement interfaces can degrade the bandwidth if not chosen carefully. For this, wafer probe measurement and chip-on-pcb-cavity techniques are chosen allowing wide bandwidth measurements. These two chip-to-measurement interface techniques also offer low thermal resistance path for the heat generated in the chip.

Table 1. Simulated performance summary. * @2GHz

BW	OIP3	OIP2	G	ΔG	ΔΦ	NF	P	Proc.
GHz	dBm	dBm	dB	dB	°	dB	mW	nm
0.01-8	28*	54*	12	0.2	6	6	800	CMOS2 2FDX

Table 1 shows the simulated performance summary of the balun amplifier in Figure 1. Note that a wide bandwidth and high linearity are achieved. Thus such high linearity and wide band CMOS balun LNAs show potential to replace the discrete LNA and balun blocks, increasing integration, leading to more compact and cost effective systems. Further research is recommended to decrease the NF and power of the proposed balun LNA without compromising other performances.

Keywords: balun amplifier, MMIC, base station, high linearity, wideband.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

TASK 2810.028, ROBUST ATE MULTI-SITE HW DESIGN TO ENABLE EFFECTIVE ANALOG TESTING IN ANALOG-MIXED-SIGNAL (AMS) SOCS

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SIGNIFICANCE AND OBJECTIVES

Mission-critical applications dictate demanding testing, with significant impact on time-to-market and manufacturing cost. Massively parallel multisite testing offers great improvements in throughput and test-cost. This project will develop tools for automatically flagging excessive site-to-site variations, identifying ATE hardware issue causing s2s variations, and enhancing multi-site ATE hardware robustness and effectiveness.

TECHNICAL APPROACH

Existing volume probe/final-test data and ATE hardware files will be used to develop statistical signal processing and machine learning algorithms to automatically process the volume data and flag the problem sites and specifications. These results will enable identification of sensitive components/nets in the ATE hardware. Targeted extraction/simulations will be run and additional GRR measurements will be taken, for identifying hardware root causes. Such learning will lead to improved test board hardware design which is robust to site-to-site variations. A framework for pre-fabrication verification, post-fabrication evaluation and site-calibration, and adaptive test flow will improve robustness and effectiveness.

SUMMARY OF RESULTS

During the first year, we have developed a method for estimating the true distribution of a given specification at an ideal reference site, called "Site 0". By comparing the actual distribution at a given site against Site 0, we have developed 3 different algorithms for automatically identifying problem sites with excessive variationss from existing probe data. We have also identified interesting correlations between certain board parameters and site-to-site variations in volume probe data.

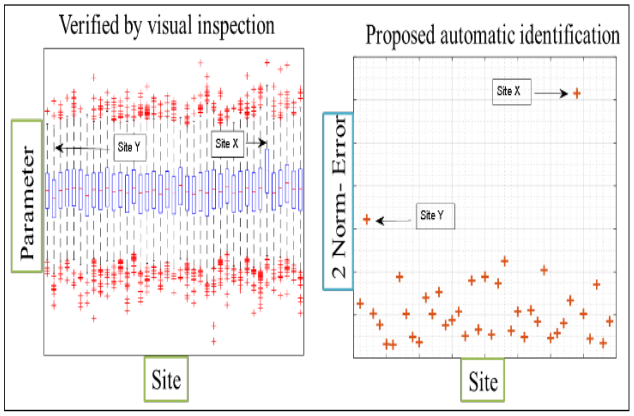

Figure 1. Example results from the first of 3 proposed issue site flagging algorithm. Volume probe data from TI are processed and a normalized error is computed for each site. The right plot shows site X and site Y flagged as issue sites, the left plot shows the box plot, confirming by human inspecting correctness of the automatic flagging.

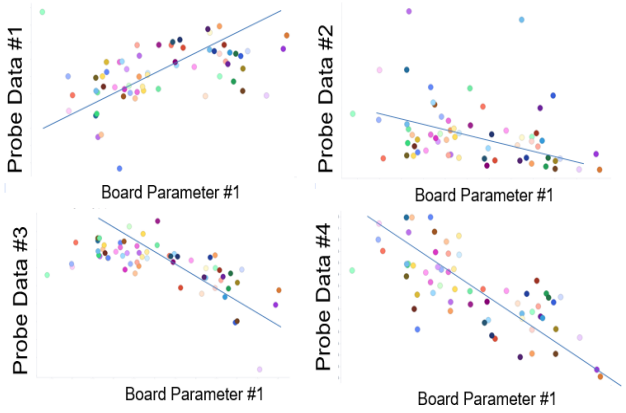

Figure 2. By analyzing correlation between certain normalized site error scores with sensitive board hardware parameters, we identified interesting correlation trends in the 4 subplots. Such information is useful for test board debugging.

Codes for the algorithm were translated from Matlab to Python. The codes and following items were delivered to TI: (i) Documentation text file and a video tutorial, (ii) Filtering script targeting modules and parameters of interest, (iii) Visualization script enabling easy visualization and incorporation in Spotfire, and (iv) Scoring scripts for identifying and flagging issue sites.

Keywords: multi-site testing, test cost reduction, site-to-site variations, volume test data learning, ATE test hardware debug/design

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] P. Farayola, S. Chaganti, A. Obaidi, A. Sheikh, S. Ravi, D. Chen. "Quantile – Quantile Fitting Approach to Detect Site to Site Variations in Massive Multi-site Testing," IEEE VLSI Test Symposium (VTS), pp 1-6, 2020.

[2] P. Farayola, S. Chaganti, A. Obaidi, A. Sheikh, S. Ravi, D. Chen. "Domain Transformation Technique to Enhance Detection of Site to Site Variations from Test Volume Date for Massive Multi-site Measurements," under TI review and approval, to be submitted to IEEE Trans. On Instr. and Meas. (TIM).

TASK 2810.029, 170GHZ – 260GHZ WIDEBAND PA AND LNA DESIGN IN SILICON

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SIGNIFICANCE AND OBJECTIVES

We design a wideband power amplifier (PA) and a low-noise amplifier (LNA) operating in the 170-260 GHz band using a commercial silicon process. Both these blocks are critical components for future high-speed wireless communication links and high-resolution 3D- imaging radars.

TECHNICAL APPROACH

The blocks are designed in a 130-nm SiGe-G2Cu BiCMOS process offered by IHP Microelectronics. The 3-stage PA uses transmission line based current combining technique to boost the saturated output power and achieve the targeted bandwidth. We have fabricated single-ended as well as differential versions of the PA with an intention to compare the overall performance. The single-ended LNA consists of 7 cascaded CE stages and uses staggered tuning approach to boost the bandwidth performance.

SUMMARY OF RESULTS

The IHP SiGe-G2Cu process has transistors having an f_T/f_{max} of 300/450 GHz. It offers MIM caps having a density of 2fF/μm^2 and it's copper backend enables the design of low-loss transmission line based passives.

The gain performance of the transistor deteriorates with the width when the operating frequencies are higher than $f_{max}/3$. We have thus resorted to output power-combining approach to boost the output power, instead of conventionally scaling the widths of the amplifying stages in the cascade chain. A cascade of 3 amplifying stages is used to achieve the gain target of 20dB.

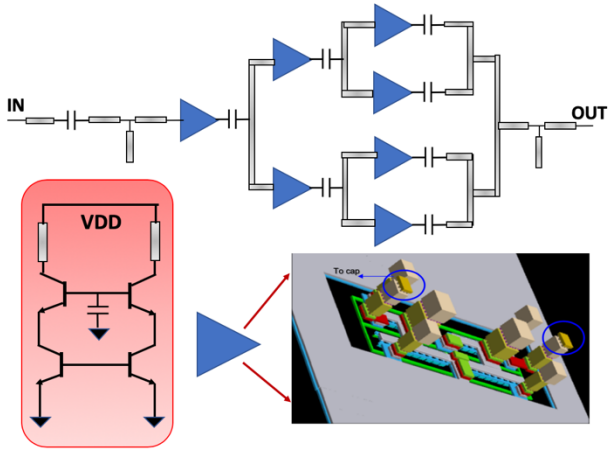

Figure 1. The architecture of the 3-stage power combining PA, along with the 3-D layout of unit stage.

As shown in Fig. 1, the output power of first stage is split and the power of 4 unit stages is combined using a passive combiner at the output. Owing to it's high output impedance and superior reverse isolation, a cascode stage with 10 finger transistors is used to form a unit stage. The interstage matching networks are designed for optimum gain, whereas the output combining network is designed for optimum power performance. A transmission line based Marchand balun is incorporated at the input and the output to facilitate single-ended measurements.

Fig. 2 shows the architecture of the 7-stage CE LNA. The stages are designed to peak at different frequencies to enhance the overall bandwidth of the LNA. The first 3 stages of the LNA are DC-biased to avoid the noise contributions of the low-Q MIM capacitor in the interstage matching networks at the operating frequencies. As shown, the first 3 stages are biased for optimium noise performance and the proceeding stages are biased for optimum gain performance.

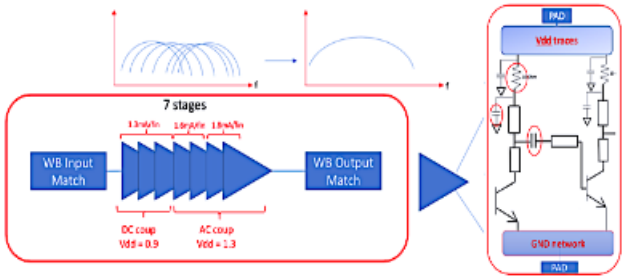

Figure 2. The architecture of the 7-stage LNA.

The input, output and the interstage wideband matching networks for both the PA and the LNA are designed using GCPW transmission lines to avoid crosstalk. To ensure stability, the biasing traces are designed using zero-Ω transmission lines. The entire layout is simulated in a 3D planar EM simulator to capture the high frequency effects. Both the designs are currently in fabrication.

Keywords: PA, LNA, Wideband, Silicon, SiGe BiCMOS.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

TASK 2810.030, NEURAL NETWORK RECOGNITION & ON-CHIP ONLINE LEARNING WITH STT-MRAM

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SIGNIFICANCE AND OBJECTIVES

Neuromorphic computing promises exceptional capabilities for artificial intelligence through highly-efficient circuit structures mimicking the structure and functionality of the human brain. This project proposes the first experimental demonstration of a neural network system that leverages the stochastic switching of STT-MRAM devices to perform analog on-chip online learning and recognition.

TECHNICAL APPROACH

We propose an STT-MRAM array with a novel analog CMOS weight-updating circuit. The STT-MRAM array is being designed to enable both deterministic switching for memory applications and stochastic switching for neuromorphic computing. The analog circuit will perform an unsupervised learning rule based on spike-timing-dependent plasticity through which the relative timing of input and output neuron spikes determine the voltages applied to the synapses. This will be the first experimental demonstration of on-chip online learning and recognition with a STT-MRAM, enabling high speed, low area, energy-efficiency and robustness. The chip will be designed and fabricated using the UMC's 22-nm technology.

SUMMARY OF RESULTS

This project is composed of three separate components that will be designed simultaneously: an STT-MRAM crossbar array, an on-chip online learning circuit, and a control & testing framework. The STT-MRAM array will store binary states in a non-volatile manner, and connect to both the control and the learning circuits. The mixed-signal on-chip learning circuit will update the synapse weights in the STT-MRAM array based on the time difference between the input and output pulse. The control circuit will enable toggling of the chip between training and inference modes, and perform signal input and parameter configuration.

This project is divided into four steps: behavioral design and simulation, transistor-level design and simulation, chip layout and fabrication, and testing. First, behavioral simulations of the circuit structure and functionality are performed in C++ to determine the optimal online learning parameters. After this, the CMOS on-chip online learning neural network will be designed and simulated in SPICE to verify the learning function with variation and noise. The circuit will then be laid out and submitted for fabrication. Finally, the fabricated circuit's neuromorphic operations will be tested with TI's iFLEX system.

The behavioral simulation results have already proven the feasibility of this STT-MRAM unsupervised learning process on the MNIST handwritten digit database. First, a simplified MNIST dataset has been used that contains ten binarized input images representing digits 0 to 9. The unsupervised STT-MRAM learning method is performed on this dataset with a single-layer neural network; after training, the same images are used to test the inference accuracy. The STT-MRAM synapse resistance map is shown in Fig. 1, and represents a recognition rate of 100%.

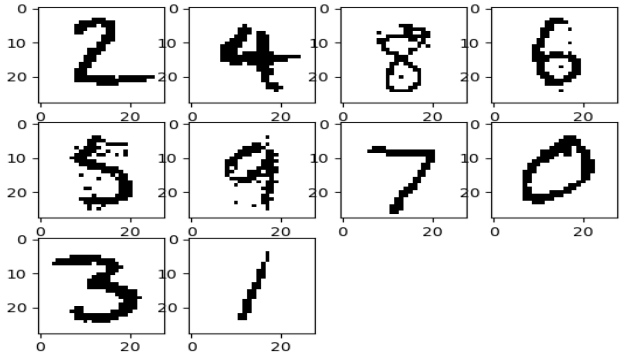

Figure 1. The resistance of synapses after training. The black pixels represent low resistance, while the white pixels represent high resistance.

Preliminary simulations have also been performed with single-layer neural networks using the standard MNIST dataset. As can be seen in Table 1, the maximum accuracy peaks below 80% with 100 output neurons, which is consistent with alternative single-layer neural networks. In order to improve the accuracy, we will design multi-layer STT-MRAM neural networks with superior learning.

Table 1. MNIST single-layer neural network simulation results.

# of Output Neurons	10	20	100	200
Inference Accuracy	45.5%	59.3%	78.7%	77.7%

In the upcoming year, these circuits will be designed and submitted for fabrication.

Keywords: STT-MRAM, Neural Network, Online Learning, Unsupervised Learning, Artificial Intelligence

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

TASK 2810.031, DEVELOPMENT AND ASSESSMENT OF MACHINE LEARNING BASED ANALOG AND MIXED-SIGNAL VERIFICATION

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SIGNIFICANCE AND OBJECTIVES

Machine learning (ML) has offered potentially transformative opportunities for verification of analog/mixed-signal (AMS) circuits. The successful application of ML-enabled verification methodologies requires to address the coverage and robustness challenges of the deployed data-driven techniques.

TECHNICAL APPROACH

We have tackled the robustness and coverage of ML-enabled AMS verification [1] from two synergistic angles: 1) assessing robustness by developing global adversarial attacks [2], and 2) developing robust machine learning methods for unsurprised rare failure/defect detection without using labeled data [3]. For the former, we develop two families of global adversarial attack methods: the alternating gradient attack method and the extreme-value-guided Markov-Chain Monte-Carlo sampling for assessing the robustness of a given ML model with respect to small input perturbations in the entire parametric space. The latter effort leads to a robust outlier/anomaly detection methodology via self-labeling of unlabeled normal design data.

SUMMARY OF RESULTS

Advanced outlier detection during post-silicon testing fulfills the critical mission of preventing shipping defective parts to customers causing field failures. Learning from customer failures to improve outlier detection during post silicon testing is critical to reach the zero-defect quality level. Due to the extreme scarcity of customer failure data, reliably detecting rare defects using unsupervised learning in a high-dimensional input feature space formed by the required large number of parametric test measurements is very challenging. We propose to train a more robust unsupervised learning model by self-labeling the normal training data via a set of transformations and using the labeled data to train a multi-class classifier through supervised training, as shown in Fig. 1. The goodness of the multi-class classification decisions with respect to an unseen input data is used as a normality score to detect anomalies. We propose to use several transformation function families including reversible information lossless transformations to retain the data information and boost the performance and robustness of the proposed self-labeling approach.

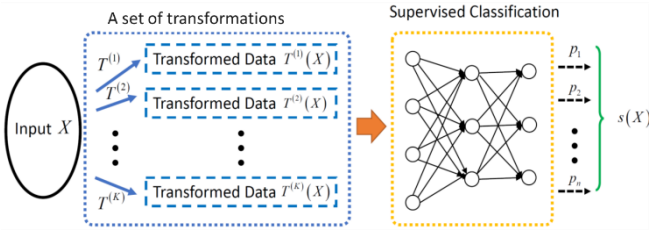

Figure 1. Proposed self-labeling unsupervised outlier detection using input/feature transformations.

Table 1 shows that the proposed methods using four transformation approaches provide higher accuracies (AUROC) than the standard techniques on unsupervised screening of rare customer returns of six industrial automotive microcontrollers using 6 to 5,5592 parametric tests or subsets of manually selected "critical" tests as features. In the future, we will continue to focus on the global robustness of ML based AMS verification by performing in-depth assessment and tradeoff analysis on local/global robustness and accuracy. We will also develop ML techniques for design verification and test.

Table 1. Results on industrial microcontroller defect detection.

	Datasets	Reference Methods				Proposed Methods			
		Gaussian	OCSVM	IsoForest	AE	PolyTrans	RevTransA	RevTransB	RevTransC
All Tests	Chip 1	0.685	0.872	0.882	0.902	0.461	0.889	0.938	0.949
	Chip 2	0.823	0.964	0.984	0.979	0.898	0.928	0.939	0.895
	Chip 3	0.882	0.94	0.937	0.977	0.928	0.934	0.954	0.973
	Chip 4	0.921	0.788	0.838	0.931	0.826	0.828	0.814	0.843
	Chip 5	0.972	0.907	0.978	0.959	0.986	0.865	0.966	0.985
	Chip 6	0.929	0.738	0.758	0.888	0.916	0.891	0.967	0.999
	Chip 1 (Critical)	0.858	0.753	0.885	0.759	0.839	0.818	0.922	0.647
	Chip 2 (Critical)	0.846	0.858	0.853	0.845	0.917	0.977	0.952	0.925
	Chip 3 (Critical)	0.587	0.874	0.932	0.733	0.992	0.815	0.826	0.986
	Chip 4 (Critical)	0.81	0.77	0.586	0.944	0.778	0.809	0.529	0.762
	Chip 5 (Critical)	0.841	0.99	0.984	0.671	0.942	0.96	0.936	0.941
	Chip 6 (Critical)	0.89	0.861	0.963	0.818	0.935	0.929	0.899	0.896
	Avg. AUROC	0.837	0.860	0.882	0.867	0.868	0.887	0.887	**0.900**
						Polynomial Transforms	Reversible Transforms		

Keywords: Machine learning, analog and mixed-signal, anomaly detection, robustness, adversarial attacks

INDUSTRY INTERACTIONS

Texas Instruments, IBM, NXP

MAJOR PAPERS/PATENTS

[1] H. Hu et al., "Enabling High-Dimensional Bayesian Optimization for Efficient Failure Detection of Analog and Mixed-Signal Circuit," IEEE/ACM DAC, June, 2019.

[2] H. Hu et al., "Assessment of Machine Learning Robustness for Analog and Mixed Signal Verification," SRC Techcon, September 2019.

[3] H. Hu et al., "Advanced Outlier Detection Using Unsupervised Learning for Screening Potential Customer Returns," ITC, 2020 (submitted).

TASK 2810.033, INTERLEAVED NOISE-SHAPING SAR ADCS FOR HIGH-SPEED AND HIGH-RESOLUTION

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SIGNIFICANCE AND OBJECTIVES

This research will deliver an energy-efficient high-speed, high-resolution ADC architecture for high performance and emerging applications, including medical imaging, 4G/5G infrastructure, radar, production test, and defense. We will expand the bandwidth of our time-interleaved (TI) noise-shaping (NS) SAR architecture by an order of magnitude to extend SAR-ADC efficiency to high speed and high resolution.

TECHNICAL APPROACH

Our new SAR-based architecture combines time-interleaving with noise-shaping, to break the tradeoff between speed and accuracy, and enable both high speed and high resolution. The target design space is unserved by state-of-the-art SAR ADCs. Different to conventional SAR and interleaved SAR converters, our approach provides both high resolution and high bandwidth. We expand our revolutionary new interleaved noise-shaping SAR ADC architecture to deliver an order-of-magnitude more bandwidth, as well as improved energy efficiency and enhanced robustness.

SUMMARY OF RESULTS

The Noise-Shaping SAR (NS-SAR) is an emerging ADC architecture that offers both high resolution and high energy efficiency. State-of-the-art NS-SAR ADCs eliminate the need for op-amps, which relaxes design complexity and technology scaling issues. However, existing NS-SAR ADCs, with a high FoM, are limited in bandwidth (typically in the MHz range). This makes NS-SAR ADCs unsuitable for applications that need bandwidths in the tens of MHz range, such as wireless communications. Traditionally, high-bandwidth and high-resolution applications utilize pipeline or continuous-time sigma-delta (CT-SD) ADCs, but these architectures are much more power hungry than the NS-SAR.

To increase the bandwidth of NS-SAR ADCs and extend their low-power advantages, this work presents a new time-interleaved noise-shaping SAR (TINS-SAR) architecture that enables a higher bandwidth. Although time-interleaving of ADCs is difficult for high resolution, interleaving impairments can be avoided when combining interleaving with noise-shaping. Our prototype 40-nm CMOS TI-NS-SAR ADC has a measured SNDR of 70.4dB for a 50MHz bandwidth without calibration. It consumes only 13mW and occupies 0.061mm^2, making it a potential substitute for CT-SD ADCs.

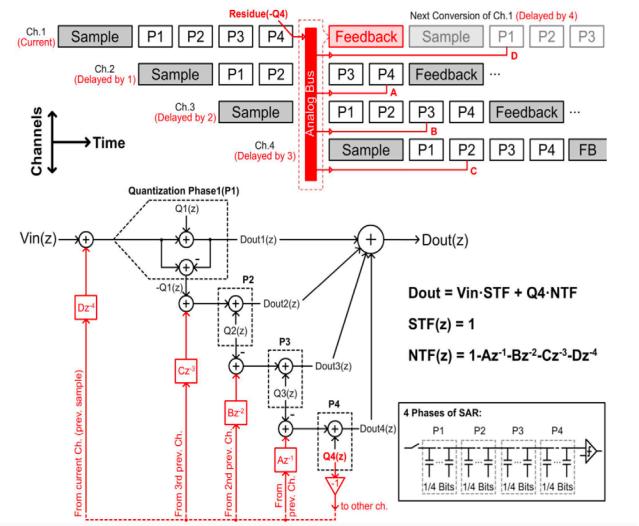

Figure 1. Interleaved noise-shaping architecture.

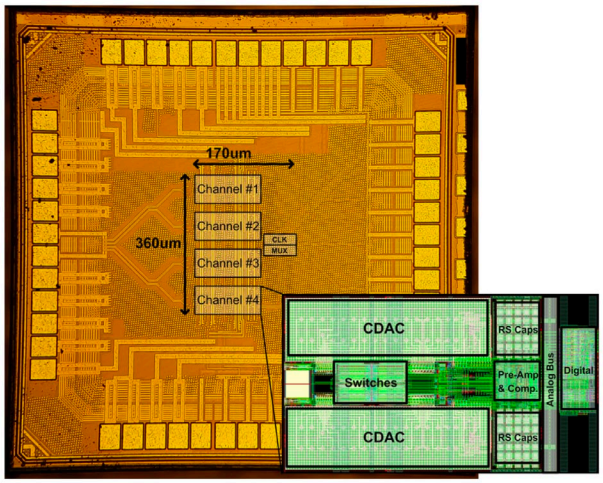

Figure 2. Protoype ADC in 40nm CMOS.

Keywords: Sigma Delta, ADC, sensor, SAR, IoT

INDUSTRY INTERACTIONS

Texas Instruments, Intel, ARM, NXP

MAJOR PAPERS/PATENTS

[1] L. Jie, B. Zheng and M. P. Flynn, "A Calibration-Free Time-Interleaved Fourth-Order Noise-Shaping SAR ADC," in IEEE Journal of Solid-State Circuits, December 2019.

[2] L. Jie, B. Zheng and M. P. Flynn, "20.3 A 50MHz-Bandwidth 70.4dB-SNDR Calibration-Free Time-Interleaved 4th-Order Noise-Shaping SAR ADC," 2019 IEEE International Solid- State Circuits Conference, (ISSCC), February 2019.

TASK 2810.036, HIGHLY STABLE INTEGRATED FREQUENCY REFERENCES

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SIGNIFICANCE AND OBJECTIVES

Stable frequency references serve many time keeping functions. While quartz crystal-based references can achieve the desired electrical performance, they are bulky, expensive, power inefficient, and suffer from long start-up time. This task will develop novel architectures and circuit techniques that will overcome these drawbacks.

TECHNICAL APPROACH

Integrated frequency references provide an attractive alternative to bulky quartz-based crystal oscillators (XOs) for reducing cost and form-factor. However, their frequency accuracy is currently at least an order-of-magnitude inferior to that of XOs. This proposal seeks to close this performance gap by employing novel digital compensation techniques that can be realized in CMOS technologies. Using only two temperature measurements, we will perform compensation and the target power efficiency is better than 1µA/MHz. Proposed techniques will be verified experimentally using prototypes fabricated in a standard CMOS process.

SUMMARY OF RESULTS

Given the drawbacks associated with prior-art, we are currently exploring techniques to compensate higher-order temperature coefficients with nearly unlimited precision. To this end, we are investigating compensation techniques that use combinations of switched-resistors that provide almost unlimited tuning resolution while using only one switch as shown in Fig. 1. In this architecture, a ring oscillator is embedded in a frequency-locked loop (FLL), and the output clock is generated by a voltage controlled oscillator driven by control voltage produced by integrating the difference between the reference voltage, V_{REF}, and frequency-dependent voltage. The oscillator outputs are used to drive a switched-capacitor resistor which causes output frequency, $F_{OUT} = 1/CR_{REF}$ in steady-state. Therefore, implementing R_{REF} using 3 switched resistors, as described earlier, eliminates the temperature dependence and significantly improves F_{OUT} accuracy. A large loop-gain of the feedback also suppresses sensitivity to voltage variations and oscillator noise, and helps to lower Allan deviation in 1-second strides to sub-ppm levels. Preliminary behavioral results indicate that it is indeed possible to achieve excellent accuracy (< 100ppm) with second-order compensation.

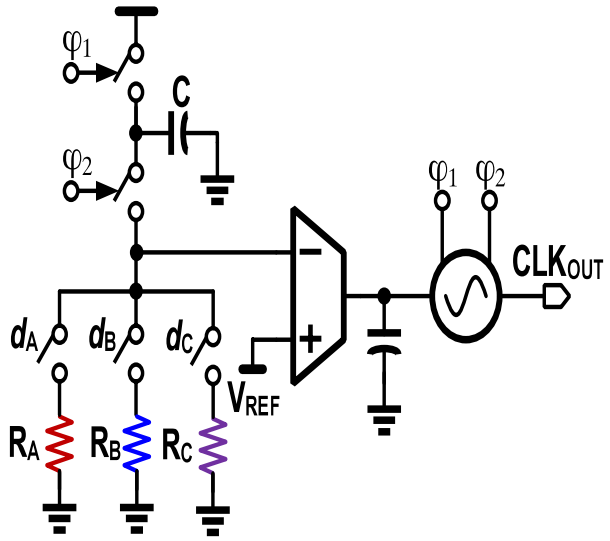

Figure 1. Proposed frequency reference.

Keywords: RTC, temperature-compensated oscillator.

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

TASK 2810.037, HIGH-PERFORMANCE RINGAMP-BASED ADCS

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SIGNIFICANCE AND OBJECTIVES

Our research goal is to solidify ring amplifier as a dominant means of amplification in mixed-mode circuits through demonstration of performance improvements over traditional operational transconductance amplifiers. In this task, high-performance ring amplifier-based ADCs in FinFET technologies are explored addressing the current need of high-speed applications in scalable CMOS.

TECHNICAL APPROACH

As most high-speed analog-to-digital converters utilize pipeline architectures with residue amplification, a need for power efficient and area compact amplifiers are necessary to replace the commonly used power-hungry traditional amplifier blocks such as folded cascode and telescopic op-amp. Process scaling has become ever important with the migration towards FinFET technologies, and maintaining performance across reducing supply voltage and tolerance in the presence of new effects on silicon such as self-heating have become extremely critical to address. Prototypes fabricated in 22-nm FinFET technology will be used to demonstrate the performance capabilities of ring amplifier based ADCs.

SUMMARY OF RESULTS

In this research, we are targeting the demonstration of a single-channel GSPS ADC with future plans to look into reaching higher sample rates through time-interleaving.

The 12-bit pipeline-SAR analog-to-digital converter aims to achieve high-speed with a low-power three-stage structure. A non-binary 2-bit-per-cycle SAR ADC resolves the first 6-bits through three cycles [1]. In the 2-bit-per-cycle scheme, the use of non-binary decision levels introduces error correction and alleviates the fluctuation of reference, comparator offset, and DAC settling time, therefore, accelerating the conversion period of the first stage. The remaining residue then undergoes residue amplification using a ring amplifier. A dual-deadzone ring amplifier [2] utilizes a process, voltage, and temperature stabilizing bias circuit [3] and achieves faster signal settling when compared with traditional op-amps. The ring amplifier performs amplification over 400ps with a dynamic power consumption of 4mW. The back-end is comprised of a two-stage passively pipelined SAR with passive inter-stage charge sharing and yields 9-bits with significant speed advantage and minimal power overhead. Redundancy is distributed throughout the ADC and a total of 12-bits quantization level is achieved. Input buffering is provided with a wide-swing and high-linearity flipped source follower.

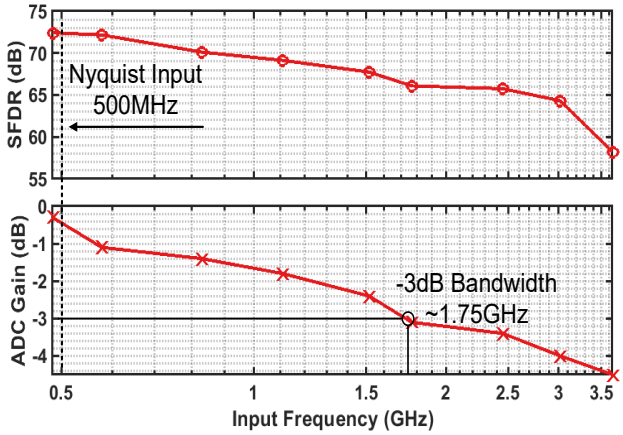

Figure 1. Simulated linearity performance and transfer gain of the passively pipelined SAR analog-to-digital converter.

Initial simulation results of the dynamic performance and transfer gain of the single-channel ADC are shown in Fig. 1. The ADC is simulated with input signal beyond Nyquist frequencies which is then sub-sampled back into the 500MHz bandwidth of the single-channel ADC. Simulation results indicate that the 3-dB bandwidth of the converter's front-end is around 1.75GHz. Preliminary noise simulation of the ADC indicates a peak SNDR of 65dB in the 500MHz Nyquist bandwidth with power of the ADC core at 8mW. The input buffer consumes an additional 6mW of power, for a total system power of 14mW.

Keywords: analog-to-digital converter, ring amplifier, gigasample, FinFET, high accuracy

INDUSTRY INTERACTIONS

NXP, Intel, Texas Instruments

MAJOR PAPERS/PATENTS

[1] H. Hong *et al.*, "An 8.6 ENOB 900MS/s time-interleaved 2b/cycle SAR ADC with a 1b/cycle reconfiguration for resolution enhancement," *IEEE Int. Solid-State Circuits Conference (ISSCC)*, Feb. 2013.

[2] A. Elshater *et al.*, "A 10-mW 16-b 15-MS/s two-step SAR ADC with 95-dB DR using dual-deadzone ring amplifier," *IEEE J. of Solid State Circuits (JSSC)*, Dec. 2019.

[3] P. Venkatachala *et al.*, "Process invariant biasing of ring amplifiers using deadzone regulation circuit," *IEEE Int. Symp. on Circuits and Systems (ISCAS)*, May 2018.

TASK 2810.043, ANALOG OPTIMIZATION HYBRIDIZING DESIGNER'S INTENT AND MACHINE LEARNING

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SIGNIFICANCE AND OBJECTIVES

Machine learning (ML) offers a new data-driven direction for optimizing analog circuits with potentially large gains in design productivity and performance. The black-box nature of ML based design optimization introduces new challenges such as lack of interpretability and lack of mechanisms for incorporating knowledge of domain experts.

TECHNICAL APPROACH

We will facilitate machine learning based analog design optimization by hybridizing ML and designer's intent via research explorations including: 1) integration of designer's knowledge and ML for hybrid analog performance models (HAPMs) that are more interpretable and robust, and trainable using smaller amounts of expensive data, 2) interfaces for specifying designer's intent and translation into internal mathematical constructs to guide the ML based optimization, 3) complimentary ML-enabled optimization approaches using Bayesian optimization (BO) and deep reinforcement learning (RL), supported by interfaces with human designers and the HAPMs, and 4) development of ML based design tools.

SUMMARY OF RESULTS

As a first step, we investigate the potential of the proposed hybrid analog performance models (HAPMs).

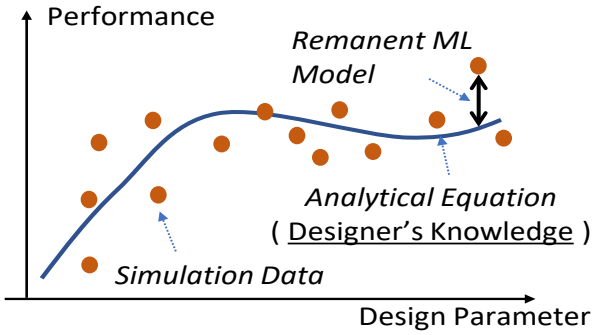

Figure 1. Hybrid analog performance models (HAPMs).

Existing analog performance models largely fall under two categories: analytical design equations and fitted black-box models. While derived based on designer's knowledge, analytical equations suffer from limited accuracy, particularly for advanced technology nodes, and can only capture a subset of design parameters. As such, they are mostly meant for deriving design insights rather than supporting precise optimization. Black-box models may well fit the simulation data for a given design/technology. However, the robustness and accuracy are subject to overfitting and noisy data, and model training may require much data. Moreover, they cannot provide design insights and lack interpretability.

We integrate the power of machine learning (ML) with designer's knowledge via a new family of hybrid analog performance models (HAPMs) as shown in Fig. 1. To predict the performance y given a set of design parameters $\boldsymbol{p}$, a HAPM superposes: 1) a (parameterized) analytical design equation f_A and 2) a trained remnant ML model f_{ML}: $y = f_{HAPM}(\boldsymbol{p}) = f_A(\boldsymbol{p}_A) + f_{ML}(\boldsymbol{p})$ where $\boldsymbol{p}_A$ is a subset of design parameters captured in the designer's equation. Given a training dataset, $f_{ML}(\boldsymbol{p})$ is trained to reflect the part of the data not covered by the design equation $f_A(\boldsymbol{p}_A)$. As such, the design equation provides a mechanism to capture the designer's knowledge while $f_{ML}(\boldsymbol{p})$ leverages the power of ML for achieving high accuracy. Table 1 shows the MSE errors of an analytical, ML (Gaussian Process), and HAPM model on modeling of the SNR of 2nd Order $\Sigma\Delta$ modulator as functions of the number of training examples (N). Both the GP and HAPM are noticeably more accurate than the analytical equation measured by mean squared error (MSE) and R2 score while the HAPM significantly outperforms the GP model when N is small.

Table 1. Accuracies of an analytical, ML (Gaussian Process) and HAPM model on the SNR of 2nd-Order ∑Δ modulator.

# Data Points	Analytical		Gaussian Process		Hybrid		R2 Increase (%)
	MSE	R2	MSE	R2	MSE	R2	Hybrid over GP
56	710.08	**0.12**	868.70	**-0.08**	816.08	**-0.01**	**83.33**
100	710.08	**0.12**	530.01	**0.34**	483.91	**0.40**	**16.67**
150	710.08	**0.12**	325.99	**0.59**	307.01	**0.62**	4.03
600	710.08	**0.12**	153.49	**0.81**	148.59	**0.82**	0.87
900	710.08	**0.12**	117.27	**0.85**	115.03	**0.86**	0.35
950	710.08	**0.12**	107.90	**0.87**	105.88	**0.87**	0.35
1000	710.08	**0.12**	95.43	**0.88**	93.06	**0.88**	0.23
1100	710.08	**0.12**	87.64	**0.89**	85.42	**0.89**	0.34
1200	710.08	**0.12**	82.16	**0.90**	79.82	**0.90**	0.33
3000	710.08	**0.12**	45.12	**0.94**	43.59	**0.95**	0.21

Keywords: Machine learning, analog circuits, design optimization, designer's intent, domain knowledge

INDUSTRY INTERACTIONS

Texas Instruments, IBM, NXP

MAJOR PAPERS/PATENTS

TASK 2810.044, HIERARCHICAL CHARACTERIZATION AND CALIBRATION OF RF/ANALOG CIRCUITS USING LIGHTWEIGHT BUILT-IN SENSORS

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SIGNIFICANCE AND OBJECTIVES

This project will explore a hierarchical calibration approach, including local calibration and system-level target setting, where information from built-in monitors is used to match the performance of individual blocks, as well as guarantee that the entire system functions in cohesion even if constraints or operating conditions change dynamically.

TECHNICAL APPROACH

Fig. 1 shows the proposed approach. Simple built-in sensors that measure current, DC voltages, and RF power are used to set local circuit parameters, such as circuit bias or matching components, to optimize the performance with respect to given specifications. System-level calibration will rely on a statistical model (e.g. machine learning), whereas circuit-level calibration can be conducted with simplified mathematical models.

SUMMARY OF RESULTS

While there has been extensive research in the design and calibration of specific N-port reflectometer (NPR) architectures for RF built-in self-test (BIST), the underlying assumption in the calibration (and by extension the design) process has been that the components used in the measurements, such as couplers, splitters, combiners, and power detectors, are fully characterized and almost ideal. This approach makes sense when using the NPR in a discrete measurement set-up. However, when designing a network analyzer for built-in self-test (BIST) applications, some of these assumptions break down. The external calibration phase during production test suppresses some of the non-idealities, such as mismatch between the gain of power detectors. However, these non-idealities change available signal power, and hence render some of the assumptions made in the design process invalid. A better accuracy can be obtained when taking all these factors into account during the design process.

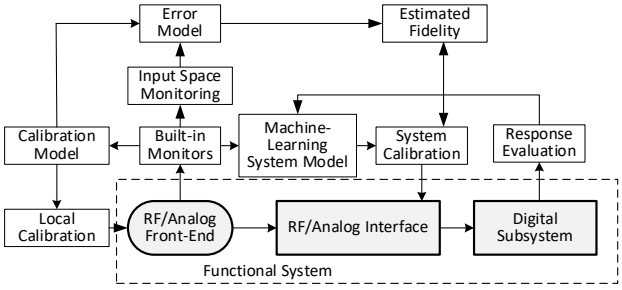

Figure 1. Overview of proposed approach.

We developed an analytical model for improving the accuracy of NPRs under noise and other imperfections. Based on this model, we propose a design flow for optimizing the NPRs for measurement accuracy under specific design constraints, such as coupler gain, noise, and power detector dynamic range. Our optimization framework applies to both traditional NPR architectures that conducts measurements in parallel and the multi-state NPR architectures that serially conduct measurements. We also implement the multi-state reflectometer architecture based on the optimized parameters using off-the-shelf RF components and evaluate the accuracy with respect to an external VNA, which is the standard of measurement for reflection coefficients. Fig. 2 shows the comparison of the NPR implemented with off the shelf components against VNA-based characterization.

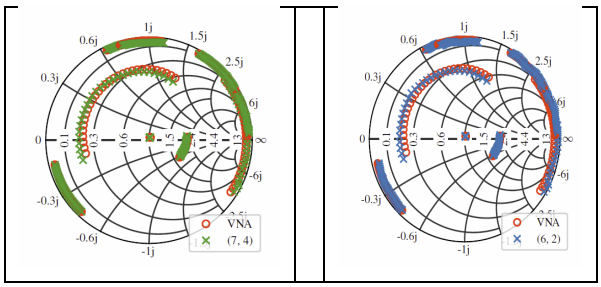

Figure 2. Measurement accuracy of two optimized NPR configurations.

Keywords: Analog BIST, Fault Simulation

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Y. Chen and D. Ma, "EMI-regulated GaN-based switching power converter with Markov continuous random spread-spectrum modulation and one-cycle on-time rebalancing," IEEE J. Solid-State Circuits (JSSC), vol. 54, no. 12, pp. 3306-3315, Dec. 2019.

[2] Y. Chen and D. Ma, "An 8.3MHz GaN power converter using Markov continuous RSSM for 35dBμV conducted EMI attenuation and one-cycle T_{ON} rebalancing for 27.6dB V_O jittering suppression," ISSCC, Feb. 2019, pp. 250-251.

APPENDIX I PUBLICATIONS OF TXACE RESEARCHERS

Conference Publications

[1] Chekuri, V., Rahman, N.M., Lee, E., Singh, A., and Mukhopadhyay, S. (2020). A Fully Synthesized Integrated Buck Regulator with Auto-generated GDS-II in 65nm CMOS Process. *IEEE Custom Integrated Circuit Conference (CICC), Boston, MA*, pp. 1-4, IEEE.

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To discuss our core facilities in Dallas and how to obtain access to them and to receive future TxACE requests for proposals, please contact:
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