TEXAS ANALOG CENTER OF EXCELLENCE

Annual Report 2016 – 2017

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TxACE
TEXAS ANALOG
CENTER OF EXCELLENCE

TxACE MISSION

The Texas Analog Center of Excellence seeks to create fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, health care, and public safety and security.

TxACE THRUSTS

- *Safety, Security and Health Care*
- *Energy Efficiency*
- *Fundamental Analog Circuits*

TxACE 2016-2017 ANNUAL REPORT

The Texas Analog Center of Excellence (TxACE), located at the University of Texas at Dallas is the largest analog research center based in an academic institution. Analog and mixed signal integrated circuits engineering is both a major opportunity and challenge. Analog circuitry is a critical component of nearly every product of the ~$350 billion per year integrated circuits industry, as a part of sensing, actuation, communication, power management and others. Digital integrated circuits such as microprocessors, logic circuits and memories are now integrating analog functions such as input/output circuits, phase locked loops, temperature sensors and power management circuits. It is also common to find microcontrollers with multiple analog-to-digital and digital-to-analog converters. These circuitries impact almost all aspect of modern life: safety security, health care, transportation, energy, entertainment and others.

Creation of advanced analog and mixed signal circuits and systems depends on the availability of engineering talent for analog research and development. TxACE was established to help translate the opportunity into economic benefits by overcoming the challenge and meeting the need. TxACE was established through a collaboration of the state of Texas, Texas Instruments, the Semiconductor Research Corporation, the University of Texas System, and The University of Texas at Dallas.

The research tasks are organized into three research thrust areas: Safety, Security and Health Care, Energy Efficiency and Fundamental Analog. The scope of investigation extends from circuits operating at dc through terahertz, data converters that sample at a few samples/sec to 10's of Giga-samples/sec, AC-to-DC and CD-to-AC converters working at µW to Watts, energy harvesting circuits, sensors and many more. Significant improvements to existing mixed signal systems and new applications have been made and continued to be anticipated. Students who have been exposed to hands-on innovative research are forming the leading edge of analog talent flow into the industry. Close collaboration with and responsiveness to industry needs provide focus to the educational experience.

DIRECTOR'S MESSAGE

The Texas Analog Center of Excellence (TxACE) is leading analog research and education. I am excited to report that the Center has been renewed for another three years and is starting its 10th year of operation this fall. I would like to thank the Semiconductor Research Corporation, Texas Instruments, University of Texas at Dallas and University of Texas System for their confidence and continuing support.

Last year, TxACE researchers published 28 journal and 48 conference papers. We also filed 4 patents and 1 invention disclosure. Twenty-three Ph.D. and four M.S. students have completed their degree program. The Center funded 59 research tasks led by 43 principal investigators at 20 academic institutions, including one international university. Five universities (SMU, Rice, Texas A&M, UT Austin, UT Dallas) were from the state of Texas. The Center supported 132 graduate and undergraduate students.

The Center accomplished much. As always, there are too many to list all here. A selected list includes demonstrations of a RISC-V system-on-chip with integrated voltage regulation and power management implemented in 28-nm FD-SOI with a total system efficiency of 41.8 double-precision GFLOPS/W, a 12-b 330MS/s single-channel pipelined-SAR ADC employing a PVT-stabilized dynamic amplifier as the residue amplifier instead of power hungry opamps that achieves an FoM of 9.5fJ per conversion, and a resonant-based circuit architecture for power isolation with the peak power efficiency of 50.7% and the maximum output power of 62mW, which achieves a 4X efficiency and a 3X power delivery improvement.

The TxACE laboratory is continuing to help advance integrated circuit research by making its instruments and expertise available to researchers and our industrial partners all over the world.

I would like to thank the students, principal investigators and staff for their efforts, and UT Dallas, the University of Texas System, TI, and SRC, as well as many friends of TxACE all over the world for their generous support. As we celebrate our 10th year, I look forward to another year of working with the TxACE team to make our world better through our research, education and innovation.

Kenneth K. O, Director TxACE
Texas Instruments Distinguished
University Chair Professor
The University of Texas at Dallas

BACKGROUND & VISION

The $350 billion per year integrated circuits industry is evolving into an analog/digital mixed signal industry. Analog circuits are providing or supporting critical functions such as sensing, actuation, communication, power management and others. These circuits impact almost all aspect of modern life including safety, security, health care, transportation, energy, and entertainment. To lead this change, in particular to lead analog and mixed signal technology education, research, commercialization, manufacturing, and job creation, the Texas Analog Center of Excellence was announced by Texas Governor Rick Perry in October 2008 as a collaboration of the Semiconductor Research Corporation, state of Texas through its Texas Emerging Technology Fund, Texas Instruments Inc., University of Texas system and University of Texas at Dallas. The Center seeks to accomplish the objectives by creating fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, healthcare, and public safety and security as well as by improving the research and educational infrastructure.

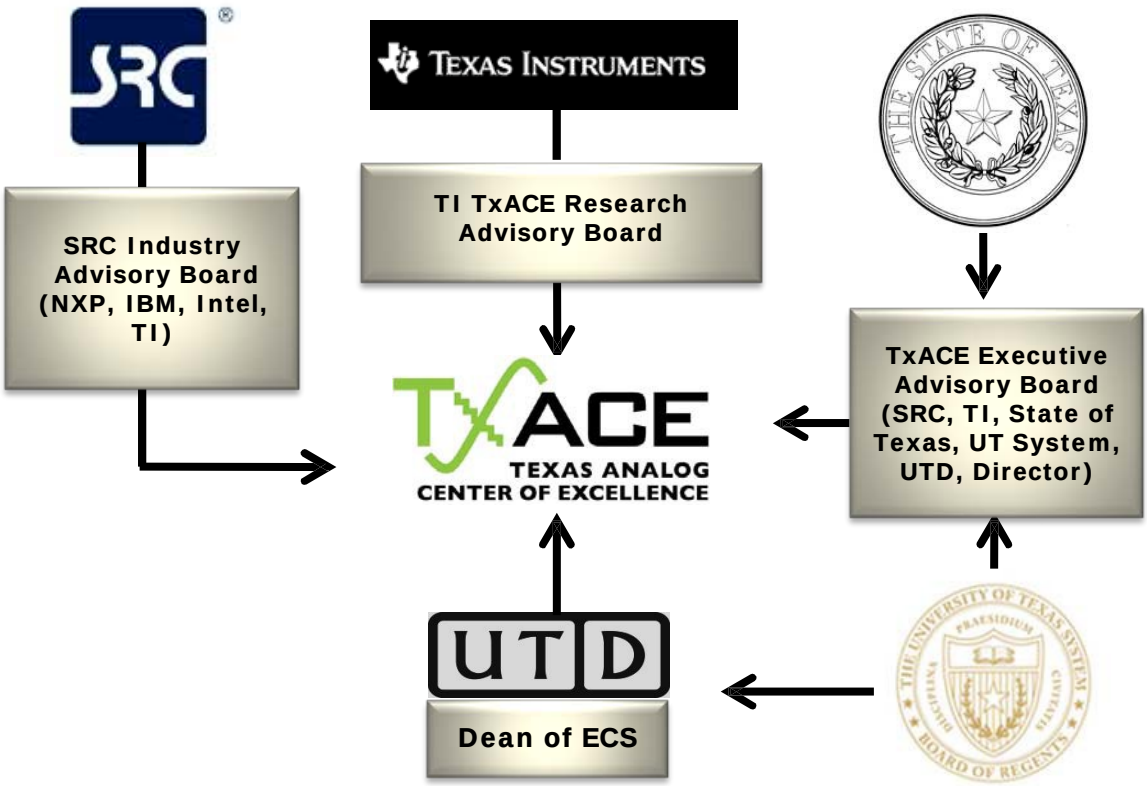


Figure 1. TxACE organization relative to the sponsoring collaboration

CENTER ORGANIZATION

The Texas Analog Center of Excellence is guided by agreements established with the Center sponsors. Members of the industrial advisory boards identify the research needs and select research tasks in consultation with the Center leadership. Figure 1 diagrams the relationship of TxACE to the members of the sponsoring collaboration.

The internal organization of the Center is structured to flexibly perform the research mission while fully embracing the educational missions of the Universities.

Figure 2 shows the center management structure. The TxACE Director is Professor Kenneth O. The research is arranged into three thrusts that comply with the center mission: Safety, Security and Health Care, Energy Efficiency and Fundamental Analog Research. The third thrust consists of vital research that cuts across the first two research thrusts. The thrust leaders are Prof. Brian A. Floyd of North Carolina State University for safety, security and health care, and Prof. Ali Niknejad of the University of California, Berkeley for energy efficiency. The interim leader for fundamental analog is Prof. Michael Flynn of University of Michigan, Ann Arbor. The thrust leaders form the executive committee. The committee, along with the director, forms the leadership team that works to improve the research productivity by increasing collaboration, better leveraging the diverse capabilities of principle investigators of the Center, and lowering research barriers. The leadership team also identifies new research opportunities for consideration by the Industrial Advisory Boards.

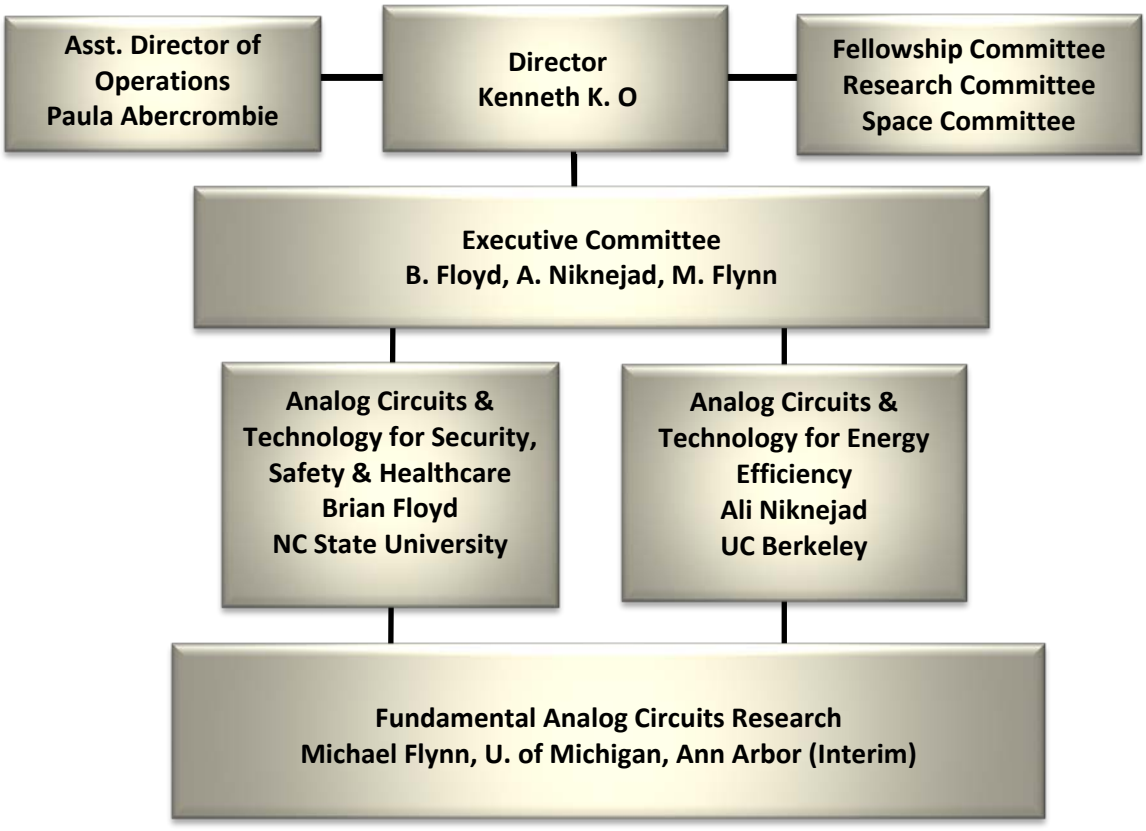


Figure 2. TxACE organization for management of research

PUBLIC SAFETY, SECURITY AND HEALTH CARE

(Thrust leader: Brian Floyd, NC State University)

TxACE is developing analog technology that enhances public safety and security, and health care. The projects are intended to enable a new generation of devices that can scan for harmful substances by researching 200-300 GHz silicon ICs for use in spectrometers as well as a CO_2 sensor. The ICs and CO_2 sensor can also be used to analyze breaths for medical applications. The thrust is also working to significantly reduce the cost of millimeter wave imaging and on-vehicle radar technology for automotive safety by researching circuit techniques that can improve manufacturing, and simplify test and packaging, as well as signal processing techniques that reduce system complexity. Lastly, this thrust is investigating vibration sensors.

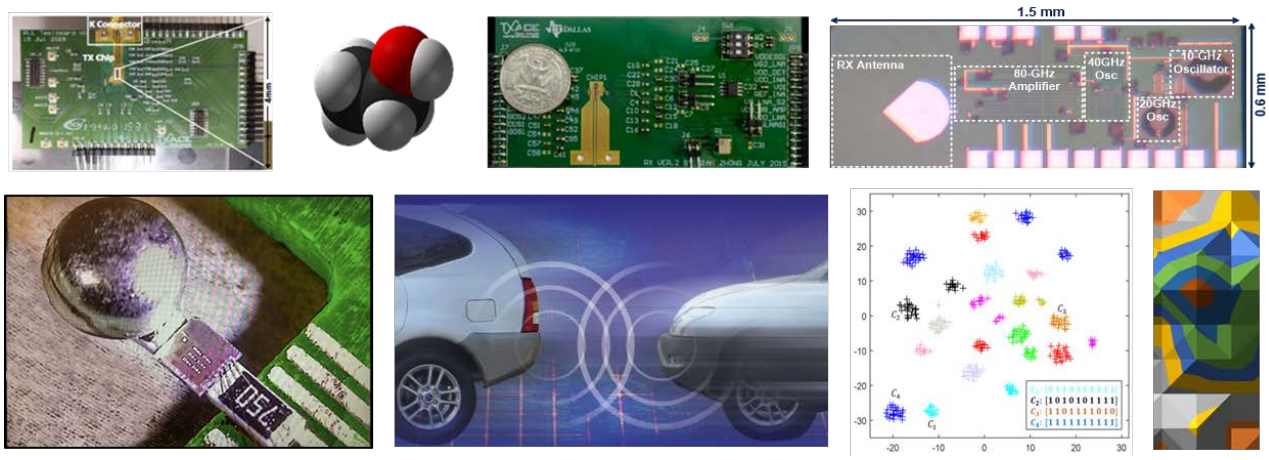


Figure 3. (Top left) 200-260 GHz CMOS transmitter and receiver for rotational spectroscopy (K. O, W. Choi, UT-Dallas), (Top right) Injection-locked receiver for synchronization of widely spaced imaging array (A. Babakhani, Rice U.), (Bottom left) Vibration sensor compatible with conventional silicon IC and packaging technologies (S. Pourkamali, UT Dallas), (Bottom left center) Automotive radar imaging (M. Torlak, UT-Dallas), (Bottom right center) Projected e-test space, where each point represents a wafer. A proper test flow to each process signature of each wafer is assigned to maximize the test cost reduction while maintaining the test escape rate below a target level. (Y. Makris, UT-Dallas), (Bottom right) Magnitude of field inside a dielectric waveguide (D. MacFarlane, SMU).

ENERGY EFFICIENCY

(Thrust leader: Ali Niknejad, UC Berkeley)

TxACE is committed to alleviate the global energy problem by improving the energy efficiency of electronic systems as well as by developing analog technologies that can make energy generation and distribution more efficient. The Center is also working to energize and power long-lasting in-situ microscale devices such as wireless microsensors, biomedical implants, and portable microelectronics.

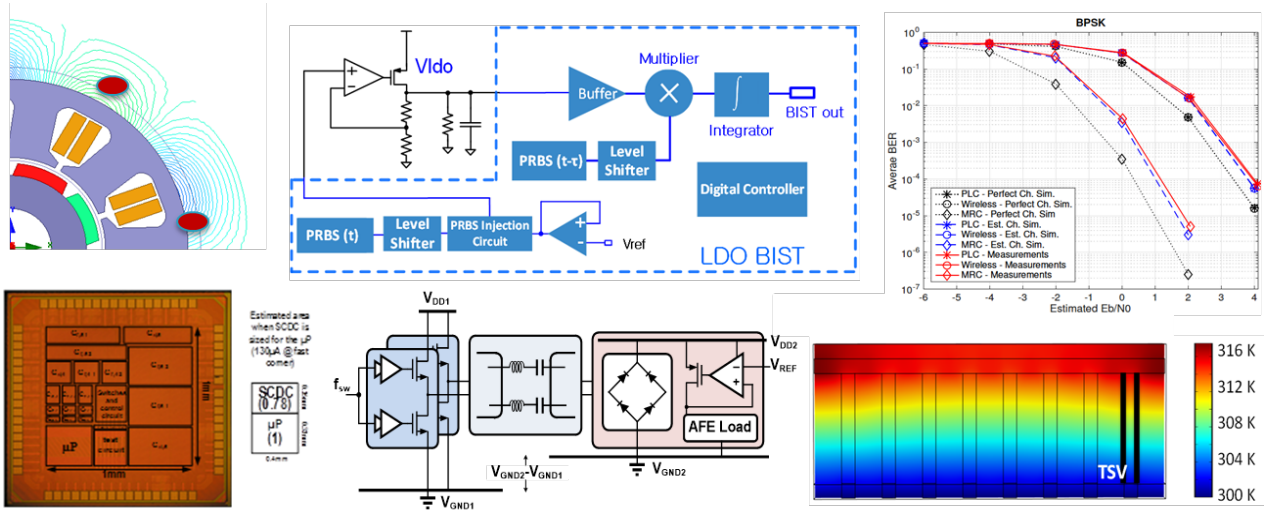


Figure 4. (Top left) Simulated flux leakage in a motor (B. Akin, UT-Dallas), (Top center) Dynamic BIST for LDO's (S. Ozev, Arizona State U.), (Top right) BER versus SNR for PLC/Wireless receiver combining techniques based on maximal-ratio-combining that take into account the impulsive nature of noise on the two links (N. Al-Dhahir, UT-Dallas, B. Evans, UT-Austin), (Bottom left) Microprocessor and switched-capacitor DC-DC converter power management unit based on direct error regulation (M. Seok, Columbia U.), (Bottom center) Resonant converter for isolated power transfer (B. Ma, UT-Dallas), (Bottom right) Simulated cross-sectional temperature distribution in a 8-row TSV arrangement (J. Lee, N. Bagherzadeh, UC-Irvine).

FUNDAMENTAL ANALOG CIRCUITS RESEARCH

(Thrust leader: U. of Michigan Ann Arbor)

Research in this thrust focuses on cross-cutting areas in Analog Circuits which impact all of the TxACE application areas (Energy Efficiency, Public Safety and Security, Health Care). The list of research includes design of a wide variety of analog-to-digital converters, communication links, temperature sensors and I/O circuits, development of CAD tools, and testing of integrated circuits.

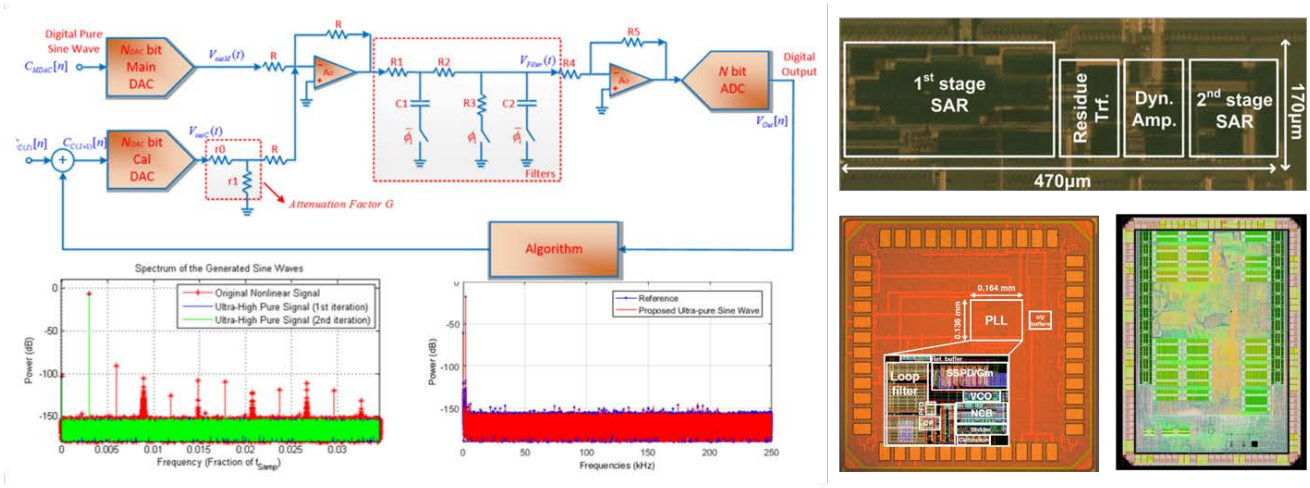


Figure 5. (Left) Low cost ultra-pure sine wave generation with self-calibration. (D. Chen, R. Geiger, Iowa State), (Top right), 12-b 330MS/s single-channel pipelined-SAR ADC (Y. Chiu, UT Dallas), (Bottom center) 2-2.8GHz 65-nm CMOS ring oscillator PLL (P. Kinget, Columbia), (Bottom right) DLL-based clock generation, with phase picking controlled by tunable replica circuits (B. Nikolic).

TXACE ANALOG RESEARCH FACILITY

The centralized group of laboratories of the Texas Analog Center of Excellence dedicated to analog engineering research and training occupies a ~8000 ft^2 area on the 3rd floor of the Engineering and Computer Science North building (Figure 6). The facility includes RF and THz, Integrated System Design, Embedded Signal Processing, and Analog & Mixed Signal laboratories as well as CAD/Design laboratory structured to promote collaborative research**.** The unique instrumentation capability includes network analyses and linearity measurements up to 325 GHz, spectrum analysis up to 120 THz, and cryo-measurements down to 2^oK. The Center also added a pulsed multiple harmonic load and source pull measurement set up (up to 60 GHz for the third harmonic) and a 325-GHz antenna measurement set up. The close proximity of researchers in an open layout enables natural interaction and compels sharing of knowledge and instrumentation among the students and faculty. The TxACE analog research facility is one of the best equipped electronics laboratories. The laboratory is available for use by TxACE researchers and industrial partners all over the world.

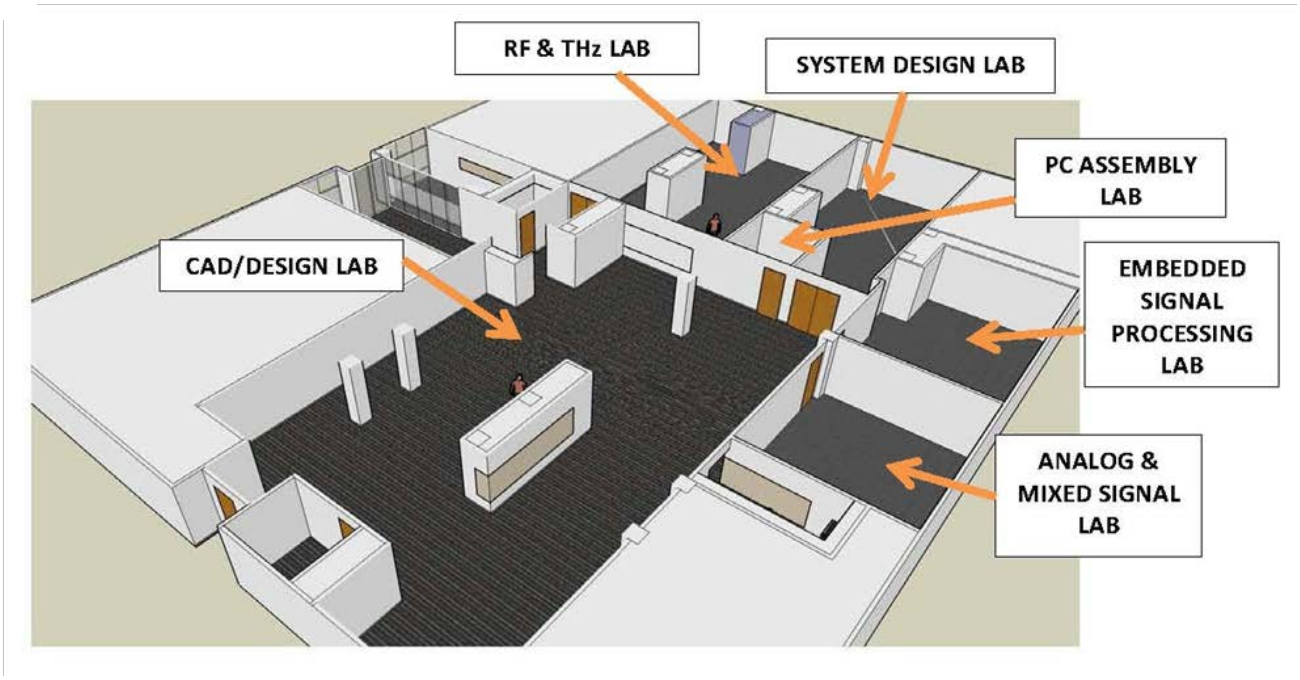


Figure 6. TxACE Analog Research Facility

RESEARCH PROJECTS AND INVESTIGATORS

The Texas Analog Center of Excellence (TxACE) is the largest university analog technology center in the world. Table 1 lists the current principal investigators of the 59 tasks from 20 academic institutions funded by TxACE. Five universities (Rice, SMU, Texas A&M, UT Austin, UT Dallas) are from the state of Texas. Fourteen are from outside of Texas. One (Seoul National University) (Figure 7) is from outside of the US. Of the 43 investigators, 18 are from Texas. During the past year, the Center supported 104 Ph.D., 16 M.S., and 12 B.S. students. Twenty-three Ph.D. and four M.S. degrees were awarded to the TxACE students.

Investigator	Institution	Investigator	Institution	Investigator	Institution
B. Akin	UT Dallas	R. Harjani	U Minnesota	A. Niknejad	UC Berkeley
N. Al-Dhahir	UT Dallas	R. Henderson	UT Dallas	B. Nikolić	UC Berkeley
A. Babakhani	Rice U	C. Kim	U Minnesota	K. O	UT Dallas
D. Blaauw	U Michigan	J. Kim	Seoul Nat.	S. Ozev	Arizona State
A. Chatterjee	Georgia Tech	P. Kinget	Columbia	S. Palermo	Texas A&M
D. Chen	Iowa State	H. Lee	UT Dallas	S. Pourkamali	UT Dallas
Z. Chen	U Arkansas	J. Lee	UC Irvine	S. Prasad	UT Dallas
Y. Chiu	UT Dallas	M. Lee	UT Dallas	A. Raychowdhury	Georgia Tech
W. Choi	UT Dallas	P. Li	Texas A&M	E. Rosenbaum	UIUC
F. De Lucia	Ohio State	D. Ma	UT Dallas	V. Sathe	U Washington
W. Eisenstadt	U Florida	D. MacFarlane	SMU	M. Seok	Columbia
B. Evans	UT Austin	N. Maghari	U Florida	G. Temes	Oregon State
M. Flynn	U Michigan	Y. Makris	UT Dallas	M. Torlak	UT Dallas
R. Geiger	Iowa State	U.-K. Moon	Oregon State		
P. Hanumolu	UIUC	S. Mukhopadhyay	Georgia Tech		

Table 1. Principal Investigators (September 2016 through August 2017)

Figure 7. Member Institutions of Texas Analog Center of Excellence

SUMMARY OF RESEARCH PROJECTS

The 59 research projects funded through TxACE during 2016-2017 are listed in Table 2 below by the Semiconductor Research Corporation task identification number.

Table 2: Funded research projects at TxACE by SRC task identification number (FA: Fundamental Analog, EE: Energy Efficiency, SSH: Safety, Security and Health Care)

	Task	Thrust	Title	Task Leader	Institution
1	1836.096	FA	Mixed-Signal Design Centering in Deeply Scaled Technologies	Nikolić, Borivoje	UC Berkeley
2	1836.110	EE	Distributed Power Delivery Architecture for 2D and 3D Integrated Circuits	Mukhopadhyay, Saibal	Georgia Tech
3	1836.111	FA	Advanced ADC-Based Serial Link Receiver Architectures	Palermo, Samuel	Texas A&M
4	1836.112	EE	Shortstop: Fast Power Supply Boosting for Energy-Efficient, High-Performance Processors	Blaauw, David	Univ. of Michigan
5	1836.117	FA	Performance and Reliability Enhancement of Embedded ADCS with Value-Added BIST	Geiger, Randall	Iowa State
6	1836.119	SSH	Demonstration of 180-300 GHz Transmitter for Rotational Spectroscopy	O, Kenneth	UT Dallas
7	1836.120	SSH	Evaluation of Frequency and Noise Performance of CMOS 180-300 GHz Spectrometer Transmitter and Receiver Components	Lee, Mark	UT Dallas
8	1836.122	SSH	On-Chip Integration Techniques for 180-300 GHz Spectrometers	Henderson, Rashaunda	UT Dallas
9	1836.124	EE	Digitally-Enhanced Clocking Strategies to Improve Energy-Efficiency of Serial Links	Hanumolu, Pavan Kumar	UIUC
10	1836.125	FA	10GS/s+ Resolution-Scalable (4-7bits) ADCs	Flynn, Michael	Univ. of Michigan
11	1836.126	SSH	Design Spin Reduction via Integrated THz Design: Applications, Physics, and System Engineering	De Lucia, Frank	Ohio State
12	1836.127	FA	Precision Test without Precision Instruments – A Necessity for Future On-Chip Self-Test and Self Healing	Chen, Degang	Iowa State
13	1836.128	FA	Statistical Analog Design Property Checking	Li, Peng	Texas A&M
14	1836.129	FA	Energy-Efficient Digitally-Enhanced Rapid ON/OFF Links in Nano-scale CMOS	Hanumolu, Pavan Kumar	UIUC
15	1836.130	EE	Built-In Self-Test Techniques for Test, Calibration, and Trimming of Power Management Units: PMU-BIST	Ozev, Sule	Arizona State
16	1836.131	SSH	Process Variation Anatomy: A Statistical Nexus Between Design, Manufacturing, and Yield	Makris, Yiorgos	UT Dallas

	Task	Thrust	Title	Task Leader	Institution
17	1836.132	FA	Fault Coverage Analysis of Analog/Mixed-Signal Tests Based on Statistical Dissimilarity	Kim, Jaeha	Seoul National Univ.
18	1836.133	EE	Energy-Efficient Signal Processing Techniques for Smart Grid Heterogeneous Communications Networks	Al-Dhahir, Naofal	UT Dallas
19	1836.134	FA	Hybrid Two-Step PLLs for Digital SoCs in Nanoscale CMOS	Kinget, Peter	Columbia
20	1836.135	SSH	Sub-Picosecond Synchronization of Widely Spaced Imaging Arrays	Babakhani, Aydin	Rice Univ.
21	1836.136	FA	Injection-Locked Ring Oscillators for Clock Distribution in Manycore Processors	Nikolić, Borivoje	UC Berkeley
22	1836.137	FA	50GS/s and Beyond Frequency-interleaved Energy-Efficient ADCs	Niknejad, Ali	UC Berkeley
23	1836.138	EE	Micro-Power Analog-to-Digital Data Converters	Temes, Gabor	Oregon State Univ.
24	1836.139	EE	Enabling Fully-Integrated VHF CLK-Sync Multiphase Switching Regulators on Silicon	Ma, Dongsheng	UT Dallas
25	1836.140	EE	Embedded & Adaptive Voltage Regulators with Proactive Noise Reduction for Digital Loads Under Wide Dynamic Range	Raychowdhury, Arijit	Georgia Tech
26	1836.141	FA	IC Design for Resilience Against System-Level ESD	Rosenbaum, Elyse	UIUC
27	1836.142	EE	Low Power Applications of FRAM	Blaauw, David	Univ. of Michigan
28	1836.143	EE	Design Techniques for Modulation-Agile and Energy-Efficient 60+Gb/s Receiver Front-Ends	Palermo, Samuel	Texas A&M
29	1836.144	EE	High-efficiency High-voltage Power Converters	Lee, Hoi	UT Dallas
30	1836.145	FA	RF and Mixed Signal Quantum CMOS Devices and Circuits	Lee, Mark Chiu, Yun	UT Dallas
31	1836.146	EE	On-Chip AC-DC Power Conversion with Ground Disturbance Shielding for Environmental Sensing Applications	Ma, Dongsheng	UT Dallas
32	1836.147	SSH	Demonstration of 180-300 GHz Receiver for Rotational Spectroscopy	Choi, Wooyeol	UT Dallas
33	1836.148	FA	50GSPS+ TI Hybrid SAR ADC Array with Comprehensive DDI Calibration	Chiu, Yun	UT Dallas
34	1836.149	EE	Condition Monitoring of PM/IPM Motors through Axial/Radial Leakage Flux	Akin, Bilal	UT Dallas
35	1836.150	SSH	Robust High Resolution Techniques for Millimeter Wave Radars in Complex Environments	Torlak, Murat	UT Dallas
36	1836.152	SSH	Feasibility of CMOS Transmitter and Receiver for 500-Gbps Communication over Dielectric Waveguide	O, Kenneth K.	UT Dallas
37	1836.153	EE	High-Speed Compact Power Supplies For Ultra-Low-Power Wireless Sensor Applications	Ma, Dongsheng	UT Dallas
38	1836.154	EE	State of The Health (SOH) for IGBTS: Incipient Fault Characterization and Degradation Monitoring	Akin, Bilal	UT Dallas

	Task	Thrust	Title	Task Leader	Institution
39	1836.155	SSH	Development of Wideband Vibration Sensors Based On Existing Process Platforms	Pourkamali, Siavash	UT Dallas
40	1836.156	SSH	Transition Design for High Data Rate Links at Submillimeter Wave Frequencies	Henderson, Rashaunda	UT Dallas
41	1836.157	FA	CMOS GSPS 12-Bit SAR ADC Array With On-Chip Reference Buffers	Chiu, Yun	UT Dallas
42	1836.158	SSH	Development of Dielectric Waveguides for THz Radiation Applications	Macfarlane, Duncan	SMU
43	1836.159	SSH	Performance of Carbon Dioxide (CO(2)) Gas Sensors	Prasad, Shalini	UT Dallas
44	2712.002	EE	On-line Self-Testing and Self-Tuning of Integrated Voltage Regulators	Mukhopadhyay, Saibal	Georgia Tech
45	2712.003	FA	Multi-Modal BIST Design and Test Metrics Evaluation for Analog/RF Circuits	Ozev, Sule	Arizona State
46	2712.004	FA	Hierarchical Analog and Mixed-Signal Verification Using Hybrid Formal and Machine Learning Techniques	Li, Peng	Texas A&M
47	2712.005	FA	Automated Cross-Level Validation and Debug of Mixed-Signal Systems in Top-Down Design: From Pre-Silicon to Post-Silicon	Chatterjee, Abhijit	Georgia Tech
48	2712.006	EE	Robust, Efficient All-Digital SIMO Converters for Future SOC Domains	Sathe, Visvesh	U Washington
49	2712.007	FA	High-Resolution Low-Voltage Hybrid ADCs for Sensor Interfaces	Flynn, Michael P.	U Michigan
50	2712.008	EE	Direct-Battery-to-Silicon Power Transfer in Advanced Nanometer CMOS	Harjani, Ramesh	U Minnesota
51	2713.009	EE	Low Power Area Efficient Flexible-rate Energy Proportional Serial Link Transceivers	Hanumolu, Pavan Kumar	UIUC
52	2712.010	FA	Ringamp-assisted Circuits/Techniques and Next-generation Ringamps	Moon, Un-Ku	Oregon State
53	2712.011	FA	Robust Reliable and Practical High Performance References in Advanced Technologies	Geiger, Randall L.	Iowa State
54	2712.012	EE	EDAC and DC-DC-Converter Co-Design for Addressing Robustness Challenges in Emerging Architectures	Seok, Mingoo	Columbia
55	2712.014	FA	Leveraging CMOS Scaling in High Performance ADCS	Maghari, Nima	U Florida
56	2712.015	FA	Area-Efficient On-Chip System-Level IEC ESD Protection for High Speed Interface ICs	Chen, Zhong	U Arkansas
57	2712.016	EE	3D IC Thermal Management Based on TSV Placement Optimization and Novel Materials	Lee, Jaeho	UC Irvine
58	2712.017	FA	Mitigating Reliability Issues in Analog Circuits	Kim, Chris H.	U Minnesota
59	2712.018	EE	Test Techniques to Approach Several Defect-per-billion for Power ICs	Eisenstadt, William	U Florida

ACCOMPLISHMENTS

In the past year, TxACE has made significant research progress. Table 3 summarizes the number of publications and inventions resulting from the TxACE research during May 2016 to April 2017, while Table 4 lists the major research accomplishments for the Center during the period. The TxACE researchers have published 48 conference papers and 29 journal papers. They have also filed one invention disclosure and 4 patents. The list of publications is included as Appendix I. Following the tabulation, brief summaries of each project are provided.

Table 3. TxACE number of publications (May 2016 through April 2017)

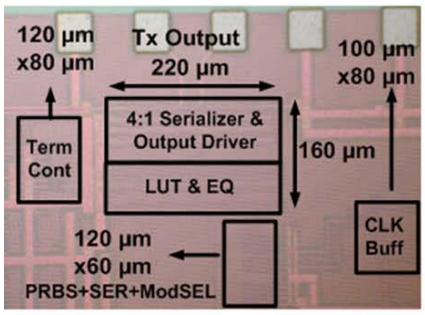
Conference Papers	Journal Papers	Invention Disclosures	Patents Filed	Patents Granted
48	28	1	4	0

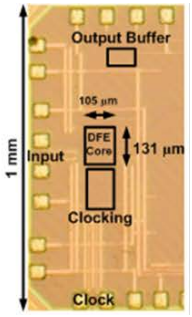
Table 4. Major TxACE Research Accomplishments (May 2016 through April 2017)

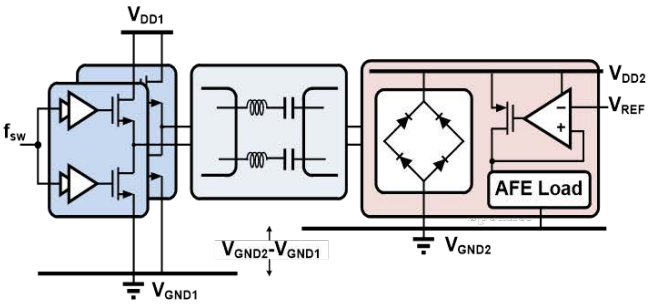
Category	Accomplishment
Fundamental Analog (Circuits)	A RISC-V system-on-chip with integrated voltage regulation and power management is implemented in 28-nm FD-SOI. A fully integrated switched-capacitor DC-DC converter, coupled with an adaptive clocking system, achieves 82-89% system conversion efficiency across a wide operating range, yielding a total system efficiency of 41.8 double-precision GFLOPS/W. (1836.136, PI: B. Nikolic, UC-Berkeley)
Fundamental Analog (Circuits)	A 12-b 330MS/s single-channel pipelined-SAR ADC employs a PVT-stabilized dynamic amplifier as the residue amplifier instead of opamp-based residue amplifiers that consume significant amounts of power due to stringent settling speed and accuracy requirements. The ADC fabricated in 65-nm CMOS with a core area of 0.08mm^2 achieves an FoM of 9.5fJ per conversion. The measured DNL and INL are +0.67/-0.56LSB and +0.7/-0.8LSB, respectively. The measured SNDR remains above 60dB even with a 500-MHz input. (1836.157, PI: Y. Chiu, UT-Dallas)
Fundamental Analog (Circuits)	A 2-2.8GHz 65-nm CMOS ring oscillator PLL occupies an active area of 0.022 mm^2, consumes 5.86mW, and achieves a 633fs RMS jitter at 2.36 GHz and an FOM$_{jitter}$ of -236 dB. It implements a low-overhead feed-forward phase and supply-noise cancellation scheme by leveraging the noise extraction inherently done by the sub-sampling phase detector. Cancellation reduces the jitter by 1.4X, the phase noise by 10.2dB to -123.5dBc/Hz at a 300KHz offset, and the ring oscillator supply sensitivity by 19.5dB for a 1-mV$_{p-p}$ 100KHz supply noise tone. (1836.134, PI: P. Kinget, Columbia University)
Energy Efficiency (Circuits)	High-speed serial link receiver design and modeling techniques are proposed to significantly improve interconnect bandwidth density in an energy-efficient manner. A statistical link modeling tool was utilized to investigate the optimal equalization partitioning and modulation format for 60+Gb/s signaling environments. A dual-mode NRZ/PAM4 SerDes was implemented in GP 65-nm CMOS and achieved 16Gb/s NRZ and 32Gb/s PAM4 operation at 10.9 and 5.5mW/Gb/s, respectively. (1836.143, PI: S. Palermo, Texas A&M University)

Category	Accomplishment
Energy Efficiency (Circuits)	Capacitive isolation is used to eliminate the bulky magnetics for highly power efficient on-silicon AC-DC power conversion for environmental sensor applications that is resilient to ground voltage disturbance. However, the low density on-chip capacitor and large parasitics limit the output power level and efficiency. A resonant-based circuit architecture for power isolation with the peak power efficiency of 50.7% and the maximum output power of 62mW is demonstrated. This design achieves a 4X efficiency and a 3X power delivery improvement over the prior art. (1836.146, PI: Brian Ma, UT-Dallas)
Safety, Security and Health Care (Systems)	Terahertz spectrometers can be used for a variety of applications including process monitoring and gas detection. A terahertz spectrometer has been used within an Applied Materials plasma reactor for process diagnostics. Studies have been completed which show that the spectrometer can accurately measure densities of plasma constituents for a number gas mixtures including CF_2, FCN, HCN, CO and others. (1836.126, Frank C. DeLucia, Ohio S. U.)

Energy Efficiency Thrust







Category	Accomplishment
Energy Efficiency (Circuits)	High-speed serial link receiver design and modeling techniques are proposed to significantly improve interconnect bandwidth density in an energy-efficient manner. A statistical link modeling tool was utilized to investigate the optimal equalization partitioning and modulation format for 60+Gb/s signaling environments. A dual-mode NRZ/PAM4 SerDes was implemented in GP 65-nm CMOS and achieved 16Gb/s NRZ and 32Gb/s PAM4 operation at 10.9 and 5.5mW/Gb/s, respectively. (1836.143, PI: S. Palermo, Texas A&M University)
Energy Efficiency (Systems)	Techniques to improve the rate, reliability, and energy efficiency of two-way between smart meters & data concentrators in smart grids using both narrow band power line communication (NB-PLC) and wireless communication are proposed. The narrowband (NB)-PLC/Wireless receiver diversity techniques improves the performance by exploiting the statistics of the impulsive noise in PLC. A new cyclostationary model for the NB-PLC noise based on frequency-shift (FRESH) filtering can be used to improve SNR by ~4dB. (1836.133, PIs: N. Al-Dhahir, UT-Dallas and B. L. Evans, UT-Austin)
Energy Efficiency (Circuits)	This project explores the circuit architecture and operation scheme for achieving highly power efficient on-silicon AC-DC power conversion in environmental sensor applications that is resilient to ground voltage disturbance. Capacitive isolation eliminates the bulky magnetics. However, the low density on-chip capacitor and large parasitics limit the output power level and efficiency. A resonant-based circuit architecture for power isolation with the peak power efficiency of 50.7% and the maximum output power of 62mW is demonstrated. This design achieves a 4X efficiency and a 3X power delivery improvement over the prior art. (1836.146, PI: Brian Ma, UT-Dallas)

TASK 1836.110, DISTRIBUTED POWER DELIVERY ARCHITECTURE FOR 2D AND 3D INTEGRATED CIRCUITS

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SIGNIFICANCE AND OBJECTIVES

The primary objective is to design a low-loss, fully integrated, and robust distributed Power Delivery Unit for multicore processors targeting low output voltage from relatively high input voltage. The central innovation is a hybrid down conversion architecture composed of a central switched capacitor (SC) converter and multiple distributed inductive buck (IB) converter.

TECHNICAL APPROACH

The key technical approach include design of the hybrid converter stage connecting switched capacitor back-end and inductive buck front-end. The key effort of last year focused on the optimizing the design of the buck stage. A single-inductor-multiple-output based buck stage was designed and integrated (off-chip) with the SC stage. We have also designed a two-phase buck stage. Finally, a very high-frequency buck stage was designed as well with fully-digital control and resistive assist based transient management circuits.

SUMMARY OF RESULTS

Design of a hybrid converter: A step down converter consisting of a switched capacitor stage followed by an inductive buck stage is designed. The SC converter is designed to produce a 4:1 down conversion from an unregulated 4.8V DC supply. The output of the switched capacitor is then fed to the feedback controlled inductive buck regulator. The buck regulator is designed in synchronous current mode control with load dependent variable frequency operation. The load current is sensed and after removal of high frequency components is fed to the oscillator that produces pulses proportional to the DC load current. The duty cycle can be adjusted to maximize the overall efficiency, by impedance matching among the load, buck converter and the switch capacitor converter. A test-chip is designed and taped-out in 130nm CMOS to study the characteristics of the hybrid converter. The test-chip includes on-chip decoupling capacitors to minimize the effect of high-frequency noise due to bond-wires. The maximum conversion ratio designed to be 16.

Single-Inductor-Multiple-Output (SIMO): We have presented a SIMO module that enables smaller passives for a given output power. First, Continuous Conduction Mode (CCM) operation is utilized to deliver higher output power for a smaller inductance; the cross-regulation in CCM operation is suppressed using a novel power-weighted CCM controller. Second, a modified power stage filter is presented using floating capacitors that utilizes Miller effect to reduce switching frequency of the output while maintaining power quality. The design is demonstrated through a 130nm CMOS test-chip that generates 4 outputs. The measurements demonstrate a 20MHz operation of the power stage with 500nH inductor and 1μF total load capacitance. DVS speed of 120mV/μs, and 73% peak efficiency at a load of 40mA are measured.

High-frequency Buck Regulator: We have designed a bond-wire inductance and on-die capacitance based high-frequency Integrated Voltage Regulator (IVR) with multi-sampled digital controller. We have also presented a resistive transient assist (RTA) circuit that utilizes multisampling and bypasses the control loop to provide charges to the output directly from input, thereby improving load and reference transients. An all-digital DCM mode and FET segment control are also included to improve low load efficiency. A 130nm CMOS test-chip demonstrates a 125MHz IVR with 250MHz compensator. The RTA circuit shows up to 2.5 x enhancements in transient settling times.

Keywords: Integrated converters, hybrid conversion, efficiency, high conversion ratio, packaging

INDUSTRY INTERACTIONS

Intel, IBM, Texas Instruments.

MAJOR PAPERS/PATENTS

[1] S. Carlo, et. al., “A High Power Density, Dynamic Voltage Scaling Compatible, Single-Inductor Four-Output Regulator using a Power-Weighted CCM Controller and a Floating Capacitor-Based Output Filter,” IEEE TPE, Vol.31, No.6, June 2016, pp. 4252-4264.

[2] M. Kar, et. al, “A Scalable Hybrid Regulator for Down Conversion of High Input Voltage Using Low Voltage Devices,” IEEE TPE, March 2016.

[3] M. Kar, et. al. “An Integrated Inductive VR with a 250MHz All-Digital Multisampled Compensator and on-Chip Auto-Tuning of Coefficients in 130nm CMOS.” ESSCIRC, 2016.

[4] M. Kar, et. al, “Impact of the Process Variation in Inductive Integrated Voltage Regulator on Delay and Power of Digital Circuits,” ISLPED, 2014.

[5] S. Carlo, et. al., “On the Potential of 3D Integration of Inductive DC-DC Converter for High-Performance Power Delivery,” DAC, June 2013.

TASK 1836.112, SHORTSTOP: FAST POWER SUPPLY BOOSTING FOR ENERGY-EFFICIENT, HIGH-PERFORMANCE PROCESSORS

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SIGNIFICANCE AND OBJECTIVES

A novel core supply boosting technique, called Shortstop, is proposed as an alternative to on-chip regulators, which require expensive inductors. Instead Shortstop leverages the innate parasitic inductance of a dedicated dirty supply rail in a boost converter-type arrangement, along with an on-chip boost capacitor.

TECHNICAL APPROACH

Figure 1 shows the high-level steps of Shortstop. On the first step Shortstop energizes the parasitic inductance of a wirebond pad by shorting it to ground. Simultaneously, an initial pre-boost of charge is delivered to the core through an on-chip boost capacitor. During step 2, the energized inductor is connected to the core (modeled as a decoupling capacitor), quickly raising the core's supply rail towards the target high voltage. Finally, once the core has reached its target high voltage any remaining charge in the parasitic inductance is used to charge the on-chip boost capacitor.

SUMMARY OF RESULTS

Figure 2 shows silicon measurements comparing boosting latency, as measured from when a boost is requested by the assertion of a 'go' signal to completing the boost, for the included M3 core using a baseline PMOS header based approach and Shortstop. The 1-pin baseline assumes Shortstop's hardware overhead can be amortized across multiple cores and hence is negligible, while the 2-pin baseline is a conservative estimate where the number of dirty supply pins equals the number of high supply pins. Vcore is the on-chip core supply net, as seen by the core being boosted. Vhigh is the clean "high voltage mode" supply net that could be shared among additional cores.

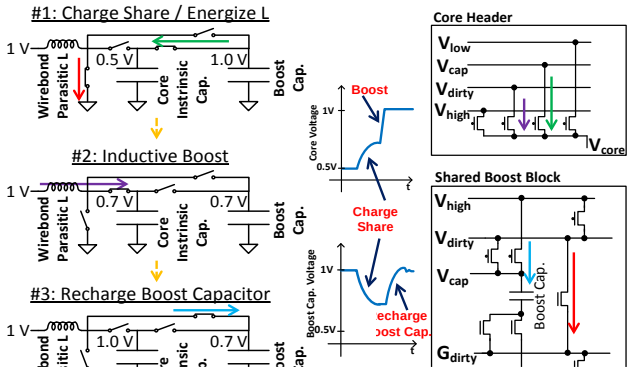

Figure 1. Overview of Shortstop concept.

Modern processors, both high-performance and mobile, are packaged using flip-chip and not wirebonded. Instead of thin wires with relatively high inductance, flip-chip packaging uses bumps to connect high-density power and I/O signals to a substrate or circuit board. Because Shortstop leverages the parasitic inductance of a package, demonstration in flip-chip, with its lower parasitic inductance, is necessary. We propose an evolution of the first Shortstop prototype that includes flip-chip power delivery, improved boost topology, and an automated tuning algorithm to calibrate delay generators used with the boosting technique. Measured results in 40nm are given in [1].

Shortstop is demonstrated in 28nm wirebond and 40nm flip-chip implementations. In 28nm it boosts a 3nF core from 0.4V to 1.0V in 26ns while maintaining acceptable supply voltage droop. This boost latency is 1.8× faster than a header-based approach, while reducing supply droop by 2-7×, and can be used in near-threshold computing to overcome serial code bottlenecks. The 40nm version is capable of boosting Shortstop boosts a 2.7mm^2 core from 0.5V to 0.75V in 14ns with 27mV of droop on a shared 0.8V supply rail, marking a 57% faster transition with 67% lower supply noise than a dual-supply PMOS header design.

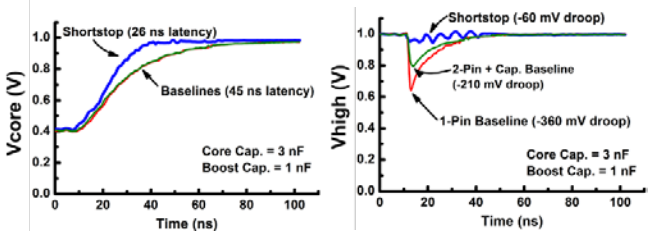

Figure 2. QFN measured results.

Keywords: DVFS, low power, CMOS, digital, microprocessor

INDUSTRY INTERACTIONS

IBM, Intel, Texas Instruments

MAJOR PAPERS/PATENTS

[1] N. Pinckney, D. Sylvester, and D. Blaauw, "Supply boosting for high-performance processors in flip-chip packages," *IEEE Europ. Solid-State Circuits Conf*, 2016.

[2] N. Pinckney, M. Fojtik, B. Giridhar, D. Sylvester, and D. Blaauw, "Shortstop: An on-chip fast supply boosting technique," *IEEE Symp. VLSI Circuits*, 2013.

TASK 1836.124, DIGITALLY-ENHANCED CLOCKING STRATEGIES TO IMPROVE ENERGY-EFFICIENCY OF SERIAL LINKS

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SIGNIFICANCE AND OBJECTIVES

Proposed research presents the first fractional-N injection-locked clock multiplier that achieves the lowest power and jitter and hence the best figure-of-merit among all the reported fractional-N synthesizers.

TECHNICAL APPROACH

The idea behind the proposed fractional-N ILCM can be understood by considering the case of multiplication factor of 4.25 (N=4, α=0.25) and the oscillator is initially set to oscillate at $4.25F_{REF}$. Noting that the oscillator accumulates an additional phase of $0.25T_{OSC}$ every reference cycle, phase error between reference clock and oscillator output can be made zero by adding the same amount of phase shift to the reference clock as well. To this end, as depicted in Fig. 1, a digitally controlled delay line (DCDL) controlled by DCW is introduced. Gain of the DCDL must be calibrated as described in [1].

SUMMARY OF RESULTS

A prototype fractional-N ILCM is implemented in a 65nm CMOS technology and occupies an active area of $0.27mm^2$. At 8GHz, it consumes 3.25mW in fractional-N mode and 2.65mW in integer-N mode from a 0.9V supply, of which the DCO and its buffer consume less than 2.2mW. The performance of the ILCM is characterized using an external 125MHz reference clock that has about $190fs_{rms}$ integrated jitter from 10kHz to 30MHz. Figure 4 shows the measured phase noise plots at 8GHz output frequency. In integer-N mode, integrated jitter is about $104fs_{rms}$. In fractional-N mode, the in-band phase noise is better than -107dBc/Hz at 100kHz offset frequency (Fig. 2). The integrated jitter is about $203fs_{rms}$ and $240fs_{rms}$ when the fractional spur is out-of-band and in-band, respectively. The proposed ILCM achieves the best power efficiency of 0.44mW/GHz and the first reported fractional-N clock multiplier with rapid on/off capability. It also achieves the best-reported FoM of -255dB (integer-N) and -247dB (fractional-N).

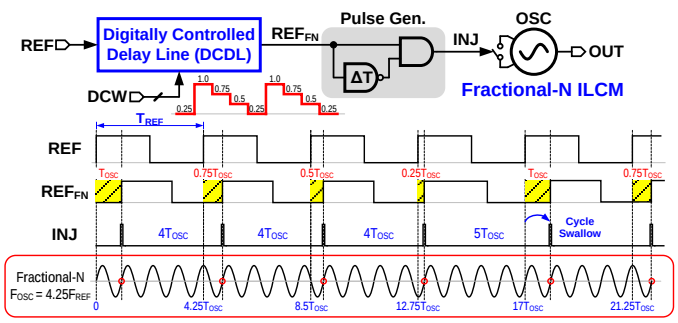

Figure 1. Block diagram of fractional-N injection locked clock multiplier.

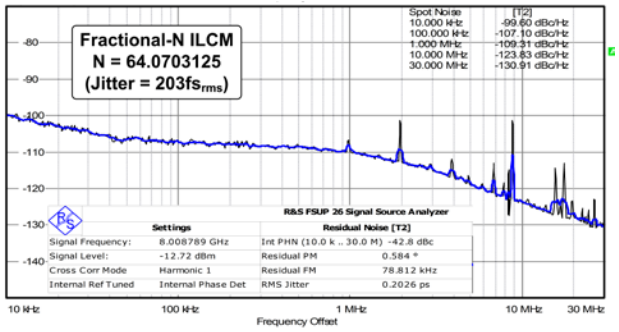

Figure 2. Measured phase noise plot.

Keywords: fractional-N frequency synthesis, low power

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] A. Elkholy, A. Elmallah, M. Elzeftawi, K. Chang, and P. Hanumolu, "A 6.75-to-8.25 GHz, $250fs_{rms}$ integrated- jitter 3.25 mW rapid on/off PVT-insensitive fractional-N injection-locked clock multiplier in 65nm CMOS," in IEEE ISSCC Dig. Tech. Papers, Feb. 2016, pp. 192-193.

TASK 1836.130, BUILT-IN SELF-TEST TECHNIQUES FOR TEST, CALIBRATION, AND TRIMMING OF POWER MANAGEMENT UNITS: PMU-BIST

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SIGNIFICANCE AND OBJECTIVES

This project aims at (a) enabling trimming and calibration of PMU/PMICs through static measurements using small footprint BIST circuitry, (b) enabling dynamic testing through open-loop measurements and mathematical modeling, (c) fault analysis and grading approaches to identify design and layout issues, and (d) correlating trim coefficients with measurements.

TECHNICAL APPROACH

We have divided this problem into two parallel threads. First, our goal was to implement a very small foot-print, low frequency analog to digital converter that works in a particular voltage range (1-1.4V) and provides 10 bits of resolution (INL<1mV). Another goal was to implement a dynamic built-in-self-test system for the converter loop to test phase margin in order to evaluate loop stability.

SUMMARY OF RESULTS

The zoom-in ADC was designed and taped out at TI India in 2016. Figure 1 shows the results from the zoom-in ADC. The INL of the ADC is below the target 1mV for window sizes below 100mV. This would indicate a 2-step conversion for the ADC. The overall measurement time is 100ms per DC measurement.

The dynamic BIST system is shown in Figure 2. All of the system components are implemented in 40-nm GF technology and taped out at NXP, Austin, TX. The overall area of the BIST circuit is 0.019mm^2 and the evaluation time is 20ms. Figure 3 shows the comparison of the BIST circuit response at various load current values to a more traditional technique for phase margin evaluation.

INL(mV)		
100mV	200mV	300mV
0.052728774	0.101196247	0.151964231
0.051742842	0.100101595	0.151045837
0.094101648	0.178332401	0.253850356
0.094286797	0.178578628	0.254121085

Figure 1. INL of the zoom-in VCO for 100mV, 200mV, and 400mV zoom window at two different temperatures (25°C shown in pink and 85°C shown in orange). Measurements are taken at Texas Instruments, India.

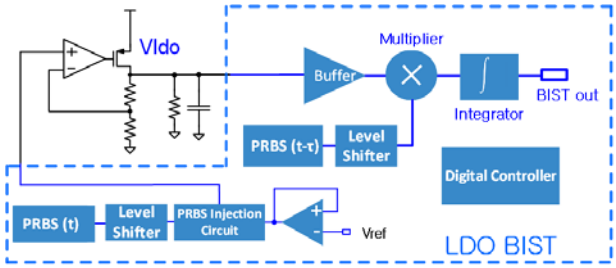

Figure 2. Dynamic BIST for LDO's.

Iload (mA)	BIST	Loop Analysis
20	60^0	59^0
30	51^0	50.5^0
40	44^0	45^0
50	40.2^0	40.7^0

Figure 3. BIST results compared with loop analysis for phase margin.

Keywords: BIST, PMU, phase margin, bandgap reference

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

[1] Navankur Beohar, Priyanka Bakliwal, Sidhanto Roy, Debashis Mandal, Bertan Bakkaloglu, Sule Ozev, "Disturbance-free BIST for Loop Characterization of DC-DC Buck Converters", IEEE VLSI Test Symposium, 2015. (Received best paper honorable mention award)

[2] Osman Emir Erol, Sule Ozev, Chandra Suresh, Rubin Parekhji, and Lakshmanan Balasubramanian. "On-chip measurement of bandgap reference voltage using a small form factor VCO based zoom-in ADC." IEEE Design, Automation & Test in Europe Conference, pp. 1559-1562, 2015.

[3] Liu, Tao, Chao Fu, Sule Ozev, and Bertan Bakkaloglu. "A built-in self-test technique for load inductance and lossless current sensing of DC-DC converters." IEEE VLSI Test Symposium (VTS), 2014. (Received Best paper award)

TASK 1836.133, ENERGY-EFFICIENT SIGNAL PROCESSING TECHNIQUES FOR SMART GRID HETEROGENEOUS COMMUNICATION NETWORKS

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BRIAN L. EVANS, UNIVERSITY OF TEXAS AT AUSTIN

SIGNIFICANCE AND OBJECTIVES

Smart Grids are supported by heterogeneous networks that employ both wireless and powerline communication (PLC) technologies since no single solution fits all scenarios. We propose a reliable hybrid power line and wireless communication transceiver for Smart Grids.

TECHNICAL APPROACH

We focus on the last mile communication link between the utility data concentrator and the residential smart meter. The transceiver is implemented over power lines in the narrowband 3-500 kHz frequency band and also over the unlicensed wireless frequency band from 902 MHz to 928 MHz. The interference on both the narrowband power line communication and the unlicensed wireless communication links is impulsive in nature. To mitigate such impulsive noise on both links, we propose a hybrid PLC/wireless communication transceiver where both links carry the same information data. We present efficient receiver diversity combining techniques for the PLC and wireless signals that takes into account the impulsive nature of the interference.

SUMMARY OF RESULTS

We propose PLC/Wireless receiver combining techniques based on maximal-ratio-combining (MRC) that take into account the impulsive nature of noise on the two links. In particular, for coherent modulation schemes, we present three PLC/Wireless receiver combining techniques with different performance/complexity tradeoffs. The proposed techniques are: average-SNR combining (ASC), power spectral density combining (PSC) and instantaneous-SNR combining (ISC). Furthermore, for differential modulation, we propose a diversity combining technique based on the received signal power and the noise PSD which outperforms the conventional average SNR and equal gain combining techniques over the whole operating SNR range.

In addition, we implemented a flexible real-time testbed to evaluate the proposed diversity combining schemes over physical PLC and wireless channels. The testbed realizes essential parts of the physical layers on which both powerline and wireless communications operate.

The real-time testbed is built using products from National Instruments. The PLC and wireless communications will be located in different places as they need different physical channels. Therefore, the two communication systems reside in different chassis. A PXI chassis has slots that can accommodate an x86 controller and various modules. As Fig. 1 depicts, a PXI-1045 chassis on the left has a PXI-8106 controller, a PXI-5421 signal generator and a PXI-5122 digitizer. This chassis functions as a baseband PLC system. Similarly, a PXIe-1082 chassis contains a PXIe-8133 controller, a PXIe-7965R FPGA module and an NI-5791 RF adapter module. Since the RF adapter module has both a transmit and a receive port, a unidirectional single-input single-output link can be established with a single adapter module.

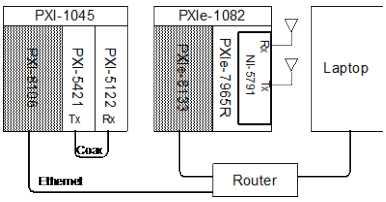

Figure 1. Hardware architecture.

The performance of the proposed combining techniques measured on the testbed is compared with computer simulation results by plotting BER curves for binary phase-shift keying (BPSK) modulation in Fig. 2 for both perfect and estimated channel scenarios.

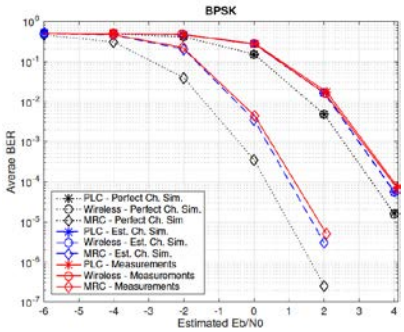

Figure 2. BER performance versus E_b/N_o.

Keywords: smart grids, power line and wireless communication, diversity, periodic impulsive noise

INDUSTRY interactions

Texas Instruments, NXP

MAJOR PAPERS

[1] M. Sayed, T. Tsiftsis, and N. Al-Dhahir, "On the Diversity of Hybrid Narrowband-PLC/Wireless Communications for Smart Grids", to appear in IEEE Transactions on Wireless Communications, 2017.

TASK 1836.138, MICRO-POWER ANALOG-TO-DIGITAL DATA CONVERTERS

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SIGNIFICANCE AND OBJECTIVES

The objective of the project was to develop improved architectures and circuits, as well as improved design processes for micro-power incremental and extended-counting analog-to-digital converters. The new concepts were then verified by the implementation and testing of appropriate test devices. The results far exceeded the state-of-the-art.

TECHNICAL APPROACH

Incremental analog-to-digital converters (IADCs) allow a single ADC to service multiple sensors. Our research developed novel IADC architectures that achieved both high accuracy and excellent power efficiency. We have found some particularly useful new IADC configurations, which need only a single active component used multiple times to achieve an excellent accuracy. This breakthrough hardware-recycling technique extends the accuracy of the converter with very low power consumption. Compared to the conventional single-step IADC of the same accuracy, the new ADCs reduce the power requirement by a factor of close to 1000. Fabricated on a chip, the novel device demonstrated superior performance.

SUMMARY OF RESULTS

Our last device realized a two-step incremental ADC (IADC) using extended counting [1]. In the first step, the IADC is configured as a first-order ΔΣ loop with an input feedforward architecture. In the second step, a two-capacitor SAR-assisted extended counting enhances the accuracy. A single active integrator is shared in both steps. The block diagram of the device is shown in Fig. 1.

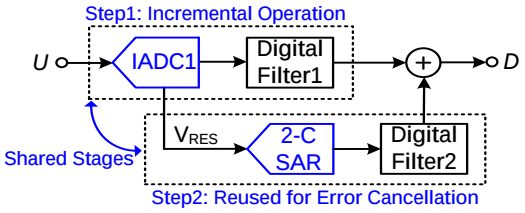

Figure 1. Conceptual block diagram of the proposed two-step IADC.

The period between adjacent resets is divided into two intervals. During the first step, the IADC realizes a first-order ΔΣ loop with a feedforward architecture. In the second step, when the control signal EN_{S2} goes high, the input path is disconnected. The quantization residue V_{RES} is quantized during the next M_2 periods by a SAR ADC, implemented by a two-capacitor DAC and the same integrator as used in the first step.

The prototype test chip was fabricated in a 0.18-µm CMOS process. Table I summarizes the measured performance of the prototype IADC, and compares it with state-of-art IADCs of earlier architectures. The IADC achieves a peak SNR/SNDR/DR of 97.1/96.6/100.2 dB over a 1.2 kHz bandwidth, while dissipating 33.2 µW from a 1.5 V supply. This gives a Schreier FoM of 175.8 dB and Walden FoM of 0.25 pJ/conv.-step, both among the best values. The combination of hardware recycling and SAR-assisted extended counting technique results in the reduction of both the power dissipation and the chip core area.

Table 1. Comparison with the state of the art.

Parameter	This Work	JSSC15	VLSI16	ISSCC16	ISSCC13
Architecture	IADC1 + Binary Counting	IADC2 +IADC1	IADC1 + Multi-Slope	Zoom ADC	Single IADC2
Technology (nm)	180	65	180	160	160
Area (mm^2)	0.27	0.2	0.32	0.16	0.45
Sampling Freq. (kHz)	642	192	642	11000	750
Bandwidth (kHz)	1.2	0.25	1	20	0.667
Power (µW)	33.2	10.7	34.6	1650	20
SNRmax (dB)	97.1	-	98.4	104.4	-
SNDRmax (dB)	96.6	90.8	96.8	98.3	81.9
DR (dB)	100.2	99.8	99.7	107.5	81.9
FoM^1_S (dB)	175.8	173.5	174.6	178.3	157.1
FoM^2_W (pJ/conv)	0.25	0.76	0.32	0.32	1.48

Keywords: multi-step incremental ADC, SAR-assisted, delta-sigma, extended counting, two-capacitor SAR

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Zhang, Y.,C-H Chen, He, T. and G.C. Temes, "A two-capacitor SAR-assisted multi-step incremental ADC with a single-amplifier achieving 96.6 dB SNDR over 1.2 kHz BW," IEEE Custom Integrated Circuits Conf., Austin, TX, Apr. 30 – May 3, 2017.

TASK 1836.139, ENABLING FULLY-INTEGRATED VHF CLK-SYNC MULTIPHASE SWITCHING REGULATORS ON SILICON

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SIGNIFICANCE AND OBJECTIVES

Voltage regulators in advanced SoC's are expected to achieve transient speed and power density higher than conventional regulators. In this project, three major issues in development of VHF (30-300 MHz range) multiphase switching regulators are investigated: high-speed feedback control, clock synchronization, and system miniaturization.

TECHNICAL APPROACH

From the perspective of control scheme, compared to its voltage-mode counterparts, the proposed current-mode approach is more robust to the noise at output voltage, as the sensed control vector is inductor current. From the perspective of system operation and circuit topology, interleaved multiphase topology can effectively improve the system response. By taking advantage of the proposed current-mode hysteretic control, a simple clock synchronization technique is proposed which achieves cycle-by-cycle regulation in each sub-converter.

From the perspective of system implementation, monolithic implementation of the regulator, which allows the power flow to follow the desired paths to reduce the parasitic is being investigated.

SUMMARY OF RESULTS

The challenge in the modern design of switching power converters has been to develop a fully integrated switching converter, which meets the additional demand for system miniaturization. In order to develop a fully integrated switching converter, it becomes necessary to operate in VHF regime to reduce the inductive and capacitive components in the power stage and to eliminate other bulky off-chip components.

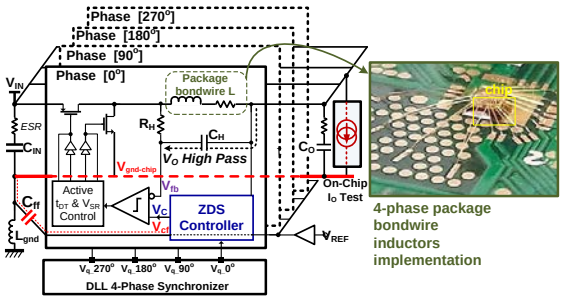

Figure 1. Block diagram of the four-phase buck converter with the photo of the package bondwire inductors implementation.

In this project, a fully on-chip integrated multiphase converter is proposed, and the system block diagram is shown in Figure 1. The four sub-converters are phase-synchronized by a built-in DLL-based synchronizer. As the proposed dual-loop control is independently conducted in each sub-converter, cycle-by-cycle current balancing is inherently implemented between phases. Moreover, the benefit of a multiphase operation is that it can achieve reduced passive components size and ns-level transient response. Thus, the required inductor size is significantly reduced to the range of the package bond wires, enabling implementation of the power inductor by using package bond wires as shown in Fig. 1. Accordingly, the system form factor, transient response, and power density have been significantly improved.

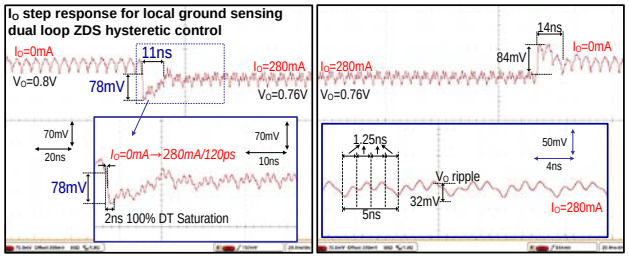

Figure 2. Measured load transient response to a load step from 0 to 280mA within 120ps with on-chip 1.97nF capacitor.

Fig. 2 shows the measured transient response and the output voltage ripple. The proposed converter employs a 1.8nF input capacitor, a 1.97nF output capacitor, and four 6.5nH bond-wire inductors without any other external components. In response to a 280mA/120ps load step-up, the voltage droop is 78mV (9.8% of output voltage) with 11ns response time. For load step-down, the converter exhibits 84mV overshoot within 14ns of 1% settling time. The output voltage ripple is maintained at 32 mV.

Keywords: fully integrated converters, VHF switching converters, multi-phase operation, feedback control

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] M. Song, et al., "A 200-MHz 4-Phase Voltage Regulator with Local Ground Sensing Dual Loop ZDS Hysteretic Control Using 6.5nH Package Bondwire Inductors on 65nm Bulk CMOS," (Invited) in 2016 ASP-DAC, pp. 1422-1425, Jan. 2014.

TASK 1836.140, EMBEDDED & ADAPTIVE VOLTAGE REGULATORS WITH PROACTIVE NOISE REDUCTION FOR DIGITAL LOADS UNDER WIDE DYNAMIC RANGE

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SIGNIFICANCE AND OBJECTIVES

The primary goal of the project is to develop an integrated power flow architecture for fine-grained spatio-temporal voltage distribution and management in microprocessors and SoC's. We investigate through models, simulations, hardware development and experimentation novel control topologies and circuit techniques for efficient wide-dynamic range linear and switched capacitor VR's.

TECHNICAL APPROACH

This project investigates power flow architecture in microprocessors and SoCs. There are two primary thrusts here: (1) development of novel control topologies for all digital linear regulators for Point of Load (PoL) regulation and (2) use of switched capacitor on-die regulators to provide power on demand for distributed IP blocks. In this phase of the program, the major accomplishments have been on the development of novel PoL topologies, circuit prototyping and measurements.

SUMMARY OF RESULTS

In the past year of performance, we have continued to investigate (1) switched mode control for ultra-fast droop recovery (2) a novel unified voltage and frequency (UVFR) topology that allows operation of digital load circuits under fine-grained DVFS states while continuing to work during a voltage droop or during PLL relocking, and (3) a multiple output switched capacitor VR. In switched mode control, the LDO differentiates between small signal regulation and the large signal performance. Small signal regulation is handled by an output pole dominant analog loop, whereas the large signal transients are handled by a digital loop (Fig. 1). Measurements show peak response time of 18 ns for large load transients, low voltage operation programmability and a peak current efficiency of 98.64%. Motivated by the observation that the main objective of supply voltage regulation in digital systems is meeting timing, we present a Unified Voltage Frequency Regulator (UVFR) that sets the supply voltage based on system timing properties, and minimizes supply noise margins by temporarily modulating the clock frequency. Measured data on a 130nm test-chip across a wide range of voltage and current inputs reveals peak current efficiency of 99.4% and 27% supply reduction at iso-performance through adaptation and resiliency which are intrinsic to the control loop. We have also proposed a multiple output SCVR (Fig. 3). This allows co-regulation across four different voltage domains and peak measured efficiency of 84%.

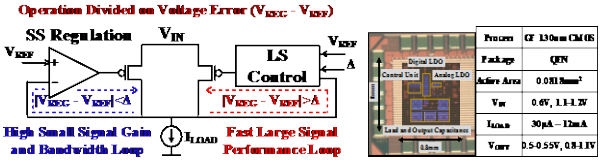

Figure 1. Switched Mode Control for LDO.

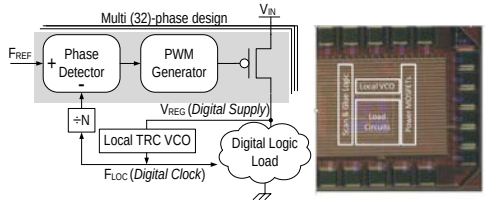

Figure 2. Unified Voltage and Frequency Regulation.

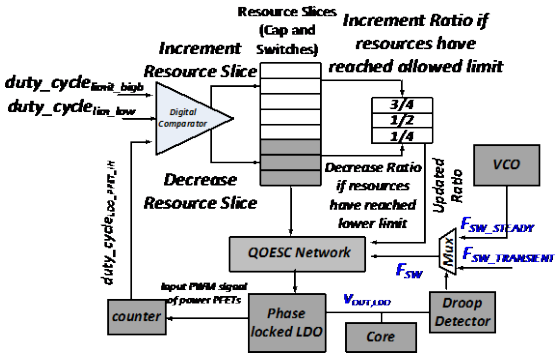

Figure 3. Multi-output SCVR architecture.

Keywords: integrated voltage regulator, discrete control, continuous time control, LDO, switched mode control

INDUSTRY INTERACTIONS

Intel, IBM

MAJOR PAPERS/PATENTS

[1] S. Gangopadhyay et al., CICC, 2017.
[2] Saad Nasir, et al. Applied Power Electronics Conference and Exposition (APEC), 2015.
[3] Saad Nasir, et al. ISSCC, 2015.
[4] Saad Nasir et al., Transactions on Power Electronics.
[5] S. Gangopadhyay et al., JSSC, 2014.
[6] Saad B. Nasir, et al. ISCAS, 2016.
[7] Saad B. Nasir, et al. ESSCIRC, 2016.
[8] S. Gangopadhyay et al., ESSCIRC, 2016.
[9] S. Gangopadhyay et al., DAC, 2015.

TASK 1836.142, LOW POWER APPLICATIONS OF FRAM

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DENNIS SYLVESTER, UNIVERSITY OF MICHIGAN

SIGNIFICANCE AND OBJECTIVES

The focus of our research is on ultra-low energy FRAM arrays for millimeter-scale sensors. The objective is to optimize FRAM for ultra-low energy operation by using an adiabatic design to reduce write energy, especially for large block writes. This report details the current test results on the FRAM prototype chip.

TECHNICAL APPROACH

The approach uses resonance to reduce energy consumption. To start the resonance PL is stepped to $V_{DD}/2$. To write new data into a row, the BLs are switched to data adiabatically by controlling the WREN and PLEN, i.e. the starting point and ending point for data '0' is 0 of PL and for data '1' is V_{DD} of PL. Each row needs one and a half cycle of resonance to write a new data, with its word-line asserted. The WL signals are overdriven to (V_{DD}+V_{TH}) to compensate for the V_{TH} drop across NMOS access transistor.

SUMMARY OF RESULTS

Fig. 1 shows the die picture of the FRAM prototype chip in a 130nm process node. It has an array size of 512x80 in 1T-1C mode, and 256x80 in the 2T-2C mode.

The prototype chip for the adiabatic FRAM design has been fabricated, and we received the dies earlier this year. The chip was then packaged, and in parallel a test board was designed, which has the LC tank on the board.

Currently, the chip is being tested. Read and write operations on the FRAM have been validated on this prototype with a conventional square waveform. The non-volatile behavior has also been tested by writing and reading across a power off sequence.

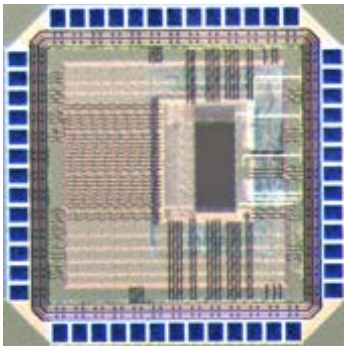

Figure 1. Die photo – 130 nm FRAM prototype chip.

Fig. 2 shows the block diagram of the FRAM prototype chip. The validation of read and write with a square waveform has allowed us to test the peripherals inside the red boundary.

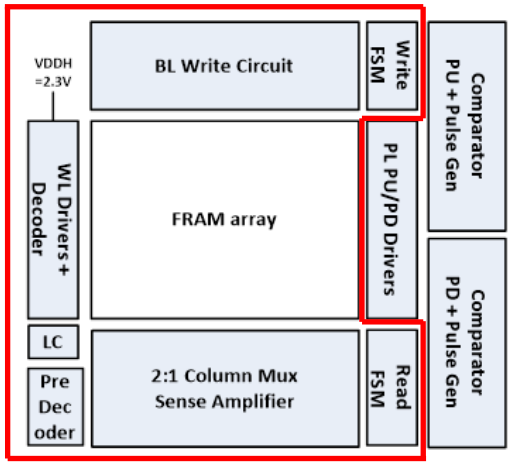

Figure 2. FRAM prototype block diagram.

For the circuit to resonate, the LC tank on the board has to be tuned with the board parasitic, and the pad parasitic, in addition to the FRAM block inside the chip. Once we find the correct LC values, it will also allow us to characterize the adiabatic FRAM, and validate the adiabatic operation. Currently, we are debugging the resonance circuits, and will share the testing results for the sinusoidal waveform based adiabatic operation, once available.

Keywords: low power, memory, non-volatile, CMOS, electronics

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

TASK 1836.143, DESIGN TECHNIQUES FOR MODULATION-AGILE AND ENERGY-EFFICIENT 60+GB/S RECEIVER FRONT-ENDS

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SIGNIFICANCE AND OBJECTIVES

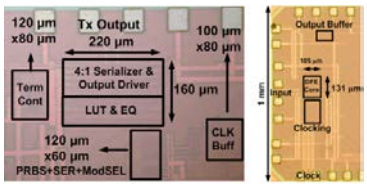
While high-performance I/O circuitry can leverage CMOS technology improvements, unfortunately the bandwidth of the electrical communication channels has not scaled in the same manner. The high-speed serial link receiver design and modeling techniques proposed here aim to significantly improve interconnect bandwidth density in an energy-efficient manner.

TECHNICAL APPROACH

In order to investigate design trade-offs, a statistical-modeling framework will be utilized to investigate power-optimum equalization partitioning and modulation format for 60+Gb/s signaling environments. This tool will be used to guide the design of a new modulation-agile receiver front-end which includes a multi-level decision-feedback equalizer (DFE) with multiple FIR/IIR feedback taps for efficient long-tail ISI cancellation. Adaptive techniques will also be developed to tune key equalization parameters, such as DFE tap time constants/weights and CTLE settings.

SUMMARY OF RESULTS

PAM4 modulation offers the potential to support ever-increasing serial I/O bandwidth density demands. While dedicated PAM4 transceivers have been developed, the majority of serial I/O standards use simple binary NRZ modulation. In order to address this, a dual-mode NRZ/PAM4 SerDes which seamlessly supports both modulations with a 1-FIR- and 2-IIR-tap DFE receiver and a 4/2-tap FFE transmitter in NRZ/PAM4 modes, respectively, was developed [1, 2]. A source-series-terminated (SST) transmitter employs lookup-table (LUT) control of a 31-segment output DAC to implement FFE equalization in NRZ and PAM4 modes with a 1.2-V_{pp} output swing and utilizes low-overhead analog impedance control. Optimization of the quarter-rate transmitter serializer is achieved with a tri-state inverter-based mux with dynamic pre-driver gates. The quarter-rate DFE receiver achieves efficient equalization with 1-FIR tap for the large first post-cursor ISI and 2-IIR taps for long-tail ISI cancellation. Fabricated in GP 65-nm CMOS (Figure 1), the transceiver occupies 0.074 mm^2 area and achieves power efficiencies of 10.9 and 5.5 mW/Gbps with 16Gb/s NRZ and 32Gb/s PAM4 data, respectively.



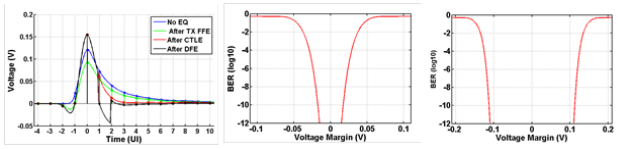
(a) (b)

TRANSCEIVER PERFORMANCE SUMMARY

References	This Work		[5]	[6]	[35]	[13]	[34]
Data Rate	32 Gb/s	16 Gb/s	20 Gb/s	56 Gb/s	56 Gb/s	28 Gb/s	16 Gb/s
Equalization	2-tap TX FFE + 1-tap FIR, 2-tap IIR RX DFE	4-tap TX FFE + 1-tap FIR, 2-tap IIR RX DFE	3-tap TX FFE	3-tap TX FFE + 1-tap RX DFE	3-tap TX FFE + RX CTLE + ADC based RX 24-tap FEE, 1-tap DFE	5-tap TX FFE + RX CTLE + 14-tap RX DFE	3-tap TX FFE + RX CTLE + 14-tap RX DFE
Modulation	PAM4	NRZ	PAM4	PAM4	PAM4	NRZ	NRZ
Total Loss @ Nyquist	13.5 dB	27.6 dB	5 dB	2 dB	25dB	40 dB for 25.78 Gb/s	34 dB
Eye Width BER	6% 10^{-12}	18% 10^{-12}	- 10^{-12}	- 10^{-12}	- 10^{-8}	23% 10^{-12}	- 10^{-15}
Supply (V)	1.2 TX, 1 RX		1.8	1.2	0.9 digital, 1.2 analog, 1.8 auxiliary	1 TX & RX, 1.25 TX driver	1/1.5 TX, 0.9 RX
Power (mW) (mW/Gbps)	176.3 5.5	173.7 10.9	408 20.4	475 8.5	550* 9.8	295* 10.5	235* 14.7
Area (mm^2)	0.074		0.43	2.74	1.4	0.62	2.15
Technology	65-nm		90-nm	65-nm TX, 40-nm RX	16-nm FinFET	28-nm	40-nm

(c)

Figure 1. 16/32Gb/s dual-mode NRZ/PAM4 SerDes in GP CMOS: (a) transmitter, (b) receiver, and (c) performance summary.



(a) (b) (c)

Figure 2. Statistical modeling of 20dB loss channel: (a) 32GS/s pulse response with and without equalization, (b) 64Gb/s PAM4 bathtub curve, and (c) 32GB/s NRZ bathtub curve.

At low BER's, transient simulations are impractical. To investigate this, this project continues to build upon the PI's statistical-modeling framework for high-speed serial links. While receiver-side DFE equalization is very power efficient for cancelling post cursor ISI, its effectiveness is limited by large pre-cursor ISI in channels with more than 15dB of loss in PAM4 mode (Figure 2). Link simulations indicate that an efficient way to deal with pre-cursor ISI is to use a pre-cursor FFE equalizer tap at the transmitter side and RX CTLE. This provides sufficient voltage margin for both 64Gb/s PAM4 and 32Gb/s NRZ operation.

Keywords: decision feedback equalizer, infinite impulse response (IIR) DFE, receiver, serial link

INDUSTRY INTERACTIONS

IBM, Texas Instruments

MAJOR PAPERS/PATENTS

[1] A. Roshan-Zamir et al., "A 16/32 Gb/s Dual-Mode NRZ/PAM4 SerDes in 65nm CMOS," IEEE CSICS, 2016.

[2] A. Roshan-Zamir et al., "A Low-Overhead Reconfigurable 16/32 Gb/s Dual-Mode NRZ/PAM4 SerDes in 65nm CMOS," accepted in IEEE JSSC.

TASK 1836.144, HIGH-EFFICIENCY HIGH-VOLTAGE POWER CONVERTERS

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SIGNIFICANCE AND OBJECTIVES

This research aims to investigate novel soft-switching techniques, synchronous gate driving techniques, and control schemes to significantly advance power efficiency and power density of today's high-voltage DC-DC converters. These developed converter technologies help greatly lower the cost and improve the energy efficiency of renewable energy, telecom, automotive and other systems.

TECHNICAL APPROACH

Hardware verifications of a high-voltage isolated GaN based bus converter shown in Fig. 1 using the proposed high-voltage gate drivers have been conducted. Four power FETs M_1 – M_4 form the two legs of the full-bridge converter. M_1 and M_2 are driven 180° out of phase, while M_4 and M_3 are driven complementary to M_1 and M_2, respectively. ZVS of power FETs M_1 – M_4 can be achieved under medium to full current conditions via resonance between the external inductor L_R and parasitic capacitance at the switching nodes (A and B). Capacitor C_B is used to block the DC difference between V_A and V_B such that any mismatch between the two legs will not saturate the primary winding of the transformer. Power FETs M_1 – M_4 are realized by 650-V eGaN FETs (GS66502B) from GaN Systems.

SUMMARY OF RESULTS

The hardware prototype of the bus converter with the proposed gate drivers is set up as shown in Fig. 2. The switch-node voltage (V_{SW1}) and the low-side gate drive voltage (V_{GS4}) are measured with a 500-MHz single-ended probe, and the high side gate drive voltage (V_{GS1}) is measured with a 500-MHz differential probe. Input voltage (120V – 400V) was provided by a 600-V power supply and two resistor boxes are used as the load of bus converter. Fig. 3 demonstrates the waveforms of switch-node voltages (V_{SW1}, V_{SW2}), low-side gate drive voltage (V_{GS4}) and high-side gate drive voltage (V_{GS1}) under the input voltage of 400V at 1-MHz switching frequency. It proves that the converter operates properly with zero-voltage switching of different power switches. The proposed gate driver reduces the turn-on delay by as much as 25ns as compared to the conventional gate drivers, reducing the power loss by 2W. The GaN isolated bus converter achieves the peak power efficiency of 90.4% at the input switching frequency of 1MHz.

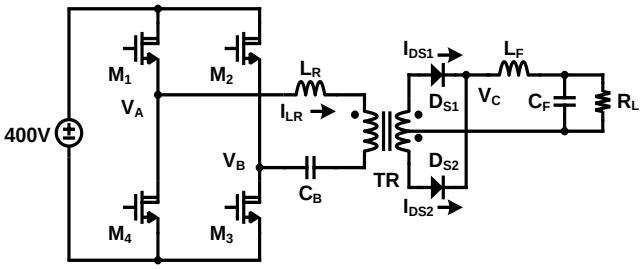

Figure 1. Structure of the isolated bus converter.

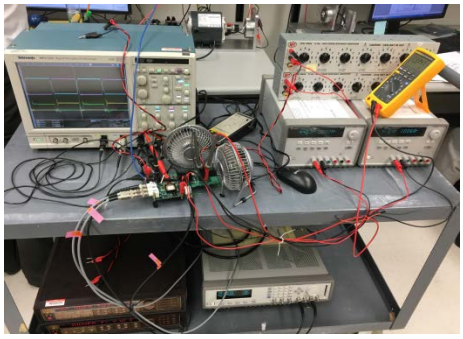

Figure 2. Test bench setup of the bus converter with the proposed gate driver.

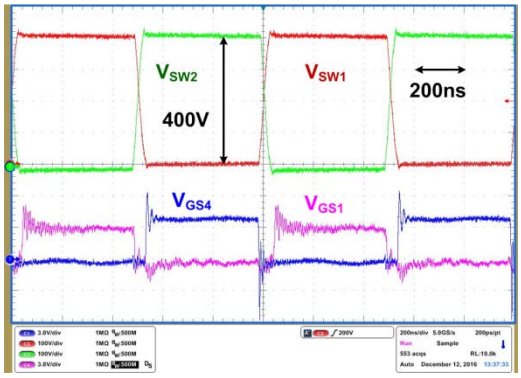

Figure 3. Steady-state operation of the converter with 400V input.

Keywords: high-voltage DC-DC converters, isolated converters, on-chip synchronous gate driver, zero-voltage switching

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] L. Cong and H. Lee, "High-voltage high-frequency DC-DC converters with passive-saving two-phase QSW-ZVS technique," *Journal of Analog Integrated Circuits and Signal Processing*, vol. 88, no. 2, pp. 303 – 317, Aug. 2016.

TASK 1836.146, ON-CHIP AC-DC POWER CONVERSION WITH GROUND DISTURBANCE SHIELDING FOR ENVIRONMENTAL SENSING APPLICATIONS

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SIGNIFICANCE AND OBJECTIVES

This project is to explore the optimal circuit architecture and operation scheme in achieving on-silicon AC-DC power conversion for environmental sensor applications. The power converter under development should be resilient to ground voltage disturbance, along with high power efficiency and small physical form factor.

TECHNICAL APPROACH

Capacitive power transfer enables the implementation of fully integrated power converters. It is resilient to ground voltage surge and noise by using a high-voltage on-chip capacitor, which provides a smaller form factor than a traditional discrete transformer. Thanks to a novel operation scheme, the proposed topology can achieve power transfer efficiency over 50% when it is operating in low power (<100mW) region.

SUMMARY OF RESULTS

Capacitive isolation replaces the bulky magnetic components with on-chip barrier, enabling low-cost monolithic implementation. However, the low density on-chip capacitor and large parasitic limit the output power level and efficiency of the capacitive power transfer system.

In order to address these issues of capacitive isolation system, a resonant-based circuit architecture, which is shown in Fig. 1, for isolation power transmission is proposed. Differentiated from the traditional capacitive coupling power systems, two inductors are placed on the power path, and form a resonant tank with an isolation capacitor and the bottom-capacitors. The inductors not only can reduce the impedance of the power path, but also limit the current peak that charge and discharge the bottom-plate capacitors.

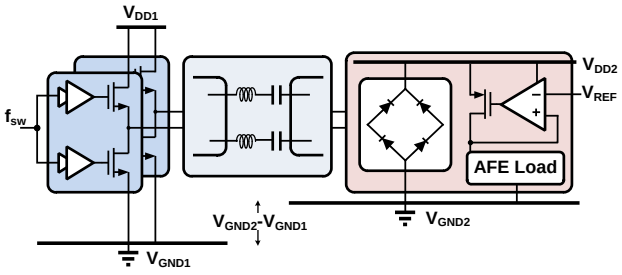

Figure 1. The resonant converter for isolation power transfer.

The operation of the resonant converter is as follows. DC voltage V_{DD1} is converted by an H-bridge circuit into a square wave with a frequency of f_{sw}. When f_{SW} is equal to the resonant frequency, the fundamental component can pass through the resonant tank. The selected AC power is rectified at the output node to provide DC power to loading circuitries.

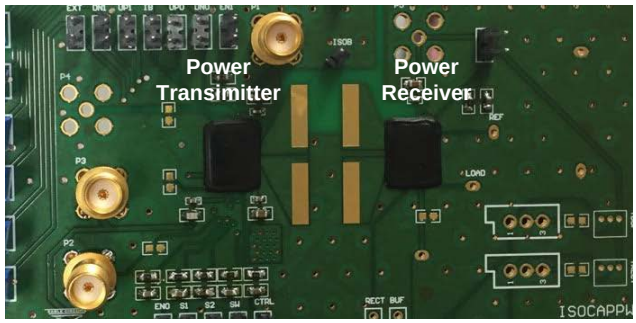

Figure 2. Photograph of fully-integrated capacitive isolation power transfer chips (transmitter and receiver) and test PCB.

The capacitive power transfer system is fabricated with a HV BCD process. The chip and PCB implementation is shown in Fig. 2. To achieve isolation, two high-voltage capacitors are integrated on-chip for each phase. Off-chip air-core inductors are used to implement the LC tanks. Thanks to the resonant operation, the peak power efficiency is 50.7% and maximum output power is 62mW. This design achieves 4× efficiency improvement and 3× power delivery than the prior art.

Keywords: power isolation, low-power sensor interface, capacitive power transfer, resonant power transfer, fully-integration power converter

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] L. Chen et al., “A 50.7% Peak Efficiency Subharmonic Resonant Isolated Capacitive Power Transfer System with 62mW Output Power for Low-Power Industrial Sensor Interfaces” 2017 ISSCC, Feb., 2017, San Francisco, USA.

TASK 1836.149, CONDITION MONITORING OF PM/IPM MOTORS THROUGH AXIAL/RADIAL LEAKAGE FLUX

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SIGNIFICANCE AND OBJECTIVES

The fault signature characteristics may cause misleading results depending on motor topology, winding configuration, and controller parameters. However, leakage flux leads superior diagnostic results in time and frequency domain. Simulation and experimental results show that the deployment of a direction-sensitive fluxgate sensor yields very promising results.

TECHNICAL APPROACH

The magnetic field distribution plays a fundamental role in motor performance. In particular, the air-gap magnetic field determines the back-emf, torque, stator flux and leakage flux. In order to analyze the circulating flux in and out of the machine, an approximate magnetic equivalent circuit including major reluctances is introduced in PMSMs (Fig.1). Among the flux components, the leakage flux has relatively low amplitude when compared to air-gap flux (ϕ_g). However, leakage components provide valuable information regarding the motor condition and can be used to detect magnet defect faults in PM motors.

SUMMARY OF RESULTS

Fig. 2 shows the radial flux component behind tooth, and tangential flux component behind slot at 200Hz supply frequency. When there is a magnet defect fault, the leakage flux content changes across the defected magnet in experimental results. Fig. 3(a) shows the spectrum of radial (behind tooth) and tangential (behind slot) leakage flux components. The signatures raise remarkably and the change in dominant components such as 0.25^{th} and 0.5^{th} harmonics is negligible when the load increases. These tests show that the magnetic field created by the rotor magnets dominates and result in load independent magnet defect analysis.

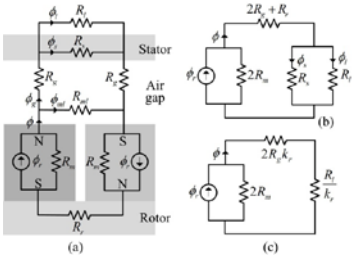

Figure 1. Conceptual fluxgate sensor permeability.

In order to show the speed effects on the fault signatures when a stator is excited, the motor is run at two different speeds under full load both in simulation and experimental tests: 600 and 3000 rpm. As shown in Fig. 3(b), the fault related harmonics are almost speed independent as in the case of open terminal test. Table 1 shows the amplitude of some characteristics fault signatures i.e. 0.25^{th} and 0.5^{th} with different controller parameters in the leakage flux spectra. These tests show that the flux based monitoring analysis is more immune to controller parameter changes than current based monitoring.

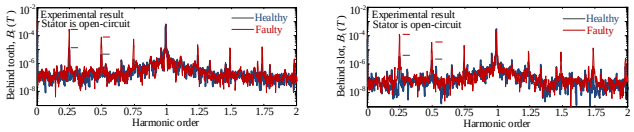

Figure 2. Measured results, terminals disconnected (back-emf).

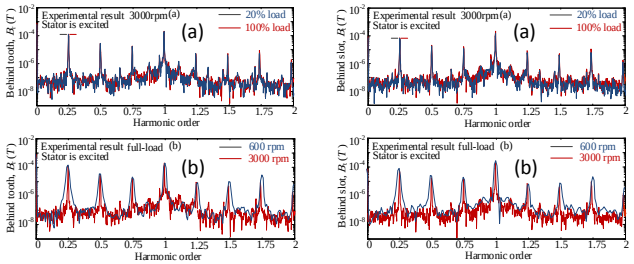

Figure 3. Measured results, Motor operation for different torque/speed profiles (a) Radial Flux (b) Tangential flux.

Table 1. The controller effects on the fault signatures.

Controller parameters	*0.25^{th} (μT)*	*0.5^{th} (μT)*	*0.25^{th} (mA)*	*0.5^{t} mA)*
k_{p_spd}=1; k_{i_spd}=0.005; k_{p_id}=1; k_{i_id}=0.0025; k_{p_iq}=1; k_{i_iq}=0.0025;	*218.5*	*59.9*	*9.19*	*24.4*
k_{p_spd}=1; k_{i_spd}=0.005; k_{p_id}=1; k_{i_id}=0.0125; k_{p_iq}=1; k_{i_iq}=0.0125;	*217.8*	*63.7*	*7.38*	*19.4*
k_{p_spd}=3; k_{i_spd}=0.005; k_{p_id}=1; k_{i_id}=0.0025; k_{p_iq}=1; k_{i_iq}=0.0025;	*211.6*	*64.4*	*7.94*	*18.6*

Keywords: fault diagnosis, condition monitoring, fluxgate sensors, leakage flux spectrum analysis

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] "Comprehensive Analysis of Magnet Defect Fault Monitoring Through Leakage Flux," in IEEE Transactions on Magnetics, vol. 53, no. 4, pp. 1-10, April 2017.

[2] "An Investigation of Motor Topology Impacts on Magnet Defect Fault Signatures," in IEEE Transactions on Industrial Electronics, vol. 64, no. 1, pp. 32-42, Jan. 2017.

TASK 1836.153, HIGH-SPEED COMPACT POWER SUPPLIES FOR ULTRA-LOW-POWER WIRELESS SENSOR APPLICATIONS

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SIGNIFICANCE AND OBJECTIVES

Efficient and compact switched-capacitor (SC) voltage regulators are highly desirable for ultra-low-power sensor applications to improve energy efficiency and reduce system form factor. This project seeks to deliver a wide-input, fully-integrated SC voltage regulator with high efficiency and fast dynamic responses for sensor systems.

TECHNICAL APPROACH

To achieve multiple conversion ratios (CRs) and wide input operation, three 2:1 unit SC cells are implemented as a reconfigurable power stage while retaining low system complexity. By swapping the input and the output for the power stage, a buck/boost voltage conversion is achieved. The single-bound hysteretic control scheme is employed in this project for the output regulation, due to the simple implementation. Besides, the hysteretic controller only requires a single analog circuit, reducing the quiescent power. A design prototype has been tested to verify the CR reconfigurations and interleaving scheme.

SUMMARY OF RESULTS

A SC voltage regulator with three 2:1 unit cells is designed to attain 5 buck CRs and 6 boost CRs, such that the input voltage can be extended to the nominal battery voltage of 5V. Furthermore, this project presents an adaptive-power single-bound hysteretic control, illustrated in Figure 1. Instead of using a high-frequency clock to avoid system metastability as the conventional approach, an RC oscillation network is controlled by a reset logic with the driving clock for the main voltage regulator. In this situation, the clock provided to the hysteretic controller is modulated by the load current such that the quiescent power in controller can be adaptively reduced for light load conditions. In addition, by adjusting the reference voltage during load transitions, the proposed hysteretic controller can immediately increase/decrease the clock frequency, minimizing load response time.

The first test prototype is implemented in a 65-nm bulk CMOS process to validate the CR reconfigurations and the interleaving scheme. The key waveforms are shown in Figure 2. With the input voltage of 1.8V, the measured SC voltage regulator modulates CR from 4:3 to 3:2 to supply 1.1V and 0.95V, respectively. Thanks to the interleaving operation, the output ripple is effectively limited within 35mV. Phase control is employed to maintain the efficiency at light load and attain output regulation. In Figure 2, varying the load from 300mA to 400mA, the number of the interleaving phases is adjusted from 9 to 12 to regulate the output voltage with low variations.

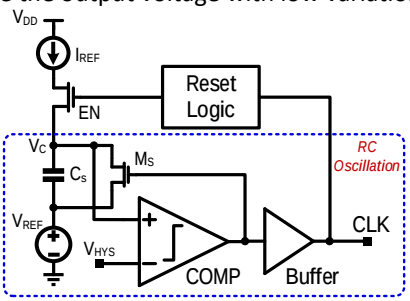

Figure 1. Circuit diagrams of proposed adaptive-power single-bound hysteretic controller.

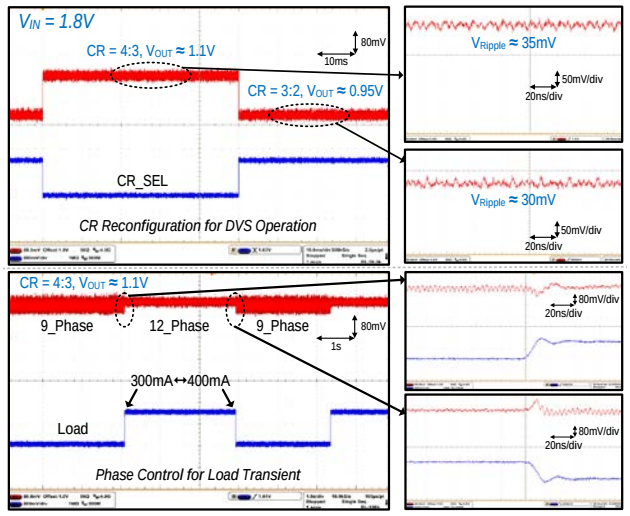

Figure 2. Key test waveforms of first prototype.

The second prototype will be fabricated to verify the entire system implementation with a hysteretic controller. To reduce the quiescent power in the controller, the study of low-power circuit design is in progress.

Keywords: wireless sensor, switched-capacitor, wide input, hysteretic control, adaptive power

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

TASK 1836.154, STATE OF THE HEALTH (SOH) FOR IGBTS: INCIPIENT FAULT CHARACTERIZATION AND DEGRADATION MONITORING

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SIGNIFICANCE AND OBJECTIVES

Continuously monitoring energy conversion systems is essential to prevent unexpected shutdowns and catastrophic failures that may result in accidents or significant operation loss.

TECHNICAL APPROACH

Prognostics and failure prediction require accurate characterization of IGBT's with respect to aging. The proposed approach determines the state of health for IGBT based on actual in-field data. So, firstly, variations in all current-voltage characteristics and parasitic elements of IGBTs at different thermal stress levels using a custom-built test bed have to be analyzed. Using these aging test data, electrically measured failure precursor has to be identified and in-situ measurement circuits need to be developed. Based on these in-situ measurements and SAM images, state of the IGBT's health will be determined.

SUMMARY OF RESULTS

As our first goal, a setup has been developed as shown in Figure 1 to apply different thermal stress levels on IGBT's emulating real-time operational conditions. Then, variations in all current-voltage characteristics and parasitic elements of IGBT's from different tests have been analyzed to determine suitable failure precursor(s). Figure 2 shows few test results. It has been found that the on-state collector-emitter voltage drop (V_{ce}) can indicate potential bond-wire and solder delamination issues whereas the gate threshold voltage (V_{TH}) has been identified as another failure precursor which can predict gate-oxide degradation at elevated temperatures. Table 1 provides the general trend for V_{CE} and V_{TH} during different thermal aging profiles.

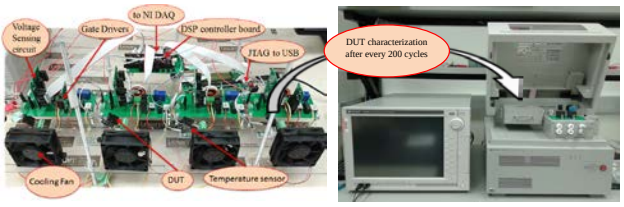

Figure 1. Aging setup schematic.

Table 1. Summary of the tests findings.

	Tj=Tc=Hi	Tj=Tc=Lo	Tj=Hi;Tc=Lo
V_{CE}			
V_{TH}			

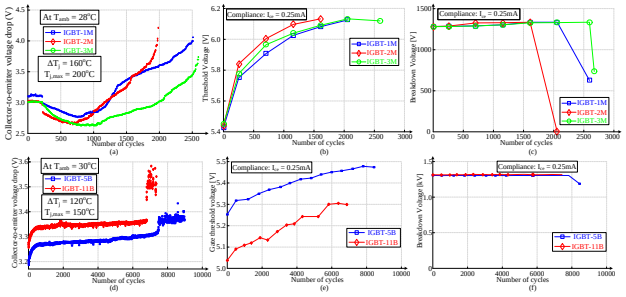

Figure 2. Comparison of failure precursor at different temperatures, (a) and (d) Vce measurement, (b) and (e) V_{TH} measurement and (c) and (f) BVces measurement for failure.

The next step is to develop the necessary in-situ measurement circuit by which these failure precursors can be observed during the course of IGBT lifetime. Additionally, the proposed circuit as shown in Figure 3 is designed such that it could be incorporated easily within the gate driver circuit.

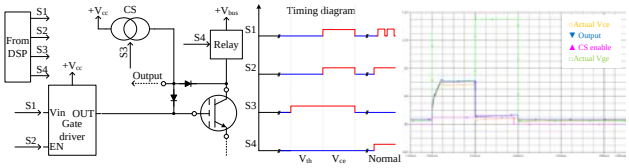

Figure 3. Proposed in-situ V_{CE} and V_{TH} measurement circuit, (a) circuit schematic, (b) timing diagram illustrating different modes of operation and (c) simulation results.

Keywords: failure diagnosis, failure precursor, on-state voltage drop, gate threshold voltage, in-situ measurement

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] "Lifetime Estimation of Discrete IGBT Devices Based on Gaussian Process," in IEEE Transactions on Industry Applications [in Press].

[2] "Aging Precursor Identification and Lifetime Estimation for Thermally Aged Discrete Package Silicon Power Switches," in IEEE Transactions on Industry Applications, vol. 53, no. 1, pp. 251-260, Jan.-Feb. 2017.

[3] "A comprehensive study on variations of discrete IGBT characteristics due to package degradation triggered by thermal stress," 2016 IEEE ECCE, Milwaukee, WI, 2016, pp. 1-6.

TASK 2712.002, ON-LINE SELF-TESTING AND SELF-TUNING OF INTEGRATED VOLTAGE REGULATORS

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SIGNIFICANCE AND OBJECTIVES

This task will develop low-complexity algorithms and low-overhead all-digital self-testing and self-tuning architecture for high-frequency integrated voltage regulators (IVR's). The proposal will focus on digitally controlled fully integrated inductive VR (FIVR), digital low-dropout regulators (DLDO), and power delivery system with FIVR and multiple distributed DLDO's.

TECHNICAL APPROACH

The challenge for testing/tuning of IVR's is the presence of high frequency closed-loop control. The proposed approach is based on the principle that in a system with IVR's and digital core(s), the testing/tuning should focus on system performance rather than the IVR in isolation. We propose to characterize the output voltage variation that ultimately determines the performance of the digital load. We consider large signal perturbations (load and reference steps) to excite transient noise in the IVR's output, and tune the IVR's loop to minimize the noise. Finally, we explore co-tuning of IVR and processor.

SUMMARY OF RESULTS

Self-tuning of High-frequency Buck Regulator: We have presented a fast and compact auto-tuning architecture to enhance tolerance to parametric variations in the filter passives without complex computation. The time domain (stable steady-state and fast transient response) behavior of an IVR output determines the system performance. We have developed a stability-figure-of-merit (SFOM) to quantify the time-domain behavior of the IVR output, computed by performing simple arithmetic operations on the output error, and the locations of compensator's poles and zeros (dictated by the compensator's coefficients). The SFOM is considered to be a linear combination of absolute error, signed error, and convergence time associated with transient response. A self-testing and self-tuning loop is designed that applies the load/reference transients for different coefficients; and finds the minimum SFOM over a range of coefficients applied to the system while observing the output error (digitized difference between output and reference). The simplicity of resulting tuning algorithm allows a light and fast tuning engine, able to operate at sampling frequency and removes requirement for storing any error samples. We have first demonstrated the effectiveness of the tuning in a 130-nm test-chip for a 125-MHz buck converter with a 11.6nH inductor and a 3.2nF capacitor. Measurements demonstrated that self-tuning help improve transient performance under variations in passives (inductor).

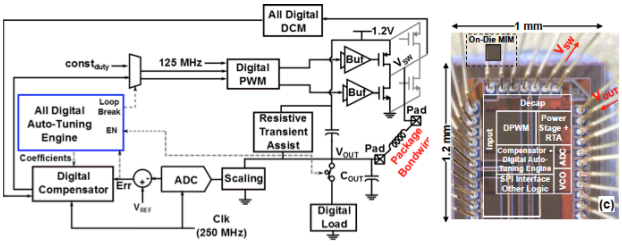

Figure 1. The preliminary architecture and test-chip for the self-tuning regulator.

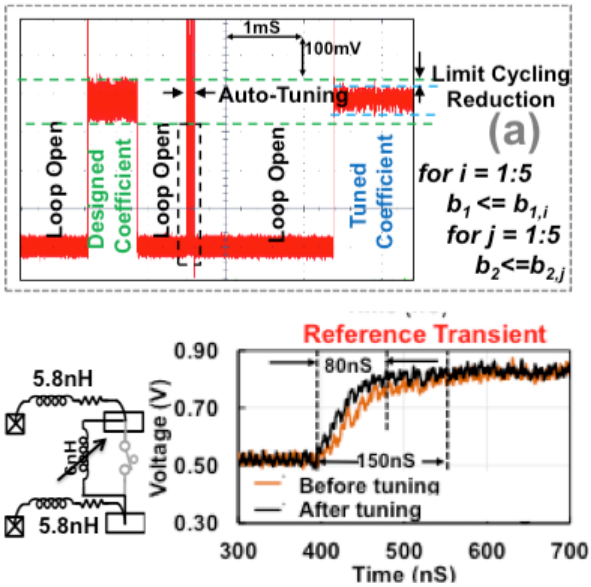

Figure 2. The measurement results showing the tuning process and effect of tuning on transient response.

Keywords: integrated voltage regulator, self-testing, and self-tuning.

INDUSTRY INTERACTIONS

Intel, NXP

MAJOR PAPERS/PATENTS

[1] M. Kar, A. Singh, A. Rajan, V. De, and S. Mukhopadhyay, "An All-Digital Fully Integrated Inductive Buck Regulator with A 250MHz Multisampled Compensator and A Lightweight Auto-Tuner in 130nm CMOS," IEEE Journal of Solid State Circuits (JSSC), July 2017.

TASK 2712.006, ROBUST, EFFICIENT ALL-DIGITAL SIMO CONVERTERS FOR FUTURE SOC DOMAINS

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SIGNIFICANCE AND OBJECTIVES

As Integrated Voltage Regulated (IVR)—enabled DVFS systems continue to be more aggressively adopted in SoC designs, their limited scalability poses a significant challenge. Single-Inductor Multiple Output converters offer a scalable solution, but face significant regulation challenges. The proposed effort seeks to provide (1) an all-digital voltage regulation system for digital SoC domains, and (2) a Unified Clock and Power (UnCaP) architecture for robust regulation and simplified (frequency-only) control of system performance.

TECHNICAL APPROACH

The effort around the UnCap architecture observes that robust voltage regulation is required for the purpose of avoiding timing failure in digital systems. As such, a fused clock-power generation architecture, relying on an "elastic" PLL to respond to voltage droops and ripples, while entrusting a slower voltage control loop to maintain the target operating frequency offers both simplicity and efficiency. This effort will be the first of its kind to build a comprehensive IVR-PLL fused system, addressing important issues pertaining to stability, margin removal, and robust synchronous operation. The technology resulting from this effort will enable the next generation fine-grained IVR systems for both data-center and IoT edge devices.

SUMMARY OF RESULTS

We have identified and outlined the architecture of the elastic ADFLL, powered by the regulated power supply domain. The ADFLL DCO is composed of a synthetic critical path circuit which allows the user to tune both the time-period of the critical path, as well as the voltage sensitivity of the critical path to droop. The DCO enables not only a much needed clock-stretch in the event of a droop, but also allows the resulting TDC measurement relative to a reference clock to be reported to the voltage regulator control to drive the regulated supply, ensuring that the DCO meets the required target frequency. A RefClk-frequency comparison approach was adopted due to its simplicity, and the absence of any performance loss. This wide lock-range architecture allows frequency-only control of the system without an accompanying a voltage ID (VID) code – The user only requests a target operating frequency and the system autonomously regulates the supply voltage in the presence of PVT variation to robustly meet this target frequency.

The proposed architecture has been evaluated through simulations and is being prepared for test-chip characterization (Fig. 1) as part of a broader regulation system for a near-V_{TH} frequency-controlled ARM microprocessor.

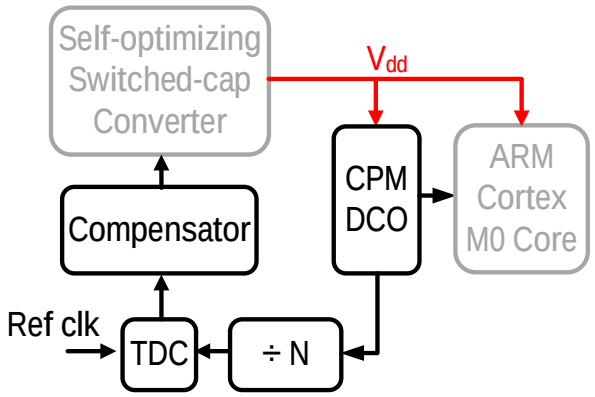

Figure 1. Proposed ADPLL architecture currently beting prototyped as part of a larger switched-capacitor system. Research effort funded by other efforts greyed out.

Keywords: FLL, PLL, IVR, unified clock-power regulation

INDUSTRY INTERACTIONS

Intel, ARM

MAJOR PAPERS/PATENTS

TASK 2712.008, DIRECT-BATTERY-TO-SILICON POWER TRANSFER IN ADVANCED NANOMETER CMOS

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SIGNIFICANCE AND OBJECTIVES

The aim of the task is to facilitate direct-battery-to-silicon high-tension-power delivery in advanced CMOS processes to bring down delivery losses and area footprint. The key objective is to develop circuit techniques to handle breakdown voltages and implement fine-grain feedforward control for SoC's while making these solutions portable across technology and types of SoC's.

TECHNICAL APPROACH

To accommodate a Dynamic Voltage Scaling system for SoC's, we need smart management of the different switched capacitor DC-DC conversion ratios. Deep-submicron technologies have ~1V as the core MOS rated voltages and at-max 2.5V for thick-oxide I/O MOS devices. In order to handle 4+V battery voltage careful stacking/design is required. During the course of the project, we will work on both capacitive and inductive converters. In this part of project, we will focus on capacitive converters and low voltage LDO's in order to regulate capacitive converter output. We will focus on an inductive converter solution in the future part of the project.

SUMMARY OF RESULTS

Capacitive converter: We implemented a software defined (SD) capacitive converter with five conversion ratios (K) and having both frequency (F) and capacitance (C) based output voltage modulation. We call this novel modulation scheme as K-F-C tuning. Fig. 1 shows the efficiency profile of SD-capacitive converter where y axis is efficiency, z axis is load current and x axis is the output voltage. For direct battery power transfer to DVS based SoC's, the wide output voltage and current ranges will be significant. The design was measured in 65 nm CMOS GP.

Low voltage LDO: In order to remove ripples from the capacitive converter, we designed the fully integrated analog LDO for sub-0.5V supply voltages. As shown in Fig. 2 (left), the LDO can operate from 0.3V-to-1.0V input voltages, and can sustain a load variation of 10mA-to-100mA at 1.0V input and 5mA-to-25mA at 0.3V input. It achieves a peak 99.1% current efficiency for a 100mA load at 0.9-V output voltage. In order to realize the gate drive at sub-0.5-V supply voltages, we introduce a negative charge pump based adaptive offset before the pass FET which provides a gate-source headroom at input operation voltages normally reserved for digital LDOs'. The prototype was fabricated in TSMC's 65 nm GP CMOS.

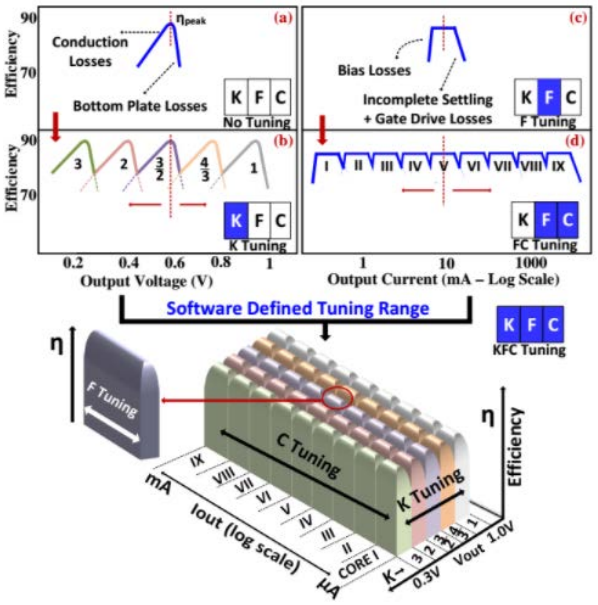

Figure 1. Efficiency profile of a capacitive converter (a) Vs output voltage (b) Vs output voltage (multiple K values) (c) Vs output current (d) Vs output current (FC tuning). Bottom 3D-plot shows KFC tuning for the proposed SDCC.

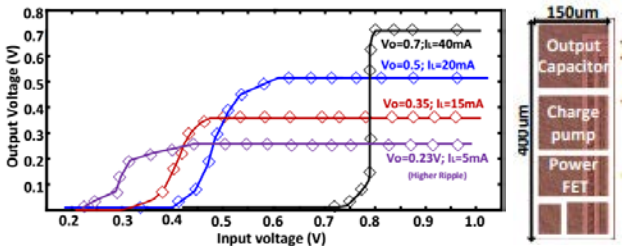

Figure 2. (Left) Output voltage Vs input voltage of Low voltage analog LDO, (Right) Chip micrograph of the LDO in 65 nm CMOS.

Keywords: direct battery to silicon, capacitive DC-DC, KFC tuning, low voltage analog LDO

INDUSTRY INTERACTIONS

Texas Instruments, Intel, IBM, NXP

MAJOR PAPERS/PATENTS

[1] Chaubey, S. & Harjani, R., "Fully Tunable Software Defined DC-DC Converter with 3000X Output Current & 4X Output Voltage Range 2010", CICC 2017, Austin.

TASK 2712.009, LOW POWER AREA EFFICIENT FLEXIBLE-RATE ENERGY PROPORTIONAL SERIAL LINK TRANSCEIVERS

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SIGNIFICANCE AND OBJECTIVES

This task seeks to explore and invent techniques to implement area and power efficient serial link transceivers that are capable of operating across a wide range of channels and data rates. The first phase of our efforts are focused on addressing the problem of baud-rate clock and data recovery circuits that can be turned on/off for achieving energy proportional operation.

TECHNICAL APPROACH

A continuous time analog front-end (AFE) consists of a CTLE (Continuous time linear equalization) followed by a variable gain amplifier (VGA). A quarter rate architecture is chosen for the discrete equalizer to reduce the clocking frequency. Each equalizer slice consists of a two-tap FFE (Feed Forward Equalizer) and two-tap DFE (Decision Feedback Equalizer). The outputs of the deserializer go to a digital logic block that combines Mueller-Muller CDR logic, burst- mode operation logic (BM), and reference as well as equalizer coefficients. The quarter rate architecture makes use of two phase rotators that provide four clock phases, ϕ_0, ϕ_{90}, ϕ_{180}, and ϕ_{270}.

SUMMARY OF RESULTS

The proposed receiver shown in Fig. 1 is designed and fabricated in a 65nm CMOS process. We will characterize its performance and report the results. In parallel, we are also investigating alternate baud-rate CDR architectures for sub-rate operation. Near future goals include exploration, design, and implementation of such sub-rate baud-rate CDRs.

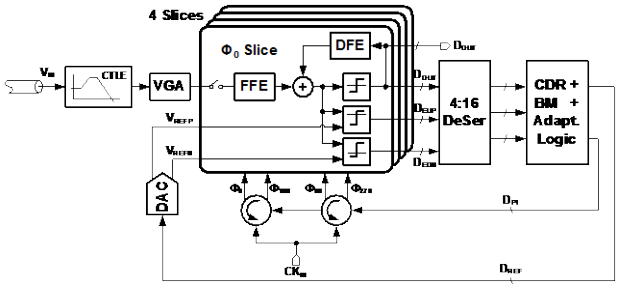

Figure 1. Proposed rapid on/off receiver with decision feedback equalizer and baud-rate CDR.

Keywords: baud-rate CDR, DFE, energy proportional

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

TASK 2712.012, EDAC AND DC-DC-CONVERTER CO-DESIGN FOR ADDRESSING ROBUSTNESS CHALLENGES IN EMERGING ARCHITECTURE

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SIGNIFICANCE AND OBJECTIVES

The goal of this project is to develop techniques on error detection and correction (EDAC) and DC-DC converter co-design for the post Moore's law era where aggressive architectures and circuits will be explored to continue performance and energy-efficiency scaling while ensuring robustness and reliability.

TECHNICAL APPROACH

We will devise the following techniques: (i) direct error regulation to make DVS energy-efficient and fully-digital while miniaturizing capacitor sizes in integrated switched-capacitor converters; (ii) EDAC+Converter for non von-Neumann and parallel architecture, such as error correction schemes for super-Vth circuits performing no instruction replay, and techniques for in and around embedded memory; (iii) EDAC+DVS for clock domain crossing with focus to simplify clock distribution and generation. We anticipate to prototype two chips to demonstrate those techniques in 65-nm or 45-nm CMOS.

SUMMARY OF RESULTS

In this period (Mar/2017-Apr/2017), we have disseminated our preliminary work on direct error regulation [1]. A microprocessor (µP) designed in near-threshold (near-V_{TH}) circuits can be highly energy-efficient. A key challenge is to address the large delay variability from process, voltage, and temperature (PVT) variations. In-situ timing error detection and correction (EDAC, aka Razor) technique has been explored, where it dynamically modulates supply voltage (V_{DD}) so as to make a µP operate at the edge of point of first failure (P_{oFF}) without the worst-case margin. This approach requires a power-management unit (PMU) to produce variable V_{DD} in the near-V_{TH} level. Existing works [1] use a voltage regulation scheme which regulates V_{DD} to reference voltage (V_{REF}) while varying V_{REF}.

This voltage regulation scheme however poses three main challenges. First, those PMU's require a variable V_{REF} generator (DAC) and comparators (CMP) but as the power consumption of a µP substantially is reduced at near-V_{TH} (the processor used here consumes ~25µW at 0.45V & FCLK=10MHz), that of DAC+CMP becomes important. The power of DAC+CMP can be reduced at the cost of operation speed, however, a large delay of DAC+CMP can also negatively affect energy efficiency and transient performance of PMU. Indeed, the latency poses a trade-off with power dissipation in DAC+CMP design. Thus, it is not trivial to improve both. Second the analog/mixed-signal circuits used in the conventional PMU can limit input voltage (V_{IN}). Limited V_{IN} scalability is undesired especially for emerging energy sources with sub-1V output such as harvesters and capacitors since they need redundant voltage conversions among energy sources, storage, and load. Finally, the PMU output (i.e., V_{DD}) may vary, e.g., ripples in switching power converters. In the worst-case design practice, this requires to increase VDD by the amount of ripples, increasing µP power dissipation and thus worsening system-level efficiency.

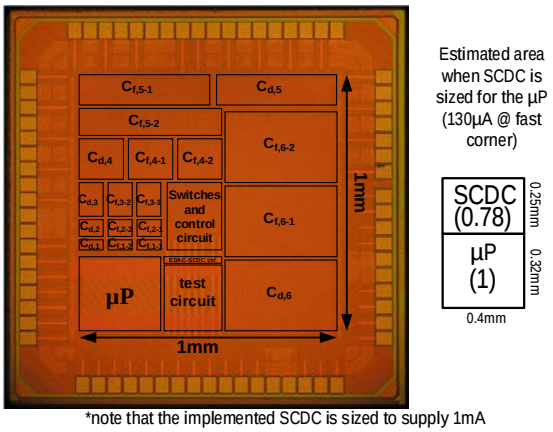

Figure 1. Test-chip Die Photo of the microprocessor and SCDC-PMU based on the proposed direct error regulation.

We demonstrated a co-design approach of µP and PMU system which can address these challenges. The system consists of (1) a µP employing near-V_{TH} EDAC; (2) 63-ratio integrated switched-capacitor DC-DC converter (SCDC); and (3) fully-digital EDAC-SCDC controller. The test-chip was prototyped (Fig. 1), demonstrating 45% system-level energy efficiency improvement over conventional design based on voltage regulation. The area overhead of EDAC in the µP is 3.2%, and that of error controller is 2.3% of the µP area.

Keywords: near/sub-V_{TH} digital circuits, power converter, direct error regulation

INDUSTRY INTERACTIONS

Intel

MAJOR PAPERS/PATENTS

[1] S. Kim, M. Seok, "Ultra-Low-Power and Robust Power-Management/Microprocessor System Using Digital Error-based Regulation," IEEE European Solid-State Circuits Conference (ESSCIRC), 2017, in press.

TASK 2712.016, 3D IC THERMAL MANAGEMENT BASED ON TSV PLACEMENT OPTIMIZATION AND NOVEL MATERIALS

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NADER BAGHERZADEH, UNIVERSITY OF CALIFORNIA, IRVINE

SIGNIFICANCE AND OBJECTIVES

The main objective is to include thermal TSV designs early in the system design process and provide thermal management solutions by addressing the workload and TSV design parameters (i.e., size, location, and material). The outcomes will lead to continued device scaling, performance improvement, and effective thermal management for 3D ICs.

TECHNICAL APPROACH

Based on a cross-disciplinary approach, we will evaluate the impact of thermal TSV's in multi-layer 3D IC's. First, several benchmarks are selected to reflect actual workloads using Gem5, providing an accurate estimation of the number of data packets traversing the TSV's for a specific workload. Mcpat estimates the power consumption of all the system components, especially the signal TSV's. Using the extracted power estimations, Hotspot generates a temperature floorplan of the system hardware down to the level of the TSV's. Finally, machine learning heuristics will be utilized to optimize the thermal and power consumption for the 3D IC.

SUMMARY OF RESULTS

In order to investigate the effect of adding thermal TSV's on the overall reduction of the TSV bundle temperature, simulations are conducted with and without the existence of thermal TSV's. We assume a 16-byte cache line that is represented by 128 bits grouped in one TSV bundle as 8 rows and 16 columns. The thermal results of the TSV bundle under a benchmark workload at a specific time show that the TSV number 51 is traversing signals at the maximum heat that correspond to 344.52-degree K. If TSV number 51 is surrounded by thermal TSV's that are grounded in both ends for the purpose of transferring the heat to the heat sink below the TSV layer (not shown in the figure), signal TSV's number 34, 35, 36, 50, 52, 66, 67 and 68 will be replaced by thermal TSV's (Figure 1a). As a result, the overall heat is decreased by more than 2 degrees. However, the number of TSV's will increase to 128 + 8 which is equal to 136 TSV's. To reduce that overhead, thermal TSV's could be applied using materials other than the usual copper that have better thermal conductivity, and these strategies will be further assessed using thermal simulators. These preliminary results are generated using Hotspot which has a high degree of flexibility to precisely evaluate the heat distribution in the whole system including the TSV's. They include the chip and TSV dimensions, position and temperature parameters.

In parallel, analytical and numerical thermal models are constructed and validated. Our analytical thermal model utilizes the thermal healing length approximation, which provides a length scale metric to optimize the location of TSV's. We have performed numerical thermal simulations using a finite element model to evaluate the impact of TSV's on temperature distributions in the system configuration that matches the electrical system-level simulators (Figure 1(b)). The models will be extended to multilayers and to evaluate the antenna effects incurred by surrounding metallic TSV's. Subsequently, an optimization algorithm for TSV floor planning will be developed to optimize the arrangement of thermal TSV's and to consider the use of novel materials. The synergy among the proposed tasks in the cross-layer modeling framework will lead to outcomes, which will be of value.

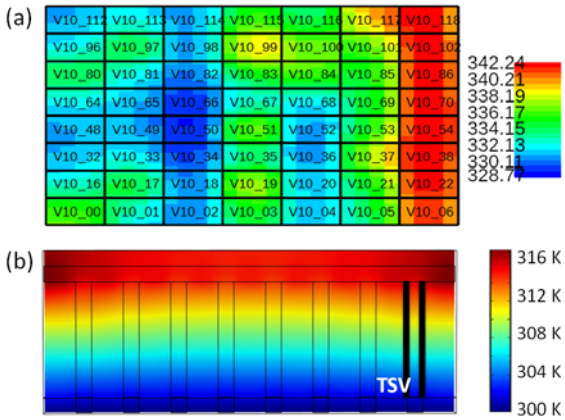

Figure 1. (a) Temperature floorplan of a 128 bit TSV bundle organized as 8 rows by 16 columns under a certain workload at a specific time, using Hotspot software. (b) Finite-element-based numerical thermal simulation result showing a cross-sectional temperature distribution in the 8-row TSV arrangement that is consistent with the 128-bit TSV floorplan.

Keywords: thermal modeling, heat transfer, passive cooling, Through-Silicon Via, electrothermal analysis

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

TASK 2712.018, TEST TECHNIQUES TO APPROACH SEVERAL DEFECT-PER-BILLION FOR POWER ICS

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SIGNIFICANCE AND OBJECTIVES

Existing test techniques for Power ICs and analog parts examine the part external terminals using a black box model but are insufficiently selective. This work will identify Power IC subcircuits prone to failures caused by outlier performance inside the sub-circuits using LDO's and Buck Converters as test vehicles.

TECHNICAL APPROACH

Task researchers will examine sub-circuit performance inside of LDO's and Buck Converters in order to achieve several orders of magnitude better discovery of power IC defects. This approach adds additional test points for bare die wafer probe. The test points are either in the wafer scribe lanes or are internal IC test pads that packaging makes inaccessible. Bare-die power IC probing allows the measurement of DC and small signal responses of sub-circuits and devices. In addition, bare die probing allows for precise control of wafer temperature and driving wafers to very cold regions of operation (up to -40^{o}C).

SUMMARY OF RESULTS

This task will develop bare die IC test strategies in simulation and then in fabricated ICs to observe following sub-circuits and IC devices.

[1] Differential circuit performance and imbalance in power IC feedback loops can cause failures. Very imbalanced differential circuits can lead to high device currents and unanticipated high biasing drain or gate voltages that in turn can cause transistor reliability issues.

[2] Power transistor weaknesses in manufactured gate structure, threshold voltages, internal current distribution, etc. can cause failures.

[3] Power IC circuit resistor and capacitor values at the edge of process tolerances can cause failures. IC resistors can vary +/-20 percent from nominal values and these resistors can set transistor bias voltages and currents in the power IC.

[4] Charge pump circuits that are producing significantly higher than nominal voltages can cause failures. If these values are too high, then there can be transistor reliability issues causing circuit failures in the field.

[5] Localized I_{DDQ} and leakage measurements identify power IC sub-circuits that are grossly out of specification. This will provide a much more fine grain supply current resolution for determining out of specification performance of the sub-circuits in the power IC.

We will initially work in collaboration with of Prof. Shuo Wang, a power electronics and with Prof. Nima Maghari, an analog IC and data converter design, to develop LDO general LDO designs that we can add the test concepts to.

The PI and students will develop LDO redesigns for enhanced internal test node observability connected with test pads in the scribe lanes. The researchers will work with Texas Instruments to provide us with LDO samples to demonstrate our test concepts and to provide the testing for these designs at TI.

We will look at operating these power IC test circuits in normal and low temperature operation and under DC and small signal test using an IC tester. Imperfections and high sigma outlier parameters that allow the LDO system to work under its internal feedback loops but create reliability issues will be investigated. The simulated test concepts will be transferred to TI by UF graduate students during student internships at TI. In addition, to the TI device fabrication the researchers will seek affordable IC design space on older IC processes in foundries such as MOSIS in order to show power IC test concepts.

Test Selection: The PI will focus on the using feedback control nodes and biasing nodes to control and test power transistors, and differential circuits. The test selection goal is to determine three to five internal IC observation nodes that can find faults in the LDO sub-circuit performance under wafer probe. The research team will run Monte Carlo simulations over process variations and perform fault determination at low temperature and room temperature. Then test approaches will be compared and the most promising ones will be identified.

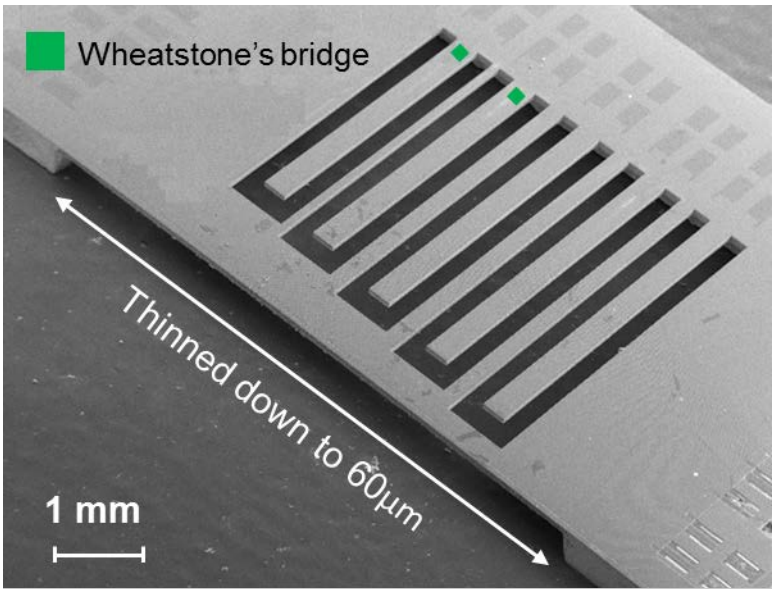
Keywords: test, analog, power, LDO, buck converter

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

Safety, Security and Health Care Thrust



Category	Accomplishment
Safety, Security and Health Care (Systems)	Terahertz spectrometers can be used for a variety of applications including process monitoring and gas detection. In this task, a terahertz spectrometer has been used within an Applied Materials plasma reactor for process diagnostics. Studies have been completed which show that the spectrometer can accurately measure densities of plasma constituents for a number of gas mixtures including CF_2, FCN, HCN, CO and others. (1836.126, DeLucia, OSU)
Safety, Security and Health Care (Systems)	Vibration sensors can be used for infrastructure and machine monitoring. A vibrometer has been fabricated using a TI CMOS process. The chip includes an array of cantilevers designed for measurements across a wide range of frequencies, DC to 10kHz, with an 1-mg resolution. Measured DC sensitivity for the longest cantilever (~2mm) is ~0.07mV/g for a 20V input. (1836.155 Pourkamali, UTD)

TASK 1836.119, DEMONSTRATION OF 180-300 GHZ TRANSMISMITTER FOR ROTATIONAL SPECTROSCOPY

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SIGNIFICANCE AND OBJECTIVES

As part of the effort to help open up the high millimeter and sub-millimeter wave frequency range for moderate volume and cost applications, this task is seeking to demonstrate a 180-300 GHz transmitter in CMOS for a rotational spectrometer that can be used to detect harmful molecules in air and to analyze breaths.

TECHNICAL APPROACH

The transmitted power should be ~10-100 uW. The main challenges are increasing the output frequency range, power, and frequency for phase locked signals. To realize a fast scan rate with a 10-kHz step, a fractional-N synthesizer is used. The synthesizer also incorporates a frequency modulation function. The output signal generation uses a combination of an N-push technique and frequency multiplication/translation techniques. This task will also help generating the receiver LO signal.

SUMMARY OF RESULTS

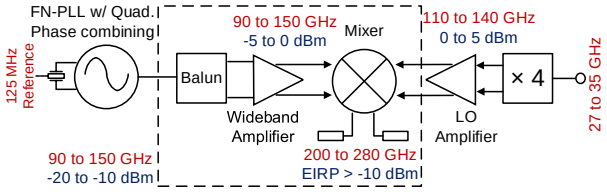

Figure 1. Block diagram of transmitter with power and frequency plans.

A 200-280 GHz RF front-end of transmitter (dotted box in Fig. 1) is demonstrated in 65-nm CMOS. The power and frequency plans for the transmitter are also shown in Fig. 1. The measured saturated EIRP of TX front-end is greater than -5dBm over a frequency range of 60GHz. When the input power is -20dBm, EIRP is greater than -10dBm, and achieves percent 3-dB and 6-dB bandwidths of 24% and 33%. The front-end was integrated with a fractional-N synthesizer to form a transmitter operating at 208-255GHz with measured EIRP of -18 to -11dBm.

Fig. 2(a) shows 200-250-GHz transmitter and receiver in a rotational spectroscopy set up. Fig. 2(b) shows correlation of the blood glucose level measured using a blood test and that estimated using a machine learning algorithm on non-invasive measurements from Type-I diabetic patients including acetone concentration in breath. The number of samples is not yet sufficiently large to make the results reliable but this suggests things to come. Fig. 2(c) shows the Ethanol line detected from a human breath using the CMOS IC's demonstrating that CMOS will be able to support practical applications at 200-300 GHz.

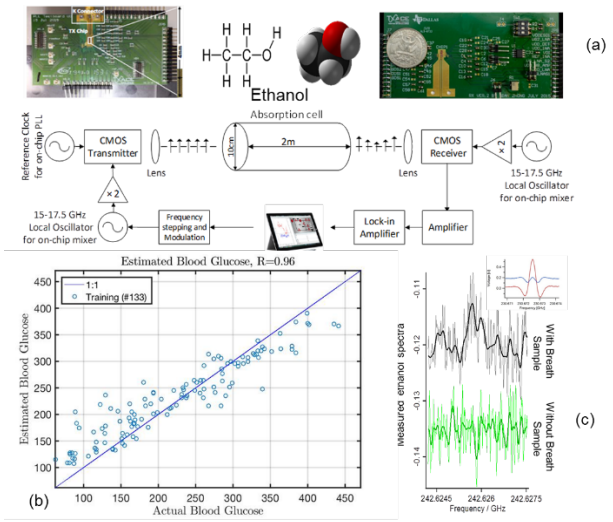

Figure 2. (a) 200-250-GHz TX and RX in a rotational spectroscopy set up, (b) Blood glucose level estimated from non-invasive tests including analyses using rotational spectroscopy for Type-I diabetic patients, (c) Ethanol line detected from a breath using the CMOS IC's.

Keywords: rotational spectrometer, transmitter, CMOS, millimeter-wave

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] J. Zhang et al., "85-to-127-GHz CMOS Signal Generation using a Quadrature VCO with Passive Coupling and Broadband Harmonic Combining for Rotational Spectroscopy," IEEE Journal of Solid State Circuits, vol. 50, no. 6, pp. 1361-1371, June 2015.

[2] N. Sharma et al., "200-280GHz CMOS RF Front-End of Transmitter for Rotational Spectroscopy," 2016 IEEE Symposium on VLSI Technology. pp., June 2016, Honolulu, Hi.

[3] N. Sharma and K. K. O, "160–310 GHz Frequency Doubler in 65-nm CMOS with 3-dBm Peak Output Power," 2016 IEEE RFIC Symposium, pp. 186-189, May, 2016, San Francisco, CA.

TASK 1836.120, EVALUATION OF FREQUENCY AND NOISE PERFORMANCE OF CMOS 180 – 300 GHZ SPECTROMETER TRANSMITTER AND RECEIVER COMPONENTS

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SIGNIFICANCE AND OBJECTIVES

A gas phase absorption spectrometer in the 100 to 1000 GHz frequency range would be extremely valuable to rapidly and precisely assay a wide range of chemical vapors. This project's objective is to quantitatively evaluate passive materials and passive and active devices for suitability as millimeter-wave components to be integrated into a spectrometer system.

TECHNICAL APPROACH

The past year of this project undertook: (1) further detailed measurements on transmittance and reflectance spectra of passive dielectric materials and numerical extraction of their complex index of refraction values as a function of frequency; (2) set-up of the free-space receiver noise temperature measurement platform; and (3) determination of the signal-to-noise ratio (SNR) limits when using a Fourier transform spectrometer (FTS) to measure the frequency spectrum of CMOS oscillators broadcasting into free-space.

SUMMARY OF RESULTS

In collaboration with Dr. Rashaunda Henderson (UTD, EE) and Dr. Julia Hsu (UTD, MSEN) we added detailed high-resolution reflection and transmission measurements of the very-low index polymer substrate polymethacrylimide (PMI) obtained from Rohacell and the transfer print lithography polymer polydimethylsiloxane (PDMS) to the catalog of dielectric materials we have measured. We also fixed some algorithmic inconsistencies with the numerical model used to solve the simultaneous non-linear equations relating the measured data to the real and imaginary parts of the index of refraction at each frequency.

In collaboration with Qian Zhong (Dr. Ken O's student) and Dr Wooyeol Choi (UTD, TxACE) we set up a free-space receiver noise temperature measurement capable of testing a probe-contacted CMOS receiver circuit in a standard Cascade probe station. The difficulty to this set-up was fitting all components onto the restricted area of a probe station while maintaining required optical lines-of-sight needed for both placing probes and for bringing RF signal to the receiver circuit. This noise measurement is via a "hot/cold load" where the receiver output power ratio is measured between two blackbody RF inputs at 77 ^{o}K and 295 ^{o}K. We tested one unpackaged 210-305 GHz receiver. However, its expected noise figure (NF) of 14-19 dB was at the edge of the SNR limits of the hot/cold load measurement system and the results could only say that the receiver NF ≥ 16 dB.

In collaboration with Navneet Sharma (Dr. Ken O's student) and Dr Wooyeol Choi (UTD, TxACE) we determined the SNR limit of using a FTS to measure the free-space broadcast frequency spectrum of CMOS mixer/multiplier oscillators. We found that to be a useful characterization tool, a spectrum should be acquired in ≤ 20 mins. Based on this integration time, the instrumental SNR = 1 at –42 dBm power collected at the input mirror of the FTS for a 240-GHz source. For many prototype CMOS oscillator designs this is a usefully low noise floor for frequency spectrum diagnostics. An example spectrum for a prototype CMOS mixer source set to output at 240 GHz is shown in Fig. 1. The primary 240 GHz signal and various harmonics generated by the source are shown along with the system noise amplitude.

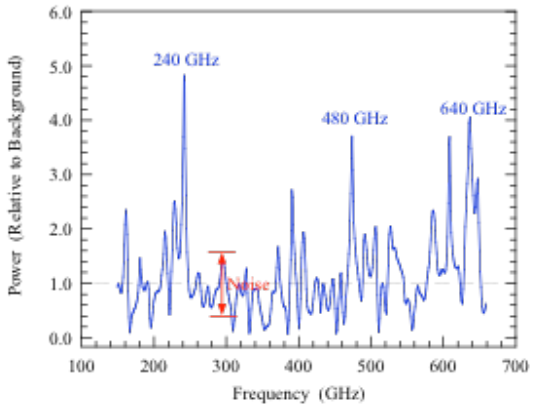

Figure 1. Free-space output spectrum as measured on a Fourier transform spectrometer of a CMOS multiplier oscillator circuit (unpackaged) set to output at 240 GHz. The noise power amplitude is indicated in red.

Keywords: millimeter-wave, terahertz, spectrometer, dielectric loss, power meter

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] E. Motaharifar, R. Henderson, and M. Lee, "Broadband Terahertz Refraction Index Dispersion and Loss of Polymeric Dielectric Substrate and Packaging Materials", to be submitted to *J. Infrared & Millimeter Waves.*

TASK 1836.122, ON-CHIP INTEGRATION TECHNIQUES FOR 180-300 GHZ SPECTROMETERS

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SIGNIFICANCE AND OBJECTIVES

This work develops techniques to integrate broadband antennas into RFIC's for 180-300 GHz CMOS-based spectrometer demonstration.

TECHNICAL APPROACH

The technical approach includes the development of fabrication processes to integrate broadband antennas with standard processed CMOS ICs; characterization of those antennas and co-development of broadband on-chip antennas.

SUMMARY OF RESULTS

An aperture bowtie antenna served as the demonstrator structure due to its ability to achieve 50% bandwidth for integration with broadband ICs fabricated by the students of Prof. K. K. O. Texas Instruments sponsored a multilayer laminate process run and UT Dallas fabricated standalone antennas on FR4 and silicon. The silicon designs require an electromagnetic bandgap (EBG) sub-layer to shield the RFIC's and provide the proper reflection phase for broadband performance. Fig. 1 shows an antenna with 4 EBGs surrounding the antenna, and achieves a 50-% bandwidth for return loss. The EBG patches are 0.230 mm on a side with 0.045 mm gaps. The EBG is separated from the ground and antenna layer by 0.075 mm.

Through collaboration with O's team to enhance the bandwidth of a foundry processed dipole, we manufactured an artificial magnetic conductor (AMC) on FR408 to improve the bandwidth by compensating the phase. Fig. 2 shows the antenna on top of the array comprised of 0.030 mm x 0.030 mm gold patches. This antenna is compact (less than 1 mm on a side) and has a 37-% bandwidth.

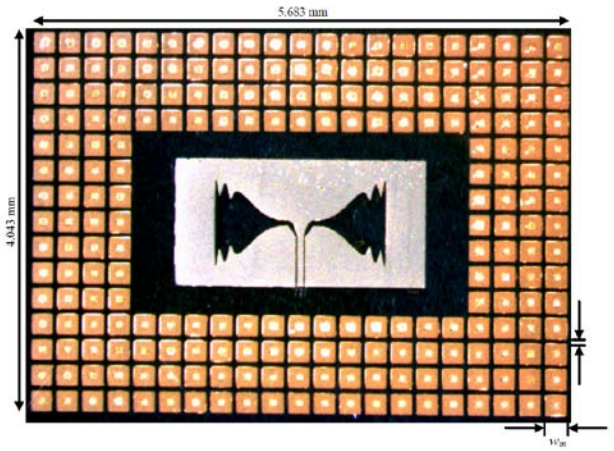

Figure 1. UT Dallas processed aperture bowtie antenna fabricated on silicon and benzocyclobutene multilayer stack. The antenna area without EBG is 2.7 mm x 1.4 mm.

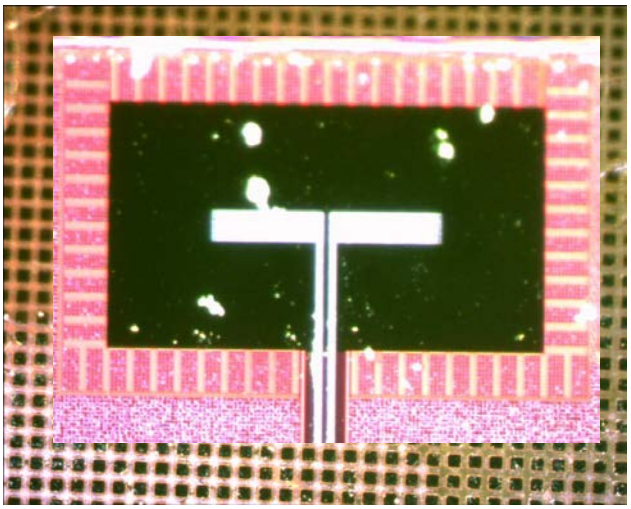

Figure 2. Foundry processed dipole antenna placed on artificial magnetic conductor (AMC) fabricated on FR408 substrate. Dipole area is 0.5 mm x 0.6 mm.

Keywords: aperture bowtie antenna, dipole antenna, artificial magnetic conductor

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] C. Miller, *Measurement of Millimeter-Wave On-Chip Antennas*, Master's Thesis, Dept. of Elect. Eng., UT Dallas, 2016.

TASK 1836.126, DESIGN SPIN REDUCTION VIA INTEGRATED THZ DESIGN: APPLICATIONS, PHYSICS, AND SYSTEM ENGINEERING

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SIGNIFICANCE AND OBJECTIVES

The objective of this project is to develop a THz System Engineering Tool that allows for analysis of systems based on the characteristics of their building blocks and to validate it by applications to systems of interest. These systems include CMOS gas sensors and systems for process diagnostics and control.

TECHNICAL APPROACH

This effort includes: (1) diagnostics and process control in semiconductor plasma reactors, and (2) in parallel the development of CMOS systems for this application, as well as more generally for gas sensors. We are also developing a computational System Evaluation Tool to aid in the design of these CMOS circuits.

SUMMARY OF RESULTS

Our effort is to demonstrate and explore applications of CMOS terahertz technology and to support development of appropriate technology. This effort has a number of mutually supporting pieces. Organizationally, we will discuss results in the context of our effort to develop a terahertz tool for the study, characterization, and process control of plasma processors for semiconductor chip manufacturing.

Physics makes this application favorable. The working pressures of these reactors, 5 – 50 mTorr, are optimal for spectroscopy in the THz and many molecules of interest have strong spectra in the THz. Moreover, these plasmas are transparent and noise free. Finally, it is an absorption technique which can provide concentration and temperatures from first principles, without system calibration.

Figure 1 shows an example of a large number of species in a variety of gas mixtures that we have studied. Molecules can have spectra whose sensitivity for trace constituents of the plasma can vary widely.

In another example, shown in Fig. 2, discharges in O_2 are often run between processing steps to clean the system and return it to a steady state. Here we show the results of using absolute measurements of the reaction product CO as an end point measurement. Modeling shows how the minimum detectable concentration varies as a function of THz system parameters.

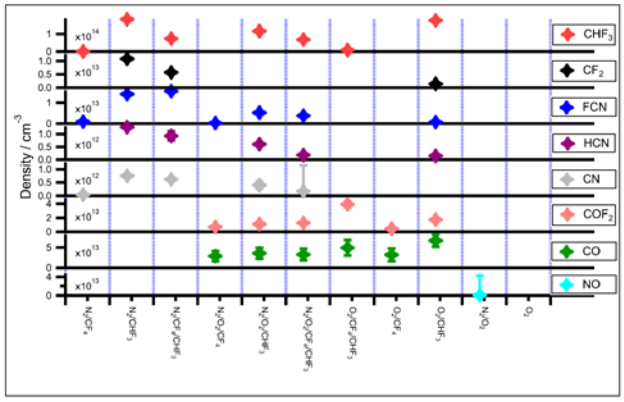

Figure 1. Measurement of absolute densities of CHF_3, CF_2, FCN, HCN, CN, COF_2, CO, and NO in a survey of plasmas produced from combinations of CF_4, CHF_3, N_2, and O_2.

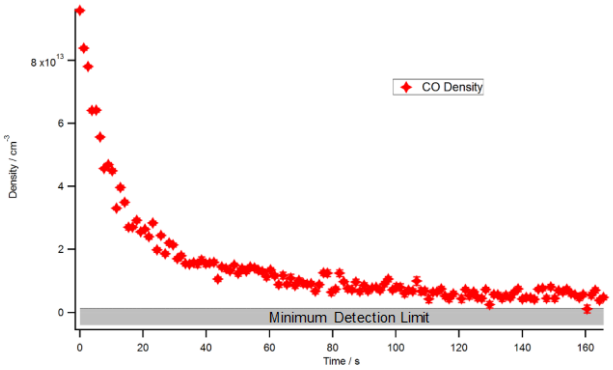

Figure 2. Measured concentration of CO in a cleaning experiment as a function of time. Also shown is the minimum detectable concentration.

Keywords: terahertz, spectroscopy, plasmas

INDUSTRY INTERACTIONS

Texas Instruments, IBM, Applied Materials

MAJOR PAPERS/PATENTS

[1] Y. Helal et al., "Spectroscopic Measurement of Molecular Densities and Temperatures in Processing Plasmas," AVS 63rd International Symposium, November 2016, Nashville, TN.

[2] F. De Lucia, "The Role of CMOS in the Development of the Submillimeter/Terahertz Spectral Region," TxACE e-Workshop, May 2016, Dallas TX.

TASK 1836.131, PROCESS VARIATION ANATOMY: A STATISTICAL NEXUS BETWEEN DESIGN, MANUFACTURING, AND YIELD

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SIGNIFICANCE AND OBJECTIVES

Wafer-level testing is a lengthy and expensive procedure particularly for Analog/RF integrated circuits. The impact of process variations on every wafer is distinct; therefore, it can be leveraged to optimize the test flow at wafer-level. As a result, test cost can be reduced while test quality remains at a target level.

TECHNICAL APPROACH

We developed an adaptive test cost reduction method, which optimizes the test flow per process signature. Indeed, depending on how a wafer has been impacted by process variations, the wafer may go through a complete test flow or a reduced test flow in order to lower the probe test time. First, wafer signature need to be extracted from e-test measurements. To do so, we project multi-dimension e-test measurements into lower space using a non-linear mapping algorithm. Next, for each group of wafers with a similar signature in the process space, probe-test flow is optimized.

SUMMARY OF RESULTS

This methodology utilizes the following principles, therefore it can be readily deployable with minimal test operations support: i) The granularity at which test elimination decisions are made is at the test group level rather than test item, ii) The granularity of the adaptation decision is at the wafer-level, i.e., all die on a wafer are subjected to the same test flow and iii) The decision is driven by a signature which reflects how process variations have affected a particular wafer.

We evaluated the effectiveness of our proposed methodology using industrial dataset of an RF transceiver. E-test measurements are the only information that is available before a wafer reaches a probe station. Fig. 1 presents the projected e-test space into two major components, where each point represents a wafer. As can be seen, wafers are grouped based on their process variation signatures. Then, the ILP-based optimization method assigned a proper test flow to each process signature to maximize the test cost reduction while the test escape rate remains below a target level. In this figure, clusters with the same marker/color have the same probe-test flow. The optimized test flows for selected clusters in this figure are shown on the bottom right of the figure.

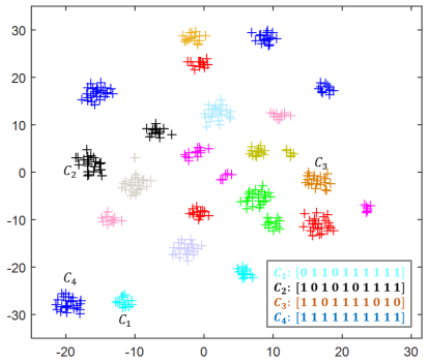

Figure 1. Final assignment of the optimized probe-test flow.

Fig. 2 demonstrates the test cost vs. test quality trade-off for various DPPM levels. The horizontal axis is the target DPPM level, and the vertical axis shows the percentage of test cost reduction. As it can be seen, the adaptive nature of the proposed test flow selection approach enables the exploration of test cost vs. test quality even for very low DPPM levels.

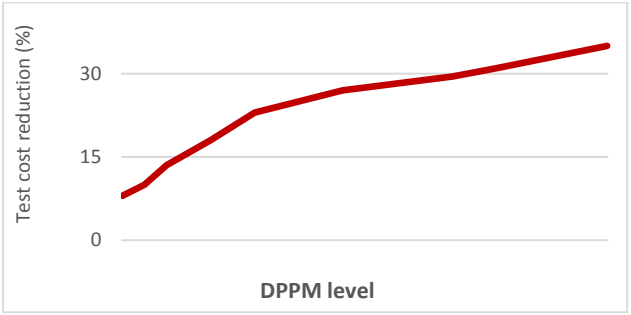

Figure 2. Test cost reduction vs. test accuracy.

Keywords: process signature, test cost reduction, test flow optimization, test escape rate

INDUSTRY INTERACTIONS

Texas Instruments, Intel, Globalfoundries

MAJOR PAPERS/PATENTS

[1] A. Ahmadi, A. Nahar, B. Orr, M. Pas, and Y. Makris, "Wafer-Level Process Variation-Driven Probe-Test Flow Selection for Test Cost Reduction in Analog/RF ICs, "IEEE VLSI Test Symposium, 2016.

[2] A. Ahmadi, C. Xanthopoulos, A. Nahar, B. Orr, M. Pas, and Y. Makris, "Harnessing Process Variations for Optimizing Wafer-level Probe-Test Flow," IEEE International Test Conference, 2016.

TASK 1836.135, SUB-PICOSECOND SYNCHRONIZATION OF WIDELY SPACED IMAGING ARRAYS

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SIGNIFICANCE AND OBJECTIVES

Tight synchronization of a distributed array with widely-spaced sparse elements is a key enabler in coherent combining of signals in space. The objective of this project is to build a wireless synchronization link capable of synchronizing a master node to multiple slave nodes with timing jitter of 500fsec in less than 10nsec.

TECHNICAL APPROACH

To achieve wireless synchronization with a sub-picosecond accuracy, we have designed and fabricated an impulse receiver based on a three-stage divide-by-8 injection-locked frequency divider. A broadband planar inverted cone antenna with a broad radiation pattern is used to receive the radiated pulses. A narrowband 80-GHz LNA amplifies one of the frequency tones close to the center frequency of the pulse and the injection-locked divider chain extracts the clock (~ 10 GHz) out of this high-power tone. This receiver is designed to extract the pulse repetition rate while adding minimum jitter to it.

SUMMARY OF RESULTS

The architecture of the receiver is shown in Fig. 1. This receiver was fabricated in a Globalfoundries 65-nm CMOS technology and has been tested using a silicon-based picosecond pulse radiator.

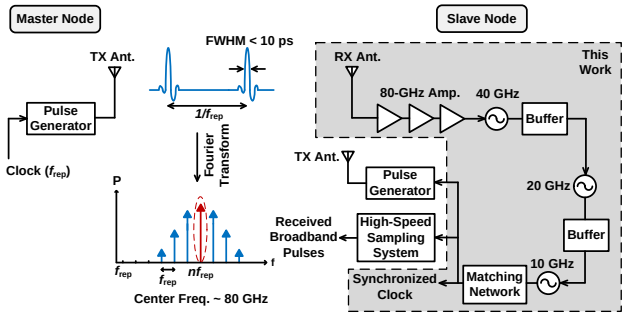

Figure 1. Injection-locked pulse receiver architecture [1].

Fig. 2 summarizes the measured results of the wireless time transfer test using a psec pulse radiator. The spectrum and the phase noise of the receiver output, before and after locking, are compared in Figs. 2(a) and (b). The time-domain waveform of the locked output is shown in Figs. 2(c) and 2(d), indicating a measured 290fs output rms jitter compared to the 260fs rms jitter of the original source used to trigger the pulse radiator.

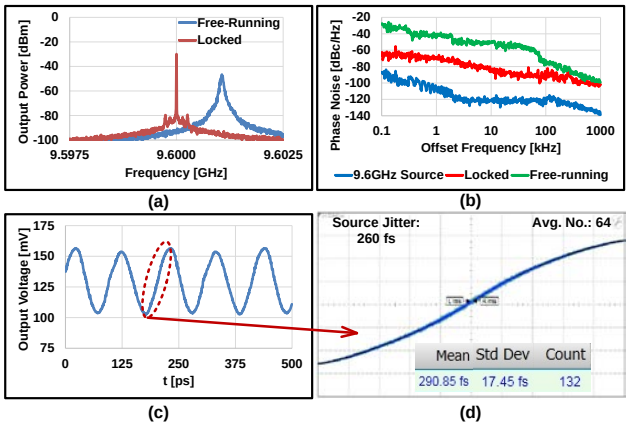

Figure 2. Measurement results of the wireless time transfer test using picosecond pulses.

Compared with our previous work which was based on a self-mixing scheme [2], this receiver achieves a lower rms jitter since it extracts the clock from a single tone and it does not accumulate noise over a wide frequency range. The micrograph of the injection-locked receiver, which occupies an active area of 0.46 mm^2 is shown in Fig. 3.

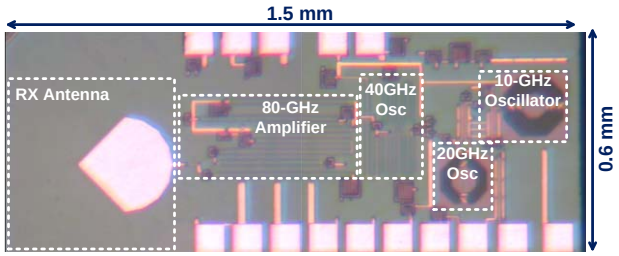

Figure 3. Chip micrograph of the injection-locked receiver.

Keywords: CMOS, injection-locking, millimeter-wave, ultra-short pulses, wireless time synchronization.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] B. Jamali and A. Babakhani, " A Fully Integrated Injection-Locked Picosecond Pulse Receiver for 0.29psrms-Jitter Wireless Clock Synchronization in 65nm CMOS," IEEE MTT-S Int. Microwave Symp., June 2017.

[2] B. Jamali and A. Babakhani, "Sub-picosecond Wireless Synchronization Based on a Millimeter-Wave Impulse Receiver with an On-chip Antenna in 0.13m SiGe BiCMOS," IEEE MTT-S Int. Microwave Symp. , May 2016.

TASK 1836.147, DEMONSTRATION OF 180-300 GHZ RECEIVER FOR ROTATIONAL SPECTROSCOPY

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SIGNIFICANCE AND OBJECTIVES

Rotational spectroscopy enables detection of gas molecules with absolute specificity. One of the key building blocks for affordable rotational spectrometers is a CMOS transceiver. A wideband receiver for detection of multiple gas molecules are developed using CMOS technologies and verified in rotational spectrometers.

TECHNICAL APPROACH

A wideband receiver is proposed and fabricated in a 65-nm CMOS process. The receiver is based on a sub-harmonic passive mixer using anti-parallel diode connected NMOS transistor pairs. A 120-GHz LO driver chain and a 20-GHz IF low noise amplifier followed by an AM detector are co-designed and integrated with the mixer to achieve best sensitivity. A wideband hybrid for RF/LO/IF combining and isolation is proposed and designed. Integration and co-optimization of wideband radiators is also investigated. The performance of the receiver is evaluated both in radiation measurements and spectrometer systems.

SUMMARY OF RESULTS

Figs. 1 and 2 depict a diagram of the 225-280-GHz receiver and a receiver module for characterization and spectrometer experiments, respectively. The receiver is composed of an on-chip radiator, a sub-harmonic mixer, a 20-GHz IF LNA, a frequency quadrupling LO driver and an AM detector followed by a buffer amplifier.

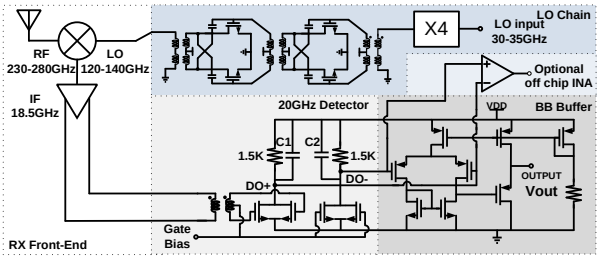

Figure 1. 225-280-GHz CMOS receiver circuit diagram.

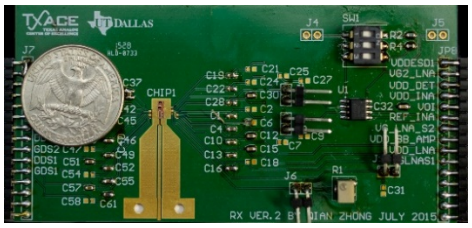

Figure 2. CMOS receiver module (10cm X 5cm).

The module is characterized in a radiation measurement setup similar to that in [1]. A 200-kHz amplitude modulated signal source is used as an input to evaluate the responsivity and the noise equivalent power (Fig. 3). The CMOS receiver module is employed in the rotational spectroscopy setup (courtesy of Prof. F. De Lucia) to perform gas molecule detection. Fig. 4 shows a part of spectrum measured using the CMOS receiver and a commercial transmitter. The measured spectral lines match with those in JPL library (blue).

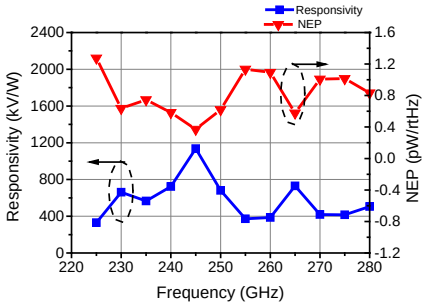

Figure 3. Performance of 225-280-GHz CMOS receiver.

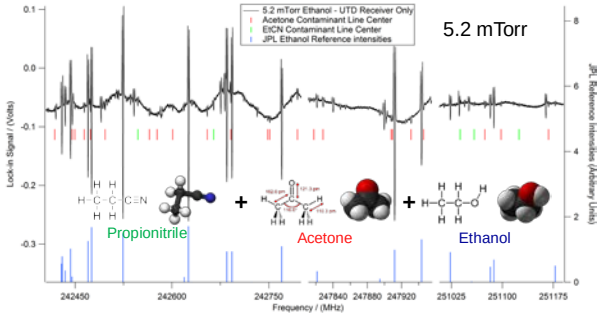

Figure 4. Measured spectrum of 5.2mTorr Ethanol with EtCN and Acetone contamination.

Keywords: integrated receiver, NFET APDP, on-chip radiator, sub-harmonic mixer, rotational spectroscopy

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] N. Sharma et al., "200-280GHz CMOS RF front-end of transmitter for rotational spectroscopy," IEEE Symp. VLSI Tech., June, 2016, Honolulu, HI, USA.

[2] Q. Zhong et al., "Wideband Receiver Front-End with Phase Compensated AMC Reflector, Wideband Hybrid and Floating Body NMOS APDP Sub-Harmonic Mixer," filed with USPTO, June, 2016.

TASK 1836.150, ROBUST HIGH RESOLUTION TECHNIQUES FOR MILLIMETER WAVE RADARS IN COMPLEX ENVIRONMENTS

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SIGNIFICANCE AND OBJECTIVES

Advancements of silicon semiconductor technology have had the profound impact on the design of mm-wave radar systems, providing higher integration and performance at lower cost. This task develops robust high resolution estimation techniques with low computational complexity for millimeter wave imaging in complex environments.

TECHNICAL APPROACH

Novel algorithms are designed to localize targets jointly across multiple dimensions using superresolution techniques. Low complexity imaging algorithms are developed using a two-stage process. The first stage is implemented using low resolution FFT based digital beamforming. Super-resolution techniques are applied at the second stage to the areas where a higher resolution is desired. Furthermore, the proposed algorithms are validated with electromagnetic simulators as well as with 24-GHz radar testbed at UT Dallas.

SUMMARY OF RESULTS

Digital beamforming (DBF) based fast Fourier transform implementation (FFT) can efficiently determine the incident angles, range, and Doppler in mm-Wave radars/imagers. Super-resolution techniques use different mechanisms to improve the resolution limit determined by the antenna/sample size. These techniques are data dependent. The 3D information such as (range, angular direction, and Doppler shifts) about targets is embedded in a rank deficient matrix formed from noise-free data. With noisy data, the appropriate subspace is estimated, usually with the eigenvalue decomposition (EVD), and the 3D parameters are extracted from the estimated subspaces. The complexity of 3D joint superresolution algorithm lies in the cost of EVD of covariance matrix and 3D exhaustive search over entire range of (range, angular direction, Doppler) domain. The FFT based DBF techniques have a low complexity of implementation; however, they have limited resolution limited by the system parameters. Thus, there exists a tradeoff between resolution and complexity. To reduce the computational complexity of superresolution imaging algorithms and still have high resolution capability, we design two stage detection techniques. The first stage is implemented using 3D FFTs. This stage is known as beamspace. Then, the super resolution techniques are applied at the second stage to the areas where a higher resolution is desired. While modeling the radar systems, the targets and channels under consideration are assumed to be ideal. The targets are modeled as objects with perfect reflectivity and the signals are assumed to propagate through unobstructed paths. To verify the viability of the proposed radar algorithms in the real world, we prototyped a 24 GHz radar testbed at UT Dallas as shown in Fig. 1(a).

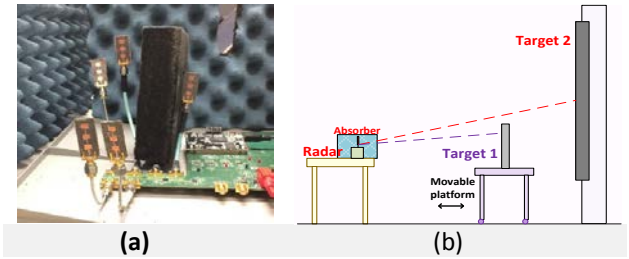

Figure 1. (a) 24 GHz mm-Wave radar testbed (b) Experimental setup to detect two targets at varying distances.

The signal bandwidth of the testbed used in these experiments is limited to 250 MHz. Hence, the range resolution of FFT based techniques is given by $\Delta R = c/250MHz$=0.6m, where $c = 3 \times 10^8$m. However, this

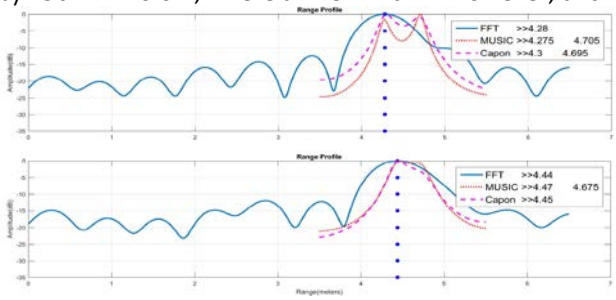

Figure 2. As the targets move closer the FFT algorithm fails. Using MUSIC at the second stage improves range resolution.

resolution limit can be improved using superresolution algorithms such as MUSIC. The bottom plot in Fig. 2 shows two targets separated by 0.2 m and their ranges resolved using the proposed two stage algorithm.

Keywords: mm-Wave imaging, space time adaptive signal processing, MIMO radar, clutter reduction

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] S. Patole et al., "Automotive Radars: A Review of Signal Processing Techniques," IEEE Signal Processing Magazine, March, 2017, vol. 34, no. 2, pp. 22-35.

TASK 1836.152, FEASIBILITY OF CMOS TRANSMITTER AND RECEIVER FOR 500-GBPS COMMUNICATION OVER DIELECTRIC WAVEGUIDE

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SIGNIFICANCE AND OBJECTIVES

The increasing bandwidth of silicon integrated circuits technology is enabling a waveguide interconnection system using sub-millimeter waves that should be able to support communication at 500-Gbps and higher. If successful, this technology will provide a bandwidth approaching that of optical systems, while bypassing the photonic component integration and coupling/packaging challenges of optical systems.

TECHNICAL APPROACH

This project in conjunction with the efforts on developing transitions and dielectric waveguides will investigate the feasibility of 500 Gbits/sec electronic communication over a 1-m dielectric waveguide using circuits fabricated in 65-nm CMOS. Use of a combination of frequency division multiple access (FDMA) (Five frequency channels), polarization division multiple access (PDMA) and a higher order signal modulation scheme will be investigated. To demonstrate the feasibility, a 120-Gbps demonstration circuit incorporating two frequency bands and two polarization modes will be implemented. Based on the results, implementation plans for a 500-Gbps dielectric waveguide communication system will be formulated.

SUMMARY OF RESULTS

Figure 1 shows a conceptual diagram of the dielectric waveguide system. It consists of transmitter, a transition/launch from the transmitter to a waveguide, a waveguide, a transition/launch from a waveguide to a receiver, and a receiver. The system uses five 45-GHz frequency bands spanning 157.5 to 382.5 GHz and supporting two polarization channels for a total of 10 channels.

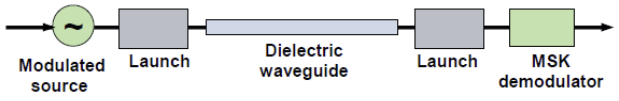

Figure 1. Conceptual diagram of the dielectric waveguide communication system.

Fig. 2 is a block diagram of transmitter for the 315-GHz band. The transmitter supports a data rate of 30Gbps with output power of -5dBm in simulation. The simulated power consumption is 200mW. Fig. 3 is a block diagram of receiver for the 315-GHz band. The receiver down converts, amplifies, demodulates and performs clock and data recovery to generate a digital output stream. Presently, the receiver can demodulate a data stream with a rate up to 10Gbps while consuming 115mW of power in simulations. The data rate is limited by the delay through the loop and approaches to increase the data rate to 30Gbps are being investigated. The receiver and transmitter designs in 65-nm CMOS have been taped out for fabrication.

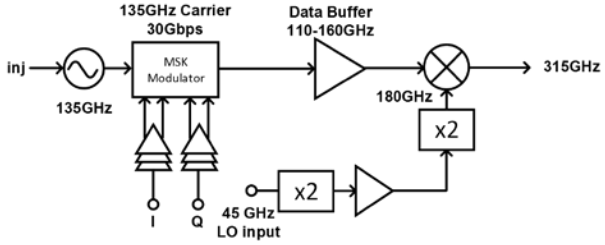

Figure 2. Block diagram of transmitter for the 315-GHz band.

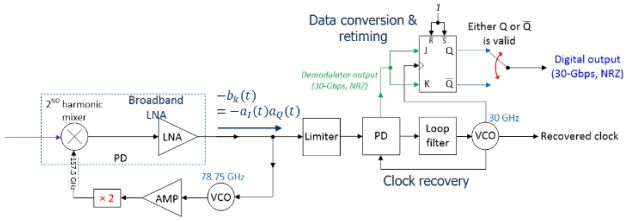

Figure 3. Block diagram of receiver for the 315-GHz band.

Keywords: dielectric, waveguide, communication, sub-millimeter, waves

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] Z. Ahmad, I. Kim, and K. K. O, "0.39-0.45THz Symmetric MOS-Varactor Freq. Tripler in 65-nm CMOS," 2015 IEEE RFIC Symposium, May 2015, Pheonix, AZ.

[2] Z. Ahmad et al., "Devices and Circuits in CMOS for THz Applications," (Invited), 2016 International Electron Device Meeting, Paper 29.8, pp. 734-737, Dec. 2016, San Francisco, CA.

[3] Q. Zhong et al., "A 210 GHz to 305 GHz Wide Band Receiver Front End with 13.9 to 19 dB Noise Figure for Spectroscopy," 2016 IEEE International Solid State Circuits Conference, pp. 426-427, Feb. 2016, San Francisco, CA.

TASK 1836.155, DEVELOPMENT OF WIDE-BAND VIBRATION SENSORS BASED ON EXISTING PROCESS PLATFORMS

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SIGNIFICANCE AND OBJECTIVES

The objective of this research is to design, implement, and characterize a chip-scale vibration sensor that can operate over a wide range of frequency (DC to 10kHz) with a resolution of 1mg or better.

TECHNICAL APPROACH

The approach is to have an array of cantilevers with different resonance frequencies so as to cover the entire vibration spectrum. These cantilevers would respond to vibrations in the form of bending that would influence the tensile and compressive stresses on the piezoresistor located at the maximum stress locations.

SUMMARY OF RESULTS

The CMOS chips (240µm thick) comprises of five cantilevers of different lengths surrounded by large vias. These vias were strategically placed around the cantilever structures and successively wet etched to reach the silicon substrate. Anisotropic plasma etching of silicon was then carried out to etch out the entire silicon layer surrounding the cantilevers. The CMOS chip was finally thinned down to ~50µm using a maskless Deep Reactive Ion Etch (DRIE) to enhance the effect of the stress on the piezoresistors. Figure 1 shows the SEM view of the post-processed CMOS chip.

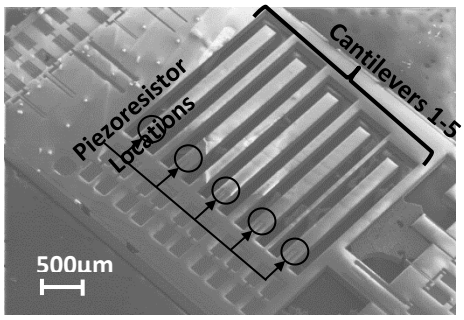

Figure 1. SEM view of the released vibration spectrometer.

The different length of the cantilevers allows each of the cantilevers to have their own resonance frequency. To measure the DC sensitivity, a point load was swept along the length of the cantilever while measuring the changes in the output voltage across the piezoresistor, incorporated as a Wheatstone bridge. Figure 2 shows the changes in output voltage for different forces applied to the cantilever. The DC sensitivity for the longest cantilever (~2000µm) is measured to be ~0.07mV/g for a 20V input.

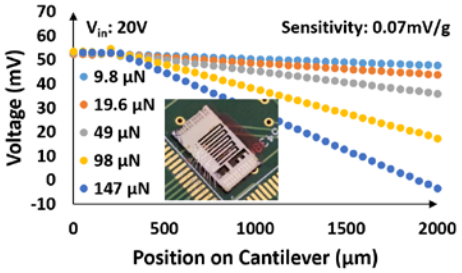

Figure 2. Changes in output voltage for the longest cantilever for different forces.

To measure the effect of vibrations on the CMOS chip, a speaker/sub-woofer was used to create sinusoidal vibrations at different frequencies using a network analyzer. The frequency spectrum for the vibration spectrometer was swept and the vibration response for two of the cantilevers (No. 2 and 4) is shown in Figure 3.

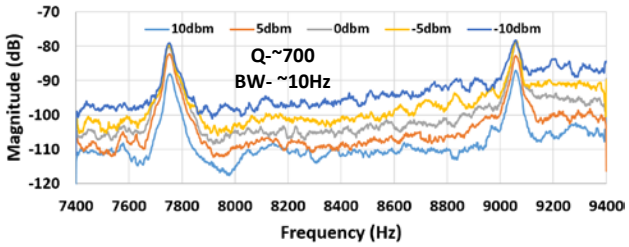

Figure 3. Resonance response obtained from cantilevers 2 and 4 for vibrations in the 7.4kHz-9.4kHz range.

The Quality factor for such cantilevers was measured to be higher than expected (~700) due to a very low 3dB bandwidth (~10Hz) of the sensor. By taking appropriate steps to reduce the quality factor (by spin-coating a layer of Photoresist for example) the total numbers of cantilevers required for operation in the DC-10kHz range can be minimized.

Keywords: vibration spectrum, CMOS- MEMS.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1]. V. Qaradaghi, M. Mahdavi, V. Kumar, S. Pourkamali, “Frequency output mems resonator on membrane pressure sensors”, IEEE Sensors 2016.

[2]. A. Abbasalipour, V. Kumar, M. Mahdavi, S. Pourkamali, "Thermal Piezoresistive Resonant Mass Balances Implemented in a Standard CMOS Process", Napa Microsystems Workshop 2017.

TASK 1836.156, TRANSITION DESIGN FOR HIGH DATA RATE LINKS AT SUBMILLIMETER WAVE FREQUENCIES

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SIGNIFICANCE AND OBJECTIVES

This project focuses on the design of interface components and multiplexers for 500 Gbps communication links using a 1m dielectric waveguide. This effort is in collaboration with the IC transceiver design (O) and polymer-based waveguide development (MacFarlane).

TECHNICAL APPROACH

The approach focuses on implementing a diplexer circuit centered at 270 and 315 GHz designed with a directional filter and one centered at 180 and 315 GHz with a manifold coupled line filter. A broadband output signal will excite a substrate-based waveguide and transfer the signal through the waveguide for transmit and receive.

SUMMARY OF RESULTS

Results include the design, simulation, and layout of a planar directional filter that is centered at 270 and 315 GHz. The 2nd order directional filter has a 20-GHz bandwidth and utilizes two one-wavelength loops and quarter-wave coupled line sections with a size of 0.78 mm x 0.66 mm area (with probe pads included). The center frequency of the directional filters can be designed individually and cascaded together to form a multiplexer. This design provides less interaction between channel filters.

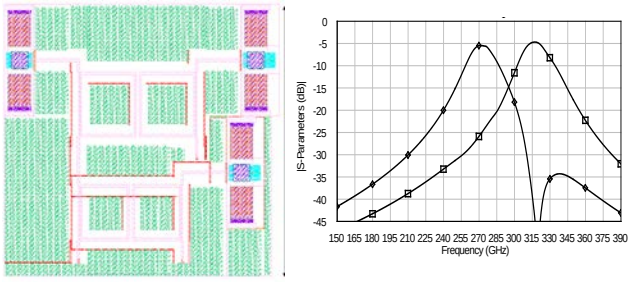

Figure 1. Layout of directional filter diplexer (0.78 mm x 0.66 mm) and simulated insertion loss at 270 and 315 GHz.

These designs are limited to narrow bandwidths (< 10%). Fig. 1 shows the two cascaded filters where the extra ports are terminated in 50 ohm resistors realized in a 16 ohm/sq. polysilicon layer in a 65-nm process. This diplexer will be measured using WR-3 waveguide modules that operate from 220 to 325 GHz.

The manifold filter implementation for 180 and 315 GHz channels is realized using straightforward coupled line bandpass filters. The input signal is split and sections of line are included to make the unwanted output signal look like an open circuit when the desired signal should be passing, and vice-versa. The design complexity increases with the additional channels due to the interaction between channel filters. Two 3rd order coupled line filters have been designed with 40 GHz bandwidth using half-wavelength sections with an area of 0.6mm x 1.4 mm (including probe pads). Fig. 2 shows the simulated insertion loss for this design.

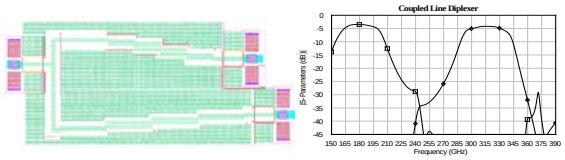

Figure 2. Layout of directional filter diplexer (0.6mm x 1.4 mm) and simulated insertion loss at 180 and 315 GHz.

This circuit will be measured using the WR-3 and WR-5 (140 – 220 GHz) RF modules. To handle this complexity we have included 50 ohm terminations at each output port to allow for two port measurements. Fig. 3 shows the simulated response of the two 315-GHz filters. One can observe the difference in bandwidth.

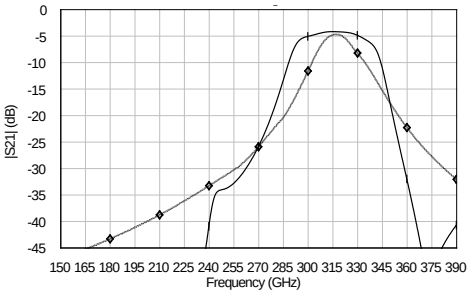

Figure 3. Simulated comparison of directional and coupled line filter responses at 315 GHz.

Keywords: multiplexer, directional filter, coupled line bandpass filter

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] N. Mahendarkar Vijayakumar, M. Gomez, R. Henderson, “Sub-Millimeter Wave Diplexer Design in 65nm Technology,” accepted for TECHCON 2017.

TASK 1836.158, DEVELOPMENT OF DIELECTRIC WAVEGUIDES FOR THZ RADIATION APPLICATIONS

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SIGNIFICANCE AND OBJECTIVES

The task comprises the design, fabrication, characterization and application of square dielectric waveguides for the propagation of THz and near-THz radiation using a "holey" fiber structure to engineer the refractive index profile and thereby supporting high-speed data transmission between integrated circuits and between boards.

TECHNICAL APPROACH

The waveguide was designed using FDTD simulation and fabricated using a custom built oven to preserve the square geometry. The waveguide was made of TOPAS (0.2 dB/cm material loss at 250 GHz). Fabricated waveguides were simulated considering fabrication defects. The simulations show a confined mode across 180 GHz to 360 GHz despite manufacturing defects (Fig. 1). Mode profile of the waveguide was mapped using a vector network analyzer (VNA) working at 220 GHz to 325 GHz and is in agreement with the simulation. The fiber loss was measured using the same VNA and added coupling components.

SUMMARY OF RESULTS

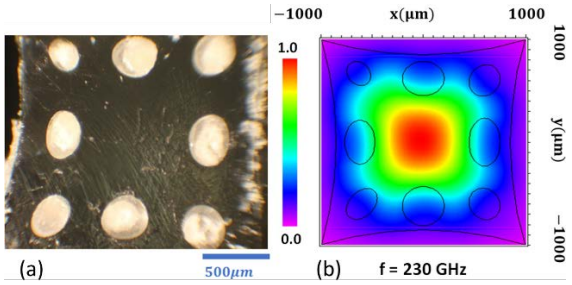

Figure 1. (a) Cross section micrograph of a fabricated waveguide. (b) Mode propagation simulation of the as-fabricated waveguide, at 230 GHz.

Loss measurement

The characterization setup consists of a VNA along with two frequency extenders which provide a source and a receiver for radiation from 220 GHz to 325 GHz as shown in Figure 2. To ensure efficient coupling, a custom built taper with a 1.3 mm × 1.3 mm aperture (comparable to the waveguide core size) was used to couple THz wave into the fiber core. A 7.00 mm × 5.84 mm aperture horn couples the THz wave out of the fiber efficiently. A 30 cm fabricated fiber mounted on X-Y-Z stages at both ends was aligned for maximum transmission.

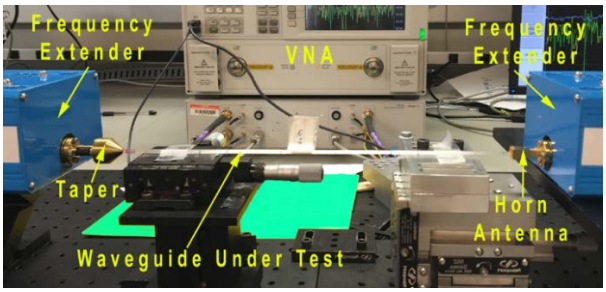

Figure 2. A VNA with frequency extenders and custom-built taper and horn antenna is used for fiber loss measurements.

The fiber was tested 5 times with fiber loss consistent across all measurements. Figure 3 shows the calculated fiber loss across the frequency range of 220 GHz to 320 GHz. Measurement shows an average fiber loss of 0.25 dB/cm across the frequency range. The fabricated waveguide has relatively low loss considering the material loss of TOPAS (0.2 dB/cm).

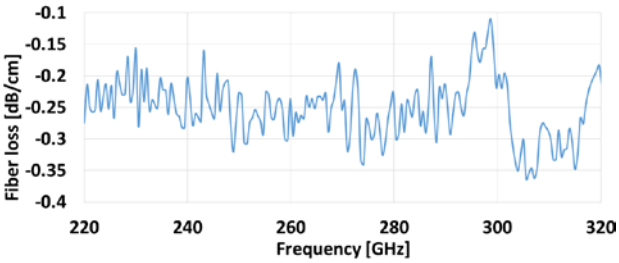

Figure 3. Measured fiber loss at 220 GHz to 320 GHz.

Keywords: dielectric losses, submillimeter waveguides, submillimeter wave propagation, transmission lines, and transmission line measurements.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] N. Aflakian, et al.," Square dielectric THz waveguides" Opt. Express 24(13) 14951-14959 (2016).
[2] N. Aflakian et al., "Square holey cladding dielectric THz waveguides for chip-to-chip communication" FiO/LS Conference, Rochester, NY (2016).
[3] N. Aflakian et al., "Square dielectric interconnect for chip-to-chip THz communication" IEEE Texas Symp. Wireless & MW. Circ. & Sys. (2017).

TASK 1836.159, PERFORMANCE OF CARBON DIOXIDE (CO_2) GAS SENSORS

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SIGNIFICANCE AND OBJECTIVES

Through the use of a semiautomatted gas mixing system and test environment, selected room temperature ionic liquids (RTIL's) were exposed to different sets of temperature and humidity and their response to these exposures was analyzed for further fluoride/non-fluoride interactions as well as possible down selection of material for the next aims.

TECHNICAL APPROACH

Through the application of a closed system that utilizes a gas mixer, the RTILs were exposed to different CO_2, humidity, and temperature variations. Exploring the response of the electrochemical double layer (EDL) capacitance generated by the different RTILs under test offers an amplifying effect. Through the use of electrochemical impedance spectroscopy, the impedance is measured utilizing a 100m-V AC signal applied to a DC offset. This AC signal swept 1 to 5 kHz to probe from the bulk effects down to the EDL interface at the electrode.

SUMMARY OF RESULTS

Understanding the effects of humidity and temperature changes on the behavior of the RTILs is necessary for exploring the effects of fluorinated and unfluorinated anions have on consistently detecting CO_2 concentration changes.

Table 1. EMIM[FAP] capacitance change between N_2 and CO_2 at selected humidity and temperature conditions.

EMIM[FAP]	(nF)	(nF)	(nF)
At 65% Humidity	400ppm	750ppm	1000ppm
65 C	3.9	3	1.4
45 C	17	27	29
At 45% Humidity	400ppm	750ppm	1000ppm
65 C	14.1	16	17.6
45 C	1.8	4.3	8.1
At 25% Humidity	400ppm	750ppm	1000ppm
65 C	0.26	0.4	0.5
45 C	0.1	0.2	0.7
25 C	5.9	8.8	11.5

EMIM[FAP] is a fluorinated RTIL that has shown consistent behavior across the different temperature regimes previously. Through the addition of different humidity exposures, general response trends were extracted through the use of a standard Randle's circuit fit. It can be seen that at high humidity, EMIM[FAP] shows an upward capacitance change versus the downward trends shown at 45% and 25% relative humidity. respecively. This points toward a change of the interaction mechanism occuring at these conditions from chemisorption dominated to physisorption dominated.

Table 2. EMIM[TF2N] capacitance change between N_2 and CO_2 at selected humidity and temperature conditions.

EMIM[TF2N]	(nF)	(nF)	(nF)
At 65% Humidity	400ppm	750ppm	1000ppm
65 C	22	1.2	0.9
45 C	67	40.1	29
At 45% Humidity	400ppm	750ppm	1000ppm
65 C	0.6	1.3	1.8
45 C	1.8	4.3	8.1
At 25% Humidity	400ppm	750ppm	1000ppm
65 C	1.5	1.8	3
45 C	0.2	0.39	1.3
25 C	2.3	4.8	19.6

EMIM[TF2N], the other fluorinated RTIL also showed a change at higher humidity. This suggests that another interation mechanism is turning on at this humidity due to changes of the chemi- and physisorption processes.

Table 3. MMIM[MeSO4] capacitance change between N_2 and CO_2 at selected humidity and temperature conditions.

MMIM[MeSO4]	(nF)	(nF)	(nF)
At 65% Humidity	400ppm	750ppm	1000ppm
65 C	5.5	12.6	15.5
45 C	390	276	201
At 45% Humidity	400ppm	750ppm	1000ppm
65 C	14.1	16	17.6
45 C	5	51	192
At 25% Humidity	400ppm	750ppm	1000ppm
65 C	69	76.3	80
45 C	74	82.4	89
25 C	88	94	99

MMIM[MeSO4], the sole non-fluorinated RTIL, shows an interesting behavior across the temperature and humdity ranges. It is only at 65°C and 65%RH that we see a return to the lower humidity behavior of an upward trend of the capacitance. Due to the physisorption proccess of this RTIL there may be physical thresholds that CO_2 has to overcome to interact with the EDL given the different RH/Temp combinations.

Keywords: CO_2, humidity, temperature, RTIL, EIS

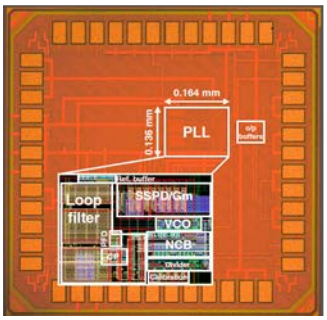
INDUSTRY INTERACTIONS

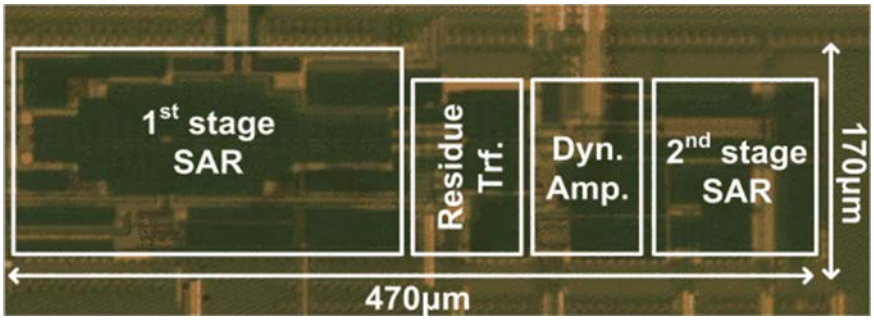
Texas Instruments

MAJOR PAPERS/PATENTS

[1] Edward Graef Jr. et al., "A Robust Electrochemical CO2 Sensor Utilizing Room Temperature Ionic Liquids," IEEE Trans. in Nanotechnology, 10.1109/TNANO.2017.2672599 (2017).

Fundamental Analog Thrust





Category	Accomplishment
Fundamental Analog (Circuits)	A RISC-V system-on-chip with integrated voltage regulation and power management is implemented in 28-nm FD-SOI. A fully integrated switched-capacitor DC-DC converter, coupled with an adaptive clocking system, achieves 82-89% system conversion efficiency across a wide operating range, yielding a total system efficiency of 41.8 double-precision GFLOPS/W. (1836.136, PI: B. Nikolic, UC-Berkeley)
Fundamental Analog (Circuits)	A 12-b 330MS/s single-channel pipelined-SAR ADC employs a PVT-stabilized dynamic amplifier as the residue amplifier instead of opamp-based residue amplifiers that consume significant amounts of power due to stringent settling speed and accuracy requirements. The ADC fabricated in 65-nm CMOS with a core area of 0.08mm^2 achieves an FoM of 9.5fJ per conversion. The measured DNL and INL are +0.67/-0.56LSB and +0.7/-0.8LSB, respectively. The measured SNDR remains above 60dB even with a 500MHz input. (1836.157, PI: Y. Chiu, UT-Dallas)
Fundamental Analog (Circuits)	A 2-2.8GHz 65-nm CMOS ring oscillator PLL occupies an active area of 0.022 mm^2, consumes 5.86mW, and achieves a 633fs RMS jitter at 2.36 GHz and an FOM$_{jitter}$ of -236 dB. It implements a low-overhead feed-forward phase and supply-noise cancellation scheme by leveraging the noise extraction inherently done by the sub-sampling phase detector. Cancellation reduces the jitter by 1.4X, the phase noise by 10.2dB to -123.5dBc/Hz at a 300KHz offset, and the ring oscillator supply sensitivity by 19.5dB for a 1-mV$_{p-p}$ 100KHz supply noise tone. (1836.134, PI: P. Kinget, Columbia University)

TASK 1836.096, MIXED-SIGNAL DESIGN CENTERING IN DEEPLY SCALED TECHNOLOGIES

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SIGNIFICANCE AND OBJECTIVES

A methodology for robust design of high-performance analog circuit blocks in highly-scaled technologies has been investigated, to enable rapid yield ramp-up in scaled technologies.

TECHNICAL APPROACH

We have developed a methodology that enables centering with respect to technology variability of high-performance mixed-signal designs in as few as one design iteration. It is based on the components, which are developed simultaneously:

- Instrumenting critical design components to accurately monitor impact of process variability on their performance.
- Creating a dedicated set of representative circuit primitives for their full variability characterization.
- Extracting a variability model from the test structures; building simplified Spice models to predict the distribution spread of critical components.

These components enable centering of critical analog blocks, such as clock and data recovery loops, high-performance data converters and sense-amplifiers.

SUMMARY OF RESULTS

We have developed an algorithm based on backward propagation of variability to improve yield prediction capability of existing models.

We have applied this methodology on a design of high-performance comparators for use in analog-to-digital converters, focal plane arrays, high-speed serial links and memory. A testchip, shown in Fig. 1, designed in a 28-nm FDSOI process contains large comparator arrays for measuring distributions of offsets, impulse sensitivity functions and transistor I-V characteristics [1]. Two new comparator designs [2], shown in Fig. 2, are tested with traditional ones, and the sample measured offset results are shown in Fig. 3.

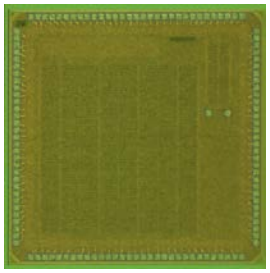

Figure 1. Die photo.

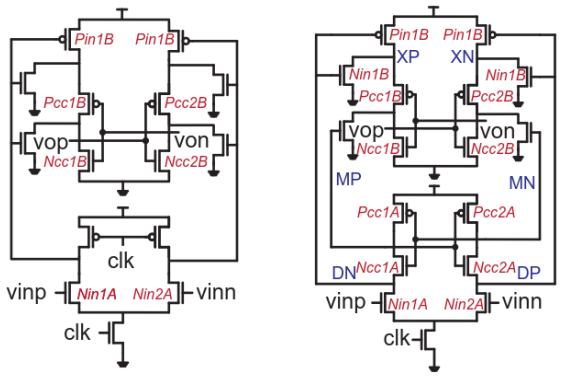

Figure 2. Double-tail sense amp (DTSA) and dual strong arm (DSA).

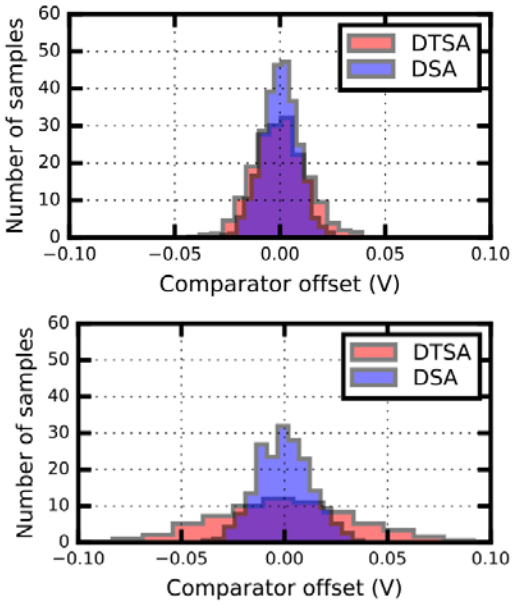

Figure 3. Measured comparator offset for DTSA and DSA at 1V and 0.7V supplies.

Keywords: CMOS, variability, yield, design optimization, comparators.

INDUSTRY INTERACTIONS

Intel

MAJOR PAPERS/PATENTS

[1] A. Papadopoulou, B. Nikolic, "A yield optimization methodology for mixed-signal circuits," *IEEE CICC*, Austin, TX, April 30-May 3, 2017.

[2] A. Papadopoulou, V. Milovanovic, B. Nikolic, "A low-voltage low-offset dual strong-arm latch comparator," *IEEE A-SSCC'17*, Seoul, Korea, November 6-8, 2017.

TASK 1836.111, ADVANCED ADC-BASED SERIAL LINK RECEIVER ARCHITECTURES

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SEBASTIAN HOYOS, TEXAS A&M UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

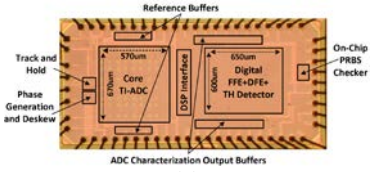
While CMOS technology scaling allows for the efficient implementation of powerful on-chip DSP algorithms for equalization and symbol detection, ADC-based receivers are generally more complex and consume higher power. The proposed ADC-based serial link techniques aim to significantly improve interconnect bandwidth density in an energy-efficient manner.

TECHNICAL APPROACH

In order to investigate design trade-offs, a novel statistical-modeling framework for advanced ADC-based serial links was developed. This tool was used to guide the design of a new hybrid ADC-based receiver architecture which combines in a power optimum manner equalization embedded in the ADC and dynamically power-gated digital equalization based on threshold detection.

SUMMARY OF RESULTS

To relax ADC-based RX power and complexity, partial equalization can be embedded inside the ADC and not be limited by the ADC resolution. While this provides improved BER, additional equalization is generally required to support channels with loss >30dB. This is addressed in an energy-efficient manner with a new hybrid ADC-based RX architecture which combines embedded ADC equalization and dynamically-enabled digital eq. based on threshold detection [1]. A 10Gb/s RX prototype with a 3-tap analog FFE embedded inside a 6-bit asynchronous SAR ADC and a dynamically-enabled digital 4-tap FFE and 3-tap DFE was fabricated in GP 65nm CMOS (Figure 1). The RX compensates for up to 36.4dB loss with 30mW savings in the digital eq. power and an overall power <90mW.



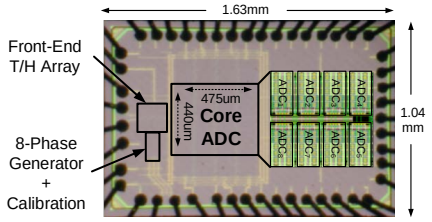
(a)

Specification	[1]	[2]	[3]	This Work	
Technology	65nm	65nm	40nm	65nm	
Power Supply (V)	N/A	1.1	N/A	1	
ADC Structure	Flash	Variable V_{REF} Flash	Rectifier Flash	TI-SAR	
Pre-Equalization	4 taps FIR (@ TX)	IIPF + 2 taps FFE	N/A	Embedded 3-tap FFE	
Post-Equalization	2-tap FFE + 5-tap DFE	5-tap DFE	Adaptive FFE+DFE	4-taps FFE + 3 taps DFE	
Sampling Rate (GS/s)	12.5	10	8.5-11.5	10	
Resolution (bit)	4.5	4	6	6	
ENOB (bit)	N/A	N/A	4.86	4.74	
Input Range (V_{pp})	N/A	0.6	N/A	1	
Area (mm^2)	0.45	0.29	0.82	0.81	
Compensated Channel Loss	-24dB @ 12.5GS/s	-29dB @ 10GS/s	-34dB @ 10.3GS/s	-25.3dB @ 10GS/s	-36.4dB @ 10GS/s
ADC Power (mW)	150	93	195	79	
DSP Power (mW)	85	37	N/A	8	10
Power Efficiency (pJ/bit)	30.7*	13	19	8.7	8.9

* Includes both the TX+RX

(b)

Figure 1. 10Gb/s hybrid ADC-based receiver, (a) GP 65nm CMOS prototype, (b) performance summary.



(a)

TABLE I: PERFORMANCE SUMMARY

Specification	[5]	[4]	This Work
Technology	65nm	32nm SOI	65nm
Power Supply	1.5V	0.9V	1V
ADC Structure	TI-Flash	TI-Flash	TI-BS
Sampling Rate	16 GS/s	20 GS/s	25 GS/s
Resolution	6 bits	6 bits	6 bits
ENOB @ Nyquist	4.36 bits	4.84 bits	4.62 bits
Area	1.47 mm^2	0.25 mm^2	0.24 mm^2
Power	435 mW	69.5 mW	88 mW
FOM ($P/2^{ENOB} \cdot f_s$)	1325 fJ/c.-s.	124 fJ/c.-s.	143 fJ/c.-s.

(b)

Figure 2. 25GS/s 6b TI binary search ADC, (a) GP 65nm CMOS prototype, (b) performance summary.

To support data rates at or above 50Gb/s, energy-efficient ADC designs with moderate resolution and very high sampling rates are required. This is addressed in a 25GS/s 6b 8-way time-interleaved binary search ADC that employs a novel soft-decision selection algorithm to relax track-and-hold (T/H) settling requirements and improve ADC meta-stability tolerance (Figure 2) [2, 3]. Fabricated in GP 65nm CMOS, the ADC occupies 0.24mm^2 total area, achieves 29.6dB SNDR at Nyquist while consuming 88mW from a 1-V supply, translating into a figure-of-merit (FoM) of 143 fJ/conv.

Keywords: analog-to-digital converter, ADC-based receiver, embedded equalization, energy efficient

INDUSTRY INTERACTIONS

NXP, Intel, Texas Instruments

MAJOR PAPERS/PATENTS

[1] A. Shafik et al., IEEE JSSC, Mar. 2016.
[2] S. Cai et al., IEEE VLSI Symp., June 2015.
[3] S. Cai et al., IEEE JSSC, Aug. 2017.

TASK 1836.117, PERFORMANCE AND RELIABILITY ENHANCEMENT OF EMBEDDED ADCS WITH VALUE-ADDED BIST

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DEGANG CHEN, IOWA STATE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

The objectives are to develop procedures for implementing parametric BIST of ADCs with minimal area overhead, to use on-chip test results to enhance performance by digitally calibrating the ADC, and to experimentally demonstrate the BIST and BIST-based calibration on the ADC12 internal to the TI MSP 430 microcontroller.

TECHNICAL APPROACH

Working with engineers at TI, the Functionally Related Excitation (FRE) approach to testing using a Stimulus Error Identification and Removal (SEIR) algorithm will be adapted to a BIST solution. The FRE/SEIR approach was developed in conjunction with TI on a previous SRC project. On-chip FRE signal generators using the shift operator will be developed for test signal generation and existing on-chip computation resources will be utilized to minimize the area overhead required to implement the SEIR algorithm. Target area overhead is at most 10% of the area of the existing uncalibrated ADC that is currently in high-volume production.

SUMMARY OF RESULTS

A block diagram showing the BIST capability and the BIST-based calibration is shown in Fig. 1 with a target 12-bit ADC. Two additional bits of resolution have been added to the SAR ADC to allow for a 2-bit improvement in linearity with the BIST-based calibration. The final output is then decimated back to 12 bits after calibration.

The signal generator will be a current ramp based integrator comprised of the output from a simple regulated cascode current source charging a nonlinear capacitor. With the FRE/SEIR approach, linearity of the ramp is of little concern. To manage the size of the integration capacitor, a series of faster-rising ramps will be used instead of a single ramp. A second-generation level-spreading ramp generator using a dithered integration starting voltage was developed to maintain approximately uniform density of the input signal throughout the input range of the ADC. A critical component is the shift generator which must have a constant shift. The second-generation shift generator of Fig. 2 that provides rail-to-rail output using correlated level shifting (CLS) and that provides the constancy needed for testing 14-bit ADCs has been designed.

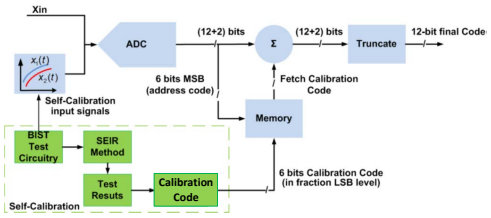

Figure 1. Block Diagram of ADC with BIST-Based Calibration and Value-Added BIST.

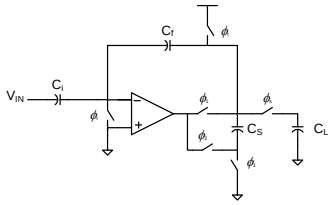

Figure 2. FRE shift generator using correlated level shifting.

For the past year, emphasis was entirely on completing design details. The circuit came back from fabrication on approximately Aug 20. Testing will start on approximately September 20 when packaging is complete.

Keywords: ADC BIST, self-calibration, analog testing, FRE signal generators, SEIR testing

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

In this custom-funding project, details about the ADC used for experimental verification are proprietary property of TI thus precluding publication of key technical details of the project. Two publications that discuss principles used in this research follow.

[1] X. Zhang et. al., "A Calibration Technique for SAR Analog-to-Digital Converter Based on INL Testing with Quantization Bits and Redundant Bit," 2015 IEEE Int. Symp.on Circuits and Systems (ISCAS), pp. 3024-3027, May, 2015.

[2] H. Meng et al., "A Simple Ramp Generator with Level Spreading for SEIR based ADC BIST Circuit," IEEE Midwest Symp. On Circuits and Systems (MWSCAS), pp. 53-56, Aug., 2015.

TASK 1836.125, 10GS/S+ RESOLUTION-SCALABLE (4-7BITS) ADCS

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SIGNIFICANCE AND OBJECTIVES

This research is developing and demonstrating new approaches to high speed ADC design. The new techniques enable energy efficient, high-speed (>10GS/s) moderate resolution analog to digital conversions (4-7b) in 28-nm or 32-nm CMOS.

TECHNICAL APPROACH

High-speed moderate resolution ADC's are vital for high-speed data links. Interleaved SAR ADC's achieve high sampling speeds and good energy efficiency. However, these ADC's are large and therefore suffer from interleaving artifacts related to size. Compact, efficient SAR ADC's are needed to address this problem. Multiple-bit-per-cycle SAR ADC's deliver high speed from a single SAR ADC, but add significant added complexity (i.e. extra quantizers and capacitor DACs) and die area. This work addresses the need for a fast, compact SAR ADC, with a 1GS/s SAR ADC that has the best Walden FoM and the smallest area among 5~6.3bit ADCs.

SUMMARY OF RESULTS

The *charge injection SAR* (or ciSAR), which is based on a charge injection DAC structure has been proposed. ciSAR achieves GHz sampling speed from a single SAR ADC and reduces area by more than half. This ADC achieves the best Walden FoM and the smallest area by leveraging two unique features of ciSAR: (i) interrupted settling and (ii) reusability of charge injection cells.

ciSAR, due to interrupted settling, is faster, simpler and more linear for high-speed applications. This is because ciSAR avoids the significant distortion suffered by conventional fast SAR ADC's due to insufficient DAC settling time. This distortion is caused by residual settling from earlier SAR conversion steps while the present DAC settling step is taking place.

Another important advantage of ciSAR is that CIC cells can be reused multiple times in a SAR conversion. Since CIC's are only active during a short time, they can utilize the rest of the time (i.e. waiting for a comparator decision) to get ready for another transfer. By reusing the CIC's for the subsequent transfer cycles, the DAC area of ciSAR can be reduced at least by half or even more, since the charge transfer process can be spread out over multiple transfer cycles to reach the desired level of transfers.

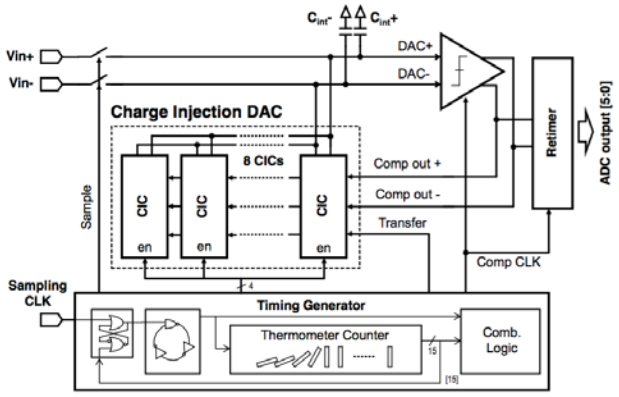

Figure 1. Block diagram of CIC-SAR 6-bit ADC.

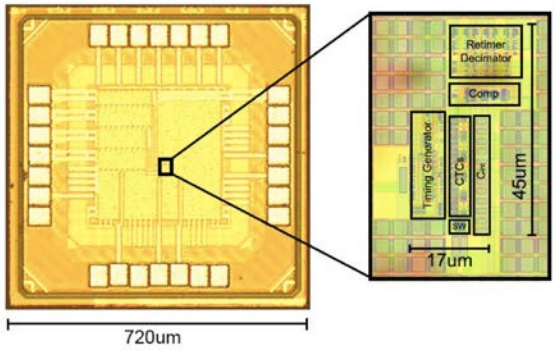

Figure 2. Die photo of 40nm CMOS 6-bit ADC.

The ADC input range is 300mVpk-pk (600mVdiffpk-pk). The integration caps are each 200fF. The integration capacitors are implemented as M1-M7 MOM capacitors and occupy only 66μm^2. This compact layout scheme is possible since mismatch between the two caps only introduces a small offset.

The prototype, fabricated in 40-nm CMOS, occupies 0.00058mm^2 and consumes 1.26mW from a 1-V supply. The measured ENOB is above 5.46b across input frequencies spanning from 30MHz to 500MHz, sampled at 1GS/s. The area is 52% of the closest competitor and the Walden FoM is measured at 28.6fJ/conv-step.

Keywords: ADC, flash, two-step, CMOS

INDUSTRY INTERACTIONS

Texas Instruments, IBM

MAJOR PAPERS/PATENTS

[1] K. Choo, J. Bell and M.P. Flynn, "Area-efficient 1GSps 6b SAR ADC with Charge-Injection Cell Based DAC," ISSCC 2016.

TASK 1836.127, PRECISION TEST WITHOUT PRECISION INSTRUMENTS – A NECESSITY FOR FUTURE ON-CHIP SELF-TEST AND SELF HEALING

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RANDY GEIGER, IOWA STATE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

Accurate spectral analysis is widely needed in IC characterization and final test. IEEE standard tests require accurate instruments and accurate test control, resulting in expensive equipment, complex test setup, demanding maintenance, TTM delays, and high test cost. The objective of this research is to develop new spectral test algorithms to remove the IEEE standard requirements, deliver accurate full spectrum test results, and greatly reduce test equipment cost, TTM delays, and test time.

TECHNICAL APPROACH

Mixed-signal spectral testing is re-casted as an identification problem of weakly nonlinear signal & systems. Statistical signal processing techniques are incorporated to develop algorithms for accurately separating and extracting all distortion, jitter and noise information with accuracy near theoretical limits out of a relatively small data set. An innovative iterative time-frequency domain processing technique is utilized to achieve the best accuracy and time efficiency trade-off, in which all spectral spurs (input, distortions, periodic jitter, etc.) are identified in frequency domain while residue error construction and noise/jitter characterization ("flat" in spectrum) are done in time domain. This dual domain approach enables high time efficiency and high dynamic range detection, allowing accurate estimation of the target components in the simultaneous presence of various error sources.

SUMMARY OF RESULTS

The final goal of the project is the elimination of all the stringent requirements in the ideal IEEE standard spectral testing. These requirements include: coherent sampling, accurate amplitude control, high purity sinusoidal signal sources, and jitter-free sampling clock signal. During the first three years, we published 3 journal papers and 13 conference papers. These papers introduced: 1) the FIRE method for removing non-coherency, 2) the FERARI method for both non-coherency and amplitude clipping, 3) a jitter and noise separation method for accurate SNR testing, 4) a comparative study of state of the art methods for dealing with non-coherent sampling, 5) an algorithm for both nonlinear signal source and non-coherent sampling, 6) an algorithms for simultaneous AC and DC test with dramatic test time reduction, 7) an algorithm for accurate SNR test in the presence of clock jitter, 8) a method for clock jitter separation and characterization, and 9) a method for generating ultra-pure sine wave signals for high resolution ADC testing. During the year May 2016 – April 2017, we published five journal papers and ten conference papers. We introduced a test method for accurate linearity testing with impure sinusoidal stimulus robust against flicker noise. We also developed an algorithm for accurate spectral testing with non-coherent sampling and large distortion to noise ratios. Furthermore, we presented a new test solution for accurate spectral testing of ADCs despite both amplitude and frequency drifts using proper segmentation and and averaging techniques. With a simple ISI model, we developed a method for accurate RJ and DJ decomposition and estimation for high-speed data links. Building upon this, we presented a low-cost method for multi-site ADC testing with clock jitter, aperture jitter and noise separation. Many of the proposed test algorithms have been validated at SRC member companies.

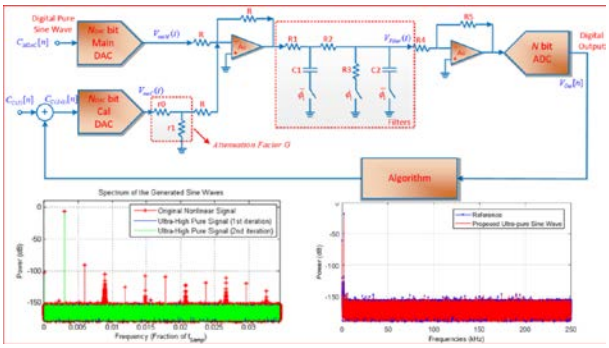

Figure 1. Low cost ultra-pure sine wave generation with self-calibration. Upper: schematic of sine wave generator with low-cost main DAC, Cal DAC with attenuator, buffer and filters, low-cost ADC, and algorithm for calibration and adaptation. Lower left: sine wave purity improvement. Lower right: accurate test of high resolution ADC.

Keywords: AC test, spectral test, nonlinear source, non-coherent sampling, amplitude clipping, jitter, noise

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

[1] Zhuang, ISCAS'16. [2] Magstadt, TIM'16. [3] Zhuang, ITC'16. [4] Zhuang, JETTA'17. [5] Zhuang, TIM'17. [6] Zhuang, TCAS-II'16. [7, 8] Zhuang, ISCAS'17. [9] Zhuang, TIM'17. [10] Xu, ITC'17. [11] Duan, ISCAS'16. [12] Duan, VTS'17. [13] Jin, ITC'17. [14] Liu, ISCAS'16. [15] Chaganti, VTS'17.

TASK 1836.128, STATISTICAL ANALOG DESIGN PROPERTY CHECKING

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SIGNIFICANCE AND OBJECTIVES

Aiding design verification, failure diagnosis, and test optimization of analog and mixed-signal circuits can be significantly benefited from advanced data analytics. Towards this end, we develop both rule based and Bayesian learning based approaches.

TECHNICAL APPROACH

We are developing a simulation-based methodology for diagnosing out-of-specification failures of analog & mixed-signal circuits. Our goal is to extract a compact set of rules that corresponding to failure conditions from simulation data in the pre-silicon phase. We are developing several techniques towards producing compact and interpretable failure rules [1].

We have continued to work on the relevance vector and feature machine (RVFM) Bayesian learning algorithm for characterizing analog circuits [2]. RVFM not only produces accurate models learned from a moderate amount of simulation or measurement data, but also computes a probabilistically inferred weighting factor quantifying the criticality of each parameter.

SUMMARY OF RESULTS

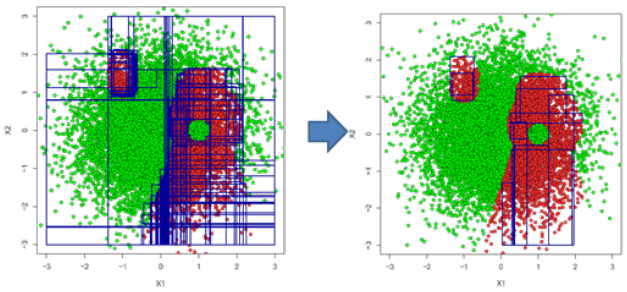

Figure 1. Extract failure rules from sum-of-tree models and merge them using post-processing.

Diagnosing out-of-specification failures in mixed-signal circuits has become increasingly challenging due to: (1) failures caused by interactions between input-signal conditions and design uncertainties, and (2) the need to identify critical input and uncertainty conditions that result operation in these regions. We propose a simulation-driven approach that first uses ensemble learning to extract if-then rules that naturally solve both problems. By ranking, pruning and clustering these rules, we then construct non-linear failure regions which can be directly employed for pre-silicon debug, as demonstrated on a phase-locked loop circuit (Fig. 1). Furthermore, these regions can be used to guide test pattern generation and/or assist with post-silicon debug.

We continued our work on relevance vector and feature machine (RVFM) based characterization of analog circuits. Compared to other popular learning-based techniques, the RVFM produces more accurate models, requires less amount of training data, and extracts more reliable parametric ranking. The effectiveness of RVFM has been demonstrated in terms of the statistical variability modeling of a low-dropout regulator (LDO) and the built-in self-test (BIST) of a charge-pump phase-locked loop (PLL).

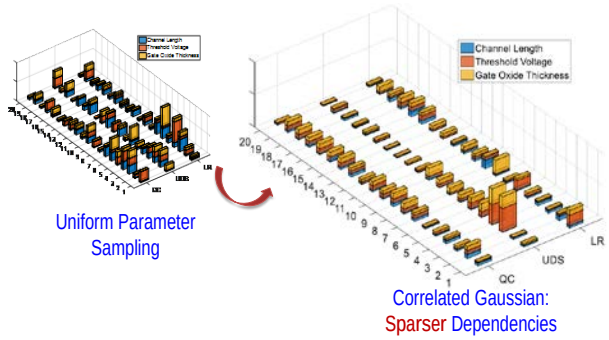

Figure 2. Extracted parameter (L_{eff}) weighting under 60 correlated Le_{ff}, T_{ox}, and V_{TH} variations.

This approach can be readily extended to consider correlated process variations and mismatch. An analysis of the LDO is shown in Fig. 2, where 60 correlated L_{eff}, T_{ox}, and V_{TH} variations are considered. Again, a weight distribution that is different from the case without correlation (independent uniform parameter sampling is used to collect the training data) has been generated.

Keywords: machine learning, rule-based learning Bayesian learning, analog verification, analog characterization, BIST.

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] Mukherjee and Li, Parijat Mukherjee, and Peng Li "Using pre-silicon knowledge to excite non-linear failure modes in large mixed-signal circuits", IEEE Design and Test, issue 5, pp. 28-34, Oct. 2016.

[2] Lin and Li, "Relevance vector and feature machine for statistical analog circuit characterization and built-in self-test optimization," IEEE/ACM DAC, Jun. 2016.

TASK 1836.129, ENERGY-EFFICIENT DIGITIALLY-ENHANCED RAPID ON/OFF LINKS IN NANO-SCALE CMOS

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SIGNIFICANCE AND OBJECTIVES

Proposed research sets out to explore energy proportion links combing rapid on/off (ROO) and dynamic voltage and frequency scaling (DVFS) to cut the power wastage so as to improve the energy efficiency at the system level. The solutions for fast response link power management and the characterization of burst-mode transceiver were proposed and evaluated.

TECHNICAL APPROACH

A source synchronous architecture shown in Fig. 1 is adopted for the link transceiver. The power management consists of a hysteretic DC-DC converter and source follower-based low dropout voltage regulator (LDO). Multiply delay locked loop (MDLL) is adopted as the fast on/off clock multiplier. A programmable divider is proposed inside MDLL to suppress the supply voltage ripple and help MDLL settle within one reference cycle.

SUMMARY OF RESULTS

This work demonstrated the first energy proportional transceiver in Fig. 2 that combines ROO and DVFS, and wake-up in less than 14ns at 6Gb/s operation. The transceiver power scales almost linearly according average data rate or utilization level (Fig. 3(a)). For 128-byte data bursts, the transceiver operating at a peak data rate of 8Gb/s in the ROO mode achieves 500X effective data rate scaling (8Gb/s–16Mb/s) while scaling the power by 84X (46.8–0.56mW) and energy efficiency by 6X (6.2–37pJ/b). With DVFS, energy efficiency varies by only 2.2X (6.2–14.1pJ/b) for 500X effective data rate scaling and 220X (46.8-0.21mW) power scaling (Fig. 3(b)). ROO by itself can provide data rate scaling of only 100X for 2X variation in efficiency. Thanks to the combination of DVFS and ROO, the proposed link extends data rate scaling beyond 100X and achieves the largest energy proportional range of 500X with only 2X energy efficiency variation.

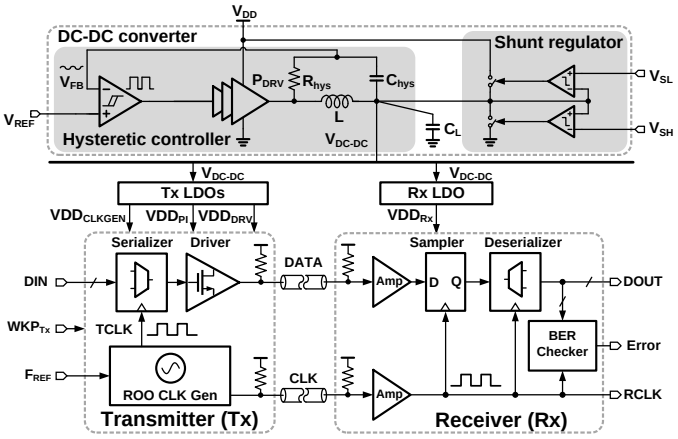

Figure 1. Block diagram of proposed link transceiver.

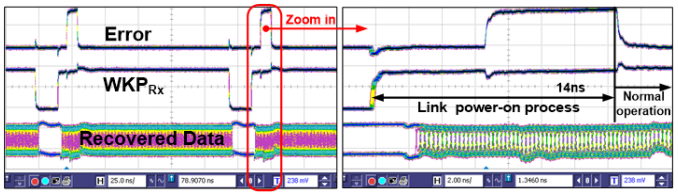

Figure 2. Measured transceiver power-on/off transient at 6Gb/s.

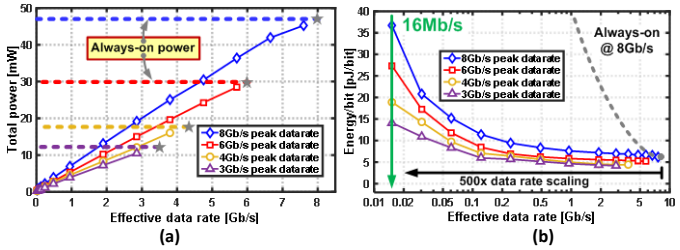

Figure 3. (a) Measured transceiver power versus effective data rate. (b) Measured transceiver energy-per-bit versus effective data rate.

Keywords: energy proportional links, dynamic power management

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] G. Shu, W. Choi, S. Saxena, S. Kim, M. Talegaonkar, R. Nandwana, A. Elkholy, D. Wei, T. Nandi, and P. Hanumolu, "A 16 Mb/s-8 Gb/s, 14.1-5.9 pJ/bit source synchronous transceiver using DVFS and rapid on/off in 65nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Jan. 2016, pp. 398-399.

TASK 1836.132, FAULT COVERAGE ANALYSIS OF ANALOG/MIXED-SIGNAL TESTS BASED ON STATISTICAL DISSIMILIARITY

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SIGNIFICANCE AND OBJECTIVES

The number of mixed-signal ICs escaping production screening is sharply rising due to the increasing use of digital circuits within analog systems. This task aims to develop a systematic way to quantitatively measure the fault coverage of a given analog/mixed-signal circuit test. This is a key pre-requisite to the automatic generation of efficient analog/mixed-signal test suites or patterns that can achieve high defect coverage and short testing time.

TECHNICAL APPROACH

This task explores ways of quantitatively measuring the fault coverage of an analog/mixed-signal test suite leveraging various statistical discrimination methods.

For instance, a test is said to cover a fault when the fault causes large enough difference in the test's response that can be distinguished from the normal statistical variations of the circuit due to global process, voltage, and temperature (PVT) variations and local transistor-to-transistor mismatches.

In addition, the correlations among the test responses can be utilized in various ways, for instance, to enhance the effective coverage of a given test suite and to estimate the statistical distributions with a small number of Monte-Carlo samples.

SUMMARY OF RESULTS

An initial study has been conducted that quantifies the test coverage of some representative analog/mixed-signal circuits over basic catastrophic stuck-short/open faults. Despite the simplistic assumptions made, the results demonstrate that the fault coverage analysis based on statistical discrimination can be an effective way to measure the fault coverage of a given test suite and guide the composition of an efficient test suite. Based on this result, an incremental, min-max search algorithm was devised to efficiently find a minimal set of tests that achieves the desired coverage, exploiting the cross-correlation among the tests.

In the last year, we have applied the fault coverage model and test generation algorithm to various analog/mixed-signal circuits, including A/D and D/A converters, phase-locked loops, and power converters. The results demonstrate that the simple stuck-short/open model is sufficient and effective in measuring the fault coverage of a given test on analog circuits.

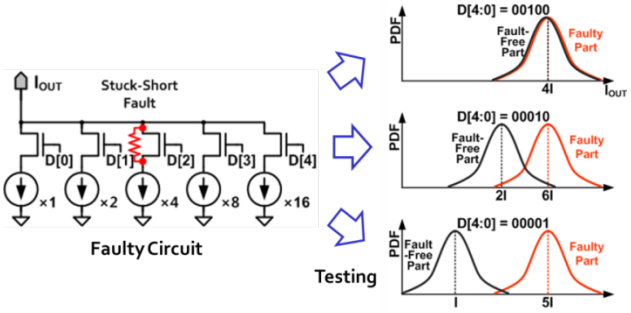

Figure 1. Determining fault coverage based on variability distribution.

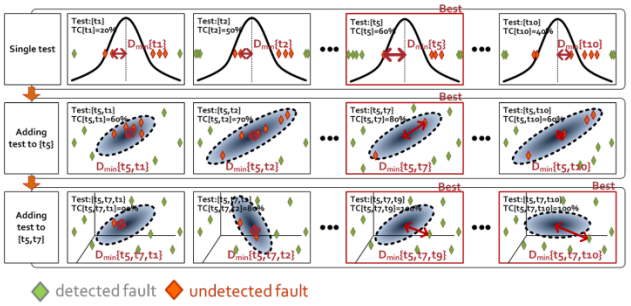

Figure 2. Efficient test compaction algorithm that finds the minimal set of tests with the desired coverage.

Keywords: analog/mixed-signal circuits, production tests, fault coverage analysis, test compaction, automatic test pattern generation.

INDUSTRY INTERACTIONS

Texas Instruments, Intel, Globalfoundries

MAJOR PAPERS/PATENTS

[1] S. Youn, C. Gu, and J. Kim, "Probabilistic Bug Localization for Analog/Mixed-Signal Circuits using Probabilistic Graphical Models," Design Automation Conf. (DAC), June 2014.

[2] S. Jung, J. Lee, and J. Kim, "Variability-Aware, Discrete Optimization for Analog Circuits," Trans. on Computer-Aided Design, 2014.

[3] S. Jung, J. Lee, and J. Kim, "Yield-Aware Pareto-Front Extraction for Discrete, Hierarchical Optimization of Analog Circuits," Trans. on Computer-Aided Design, 2014.

[4] J. Kim, et al., "Discretization and Discrimination Methods for Design, Verification, and Testing of Analog/Mixed-Signal Circuits," Custom Integrated Circuits Conf., 2013.

TASK 1836.134, HYBRID TWO-STEP PLLS FOR DIGITAL SOC'S IN NANOSCALE CMOS

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SIGNIFICANCE AND OBJECTIVES

PLL's are a critical part of today's communication systems. Their performance optimization is essential for modern SoC's. The objective of this project is to replace the bulky on-chip inductors used in low-jitter PLL's with compact ring oscillators, while still preserving the performance. This calls for development of a hybrid two-step PLL.

TECHNICAL APPROACH

The overall frequency conversion is divided into two cascaded stages (Fig.1). The first stage, employing noise cancellation, generates a high quality, high frequency reference for the second stage. A novel noise cancellation technique is employed to achieve low noise, high ratio frequency multiplication. The wide loop bandwidth allows the usage of compact ring oscillators. The second stage, a fractional-N PLL, provides the required fine resolution. Due to the low-ratio multiplication, it has much reduced noise impact.

SUMMARY OF RESULTS

The usage of large bandwidth (>1MHz) in the two-step PLL architecture (Fig. 1) reduces the noise impact of the VCO's. This enables the usage of compact ring oscillators in spite of their poorer performance in comparison to large-size LC oscillators. The large BW also helps in shrinking the loop filter area, further reducing the area of the PLL. The research is currently focused on the first-stage ring-oscillator PLL architecture and circuit design. The PLL uses a high-gain, low-noise sampling phase detector that maintains the phase lock between the VCO and reference frequency. The PLL has a high loop bandwidth of 2.5 MHz.

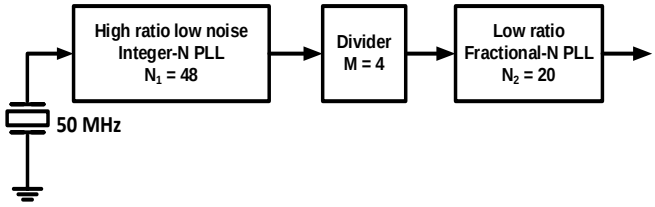

Figure 1. Block diagram of the proposed two step PLL.

The key innovation we are prototyping for the first-stage ring-oscillator PLL is the use of a feed-forward phase-noise-cancellation stage following the output of the PLL. The cancellation is implemented with a variable delay that receives its control information from the sub-sampling phase detector itself.

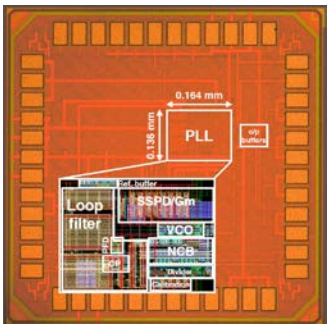

Figure 2. Die photo of the ring-oscillator PLL prototype with feed-forward noise cancellation.

The PLL prototype was taped out in 65-nm CMOS (Fig. 2) in May 2016. The phase noise measurement results for the first-stage PLL before and after cancellation are shown in Fig. 3. The RMS jitter reduces by 1.4 times from 890 fs to 630fs.

A new prototype PLL with enhanced loop bandwidth for better noise performance has been taped out in May 2017.

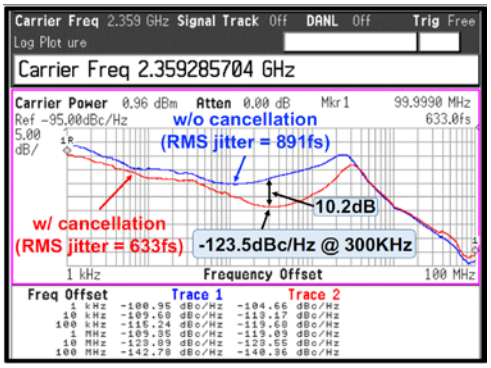

Figure 3. Measured phase noise of the first-stage PLL prototype, before and after noise cancellation.

Keywords: two-step PLLs, sub-sampling phase detectors, ring oscillators, wide-band phase noise cancellation.

INDUSTRY INTERACTIONS

Intel, Texas Instruments, Globalfoundries.

MAJOR PAPERS/PATENTS

[1] Shravan Nagam and P. R. Kinget, "A -236.3dB FoM Sub-Sampling Low-Jitter Supply-Robust Ring-Oscillator PLL for Clocking Applications with Feed-Forward Noise-Cancellation," 2017 IEEE Custom Integrated Circuits Conference (CICC).

TASK 1836.136, INJECTION-LOCKED RING OSCILLATORS FOR CLOCK DISTRIBUTION IN MANYCORE PROCESSORS

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SIGNIFICANCE AND OBJECTIVES

Technology scaling has enabled integration of many independent processing elements on a single die or in the same module. Energy-efficient circuit design for synchronization of manycore processors, based on both traditional PLL's and DLL's and on injection-locked ring oscillators is the objective of this work.

TECHNICAL APPROACH

We are developing a low-overhead global clock distribution scheme for manycore processors and heterogeneous SoC's. We have studied distribution based on DLL's and injection-locked MDLL's and implemented prototypes on several test chips.

SUMMARY OF RESULTS

We have developed three designs for clock generation in manycore processors, based a central PLL, followed by a per-core delay-locked loop (DLL) or a multiplying DLL (MDLL), and implemented them in four test chips (Fig 1). In the first approach [1-2], a ~2GHz reference clock is distributed to DLL's, which generate 16 uniformly-distributed clock phases. A phase-picking clock generator picks the appropriate phase for each clock cycle, based on an information from the timing replica path.

The design, implemented in a 28-nm ultra-thin body and BOX fully-depleted silicon-on-insulator (UTBB FDSOI) technology is fully functional and occupies 32µm x 30µm (Fig. 1). Generated clock frequency is in the range 550-2260MHz at 1V and 100-625MHz at 0.5V.

The second clock generation scheme is self-timed [2]. Figure 2 shows the schematic of the adaptive clock generator. The delay units are composed of four tunable delay banks, each of which uses a different cell for its delay element and can be tuned independently. Instead of using the delay line outputs for selecting DLL phases, in this approach we simply asynchronously toggle a standard flip-flop through its set/reset inputs. This design was also implemented in a 28-nm UTBB FDSOI process and achieved similar performance with much lower complexity.

Finally, the main clock in our third 28-nm test chip is generated by using a bang-bang ring-oscillator based PLL with pseudorandom dithering to eliminate spurs. It is coupled to an injection-locked MDLL in the fourth chip.

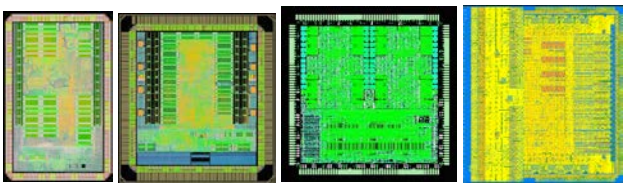

Figure 1. Four test chips.

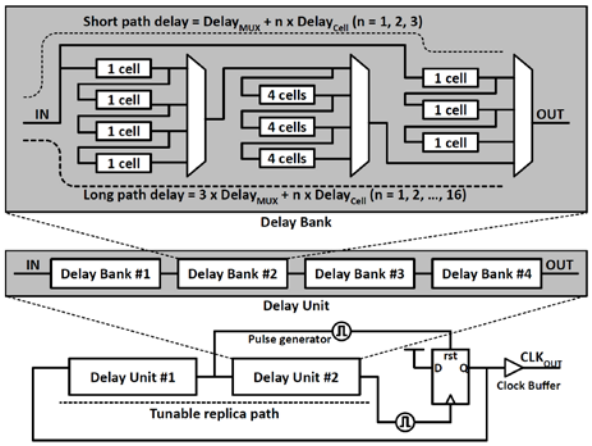

Figure 2. Self-timed clock generation.

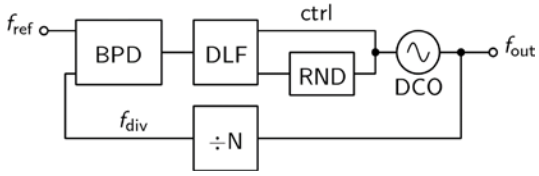

Figure 3. Bang-bang PLL.

Keywords: CMOS, clock, manycore, DLL, PLL.

INDUSTRY INTERACTIONS

Intel

MAJOR PAPERS/PATENTS

[1] B. Zimmer, *et al*, "A RISC-V vector processor with simultaneous-switching switched-capacitor DC-DC converters in 28nm FDSOI," *IEEE Jo. Solid-State Circuits*, 2016, vol. 51, no. 4, pp. 930-942, Apr. 2016.

[2] J. Kwak, B. Nikolić, "A self-adjustable clock generator with wide dynamic range in 28nm FDSOI," *IEEE Jo. Solid-State Circuits*, vol. 51, no. 10, pp. 2368-2379, Oct. 2016.

[3] B. Keller, et al, "A RISC-V processor SoC with integrated power management at sub-microsecond timescales in 28nm FD-SOI," to appear in *IEEE Jo. Solid-State Circuits*, vol. 52, no.7, Jul. 2017.

TASK 1836.137, 50GS/S AND BEYOND FREQUENCY-INTERLEAVED ENERGY-EFFICIENT ADCS

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SIGNIFICANCE AND OBJECTIVES

This research explores a novel ADC architecture to realize a frequency-interleaved analog-to-digital conversion (FI-ADC), ultimately to push the performance limits of very high-speed ADC's. Performance of conventional high-speed ADC's is limited by jitter and we aim to determine if and how the FI-ADC can mitigate the jitter sensitivity of high-speed ADC's.

TECHNICAL APPROACH

One of the key focus areas of this work has been the development of a comprehensive model for comparing the FI-ADC to the time-interleaved ADC (TI-ADC). A comprehensive quantitative analysis was performed in addition to system-level simulations that compare the two architectures. The simulations support the theoretical findings and additionally provide further insight into the conditions under which the FI-ADC outperforms the TI-ADC.

SUMMARY OF RESULTS

One of the key results from this work is the detailed analysis of the impact of jitter and phase noise on the FI-ADC. Previous works have hinted at the reduced jitter sensitivity of the FI-ADC due to the reduced bandwidths presented to the sampling network, but have failed to provide an analysis of the impact of phase noise introduced during the downconversion which occurs in each passband channel. Quantitative analysis shows that the phase noise on the LO's used for downconversion plays a critical role in determining if the FI-ADC outperforms the TI-ADC. In general, the FI-ADC has the potential to improve performance for high input frequencies but may sacrifice performance at lower frequencies depending on the implemented architecture.

Figure 1 shows a comparison of the SNR vs. input frequency for the two architectures. For our design, the FI-ADC outperforms the TI-ADC. Figure 2 shows the SNR improvement against different number of channels for different mixing architectures. Using our comprehensive model, we can predict the maximum achievable SNR. Results have been published in Techcon 2016 in detail [1].

A new chip in 28-nm CMOS has been fabricated to explore an approach for the FI-ADC based on the interactive down-conversion approach [2]. This chip has returned from fabrication and will be tested in the summer of 2017.

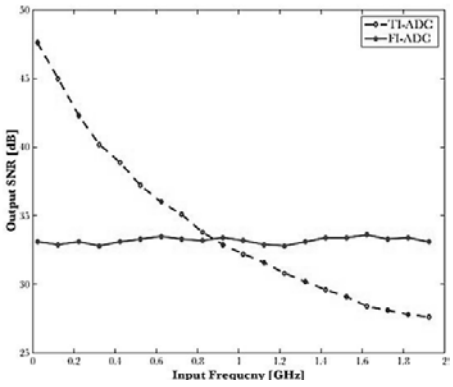

Figure 1. System-level simulations of the FI-ADC and TI-ADC.

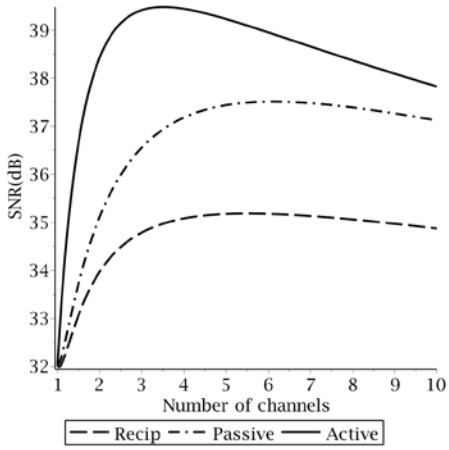

Figure 2. Achievable SNR for FI-ADC using different mixing architectures.

Keywords: high-speed ADC, frequency-interleaved, channelized front-end, wideband receiver

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] N. Baniasadi and A. M. Niknejad, "Jitter Analysis in Frequency-Interleaved ADC's," Techcon 2016.

[2] Krishnaswamy et al., "RF channelizer architectures using Iterative Downconversion for concurrent or fast-switching spectrum analysis," 2014 IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS), College Station, TX, 2014, pp. 977-980.

TASK 1836.141, IC DESIGN FOR RESILIENCE AGAINST SYSTEM-LEVEL ESD

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SIGNIFICANCE AND OBJECTIVES

System-level ESD reliability is uncorrelated with component-level ESD reliability yet IC designers are asked to build-in system-level ESD resilience. This project's objective is to develop integrated circuit designs that are resilient to power-on ESD and a behavioral model of the IC that can be used for system ESD design.

TECHNICAL APPROACH

ESD testing of a prototype system containing a custom test chip is used to ascertain the causes of ESD-induced soft failures. Each test chip's rail clamp circuits are designed for power-on ESD. The test chips contain supply noise monitor circuits as well as circuitry to detect out-of-range IO signals or glitches. On-chip supplies are powered from either an external voltage regulator or an integrated regulator. Circuit simulations are performed to ascertain whether they can accurately predict an IC's internal response to system-level ESD. A piecewise linear model with a transient relaxation (PWL-TR) model template is developed for modeling ESD protection devices.

SUMMARY OF RESULTS

If a large ESD current is allowed to enter an IC, e.g., in the absence of on-board protection, supply bounce on the order of volts arises if (1) an active rail clamp circuit becomes biased in an unstable operating regime, or (2) there is severe Ldi/dt noise due to the package inductance. Active rail clamp circuits that eliminate the first hazard were demonstrated. Eliminating Ldi/dt noise on the supply is more difficult. The ESD current is shunted, by design, to the power and ground busses and its time-derivative can be as large 10^{10} A/s. Nanofarad-scale on-chip decoupling capacitance will reduce the supply noise, but the area penalty is excessive. Integrated voltage regulators provide a feasible way to reduce supply noise propagation from the IO supply to the other on-chip power supplies, referred to as the "core" supplies. If the core supplies are powered from an external regulator, measurement and simulation both show that the noise on the core supply bus is comparable to that on the IO supply bus. The ESD-induced noise propagates from the IO supply domain to the core supply domain(s) via the ground net(s). ESD design guidelines for on-chip LDO were formulated and validated in a 65- nm Design A (good power supply integrity) and 130-nm Design B (poor power supply integrity) – see Fig. 1, and Tables 1 and 2.

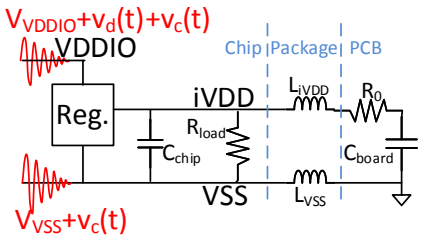

Figure 1. ESD noise propagates from the high-voltage (VDDIO) supply to a lower-voltage supply net (iVDD). An LDO provides integrated voltage regulation. iVDD will be quiet if C_{board} = 0 and/or the LDO has high gain and bandwidth.

Table 1. Design A. eVDD and iVDD are externally and internally generated 1.2-V supplies, respectively. Bit flips in latches are first observed at the ESD levels listed; iVDD is quieter.

eVDD	+2 kV	-2 kV
iVDD	+6 kV	-6 kV

Table 2. Design B. eVDD and iVDD are 1.5-V supplies. The table lists the ESD level at which V_{min}—the lowest voltage excursion on the supply fell below the given threshold. iVDD is even more noisy than eVDD.

	eVDD	**iVDD**
V_{min} < 1.15 V	± 1 kV	± 0.5 kV
V_{min} < 0.54 V	+3 kV; -5 kV	-2 kV
V_{min} < 0.13 V	+4 kV	+1.5 kV; -3 kV

If the ESD current is prevented from entering the chip by good system design (shielding) or with the use of on-board protection (transient voltage suppressor), magnetic coupling and/or radiated emissions still produce glitches at input pins. Input circuits that operate at an increased voltage (e.g. 2.5-3.3 V rather than 1-1.5 V) are able to reject the noise; however, low-voltage IO circuits without filters or Schmitt triggers are found to have logic errors at fairly low ESD levels (e.g. 2 kV IEC 61000-4-2). In such cases, the signaling protocol must be designed to reject the noise.

Keywords: ESD, soft failures, modeling

INDUSTRY INTERACTIONS

Intel, NXP, Texas Instruments

MAJOR PAPERS/PATENTS

[1] Y. Xiu et al., "Chip-level ESD-induced noise on internally and externally regulated power supplies," accepted for presentation at *2017 EOS/ESD Symp*.

[2] M. Keel and E. Rosenbaum, (Invited) "CDM-reliable T-coil techniques for a 25-Gb/s wireline receiver front-end," *IEEE Trans. Dev. Materials Rel.,* vol. 16, no. 4, 2016.

TASK 1836.145, RF AND MIXED SIGNAL QUANTUM CMOS DEVICES AND CIRCUITS

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YUN CHIU, THE UNIVERSITY OF TEXAS AT DALLAS

SIGNIFICANCE AND OBJECTIVES

This project pioneers a path towards explicit quantum mechanical operation in industrial CMOS by demonstrating a new class of quantum MOS devices and circuits. This work will develop understanding of quantum MOS device physics and incorporation of such devices into RF and mixed-signal circuits operating at or near room temperature.

TECHNICAL APPROACH

This project introduces quantum well (QW) NMOS transistors showing quantum transport characteristics in the form of negative transconductances (NTC's). A main focus is to understand the device physics and how to make QW NMOS devices useful in circuits designed to exploit the NTC's. In the past year we showed that QW NMOS devices can have intrinsic gain magnitudes exceeding unity at room temperature in both conventional and quantum operation regimes. This result proves that QW NMOS devices can be potentially useful in amplifier and oscillator circuits.

SUMMARY OF RESULTS

Over the third year of this project we completed full characterization of the intrinsic gain characteristics of QW NMOS devices. Devices showing NTC can be highly useful in amplifiers and oscillators. However, a significant concern with QW NMOS is that in the NTC regime the devices used in [1] had voltage gain $A_V = \partial V_{DS}/\partial V_{GS}$ with $|A_V| < 1$ at room temperature, limiting output power. It has been uncertain whether a QW NMOS could exhibit $|A_V| > 1$ when biased to a NTC regime at room temperature. This is an important question because a sub-unity gain magnitude would curtail the use of QW NMOS devices in amplifier and oscillator applications and restrict their ability to drive subsequent circuit stages without a buffer. For these reasons it was imperative to elucidate whether QW NMOS devices can operate with $|A_V| > 1$ near 300 ^{o}K.

Fig. 1 summarizes the complete set of gain data on a typical QW NMOS at room temperature as a contour map showing gain as a function of V_{GS} and V_{DS}. The sign of A_V follows the sign of transconductance, so operation in a NTC means $A_V < 0$. In such a quantum regime, $|A_V| > 1$ only for $V_{DS} > 0.75$ V. Previous studies showing $|A_V| < 1$ did not explore a high enough drain bias regime.

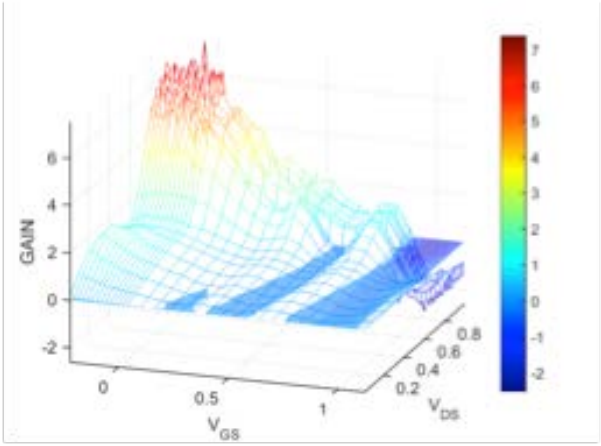

Figure 1. Complete map of gain for a typical QW NMOS device as a function of bias V_{GS} and V_{DS} at room temperature. The sign of gain depends on whether the QW NMOS is biased in conventional operation (gain > 0) or QW operation (gain < 0). The blue plane indicates the plane of gain = 0.

Typical gains measured in the QW NMOS were 7 to 8 in the positive and –3 to –2 in the negative gain regimes. The positive gains are 10 to 13 times smaller than the gain values measured in conventional NMOS devices with the same layout fabricated on the same wafer die. Finally, the NTC features result in an oscillatory gain as a function of V_{GS}. In addition to a non-constant gain, this means that $|A_V| > 1$ over ranges of V_{GS} values of 0.2 to 0.3 V. In practice this can be expected to limit input swing in a circuit.

Keywords: quantum devices, quantum circuits, negative differential conductance, quantum well, quantum CMOS

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] C. Naquin, Y. Cai, G. Hu, M. Lee, Y. Chiu, H. L. Edwards, G. Mathur, T. Chatterjee, and K. Maggio, "Application of a Quantum-Well Silicon NMOS Transistor as a Folding Amplifier Frequency Multiplier", IEEE *J. Elec. Device Soc.* vol 5, no. 3, pp. 224-231 (2017)

[2] G. Hu, U. Wijesinghe, C. Naquin, K. Maggio, H. L. Edwards, and M. Lee, "Positive and Negative Gain Exceeding Unity Magnitude in Silicon Quantum Well NMOS Transistors," submitted to IEEE *J. Elec. Device Soc.* (2017)

TASK 1836.148, 50GSPS+ TI HYBRID SAR ADC ARRAY WITH COMPREHENSIVE DDI CALIBRATION

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SIGNIFICANCE AND OBJECTIVES

Time interleaving is an effective way to increase analog-to-digital conversion (ADC) speed. A low-power, high-speed sub-ADC is needed to reduce the interleaving complexity and power consumption. This work introduces a V-T hybrid two-step SAR ADC that meet both the speed and the efficiency targets. Also, a reference dither based skew calibration is introduced to calibrate the timing mismatch of the interleaving array.

TECHNICAL APPROACH

A comparator's resolving time is roughly inversely proportional to its input voltage magnitude. In this work the comparator resolving time of the residue voltage on the summing node of a SAR ADC is quantized by the second-stage time-to-digital converter (TDC), resulting in an efficient two-step quantization structure. A slow-but-accurate reference ADC with precise timing is introduced and used as timing reference of the array. The ref. ADC clock is modulated by a 1b pseudorandom signal and the skew information is extracted by correlating the PN signal with the output difference between the ref. ADC and the sub-ADCs.

SUMMARY OF RESULTS

The previous phases of this project we designed and tested a 24GS/s TI-ADC. Important lessons are learned from that design and paves our way to the 50GS/s TI-ADC. Instead of doubling the interleaving factor to achieve twice sampling frequency, some crucial modification is necessary. Our plan is to keep the interleaving factor=16 and increase the single channel speed to 3.125GS/s with multibit/stage approach. This allows us to keep a simple floor plan and to minimize the calibration overhead. Also hierarchical sampling will be adopted to alleviate the burden of front-end sampling and skew calibration.

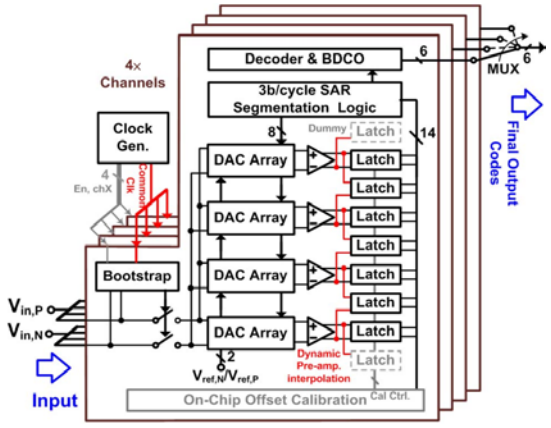

Figure 1. 3b/cycle SAR [Chan, ISSCC 2015].

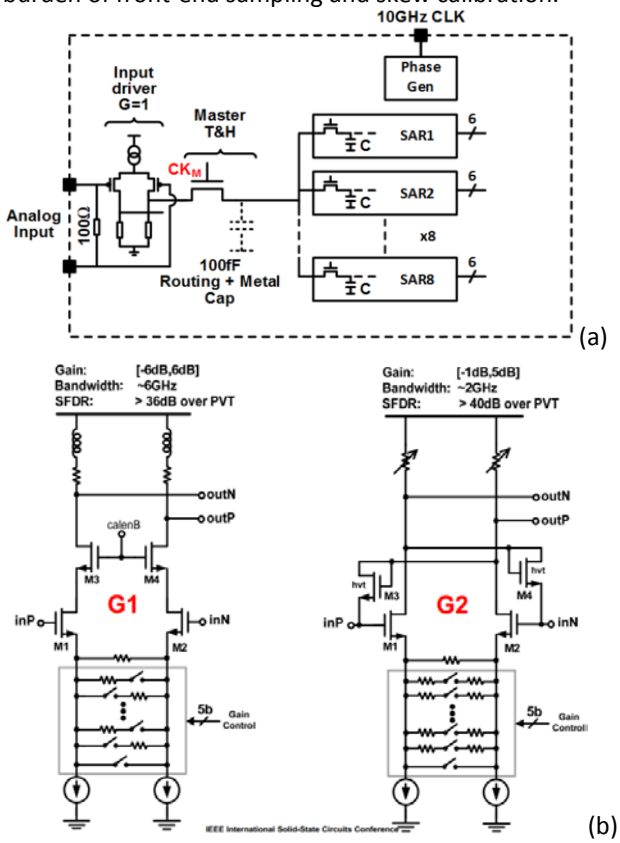

Figure 2. (a) common source input buffer [Le Tual, ISSCC 2014] (b) common source with inductive peaking buffer [Varzaghani, JSSC 2013].

Keywords: TI-ADC, calibration, hybrid SAR, reference-ADC equalization, direct derivative information

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] B. Xu, Y. Zhou, and Y. Chiu, "A 23-mW 24-GS/s 6-bit voltage-time hybrid time-interleaved ADC in 28-nm CMOS," IEEE Journal of Solid-State Circuits, vol. 52, pp. 1091-1100, Apr. 2017.

[2] U.S. Patent application # 15/620,821, "Pipelined SAR ADC using comparator as a voltage-to-time converter with multi-bit second stage," Jun. 2017.

TASK 1836.157, CMOS GSPS 12-BIT SAR ADC ARRAY WITH ON-CHIP REFERENCE BUFFERS

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SIGNIFICANCE AND OBJECTIVES

ADC's that can deliver GS/s, 12-14-bit performance are of critical demand for applications such as wireless base stations, instrumentations, and software-defined radios, and usually consume more than 500 mW. The target of this work is to time-interleave 4 pipelined two-step SAR ADC's to achieve GSPS throughputs at a 12-bit resolution with a power consumption of less than 50 mW.

TECHNICAL APPROACH

The sub ADC used in the time-interleave array is based on the pipelined two-step SAR architecture which can deliver a desirable throughput while maintaining high power efficiency [1]. To further enhance the conversion speed, a 2b/cycle conversion scheme is exploited by the first stage [2]. The offsets of first-stage comparators are calibrated in a foreground way to remove the impact on the overall conversion accuracy. Meanwhile, the dynamic amplifier is employed as the inter-stage residue amplifier. Benefiting from the dynamic amplifier, a very power efficient residue amplification that also consumes less time relative to the conventional amplifier is obtained.

SUMMARY OF RESULTS

A 4-way time-interleaved SAR ADC array in 65-nm CMOS has been taped out. It consists of 4 single channel pipelined SAR ADC's operating at a 250MS/s conversion rate. The design is based on our previous work published in [1] and [4]. The calibration algorithm published in [2] is implemented in this work to calibrate the inter-channel gain, offset and skew mismatches.

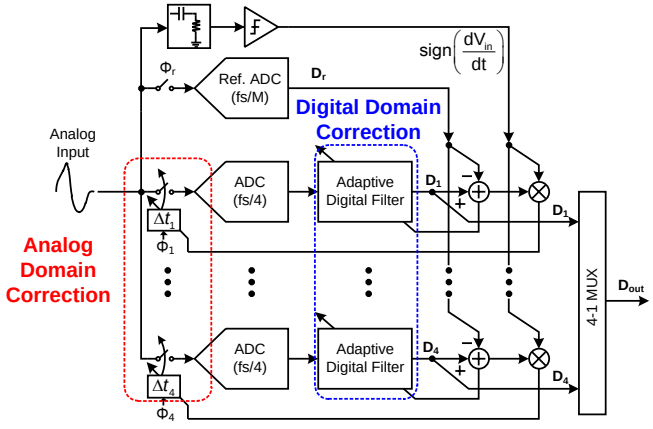

Figure 1. Block diagram of the prototype 12b, 1GS/s time-interleaved ADC array.

Fig. 1 illustrates the block diagram of the prototype TI-ADC. The sub-ADC's utilize an asynchronous SAR timing scheme, with integrated on-chip reference buffers. The SAR raw outputs are background calibrated in the digital domain. Four digitally controlled delay lines (DCDL) are also employed to fine-tune the sampling clock phases of the sub-ADC's to minimize any skew mismatch errors.

Fig. 2 shows a layout screenshot of the 12bit 1GS/s ADC array implemented in the Globalfoundries 65-nm CMOS process. The reference ADC and the high-pass filter are all implemented on-chip. Table 1 summarizes the post-layout simulation results.

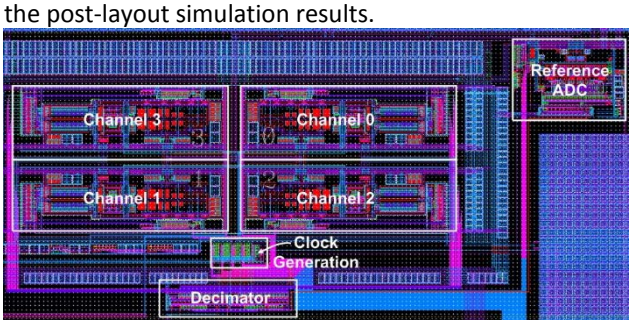

Figure 2. Layout screenshot of the prototype.

Table 1. Summary of the post-layout simulation results

Process	65-nm CMOS	
Sampling speed	1 GS/s	
Input swing	2.4 V	
SNDR	71.5 dB	
	Single	5.5mW
	Total	30.0mW

Keywords: time-interleaved ADC, split-ADC, pipelined two-step SAR, dynamic amplifier

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] H. Huang, L. Du, and Y. Chiu, "A 1.2-GS/s 8-bit two-step SAR ADC in 65-nm CMOS with passive residue transfer," IEEE Journal of Solid-State Circuits, vol. 52, pp. 1551-1562, Jun. 2017.

[2] H. Huang, S. Sarkar, B. Elies, and Y. Chiu, "A 12b 330MS/s pipelined-SAR ADC with PVT stabilized dynamic amplifier achieving <1dB SNDR variation," in IEEE ISSCC'17, San Francisco, CA, 2017.

TASK 2712.003, MULTI-MODAL BIST DESIGN AND TEST METRICS EVALUATION FOR ANALOG/RF CIRCUITS

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SIGNIFICANCE AND OBJECTIVES

This project aims at developing a BIST methodology for analog and RF circuits that relies on building blocks that can be redesigned with a minimal effort. These building blocks will be used with mathematical models and analyses to extract desired parameters of analog/RF circuits without relying on BIST circuit performance.

TECHNICAL APPROACH

The proposed approach is based on three principles. A library of BIST components for on-chip excitation and measurement will be built and characterized. The goal is to make most library components parametrizable so they can be used in many applications. Along with the library of building blocks, mathematical models will be developed to extract target parameters independent of circuit behavior. A design automation flow will be developed to analyze a target circuit under test and target specifications and insert the necessary BIST components. The BIST circuit will be co-designed with the primary circuit to avoid performance degradation.

SUMMARY OF RESULTS

We have developed a streamlined method for using low-linearity analog to digital and digital to analog converters for high precision testing. The concept is to extract and decouple complex non-linearity coefficients of the DAC/ADC pair as a first step and use these coefficients to pre-distort or de-embed the parameters of the device under test. In order to do this, we first connect the DAC/ADC pair in a loopback configuration. A sinusoidal input will be used to excite the DAC/ADC pair and spectral analyses will be performed using the digital output. Harmonics at the output are measured to compute the non-linearity coefficients. For this extraction, we use a Volterra-series model for the ADC and DAC. In our experiments, we used a 5th order model both for the ADC and for the DAC. A non-linear solver can be used to match the measured power of each harmonic to the mathematical model.

While this process seems straightforward at first look, decoupling the parameters of two cascaded blocks is not possible due to the equations becoming linearly dependent. Thus, we need an approach to generate more linearly independent equations. There are multiple ways of accomplishing this. One way is to introduce a DC offset between the DAC output and the ADC input. Another way is to introduce an attenuator in the same location. We have chosen the attenuator option because it can be implemented with simple resistive (or capacitive) dividers. Figure 1 shows the overall architecture of this DAC/ADC non-linearity coefficient characterization. α_1 through α_5 are the coefficients of the DAC response and β_1 through β_5 are the coefficients of the ADC. K is the attenuator value and ω is the frequency of excitation.

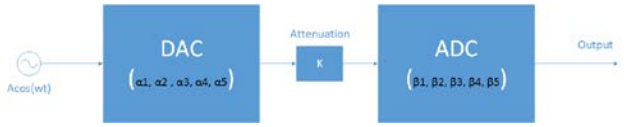

Figure 1. DAC/ADC loop-back for characterization of non-linearity coefficients.

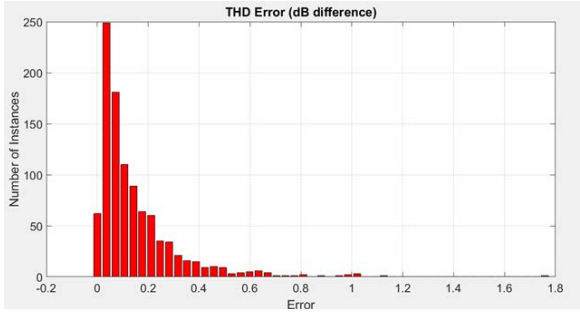

Figure 2. Error in computing the total harmonic distortion of the ADC when looped-back with a nonlinear DAC based on the decoupling approach.

Figure 2 shows the results of the extraction process using MATLAB based Monte-Carlo simulations. Figure represents the results form 100 simulation samples.

Keywords: BIST, non-linearity, ADC characterization

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

[1] M. Ince, E. Yilmaz, L. Winemberg, and S. Ozev, “Evaluation of Loop Transfer Function Based Dynamic Testing of LDOs", accepted at ITC Asia.

TASK 2712.004, HIERARCHICAL ANALOG AND MIXED-SIGNAL VERIFICATION USING HYBRID FORMAL AND MACHINE LEARNING TECHNIQUES

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SIGNIFICANCE AND OBJECTIVES

On one hand, formal verification is appealing as it provides a provable "yes/no" answer w.r.t the specifications under check. However, capturing essential nonlinear/analog device/circuit effects significantly complicates the circuit model that must be verified formally, and severely limits the scalability. To date, formal techniques are only feasible for small analog blocks described using idealistic models, falling much behind the practical industrial needs. On the other hand, one may employ machine learning to extract performance models for AMS verification with the key advantages being data-driven, incremental, and much more scalable, particularly when a sufficient amount of training data can be collected either through simulation or silicon measurement. However, learning-based models do not provide a formal answer, and come with inherent uncertainty. This work aims to address the above challenges by taking a hybrid formal and machine learning approach.

TECHNICAL APPROACH

This project presents a new perspective in AMS verification with a hierarchical framework that simultaneously exploits formal and machine learning techniques, as depicted in Fig. 1. This framework has the best of the two worlds: it adds a degree of formalism on top of learning-based models by utilizing satisfiability modulo theories (SMT) based formal techniques; and it is much more scalable than pure formal techniques at the same time. While existing vendor tools often assume that underlying process variations are Gaussian, the formal nature of the proposed framework will be exploited to account for both statistically characterized variations and pure design uncertainty, for the latter of which no statistical assumptions are made. Furthermore, the proposed framework "formally" bounds learning model uncertainty and extract trustable behavior models for scalable simulation and verification of large AMS circuits consisting of multiple building blocks.

SUMMARY OF RESULTS

As a first step, we formulate our hybrid verification problem as one that checks if a targeted specification is met with at least a probability of P_0 in a given uncertainty (parametric) space (e.g. the space of PVT parameters).

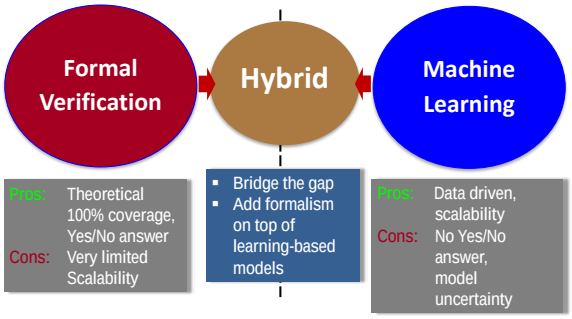

Figure 1. Hybrid verification approach aims to bridge the gap between formal and machine learning based techniques.

The formal nature of the above problem stems from the fact that the above check is performed exhaustively in the entirety of the uncertainty space. To make the problem computationally tractable and to predict the performance over the uncertainty space, a trained probabilistic machine learning model (e.g. one that is based on Bayesian learning) is adopted. The hybrid methodology does not depend on any specific choice of probabilistic machine learning models, and hence is rather generic.

Quiescent Current I_q (mA): I_q < Spec				Overshoot (mV): Overshoot < Spec			
Spec	# Failures in 30K SPICE	# Failures by Hybrid	Runtime of Hybrid	Spec	# Failures in 30K SPICE	# Failures by Hybrid	Runtime of Hybrid
7.9 mA	0	0	<1s	70 mV	0	0	12h26m
7.5 mA	0	*19	12h08m	60 mV	0	*12	13h18m
7.0 mA	24	*68	11h42m	50 mV	1	*8	13h21m

Figure 2. Hybrid verification of quiescent current and overshoot of an LDO under 60 correlated L_{eff}, T_{ox}, and V_{TH} variations.

As a preliminary demonstration, we consider an LDO subjected to 60 transistor-level process variations. The LDO has several different specification targets for quiescent current and overshoot. As in Fig. 2, 30,000 time-consuming random SPICE simulations completely miss all design failures. Our hybrid verification technique can catch multiple small discretized failure regions.

Keywords: machine learning, formal verification, hybrid verification, analog and mixed-signal.

INDUSTRY INTERACTIONS

Intel, Texas Instruments

MAJOR PAPERS/PATENTS

TASK 2712.005, AUTOMATED CROSS-LEVEL VALIDATION AND DEBUG OF MIXED-SIGNAL SYSTEMS IN TOP-DOWN DESIGN: FROM PRE-SILICON TO POST-SILICON

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SIGNIFICANCE AND OBJECTIVES

Given a hierarchical design description (behavioral to transistor level to manufactured silicon), we desire to determine if it contains one or more design bugs (errors) and to automatically generate bug diagnostic information that can be used to "fix" the design as early on in a top-down design methodology as possible.

TECHNICAL APPROACH

A completely automated algorithmic framework based on collaborative test stimulus generation and behavior learning is proposed for systematic debug of mixed-signal systems in the presence of unknown (buggy) circuit behavior. The proposed approach is driven by: (a) rapid detection and diagnosis of (unknown) logical and electrical bugs with a minimal amount of computational effort using directed search strategies, (b) automatic generation of bug models using learning algorithms that can be fed back to the designer for design error correction, and (c) response-inconsistency driven diagnosis of multiple design bugs down to individual design macro-blocks or sets of modules of minimum size.

SUMMARY OF RESULTS

Initial efforts have focused on automated design bug learning algorithms and on design bug diagnosis. The latter uses localized behavior learning around design sub-modules. Both bug learning and bug diagnosis are driven by stochastic test generation algorithms that excite unknown design behaviors using iterative cost optimization algorithms.

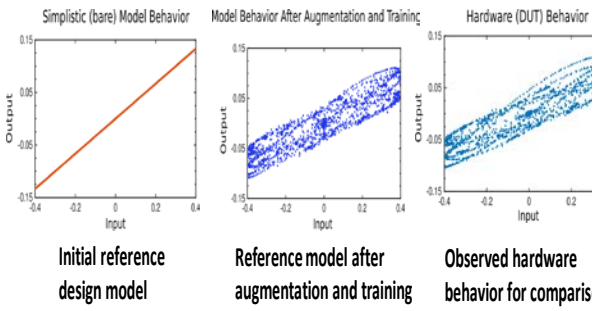

Figure 1. Behavior learning on RF power amplifier.

For behavior learning, the reference design is augmented with a system bug learning kernel (e.g. Neural network, Volterra and Wiener filters) which is trained to "eliminate" the behavioral differences observed using machine learning algorithms. After initial bug effects are nulled, test generation followed by machine learning is repeated again to discover other bugs. This is repeated in an iterative manner until no further behavioral differences between the reference design and the DUV can be found using test stimulus generation. At the end of this procedure, a set of learning kernels that describe the behavioral differences observed in each iteration of testing and machine learning procedure is obtained. These collectively describe the behaviors induced by logical and electrical bugs in the design (electrical bugs are harder to model in simulation but can be excited in fabricated silicon). Figure 1 shows the ideal model (left), "learned" model (center) and corresponding hardware measurements (right) for an RF power amplifier. Note that the "learned" model accurately captures hysteresis in the amplifier.

Experiments were also conducted to validate the proposed bug diagnosis approach. This involves the use of localized bug learning kernels around each of the design sub-modules in turn. Minimum error of the expected vs. the observed error at the system output occurs when the bug effects are compensated at their source (the affected module) vs. other bug-free modules. The method has been demonstrated on RF devices and a PLL design.

Keywords: design validation, test generation, machine learning, mixed-signal, radio-frequency

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] B. Muldrey, S. Deyati and A. Chatterjee, "Post-Silicon Validation: Automatic Characterization of RF Device Nonidealities via Iterative Learning Experiments on Hardware," International Conference on VLSI Design, Hyderabad, 2017, pp. 403-408.

[2] B. Muldrey, S. Deyati and A. Chatterjee, "DE-LOC: Design validation and debugging under limited observation and control, pre- and post-silicon for mixed-signal systems," 2016 IEEE International Test Conference (ITC), Fort Worth, TX, 2016, pp. 1-10.

TASK 2712.007, HIGH-RESOLUTION LOW-VOLTAGE HYBRID ADC'S FOR SENSOR INTERFACES

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SIGNIFICANCE AND OBJECTIVES

The goal of this research is extend the state-of-the-art of high resolution sensor interface ADC's through research and development of a hybrid ADC architectures, that are also easy to drive.

TECHNICAL APPROACH

This new class of converters will facilitate and improve sensing and IoT applications. These needs are currently unmet since state-of-the-art low-power ADC's are difficult to drive (i.e. requiring filter and input buffer), and are limited in either resolution or power consumption. This research addresses SRC needs C1.1 "Very energy efficient digital and analog circuits", C4.1 "Area efficient analog/RF/Clocking/IO design in scaled digital technologies", and C4.4 "Low voltage digital and analog circuit design including moderate inversion and weak inversion regions of operation".

In this research, we will develop and demonstrate a new 14-16b, low power ADC for sensors. The goal is also to make the ADC easy to drive. Power consumption of the driver and references will be considered in addition to the ADC power to achieve the best overall system performance.

Although tremendous progress has been made on the energy efficiency of ADC's, they are still a bottleneck in many systems because they are difficult to drive and suffer from many other practical limitations. SAR ADC's have impressive reported efficiency, however, the large switched capacitive input in a moderate/high resolution SAR necessitates a highly capable ADC driver which itself consumes considerable power. For example, the highly efficient TI OPA835 (-70dB HD2) SAR ADC driver consumes 1mW, which dwarfs the ADC power. Moreover, SAR ADC energy efficiency drops steadily as the ADC ENOB increases above 10b. The anti-alias filter is another huge challenge to the practical implementation of many systems. If a near-minimum sampling speed is selected to minimize ADC power, then the resulting sharp cutoff anti-alias filter can easily be more challenging to design than the ADC itself.

ADC's for sensors are often implemented as SAR or oversampling ADC's. SAR ADC's achieve excellent energy efficiency, but are limited to a moderate resolution. Calibration adds complexity, and may need to be adjusted continually with temperature and supply changes. Sigma Delta ADC's and incremental converters can achieve higher resolution, but are constrained by the requirements of the op-amps and switches.

Oversampled discrete time converters have the advantage of relaxing the specifications of the anti-alias filter. Sigma Delta converters are also relatively efficient at high ENOB. Nevertheless, discrete-time Sigma Delta ADC's in common with SAR ADC's and all discrete time ADC's, present a switched-capacitor input which is difficult to drive. Besides the switched load, a further challenge is the input side switch, which often limits the linearity.

SUMMARY OF RESULTS

Keywords: sigma delta, ADC, senor, IoT

INDUSTRY INTERACTIONS

Texas Instruments, Intel, ARM

MAJOR PAPERS/PATENTS

TASK 2712.010, RINGAMP-ASSISTED CIRCUITS/TECHNIQUES AND NEXT-GENERATION RINGAMPS

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SIGNIFICANCE AND OBJECTIVES

Owing to the degradation of key analog parameters, such as intrinsic gain and supply voltage, many state-of-art systems use digitally-assisted analog circuits. This often takes place as calibration circuits for non-ideal opamps. However, efficiency improvements can still be realized with improved analog circuits.

TECHNICAL APPROACH

This work's approach is to improve analog circuit efficiency utilizing ring amplifiers. A recent and prominent scalable circuit, the ring amplifier is based off a three-stage uncompensated architecture built out of inverter based blocks. This allows for low-power, low-area, high-accuracy switched-capacitor amplifiers. One approach will be to broaden the applications of ring amplifiers which have only been used as residue amplifiers. In addition, next-generation ring amplifiers will be designed and tested for increased efficiency.

SUMMARY OF RESULTS

Ring amplifiers can be thought of as a dynamic amplifier for switched-capacitors. They still operate in negative feedback with a fixed feedback factor and a high open-loop gain like traditional opamps. However, their bandwidth in general changes (decreases) during the amplification period. This allows ring amplifiers to achieve lower power settling when compared to traditional opamps. Driving large load capacitances is easy for ring amplifier stability as they contain a dominant pole at the output at the end of settling.

Ring amplifiers are not without limitations. The cascaded three-stage structure provides a high gain, but in scaled processes or high-resolution applications gain can still be a limitation. Gain can be increased by increasing the length of the output transistors, but it is eventually limited. Increasing the length of the first two-stages penalizes speed by moving non-dominant poles to lower frequency.

This work's approach is to instead use the ring amplifier in a correlated-level-shifting (CLS) MDAC (Fig. 1). The principle of CLS is to split amplification into an estimate and fine settling phases. The output voltage at the end of the estimate phase is added in series with the amplifier in the fine phase for increased gain.

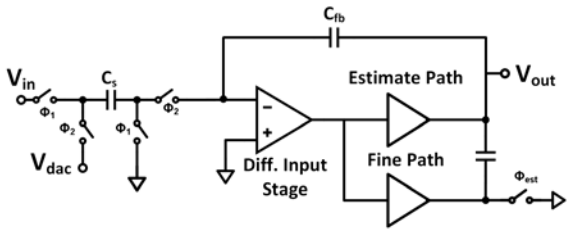

Figure 1. Correlated-level shifting MDAC.

The ring amplifier used in the CLS MDAC will be a dual-path ring amplifier. It involves two ring amplifier output-stages based off current-starved inverters driven by a singular differential pair. The two separate output stages allow the design of slewing and settling to be decoupled. Allowing the estimate path to be sized for slewing with no worry of settling allows for a low power solution. In addition, the first stage and its auto-zeroing capacitor are used in both phases, reducing area.

To demonstrate this technique, a 17 -bit pipeline has been designed incorporating the dual-path CLS ring amplifier. Designed in a 180-nm CMOS process, we expect about 4mW at 20MSPS. With Nyquist input, a 20-MSPS output spectrum is shown in Figure 2. With transient noise and extracted capacitors the analog-to-digital converter achieves 13+bit ENOB in simulation.

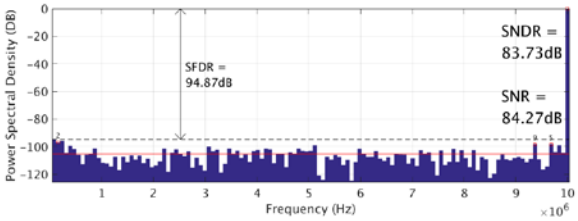

Figure 2. Nyquist input spectrum of 17-bit pipeline with extracted capacitors and transient noise.

Into the future, this 17-bit pipeline is expected to be evaluated in Fall 2017. Future work plans include the design of a ring amplifier assisted CTDSM, and investigation of ultra-low voltage applications.

Keywords: ring amplifier, analog-to-digital converter, scaling

INDUSTRY INTERACTIONS

Texas Instruments, Intel, NXP

MAJOR PAPERS/PATENTS

TASK 2712.011, ROBUST RELIABLE AND PRACTICAL HIGH PERFORMANCE REFERENCES IN ADVANCED TECHNOLOGIES

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DEGANG CHEN, IOWA STATE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

The primary objective is to develop new methods for building practical references that explicitly express the bandgap voltage at the output over a large range of temperatures with a single electrical trim. Significance will be in improved performance of references over what is attainable with existing state of the art.

TECHNICAL APPROACH

Emphasis will be placed on developing circuits that cancel all temperature dependence at the output leaving an output that is proportional to only the bandgap voltage, a physical constant. This is in contrast to most existing approaches that target circuits with a temperature derivative that vanishes at either a single temperature or two temperatures. If successful, we should be able to reduce or eliminate the T|ln(T) induced performance bound inherent in most existing approaches. Two test chips will be designed to obtain experimental verification of the performance of the new precision reference circuits.

SUMMARY OF RESULTS

The basic concept of expressing the bandgap voltage of silicon, V_{G0}, at the output of a circuit is depicted in Figure 1. The Bandgap Separator extracts V_{G0} which is embedded as an exponent in the I-V characteristics of a pn junction (1) and presents it as a linear term at the output, V_{BS}, along with a nonlinear temperature dependent term, bT+cTln(T) as indicated in (2).

$$I_D(T) = J_{SX} A T^m e^{-\frac{qV_{G0}}{kT}} e^{\frac{qV_D}{kT}} \quad (1)$$

$$V_{BS} = V_{G0} + bT + cT\ln(T) \quad (2)$$

A Temperature Sensor independently generates an output proportional to temperature. A Function Generator is used to generate the same nonlinear temperature dependent term which is then subtracted from V_{BS} to obtain an output, V_{REF}, that expresses the bandgap voltage at the output.

An implementation of a precision bandgap reference is shown in Figure 2. The nonlinear correction signals are generated with the diode-connected transistor Q_3 and the correction signals are summed into nodes V_A and V_B of the basic Banba voltage reference.

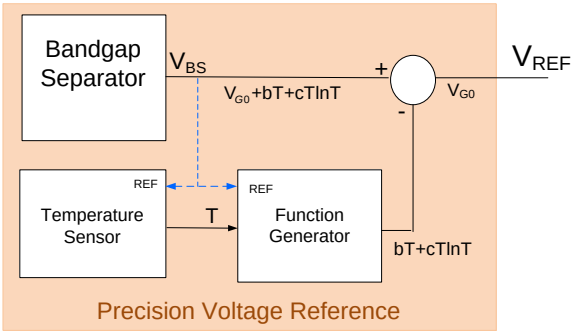

Figure 1. Precision voltage reference using Tln(T) isolation.

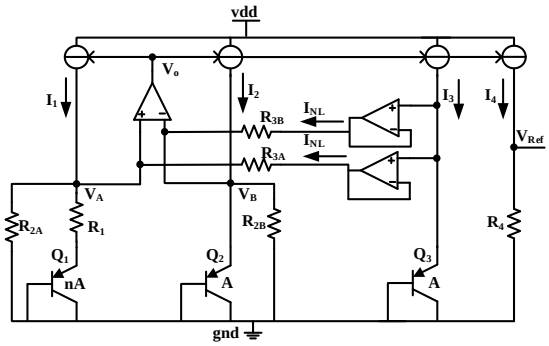

Figure 2. Precision bandgap reference.

Simulation results for an implementation of this circuit in a Globalfoundries 0.13-µm CMOS process with device matching provide an un-trimmed temperature coefficient over a 165°C temperature range of 0.25ppm/°C at TT and a worst-case temperature coefficient of 2.25 ppm/°C over the four process corners. This is contrasted to a theoretical best-case TC with trimming of several of the basic bandgap circuits of approximately 2.25 ppm/°C with a two-point trim over the same temperature range.

Keywords: bandgap, voltage veference, VGO, self-calibrated

INDUSTRY INTERACTIONS

Texas Instruments, NXP, Intel

MAJOR PAPERS/PATENTS

[1] Z. Liu and D. Chen, "A Voltage Reference Generator Targeted at Extracting the Silicon Bandgap V_{GO} from V_{BE}", IEEE International Symposium on Circuits and Systems (ISCAS), Baltimore, May 2017.

TASK 2712.014, LEVERAGING CMOS SCALING IN HIGH PERFORMANCE ADC'S

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SIGNIFICANCE AND OBJECTIVES

The objective of this work is to develop circuit and system level solutions to improve the performance of ADC's in scaled CMOS nodes in terms of speed, resolution, silicon area and power consumption.

TECHNICAL APPROACH

By introducing new approaches to multiple time/frequency conversions, we will exploit the reduced gate delay in the advanced nodes in the most efficient way. In these ADC's, the underlying principle will be to move towards time/phase based signal processing by leveraging existing structures such as Noise-shaped Integrating Quantizer [1] and GRO/VCO quantizer [2] in combination with new scalable innovative solutions.

SUMMARY OF RESULTS

Our latest effort published at ISSCC 2017 [3], prior to the start of this project, used a combination of NSIQ and GRO to achieve 6-bit quantization and two orders of noise-shaping in a CT-DSM, as shown in Figure 1. The proposed work achieved excellent performance (FoMSch =174dB) in a 0.13-µm process. Based on this multi-step time-based quantizer, we have proposed to use a 3-step 8-9 bit quantizer to be used in a high-speed CT-DSM.

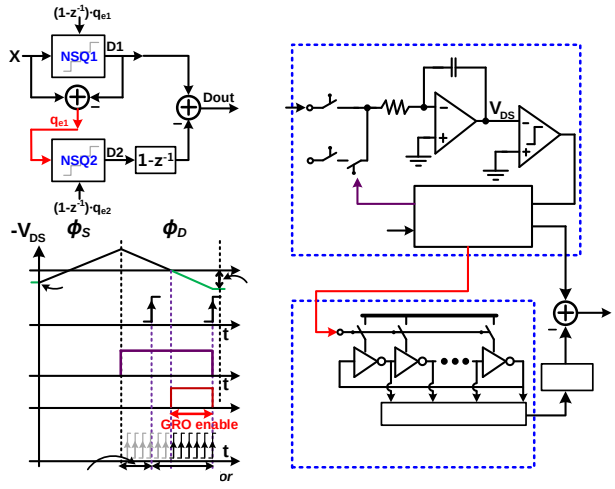

Figure 1. Double noise-shaped quantizer [3].

Providing a very large number of bits at the back-end of DSM allows reducing OSR substantially (<10), but raises the complexity of both Quantizer and the global DAC. The 3-step DNSQ shown in Figure 2 (a) using a flash as the first step, although simple, poses a critical challenge on the back-end global DAC and its matching requirements. That is, any mismatch between DAC1 and DAC2 will result in the leakage of the qe1 to appear at the output, unshaped.

To overcome this limitation, we propose a DAC-mismatch shaped 3-step quantizer, as shown in Figure 2(b). This architecture uses a VCO as the first step quantizer. Therefore, the extracted error will be a first order shaped quantization error. Here, the non-perfect cancellation of this error due to the DAC mismatch will contain a first order high pass shaped leakage, reducing the sensitivity to global DAC gain mismatch. We expect a tapeout in TMSC 65-nm in August 2017. The expected performance is shown in Table 1.

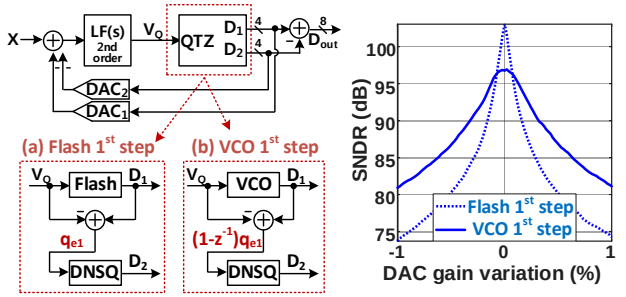

Figure 2. 3-step quantizer using (a) flash (b) VCO as the first step. Matlab simulation results of gain matching between DAC1 and DAC2.

Table 1. Expected performance merits.

Performance	fs	BW	SNDR	Power
Value	1GHz	50MHz	78dB	20mW

Keywords: delta-sigma, ADC, time-based, VCO, quantizer, mismatch shaping

INDUSTRY INTERACTIONS

Texas Instruments, Intel, NXP.

MAJOR PAPERS/PATENTS

[1] N. Maghari et al., "A third-order DT $\Sigma\Delta$ modulator using noise-shaped bi-directional single-slope quantizer," IEEE JSSC 2011.

[2] M. Straayer et al., "A 12-bit, 10-MHz bandwidth, continuous-time $\Sigma\Delta$ ADC with a 5-bit, 950-MS/s VCO-based quantizer," IEEE JSSC 2008.

[3] T. Kim et al., "A 11.4 mW 80.4 dB SNDR 15 MHz-BW CT Delta-Sigma Modulator Using 6-bit Double Noise-Shaped Quantizer," IEEE ISSCC 2017.

TASK 2712.015, AREA-EFFICIENT ON-CHIP SYSTEM-LEVEL IEC ESD PROTECTION FOR HIGH SPEED INTERFACE IC'S

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SIGNIFICANCE AND OBJECTIVES

Area-efficient, low-capacitance, on-chip system-level IEC ESD protection solutions for high-speed interface ICs will be designed, fabricated and characterized. Device physics for substrate parasitic PNP structure using p^+/n-well diodes will be modeled. Novel designs of IEC ESD structures will be provided for cost-effective system-level ESD protections on high-speed interface ICs.

TECHNICAL APPROACH

To reduce the total ESD device areas and reduce the parasitic capacitance, our approach is to utilize the inherent parasitic PNP structure in the high-side ESD diode as a parallel path to shunt the ESD discharge current. The key for this approach is to understand and adjust the characteristics of substrate PNP structures, such that the triggering and ESD clamping voltage of parasitic PNP structure is within the specific ESD protection window. Meanwhile, the clamping voltage of the primary ESD protection path needs to be higher than the triggering voltage of the parasitic PNP device.

SUMMARY OF RESULTS

To adjust the ESD performance of parasitic PNP, the ESD characteristics of the bipolar devices are studied to understand the relationship between device geometry and triggering/holding voltage.

For parasitic PNP using a p^+/n-well diode (as shown in Figure 1), there are several distance/spacing in the devices, which are expected to impact the ESD triggering voltage and holding voltage. The triggering voltage of the parasitic PNP is mainly determined by the avalanche breakdown between collector and base, which is due to an impact ionization process. The doping concentration of the collector and base region will strongly affect the triggering of the PNP. The holding voltage of parasitic PNP are decided by the current gain of the device and the avalanche multiplication factor (M). Eq. (1) shows the definition of M, which is affected by the breakdown voltage (V_B). The breakdown voltage is decided by the critical field (Eq. (2)). Eq. (3) defines the snapback behavior of BJT.

$$M = \frac{1}{1-\left(\frac{V}{V_B}\right)^n} \quad (1) \qquad V_B = \frac{\varepsilon_s \xi_{crit}^{\ 2}}{2qN} \quad (2) \qquad \alpha M = 1 + \frac{I_B}{I_E} \quad (3)$$

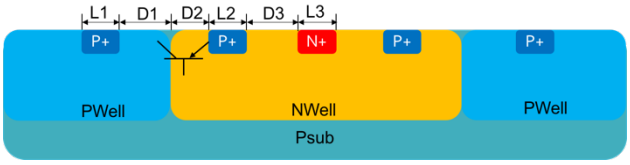

Figure 1. The device cross-section of parasitic PNP structure in the p^+/n-well ESD diode.

Figure 1 shows the critical distances or spacing in the design of the p^+/n-well diode. L1, L2 and L3 are the width of the n^+/p^+ diffusions. D1, D2 and D3 are the distance between the diffusions and Wells. From the Eq. (3), current gain of BJT will strongly affect the holding voltage. D2 and D3 are expected to impact the base resistance of the parasitic PNP structure. Therefore, the holding voltage of the PNP will be varied by these two parameters. L1 and D1 (emitter doping and efficiency) are also expected to change the ESD performance of the parasitic PNP. In addition to the baseline structure in Figure 1, more device designs are proposed.

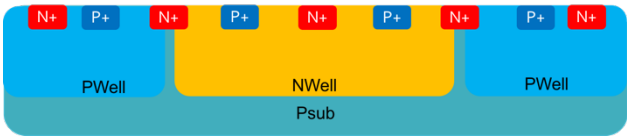

Figure 2. The device cross-section of proposed parasitic PNP structure in the p^+/n-well ESD diode.

Figure 2 shows the one of the proposed p^+/n-well ESD diodes with the separation of n and p-well, n^+ bridging and floating n^+ region to further adjust the triggering and holding voltage of the parasitic PNP structure.

To develop novel ESD protections with low capacitance and high failure current, device TCAD simulations are needed to understand the critical dimensions and their impacts to the ESD performance. For this purpose, TCAD simulations are planned in the next few months to understand the device structure. Silvaco TCAD workbench will be used to estimate the ESD performance of different diode layout styles prior to the tape-out.

Keywords: ESD, PNP, BJT, parasitic, IEC

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

TASK 2712.017, MITIGATING RELIABILITY ISSUES IN ANALOG CIRCUITS

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SIGNIFICANCE AND OBJECTIVES

Despite the growing interest in analog circuit reliability, very few experimental results have been reported on this issue. In an effort to gain a deeper understanding on fast degradation and recovery effects in analog circuits, we will design and fabricate several dedicated test chips including a SAR-ADC and bias generator, and study their reliability.

TECHNICAL APPROACH

Bias temperature instability (BTI) is a major reliability mechanism that can cause the transistor V_{TH} to degrade or recover within a few microseconds. When a voltage comparator circuit is exposed to two very different input voltages, the asymmetric BTI aging experienced by the two input transistors can lead to a time-dependent offset voltage. This issue can be detrimental to the linearity and resolution of SAR-ADC's even for a fresh chip [1]. In this work, we will design a test chip specifically to study the impact of BTI aging on SAR-ADC's under both short-term and long-term stress. The new chip will allow us to quantify the aforementioned instability issue for SAR-ADC's with different resolution and sampling rates.

SUMMARY OF RESULTS

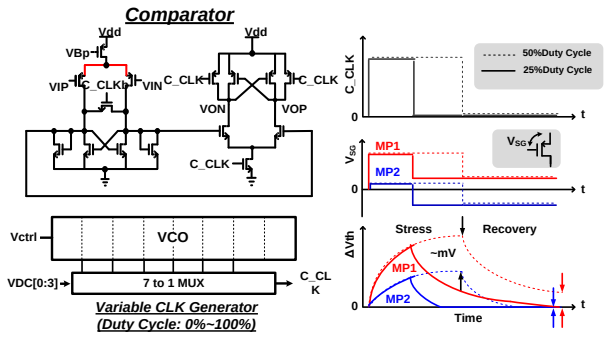

Figure 1. Variable duty-cycle clock generator for understanding fast BTI effects in comparator circuits.

First, we will experimentally study the effect of duty cycle on BTI effects in SAR-ADC. We expect a low duty-cycle clock to reduce BTI induced V_{TH} shift by virtue of a short stress time and a long recovery time. That is, the difference in V_{TH} shift in the comparator input pair transistors will reduce, as illustrated in Figure 1. A low duty-cycle clock will however have a negative impact on ADC performance. Furthermore, care must be taken to ensure that the narrow pulse width is sustained while the clock is propagating. In this work, we will carefully examine the pros and cons of using a variable duty-cycle clock by considering both the impact on BTI aging and ADC performance.

Second, we will study the impact of operating frequency on short-term BTI effects in SAR-ADC. The error caused by BTI is expected to be reduced at higher frequencies due to the shorter stress time. However, increasing the operating frequency may cause other errors due to insufficient settling time. The goal is to find the optimal operating frequency by characterizing ADC error versus frequency.

Third, a new in-situ INL/DNL measurement circuitry shown in Figure 2 will be implemented to pick up any subtle changes in ADC linearity. The circuit consists of decoders and a counter bank connected to the SAR-ADC output, and basically counts the number of times the ADC produces a particular output code. The counts are then scanned out for INL/DNL analyses. To further reduce the area of the large counter block, we propose a measurement method based on repetitive ramp-up and ramp-down tests. After repetitive voltage sweeps, we will stitch the partial distributions together to construct the full count distribution. This technique will provide a number of important benefits over traditional ADC measurement methods such as higher accuracy, lower noise, simpler test setup, and reduced test time.

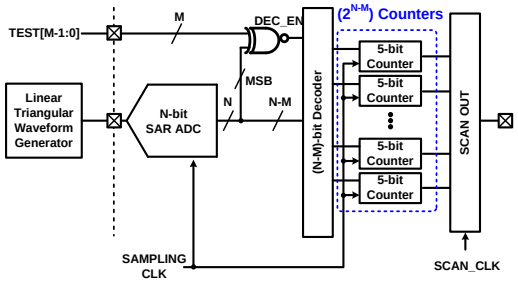

Figure 2. Proposed in-situ INL/DNL measurement circuit.

Lastly, based on the detailed measured data from the SAR-ADC test chip, we will evaluate circuit techniques for mitigating BTI effects in SAR-ADC. Two techniques will be considered: inducing recovery in the two input transistors but either turning off the input voltages or turning off the common pull up device in Fig. 1 (left).

Keywords: analog circuit reliability, BTI, SAR-ADC, variable duty-cycle, in-situ INL/DNL measurement

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] W. Choi, et al., CICC, Sep., 2015.

APPENDIX I PUBLICATIONS OF TXACE RESEARCHERS

Conference Publications

[1] Papadopoulou, A., Nikolić, B. (2017). A yield optimization methodology for mixed-signal circuits. *IEEE Custom Integrated Conference, Austin, TX, IEEE.*

[2] Kar, M., Singh, A., Rajan, A., De, V., Mukhopadhyay, S. (2016). An Integrated Inductive VR with a 250MHz All-Digital Multisampled Compensator and on-Chip Auto-Tuning of Coefficients in 130nm CMOS. *IEEE European Solid State Circuit Conference (ESSCIRC), Laussane, Switzerland*.

[3] Pinckney, N., Sylvester, D., Blaauw, D. (2016). Supply Boosting for High-Performance Processors in Flip-Chip Packages. *IEEE European Solid-State Circuits Conference, Lausanne, Swizterland, pp 4, IEEE*.

[4] Choo, K., Bell, J., Flynn, M. (2016). Area-efficient 1GSps 6b SAR ADC with Charge-Injection Cell Based DAC. *International Solid-State Circuits Conference (ISSCC), San Francisco, CA, IEEE*.

[5] Helal, Y., Neese, C. , De Lucia, F., Agarwal, A., Craver, B., Ewing, P., Stout, P., Armacost, M. (2016). Spectroscopic Measurement of Molecular Densities and Temperatures in Processing Plasmas. *AVS 63rd International Symposium & Exhibition, Nashville, TX*.

[6] O, K. K., Zhong, Q., Sharma, N., Choi, W., Schueler, R., Medvedev, I. R., Nam, H.-J., Raskin, P., De Lucia, F. C., McMillan, J. P., Neese, C. F., Lary, D., Kim, I. (2017). Demonstration of Breath Analyses Using CMOS Integrated Circuits for Rotational Spectroscopy. *International Workshop on Nanodevice Technology, Hiroshima, Japan*.

[7] Zhuang, Y., Chen, D. (2016). New Strategies in Removing Non-coherency from Signals with Large Distortion to Noise Ratios. *IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, Canada, pp 1-2, IEEE*.

[8] Zhuang, Z., Unnithan, A., Joseph, A., Sudani, S., Magstadt, B., Chen, D. (2016). Low Cost Ultra-Pure Sine Wave Generation with Self Calibration. *IEEE International Test Conference (ITC), Fort Worth, pp 1-9, IEEE*.

[9] Duan, Y., Chen, T., Chen, D. (2016). Low-cost Dithering Generator for Accurate ADC Linearity Test. *IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, Canada, pp 1-2, IEEE*.

[10] Duan, Y., Chen, D. (2017). Accurate Jitter Decomposition in High-Speed Links. *35th IEEE VLSI Test Symposium (VTS), Las Vegas, Nevada*.

[11] Liu, Z., Chaganti, S., Chen, D. (2016). Toward Complete Analog Fault Coverage with Minimal Observation Points Using a Fault Propagation Graph. *IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, Canada*, pp 1-2, IEEE.

[12] Liu, Z., Chaganti, S., Chen, D. (2016). Efficient Fault Coverage Assessment for Analog Circuit Test Evaluation with Graph-based Circuit Partition. *ART 2016: First IEEE International Workshop on Automotive Reliability & Test, Fort Worth, TX*.

[13] Chaganti, S. K., Xu, L., Chen, D. (2017). A Low-cost Method for Separation and Accurate Estimation of ADC Noise, Aperture Jitter, and Clock Jitter. *35th IEEE VLSI Test Symposium (VTS), Las Vegas, Nevada*.

[14] Lin, H., Li, P. (2016). Relevance vector and feature machine for statistical analog circuit characterization and built-in self-test optimization. *IEEE/ACM Design Automation Conference, Austin, TX*.

[15] Ahmadi, A., Nahar, A., Orr, B., Pas, M., Carulli, J., Makris, Y. (2016). Harnessing Fabrication Process Signature for Predicting Yield Across Designs. *International Symposium on Circuits & Systems (ISCAS), Montreal, Canada*.

[16] Ahmadi, A., Xanthopoulos, C., Nahar, A., Orr, B., Pas, M., Makris, Y. (2016). Harnessing Process Variations for Optimizing Wafer-Level Probe-Test Flow. *International Test Conference (ITC),*

Forth Worth, TX.

[17] Ahmadi, A., Bidmeshki, M., Nahar, A., Orr, B., Pas, M., Makris, Y. (2016). A Machine Learning Approach to Fab-of-Origin Attestation*. IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Austin, TX*.

[18] Sayed, M. and Al-Dhahir N. (2016). Differential Modulation Diversity Combining for Hybrid Narrowband-Powerline/Wireless Smart Grid Communications. *IEEE Global Conference on Signal and Information Processing (GlobalSIP), Washington, D.C*.

[19] Elgenedy, M., Sayed, M., El-Shafie, A., Kim, I. H. and Al-Dhahir, N. (2016). Cyclostationary Noise Modeling Based on Frequency-Shift Filtering in NB-PLC. *IEEE Global Communications Conference (Globecom), Washington, D.C*.

[20] Jamali, B., and Babakhani, A. (2016). Sub-picosecond Wireless Synchronization Based on a Millimeter-Wave Impulse Receiver with an On-chip Antenna in 0.13µm SiGe BiCMOS. *IEEE MTT-S International Microwave Symposium (IMS), San Francisco, CA*.

[21] Jamali, B., and Babakhani, A. (2017). A Fully Integrated Injection-Locked Picosecond Pulse Receiver for 0.29psrms-Jitter Wireless Clock Synchronization in 65nm CMOS. *IEEE MTT-S International Microwave Symposium (IMS), Honolulu, HI*.

[22] Keller, B., Cochet, M., Zimmer, B., Lee, Y, Blagojevic, M., Kwak, J., Puggelli, A., Bailey, S., Chiu, P. F., Dabbelt, D. P., Schmidt, C., Alon, E., Asanovic, K., Nikolic, B. (2016). Sub-microsecond adaptive voltage scaling in a 28nm FD-SOI processor SoC. *IEEE European Solid-State Circuits Conference, ESSCIRC'16, Lausanne, Switzerland*.

[23] Baniasadi, N., Niknejad, A. (2016). Jitter Analysis in Frequency-Interleaved ADCs. SRC *TechCon, Austin, TX*.

[24] Chen, C.–H., Zhang, Y., He, T., Temes, G. C. (2016). An incremental analog-to-digital converter with multi-step extended counting for sensor interfaces. *IEEE International Symposium on Circuits and systems (ISCAS), Montreal, Canada*.

[25] Cao, J., Temes, G. C. (2016). Power-on Digital Calibration Method for Delta-Sigma ADCs. *IEEE International Symposium on Circuits and systems (ISCAS), Montreal, Canada*.

[26] Chen, C.-H., Zhang, Y., Temes, G.C. (2016). History, present state-of-art and future of incremental ADCs. *IEEE European Solid-State Circuits Conference (ESSCIRC), Lausanne, Switzerland*.

[27] Zhang, Y., Chen, C.-H., He, T., Temes, G.C. (2016). A 35 uW 96.8 dB SNDR 1 kHz BW multi-step incremental ADC using multi-slope extended counting with a single integrator. *IEEE Symposium on VLSI Circuits, Honolulu, HI*.

[28] Lee, B., Song, M. K., Maity, A., & Ma, D. B. (2017). A 25MHz 4-Phase SAW Hysteretic DC-DC Converter with 1-Cycle APC Achieving 190ns tsettle to 4A Load Transient and Above 80% Efficiency in 96.7% of the Power Range. *IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA*.

[29] Nasir, S. B., Raychowdhury A. (2016). All-Digital Linear Regulators with Proactive and Reactive Gain-Boosting for Supply Droop Mitigation in Digital Load Circuits. *IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, Canada*.

[30] Nasir, S. B., Sen, S., Raychowdhury A. (2016). A 130nm Hybrid Low Dropout Regulator Based on Switched Mode Control for Digital Load Circuits. *IEEE European Solid-State Circuits Conference, Lausanne, Switzerland*.

[31] Gangopadhyay, S., Nasir, S., Subramanian, A., Sathe, V., Raychowdhury, A. (2016). A 32 nm Embedded, Fully-Digital, Phase-Locked Low Dropout Regulator for Fine Grained Power Management in Digital Circuit. *IEEE European Solid-State Circuits Conference, Lausanne, Switzerland*.

[32] Xiu, Y.; Farbiz, F.; Salman, A.; Zu, Y.; Dissegna, M.; Boselli, G.; Rosenbaum, E. (2016). Case study of DPI robustness of a MOS-SCR structure for automotive applications. *38th Annual EOS/ESD Symposium & Exhibits, Anaheim, CA*.

[33] Zafarani, M., Goktas, T., Akin, B. (2016). Analysis of Magnet Defect Faults in Permanent Magnet Synchronous Motors Through Fluxgate Sensor. *IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA,* pp. 2875-2880, IEEE.

[34] Qi, Y., Zafarani, M., Akin, B. (2016). A Diagnosis Procedure in Standalone Mode for Inter Turn Short Circuit Fault of PMSMs through Modified Self-Commissioning. *IEEE Energy Conversion Congress and Exposition, Milwaukee, WI*.

[35] Ahmad, Z., Choi, W., Sharma, N., Zhang, J., Zhong, Q., Kim, D.-Y., Chen, Z., Zhang, Y., Han, R., Shim, D., Sankaran, S., Seok, E.-Y., Cao, C., Mao, C., Schueler, R. M., Medvedev, I. R., Lary, D. J., Nam, H.-J., Raskin, P., DeLucia, F. C., McMillan, J. P., Neese, C. F., Kim, I., Momson, I., Yellswarapu, P., Dong, S., Kim, B.-K., O, K .K. (2016). Devices and Circuits in CMOS for THz Applications. *IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, pp. 734-737.*

[36] Zhong, Q., Choi, W., Sharma, N., Ahmad, Z., McMillan, J., Neese, C. F., De Lucia, F. C., O, K. K. (2016). 225-280 GHz Receiver for Rotational Spectroscopy. *IEEE Radio Frequency Integrated Circuits Symposium (RFIC), San Francisco, CA*, pp. 298-301.

[37] Ali, S. H., Dusmez, S., Akin, B. (2016). A comprehensive study on variations of discrete IGBT characteristics due to package degradation triggered by thermal stress. *IEEE Energy Conversion Congress and Exposition, Milwaukee, WI*, pp. 1-6.

[38] Ali, S. H., Dusmez, S., Akin, B. (2016). Investigation of collector emitter voltage characteristics in thermally stressed discrete IGBT devices. *IEEE Energy Conversion Congress and Exposition, Milwaukee, WI*, pp. 1-6.

[39] Heydarzadeh, M., Dusmez, S., Nourani, M., Akin, B. (2017). Bayesian Remaining Useful Lifetime Prediction of Thermally Aged Power FETs. *IEEE Applied Power Electronics Conference and Exposition, Tampa, FL*, pp. 1-6.

[40] Qaradagi, V., Mahdavi, M., Kumar, V., Pourkamali, S. (2016). Frequency output mems resonator on membrane pressure sensors. *IEEE Sensors, Orlando, FL*.

[41] Huang, H., Sarkar, S., Elies, B., Chiu, Y. (2017). A 12b 330MS/s pipelined-SAR ADC with PVT stabilized dynamic amplifier achieving <1dB SNDR variation. *International Solid-State Circuits Conference, San Francisco, CA*.

[42] Aflakian, N., Yang, N., LaFave Jr, T., Henderson, R., O, K. K., MacFarlane, D. (2016). Square holey cladding dielectric THz waveguides for chip-to-chip communication. *OSA, FiO/LS, Rochester, NY*.

[43] Aflakian, N., Yang, N., LaFave Jr, T., Henderson, R., O, K. K., MacFarlane, D. (2017). Square dielectric interconnect for chip-to-chip THz communication. *IEEE Texas Symposium on Wireless & Microwave Circuits & Systems, Waco, TX*.

[44] Aflakian, N., LaFave Jr, T., O, K. K., Ashrafi, S., MacFarlane, D. (2017). Fabrication and demonstration of vortex dielectric THz waveguide. *OSA Design Fabrication Conference, Denver, CO*, pp. 7123-7129, OSA Publishing.

[45] Munje, R., Graef E., Prasad, S. (2016). Interfacial impedance based electrochemical detection of carbon dioxide using RTIL. *IEEE Nanotechnology Materials and Devices Conferences (NMDC), Toulouse, France*.

[46] Muldrey B., Deyati S. and Chatterjee, A. (2017). Post-Silicon Validation: Automatic Characterization of RF Device Nonidealities via Iterative Learning Experiments on Hardware. *IEEE VLSI Design Conference, Hyderabad, India*, pp. 403-408.

[47] Muldrey B., Deyati S. and Chatterjee, A. (2016). DE-LOC: Design Validation and Debugging Under Limited Observation and Control, Pre- and Post-silicon for Mixed-Signal Systems. *IEEE International Test Conference, Fort Worth, TX*, pp. 1-10.

[48] Chaubey, S., Harjani, R. (2017). Fully Tunable Software Defined DC-DC Converter with 300X Output Current & 4X Output Voltage Range. *IEEE Custom Integrated Circuits Conference (CICC), Austin, TX*.

Journal Publications

[1] Kar, M., Ahmed, K. A., Mukhopadhyay, S. (2016). A Scalable Hybrid Regulator For Down Conversion of High Input Voltage Using Low-Voltage Devices. *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 1857-1862.

[2] Carlo, S., Mukhopadhyay, S. (2016). A High Power Density Dynamic Voltage Scaling Enabling a Single-Inductor Four-Output Regulator Using a Power-Weighted CCM Controller and a Floating Capacitor-Based Output Filter. *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4252-4264.

[3] Cai, S., Tabasy, E., Shafik, A., Kiran, S., Hoyos, S., Palermo, S. (2017). A 25GS/s 6b TI Two-Stage Multi-Bit Search ADC with Soft-Decision Selection Algorithm in 65nm CMOS. *IEEE Journal of Solid-State Circuits*, vol. 52, no. 8, pp. 2168-2179.

[4] Zhuang, Y., Magstadt, B., Chen, D. (2016). Accurate Spectral Testing with Impure Source and Non-coherent Sampling. *IEEE Transactions on Instrumentation and Measurement (TIM)*, vol. 65, no. 11, pp. 2454-2463.

[5] Zhuang, Y., Chen, D. (2016). New Strategies in Removing Non-coherency from Signals with Large Distortion to Noise Ratios. *IEEE Transactions on Circuits and Systems II (TCAS-II)*, vol. 63, no. 12, pp. 1136-1140.

[6] Zhuang, Y., Chen, D. (2017). ADC Spectral Testing with Signal Amplitude Drift and Simultaneous Non-coherent Sampling. *Journal of Electronic Testing: Theory and Applications (JETTA)*, vol. 33, no. 3, pp. 305-313.

[7] Zhuang, Y., Xu, L., Chen, D. (2017). Accurate Spectral Testing with Arbitrary Non-coherency in Sampling and Simultaneous Drifts in Amplitude and Frequency. *IEEE Transactions on Instrumentation and Measurement (TIM)*, vol. 66, no. 5, pp. 1002-1012.

[8] Zhuang, Y., Chen, D. (2017). Algorithms for Accurate Spectral Analysis in the Presence of Arbitrary Non-coherency and Large Distortion. *IEEE Transactions on Instrumentation and Measurement (TIM)*, vol. PP, no. 99, pp. 1-10.

[9] Zhuang, Y., Chen, D. (2017). Accurate Spectral Testing with Non-coherent Sampling for Multi Tone Applications. *IEEE Transactions on Circuits and Systems II (TCAS-II)*, vol. PP, no. 99, pp. 1-1.

[10] Mukherjee, P., Li, P. (2016). Using pre-silicon knowledge to excite non-linear failure modes in large mixed-signal circuits. *IEEE Design and Test*, vol. 33, no. 5, pp. 28-34.

[11] Lee, J., Kim, J. (2016). Efficient Global Optimization of Analog Circuits Using Predictive Response Surface Models on Discretized Design Space. *IEEE Design & Test*, vol. 33, no. 5, pp. 16-27.

[12] Sayed, M., Tsiftsis, T. A., and Al-Dhahir, N. (2017). On the Diversity of Hybrid Narrowband-PLC/Wireless Communications for Smart Grids. *IEEE Transactions on Wireless Communications*, vol. 16, no. 7, pp. 4344-4360.

[13] Aggrawal, H., Chen, P., Assefzadeh, M., Jamali, B., & Babakhani, A. (2016). Gone in a Picosecond: Techniques for the Generation and Detection of Picosecond Pulses and Their Applications. *IEEE Microwave Magazine*, vol. 17, no. 12, pp. 24-38.

[14] Kwak, J, Nikolic, B. (2016). A self-adjustable clock generator with wide dynamic range in 28nm FDSOI. *IEEE Journal of Solid-State Circuits*, vol. 51, no. 10, pp. 2368-2379.

[15] Keller, B., Cochet, M., Zimmer, B., Lee, Y, Blagojevic, M., Kwak, J.., Puggelli, A., Bailey, S., Chiu, P. F., Dabbelt, D. P., Schmidt, C., Alon, E., Asanovic, K., Nikolić, B. (2017). A RISC-V processor SoC with integrated power management at sub-microsecond timescales in 28nm FD-SOI. *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 52, no. 7, pp. 1863-1875.

[16] Zhang, Y., Chen, C.-H., He, T., Temes, G.C. (2017). A 16 b multi-step incremental Analog-to-Digital converter with single-opamp multi-slope extended counting. *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 52, no. 4, pp. 1066-1076.
[17] Nasir, S. B., Gangopadhyay S., Raychowdhury, A. (2016). All-Digital Low-Dropout Regulator with Adaptive Control and Reduced Dynamic Stability for Digital Load Circuits. *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8293-8302.
[18] Keel, M.-S., Rosenbaum, E. (2016). CDM-reliable T-coil techniques for a 25-Gb/s wireline receiver front-end. *IEEE Transactions on Device and Materials Reliability*, vol. 16, no. 4, pp. 513-520.
[19] Thomson, N., Xiu, Y., Rosenbaum, E. (2017). Soft-failures induced by system-level ESD. *IEEE Transactions on Device and Materials Reliability*, vol. 17, no. 1, pp. 90-98.
[20] Cong, L. and Lee, H. (2016). High-voltage high-frequency DC-DC converters with passive-saving two-phase QSW-ZVS technique. *Journal of Analog Integrated Circuits and Signal Processing*, vol. 88, no. 2, pp. 303-317.
[21] Xu, B., Zhou, Y., Chiu, Y. (2017). A 23-mW 24-GS/s 6-bit voltage-time hybrid time-interleaved ADC in 28-nm CMOS. *IEEE Journal of Solid-State Circuits*, vol. 52, no. 4, pp. 1091-1100.
[22] Goktas, T., Zafarani, M., Lee, K., Akin, B., Sculley, T. (2017). Comprehensive Analysis of Magnet Defect Fault Monitoring Through Leakage Flux. *IEEE Transaction on Magnetics*, vol. 53, no. 4, pp. 1-10.
[23] Zafarani, M., Goktas, T., Akin, B., Fedigan, S. (2017). An Investigation of Motor Topology Impacts on Magnet Defect Fault Signatures. *IEEE Transactions on Industrial Electronics*, vol. 64, no. 1, pp. 32-42.
[24] Patole, S., Torlak, M., Wang, D., & Ali, M. (2017). Automotive radars: A review of signal processing techniques. *IEEE Signal Processing Magazine*, vol. 34, no. 2, pp. 22-35.
[25] Dusmez, S., Ali,S. H., Heydarzadeh, M., Kamath, A. S., Duran, H. & Akin, B. (2017). Aging Precursor Identification and Lifetime Estimation for Thermally Aged Discrete Package Silicon Power Switches. *IEEE Transactions on Industry Applications*, vol. 53, no. 1, pp. 251-260.
[26] Huang, H., Du, L., Chiu, Y. (2017). A 1.2-GS/s 8-bit two-step SAR ADC in 65-nm CMOS with passive residue transfer. *IEEE Journal of Solid State-Circuits*, vol. 52, no. 6, pp. 1551-1562.
[27] Aflakian, N., Yang, N., LaFave Jr, T., Henderson, R., O, K. K., MacFarlane, D. (2016). Square dielectric THz waveguides. *Optics Express*, vol. 24, no. 13, pp. 14951-14959.
[28] Graef, E., Munje, R., Prasad, S. (2017). A Robust Electrochemical CO2 Sensor Utilizing Room Temperature Ionic Liquids. *IEEE Transactions Nanotechnology*, vol. PP, no. 99, pp. 1-1.

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