# TEXAS ANALOG CENTER OF EXCELLENCE

ERIK JONSSON SCHOOL OF ENGINEERING AND COMPUTER SCIENCE

# Annual Report 2020 – 2021

SRC®

TxACE TEXAS ANALOG CENTER OF EXCELLENCE

UT DALLAS The University of Texas at Dallas

# TxACE MISSION

The Texas Analog Center of Excellence seeks to create fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, health care, and public safety and security.

# TxACE THRUSTS

- *Safety, Security and Health Care*
- *Energy Efficiency*
- *Fundamental Analog Circuits*

# TxACE 2020–2021 ANNUAL REPORT

The Texas Analog Center of Excellence (TxACE), located at the University of Texas at Dallas is the largest analog research center based in an academic institution. Analog and mixed signal integrated circuits engineering is both a major opportunity and challenge. Analog circuitry is a critical component of the majority of products for the $400+ billion per year integrated circuits industry, as a part of sensing, actuation, communication, power management and others. Digital integrated circuits such as microprocessors, logic circuits and memories are now integrating analog functions such as input/output circuits, phase locked loops, temperature sensors and power management circuits. It is also common to find microcontrollers with multiple analog-to-digital and digital-to-analog converters. These circuitries impact almost all aspect of modern life: safety security, health care, transportation, energy, entertainment and others.

Creation of advanced analog and mixed signal circuits and systems depends on the availability of engineering talent for analog research and development. TxACE was established to help translate the opportunity into economic benefits by overcoming the challenge and meeting the need. TxACE was established through a collaboration of the state of Texas, Texas Instruments, the Semiconductor Research Corporation, the University of Texas System, and The University of Texas at Dallas.

The research tasks are organized into three research thrust areas: Safety, Security and Health Care, Energy Efficiency and Fundamental Analog. The scope of investigation extends from circuits operating at dc through terahertz, data converters that sample at a few samples/sec to 10's of Giga-samples/sec, AC-to-DC and DC-to-AC converters working at µW to Watts, energy harvesting circuits, sensors and many more. Significant improvements to existing mixed signal systems and new applications have been made and continued to be anticipated. Students who have been exposed to hands-on innovative research are forming the leading edge of analog talent flow into the industry. Close collaboration with and responsiveness to industry needs provide focus to the educational experience.

## DIRECTOR'S MESSAGE

The Texas Analog Center of Excellence (TxACE) is leading analog research and education. During this second year of COVID-19 pandemic, the Center has focused on executing its core mission, in turn is creating technologies that are helping our world better manage through this challenging time. We are privileged to be able to contribute toward this.

The Center funded 89 research tasks led by 74 principal investigators at 33 institutions, including three international universities. The Center supported 201 graduate and undergraduate students.

Over the past year, TxACE researchers published 30 journal and 41 conference papers. We also filed 5 patent applications and 4 invention disclosures and were granted 4 patents. 23 Ph.D. and 3 M.S. students have completed their degree program.

There are always too many research accomplishments to list all here. A selected list includes demonstration of an end-to-end key word spotting system that consumes 205~570nW power and scales with input rate due to use of a fully spike-event-driven classifier, discovery that the compressive biaxial stress common in most commercial packages increases intrinsic carrier concentration and electron mobility in npn transistors, both of which increase collector current, demonstration of an RC 100-MHz frequency reference fabricated in 65-nm CMOS achieving an inaccuracy of ±140ppm over -40 to 95$^{o}$C and 1µW/MHz power efficiency, and a domain-scalable run-time programmable integrated voltage regulator fabric using a single inductor multiple output (SIMO) buck converter for power-delivery and regulation.

The TxACE laboratory is continuing to help advance integrated circuit research by making its instruments and expertise available to researchers and our industrial partners all over the world.

I am happy to report that MediaTek has joined TxACE and SRC. I would like to thank UT Dallas, the University of Texas System, TI, and SRC, as well as many friends of TxACE all over the world for their generous support. Lastly, I would like to thank the students, principal investigators and staff for their efforts. I look forward to another year of working with the TxACE team to make our way of life better, safer and healthier through our research, education and innovation.

Most importantly, I wish everybody health and safety.

**Kenneth K. O, Director TxACE**
**Texas Instruments Distinguished**
**University Chair Professor**
**The University of Texas at Dallas**

## BACKGROUND & VISION

The $450+ billion per year integrated circuits industry is evolving into an analog/digital mixed signal industry. Analog circuits are providing or supporting critical functions such as sensing, actuation, communication, power management and others. These circuits impact almost all aspect of modern life including safety, security, health care, transportation, energy, and entertainment. To lead this change, in particular to lead analog and mixed signal technology education, research, commercialization, manufacturing, and job creation, the Texas Analog Center of Excellence was announced by Texas Governor Rick Perry in October 2008 as a collaboration of the Semiconductor Research Corporation, state of Texas through its Texas Emerging Technology Fund, Texas Instruments Inc., University of Texas system and University of Texas at Dallas. The Center seeks to accomplish the objectives by creating fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, healthcare, and public safety and security as well as by improving the research and educational infrastructure.

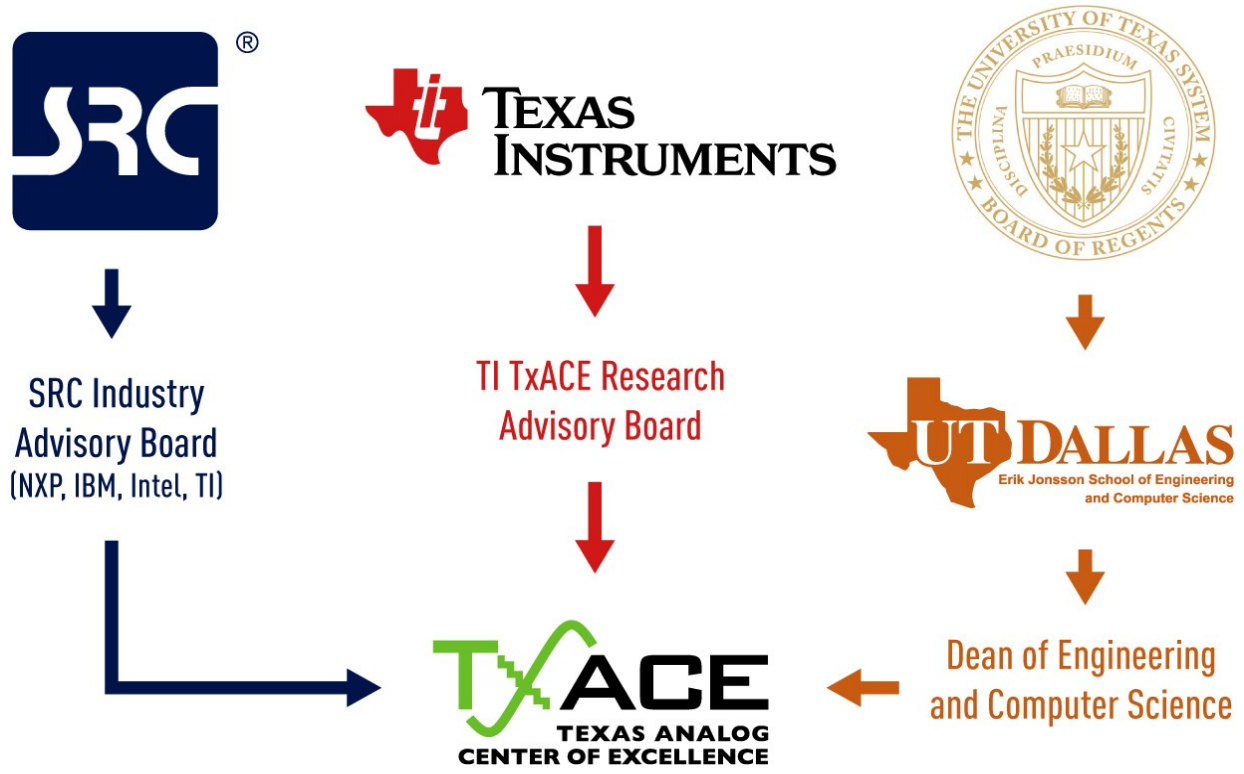



**Figure 1. TxACE organization relative to the sponsoring collaboration (2019-2020).**

## CENTER ORGANIZATION

The Texas Analog Center of Excellence is guided by agreements established with the Center sponsors. Members of the industrial advisory boards identify the research needs and select research tasks in consultation with the Center leadership. Figure 1 diagrams the relationship of TxACE to the members of the sponsoring collaboration.

*The internal organization of the Center is structured to flexibly perform the research mission while fully embracing the educational missions of the Universities.*

Figure 2 shows the center management structure. The TxACE Director is Professor Kenneth O. The research is arranged into three thrusts that comply with the center mission: Safety, Security and Health Care, Energy Efficiency and Fundamental Analog Research. The third thrust consists of vital research that cuts across the first two research thrusts. The thrust leaders are Prof. Yiorgos Makris of the University of Texas at Dallas for safety, security and health care, and Prof. Ali Niknejad of the University of California, Berkeley for energy efficiency. The leader for fundamental analog is Prof. Pavan Hanumolu of University of Illinois, Urbana-Champaign. The thrust leaders along with Professor Dongsheng Ma of the The University of Texas at Dallas form the executive committee. The committee, along with the director, forms the leadership team that works to improve the research productivity by increasing collaboration, better leveraging the diverse capabilities of principle investigators of the Center, and lowering research barriers. The leadership team also identifies new research opportunities for consideration by the Industrial Advisory Boards.

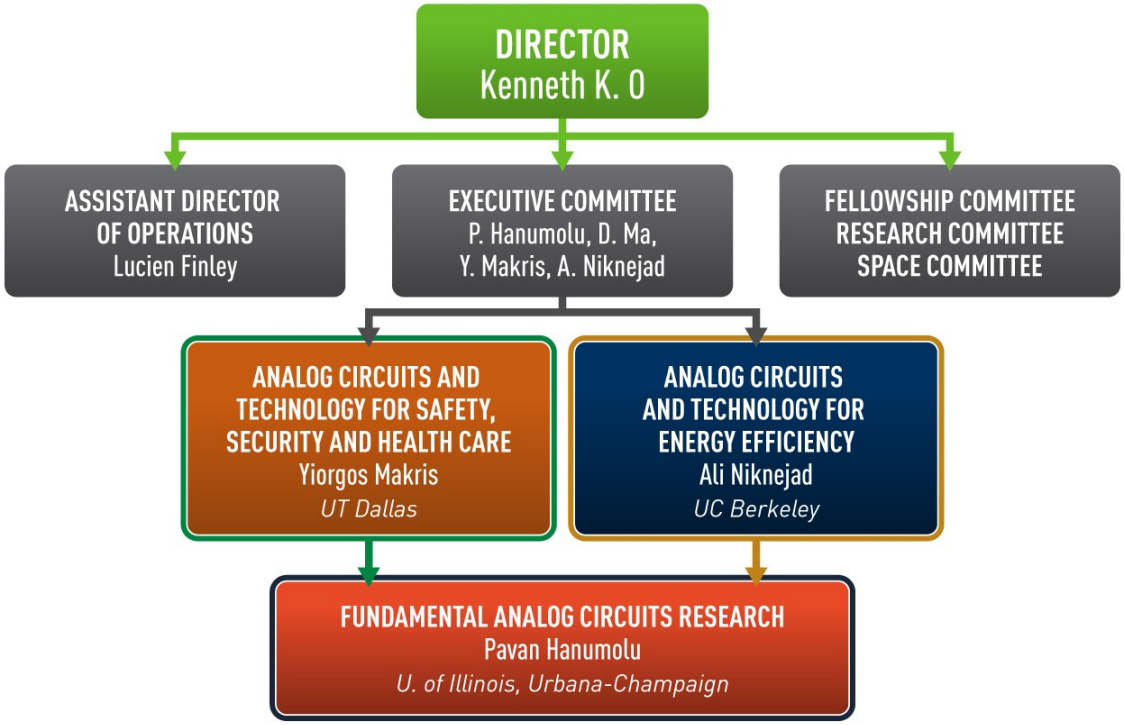



**Figure 2. TxACE organization for management of research**

## SAFETY, SECURITY & HEALTH CARE

(Thrust leader: Yiorgos Makris, University of Texas at Dallas)

The portfolio of TxACE research activities includes a broad range of analog technologies which seek to promote public safety and security, as well as to improve health care. Efforts in this thrust focus on improving safety by mitigating various reliability threats in analog/RF devices, including ESD, supply noise, temperature stress/strain and electro-migration, as well as by developing effective machine learning-based design, verification and self-test solutions. Particular emphasis has been placed on characterizing circuit aging, predicting failures and increasing lifetime of nano-scale CMOS circuits. This thrust also seeks to reduce the cost of millimeter wave imaging and on-vehicle radar technology for automotive safety by researching signal processing techniques that reduce system complexity and transmitter architecture that can efficiently adapt to changing antenna characteristics, as well as sensor fusion techniques that can enable monitoring behaviors of a driver in an automobile. Furthermore, this thrust is investigating methods for remote attestation of IoT edge devices, security aware dynamic power management and secure power IC design through EMI regulation. Additionally, this thrust includes research towards MEMS-based gas sensing, high-resolution TEM imaging-based reliability analysis of novel devices, as well as design of efficient temperature sensors for thermal performance characterization in power ICs.

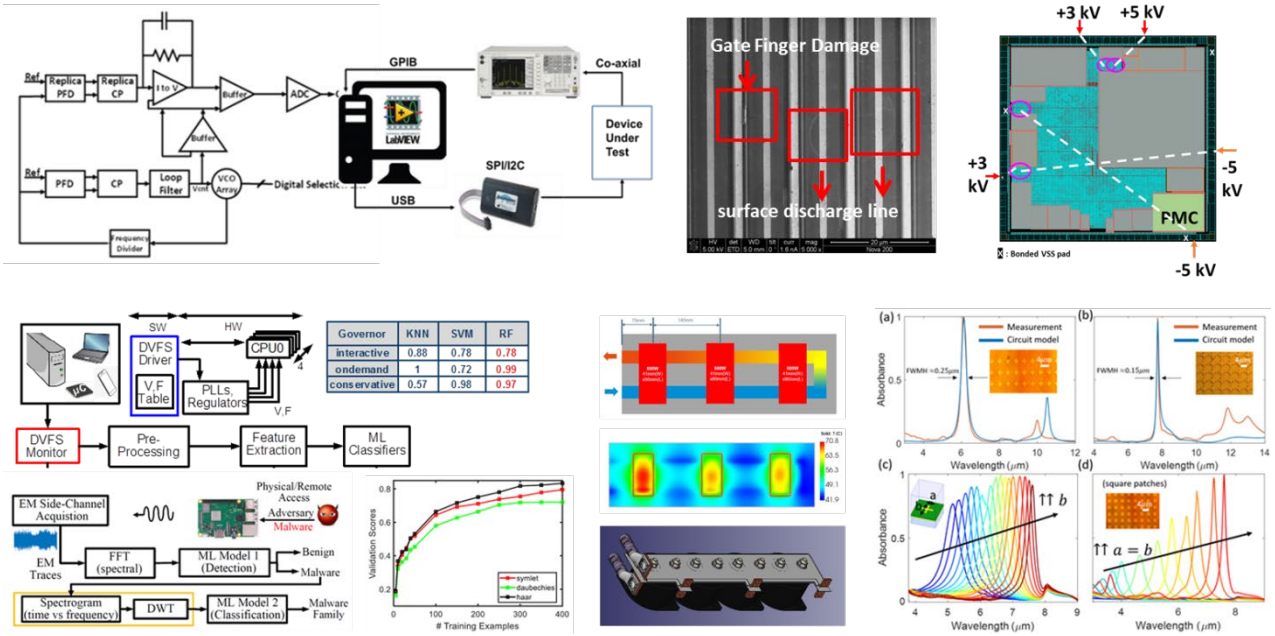



**Figure 3. (Top left) PLL incorporating 4.3-GHz VCO using programmable array of cross-coupled NMOS transistors for automated low phase noise calibration (K. K. O, University of Texas at Dallas), (Top center) Plan-view SEM images of gate finger damage with surface discharge lines (M. Kim, University of Texas at Dallas), (Top right) Powered ESD-caused latch-up in a commercial MCU, attributed to reverse body bias scheme used for power reduction. (E. Rosenbaum, University of Illinois Urbana Champaign), (Bottom left) Electromagnetic emission-based malware analysis (S. Mukhopadhyay, Georgia Institute of Technology), (Bottom center) Custom designed components for AC power cycling test setup (B. Akin, University of Texas at Dallas) (Bottom right) Experimental study of meta-surface IR absorbers for MEMS-based gas sensing (J. Sebastian Gomez Diaz, University of California, Davis).**

## ENERGY EFFICIENCY

(Thrust leader: Ali Niknejad, UC Berkeley)

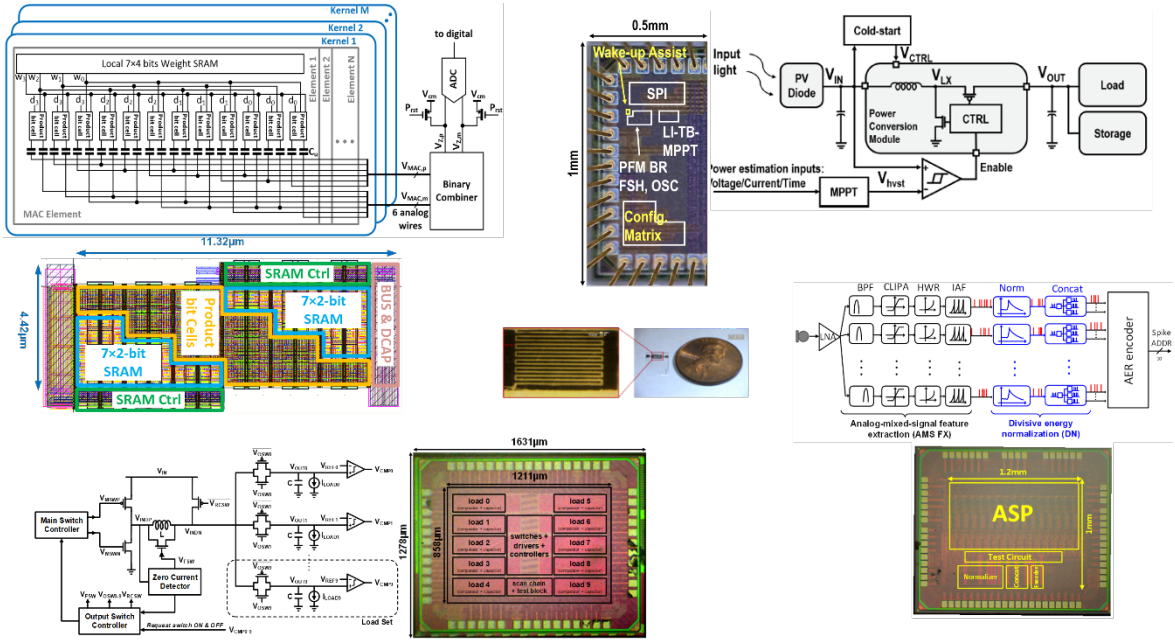



**Figure 4. The TxACE Energy Efficiency thrust has diverse tasks ranging from power management to analog mixed-signal AI, and devices and packaging solutions for the implementation of modern systems in increasingly smaller form factors.**

The TxACE Energy and Efficiency thrust is committed to tackling energy efficiency in electronic systems, spanning from traditional power management, all the way to the emerging fields of low power machine learning/AI for edge computing and applications to IoT sensor nodes. The power management research forms the foundation of the center and tackles important issues of efficiency in complex system applications, for example in digital multi-core systems that use single inductor multiple output (SIMO) DC-DC converters, addressing modeling and simulation and optimization of performance (voltage ripple, EMI) using non-linear control, mixed-signal techniques, digital signal processing, and adaptive algorithms. Tasks investigate non-conventional hybrid architectures and integration strategies for applications in computing, large-ratio conversion from 48V down to 1V and below, EV traction, and charging applications. Many of the solutions employ mixed-signal techniques, exploiting digital trends, and utilize novel scaling-friendly analog architectures to improve the control and expand the flexibility of the overall system.

## FUNDAMENTAL ANALOG CIRCUITS RESEARCH

(Thrust leader: Pavan Hanumolu, U. of Illinois Urbana-Champaign)

The research in this thrust focuses on cross-cutting areas in analog and mixed signal circuits which impact all of the TxACE application areas (Energy Efficiency, Public Safety, Security, and Health Care). The research includes the design of a wide variety of analog-to-digital converters, communication links, low-power crystal oscillators, I/O circuits, noise reduction techniques, new amplifier topologies suitable for use in nano-scale CMOS, development of CAD tools, and testing of integrated circuits.

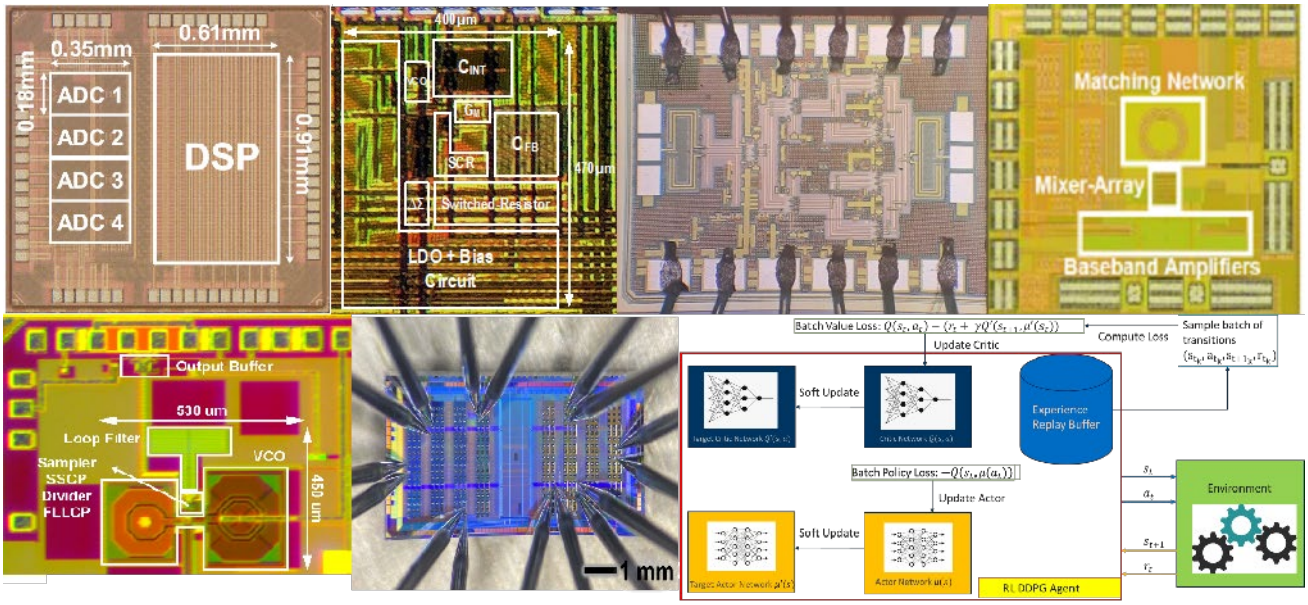



**Figure 5. (Top row: from left) Speech-recognition using adaptive beamforming and feature extraction (M. Flynn, University of Michigan), RC-based temperature compensated 100MHz frequency reference (P. Hanumolu, University of Illinois), 170 - 260 GHz wideband power amplifier (A. Babakhani, UCLA), PLL with post-fabrication phase noise reduction capability (K. O, UT Dallas) (Bottom row: from left) Low-jitter sub-sampling PLL (A. Niknehad, UC Berkeley), On-chip online learning circuit with STT-MRAM (J. Friedman, UT Dallas), Sample-efficient reinforcement learning approach for analog circuit optimization (P. Li, UCSB)**

## TXACE ANALOG RESEARCH FACILITY

The centralized group of laboratories of the Texas Analog Center of Excellence dedicated to analog engineering research and training occupy a ~ 8000-ft2 area on the 3rd floor of the Engineering and Computer Science North building (Figure 6). The facility includes RF and THz, Integrated System Design, Embedded Signal Processing, and Analog & Mixed Signal laboratories as well as CAD/Design laboratory structured to promote collaborative research**.** The unique instrumentation capability includes network analyses and linearity measurements up to 325 GHz, spectrum analysis up to 120 THz, and cryo-measurements down to 2$^{o}$K. The Center also added a pulsed multiple harmonic load and source pull measurement set up (up to 60 GHz for the third harmonic) and a 325-GHz antenna measurement set up. The close proximity of researchers in an open layout enables natural interaction and compels sharing of knowledge and instrumentation among the students and faculty. The TxACE analog research facility is one of the best equipped electronics laboratories. The laboratory is available for use by TxACE researchers and industrial partners all over the world.

**Figure 6. TxACE Analog Research Facility**

## RESEARCH PROJECTS AND INVESTIGATORS

The Texas Analog Center of Excellence (TxACE) is the largest university analog technology center in the world. Table 1 lists the current principal investigators of the 89 tasks from 33 academic institutions funded by TxACE. Four universities (SMU, Texas A&M, UT Austin, UT Dallas) are from the state of Texas. 29 are from outside of Texas. Three (Delft University of Technology, Indian Institute of Tech. Kharagpur, and University of Toronto) (Figure 7) are from outside of the US. Of the 74 investigators, 23 are from Texas. During the past year, the Center supported 167 Ph.D., 23 M.S., and 11 B.S. students. 23 Ph.D. and 3 M.S. degrees were awarded to the TxACE students.

| Investigator | Institution | Investigator | Institution | Investigator | Institution |
|---|---|---|---|---|---|
| B. Akin | UT/Dallas | J. Gu | Northwestern U. | N. Maghari | UT/Dallas |
| N. Al-Dhahir | UT/Dallas | P. Gui | SMU | K. Makinwa | Delft University |
| D. Allstot | UT/Dallas | A. Hanson | UT/Austin | Y. Makris | UT/Dallas |
| R. Ayyanar | Arizona State U. | P. Hanumolu | UIUC | Y. Mengüç | Oregon State U. |
| A. Babakhani | UC/Los Angeles | A. Hazra | Indian Institute of Tech. Kharagpur | P. Mercier | UC/San Diego |
| B. Bakkaloglu | Arizona State U. | R. Henderson | UT/Dallas | U. Moon | Oregon State U. |
| S. Bhunia | U. Florida | D. Heo | Washington State University | S. Mukhopadhyay | Georgia Tech. |
| D. Blaauw | U. Michigan | S. Hoyos | TEES | B. Murmann | Stanford U. |
| P. Blanche | U. Arizona | J. Hu | TEES | F. Najm | U. Toronto |
| C. Busso | UT/Dallas | M. Iyer | UT/Dallas | A. Niknejad | UC/Berkeley |
| A. Chatterjee | Georgia Tech. | M. Johnston | Oregon State U. | K. O | UT/Dallas |
| D. Chen | Iowa State U. | C. Kim | U. Minnesota | S. Ozev | Arizona State U. |
| Y. Chen | Duke U. | M. Kim | UT/Dallas | S. Palermo | TEES |
| Z. Chen | U. Arkansas, Fayetteville | H. Le | UC/San Diego | S. Pamarti | UC/Los Angeles |
| P. Dasgupta | Indian Institute of Tech. Kharagpur | G. Lee | UT/Dallas | P. Pande | Washington State U. |
| J. Doppa | Washington State University | H. Lee | UT/Dallas | G. Rincón-Mora | Georgia Tech. |
| W. Eisenstadt | U. Florida | M. Lee | UT/Dallas | R. Rohrer | SMU |
| M. Flynn | U. Michigan | P. Li | UC/Santa Barbara | E. Rosenbaum | UIUC |
| J. Friedman | UT/Dallas | J. Liu | UT/Dallas | A. Sanyal | U. at Buffalo |
| R. Geiger | Iowa State U. | H. Lu | UT/Dallas | V. Sathe | U. of Washington |
| S. Gómez-Díaz | UC/Davis | D. Ma | UT/Dallas | K. Sengupta | Princeton U. |

| Investigator | Institution | Investigator | Institution | Investigator | Institution |
|---|---|---|---|---|---|
| M. Seok | Columbia U. | D. Sylvester | U. Michigan | M. Torlak | UT/Dallas |
| H. Shichijo | UT/Dallas | Y. Takashima | U. Arizona | A. Trivedi | U. Illinois, Chicago |
| J. Stauth | Dartmouth College | G. Temes | Oregon State U. | X. Zhang | Washington U., St. Louis |
| M. Swaminathan | Georgia Tech. | S. Thompson | U. Florida | | |

**Table 1. Principal Investigators (May 2020 through April 2021)**

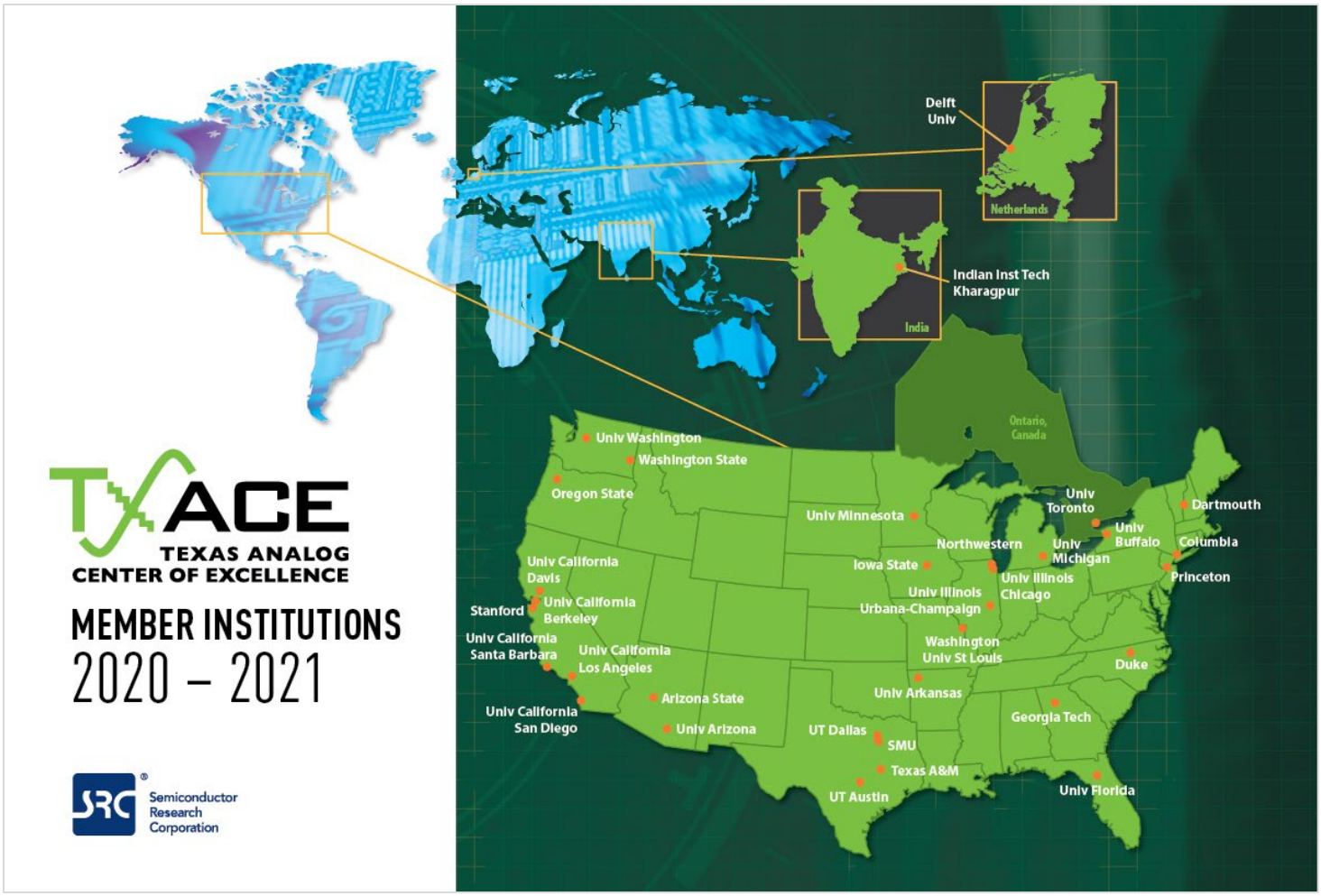



**Figure 7. Member Institutions of Texas Analog Center of Excellence**

## SUMMARY OF RESEARCH PROJECTS

The 89 research projects funded through TxACE during 2020-2021 are listed in Table 2 below by the Semiconductor Research Corporation task identification number.

| | Task | Thrust | Title | Task Leader | Institution |
|---|---|---|---|---|---|
| **1** | 2712.006 | EE | Robust, Efficient All-Digital SIMO Converters for Future SOC Domains | Sathe, Visvesh | University of Washington |
| **2** | 2712.011 | FA | Robust Reliable and Practical High Performance References in Advanced Technologies | Geiger, Randall<br>Chen, Degang | Iowa State University |
| **3** | 2712.012 | EE | EDAC and DCDC-Converter Co-Design for Addressing Robustness Challenges in Emerging Architectures | Seok, Mingoo | Columbia University |
| **4** | 2712.013 | SS | Reconfigurable MM-Wave Tx Architecture and Antenna Interface with Active Impedance Synthesis in Multi-Port Node-Conjugated Combiner | Sengupta, Kaushik | Princeton University |
| **5** | 2712.14 | FA | Leveraging CMOS Scaling in High Performance ADCS | Maghari, Nima | University of Florida |
| **6** | 2712.015 | SS | Area-Efficient On-Chip System-Level IEC ESD Protection for High Speed Interface ICs | Chen, Zhong | U. of Arkansas, Fayetteville |
| **7** | 2712.017 | SS | Mitigating Reliability Issues in Analog Circuits | Kim, Chris | U. of Minnesota |
| **8** | 2712.018 | SS/EE | Test Techniques to Approach Several Defect-per-billion for Power ICs | Eisenstadt, William | University of Florida |
| **9** | 2712.020 | EE | Low-Power Mostly Digital Time-Domain Delta-Sigma ADCs for IoT | Sanyal, Arindam | University at Buffalo |
| **10** | 2712.021 | SS | Distributed Silicon Circuits and Sensors in 3D-Printed Systems for Wearable IoT Sensors | Johnston, Matthew<br>Mengüç, Yiğit | Oregon State University |
| **11** | 2712.022 | SS | Intrinsic Identifiers for Database-Free Remote Authentication of IoT Edge Devices | Bhunia, Swarup<br>Trivedi, Amit | U. of Florida and U. Illinois, Chicago |
| **12** | 2712.024 | EE | A System-In-Package Platform for Energy Harvesting and Delivery for IoT Edge Devices | Mukhopadhyay, S.<br>Madhavan, S. | Georgia Tech. |

| | Task | Thrust | Title | Task Leader | Institution |
|---|---|---|---|---|---|
| **13** | 2712.025 | FA | Reduction of Low Frequency Noise Impact in Nano-Scale CMOS Circuits | O, Kenneth | UT/Dallas |
| **14** | 2712.026 | SS | Fault Characterization and Degradation Monitoring of SiC Devices | Akin, Bilal | UT/Dallas |
| **15** | 2712.027 | EE | Gate Driving Techniques and Circuits for Automotive-Use GaN Power Circuits | Ma, D. Brian | UT/Dallas |
| **16** | 2712.028 | EE | High Performance Micro-supercapacitor on a Chip Based on a Hierarchical Network of Nitrogen Doped Carbon Nanotube Sheets Supported MnO2 Nanoparticles | Lee, Gill | UT/Dallas |
| **17** | 2712.029 | SS | Novel Super-resolution and MIMO Techniques for Automotive and Emerging Radar Applications | Torlak, Murat | UT/Dallas |
| **18** | 2712.031 | FA | Adaptive Trimming and Testing of Analog/RF Integrated Circuits (ICs) | Makris, Yiorgos | UT/Dallas |
| **19** | 2810.002 | SS/EE | Security-Aware Dynamic Power Management for System-on-Chips | Mukhopadhyay, Saibal | Georgia Tech. |
| **20** | 2810.003 | EE | Integrated Voltage Regulator Management for System-on-Chip Architectures | Zhang, Xuan | Washington University |
| **21** | 2810.005 | FA/SS | Circuit Design for ESD and Supply Noise Mitigation | Rosenbaum, Elyse | UIUC |
| **22** | 2810.006 | EE | Combating Unprecedented Efficiency, Noise and Frequency Challenges in Modern High Current Integrated Power Converters | Ma, D. Brian | UT/Dallas |
| **23** | 2810.007 | FA | Fully Integrated Phase Noise Cancellation Techniques | Niknejad, Ali | UC/Berkeley |
| **24** | 2810.008 | EE | Circuit Techniques for Fast Start-Up of Crystal Oscillators | Pamarti, Sudhakar | UCLA |
| **25** | 2810.009 | EE/FA | Mixed-Signal Building Blocks for Ultra-low Power Wireless Sensor Nodes | Sylvester, Dennis Blaauw, David | U. of Michigan |
| **26** | 2810.010 | EE | GS/s ADC Based Cycle-to-Cycle Closed-Loop Adaptive Smart Driver for High-Performance SiC/GaN Power Devices | Gui, Ping | SMU |

| | Task | Thrust | Title | Task Leader | Institution |
|---|---|---|---|---|---|
| **27** | 2810.011 | EE | Micro-Power Analog-to-Digital Data Converters for Sensor Interfaces | Temes, Gabor | Oregon State University |
| **28** | 2810.012 | EE | NPSense - Nano-Power Current Sensing | Makinwa, Kofi | Delft University |
| **29** | 2810.013 | FA | Frequency-Domain ADC-Based Serial Link Receiver Architectures for 100+Gb/s Serial Links | Palermo, Samuel<br>Hoyos, Sebastian | TEES |
| **30** | 2810.014 | SS | Deep Learning Solutions for ADAS: From Algorithms to Real-World Driving Evaluations | Busso, Carlos<br>Al-Dhahir, Naofal | UT/Dallas |
| **31** | 2810.015 | FA | Demonstration of 120-Gbps Dielectric Waveguide Communication Using Frequency Division Multiplexing (FDM) and Polarization Division Multiplexing (PDM) | O, Kenneth | UT/Dallas |
| **32** | 2810.016 | SS | Condition Monitoring of Industrial/Automotive Drive Components through Leakage Flux | Akin, Bilal | UT/Dallas |
| **33** | 2810.017 | SS | Reliability Study of E-mode GaN HEMT Devices | Kim, Moon<br>Shichijo, Hishashi | UT/Dallas |
| **34** | 2810.018 | FA | Transition Design for High Data Rate Links at Submillimeter Wave Frequencies | Henderson, Rashaunda | UT/Dallas |
| **35** | 2810.019 | FA | Design Automation for Coverage Management in Analog and Mixed-Signal SOCs | Dasgupta, Pallab<br>Hazra, Aritra | Indian Institute of Tech. Kharagpur |
| **36** | 2810.020 | FA | Analog/Mixed-Signal RF Circuit Time Domain Sensitivity and Its Applications | Rohrer, Ronald | SMU |
| **37** | 2810.021 | SS | A Collaborative Machine Learning Approach to Fast and High-Fidelity Design Prediction | Hu, Jiang<br>Chen, Yiran | TEES and Duke University |
| **38** | 2810.022 | SS | A Collaborative Machine Learning Approach to Fast and High-Fidelity Design Prediction | Chen, Yiran<br>Hu, Jiang | Duke University And TEES |
| **39** | 2810.023 | SS | Machine Learning Driven Automatic Mixed-Signal Design Verification-Validation for Automotive Applications | Chatterjee, Abhijit | Georgia Tech. |
| **40** | 2810.025 | SS | Machine Learning-Based Layout Analysis and Netlist Optimization for Defect Tolerance and Design Robustness to Process Imperfections and Variations | Makris, Yiorgos | UT/Dallas |

| | Task | Thrust | Title | Task Leader | Institution |
|---|---|---|---|---|---|
| **41** | 2810.027 | SS | Measurement and Modeling of Stress/Strain on Analog Transistor and Circuit Parameters | Thompson, Scott | University of Florida |
| **42** | 2810.028 | FA | Robust ATE Multi-Site HW Design to Enable Effective Analog Performance Testing in Analog-Mixed-Signal (AMS) SoCs | Chen, Degang | Iowa State University |
| **43** | 2810.029 | FA | 170GHz – 260GHz Wideband PA and LNA Design in Silicon | Babakhani, Aydin | UCLA |
| **44** | 2810.030 | FA | Neural Network Recognition & On-Chip Online Learning with STT-MRAM | Friedman, Joseph | UT/Dallas |
| **45** | 2810.031 | FA | Development and Asssessment of Machine Learning Based Analog and Mixed-Signal Verification | Li, Peng | UC/Santa Barbara |
| **46** | 2810.032 | EE | DRIVR: A Digital, Re-configurable, Unified Clock-Power (UniCaP) Fabric for Energy-Efficient SoCs | Sathe, Visvesh | University of Washington |
| **47** | 2810.033 | FA | Interleaved Noise-Shaping SAR ADCs for High-Speed and High-Resolution | Flynn, Michael | U. of Michigan |
| **48** | 2810.034 | EE | Always-on Keyword Spotting based on Analog-Mixed-Signal Computing Hardware | Seok, Mingoo | Columbia University |
| **49** | 2810.035 | EE | Computationally Controlled Integrated Voltage Regulators | Sathe, Visvesh | University of Washington |
| **50** | 2810.036 | FA | Highly Stable Integrated Frequency References | Hanumolu, Pavan | UIUC |
| **51** | 2810.037 | FA | High-performance Ringamp-based ADCs | Moon, Un-Ku | Oregon State University |
| **52** | 2810.038 | SS | Extreme Temperature Digital, Analog, and Mixed-Signal Circuits (ET-DAMS) | Kim, Chris | U. of Minnesota |
| **53** | 2810.039 | EE | Development of Compact and Low Cost Fully Integrated DC-DC Converter with Resonant Gate Drive and Intelligent Transient Response | Gu, Jie | Northwestern University |
| **54** | 2810.040 | EE | Hybrid/Resonant Sc Converters with Integrated Lc Resonator for High-Density Monolithic Power Delivery | Stauth, Jason | Dartmouth College |

| | Task | Thrust | Title | Task Leader | Institution |
|---|---|---|---|---|---|
| **55** | 2810.041 | SS | ESD Protection for IO Operating at 56 Gb/s and Beyond | Rosenbaum, Elyse | UIUC |
| **56** | 2810.042 | EE | Digitally Enhanced High Efficiency, Fast Settling Augmented DCDC Converters | Bakkaloglu, Bertan | Arizona State University |
| **57** | 2810.043 | FA | Analog Optimization Hybridizing Designer's Intent and Machine Learning | Li, Peng | UC/Santa Barbara |
| **58** | 2810.044 | FA | Hierarchical Characterization and Calibration of RF/Analog Circuits Using Lightweight Built-in Sensors | Ozev, Sule | Arizona State University |
| **59** | 2810.046 | SS | Generating Current Constraints for Electromigration Safety | Najm, Farid | University of Toronto |
| **60** | 2810.047 | SS | Architecture and DfT methods for improving life time reliability and functional safety of electronic circuits and systems out of application context | Chen, Degang | Iowa State University |
| **61** | 2810.048 | SS | Characterization and Mitigation of Electromigration Effects in Advanced Technology Nodes | Kim, Chris | U. of Minnesota |
| **62** | 2810.049 | EE | 1-W Battery-Charging CMOS Buck Regulator | Rincón-Mora, Gabriel | Georgia Tech. |
| **63** | 2810.050 | SS | Integrating Metasurfaces and MEMS for Gas Sensing | Gómez-Díaz, Sebastian | UC Davis |
| **64** | 2810.051 | SS/EE | High Gain DC-DC Converter for EV Traction System | Ayyanar, Raja | Arizona State University |
| **65** | 2810.052 | FA | TI PLM as Hologram Generator for HUD (Head Up Display) and AR | Blanche, Pierre | University of Arizona |
| **66** | 2810.053 | FA | TI PLM to Advanced Lidar and Display Systems | Takashima, Yuzuru | University of Arizona |
| **67** | 2810.054 | SS | Reconfigurable AC Power Cycling Setup and Plug-in Condition Monitoring Tools for High Power IGBT and SiC Modules | Akin, Bilal | UT/Dallas |
| **68** | 2810.055 | SS/EE | EMI-Regulated Secure Automotive Power ICs | Ma, D. Brian | UT/Dallas |

| | Task | Thrust | Title | Task Leader | Institution |
|---|---|---|---|---|---|
| **69** | 2810.056 | FA | Millimeter Wave Packaging Research - Antenna in Package | Iyer, Devan | UT/Dallas |
| **70** | 2810.057 | SS | Reliability Study of E-mode GaN HEMT Devices by AC TDDB and High Resolution TEM | Kim, Moon<br>Shichijo, Hishashi | UT/Dallas |
| **71** | 2810.058 | SS/FA | Machine Learning-Based Overkill/Underkill Reduction in Analog/RF IC Testing | Makris, Yiorgos | UT/Dallas |
| **72** | 2810.060 | FA | Intelligent, Learning ADCs for the Post Figure-of-Merit World | Flynn, Michael | U. of Michigan |
| **73** | 2810.061 | EE | Two-Stage Vertical Power Delivery and Management for Efficient High-Performance Computing | Le, Hanh-Phuc<br>Mercier, Patrick | UC/San Diego |
| **74** | 2810.062 | FA | Multi-Carrier DAC-Based Transmitter Architectures for 100+Gb/s Serial Links | Palermo, Samuel<br>Hoyos, Sebastian | TEES |
| **75** | 2810.063 | FA | Analog and Digital Assist Techniques to Improve Mixed-Signal Performance | Sylvester, Dennis<br>Blaauw, David | U. of Michigan |
| **76** | 2810.064 | SS | Characterization and Tolerance of Ageing in Integrated Voltage Regulators | Mukhopadhyay, Saibal | Georgia Tech |
| **77** | 2810.065 | EE/SS | Power-Efficient and Reliable 48-V DC-DC Converter with Direct Signal-to-Feature Extraction and DNN-Assisted Multi-Input Multiple-Output Feedback Control | Seok, Mingoo | Columbia University |
| **78** | 2810.066 | SS | Demonstrably Generalizable Compact Models of ESD Devices | Rosenbaum, Elyse | UIUC |
| **79** | 2810.067 | EE | Highly Efficient Extreme-Conversion-Ratio Buck Hybrid Converters | Pande, Partha<br>Heo, Deuk<br>Doppa, Jana | Washington State University |
| **80** | 2810.068 | EE | Active EMI Filtering with Switch-Mode Amplifier for High Efficiency | Hanson, Alex | UT Austin |
| **81** | 2810.070 | SS | Early and Late Life Failure Prediction Methods for Analog and Mixed-Signal Circuits | Kim, Chris | U. of Minnesota |

| | Task | Thrust | Title | Task Leader | Institution |
|---|---|---|---|---|---|
| **82** | 2810.071 | FA | Accurate Compact Temperature Sensors for Thermal Management of High Performance Computing Platforms | Geiger, Randall<br>Chen, Degang | Iowa State University |
| **83** | 2810.072 | EE | AI/ML Edge Hardware for Ultra-reliable Wireless Networks | Allstot, David | Oregon State University |
| **84** | 2810.073 | EE | AI/ML Edge Hardware for Ultra-reliable Wireless Networks | Makris, Yiorgos | UT/Dallas |
| **85** | 2810.074 | SS | Thermal Performance Characterization and Degradation Monitoring of LDMOS based Integrated Power IC with On-Die Temperature Sensors | Akin, Bilal | UT/Dallas |
| **86** | 2810.075 | EE | Hybrid Step-Down DC-DC Converters with Large Conversion Ratios for 48V Automotive Applications | Lee, Hoi<br>Liu, Jin | UT/Dallas |
| **87** | 2810.076 | FA | High Precision Positioning Techniques Based on Multiple Technologies and Frequency Bands | Al-Dhahir, Naofal<br>Torlak, Murat | UT/Dallas |
| **88** | 2810.077 | SS | Increasing Lifetime of Nano-Scale CMOS Circuits | O, Kenneth | UT/Dallas |
| **89** | 2810.078 | EE | Programmable Mixed-Signal Accelerator for DNNs with Depthwise Separable Convolution Layers | Murmann, Boris | Stanford University |

**Table 2: Funded research projects at TxACE by SRC task identification number (FA: Fundamental Analog, EE: Energy Efficiency, SS: Safety, Security and Health Care)**

# ACCOMPLISHMENTS

In the past year, TxACE has made significant research progress. Table 3 summarizes the number of publications and inventions resulting from the TxACE research during May 2020 to April 2021, while Table 4 lists the major research accomplishments for the Center during the period. The TxACE researchers have published 41 conference papers and 30 journal papers. They have also made 4 invention disclosure, filed 5 patent applications, and were granted 4 patents. The list of publications is included as Appendix I. Following the tabulation, brief summaries of each project are provided.

**Table 3. TxACE number of publications (May 2020 through April 2021)**

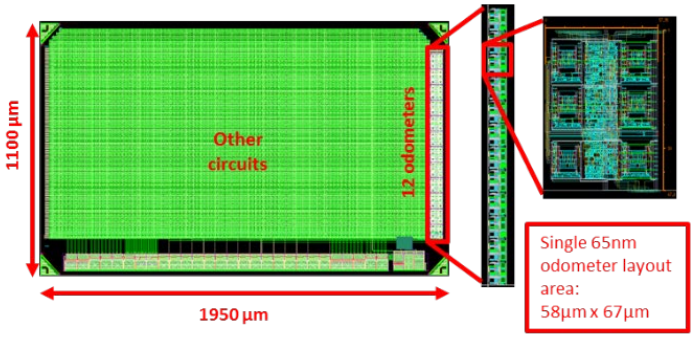
| Conference Papers | Journal Papers | Invention Disclosures | Patents Filed | Patents Granted |
|---|---|---|---|---|
| 41 | 30 | 4 | 5 | 4 |

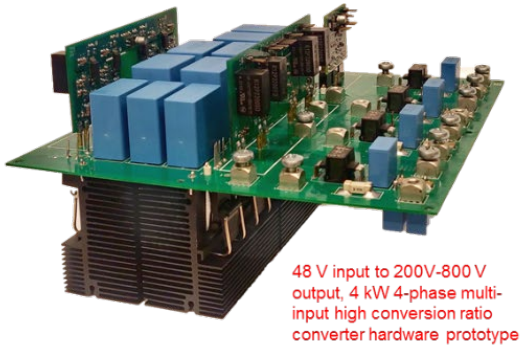
**Table 4. Major TxACE Research Accomplishments (May 2020 through April 2021)**

| Category | Accomplishment |
|---|---|
| Energy Efficiency (Circuits) | A ±2A fully-integrated current sensor with a 20-mΩ on-chip shunt (resistor) has been demonstrated. It uses an energy-efficient hybrid sigma-delta ADC with an FIR-DAC and consumes only 1.4 µA, a 3× improvement on the state-of-the-art. A tunable analog temperature-compensation scheme allows ±2A currents to be digitized with 0.35% gain error from −40 to 85 ° C. A gain error of about 0.6% for ±15A currents was achieved with a 3-mΩ PCB shunt. The sensor occupies 1.6 $mm^2$ in 180-nm CMOS. (2810.012, K. Makinwa, TU Delft) |
| Energy Efficiency (Circuits) | A Single Inductor Multiple Output (SIMO) regulated SoC in 65-nm CMOS demonstrated two techniques that mitigate the prohibitive voltage droop and ripple margin problems of SIMO regulated domains. The first extends the Unified Clock and Power (UniCaP) adaptive clocking architecture to multiple domains and achieves 98% average voltage margin reduction. The second introduces Dynamic Droop Allocation, which concurrently analyzes charge delivery requirements and equalizes droop across all domains to reduce worst-case transient droop by 73%. (2810.032, V. Sathe, U. Washington) |
| Energy Efficiency (Circuits) | Always-on keyword spotting (KWS) is essential for a voice-based user interface in mobile and edge devices. This project uses the hybridization of analog-mixed-signal and digital hardware and demonstrated a sub-600nW KWS system with environmental noise and process variation robustness. The system incorporates a 5-layer spiking neural network (SNN) classifier having 650 neurons and 67,000 synapses fabricated in 65-nm CMOS. The SNN hardware demonstrates 7 to 1000X reduced power consumption. (2810.034, M. Seok, Columbia) |
| Fundamental Analog (Circuits) | A compact, low-power microphone-to-spectrogram beamforming frontend processor for speech recognition is demonstrated by bit-stream processing of the outputs generated by an array of sigma-delta modulators that digitize microphone outputs. The prototype beamformer fabricated in a 40-nm CMOS process occupies an active area of 0.89$mm^2$ and improves speech recognition accuracy in noisy conditions from 64% to 90%. (2810.060, M. Flynn, U. Michigan) |

| | |
|---|---|
| Fundamental Analog (Circuits) | High accuracy RC oscillator-based frequency reference is demonstrated by precise and robust cancellation of the resistor temperature coefficient (TC) across the process. Using a parallel combination of switched-resistors that are digitally controlled by temperature-compensating pulse-density modulated sequences, the output frequency's first- and second-order TCs are suppressed. A prototype 100MHz frequency reference fabricated in a 65-nm CMOS process achieved an inaccuracy of 140ppm, 80ppm/V voltage sensitivity, 2.5ppm Allan deviation, and 1μW/MHz power efficiency. (2810.036, P. Hanumolu, UIUC) |
| Safety, Security and Health Care (CADT) | Packaging of electronic devices introduces compressive biaxial stress and variable vertical stress due to silicon particles in the epoxy. The compressive biaxial stress (a common type in most commercial packages) increases intrinsic carrier concentration and electron mobility in npn transistors, both of which increases collector current. Tensile stress reduces the packaging effect to the collector current of npn transistors. (2810.027, S. Thomson, U. of Florida) |

# Safety, Security and Health Care Thrust




| Category | Accomplishment |
|---|---|
| Safety, Security and Health Care (Systems) | The goal of this project is to demonstrate miniaturized infrared (IR) gas sensors ($CO_2$, NO, $NO_2$, Ethylene ..) operating at room temperature based on ultrathin meta-surfaces (MTSs) integrated within a nano-mechanical resonator system (NMEMS). The first set of meta-surfaces based on gold nano-resonators deposited on 200nm of $SiO_2$ provides almost 100% absorption at the desired wavelength with an FWHM≈0.25µm or Q of ~20. The meta-surfaces will be integrated with NMEMS resonators to demonstrate a complete gas sensing system. (2810.050, S. Gómez-Díaz, UC Davis) |
| Safety, Security and Health Care (CADT) | Packaging of electronic devices introduces compressive biaxial stress and variable vertical stress due to silicon particles in the epoxy. The compressive biaxial stress (a common type in most commercial packages) increases intrinsic carrier concentration and electron mobility in npn transistors, both of which increase collector current. Tensile stress reduces the packaging effect to the collector current of npn transistors. (2810.027, S. Thomson, U. of Florida) |
| Safety, Security and Health Care Energy Efficiency (Circuits) | A high gain, wide output voltage range multi-input high gain DC-DC converter with low voltage and current stress semiconductor devices has been developed. Multiple low voltage battery packs are employed in cell balancing due to independent charging-discharging of each battery module and increased safety for EV traction system. The proposed concept has been verified through a hardware prototype attaining a peak efficiency of 98.3 % at 48 V input to 400 V output at 2 kW. (2810.051, R. Ayyanar, Arizona State University) |

# TASK 2712.013, RECONFIGURABLE MM-WAVE TX ARCHITECTURE AND ANTENNA INTERFACE WITH ACTIVE IMPEDANCE SYNTHESIS IN MULTI-PORT NODE-CONJUGATED COMBINER

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## SIGNIFICANCE AND OBJECTIVES

In this project, we demonstrated a generalized multi-port approach for 1) Broadband VSWR-reconfigurable PA architecture with a multi-port DAC based topology (VLSI'19, TMTT Apr'20), 2) first mm-Wave Load Modulated Balanced Amplifier (LMBA) that aims broadband and back-off efficiency in the 5G bands (IMS'2020 **Best student paper 2nd prize,** TMTT paper in prep., patent filed).

## TECHNICAL APPROACH

We proposed a generalized method of load pulling to overcome VSWR in a reconfigurable fashion between 26-40 GHz. For the LMBA, we presented the first mmWave load modulated balanced PA architecture with adaptive biasing for enhanced linearity.

## SUMMARY OF RESULTS

We demonstrated the first mm-Wave load-balanced PA with a transformer-based hybrid at input and output to allow wideband power combining and achieve high isolation with PA control for load-modulation and back-off efficiency enhancement across 30-40 GHz.

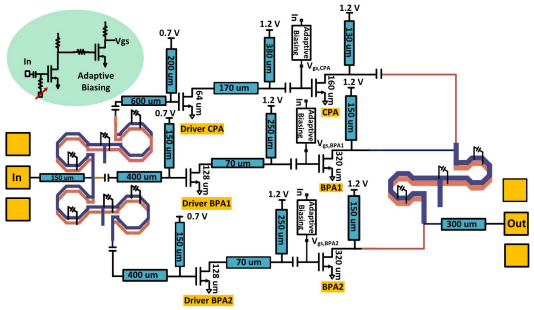


**Figure 1. Schematic of the broadband VSWR-tolerant PA architecture in 65-nm CMOS operating across 26-40 GHz.**

To overcome the compressive behavior of an LMBA and enhance linearity, an integrated adaptive biasing is integrated on-chip allowing superior ACLR performance across 30-40 GHz (Fig. 1). Under CW excitation, the two-stage LMBA demonstrates output power of 18.5-20 dBm, output drain efficiency >30% across 30-40 GHz (Fig. 2). The modulation capabilities of LMBA are tested using a 64 QAM signal with a data rate of 6Gbps wherein PA demonstrates EVM of -26.4 dB and ACLR of -29 dBc at an average output power of 10.6 dBm (Fig. 2).

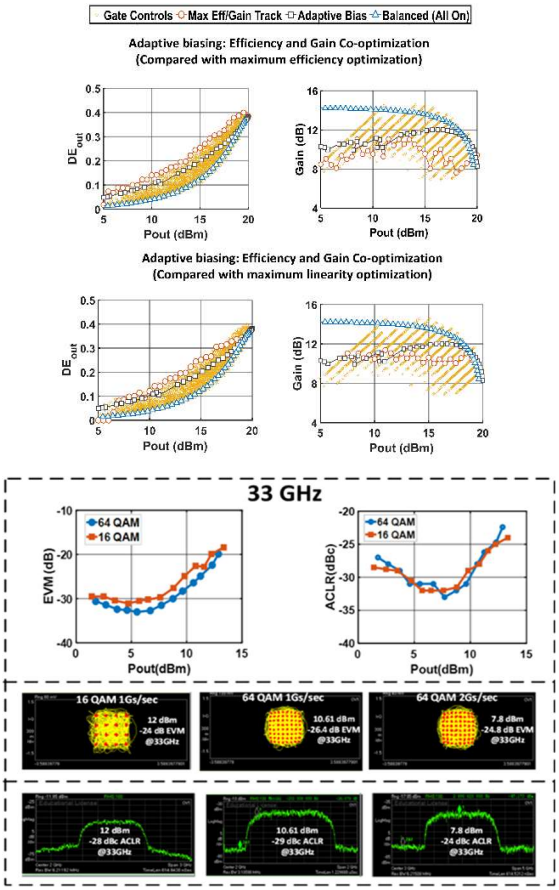


**Figure 2. Linearity measurements of LMBA across 30-40 GHz along with drive ups at 33,36 and 40 GHz. EVM and ACLR vs average output power for a 16/64 QAM signal at 33 GHz. 16QAM and 64QAM constellations and spectra.**

Spectrally-agile transmitters between 30-100 GHz should be investigated.

**Keywords:** mmWave, PA, load modulation, 5G

## INDUSTRY INTERACTIONS

Texas Instruments, Intel, NXP

## MAJOR PAPERS/PATENTS

[1] C.R.Chappidi, T.Sharma, Z.Lu, and K.Sengupta, "Load Modulated Balanced mm-Wave CMOS PA with Integrated Linearity Enhancement for 5G applications," *IMS 2020 (Best student paper 2nd prize).*

[2] Kaushik Sengupta and Chandrakanth Chappidi, "Load modulated balanced mm-Wave PA architecture," provisional patent filed.

# TASK 2712.015, AREA-EFFICIENT ON-CHIP SYSTEM-LEVEL IEC ESD PROTECTION FOR HIGH SPEED INTERFACE ICS

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## SIGNIFICANCE AND OBJECTIVES

Area-efficient, low-capacitance, on-chip system-level IEC ESD protection solutions for high-speed interface ICs will be designed, fabricated, characterized, and optimized based on the dual-diode ESD protection structure.

## TECHNICAL APPROACH

To reduce the total ESD device areas and the parasitic capacitance, our approach is to utilize the inherent parasitic PNP structure in the high-side ESD diode as a parallel path to shunt the ESD discharge current. The key for this approach is to adjust the characteristics of substrate PNP structures by optimizing the layout such that the triggering and ESD clamping voltage of the parasitic PNP structure is within the specific ESD protection window.

## SUMMARY OF RESULTS

Various ESD protection diodes with finger-type and island-type layouts were fabricated in a UMC65-nm process and characterized to compare the ESD behaviors (e.g., current carrying efficiency, parasitic capacitance, and leakage current). The leakage current and parasitic capacitance of both island-type and finger-type diodes are small such that they can be used for the high-speed applications. The island-type layout design can achieve higher failure current through the inherent parasitic PNP structure compared to the finger-type counterpart with the same area. The high-level metal routing helps reduce the total parasitic capacitance of ESD diodes.

The proposed ESD diode with the optimized parasitic PNP structure is connected with external "forward diodes" as the primary ESD cell (shown in Figure 1). This test structure of ESD protection path is used to demonstrate the improved ESD performance with optimized ESD diode. Three TLP (Transmission-Line Pulse) measurements were carried out in sequence: (1) Individual Path 1 represents the "high-side forward diode + primary ESD cell"; (2) individual lateral parasitic PNP (labeled "Path 3") with base floating; (3) Path 1 and Path 3 (in-parallel) configuration. Figure 1 also presents the TLP I-V characterization results. Using 5 forward biased diodes in series with a 62Ω resistor as a primary ESD cell, it shows that $V_{t1}$ of Path 1 and Path 3 is 5V and 11V, respectively. When the optimized ESD path (i.e., "High-side diode + Parasitic PNP+ Primary ESD Cell" configuration) turns on under the ESD event, the point ② in Fig. 1 indicates the turn-on of the lateral parasitic PNP (Path 3) which is around 11V, and it dominates over vertical PNP (Path 2) to help shunt current in parallel with Path 1. It verifies the operation of our proposed ESD cell with optimized parasitic PNP.

Moreover, the displacement current induced by the parasitic capacitance on the power supply or the current injected by the primary ESD cell may affect the ESD behavior of the inherent parasitic substrate PNP during power-on condition. Three comparison groups (a. the direction of the injected current, b. the location of the current injection point, and c. the level of injected current) were designed and tested to evaluate the effects.

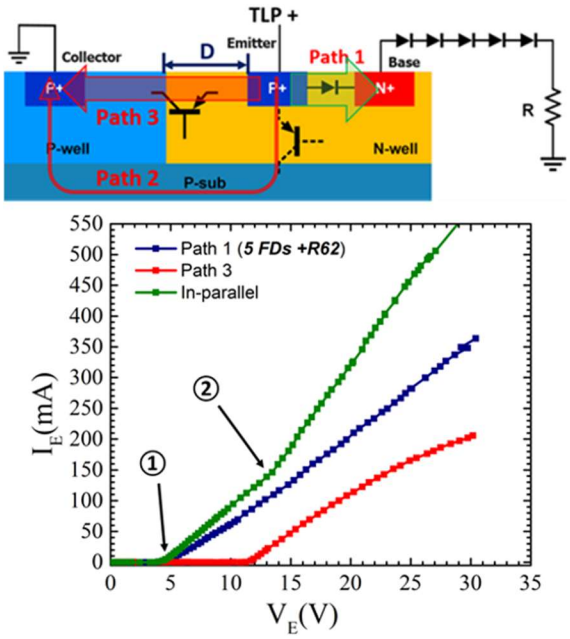


**Figure 1. The testing configuration of the proposed P+/N-well diode connected with external "forwards" as primary ESD cell for the demonstration and TLP characterization results.**

**Keywords:** ESD, PNP, IEC, TCAD, Current injection

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] H. Wang, et al, "Area-efficient Dual-diode with Optimized Parasitic Bipolar Structure for Rail-based ESD Protections", Microelectronics Reliability, in press.
[2] Z. Chen, M. Ali, and H. Wang., "ESD Self-protection of Output Circuitry Using Substrate Bipolar Structure," provisional patent filed.

# TASK 2712.017, MITIGATING RELIABILITY ISSUES IN ANALOG CIRCUITS

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## SIGNIFICANCE AND OBJECTIVES

An on-chip analog waveform sampling system was demonstrated in a 65-nm process focusing on extreme temperature step response measurements. Amplifier output waveforms were measured under different temperatures ranging from -40 degrees Celsius ambient temperature to 300 degrees Celsius heater temperature.

## TECHNICAL APPROACH

We demonstrated a fully integrated measurement system for characterizing analog signal waveforms at extremely high temperatures. We employed the sub-sampling technique, where the signal level of a repetitive high-speed analog signal is detected by sweeping a known reference voltage until the signal level is reached. The voltage sweep measurement is repeated while incrementing the time offset between the triggering clock and the sampling clock to reconstruct the full waveform. To raise the local circuit temperature without damaging the package and test board, we integrated a metal heater with serpentine wires above the circuit under test.

## SUMMARY OF RESULTS

Fig. 1 shows the operating principle of the sub-sampling technique used in this work. For a repetitive analog signal, we obtained the sweep voltage versus occurrence curve at each sampling time. If sweep voltage is below the analog signal voltage, then the occurrence is low, and vice versa. The 50% point represents the sampled voltage. The occurrence curve is recorded while incrementing the sampling time offset until the time window of interest is measured. The occurrence curves are stitched together to recreate the analog waveform.

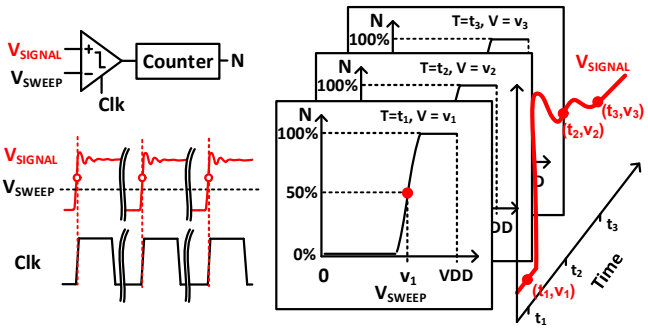


**Figure 1. On-chip sub-sampling of repetitive analog signals and waveform reconstruction method.**

Fig. 2 shows the 65-nm test chip die photo and testing environment. Fig. 3 shows the characterization results of 8 amplifiers from the same chip at 1.3V. The input step voltage is switched from 0.4V to 0.9V. The 1.3V supply voltage used in the experiments is 100mV higher than the nominal voltage to allow more headroom during voltage overshoot events. We can see that the overshoot decreases slightly until 125°C but degrades significantly at 300°C. The slew rate increases with temperature at first but decreases for a heater temperature of 300°C and an ambient temperature of 120°C, likely due to the threshold voltage reduction being dominant compared to the mobility degradation. The settling time is generally longer below 0°C compared with room temperature and 300°C cases.

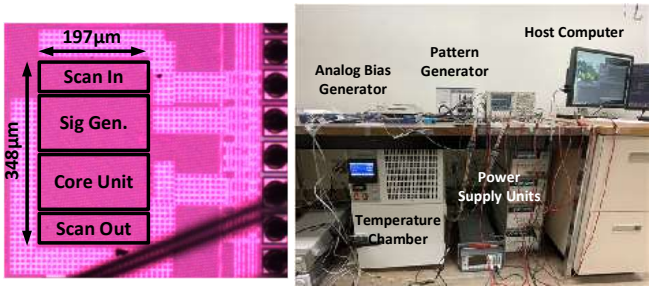


**Figure 2. 65-nm test chip die photo and testing setup.**

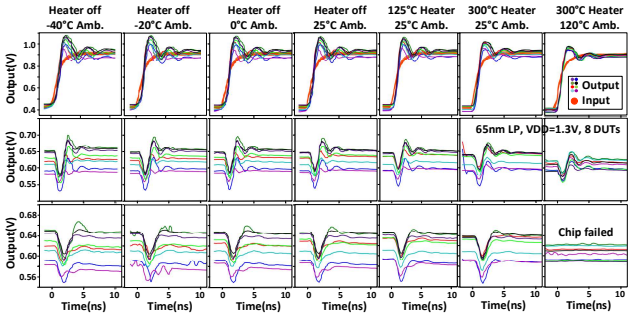


**Figure 3. Device characterization array schematic.**

**Keywords:** High temperature, amplifier response, on-chip heater, analog reliability, sub-sampling technique

## INDUSTRY INTERACTIONS

Texas Instruments, Intel

## MAJOR PAPERS/PATENTS

[1] H. Yu, G. Park, and C.H. Kim, "Extreme Temperature Characterization of Amplifier Response Up to 300 Degrees Celsius Using Integrated Heaters and On-Chip Samplers", ESSCIRC, 2021 (to appear)

# TASK 2712.018, TEST TECHNIQUES TO APPROACH SEVERAL DEFECT-PER-BILLION FOR POWER ICS

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## SIGNIFICANCE AND OBJECTIVES

This work designed, simulated, and tested custom LDO and Buck Converter power ICs using additional bare-die test points to improve part failure rates. The goal was to test yield enhancement by culling power ICs with outlier subcircuit performance. Recent work characterized small-signal LDO control loop gain using IC external pins.

## TECHNICAL APPROACH

Researchers developed simulations of power ICs with internal IC test features for enhanced testing. These were used to determine subcircuit performance inside of 65-nm CMOS LDOs and Buck Converters. Analyses and simulations of custom-designed LDO and Buck converters were performed to prove these new test concepts. A 65-nm CMOS LDO test IC and a Buck converter test IC were fabricated and tested. The functional LDO IC was used to characterize on-chip power IC control loop gain and phase response and develop fast methods to do this on the ATE.

## SUMMARY OF RESULTS

For the final six months of this project, TI proposed the new goal of devising a method of quickly testing existing LDO's. The prior work was limited to the observation of the LDO IC with advanced test features and external control loop components. Modern LDO's use internal compensation techniques with Miller capacitors or cascode capacitors to provide LDO control compensation.

In this work, researchers focused on analyzing a generic Miller compensated LDO IC design with good simulated line regulation, load regulation, PSSR, and a unity gain frequency of 2.2 MHz with a phase margin of -67°. Cascode compensated LDOs yield similar results. The generic Miller compensated LDO was placed in a Servo-loop test as shown in Figure 1. This configuration can be easily realized on the load board and used during ATE test.

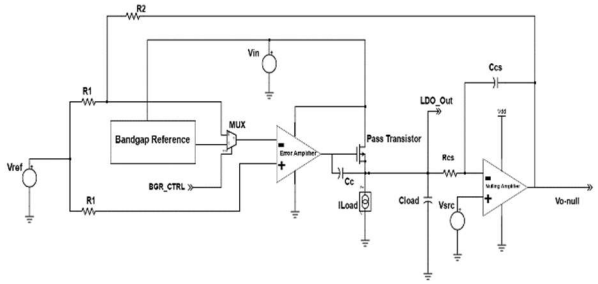


**Figure 1. A Generic Miller Compensated LDO inside a servo-loop for test simulations.**

Servo-loop test simulations were performed. The servo-loop measurement simulations of DC gain were compared with the extracted DC gain from the Cadence Spectre software using stability analysis. The simulations agreed closely. The Miller capacitor compensated LDO showed an inverse linear control-loop cutoff variation with the Miller capacitor value (proportional to 1/Cc).

A goal of this year's work was to test the LDO frequency response in 20mS. The Servo-loop test can characterize the gain bandwidth curve using three frequency points and be used to extrapolate loop cutoff frequency and loop capacitance. Figure 2 shows simulations of generic Miller compensated LDO control-loop bandwidth versus compensation capacitor value. A nominal compensation capacitor of 20 pF yields a control loop bandwidth of 2.2 MHz. If the compensation capacitor is lowered to 15pF then the loop bandwidth is 2.6 MHz and if the compensation capacitor value is raised 25pF the loop bandwidth is 1.9 MHz. So, one could determine a bad on-chip compensation capacitor value by injecting three signals into the servo-loop, 20% above the nominal cutoff, at the cutoff frequency, and 20% below the LDO cutoff frequency and measuring the loop gain.

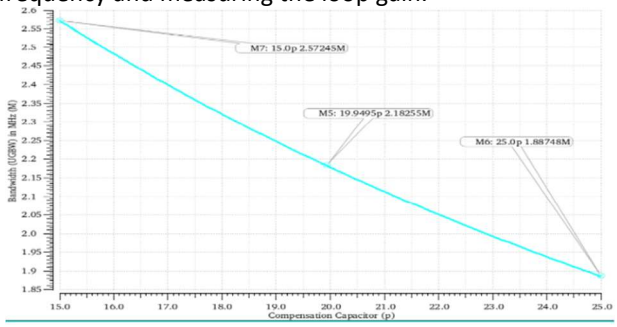


**Figure 2. Simulations of Generic Miller Compensated LDO inside a test servo-loop.**

Integrating a compensated servo-loop for a small signal test on chip is feasible. An integrated servo-loop would require a small area of the LDO chip compared to the other LDO subcircuits.

**Keywords:** Test, Analog, Power, LDO, Buck Converter

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] Anurag Tulsiram and William R. Eisenstadt, "Design for Testability of Low Dropout Regulators," IEEE VLSI Test Symposium 2021, April 26-28, 2021, Virtual Interactive Live Event.

# TASK 2712.021, DISTRIBUTED SILICON CIRCUITS AND SENSORS IN 3D-PRINTED SYSTEMS FOR WEARABLE IOT SENSORS

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YIĞIT MENGÜÇ, OREGON STATE UNIVERSITY

## SIGNIFICANCE AND OBJECTIVES

There is an emerging set of applications that require stretchable, compliant electronics – including wearable devices, instrumented fabrics, and soft robots with distributed sensors and computation. In this project, we are working to demonstrate a fundamentally new method for the fabrication of stretchable, 3D-printed objects containing distributed sensors and silicon ICs.

## TECHNICAL APPROACH

Developing stretchable electronics faces two primary challenges: integration of active semiconductor devices in elastic substrates and providing stretchable, conductive interconnects. In this project, we combine 3D printing of liquid metal materials and silicone rubber with PCB fabrication techniques to build solid 3D objects with electronic components distributed throughout. Silicon integrated circuits, used for computation, sensing, and actuation, will be connected through liquid metal conductors confined to 3D microfluidic channels. Through additive, layer-by-layer construction, electronic devices can be inserted and connected throughout the 3D structure. We will also develop compact models for the interconnects, which will be used to design adaptable front-end circuits for stretchable interconnect interfaces.

## SUMMARY OF RESULTS

For this project, we have demonstrated progress (Fig. 1) in printing multi-layer stretchable circuits using discrete components, extended strain testing of liquid metal paste material, and developed a compact modeling framework for stretchable interconnects. Specific outcomes have included:

- Demonstrated printing of sensors and analog and digital interconnects using discrete active and passive components [1,2].
- Extended testing of stretchable interconnects, demonstrating <5% change in resistance over 100,000 stretch cycles at 50% strain (1.5X) [4].
- Compact modeling framework for Cadence-compatible simulation of stretchable interconnects under static and dynamic strain conditions [3].
- Printed antenna structures for future integration into stretchable circuits with wireless communication.
- Developed both 3D-printing and stencil-based fabrication methods for stretchable circuits [5, 6].

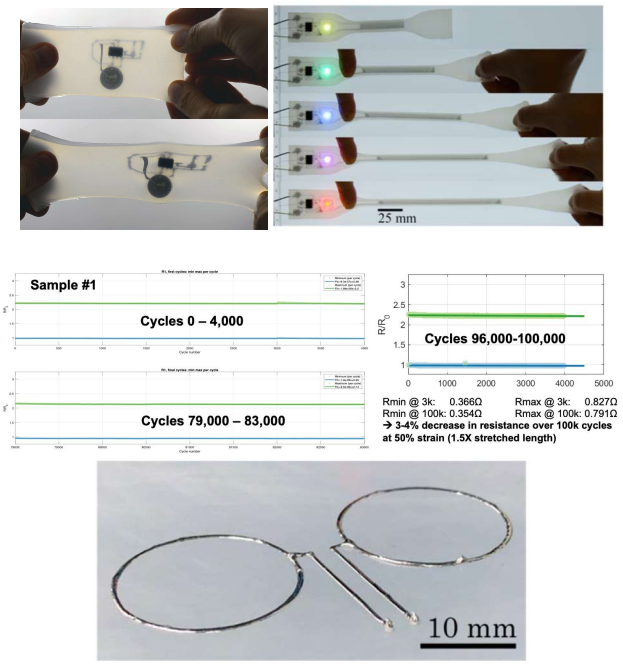


**Figure 1. Printed stretchable circuits (top) with active and passive components [1]; 100,000 cycle strain data (middle); printed stretchable devices such as antennas (bottom) are also feasible using the liquid metal paste materials and methods.**

**Keywords:** Stretchable electronics, 3D printing, wearable devices, packaging, sensor interfaces

## INDUSTRY INTERACTIONS

Texas Instruments, Intel, IBM

## MAJOR PAPERS/PATENTS

[1] C. Votzke, U. Daalkhaijav, Y. Mengüç, and M.L. Johnston, "3D-printed liquid metal interconnects for stretchable electronics," *IEEE Sensors Journal*, vol. 19, no. 10, pp. 3832 - 3840, 2019.

[2] C. Votzke et al., "Highly-stretchable biomechanical strain sensor using printed liquid metal paste," *IEEE BioCAS,* 2018.

[3] K. Clocker et al., "Compact modeling of stretchable printed liquid metal electrical…," *IEEE FLEPS,* 2019.

[4] C. Votzke et al., "Electrical characterization of stretchable printed liquid metal interconnects under repeated cyclic loading," *IEEE FLEPS,* 2019.

[5] C. Votzke et al., "Stenciled liquid metal paste for robust stretchable electrical interconnects," *IEEE FLEPS,* 2021.

[6] C. Votzke, et al., "Auger-based 3D printing of stretchable liquid metal paste…," *IEEE FLEPS,* 2021.

# TASK 2712.022, INTRINSIC IDENTIFIERS FOR DATABASE-FREE REMOTE AUTHENTICATION OF IOT EDGE DEVICES

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AMIT RANJAN TRIVEDI, UNIVERSITY OF ILLINOIS AT CHICAGO

## SIGNIFICANCE AND OBJECTIVES

We have developed a low-power CMOS framework and testchip for non-parametric density estimation of time-series and anomaly detection in low-likelihood samples. We have also introduced a current and delay signature-based authentication technique for IC and PCB integrity verification utilizing the onboard JTAG structure that protects against counterfeiting/cloning/in-field tampering attacks.

## TECHNICAL APPROACH

We have fabricated a testchip to learn non-parametric statistics of streaming sensor data using kernel density estimation (KDE) technique. KDE is realized using Gaussian kernel functions. The anomaly detection framework allows for programming parameters such as sliding-window length, kernel standard deviation, and likelihood threshold to ensure efficient detection. Meanwhile, through physical measurements, we observe that the supply current in a PCB heavily fluctuates depending on the overall in-circuit switching activities in the boundary scan chain of the PCB, which is utilized to authenticate ICs, and PCBs concurrently and detect in-field tampering

## SUMMARY OF RESULTS

In the PCB verification technique, we deploy a custom hardware platform that consists of two chips (an FPGA and a microcontroller) in its boundary-scan architecture (BSA). Using the industry standard, we transmit test data into BSA, and meanwhile, perform hands-on current measurements at both chip level and PCB level over 20 boards to generate device-specific signatures that demonstrate high uniqueness, robustness, and randomness properties. The block diagram of the system-level connection is depicted in Figure 1. The experiments are run over 20 different PCBs of the same kind at five different supply voltage levels. Figure 2(a) illustrates the percentage bit errors from every operating point, demonstrating the robustness of the generated signatures. Finally, we conduct intentional alteration experiments by replacing onboard FPGA to replicate the scenario of PCB tampering. The results (Figure 2(b)) indicate the successful detection of the intentional modifications introduced to the boundary-scan chain of the PCB. Figure 3(a) shows the testchip to learn the non-parametric statistics of time-series data in an unsupervised setting. Figure 3(b) shows the measured densities of Gaussian statistics with different means. Further, the test setup to characterize the multi-modal densities is being developed for detecting side-channel fault-injection attacks on crypto-hardware.

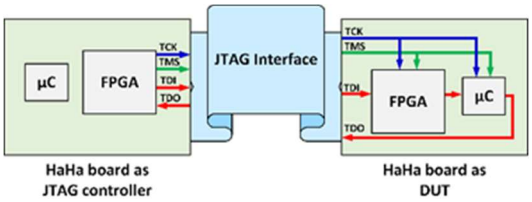


**Figure 1. Block diagram of IC and PCB level connections.**

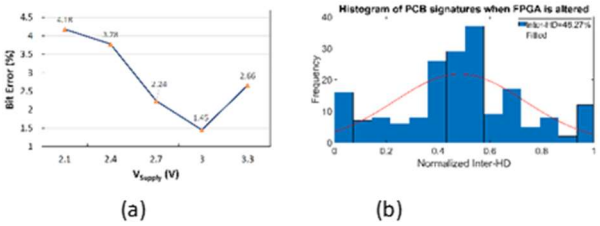


**Figure 2. (a) $V_{supply}$ variation results; (b) inter-Hamming distance results for intentional alteration experiments.**

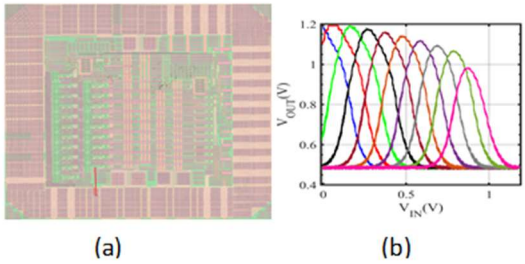


**Figure 3. (a) Test-chip for no parametric density estimation; (b) density estimation of Gaussian statistics with different means.**

**Keywords:** Kernel density estimation, non-parametric, anomaly detection, authentication, Hamming, JTAG, PUF

## INDUSTRY INTERACTIONS

Texas Instruments, Intel, IBM

## MAJOR PAPERS/PATENTS

[1] S. Bhunia et al., U.S. Patent, Filed with U. Florida, App. 17/097,446.
[2] S.D. Paul et al., "SILVerIn: Systematic Integrity Verification of Printed Circuit Board Using JTAG Infrastructure," ACM JETC.

# TASK 2712.026, FAULT CHARACTERIZATION AND DEGRADATION MONITORING OF SIC DEVICES

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## SIGNIFICANCE AND OBJECTIVES

In this project term, real-time condition monitoring circuits are proposed and developed based on switching transient to detect device degradation and monitor junction temperature. Experimental results are carried out to verify the accuracy of the proposed junction temperature measurement with aging compensation.

## TECHNICAL APPROACH

In this study, a widely adopted power cycling test is used to induce thermal-mechanical and electro-thermal stresses to SiC MOSFETs. To evaluate the device's aging impact on its switching performance, a double pulse tester platform is developed and employed. Both turn-on and turn-off transients are collected over the lifetime of the device under test (DUT). Based on the observed aging precursor, an aging detection circuit is designed and developed. To achieve on-line condition monitoring for real-time aging detection, a junction temperature ($T_j$) compensation technique is proposed and developed.

## SUMMARY OF RESULTS

To investigate the device's switching performance shift throughout aging, a double pulse test circuit is built, and the turn-on delay ($T_{d,on}$) shift of a commercial SiC MOSFET is tested at different $T_j$. It is observed that as $T_j$ goes up, the threshold voltage drops linearly, and the turn-on delay time decreases accordingly. Meanwhile, device aging causes retardation in $T_{d,on}$ as indicated at 0 and 6000 power cycles. On the contrary, it suggests a decreased turn-off delay ($T_{d,off}$) over aging.

The proposed aging detection circuit diagram is shown in Fig. 1.

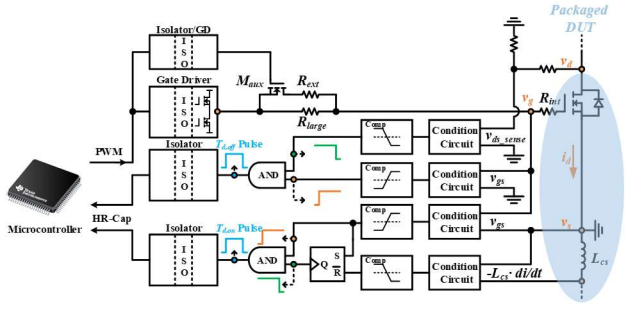


Figure 1. Circuit diagram of real-time aging detection circuit.

To mimic device degradation patterns in realistic cases, the DUT is decapsulated and its power-source bond wires are cut off from the leads. The experimental results of $T_{d,on}$, and $T_{d,off}$ measurements are shown in Fig. 2 and Fig. 3, respectively. The mismatch of the read $T_j$ through $T_{d,on}$ and $T_{d,off}$ are caused by the device's aging. By capturing this $T_j$ mismatch shift over aging, the temperature impact on aging precursors is compensated and real-time aging detection is achieved.

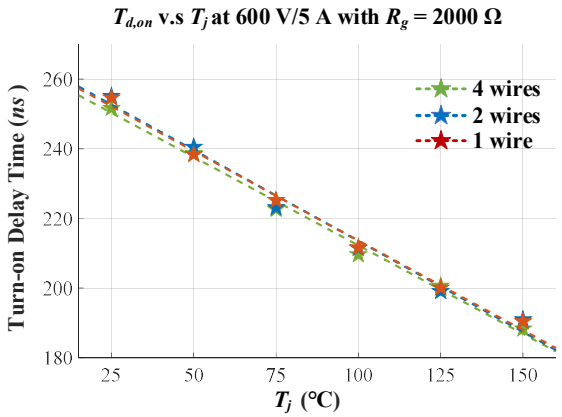


Figure 2. Measured turn-on delay at different state-of-health.

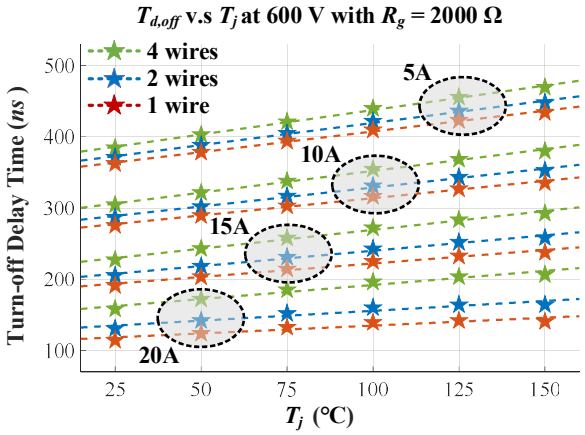


Figure 3. Measured turn-off delay at different state-of-health.

**Keywords:** aging detection, reliability, SiC MOSFETs

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] F. Yang, S. Pu, C. Xu and B. Akin, "Turn-on Delay Based Real-Time Junction Temperature Measurement for SiC MOSFETs With Aging Compensation," in IEEE Transactions on Power Electronics, vol. 36, no. 2, pp. 1280-1294, Feb. 2021.

# TASK 2712.029, NOVEL SUPER-RESOLUTION AND MIMO TECHNIQUES FOR AUTOMOTIVE AND EMERGING RADAR APPLICATIONS

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## SIGNIFICANCE AND OBJECTIVES

Millimeter wave (mmWave) radar sensors provide the ability to meet privacy requirements in addition to being unobtrusive and non-intrusive, with their capability of detecting motion and vital signs from a distance, while maintaining accuracy. In the past year, we studied and constructed a new lens enabled mmWave multiple-input multiple-output (MIMO) mmWave radar system for vital signal sign detection. This report presents preliminary empirical results on vital signs detection algorithms using mmWave radar sensors enhanced with a lens.

## TECHNICAL APPROACH

The focusing nature of the lens can be utilized to study the points in the body which is suitable for vital sign detection and evaluate the variations in heart rate detection, depending on the angle of the subject. In particular, a lens cage system (shown in Fig. 1) is devised, and 3D printed to study the impact of lens systems and to optimize the capture of heart rate signals. In this report, we propose improved heart rate detection strategies that are useful in enhancing heart rate detection in instances of some small-scale motion, and in driver vital signs detection systems and patient heart rate monitoring systems.

## SUMMARY OF RESULTS

We designed a lens cage system that could be mounted on a mechanical scanner. The lens cage holds the lens and sensor system in place, and the mechanical scanner allowed us to move the entire system around and evaluate variations in doppler results depending on where the signal was focused on across the human body. Due to the unavailability of commercial lens cage systems for the 4" lens used in our study, the lens cage and mounting plates were all 3D printed. A setup using this system is shown in Fig.1. The method concerning subject (or object) detection and then vital signs monitoring is broken down into many steps. The first idea is to differentiate a space containing static clutter and remove it to contain returns from human subjects.

There are many implications that matter for vital signs detection when lenses are used with MIMO arrays. The first is that within the aperture of the lens, the range measurement of objects is enhanced. The squared amplitude of a point reflector as it is moved at discrete points (not continuously as before) in cross-range. The relatively stable amplitude is observed for the case where there is no lens in front of the sensor. For the case where a lens is placed in front of the sensor, within a certain window that is comparable to the diameter of the lens, there is a big gain in the detection of the point reflector. The setup of the lens and lens cage system ensures that the transmit signal is collimated and the field of view of the system is restricted. To validate that this was indeed happening, the mechanical scanner was used to move the lens cage system across the azimuth and elevation while a corner reflector was kept at a certain fixed distance at approximate boresight of the lens.

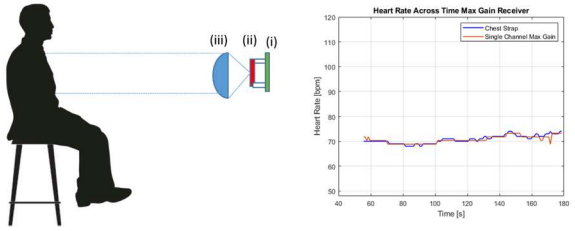


**Figure 1. Left: Measurement Setup with Lens with (i), (ii), and (iii) being the data capture board, the radar sensor, and the Plano-convex lens GHz. Right: Heart rate tracking capture captured at a position optimized point.**

The use of the lens provides gains in range and doppler domains, and these gains are provided mostly within the aperture radius of the lens. However, due to spatial differences in the antenna locations, there is a spatial diversity introduced in the system. This would imply that the received signals in the eight possible channels are obtained from different directions. However, there are still differences in the quality of the signal depending on where we place the sensor and lens system in the elevation. Since the height of the antennas is the same, to study the effect of vital sign detection depending on the height of the subject, a stable mechanical system that can move to focus in a certain direction is necessary. Depending on where the system focuses, different points in the torso are illuminated.

This can be validated by the heart rate tracking results of a subject with the sensor targeting the optimal region in the torso. A sample result is shown in Fig. 1 (right).

**Keywords**: mmWave, radar, lens array, vital sign monitor

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] J. W. Smith, M. E. Yanik and M. Torlak, "Near-Field MIMO-ISAR Millimeter-Wave Imaging," *Proc. IEEE Radar Conf.,* Sept. 2020, pp. 1-6, Florence, Italy.

# TASK 2810.002, SECURITY-AWARE DYNAMIC POWER MANAGEMENT FOR SYSTEM-ON-CHIPS

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## SIGNIFICANCE AND OBJECTIVES

The proposed research investigates the energy-security trade-offs associated with Dynamic Power Management (DPM). The proposed effort will develop a methodology to characterize security implications of DPM in SoCs and design circuit/system techniques to co-optimize security and energy efficiency of DPM.

## TECHNICAL APPROACH

This effort will pursue a cross-layer approach to understand the energy-security trade-offs in Dynamic Voltage Frequency Scaling (DVFS). We have designed power domains that are secure against power-/EM- side-channel analysis by leveraging the distributed integrated voltage regulators. We have investigated the energy-security trade-off at the chip level by focusing on the DVFS controller and algorithm.

## SUMMARY OF RESULTS

***DVFS as a Security Exploit [1]:*** Dynamic Voltage and Frequency Scaling (DVFS) plays an integral role in reducing the energy consumption of mobile devices, meeting the targeted performance requirements at the same time. We examine the security obliviousness of CPU Freq. in DVFS framework of Linux-kernel based systems. Since Linux-kernel based operating systems are present in a wide array of applications, the high-level CPU Freq policies are designed to be platform-independent. Using these policies, we present BiasP exploit, which restricts the allocation of CPU resources to a set of targeted applications degrading their performance.

***Trustworthy Hardware based Malware Detector (HMD) [2]***: The machine learning (ML) models used in HMDs are agnostic to the uncertainty that determine whether the model "knows what it knows," severely undermining their trustworthiness. We propose an ensemble-based approach that quantifies uncertainty in predictions made by ML models of an HMD when it encounters an unknown workload than the ones it was trained on. We test our approach on power management-based and performance counter-based HMDs.

***Securing IoT Devices using Dynamic Power Management [3]:*** We demonstrated Dynamic Voltage and Frequency Scaling (DVFS) states form a signature pertinent to an application, and its run-time variations comprise of features essential for securing IoT devices against malware attacks. We have demonstrated this proof of concept by performing experimental analysis on Snapdragon 820 mobile processor, hosting Android operating system (OS). We developed a supervised machine learning model for application classification and malware identification by extracting features from the DVFS states time-series. We also performed power measurements under different governors to evaluate power-security aware governor.

***Machine Learning in Wavelet Domain for Electromagnetic Emission Based Malware Analysis [4]:*** We have presented a signal processing and machine learning (ML) based methodology to leverage Electromagnetic (EM) emissions from an embedded device to remotely detect a malicious application running on the device and classify the application into a malware family. We have developed Fast Fourier Transform (FFT) based feature extraction followed by Support Vector Machine (SVM) and Random Forest (RF) based ML models to detect a malware. We further demonstrated the use of Discrete Wavelet Transform (DWT) based feature extraction from spectrograms of EM side-channel traces and perform ML on the extracted features to learn fine-grained patterns of malware families.

**Keywords:** Side-channel, EM emission, Dynamic Power Management, Machine Learning, Malware Detection

## INDUSTRY INTERACTIONS

Intel, IBM

## MAJOR PAPERS/PATENTS

[1] H. Kumar, et. al, "BiasP: A DVFS based Exploit to Undermine Resource Allocation Fairness in Linux Platforms," IEEE/ACM International Symposium on Low-Power Electronic Design (ISLPED), August 2020.

[2] H. Kumar, et. al., "Towards Improving the Trustworthiness of Hardware based Malware Detector using Online Uncertainty Estimation," Design Automation Conference (DAC), 2021.

[3] N. Chawla, et.al, "Securing IoT Devices using Dynamic Power Management: Machine Learning Approach," IEEE Internet of Things Journal.

[4] N. Chawla, et. al., "Machine Learning in Wavelet Domain for Electromagnetic Emission Based Malware Analysis," IEEE Transactions on Information Forensics and Security (TIFS), vol. 16, May 2021, pp. 3426-3441.

# TASK 2810.005, CIRCUIT DESIGN FOR ESD AND SUPPLY NOISE MITIGATION

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## SIGNIFICANCE AND OBJECTIVES

This project sought to develop (1) IC-level power distribution networks that promote power integrity even in the presence of power-on ESD, and (2) understand and mitigate latch-up that occurs in response to power-on ESD.

## TECHNICAL APPROACH

This work identifies ESD-induced reliability hazards, including latch-up, and evaluates solutions. There is a special emphasis on power-on ESD, e.g. from system-level discharges. Laboratory characterization of custom-designed test chips is the primary method used to investigate reliability hazards and evaluate proposed solutions. Power-on ESD induces supply noise and an effort is made to accurately measure the on-chip noise; board-level measurements are unsuitable because the package inductance decouples the noise signals at the board and chip levels. Therefore, the researchers develop and deploy on-chip noise sensors. Measurement results are interpreted with the aid of circuit and electromagnetic simulations.

## SUMMARY OF RESULTS

Power-on ESD, e.g. system-level ESD, induces noise on the chip ground bus, and ground noise may be converted to supply noise. This work found a strong positive correlation between the amplitude of the ESD-induced noise on the core power supply and the occurrence of bit flips in registers or memory cells. That study was carried out in the context of a semi-custom OpenMSP430 microcontroller test chip [1]. The on-chip supply noise was measured using supply noise monitor circuits.

This work established that internally regulated supplies reject the ESD-induced ground noise provided that there are no package pins connected to the regulated supply bus [2]. In the absence of an integrated voltage regulator, partial mitigation of the supply noise may be obtained by using separate ground busses for the IO circuits and the core logic. Those grounds cannot be completely isolated from one another due to component-level ESD requirements.

A previously unrecognized cause of transient latch-up (TLU) was identified for chip designs that have reverse body bias capability [3]. TLU is triggered by current injection at an IO pin, most notably from power-on ESD. The ampere-scale ESD current produces potential gradients across the ground net. Those gradients may cause the parasitic NPN devices associated with NMOS transistors in the circuit to turn on. Specifically, the NPN gets biased in the forward active region because the NMOS body voltage, which is driven by the regulator or charge pump circuit, is at a higher potential than the source, which is connected to the local VSS bus. The ground references for the transistor and for the regulator can differ by 1 V or more during ESD. The NPN base current provides the trigger for latch-up.

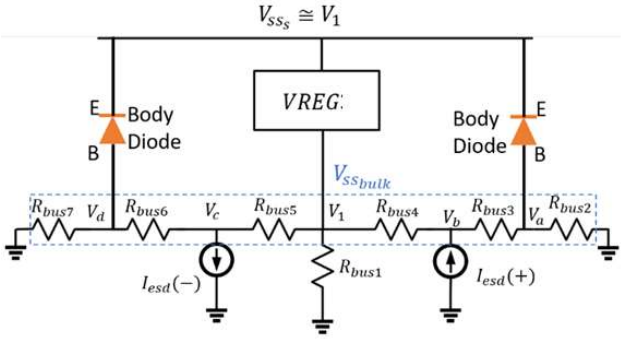


**Figure 1. Resistive model of an on-chip ground net, for a chip with reverse body bias capability. The figure illustrates how a positive bias on the base-emitter junction of the parasitic NPN may develop during ESD current injection. The resultant P-well current triggers on PNPN devices in the layout, resulting in latch-up.**

**Keywords:** ESD, power integrity, latch-up

## INDUSTRY INTERACTIONS

NXP, Texas Instruments, Intel

## MAJOR PAPERS/PATENTS

[1] S. Vora and E. Rosenbaum, "Analysis of system-level ESD-induced soft failures in a CMOS microcontroller," *IEEE Trans. EMC*, 62 (6), 2020.

[2] Y. Xiu and E. Rosenbaum, "Analysis and design of integrated voltage regulators for supply noise rejection during system-level ESD," IEEE Trans. CAS I, 67 (12), 2020.

[3] S. Vora et al., "Increased latch-up susceptibility of ICs using reverse body bias," *EOS/ESD Symp.*, 2020.

# TASK 2810.014, DEEP LEARNING SOLUTIONS FOR ADAS: FROM ALGORITHMS TO REAL-WORLD DRIVING EVALUATIONS

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NAOFAL AL-DHAHIR, THE UNIVERSITY OF TEXAS AT DALLAS

## SIGNIFICANCE AND OBJECTIVES

Investigate deep-learning-based algorithms and evaluate their performance using fusion of sensing technologies (regular cameras, infrared lenses, RADAR) to estimate the driver's visual attention in real-world driving conditions. The project explores novel probabilistic models of visual attention, creating shared representation across multiple sensing technologies.

## TECHNICAL APPROACH

We analyze alternative sensing technologies suitable for head pose estimation for in-vehicle applications, creating novel visual attention models (gaze). We perform real-world driving tests to evaluate alternative sensors that are appropriate for head pose estimation. We develop novel probabilistic models of the visual attention of the drivers describing confidence regions of the gaze given the position and orientations of the driver's head using deep learning. We propose multimodal deep learning frameworks to fuse sensors using a shared layer representation between modalities, creating robust and accurate solutions regardless of the environment.

## SUMMARY OF RESULTS

1) Data collection: We have established the Multimodal Driver Monitoring Database, which has multiple sensors to study visual attention of the driver (four cameras, depth cameras, and CAN-Bus).

2) Dynamic head pose estimation from Point-Cloud Data: In the automotive context, head pose provides crucial information about the driver's mental state, including drowsiness, distraction and attention. Head pose estimation is a challenging problem in the car due to sudden illumination changes, occlusions and large head rotations that are common in a vehicle. These issues can be partially alleviated by using depth cameras. Head rotation trajectories are continuous with important temporal dependencies. Our study leverages this observation, proposing a novel temporal deep learning model for head pose estimation from point cloud. The approach extracts discriminative feature representation directly from point cloud data. The frame-based representations are then combined with bidirectional long short-term memory (BLSTM) layers. We achieve better results compared to non-temporal algorithms using point cloud data, and state-of-the-art models using RGB images.

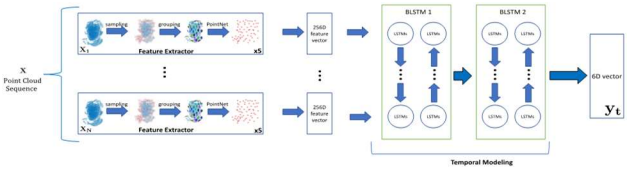


**Figure 1. Dynamic head pose estimation from Point-Cloud Data**

3) Visual attention using head pose and eye appearance: The knowledge of the driver visual attention can be helpful in designing intelligent vehicles. The gaze of the driver can be formulated in terms of a probabilistic visual map that represents a region around which the driver's attention is focused. The area of the predicted region changes based on the level of confidence of the prediction. We proposed a framework based on convolutional neural network (CNN) that takes the head pose and the eye appearance of the driver as input, and creates a fusion model that predicts the driver's gaze in a 2D grid. The model contains upsampling layers to create predictions at multiple resolutions. The proposed model predicts the region of the gaze with the target lying within the 75% region with an accuracy of 91.54%.

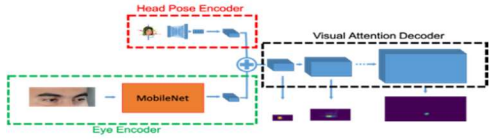


**Figure 2. Visual attention using head pose and eye appearance**

**Keywords:** ADAS, head pose estimation, deep learning, visual attention, multimodal sensing

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] T. Hu, S. Jha, and C. Busso, "Robust driver head pose estimation in naturalistic conditions from point-cloud data," in IEEE Intell. Veh. Sym. (IV2020), June 2020.
[2] T. Hu, S. Jha, and C. Busso, "Temporal head pose estimation from point cloud in naturalistic driving…," IEEE Trans. Intell. Transp. Sys, accepted,2021
[3] S. Jha and C. Busso. "Estimation of driver's gaze region from head position and orientation using probabilistic confidence regions." IEEE Trans. Intell. Veh., Submitted.
[4] S. Jha, M. Marzban, T. Hu, M.H. Mahmoud, N. Al-Dhahir, and C. Busso. "The multimodal driver monitoring database: A naturalistic corpus to study driver attention." IEEE Trans. Intelligent Transportation Systems, submitted.

# TASK 2810.016, CONDITION MONITORING OF INDUSTRIAL/ AUTOMOTIVE DRIVE COMPONENTS THROUGH LEAKAGE FLUX

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## SIGNIFICANCE AND OBJECTIVES

Condition monitoring of electrical motors is performed by using parameters such as current, back emf, vibration, etc. In this research, the stray magnetic field around the motor is used for detecting the inter-turn short circuit fault and temperature estimation of permanent magnets in a permanent magnet synchronous motor (PMSM) using TI DRV425's.

## TECHNICAL APPROACH

Electromechanical energy conversion in electrical motors takes place via a magnetic field. Any fault that occurred in a motor is more likely to have fault signatures in its air gap magnetic field. Since it is not possible to measure the air gap magnetic field, the stray magnetic field around the motor reflects the variation in the air gap magnetic field which makes it a promising condition monitoring tool.

## SUMMARY OF RESULTS

Temperature monitoring of permanent magnets is essential since the magnets are susceptible to thermal demagnetization. In this research, we are proposing a method to estimate the temperature of permanent magnets through the stray magnetic field. The change in permanent magnet flux due to temperature affects the stray magnetic field around the motor. It is also affected by the magnetic field due to stator current and variation in permeability of steel core due to a change in operating point. A compensation coefficient is introduced to compensate for the effect of variation of stator permeability due to the change in the operating point of magnets. The flux due to a permanent magnet is decoupled from measured stray magnetic flux using the proposed coefficient and stator current information.

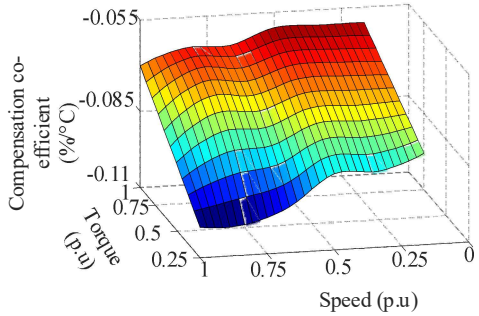


**Figure 1. Experimentally calculated compensation co-efficient.**

The proposed coefficient values are calculated for different operating conditions and used as a look up table to calculate the compensated flux density. The magnet temperature is estimated online using the compensated stray magnetic flux density. Extensive experiments are performed under various dynamic operating conditions to estimate the permanent magnet temperature online to validate the method. The estimated temperature results show that the proposed method can estimate the temperature within 5°C of actual.

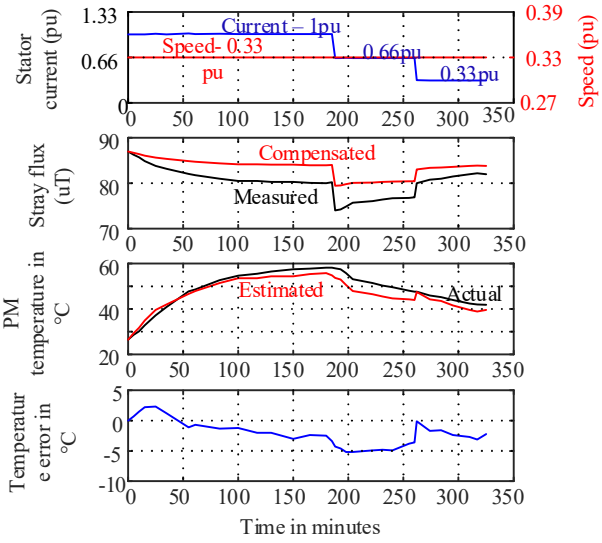


**Figure 2. Online temperature estimation of permanent magnets in a PMSM.**

**Keywords: stray magnetic flux, PMSM, condition monitoring, permanent magnet temperature estimation**

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] V. Gurusamy, E. Bostanci, C. Li, Y. Qi and B. Akin, "A Stray Magnetic Flux-Based Robust Diagnosis Method for Detection and Location of Interturn Short Circuit Fault in PMSM," in *IEEE Transactions on Instrumentation and Measurement*, vol. 70, pp. 1-11, 2021, Art no. 3500811.

[2] V. Gurusamy, K. H. Baruti, M. Zafarani, W. Lee and B. Akin, "Effect of Magnets Asymmetry on Stray Magnetic Flux Based Bearing Damage Detection in PMSM," in IEEE Access, vol. 9, pp. 68849-68860, 2021.

# TASK 2810.017, RELIABILITY STUDY OF E-MODE GAN HEMT DEVICES

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HISASHI SHICHIJO, THE UNIVERSITY OF TEXAS AT DALLAS

## SIGNIFICANCE AND OBJECTIVES

AlGaN/GaN High Electron Mobility Transistors (HEMTs) are excellent candidates for high-voltage power switching applications. This work involves TDDB of commercial p-GaN gate E-mode HEMTs. Failed devices were inspected employing SEM/FIB to locate the failure precisely and HR TEM imaging to identify the physical mechanism for the failure.

## TECHNICAL APPROACH

Commercially available AlGaN/GaN E-mode HEMTs were characterized for their electrical and physical characteristics. Electrical measurements include Time Dependent Dielectric Breakdown (TDDB) tests at various gate stressing voltage, current, and different temperatures to obtain the device response and time to fail data. Physical characterization of the device before and after the breakdown was performed with high-resolution electron microscopy techniques, including in-situ TEM electrical measurements.

## SUMMARY OF RESULTS

The E-mode p-GaN gate GaN HEMTs were pulse stressed at 7V, 7.5V, and 8V with a pulse duration of 3.2 ms for both on and off period. The devices showed a step-like failure, where $I_G$ increased in steps and stays stable until it finally fails with a large increase of $I_G$. Fig. 1(a) shows a plot of $I_G$ versus 7.5-V pulsed stress time. Fig. 1(b) shows the entire sweep for the device. The first stage is partial Schottky failure with charges leaking in the p-GaN layer from metal/p-GaN contact and channel, and the final is the complete failure of the gate when the gate loses its control over the transistor.

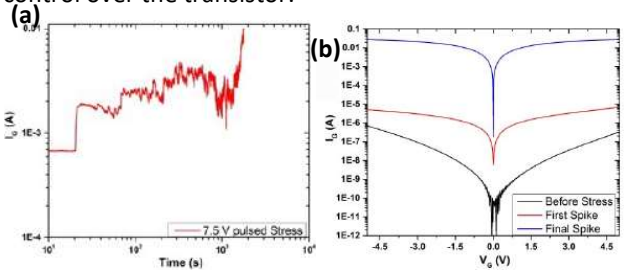


**Figure 1. (a) 7.5-V pulse stressed data with $I_G$ spikes and (b) corresponding gate characteristics.**

The modeling of TDDB of p-GaN gate GaN HEMTs is based on the thermos-chemical model, which explains the lattice distortion/strain due to the high electric field in the depletion region of the p-GaN gate and describes the time-to-fail (TTF) as an exponential function of the electric field. The magnitude of the electric field in the depletion region is estimated from the measured gate capacitance. The field acceleration parameter ϒ extracted by fitting the TTF to the experimental data is shown to be in a reasonable range expected from the dielectric constant of GaN (Fig. 2). It is noted that the calculated electric field in the p-GaN region is around 3.7MV/cm, which is close to the breakdown field.

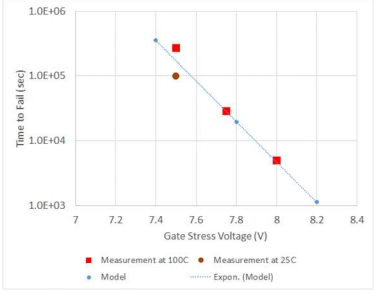


**Figure 2. (a) Model fit (line) to the experimental TDDV data (red squares).**

An in-situ TEM sample was made out of the device's active area using the FIB lift-off technique and was further thinned down to form p-GaN gate column-stacks. Isolation was done to make sure current flows through the gate to the GaN. Fig. 3 shows the final device structure with the gate stack and the TEM setup for in-situ measurement. Our results demonstrate the capability of the in-situ experiment, but our findings point out the stand-alone gate column sample is not conducting the current. This helps us conclude that the substrate and the GaN region of the device are un-doped. The source or drain region of the device will also be necessary for this sample to induce the current flow through the gate.

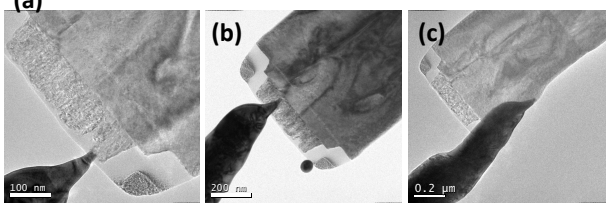


**Figure 3. TEM images of in-situ probe contacting (a) TiN, (b) near to the gate, and (c) on the GaN part of the stack.**

**Keywords:** E-mode GaN HEMT, Reliability, in-situ TEM

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

# TASK 2810.021, A COLLABORATIVE MACHINE LEARNING APPROACH TO FAST AND HIGH-FIDELITY DESIGN PREDICTION

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YIRAN CHEN, DUKE UNIVERSITY

## SIGNIFICANCE AND OBJECTIVES

The objective of this work is to enable crosstalk prediction at the cell placement stage. To the best of our knowledge, this is the first crosstalk prediction technique that does not rely on any trial routing.

## TECHNICAL APPROACH

Machine learning (ML) techniques are developed for routing-free crosstalk prediction. Four machine learning engines are evaluated, including logistic regression (LR), neural network (NN), random forest (RF), and XGBoost. The machine learning models are applied to predict coupling capacitance, crosstalk noise, and delay increase due to crosstalk. By allowing a routing-free approach, early crosstalk estimation can be computed at a much faster speed than existing techniques.

## SUMMARY OF RESULTS

The machine learning-based crosstalk prediction flow is outlined in Figure 1. It takes a placement solution as input and predicts coupling capacitance, crosstalk noise, and crosstalk-induced delay of each signal net. The crosstalk noise is measured by the product between noise pulse width and height.

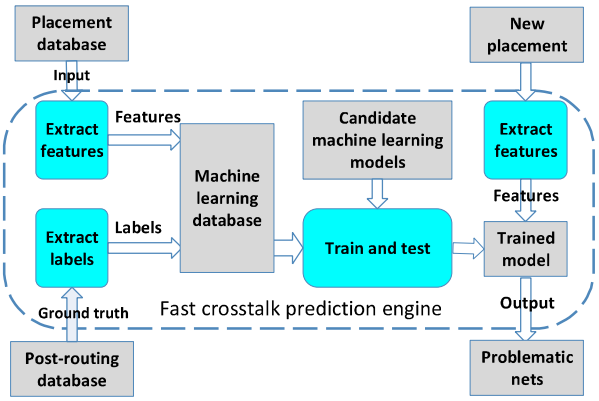


**Figure 1. Crosstalk prediction flow.**

The input features to ML models include the following:

- RUDY (rectangular uniform wire density), which is a simplified wire density estimate for placement.
- Fan-out size for each net.
- The maximum source-sink distance for each net.
- Net driver type with one-hot encoding.
- Net source capacitance.
- Total sink capacitance of a net.
- Fan-in of the source cell.
- Pre-routing wire delay from static timing analysis.
- Output slew of the source cell of a net.
- The number of neighboring nets, in terms of net bounding box overlap.
- The mean, standard deviation, and maximum of the overlap with one's neighboring nets.

**Table 1. Coupling capacitance prediction results.**

| Model | FPR | TPR | F1 | BAcc | AUC |
|---|---|---|---|---|---|
| Baseline | 1.06% | 78.93% | 53.14% | 88.94% | 0.993 |
| LR | 1.03% | 80.91% | 50.98% | 89.94% | 0.899 |
| NN | 0.98% | 80.73% | 51.90% | 89.87% | 0.959 |
| RF | 0.90% | 81.62% | 54.16% | 90.36% | 0.994 |
| XG | 0.89% | 81.87% | 54.62% | 90.49% | 0.994 |

**Table 2. Crosstalk noise prediction results.**

| Model | FPR | TPR | F1 | BAcc | AUC |
|---|---|---|---|---|---|
| Baseline | 1.56% | 50.88% | 37.47% | 74.66% | 0.970 |
| LR | 1.62% | 75.15% | 47.17% | 86.77% | 0.868 |
| NN | 1.45% | 66.56% | 45.09% | 82.55% | 0.846 |
| RF | 1.31% | 76.34% | 52.27% | 87.51% | 0.987 |
| XG | 1.28% | 78.37% | 53.69% | 88.54% | 0.990 |

**Table 3. Crosstalk-induced delay increases prediction results.**

| Model | FPR | TPR | F1 | BAcc | AUC |
|---|---|---|---|---|---|
| Baseline | 4.35% | 52.83% | 18.71% | 74.24% | 0.937 |
| LR | 2.43% | 69.29% | 33.19% | 83.43% | 0.834 |
| NN | 2.39% | 73.10% | 35.07% | 85.35% | 0.939 |
| RF | 2.10% | 74.74% | 38.45% | 86.32% | 0.978 |
| XG | 1.80% | 76.25% | 42.35% | 87.23% | 0.986 |

The results from IWLS 2005 benchmark are summarized in Tables 1, 2, and 3, where FPR and TPR mean false positive rate and true positive rate, respectively. F1 = TP/(FP+TP). BAcc is balanced accuracy: (1-FPR+TPR)/2. AUC represents the area under the receiver operating characteristic curve. The ML approaches are 500X faster than the baseline, which is based on global routing.

**Keywords:** crosstalk noise, machine learning, design prediction, signal integrity, circuit timing

## INDUSTRY INTERACTIONS

IBM, NXP, ARM

## MAJOR PAPERS/PATENTS

[1] C. Mao R. Liang, Z. Xie, J. Jung, V. Chauhan, Y. Chen, J. Hu, H. Xiang, and G.-J. Nam, "Routing-Free Crosstalk Prediction," *IEEE/ACM International Conference on Computer-Aided Design*, 2020.

# TASK 2810.022, A COLLABORATIVE MACHINE LEARNING APPROACH TO FAST AND HIGH-FIDELITY DESIGN PREDICTION

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JIANG HU, TEXAS A&M UNIVERSITY

## SIGNIFICANCE AND OBJECTIVES

The objective of this work is to predict individual net length before placement. This is the first work making use of GNN for pre-placement net length prediction.

## TECHNICAL APPROACH

We propose a graph attention network (GAT)-based model named Net$^2$, which is customized for this net length problem. In Net$^2$, we extract global topology information through partitioning. Based on partition results, we define innovative directional edge features between nets, which substantially contribute to Net$^{2}$'s superior accuracy.

## SUMMARY OF RESULTS

To apply graph-based methods for net size prediction, we convert each netlist to one directed graph, where each net is represented as a node. Each node's length is the HPWL of the bounding box of the net after placement.

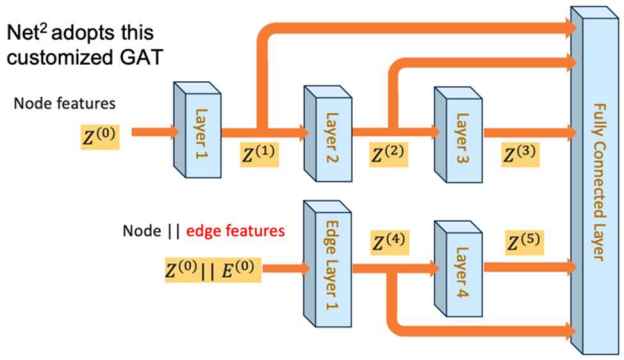


**Figure 1. Customized GAT model in Net$^2$.**

The input features at each node/net include the following:

- Fan-in size and fan-out size
- Area of the driver cell and all cells
- Neighboring nodes' fan-in/fan-out/area info

For each net, besides its local information defined in the above node features, the big picture/global information, which reflects its position in the whole netlist, is extremely important for accurate prediction. To capture the global information, we use an efficient multi-level partitioning method to divide one netlist into multiple partitions, and then incorporate global information from these partitions into edge features of the graph. Then as Figure 1 shows, we develop a customized GAT model to process all these node and edge features.

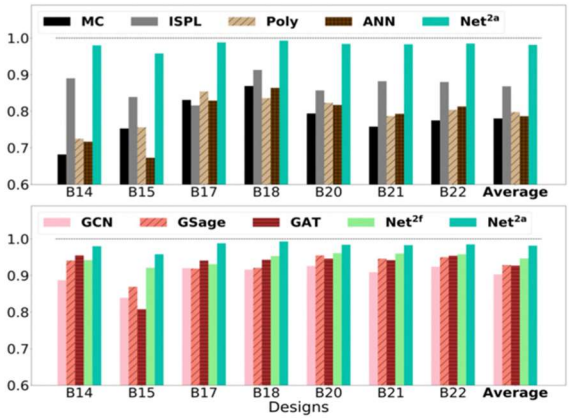


**Figure 2. Net size prediction results.**

**Table 1. Path length prediction results.**

| Methods | B14 | B15 | B17 | B18 | B20 | B21 | B22 | Ave |
|---|---|---|---|---|---|---|---|---|
| ISPL | 58.9 | 57.5 | 56.5 | 74.0 | 72.5 | 63.0 | 75.5 | 65.4 |
| Poly | 65.5 | 80.0 | 78.0 | 68.0 | 82.0 | 85.0 | 84.0 | 77.5 |
| ANN | 68.0 | 76.0 | 80.0 | 69.0 | 78.5 | 82.0 | 75.5 | 75.6 |
| GCN | 63.5 | 75.0 | 86.5 | 56.0 | 82.0 | 81.5 | 85.5 | 75.7 |
| GSage | 65.0 | 88.0 | 93.0 | 77.0 | 81.5 | 67.0 | 80.0 | 78.8 |
| GAT | 63.0 | 92.0 | 95.0 | 83.5 | 83.5 | 76.0 | 89.5 | 83.2 |
| Net$^{2f}$ | 79.0 | 88.5 | 97.5 | 84.0 | 75.5 | 83.0 | 92.0 | 85.6 |
| Net$^{2a}$ | 86.5 | 95.0 | 96.0 | 90.5 | 90.5 | 93.5 | 95.5 | 92.5 |

The results from the ITC'99 benchmark are summarized in Table 1 and Figure 2. The net size prediction accuracies measured by correlation coefficient are shown in Figure 2. We provide an accuracy-oriented version Net$^{2a}$ and a fast version Net$^{2f}$ for different application scenarios. Both of them outperform all previous methods.

An application of net length estimation is to predict the length of any given path, which correlates with post-placement wire delay on the path. The accuracy is shown in Table 1. We observe a similar trend, demonstrating the superior performance of our Net$^2$ methods.

**Keywords:** wire length, net size, machine learning, design prediction, physical-aware synthesis

## INDUSTRY INTERACTIONS

IBM, NXP, ARM

## MAJOR PAPERS/PATENTS

[1] Zhiyao Xie, Rongjian Liang, Xiaoqing Xu, Jiang Hu, Yixiao Duan, Yiran Chen, "Net$^2$: A graph Attention Network Method Customized for Pre-Placement Net Length Estimation," *Asia and South Pacific Design Automation Conference*, 2021.

# TASK 2810.023, MACHINE LEARNING DRIVEN AUTOMATIC MIXED-SIGNAL DESIGN VERIFICATION-VALIDATION FOR AUTOMOTIVE APPLICATIONS

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## SIGNIFICANCE AND OBJECTIVES

The research will develop the next generation of pre- and post-silicon design model extraction and validation tools that will allow complex mixed-signal systems to be tested and debugged automatically orders of magnitude more efficiently (speed, accuracy) than current techniques while providing diagnosis down to the physical level for quick design fixes.

## TECHNICAL APPROACH

The proposed approach involves developing a frequency-based stimulus generation algorithm that exposes behavioral discrepancies between high level AMS circuits and their silicon implementations across all possible inputs. Such discrepancies may occur because of one or more design bugs in circuit modules. To diagnose such bugs, we perform multiple bug correction experiments. Learning kernels are placed across modules in the high-level model and trained to replicate the buggy response. An error response clustering algorithm along with knowledge of the placement of kernels is used to diagnose likely buggy modules. Results on multiple mixed-signal designs prove the viability of the proposed approach.

## SUMMARY OF RESULTS

The key focus of this research is on post-silicon bug diagnosis: identifying circuit modules with buggy behaviors. Buggy module behaviors are defined as input-output transformations in hardware that are different from those predicted by pre-silicon simulation models by larger than a calibrated threshold. There may be multiple bugs in a module and multiple circuit modules may be buggy. Specific contributions are as follows: a novel frequency domain diagnostic test stimulus generation algorithm is developed that allows exposure of multiple design bugs using iterative bug behavior learning iterations. Therefore, multiple types of bug effects within each circuit module and across different modules are exposed by the test suite. This is particularly important for correct (multiple) bug diagnoses.

The use of a diverse set of design bug correction experiments is proposed. Since there is limited observability in silicon, these experiments are performed on simulation models of the circuit to recreate the bug effects as observed on the circuit outputs in silicon by concurrently correcting the outputs of multiple circuit modules using dedicated machine learning kernels as opposed to sequential correction. We propose the use of a response clustering algorithm for analyzing data generated by the correction experiments for diagnosis. Ordered lists of likely buggy modules are generated, including modules that may be simultaneously buggy. Overview of the test generation algorithm and the selected diagnosis results on PLL is shown in Figure 1 and Table 1, respectively.

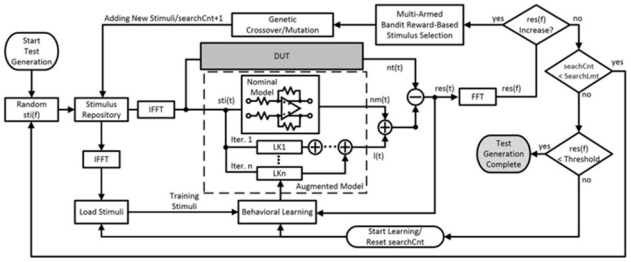


**Figure 1. Overview of the proposed frequency-based test generation algorithm.**

**Table 1. Diagnosis results on a type II, 3rd order PLL.**

| Test Vehicle | Buggy Module | Bug Type | Diagnosis Ranking | | | Successful Diagnosis? |
|---|---|---|---|---|---|---|
| | | | 1st | 2nd | 3rd | |
| PLL | (1) | VCO Nonlin. | (1) | (1) | N/A | Yes |
| | (2) | Filter Nonlin. | (2) | (1,2) | N/A | Yes |
| | (3) | CP Current Mismatch | (3) | (3) | (2,3) | Yes |
| | (1,2) | (1) VCO Nonlin. (2) Filter Nonlin. | (1,2) | (1) | N/A | Yes |
| | (1,3) | (1) VCO Nonlin. (3) CP Current Mismatch | (1,3) | (1) | (1) | Yes |
| | (2,3) | (2) Filter Nonlin. (3) CP Current Mismatch | (2,3) | (2) | ∅ | Yes |
| | (1,2,3) | (1) VCO Nonlin. (2) Filter Nonlin. (3) CP Current Mismatch | (1,2,3) | N/A | N/A | Yes |

**Keywords:** Analog/RF design validation, test generation, machine learning

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] J. Y. Lei and A. Chatterjee, "Automatic surrogate model generation and debugging of analog/mixed-signal designs via collaborative stimulus generation and machine learning," in 2021 26th Asia and South Pacific Design Automation Conference (ASP-DAC). IEEE, 2021, pp. 140–145.

# TASK 2810.025, MACHINE LEARNING-BASED LAYOUT ANALYSIS AND NETLIST OPTIMIZATION FOR DEFECT TOLERANCE AND DESIGN ROBUSTNESS TO PROCESS IMPERFECTIONS AND VARIATIONS

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## SIGNIFICANCE AND OBJECTIVES

This work focuses on using Machine Learning (ML) towards obtaining defect tolerant IC layouts and netlists. Currently, we focus on: (i) Developing coverage metrics and confidence estimation methods to enhance layout Design Space Exploration (DSE). (ii) Developing methods to characterize the effects of design-process interactions on timing, thereby, synthesizing defect tolerant netlists.

## TECHNICAL APPROACH

**Layout-level methods:** We evaluated different types of feature extraction (F.E) procedures for improving lithographic hotspot detection in layouts. We examined 3 different types of feature extraction (F.E) procedures which can be broadly classified into density-based methods and fragment-based methods. We identified two procedures from density-based methods, namely density and co-ordinate, and one from the fragment-based methods, namely Fragment Transform Plus, to compare their hotspot hit rates using standardized metrics and list their merits and demerits.

**Netlist-level methods:** Our methods include characterization of the cell library database for delay defects, quantification of defect tolerance of netlists, and usage of defect characterization to drive the identification and rewiring/redesigning of netlists, to increase delay defect tolerance.

## SUMMARY OF RESULTS

**ML-based layout analysis:** There has been a lot of work to improve hotspot detection through developing state-of-the-art benchmarks (*ICCAD'19 benchmarks*), providing clarity and identifying pitfalls in existing benchmarks, and offering recommendations in improving the quality of hotspot detection. We focused on another integral part of hotspot detection, which is the feature vector extraction. This is important because it focuses on converting an image hotspot to a numerical one. If not done right, there may be important features that will be lost and hence will hinder the machine learning procedure. We explored two density-based FE methods, a) Density FE – This is the simplest and fastest FE method that captures the amount of metal area present in a defined area. b) Co-ordinate FE – This captures the coordinates of the metal that are present in a defined area with corner information (if there is a change in direction in the metal orientation). The third FE method was a fragment-based FE method that would capture the neighboring metal information such as the number of parallel fragments, the orientation of the parallel fragments. Upon adding weights to each of these, we found that the results improved while doing so as we were assisting the ML algorithm to converge.

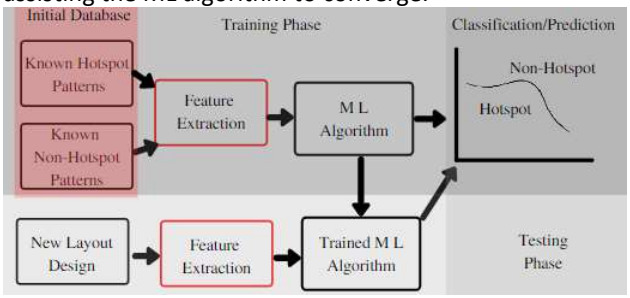


**Figure 1. ML-Based Layout Procedure for identifying hotspots.**

**ML-based netlist optimization:** To develop defect tolerant netlists, the synthesis tool must be supplied with databases that are characterized for their delay vulnerability under small delay defects (SDDs) and a method to bias the synthesis towards creating design netlists using robust cells in the library. For this purpose, we developed automation to characterize a subset of 12-nm cell libraries (~1000 cells), containing 80 cells, for its delay timings by injecting defects modeled as parasitic resistances/capacitances and performed SPICE simulations with the SiliconSmart tool. The delay responses of these simulations were used to modify the delays of the original library database to reflect the cell delay vulnerabilities. The "defect-aware" library database was provided to the synthesis tools (bias) to pick robust cells while generating the "defect-aware" netlists. We are currently evaluating these "defect-aware" netlists to quantify their delay defect tolerance using cell timing information from the PrimeTime database.

**Keywords:** Layout analysis, Coverage estimation, Benchmarks, Netlist optimization, Defect tolerance

## INDUSTRY INTERACTIONS

Intel, Mentor, A Siemens Business

## MAJOR PAPERS/PATENTS

[1] S. S. Thiagarajan, S. Natarajan, and Y. Makris, "Defect Tolerance Estimation and Netlist Optimization for Digital Designs," SRC TECHCON, 2020.

# TASK 2810.027, MEASUREMENT AND MODELING OF STRESS/STRAIN ON ANALOG TRANSISTOR AND CIRCUIT PARAMETERS

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## SIGNIFICANCE AND OBJECTIVES

Packaging of electronic devices introduces compressive biaxial stress and variable vertical stress due to silicon particles in the epoxy. We show that due to the non-linear nature of the intrinsic carrier concentration, compressive biaxial stress (a common type in most commercial packages) is disadvantageous to bipolar device variability. Significantly improved matching could be obtained if transistors were packaged with tensile stress. PNP transistors are also shown to be less affected by packaging stress

## TECHNICAL APPROACH

The BJT matching due to packaging stress is modeled using device simulation. The BJT shift for analog transistors will be measured using a 4-point bending flexure wafer bending jig. Measurements and modeling are compared.

## SUMMARY OF RESULTS

The goal is to develop a detailed understanding of packaging stress that results in voltage offset for a typical differential amplifier circuit (see Fig. 1).

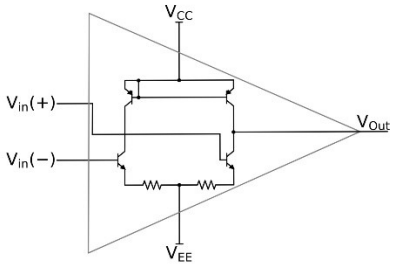


**Figure 1. Example matching circuit.**

Using wafer bending and simulations we show collector current due to stress can be approximated by a summation due to the change in intrinsic carrier concentration and mobility:

$$I_s = \frac{k_B T}{q}\frac{A}{W}\sigma^{Minority} = \frac{k_B T}{q}\frac{A}{W} * \frac{q}{N_{Majority}} n_i^2 \mu \quad (1)$$

$$\frac{\Delta I_c}{I_c} = \frac{\Delta I_s}{I_s} = \frac{\Delta(n_i^2\mu)}{n_i^2\mu} \approx \frac{\Delta\mu}{\mu} + \frac{\Delta n_i^2}{n_i^2} \quad (2)$$

We show that PNP (vs NPN) transistors are less sensitive to packaging stress. NPN and other transistors with built-in global packaging compressive stress are more sensitive to silica filler particle stress. Key data to support these claims is shown in Figs. 1-3.

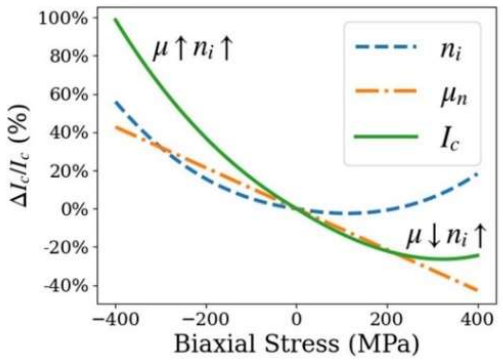


**Figure 1. Change in collector current vs package stress.**

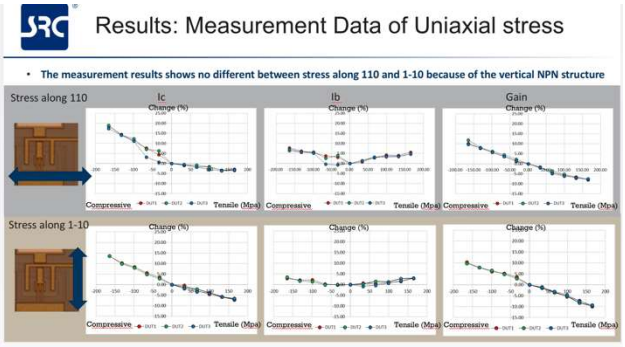


**Figure 2. Changes in NPN transistor characterisitics for 110 and 1-10 compressive and tensile stress.**

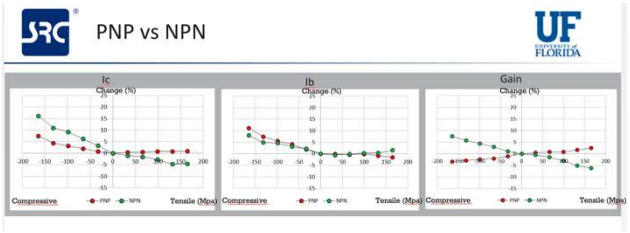


**Figure 3. Stress results for NPN and PNP transistors.**

**Keywords:** strained Silicon, BJT matching, packaging stress

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] "Negative Impact of Compressive Biaxial Stress on High Precision Bipolar Devices," submitted to EDL May 2020.

# TASK 2810.038, EXTREME TEMPERATURE DIGITAL, ANALOG, AND MIXED-SIGNAL CIRCUITS (ET-DAMS)

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## SIGNIFICANCE AND OBJECTIVES

An array-based, densely populated transistor characterization circuit is implemented in a 0.35-µm process. An on-chip heater is designed to raise the die to an extremely high temperature using snake-shaped M3 wire. An M1-based temperature sensor is designed under the heater to characterize the heat distribution.

## TECHNICAL APPROACH

An array-based transistor characterization circuit is implemented in an individually addressable manner to efficiently stress the transistor for HCI and BTI degradation and measure the transistor I-V behavior under extreme temperature. With regards to the heating method, the traditional oven-based heating method is usually limited by its temperature range (our target is 200°C and higher), and local and fine-grain temperature control. We have implemented a metal-based, small-sized on-chip heater to help us reach the target temperature using joule-heating. In this work, we proposed to use a M1 resistance-based temperature measurement method.

## SUMMARY OF RESULTS

Fig. 1 (top) shows the schematic of the device array. Both NMOS and PMOS array contains 6,144 transistors, with 64 transistors in each column and 96 columns in total. To minimize the leakage current under extremely high temperatures, which might influence the measurement accuracy, we adopted the test structure introduced by IBM for local mismatch measurement. Transistors from the same row share one source line, and transistors from the same column share the gate and drain lines. Two drivers are placed at both top and bottom of each column to minimize the voltage drop introduced by the parasitic resistance of the wire. The small height of the array can also limit the voltage difference across the wire. Current measure switches are placed at one side of the array. Current from the selected row will flow into the $I_{measure}$ path, and current from the unselected row will flow into the $I_{sink}$ path to ensure measurement accuracy. Voltage measure switches are placed on the other side of the array. Since the current will be flowing in one direction, the source voltage could be measured accurately by activating the voltage measure switch. The driver units have three operation modes. It can drive voltage to the desired value when selected or clamp voltage to the desired value when not selected. It can also sense the voltage of the selected gate/drain line. Fig. 1 (bottom) shows the full chip layout of the chip that was taped out in October 2020.

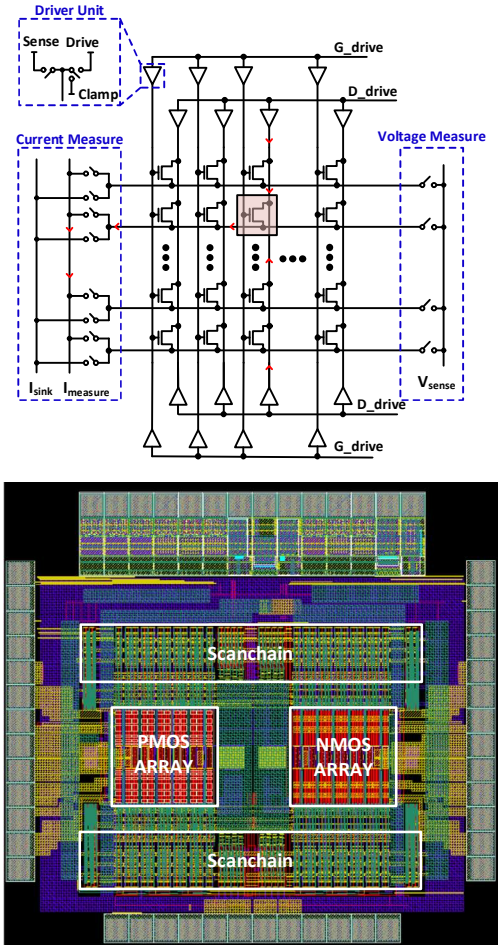


**Figure 1. (top) Device characterization array schematic, (bottom) Full chip layout.**

**Keywords:** High temperature, device characterization, on-chip heater, local mismatch, test chip

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] H. Yu, G. Park, and C.H. Kim, "Extreme Temperature Characterization of Amplifier Response Up to 300 Degrees Celsius Using Integrated…," ESSCIRC, 2021 (to appear, chip design was supported by Task 2712.017 (expired), testing was supported by this task)

# TASK 2810.041, ESD PROTECTION FOR IO OPERATING AT 56 GB/S AND BEYOND

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## SIGNIFICANCE AND OBJECTIVES

The project objective is to develop a co-design methodology for ESD-protected front-end circuits in receivers that employ PAM4 signaling. This will enable a designer to achieve adequate component-level ESD protection without increasing the required equalization.

## TECHNICAL APPROACH

A four-pronged technical approach has been developed. First, ESD hazards arising from a variety of bandwidth extension techniques are identified. The second step is to identify the $V_{MAX}$ for each circuit topology under consideration, where $V_{MAX}$ is the maximum tolerable voltage at the IO pin under ESD conditions. Generally, the designer has multiple receiver topologies to choose between. Third, the available protection devices are characterized using the metric $I_{fail}$/Capacitance and $R_{on}$*Capacitance. Finally, the performance and reliability of each candidate circuit are optimized through co-design. Much of the work is carried out using analysis and circuit simulation, but test chip fabrication and measurement will be used for proof of concept.

## SUMMARY OF RESULTS

It is customary to use a continuous-time linear equalizer (CTLE) as the front-end receiver circuit. In the advanced process nodes used for high-speed signaling, an inverter-based design may offer power and area advantages over the more established analog circuit implementation of a CTLE. Using ESD circuit simulation, we found that the voltage stress applied to the gate dielectric of the input transistor(s) is significantly larger for the inverter-based CTLE; therefore, larger input protection devices must be used for the inverter-based design. A more optimal balance of performance and reliability can be achieved by using an analog CTLE.

The ESD robustness of both CTLE designs can be improved further by the addition of control circuitry and without compromising performance. Increasing the circuit's ESD intrinsic robustness allows one to downsize the protection devices, potentially resulting in enhanced performance. The added circuits control the bias applied to the gates of certain transistors in the CTLE during an ESD event. Those transistors lie off the main signal path. The energy of the ESD discharge is used to power on the control circuitry. Proof of concept has been established using circuit simulation of designs executed in a 65-nm PDK. Those findings will be verified by test chip measurements. A Fall 2021 tapeout is expected.

Bias conditioning circuits have a finite turn-on delay, typically about 100 ps. The gate oxide stress is elevated during the turn-on. The quantitative effect of a very-short duration stress cannot be determined on the basis of data included in a PDK. Therefore, the dielectric wearout will be investigated by physical experiments, using test structures included on the test chip.

Without codesign and bias conditioning, the achievable ESD levels will decrease as data rates increase. This is shown in Fig. 1. It has not been established that high yield is achievable at CDM levels less than 200-V and thus the codesign approach described here is attractive.

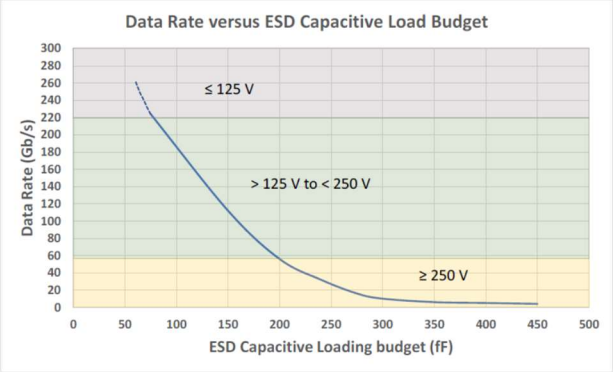


**Figure 1. Using existing design methods, the Industry Council on ESD Target Levels (White Paper 2, Rev. 3.0, 2021) postulates a fixed relationship between data rate and allowable capacitance ($C_{ESD}$), as well as a fixed relationship between $C_{ESD}$ and the achievable protection level**

**Keywords:** SerDes, PAM4, CDM, ESD

## INDUSTRY INTERACTIONS

Texas Instruments, IBM, Intel

## MAJOR PAPERS/PATENTS

# TASK 2810.046, GENERATING CURRENT CONSTRAINTS FOR ELECTROMIGRATION SAFETY

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## SIGNIFICANCE AND OBJECTIVES

We focus on electromigration (EM) failures in on-chip metal lines and are developing tools to guarantee chip robustness in the face of EM degradation. Our goal is to provide techniques by which one can ensure EM reliability-by-design. The key advantage is improved accuracy and reduced conservatism.

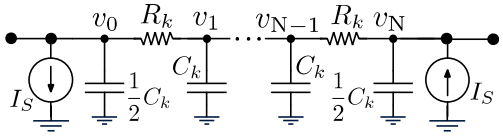
## TECHNICAL APPROACH

It is difficult to achieve EM sign-off on modern chip designs, due to the limitations of traditional empirical models that are built into existing tools. Modern physical EM models allow one to overcome this limitation, but are expensive to use, especially when doing EM simulation on large chip power grids. Instead of simulation, we will develop an "inverse approach": generate design-aware constraints on the circuit currents which, if guaranteed during chip design, would ensure EM safety for the desired lifetime. Since these constraints correspond to the specific design, this has the potential to improve accuracy and reduce pessimism.

## SUMMARY OF RESULTS

A physical model for EM was proposed in 1993 that describes the evolution over time of the mechanical stress (built-up internal pressure) in a metal line under high enough current density. This stress is the root cause of EM failures. Based on this, we had previously developed a linear (LTI) system that describes the time-evolution of the stress vector as a function of line currents. In the "forward" approach, we have previously used this to build a simulation engine for tracking the evolution of EM over time. In the "inverse" approach, under this project, we have been developing an approach by which, given a metal network, we would generate the set of constraints on the input currents that would guarantee that the lifetime of the metal structure is within specification. There have been three key achievements this year.

First, we have discovered that the relations between stress and flux in a metal network are exactly the same as those between voltage and current in a specially designed electrical circuit (an RC network). We call this circuit an "equivalent circuit," and it can be automatically built for any given metal interconnect tree. If you solve the voltage-current problem for the equivalent circuit, you have automatically solved the stress-flux problem for the interconnect tree. For example, an one-line interconnect tree translates to the equivalent circuit shown below, which is an RC network of identical topology as the original tree. The conservation of mass in the original tree, due to the isolation from other trees, when it comes to atomic flux, translates to a conservation of charge in the equivalent circuit.




Second, by writing the steady-state nodal equations for the equivalent circuit, we have identified the "safe space" of input currents which guarantee EM safety in the steady-state. If u is the vector of input currents, **1** is the vector of all 1's, then the set of safe input vectors is given by:

$$S_\infty = \left\{u \in \mathbb{R}^m : \mathbb{1}^T u = 0 \text{ and } \left(I - \mathbb{1}\alpha^T\right) G^+ H u \leq \sigma_{\text{crit}} - \alpha^T \sigma_0 \mathbb{1}\right\}$$

where the various symbols are known vectors & matrices. The only computationally difficult part of these results is finding the matrix G+, which we can find in O(n^2) time. Our test results show that we can generate the constraints for a 400K-node tree in about 9.5 hours. This is not cheap, but the algorithm is highly parallelizable, so that each row can be computed separately and independently, and so there are lots of room to speed up the solution.

Third, for the transient case, i.e., for any given time *T* less than infinity, and based on the equivalent circuit, we have identified the "safe space" for safety at the given time T, which depends on only a single matrix exponential evaluation. The safe space is given by:

$$S(T) = \left\{u \in \mathbb{R}^m : \mathbb{1}^T u = 0 \text{ and } \left(I - e^{AT}\right) G^+ H u \leq \sigma_{\text{crit}} - e^{AT} \sigma_0\right\}$$

where exp(*AT*) is the matrix exponential, which is normally very expensive to compute. However, we have identified two approximation strategies that we believe will be quite successful: 1) we would replace the G matrix by only its diagonal, which is the familiar TICER approximation from 20 years ago for RC trees, 2) normalize the C matrix. This approach is currently under implementation.

**Keywords:** integrated circuits, electromigration, stress, reliability, current constraints.

## INDUSTRY INTERACTIONS

Mentor, A Siemens Business

## MAJOR PAPERS/PATENTS

# TASK 2810.047, ARCHITECTURE AND DFT METHODS FOR IMPROVING LIFE TIME RELIABBILTY AND FUNC. SAFETY OF ELEC. CIR. AND SYS.

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## SIGNIFICANCE AND OBJECTIVES

Increasingly more ICs are deployed in mission-critical applications to improve performance, reduce accidents, and save lives. Stringent requirements on lifetime reliability and functional safety (LRFS) are imposed but methodologies are significantly lagging for analog circuits. This project develops cost-effective DfT methods for greatly improving LRFS for analog and mixed-signal circuits.

## TECHNICAL APPROACH

We will develop a DfT architecture and multilevel monitoring and healing solutions for ensuring lifetime reliability and functional safety. Digital DfT is assumed available to check our circuits. At power-on, we will use digital-like controls and detectors to verify all-analog connectivity and topological correctness, which ensures the functionality of basic analog components. With intrinsic process matching, we then perform accurate AMS BIST and calibration. After that, various health and aging monitors will go online. A concurrent sampling strategy will enable simultaneous measurements of many health and safety conditions and will trigger recalibration and/or safety actions as necessary.

## SUMMARY OF RESULTS

We have developed digital-like DfT tests for analog circuit fault detection and fault coverage; completed design and tapeout of a wide-range temperature to digital converter; developed a digital strategy for checking all component connectivity inside a SAR ADC with capacitor DAC; developed preliminary online detectors for excessive transients, NBTI aging, and TDDB aging; developed a concurrent sampling strategy that enables simultaneous measurement of many nodes under monitoring for reliability and safety.

We have also developed a method for identifying nonlinearity errors for both DAC and ADC in a single shot with no need for external instruments. The results can be then used to calibrate both the ADC and DAC to improve their linearity and spectral performance. This can be done at every power-up, thus improving reliability by always ensuring fresh calibrated performance. Figure 1 shows that the proposed method can accurately identify the nonlinearities in both ADC and DAC, with estimation error to true nonlinearity ratio in the 1% range. Figure 2 shows the effect of using the identified nonlinearities for self-calibration of the converter, improving both SFDR and THD performance by 30 to 40 dBs.

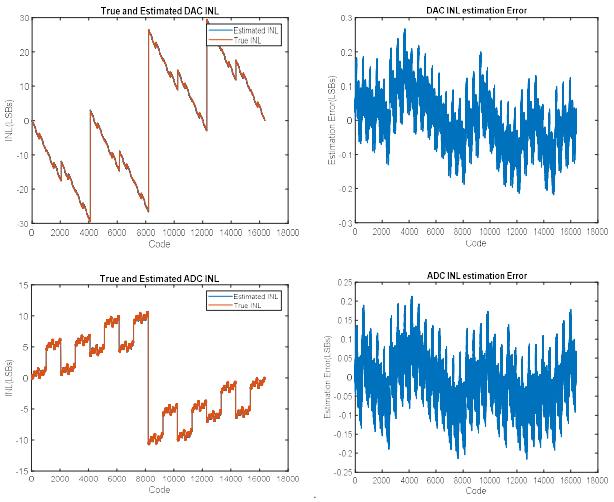


**Figure 1. Left: true and estimated DAC INL (top) and true and estimated ADC INL (bottom), Right: estimation errors.**

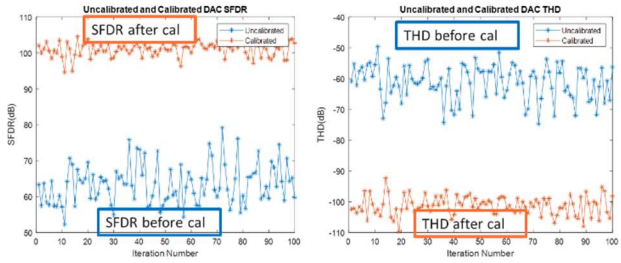


**Figure 2. The SFDR and THD performance of the converter before and after self-calibration using the estimated INL.**

In the future, we will further develop fault detection and fault coverage, with liaison interested circuits, refine the power-on test, design various aging sensors for real-time chip health condition monitoring and/or prediction, and demonstrate self-test and self-calibration of ADC/DAC without external instruments.

**Keywords**: lifetime reliability and functional safety, power-on digital-like test for analog, built-in self-test, and calibration for AMS, online health/aging monitors, online concurrent sampling of many nodes

## INDUSTRY INTERACTIONS

Texas Instruments, NXP, Intel

## MAJOR PAPERS/PATENTS

[1] Marampally Saikiran, et. al, “Robust DfT Techniques for Built-in Fault Detection in Operational Amplifiers…,” in IEEE International Test Conference (ITC), 2020.

# TASK 2810.048, CHARACTERIZATION AND MITIGATION OF ELECTROMIGRATION EFFECTS IN ADVANCED TECHNOLOGY NODES

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## SIGNIFICANCE AND OBJECTIVES

Electromigration (EM) is becoming one of the significant reliability issues in cutting-edge technologies due to higher current densities and increased Joule heating. In this work, we have taped out power-grid structures in a 28-nm technology to collect massive statistical EM data from a realistic power grid.

## TECHNICAL APPROACH

A test vehicle capable of measuring electromigration (EM) failure on a power grid is proposed. The power-grids were generated using the synthesis and placement-and-route process. A custom-designed equivalent quasi-loads were designed to replace the standard cells in the power-grids. Four designs under test (DUT) have different via and metal-grid connections to compare the EM effects with various stress bottlenecks. Metal on-chip heaters located on the heating area will raise the die temperature (> 300 °C) to accelerate the EM failure. Analog mux-based scanning circuits can monitor >1000 tapping nodes to track the voltage drop of quasi-loads and the IR drop in the power grids.

## SUMMARY OF RESULTS

Fig. 1 (Left) is an overview of a single EM test structure designed with a 28-nm CMOS process. Inside the heating area, the quasi power-grid and two on-chip metal heaters are located. While a constant current or voltage stresses the power-grid to induce EM failure, the two metal heaters will raise the power-grid temperature to facilitate the mechanism. Simultaneously, the analog mux-based scanning circuit, which is located away from the heating area, will measure the 1024 voltages inside the power-grid. Fig. 1 (Right) is the entire layout, including four different DUT structures. Since the power-grid is a rather complicated structure, including vias, metal-grids, and loads, the failure location is not definitive. Thus, four different DUTs are included to compare the EM effects on metal-grids and vias.

Fig. 2 shows the power-grid and on-chip heater design in the heating area. The quasi power-grid was first generated by a typical synthesis and PnR process. After the generation of the power-grid, the standard logic cells were selectively replaced by the equivalent quasi-loads. The two on-chip metal heaters (Fig.2 (Right)), which cover the heating area, could elevate and sustain the temperature of the quasi power-grid. Furthermore, parallel-connected M2 metal resistors (Fig.2(Left)) will be used as a temperature sensor, capable of measuring the actual DUT temperature will allow more accurate temperature control.

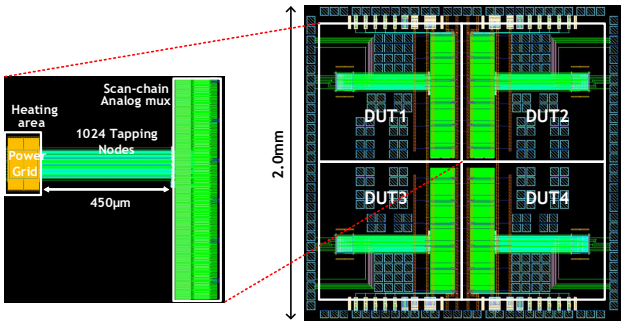


**Figure 1. (Left) Proposed 28-nm EM test-vehicle including quasi power-grid, on-chip heater, and voltage scanning circuits. (Right) 2x2mm² full-chip layout with four different DUT structures.**

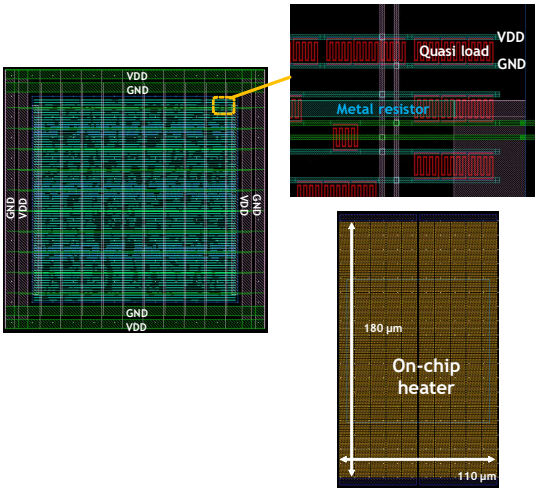


**Figure 2. (Left) Power-grid and quasi-load layout. (Right) On-chip metal heater.**

**Keywords:** Electromigration, power grid, lifetime, characterization, test structure

## INDUSTRY INTERACTIONS

Intel, Texas Instruments, Mentor, A Siemens Business

## MAJOR PAPERS/PATENTS

[1] C. Kim, "Characterization and Mitigation of Electromigration Effects in Advanced Nodes," International Interconnect Technology Conference (IITC), Oct. 2020.

# TASK 2810.050, INTEGRATING METASURFACES AND MEMS FOR GAS SENSING

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## SIGNIFICANCE AND OBJECTIVES

The goal is to demonstrate miniaturized infrared (IR) sensors operating at room temperature based on ultrathin metasurfaces (MTSs) integrated within a nanomechanical resonator system (NMEMS). The device will be optimized for gas sensing, an application whose value is expected to increase to $1B worldwide in 2022.

## TECHNICAL APPROACH

By merging tailored electromagnetic (EM) and electromechanical resonances, a miniaturized and fast IR detector operating at room temperature will be demonstrated. This device exhibits superior performance than competing technologies in terms of speed, noise, and sensitivity over a relatively narrow band in the IR. The goal is to drastically improve the selectivity of the IR resonance by optimizing the MTS nanoresonators, aiming to achieve absorption responses with a full width half maximum (FWHM) below 0.25-μm. In the next step of the project, the metasurfaces will be integrated with NMEMS resonators to demonstrate a complete gas sensing system.

## SUMMARY OF RESULTS

In close collaboration with Texas Instruments, we have designed ultrathin metasurfaces able to absorb infrared energy as the spectral fingerprints of targeted gases. Considering the dispersive response of materials in the infrared band, we have employed electromagnetic simulators to analyze and design such structures and we have developed an equivalent circuit model that will be used to accelerate the modeling of the nanostructures. We have fabricated and characterized the first set of metasurfaces based on gold nanoresonators deposited over 200nm of $SiO_2$ (Figure 1) that provide 100% absorption at the desired wavelength with an FWHM ≈ 0.25μm. Then, we have analyzed, designed, fabricated, and characterized, similar metasurfaces based on aluminum nanoresonators instead of gold. The use of aluminum is critical in this type of sensor, as this material is compatible with the fabrication processes available in commercial foundries.

Our metasurface designs can closely overlap desired spectral fingerprints of a wide variety of gases (Figure 2). Currently, we are working on integration of the metasurfaces within state-of-the-art NMEMS and on characterization of the overall system using a top-bench automated approach.

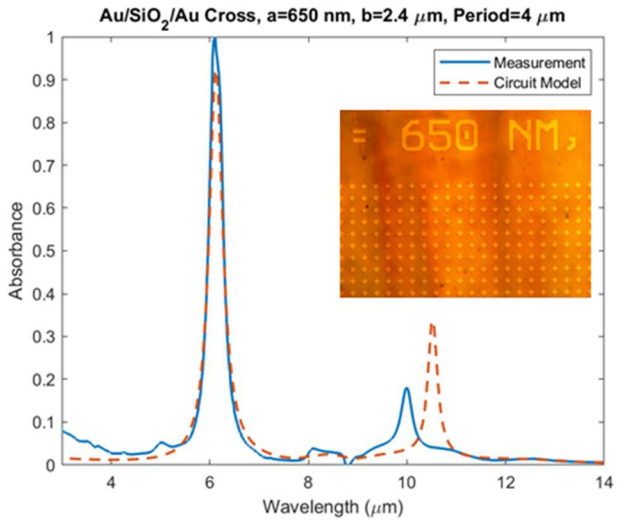


**Figure 1. Measured absorption of metasurfaces, compared to circuit model. Optical microscopy image of metasurface (inset).**

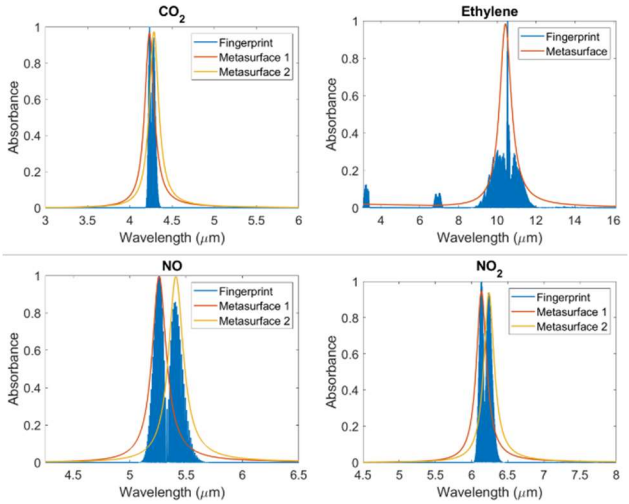


**Figure 2. Matching the spectral fingerprints of various gases using tailored ultrathin metasurfaces.**

**Keywords:** NMEMS, ultrathin metasurfaces, IR sensors, gas sensing, AlN resonators

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

# TASK 2810.051, HIGH GAIN DC-DC CONVERTER FOR EV TRACTION SYSTEM

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## SIGNIFICANCE AND OBJECTIVES

Experimental validation of the proposed multi-input, high-conversion-ratio DC-DC converter for electric vehicle traction system involving low-voltage battery pack and variable DC link voltage. The proposed architecture increases safety, minimizes cell balancing issues in batteries, eliminates the need for an auxiliary DC-DC converter, and improves the overall efficiency of the system.

## TECHNICAL APPROACH

In EV traction systems, higher voltage motors offer improved efficiency and power density. Also, variable DC link voltage has been shown to improve the overall efficiency of the traction system. The proposed multi-input high conversion ratio converter (HCRC) can achieve high and variable voltage gain (4 to 20 times for a 4-phase converter) with a significant reduction in voltage and current stress across its devices. This enables the use of a 48V battery pack which significantly increases the overall safety. Each phase of HCRC is connected to a separate battery module whose charging-discharging can be independently controlled to achieve cell balancing easily.

## SUMMARY OF RESULTS

A scaled hardware prototype of a 4-phase multi-input HCRC is developed to verify the proposed concept as shown in Figure. 1. Due to the limited testing facility availability, the prototype is rated for 4 kW operating at 48 V input voltage. The output voltage can vary from 200 V to 800 V achieving a conversion ratio of 4 to 17 without any transient spikes in switch voltage or current. The converter has two zones of operation based on the duty ratio of operation. In Zone I (duty > 0.5), the converter has inherent current sharing and low device voltage stress which is not present in Zone II (duty < 0.5) operation.

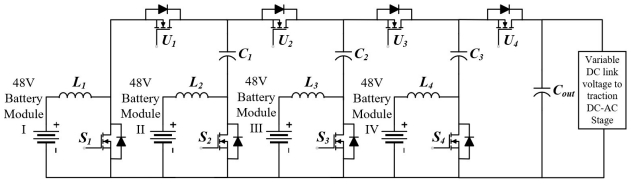


**Figure 1. Proposed 4-phase multi-input high conversion ratio converter for EV traction system.**

The hardware prototype is operated in dual-loop control with an inner current loop and outer voltage loop. The inner current loop regulates the current supplied by each input source while the voltage controller regulates the output voltage to the desired value. The converter can operate at both equal and un-equal current sharing among the different input phases over the whole range of operation with the output voltage regulated to the desired value. The converter has bi-directional power flow capability allowing it to operate in buck mode during regenerative braking in an electric vehicle. The converter operation in both boost and buck mode is verified experimentally through the hardware prototype.

The converter performance for different output voltage and power conditions in boost mode is presented in Table 1. As the converter has low voltage stress across the devices, 650-V SiC MOSFETs are selected which have low on-state resistance to minimize the conduction losses. The converter can achieve a peak efficiency of 98.24% at 48V to 400V, 2 kW. The converter has similar performance results in buck mode where it can achieve 98.16% efficiency for 400 V to 48 V operation at 2 kW, 50 kHz.

**Table 1. 4-phase HCRC performance in boost mode for 48 V input at 50 kHz switching frequency.**

| Output voltage | Output Power | Device Voltage Stress (Bottom / Top Switch) | Efficiency |
|---|---|---|---|
| 200 V | 1000 W | 200 V/ 145 V | 97.4 % |
| 400 V | 2000 W | 100 V/ 200 V | 98.24 % |
| 800 V | 4000 W | 200 V/ 400 V | 97.06 % |

The converter will be further optimized for power density by reducing the inductor size using interleaving among the different input phases which will reduce the input current ripple as well.

**Keywords:** DC-DC Converter, High Gain, Non-isolated boost, Variable DC link voltage, Electric Vehicle Traction System

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] J. Roy, A. Gupta, and R. Ayyanar, "Discontinuous Conduction Mode Analysis of High Gain Extended-Duty-Ratio Boost Converter," in IEEE Open Journal of the Industrial Electronics Society, vol. 2, pp. 372-387, 2021, DOI: 10.1109/OJIES.2021.3077982.

[2] A. Gupta, R. Ayyanar and S. Chakraborty, “Phase-Shedding Control Scheme for Wide Voltage Range Operation of Extended-Duty-Ratio Boost Converter,” Accepted to APEC 2021.

# TASK 2810.054, RECONFIGURABLE AC POWER CYCLING SETUP AND PLUG-IN CONDITION MONITORING TOOLS FOR HIGH POWER IGBT AND SIC MODULES

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## SIGNIFICANCE AND OBJECTIVES

The long-term reliability of SiC MOSFET is a concern limiting its wide application in industry. This research investigates the performance change of SiC MOSFETs over aging through the AC power cycling as the most realistic aging test. The specific precursors will be identified for Si IGBT and SiC MOSFET modules; and in-situ/online condition monitoring circuits, lifetime models, and remaining useful lifetime estimation tools will be developed.

## TECHNICAL APPROACH

Utilizing the TI UCC5870 gate driver IC, a smart gate driver board with condition monitoring (CM) circuits has been designed and fabricated. The CM circuits in the board can monitor all three main aging mechanisms. Also, the power stage of the AC power cycling setup has been designed. A three-phase laminated busbar with low stray inductance was modeled and fabricated for each inverter in the AC test setup. Also, the thermal operation of the test setup under different conditions is simulated, and based on the thermal profile, suitable cooling plates are designed and fabricated to meet the requirements.

## SUMMARY OF RESULTS

Different kinds of aging mechanisms and their condition monitoring circuits are evaluated. Based on this evaluation, a gate driver board is developed for condition monitoring purposes to determine the state-of-health of the devices in real applications (Fig. 1). The gate driver can monitor on-resistance, threshold voltage, body diode voltage, and transconductance accurately at the same time. Therefore, we can monitor package degradation, gate oxide degradation, and body diode degradation of SiC MOSFETs simultaneously. Also, all of the protection functions of TI UCC5870 are implemented to test the capability of this IC as a high-power converter. An upstream controller board is also designed to communicate with all these gate driver boards and control the back-to-back inverters currents to create AC thermal cycles.

The AC test setup is thermally simulated, and the hot points and power losses are derived. As shown in Figure 2, a custom-designed cold plate is fabricated to meet the thermal requirement in the previous step. The fabricated cold plate can withstand the max baseplate temperature of 130°C without fluid running through the system and the pressure drop for coldplate is approximately 0.4 psi without connectors.

Also, an Electroless Nickel plated two-layer laminated edge sealed bus bar is designed with low inductance to connect power modules in the power stage. As it can be seen in Figure 3, in this design DC link capacitors are distributed on the busbar to minimize stary inductance as much as possible.

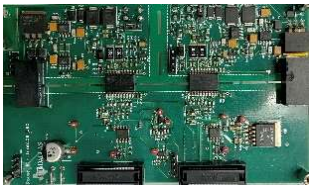

**Figure 1. The gate driver board with embedded condition monitoring systems for different aging mechanisms.**

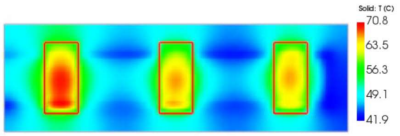


**Figure 2. Thermal performance of cooling plates at a flow rate of 4 LPM.**

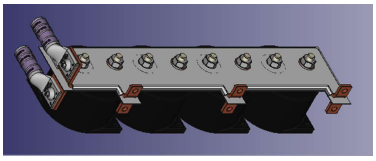

**Figure 3. 3D view of the inverter bubar for 400A and 1100V.**

**Keywords:** SiC MOSFETs, AC power cycling, performance degradation, condition monitoring, reliability

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] B. T. Vankayalapati et al., “Closed-loop Junction Temperature Control of SiC MOSFETs in DC Power Cycling for Accurate Reliability Assessments,” SDEMPED 2021, 2021, Dallas, USA.

[2] B. T. Vankayalapati et al., "A Highly Scalable, Modular Test Bench Architecture for Large-Scale DC Power Cycling of SiC MOSFETs: Towards Data Enabled Reliability," Accepted to IEEE Power Elec. Mag., 2021.

# TASK 2810.055, EMI-REGULATED SECURE AUTOMOTIVE POWER ICS

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## SIGNIFICANCE AND OBJECTIVES

With ever-growing electronic devices being employed in electric vehicles, electromagnetic interference (EMI) emission in modern automotive electronics has been record-high. The situation deteriorates further due to high dv/dt and di/dt transients, as more high-end power modules shift to adopt high-performance GaN power switches for faster and more efficient operation. The proposed techniques support effective EMI suppression and minimize switching power losses.

## TECHNICAL APPROACH

To regulate and suppress elevated EMI by automotive power ICs, spread-spectrum modulation (SSM) technique and circuit will be developed. By actively modulating switching frequencies of power circuits at multiple rates, the technique expects to shape EMI spectrum adaptively while accommodating in-cycle zero-voltage switching to accomplish a balanced EMI regulation and power control.

## SUMMARY OF RESULTS

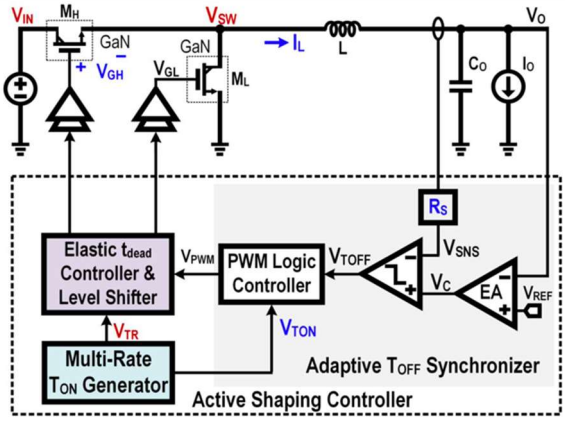


**Figure 1. Block diagram of the proposed GaN power converter.**

Fig. 1 shows the block diagram of the proposed GaN power converter. An anti-aliasing MR-SSM technique is incorporated through an active shaping controller for effective EMI reduction. To implement such, a multi-rate $T_{ON}$ generator is designed, which regulates the on-duty time ($T_{ON}$) with multiple coded rates. Compared to the classic FR-SSM, it successfully achieves a targeted redistribution of EMI energy by adapting the $f_{SW}$ modulation rate to the frequency range. Specifically, as shown in Figs. 2 and 3, a lower $f_{SW}$ is modulated with a faster rate, reducing its occurrence in the time domain. Thus, the EMI energy carried by such a frequency component and its corresponding harmonics is suppressed, eliminating the EMI power aliasing spikes, which are inevitable in the FR-SSM. Meanwhile, the off-duty time ($T_{OFF}$) is adaptively defined by an adaptive $T_{OFF}$ synchronizer. In response to a longer $T_{ON}$, $T_{OFF}$ is extended correspondingly while retaining a near-constant $T_{ON}/T_{OFF}$, and thus a near-constant $V_O$.

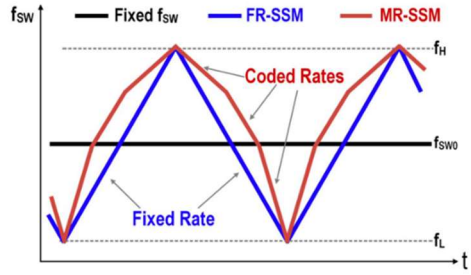


**Figure 2. Comparing MR-SSM to FR-SSM in time domain.**

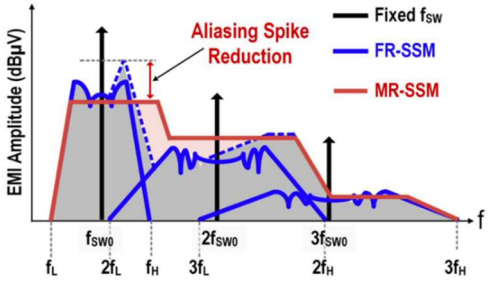


**Figure 3. Comparing MR-SSM to FR-SSM in frequency domain.**

On the other hand, as $f_{SW}$ varies continuously, ZVS operation is difficult to accomplish. Continuously varying peak and valley inductor currents induce extra switching and reverse conduction losses during switching deadtimes. Therefore, the elastic deadtime ($t_{dead}$) controller will be developed to realize in-cycle ZVS by predicting the expected inductor current.

**Keywords:** GaN, FR-SSM, EMI noise, IC security

## INDUSTRY INTERACTIONS

Texas Instruments, IBM, NXP

## MAJOR PAPERS/PATENTS

[1] D. Yan and D. B. Ma, "An Automotive-Use Battery-to-Load GaN-Based Power Converter with Anti-Aliasing Multi-Rate Spread-Spectrum Modulation and In-Cycle ZVS Switching," IEEE Symp. VLSI Circuits, Honolulu, HI, USA, Jun. 2020, pp. 1–2.

[2] D. Yan and D. B. Ma, "An Automotive-Use Battery-to-Load GaN-Based Switching Power Converter With Anti-Aliasing MR-SSM and In-Cycle Adaptive ZVS Techniques," IEEE Journal of Solid-State Circuits, Vol. 57, No. 4, pp. 1186-1196, Apr. 2021.

# TASK 2810.057, RELIABILITY STUDY OF E-MODE GAN HEMT DEVICES BY AC TDDB AND HIGH RESOLUTION TEM

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HISHASHI SHICHIJO, THE UNIVERSITY OF TEXAS AT DALLAS

## SIGNIFICANCE AND OBJECTIVES

Among various AlGaN/GaN HEMTs, normally-off E-mode GaN HEMTs with the p-GaN gate is the most attractive due to their high gate bias swing and a simpler fabrication process. This work involves "X-GaN" device structure, AC and DC TDDB, and in-situ TEM for better understanding of the failure mechanisms.

## TECHNICAL APPROACH

Commercially available "X-GaN" or "Gate Injection Transistor" E-mode GaN HEMTs were characterized for their electrical and physical characteristics. Electrical measurements include both AC and DC Time Dependent Dielectric Breakdown (TDDB) tests at various gate stressing conditions to obtain the device response and time to fail data. Physical characterization of the device before and after the breakdown is performed with high-resolution electron microscopy techniques, including in-situ TEM electrical measurements.

## SUMMARY OF RESULTS

A new p-GaN Gate Injection Transistor device was characterized by aberration-corrected scanning transmission electron microscopy (STEM), as shown in Figure 1. The distinct feature of the device is its bulky metal contacts that facilitate the high output current without damaging the contact themselves and are made of Cu-Au alloy. The device has an AlGaN/GaN structure on a Si substrate with an AlN buffer and the super-lattice structure (SLS) of AlGaN/AlN. Figure 1(b) shows the recessed p-GaN into the AlGaN layer. The measured AlGaN thickness is 66nm and 70 nm in the cap region, while it is only 18nm thick in the recess region.

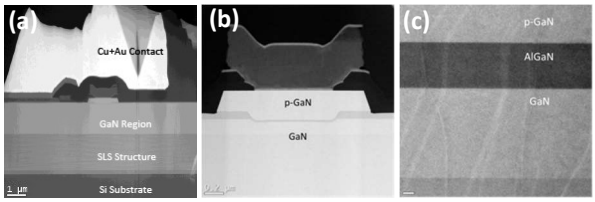


**Figure 1. (a) STEM HAADF images of the X-GaN device layers, (b) recessed p-GaN gate, and (c) p-GaN/AlGaN/GaN below the gate cap.**

These gate injection E-Mode GaN HEMT transistors with hybrid drain configuration (HD-GIT) were tested for static gate stress, constant voltage stress (CVS), and constant current stress (CCS). Devices were subjected to CV & CC stress to induce time-dependent breakdown. Figure 2(a) shows CV stress data for the devices stressed at a gate voltage of 7V with the occurrence of breakdown indicated by an increase in the recorded $I_G$ values. The device shows a stable operation, and the time to fail is approximately dependent on the operating voltage. Figures 2(b) and (c) show the CC stress data for HD-GIT devices, which were stressed at 1 A and 1.25 A, respectively. The time to fail is strongly dependent on stress current, unlike weak voltage dependence in CV stress.

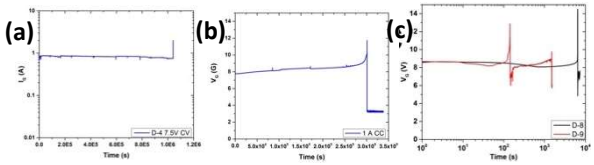


**Figure 2. Constant voltage (a) and Constant current (b,c) stress data for the HD-GiT device.**

A new design of an in-situ electrical biasing sample is being made for two probe biasing inside a TEM. The in-situ test sample has source and gate contacts, and the source is further extended using Pt deposition, which is to be connected to the Copper TEM grid. The active probe will be used for applying a voltage to the gate, and the source will be zeroed. Figure 3 shows the new design structure of the two-probe system.

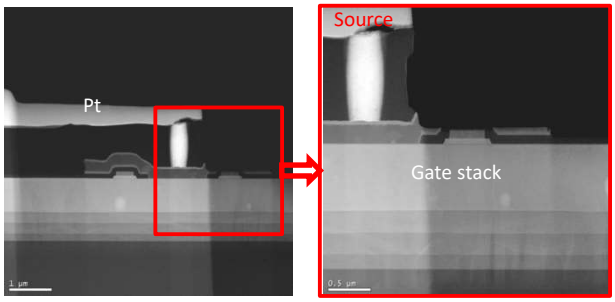


**Figure 3. STEM images of new two probe design for in-situ TEM electrical biasing of E-mode GaN HEMT devices.**

**Keywords:** E-mode GaN HEMT device, Reliability, in-situ TEM probing

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

# TASK 2810.058, MACHINE LEARNING-BASED OVERKILL/UNDERKILL REDUCTION IN ANALOG/RF IC TESTING

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## SIGNIFICANCE AND OBJECTIVES

With the rising complexity of semiconductor devices, testing procedures have become complex and time-consuming. Depending on the nature of the test solution, some good chips will be discarded (overkill) or some defective chips being retained (underkill). We exploit machine learning-based solutions to develop a comprehensive yield management scheme.

## TECHNICAL APPROACH

For the problem of overkill, we propose a multivariate regression-based solution that predicts the values of empirically defined test measurements. We take advantage of the correlation among different test measurements and use the tests that are part of product specifications as predictors. For underkill, we use the devices probe test measurements across multiple insertions as predictors and train a one-class classifier to identify devices that may fail on-site and end up being a customer return. Due to the vastness of probe test measurements, we first subject them to agglomerative feature reduction and then employ the classifier.

## SUMMARY OF RESULTS

For overkill, an industrial dataset of 92,022 devices with measurements from 66 tests that are part of product specification and 241 tests that are empirically defined is utilized. The dataset was provided by Texas Instruments Inc. Out of the 92,022 devices, 9.6% of devices fall on our focus group which passes the product specification tests but fails tests that are empirically defined. We used the 87.21% of devices that pass both sets of tests as our predictors in our regression model to predict the 241 test measurements' values for the 9.6% of the devices.

**Table 1. Test Outcome after Regression.**

| | | Tests part of Product Specification | |
|---|---|---|---|
| | | **Pass** | **Fail** |
| **Empirically defined tests** | **Pass** | 80,261 **+ 7953** | **887** |
| | **Fail** | 726 | 2195 |

Based on Table 1, we can observe that before regression the 8,840 devices that fail empirically defined tests and pass all the tests that are product specification but were still discarded as fail. After regression and based on the predicted values, we were able to recover around 7,953 devices and move them back to the group where they pass both sets of tests. We are currently exploring ways to verify our results since there is no existing ground truth.

For underkill, an industrial dataset of 24,000 devices was provided by Texas Instruments Inc. The dataset consisted of 19 customer returns and each of these can be further classified into different fault-id. Due to the limited customer return data, we generate synthetic instances of customer returns to train the classifier for each fault ID.

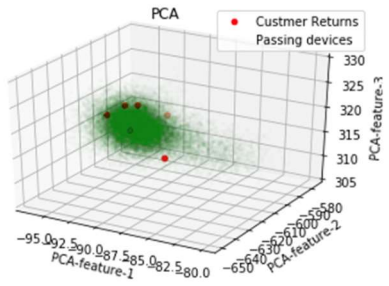


**Figure 1. Classification of customer returns for Fault ID 1.**

From the confusion matrix in Table 2, for fault-id 1, we get an accuracy of 90.7% for the classifier and this resulted in 81.56% of the customer returns being classified accurately. Similarly, results were observed for other fault IDs as well.

**Table 2. Confusion Matrix of Fault ID = 1 – Classification.**

| | **Customer Returns** | **Passing Devices** |
|---|---|---|
| **Customer Returns** | 6551 | 1481 |
| **Passing Devices** | 0 | 8011 |

We presented two adaptive, machine learning-based approaches to address the problems of overkill and underkill. We are working on verifying the results and exploring unsupervised learning solutions as well.

**Keywords:** adaptive test, post-silicon calibration, machine learning

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] D. Neethirajan, V. A. Niranjan, D. Webster, A. Nahar and Y. Makris, "Machine Learning-Based Overkill Reduction through Inter-Probe Test Correlation." (Conference paper in preparation)

# TASK 2810.064, CHARACTERIZATION AND TOLERANCE OF AGEING IN INTEGRATED VOLTAGE REGULATORS

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## SIGNIFICANCE AND OBJECTIVES

The project will develop circuit techniques and design methodologies to model, characterize and tolerate ageing in integrated voltage regulators, including on-chip inductive buck and digital low dropout regulators, used in modern SoCs.

## TECHNICAL APPROACH

The objectives of this research are to analyze the effects of ageing in IVRs, design a test circuit to efficiently characterize ageing in IVRs, estimate ageing-induced design margin for IVR and develop circuit techniques to tolerate ageing, and explore online tuning for tolerating ageing in IVRs. We will focus on high-frequency inductive buck regulators and DLDOs, both with digital voltage-mode control topologies.

## SUMMARY OF RESULTS

Our prior work has analyzed the effect of BTI-induced ageing on transient performances of DLDO and buck regulators [1-2]. We have developed a simulation methodology that coupled analytically computed threshold voltage ($V_{th}$) shifts of transistors (130nm/65nm CMOS), SPICE simulations-based estimation of shifts in the power stage on-resistance ($\Delta R_{on}$) and critical path delay (and maximum sampling frequency, $\Delta F_{samp}$ ) of the compensator, and Simulink based time and frequency domain model of buck and DLDO [1-2]. The coupled model was used to estimate degradations in transient performance (load transient) and efficiency. The simulation results were further validated with measured data from test chips in 130-nm and 65-nm CMOS [1-2] (Fig. 1). We observed that power stage ageing has a limited effect on the performance of buck regulators as power devices switch continuously and performance is dominated by the LC pole. On the other hand, as PMOS's are continuously on in a DLDO and performance is dominated by RC pole at the output, the transient performance is strongly impacted by power stage ageing (Fig. 2). The simulation of controller ageing has shown a similar impact for both buck and DLDO. We observed that, in high frequency (~100s MHz) IVRs, ageing-induced shifts in the $V_{th}$ and delay of the critical path can induce appreciable change in the transient performance (Fig. 3). The preliminary analysis shows the need for considering ageing as an important aspect of the design of high-frequency IVRs for modern SoC's.

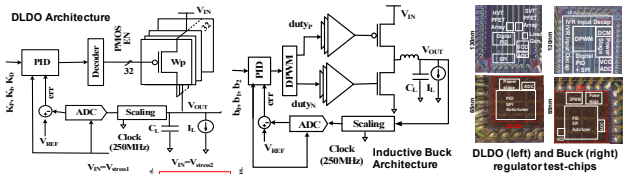


**Figure 1. Our prior test chip was designed in 130nm and 65nm CMOS to characterize the effect of BTI.**

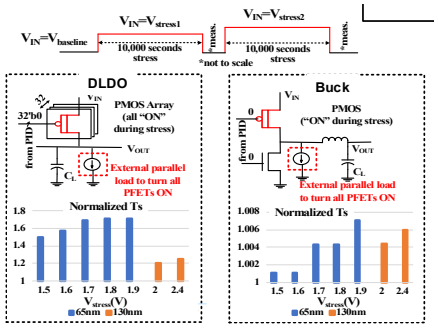


**Figure 2. Measurement results showing the effect of BTI ageing of the power stage.**

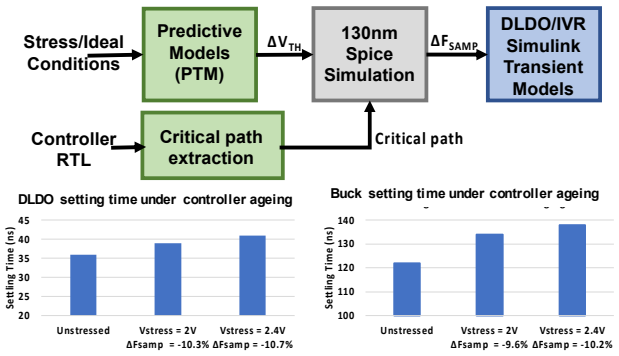


**Figure 3. Simulation results showing transient performance considering BTI-induced ageing of the controller.**

**Keywords:** Integrated voltage regulator, ageing

## INDUSTRY INTERACTIONS

Intel, IBM

## MAJOR PAPERS/PATENTS

[1] V. Chekuri, et. al., "On the Effect of NBTI Induced Ageing of Power Stage on the Transient Performance of On-Chip Voltage Regulators," IEEE International Reliability Physics Symposium (IRPS), 2019.

[2] V. C. K. Chekuri, et. al., "Ageing Challenges in On-chip Voltage Regulator Design," IEEE International Reliability Physics Symposium (IRPS), 2020.

# TASK 2810.065, POWER-EFFICIENT AND RELIABLE 48-V DC-DC CONVERTER WITH DIRECT SIGNAL-TO-FEATURE EXTRACTION AND DNN-ASSISTED MULTI-INPUT MULTIPLE-OUTPUT FEEDBACK CONTROL

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## SIGNIFICANCE AND OBJECTIVES

The goal of the project is to embed deep-neural-network (DNN) assisted digital feedback control systems for a 48V DC-DC converter for the data center application. The proposed control systems will enable two sought-after capabilities, namely the maximum PCE point tracking, and the in-field reliability diagnostics and remedy while consuming a small amount of hardware and energy.

## TECHNICAL APPROACH

We will develop mainly two features. First, we will design a digital DNN-assisted controller for tracking the maximum power conversion efficiency (PCE) point. It will take multiple inputs such as average load levels in the past and present monitoring windows. Then, it modulates several parameters such as duty cycle, switching frequency, dead zones, and switch widths. Second, we will develop long-term reliability diagnostics. We will focus on the long-term degradation of output capacitors and power switches. Capacitor aging, for example, induces an effective series resistance increase. To track them we will monitor the power spectral density of the output voltage. To reduce hardware overhead, we will recycle the hardware for the two features.

## SUMMARY OF RESULTS

We have first reviewed, compared the published 48V-to-1V converter topologies. Then, we have chosen and designed the 20-level series capacitor typology (Fig. 1). We augmented it with the gate width modulation technique to enable high PCE over a range of load current.

The multi-level series capacitor buck converter is chosen due to its lower power loss due to switch devices. By introducing series capacitors at each level, we can divide the converter with a high step-down ratio into multiple sub-converters with a lower step-down ratio. This allows each sub-converter to employ the *on-chip* power FETs which have superior figure-of-merits (FoM) than *off-chip* counterparts. This results in smaller conduction and switching loss and high PCE.

We chose the number of levels to be 20 to optimize the power loss while avoiding the short-circuit current in the high-side switches. Fewer levels would (i) increase the voltage tolerance requirement of switches, (ii) enlarge the current in each sub-converter, and (iii) require additional LDOs to regulate switch drivers' power supply. They all increase power loss. On the other hand, more levels would have a high risk of causing on-time overlapping in the high-side switches.

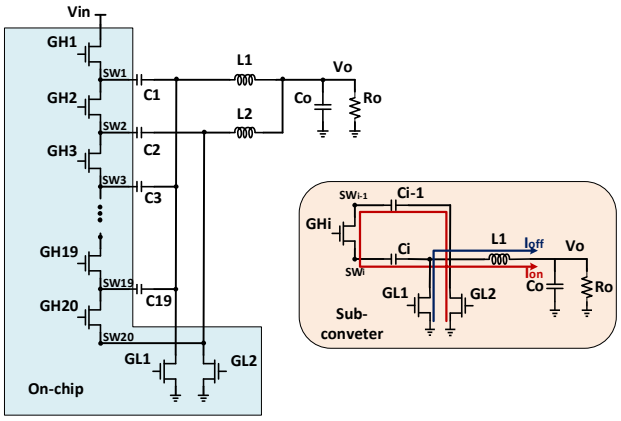


**Figure 1. (left) 20-level series-capacitor buck converter architecture; (right) A sub-converter for each level.**

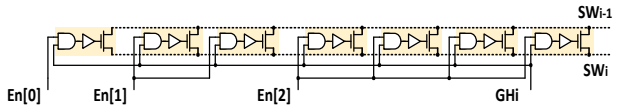


**Figure 2. Gate width modulation technique, one switch is divided into 7 segments.**

To keep a high PCE over a range of load current, we have investigated the trade-off between the conduction loss and driver loss at a different load level through the gate width modulation (Fig. 2). By controlling the enable bits, *En[2:0]*, we can increase the switch width at heavy load to reduce the conduction loss, while decreasing the switch width to reduce the driver loss at light load.

**Keywords:** Multi-level series capacitor buck converter, gate width modulation, power conversion efficiency (PCE)

## INDUSTRY INTERACTIONS

IBM, Intel, Texas Instruments

## MAJOR PAPERS/PATENTS

# TASK 2810.066, DEMONSTRABLY GENERALIZABLE COMPACT MODELS OF ESD DEVICES

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## SIGNIFICANCE AND OBJECTIVES

This project will develop methodologies for creating charge-based compact models of ESD protection devices and verifying that the model correctly represents the device's response to arbitrary stimuli. This will allow designers to use simulation to create protection circuits that can protect circuits in advanced nodes without compromising signal integrity.

## TECHNICAL APPROACH

Using a charge-based approach, compact models suitable for both transient and AC analysis will be developed. Dual-purpose devices, e.g. MOSFETs, are used both in the functional circuits and the on-chip protection networks. For those devices, we will demonstrate ESD shell models that do not compromise the accuracy of AC and transient simulations of the normal operating conditions. Transient models of ESD devices will be validated using waveforms that are different from those used for parameter extraction, and this work will develop measurement setups to produce those stimuli. Package models suitable for circuit simulation of CDM-ESD will be created.

## SUMMARY OF RESULTS

A previously developed non-quasi static model of the P-well ESD diode was modified to properly represent the long-tail of the reverse recovery current transient. Specifically, we split the device into one short base diode and one longer base diode; under the high-level injection conditions characteristic of ESD, excess minority charge is stored deep in the well, and the relatively slow removal of those charges is the source of the "tail" current. A reverse bias develops across the junction long before the reverse current subsides to its final "leakage current" value, and measurements reveal that the current undergoes avalanche multiplication following a nanosecond-scale delay. The new model includes a representation of time-delayed avalanche multiplication.

A measurement setup that produces decaying sinusoidal pulses was used to validate the model predictions. In the simulation, the model correctly represents the device dynamics when the applied bias is switched from forward to reverse and back to forward bias again.

New test structures have been designed and are currently being fabricated. Those devices will be used to extend the work to N-well diodes, which contain a parasitic PNP, and to investigate the off-state AC representation of the ESD diodes.

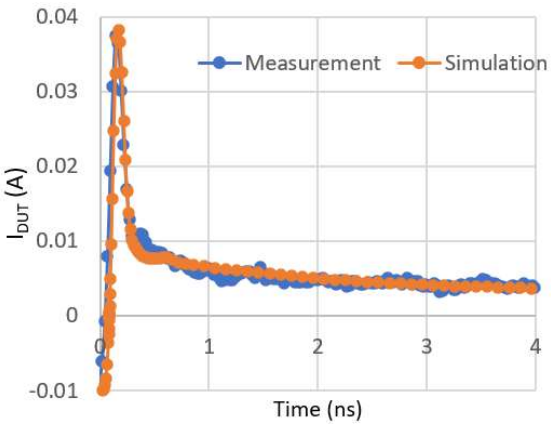


**Figure 1. Measured and simulated reverse recovery transient. 8 V reverse pulse; 10 mA initial forward current.**

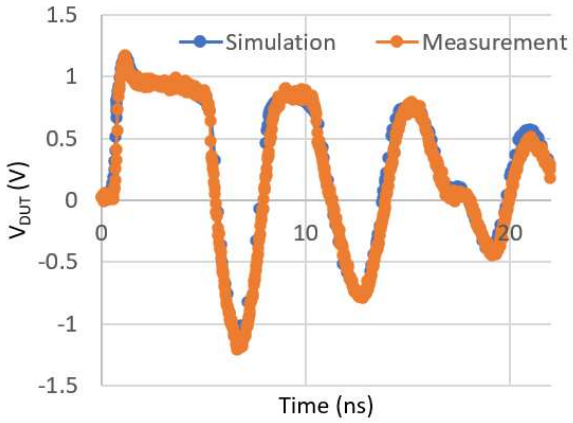


**Figure 2. Measured and simulated responses of an ESD diode to an oscillatory TLP (Transmission Line Pulse) stimulus.**

**Keywords:** ESD, compact models, circuit simulation

## INDUSTRY INTERACTIONS

AMD, NXP

## MAJOR PAPERS/PATENTS

[1] S. Huang and E. Rosenbaum, "Compact model of ESD diode suitable for sub-nanosecond switching transients," in Proc. *2021 IRPS*.

# TASK 2810.070, EARLY AND LATE LIFE FAILURE PREDICTION METHODS FOR ANALOG AND MIXED-SIGNAL CIRCUITS

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## SIGNIFICANCE AND OBJECTIVES

One of the goals of this task is to develop a synthesizable odometer IP for effectively monitoring long-term aging in a real IC product. In addition to the circuit implementation, we will address practical design issues such as the communication protocol, building a system of odometer IPs, and firmware support.

## TECHNICAL APPROACH

We have developed a synthesizable odometer IP that can be implemented using standard EDA tools. Our previous odometers were designed for understanding fundamental aspects of circuit aging, requiring many external analogs and digital control signals. In contrast, the focus of this work is on demonstrating a commercial odometer IP block that can be readily plugged into a large system-on-chip with no connection to the outside world except for the clock and data communication channel with the CPU.

## SUMMARY OF RESULTS

Figure 1 shows the different Verilog codes written for the odometer circuit. Apart from the ring oscillator and local power gating circuit, the odometer block was implemented using behavioral Verilog language which makes it easy to migrate to another process technology. Different modes of the odometer circuit operation such as calibration, stress, and measurement, were handled entirely by a simple digital interface, which necessitated critical modifications to the previous academic-style odometer design. The user can customize the type of gate (INV, NOR, NAND), technology flavor (low Vt, regular Vt, high Vt), the ring oscillator length and sizing, and the number of instances, based on the area and power constraints of the specific application. Although the previous odometer designs utilize mostly digital gates, certain internal operations such as the ring oscillator frequency trimming were implemented using capacitors and switches, which requires manual layout effort. For a fully synthesizable design, we converted these analog circuits to standard digital gate-based designs. One specific challenge was the design of the programmable power gating block for trimming the initial beat frequency count to attain high resolution (e.g. few picoseconds) and wide dynamic range (e.g. 10% frequency shift). A new power control circuit using layouts from the standard cell library allowed us to program the virtual supply voltage of the ring oscillators for high resolution and wide dynamic range. Figure 2 (upper) shows a single odometer block implemented using standard EDA tools in a 22-nm FinFET technology. The odometer IPs were daisy chained as shown in Figure 2 (lower) so that statistically significant aging data can be collected from different ring oscillator types. The chip was taped out.

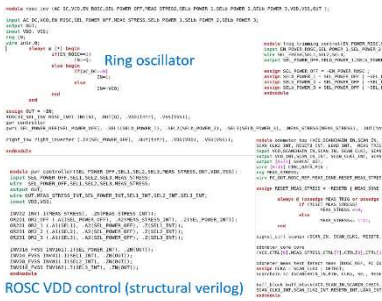


**Figure 1. Silicon odometer circuit written in behavioral and structural Verilog for physical design tools.**

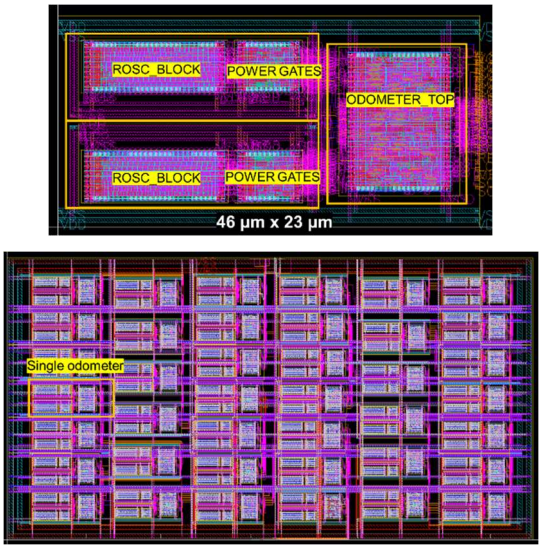


**Figure 2. (Upper) Single odometer block synthesized and automatically placed and routed using standard EDA tools in a 22-nm FinFET technology. (Lower) 40 odometers daisy chained for massive aging data collection.**

**Keywords:** Silicon odometer, synthesizable, Verilog, automatic place and route, 22nm test chip

## INDUSTRY INTERACTIONS

NXP, Intel

## MAJOR PAPERS/PATENTS

# TASK 2810.074, THERMAL PERFORMANCE CHARACTERIZATION AND DEGRADATION MONITORING OF LDMOS BASED INTEGRATED POWER IC WITH ON-DIE TEMPERATURE SENSORS

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## SIGNIFICANCE AND OBJECTIVES

Power integration is pivotal to achieve aggressive performance targets in high-performance circuits. This research aims to investigate the static and dynamic thermal performance and degradation of LDMOS using on-die temperature sensors under high voltage, high current, and high junction temperature conditions.

## TECHNICAL APPROACH

The power MOSFETs are stressed into the avalanche breakdown region by a customized current pulse generator (CPG) under two different pulse widths, i.e., short and long pulses, to differentiate the die-related and package-related degradation. The parameter shifts are recorded over the aging cycling process to compare the performance degradation and detect aging precursors under both stress conditions. Finally, failure analysis is conducted on the failed devices under two conditions to reveal different failure mechanisms.

## SUMMARY OF RESULTS

A high-resolution and cost-effective nanosecond current pulse generator (CPG) is proposed as indicated in Figure 1. Short current pulses can be generated in the order of 100 picoseconds where the magnitude and duration of the current pulse width can be adjusted precisely. The device under test (DUT) is charged up by the current into avalanche breakdown.

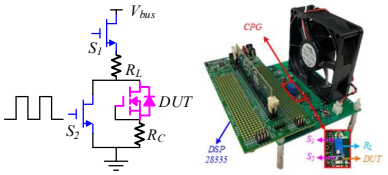


**Figure 1. Proposed current pulse generator.**

During the aging process, devices are tested under 2 A repetitive current strike with two different pulse durations, namely, 10 ns and 100 ms. All the devices show a gradual increase in the on-state resistance; however, the root causes are different, which is verified by the body diode voltage drops ($V_f$) under both high and low current. For the short pulse test, the changes in $V_f$ keep the same for both high and low current, which indicates there is no degradation in the package. On the other hand, for the long pulse test, $V_f$ shows an increase at high current and no changes at low current as given in Figure 2, which suggests the degradation located in the package. The assumption is verified by the on-state resistance difference $\Delta R_{ds,on}$ between fresh and aged devices under different gate-source voltages $V_{gs}$ as plotted in Figure 3.

Therefore, different pulse duration stresses trigger different degradation mechanisms. For the short-pulse stress, the die-related degradation is more significant. For the long pulse stress, the package-related degradation caused by high-temperature swing is the main reason for device degradation. Though all the DUTs show a short circuit failure, the failure mechanisms are different as revealed by the decapsulation shown in Figure 4. Electrical stress and thermal stress are the main causes for the short and long pulse stress, respectively.

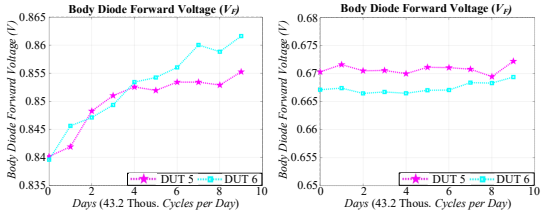


**Figure 2. $V_f$ under high (left) and low (right) current.**

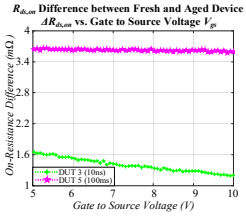


**Figure 3. On-state resistance difference between fresh and aged device vs. gate to source voltage.**

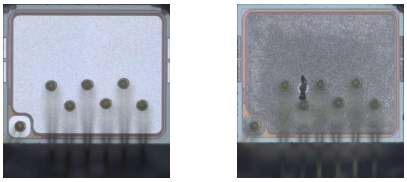

**Figure 4. Decapsulated image of the DUTs under long (left) and short (right) pulse stress.**

**Keywords:** Power MOSFETs, reliability, avalanche breakdown, degradation mechanisms, an aging precursor

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] C. Xu et al., "Performance Degradation of Automotive Power MOSFETs Under Repetitive Avalanche Breakdown Test," in *IEEE Trans. Transp. Electrific*.

# TASK 2810.077, INCREASING LIFETIME OF NANO-SCALE CMOS CIRCUITS

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## SIGNIFICANCE AND OBJECTIVES

This research seeks to increase lifetime and to enable circuit operation closer to the reliability limit to improve performance. To reduce complexity and cost approaches to estimate the noise degradation using surrogate sensors will be investigated. This research may provide a step toward a framework for predicting time to failure.

## TECHNICAL APPROACH

Noting that the aging of nano-scale transistors is highly variable, and noise is one of the most sensitive parameters to transistor aging, this research will investigate the feasibility of increasing the lifetime of circuits by monitoring noise performance degradation and intelligent circuit reconfiguration. More specifically, downconverters using arrays of near minimum size transistors that can be used for post-fabrication selection of a subset to reduce noise will be utilized. The feasibility of replacing the transistors with increased noise due to aging with fresh transistors that have lower noise to recover the circuit noise performance will be evaluated.

## SUMMARY OF RESULTS

This research effort involving collaboration with Prof. Y. Makris of UT Dallas and Prof. C. Kim of U. of Minnesota is a new task that started early this year. A more detailed research plan is discussed in this section. To experimentally evaluate the initial feasibility to increase lifetime by replacing the degraded devices with low noise devices that are not aged, the existing PLL (Fig. 1) and mixer circuits will be stressed using high voltage and the degradation of low-frequency noise on individual cells as well as the noise performance of the entire circuits will be characterized. The circuit-level degradation will be correlated with the low-frequency noise degradation of individual cells. The sensitivity of the degradation of these circuits to the current, supply voltage, temperature, and others will be investigated.

To ensure that the proposed technique applies to the circuits with the leading-edge performance, the downconverter will be refined to improve its performance. The technique will also be applied to the baseband amplifier of down converters. The circuits will be fabricated in the UMC 65-nm CMOS. The sensors for critical factors affecting degradation will be incorporated with the down converter and used to track the stress history of the circuits during normal operation and accelerated stress testing. This project will investigate genetic algorithms to select an optimal combination while minimizing the number of measurements.

Printed circuit boards including a microcontroller and an ADC, which automate the monitoring of the degradation of down converter and the measurement circuits will be constructed and utilized for collection of history of stress over time from a large number of samples as possible during normal operation and accelerated stress testing. Prediction of degradation based on accelerated testing will be compared to that of degradation during normal operation. The data will be used to develop a machine learning model for the dependence of noise performance degradation on surrogate measurements (e.g., peak and average current, voltage, temperature and others) to define aging monitoring strategies that are more straightforward and lower cost.

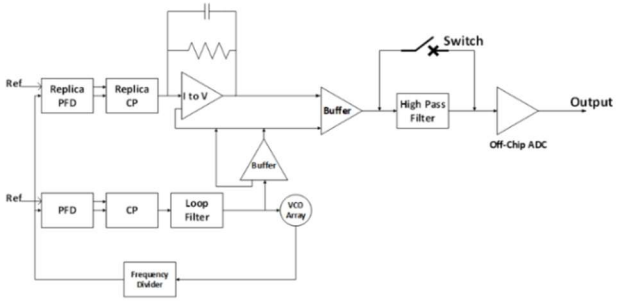



**Figure 1. PLL with an on-chip phase noise measurement circuit that will be used for initial stress and heal experiments to investigate feasibility of improving lifetime.**

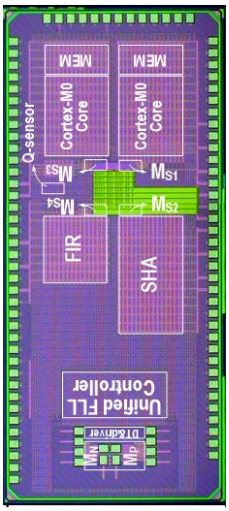
**Keywords:** PLL, downconverter, noise measurements, post-aging selection, lifetime

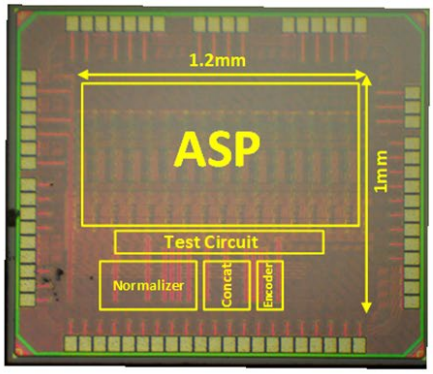
## INDUSTRY INTERACTIONS

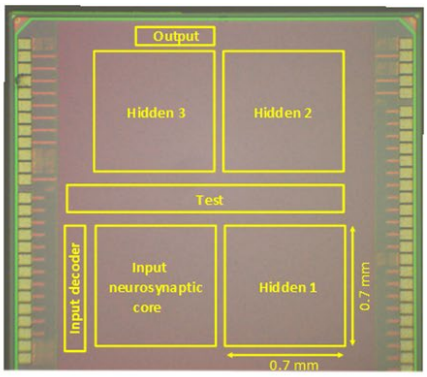
Texas Instruments, Intel

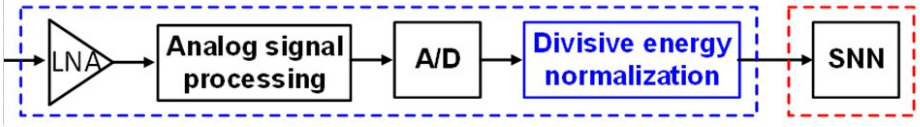
## MAJOR PAPERS/PATENTS

# Energy Efficiency Thrust




| Category | Accomplishment |
|---|---|
| Energy Efficiency (Circuits) | A ±2A fully-integrated current sensor with a 20-mΩ on-chip shunt (resistor) has been demonstrated. It uses an energy-efficient hybrid sigma-delta ADC with an FIR-DAC and consumes only 1.4 µA, a 3× improvement on the state-of-the-art. A tunable analog temperature-compensation scheme allows ±2A currentsto be digitized with 0.35% gain error from −40 to 85 ° C. A gain error of about 0.6% for ±15A currents was achieved with a 3-mΩ PCB shunt. The sensor occupies 1.6 $mm^2$ in 180-nm CMOS. (2810.012, K. Makinwa, TU Delft) |
| Energy Efficiency (Circuits) | A Single Inductor Multiple Output (SIMO) regulated SoC in 65-nm CMOS demonstrated two techniques that mitigate the prohibitive voltage droop and ripple margin problems of SIMO regulated domains. The first extends the Unified Clock and Power (UniCaP) adaptive clocking architecture to multiple domains and achieves 98% average voltage margin reduction. The second introduces Dynamic Droop Allocation, which concurrently analyzes charge delivery requirements and equalizes droop across all domains to reduce worst-case transient droop by 73%. (2810.032, V. Sathe, U. Washington) |
| Energy Efficiency (Circuits) | Always-on keyword spotting (KWS) is essential for a voice-based user interface in mobile and edge devices. This project uses the hybridization of analog-mixed- signal and digital hardware and demonstrated a sub-600nW KWS system with environmental noise and process variation robustness. The system incorporates a 5-layer spiking neural network (SNN) classifier having 650 neurons and 67,000 synapses fabricated in 65-nm CMOS. The SNN hardware demonstrates 7 to 1000X reduced power consumption. (2810.034, M. Seok, Columbia) |

# TASK 2712.006, ROBUST, EFFICIENT ALL-DIGITAL SIMO CONVERTERS FOR FUTURE SOC DOMAINS

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## SIGNIFICANCE AND OBJECTIVES

The Domain-scalability of Integrated Voltage Regulation (IVR) continues to pose a significant challenge. Single-Inductor Multiple Output (SIMO) converters offer a scalable solution but face significant regulation challenges. The proposed effort seeks to address the problem of prohibitive voltage margins due to poor transient response and voltage ripple in SIMO regulators.

## TECHNICAL APPROACH

We noted that SIMO converters offer particularly poor levels of load regulation and have successfully demonstrated Unified Clock and Power (UniCaP) architectures to aggressively remove droop, temperature, and ripple induced margins to dramatically improve system efficiencies. The recent focus of our work has been on demonstrating the proposed SIMO system that employs both UniCaP and Dynamic Droop Allocation, a technique that employs concurrent control of all voltage domains to minimize voltage droop. This technique will be tested in a 65-nm CMOS SIMO-regulated SoC.

## SUMMARY OF RESULTS

We leveraged the learning from our prior funded work on computational control (ISSCC'19 and VLSI'20) and UniCaP (ISSCC'18, VLSI'18, VLSI'20) into our proposed 4-domain integrated SIMO regulated SoC. A die photograph of the test chip is shown in Figure 1.

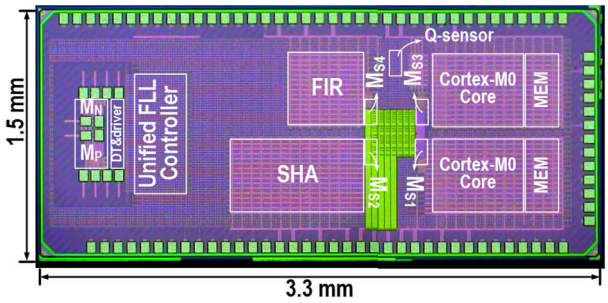


**Figure 1. Die photograph of the SIMO testchip.**

The testchip consists of two Cortex M0 processor cores and an FIR and an SHA accelerator. The SIMO regulator employs UniCaP to effectively tolerate voltage droop, ripple, and in-rush decap current challenges in SIMO designs while aggressively reducing required voltage margins compared to conventional implementation by 98%. Fig. 2 shows the architecture of the testchip. Fig. 3 shows the effectiveness of the proposed Dynamic Droop Allocation (DDA) architecture.

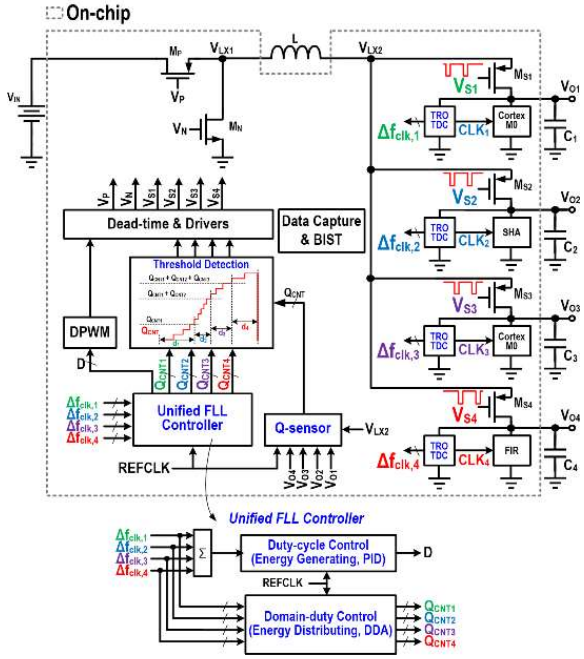


**Figure 2. Overall block diagram of the SIMO test chip.**

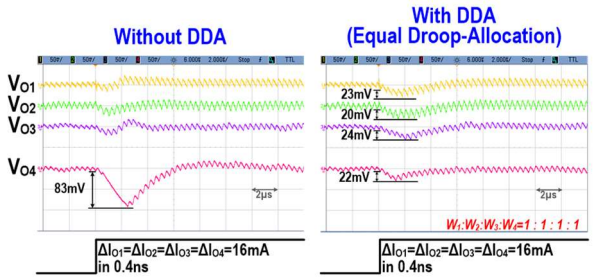


**Figure 3. DDA-SIMO to achieves 3X reduction in voltage droop over conventional SIMO designs.**

The validation of the testchip and the measured effectiveness of UniCaP and DDA in aggressively reducing voltage margins successfully concludes this SRC project.

**Keywords:** SIMO Converter, Unified Clock and Power, Clock Stretching

## INDUSTRY INTERACTIONS

Intel, ARM, NXP

## MAJOR PAPERS/PATENTS

[1] Huang, C-H et. al., "A Single-Inductor 4-Output SoC with Dynamic Droop Allocation and Adaptive Clocking for Enhanced Performance and Energy Efficiency in 65nm CMOS," ISSCC 2021.

# TASK 2712.012, EDAC AND DCDC-CONVERTER CO-DESIGN FOR ADDRESSING ROBUSTNESS CHALLENGES IN EMERGING ARCHITECTURES

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## SIGNIFICANCE AND OBJECTIVES

The goal of this project is to develop techniques for EDAC and DCDC converter co-design in the post-Moore's law era where aggressive architectures and circuits will be explored to continue performance and energy-efficiency scaling while ensuring robustness and reliability.

## TECHNICAL APPROACH

We will devise the following techniques: (i) direct error regulation to make DVS energy-efficient and fully digital while miniaturizing capacitor sizes in the integrated switched-capacitor converter; (ii) EDAC+Converter for non-von-Neumann and parallel architecture, such as error correction scheme for super-Vt circuits performing no instruction replay, and techniques for in and around embedded memory; (iii) EDAC+DVS for clock domain crossing to simplify clock distribution and generation.

## SUMMARY OF RESULTS

Between May and Dec 2020, we have worked on two subtasks. In the first subtask, we have written/published the journal article on the *in-situ* metastability condition detection and correction (MEDAC) chip [1]. In the network-on-chip (NoC) design, use of a synchronizer has been effective for clock domain crossing (CDC), but it neither guarantees the correctness of data nor provides long-term mitigation. In this project, thus, we have replaced the conventional synchronizer with the proposed MEDAC unit and demonstrated the NoC testchip that contains four voltage/frequency (V/F) domains interconnected with an NoC (Figure 1).

The MEDAC unit can detect and flag if the data arrives too close to the RX (sampling) clock edge. Once it detects such a metastability-inducing condition, the proposed MEDAC takes preventive action to reduce the probability of future metastability. Specifically, we have devised a scheme of optimally and dynamically adjusting the phase, without knowing the current phase difference between the data and the sampling clock edge, while maximally extending the time to the next metastability.

In the second subtask, we have written/published the journal article on the single-inductor-multiple-output (SIMO) buck converter for a sub-milliwatt digital system-on-chip (SoC) [2]. An emerging sub-mW near-threshold-voltage (NTV) system-on-chip (SoC) integrates multiple cores, embedded SRAM, network-on-chips (NoC), and other building blocks. To create multiple independent voltage domains, conventionally an off-chip switching converter followed by an array of low-dropout voltage regulators (LDOs) is employed. However, this approach becomes less power efficient as the number of independent voltage domains increases and also the output voltage levels spread over an increasingly wider range, e.g., from I/O voltage down to near/sub-threshold core voltages.

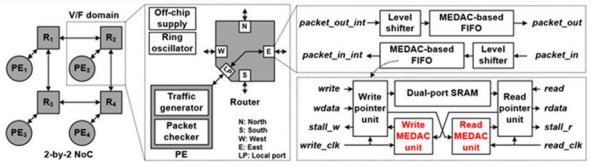


**Figure 1. Proposed MEDAC-based 2-by-2 locally synchronous locally asynchronous (GALS) NoC architecture [1].**

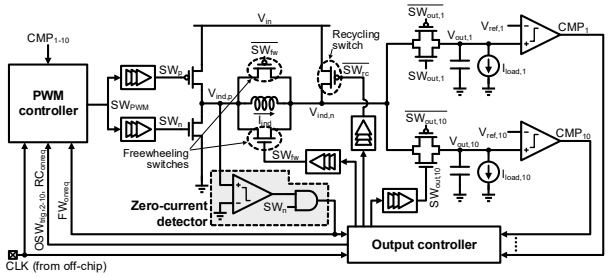


**Figure 2. Proposed SIMO DC-DC converter architecture [2].**

A single-inductor-multiple-output (SIMO) DC-DC buck converter is a good candidate as it provides higher power conversion efficiency (PCE) while requiring only one off-chip inductor, provided we can integrate all the output capacitors on a chip. To reduce the output capacitor size to an integrable level (~100 pF), we choose to use a large inductor, which reduces the size of the inductor current ripple. This allows us to reduce output capacitor size for on-chip integration. Based on this idea, we designed and prototyped the SIMO converter and demonstrated its efficacy.

**Keywords:** NTV, EDAC, Clock Domain Crossing, Metastability, SIMO DC-DC Converter

## INDUSTRY INTERACTIONS

Intel, Texas Instruments

## MAJOR PAPERS/PATENTS

[1] Chuxiong Lin, et al., "MEDAC: A Metastability Condition Detection and Correction…," JSSC, 2020.

[2] Dongkwun Kim, et al., "A 10-Output, Integrated-Output-Capacitor Single-Inductor-Multiple-Output DC-DC Buck Converter with Integrated Output…," SSCL, 2021.

# TASK 2712.018, TEST TECHNIQUES TO APPROACH SEVERAL DEFECT-PER-BILLION FOR POWER ICS

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## SIGNIFICANCE AND OBJECTIVES

This work designed, simulated, and tested custom LDO and Buck Converter power ICs using additional bare-die test points to improve part failure rates. The goal was to test yield enhancement by culling power ICs with outlier subcircuit performance. Recent work characterized small-signal LDO control loop gain using IC external pins.

## TECHNICAL APPROACH

Researchers developed simulations of power ICs with internal IC test features for enhanced testing. These were used to determine subcircuit performance inside of 65-nm CMOS LDOs and Buck Converters. Analyses and simulations of custom-designed LDO and Buck converters were performed to prove these new test concepts. A 65-nm CMOS LDO test IC and a Buck converter test IC were fabricated and tested. The functional LDO IC was used to characterize on-chip power IC control loop gain and phase response and develop fast methods to do this on the ATE.

## SUMMARY OF RESULTS

For the final six months of this project, TI proposed the new goal of devising a method of quickly testing existing LDO's. The prior work was limited to the observation of the LDO IC with advanced test features and external control loop components. Modern LDO's use internal compensation techniques with Miller capacitors or cascode capacitors to provide LDO control compensation.

In this work, researchers focused on analyzing a generic Miller compensated LDO IC design with good simulated line regulation, load regulation, PSSR, and a unity gain frequency of 2.2 MHz with a phase margin of -67°. Cascode compensated LDOs yield similar results. The generic Miller compensated LDO was placed in a Servo-loop test as shown in Figure 1. This configuration can be easily realized on the load board and used during ATE test.

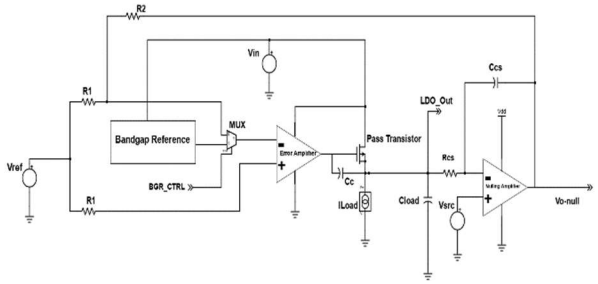


**Figure 1. A Generic Miller Compensated LDO inside a servo-loop for test simulations.**

Servo-loop test simulations were performed. The servo-loop measurement simulations of DC gain were compared with the extracted DC gain from the Cadence Spectre software using stability analysis. The simulations agreed closely. The Miller capacitor compensated LDO showed an inverse linear control-loop cutoff variation with the Miller capacitor value (proportional to 1/Cc).

A goal of this year's work was to test the LDO frequency response in 20mS. The Servo-loop test can characterize the gain bandwidth curve using three frequency points and be used to extrapolate loop cutoff frequency and loop capacitance. Figure 2 shows simulations of generic Miller compensated LDO control-loop bandwidth versus compensation capacitor value. A nominal compensation capacitor of 20 pF yields a control loop bandwidth of 2.2 MHz. If the compensation capacitor is lowered to 15pF then the loop bandwidth is 2.6 MHz and if the compensation capacitor value is raised 25pF the loop bandwidth is 1.9 MHz. So, one could determine a bad on-chip compensation capacitor value by injecting three signals into the servo-loop, 20% above the nominal cutoff, at the cutoff frequency, and 20% below the LDO cutoff frequency and measuring the loop gain.

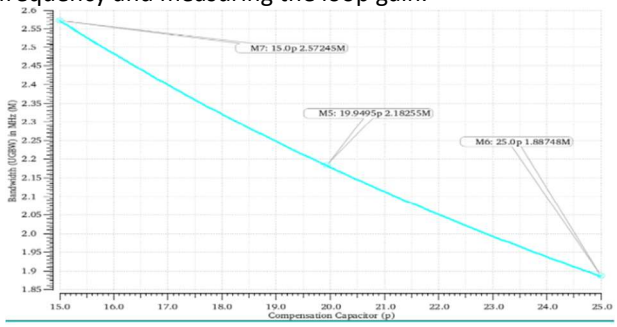


**Figure 2. Simulations of Generic Miller Compensated LDO inside a test servo-loop.**

Integrating a compensated servo-loop for a small signal test on chip is feasible. An integrated servo-loop would require a small area of the LDO chip compared to the other LDO subcircuits.

**Keywords:** Test, Analog, Power, LDO, Buck Converter

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] Anurag Tulsiram and William R. Eisenstadt, "Design for Testability of Low Dropout Regulators," IEEE VLSI Test Symposium 2021, April 26-28, 2021, Virtual Interactive Live Event.

# TASK 2712.020, LOW-POWER MOSTLY DIGITAL TIME-DOMAIN DELTA-SIGMA ADCS FOR IOT

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## SIGNIFICANCE AND OBJECTIVES

This project aims to develop low-power, delta-sigma ADCs for IoT. A purely VCO-based highly digital architecture is investigated in this project. The target is to design a high-order, digital delta-sigma ADC with a power consumption of less than 100uW.

## TECHNICAL APPROACH

A modified digital phase-locked loop (DPLL) architecture is used for the proposed ADC design. The analog input perturbs the digitally controlled oscillator (DCO) phase and the DPLL changes the DCO control word to cancel out the phase perturbation. Thus, the DCO control word acts as a quantized representation of the analog input. Ring oscillators are used as the DCO and DPLL loop filters, resulting in highly digital architecture and high-order quantization noise shaping. The merits of the proposed ADC are (a) no nonlinearity calibration, (b) excess loop delay can be compensated without requiring auxiliary DAC, and (c) inherent DAC mismatch shaping.

## SUMMARY OF RESULTS

We fabricated a 65-nm prototype VCO-based BP-ADC by 4x time-interleaving our prior second-order LP-ADC [1]. The prototype ADC achieves a band-pass Walden FoM of only 57fJ/step which is the best reported so far.

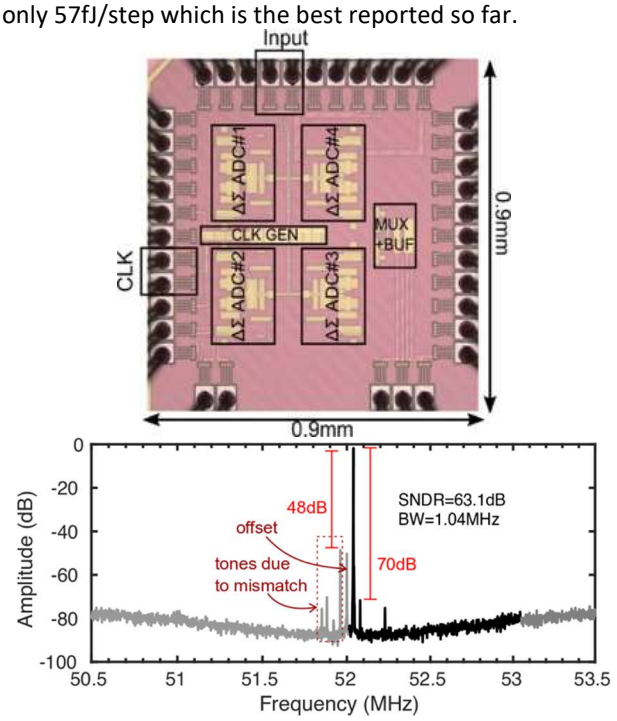


**Figure 1. Prototype BP-ADC and FFT plot.**

While each sub-ADC has an NTF (Noise Transfer Function) proportional to $(1-z^{-1})^2$, the TI-ADC has an NTF proportional to $(1-z^{-4})^2$ since even though the TI-ADC runs 4x faster, the relationship between quantization error of adjacent samples in each sub-ADC is preserved. The BP-ADC uses front-end passive-mixers to down-convert the input signal before feeding to the LP sub-ADCs. The sub-ADCs has intrinsic anti-aliasing that filters out replicas created due to mixing. After the sub-ADC outputs are sampled, only the input frequency signal is retained at the combined output while the replicas are canceled. In the presence of timing/gain mismatch between the sub-ADCs, the replicas are not perfectly canceled but fall out of band. Thus, the proposed BP-ADC does not need calibration for mismatch errors. Use of passive-mixers reduce ADC SNR while maintaining CT operation. ADC SNR can be improved by sampling the input signal prior to quantization.

Figure 1 shows the die photograph of our BP ADC as well as the measured FFT plot. The ADC has a dynamic range of 66dB at 1MHz bandwidth. Table 1 shows a performance summary of the prototype VCO based BP ADC [2].

**Table 1. Performance summary.**

| Tech (nm) | Fs (MHz) | BW (MHz) | Power (mW) | SNDR (dB) | FoM_bp (fJ/step) |
|---|---|---|---|---|---|
| 65 | 208 | 1 | 0.36 | 63 | 57 |
| | | 4.3 | 0.36 | 59 | 21 |

The future direction is to extend the order of noise-shaping by adding a noise-shaping SAR stage in front of the VCO ADC which will increase noise-shaping order and allow rail-to-rail input swing handling.

**Keywords:** ADC, VCO, DPLL, Delta-Sigma, Noise-shaping

## INDUSTRY INTERACTIONS

Texas Instruments, NXP

## MAJOR PAPERS/PATENTS

[1] A. Jayaraj et al., "8.6fJ/step VCO-based CT 2nd-order delta-sigma ADC,'' IEEE A-SSCC, pp. 197-200, 2019.
[2] S. T. Chandrasekaran, et. al., "21fJ/step OTA-less, mismatch-tolerant continuous-time VCO-based band-pass ADC," IEEE SSC-L (special section for ESSCIRC), pp. 342-345, 2020.

# TASK 2712.024, A SYSTEM-IN-PACKAGE PLATFORM FOR ENERGY HARVESTING AND DELIVERY FOR IOT EDGE DEVICES

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MADHAVAN SWAMINATHAN, GEORGIA INSTITUTE OF TECHNOLOGY

## SIGNIFICANCE AND OBJECTIVES

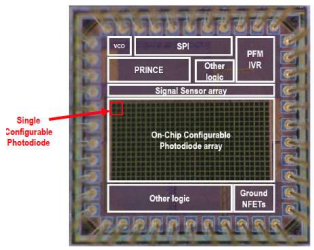
The proposed research aims to design a System-In-Package (SIP) based energy delivery system for powering wireless sensor nodes and IoT edge devices.

## TECHNICAL APPROACH

We will develop the architecture of the proposed system-in-package based energy harvesting and delivery system. We will design and fabricate the on-package inductor for the proposed energy delivery system. We will design, fabricate, and test the power management unit of the proposed SIP.

## SUMMARY OF RESULTS

**Self-powered Authentication IC [1]:** This design presented an authentication IC in 65-nm CMOS. The IC is interrogated using optical power transfer via off-chip photodiodes and visible light based data transfer via on-chip CMOS diodes. Authentication is performed with a lightweight encryption engine PRINCE. The IC consumes 2.29µW standby power and achieves a 53.8kbps data rate.




| | |
|---|---|
| Technology | 65nm CMOS |
| Package | CLCC44 |
| Area | 1mm x 1mm |
| Photodiode Area | 720µm x 360µm |
| Photodiode FF | 77% |
| VCO Max. Freq | 500MHz |
| Encrypt. Eng Area | 430µm x 180µm |
| IVR Area | 15µm x 54 µm |

**Figure 1. Summary of the self-powered authentication IC.**

**A low-overhead PMU Test-chip for energy harvesting [2]**: We have developed a low-overhead energy harvesting and delivery system (EHDS) with pulse frequency modulated (PFM) integrated voltage regulator (IVR) power conversion and self-tuned maximization of system output power. Compared to prior works that rely heavily on high inductance to improve end-to-end efficiency, the proposed EHDS demonstrates orders of magnitude reduction in the amount of passives while demonstrating a slight decrease in end-to-end efficiency compared to the state-of-the-art. Instead of implementing conventional source-oriented harvesting control, a novel system-focused approach is developed to tune PFM-IVR operation based on both source capabilities and load demand on the fly. A configurable fractional sample & hold (FSH) circuit that provides flexibility for harvesting window control relieves the use of high passives when combined with output regulation based load-inclusive time-based maximum power point tracking (LI-TB-MPPT). The system is demonstrated in a 65-nm CMOS process. Observed switching frequency tuning embedded into LI-TB-MPPT allows end-to-end efficiency optimization with up to a 15% increase in conversion efficiency against variations. A wake-up assist circuit provides two improvements on top of the effect of reduced passive to achieve a cold-start period of 3.8ms. Altogether, the design provides a compact solution for self-sustained cost-restricted standalone systems.

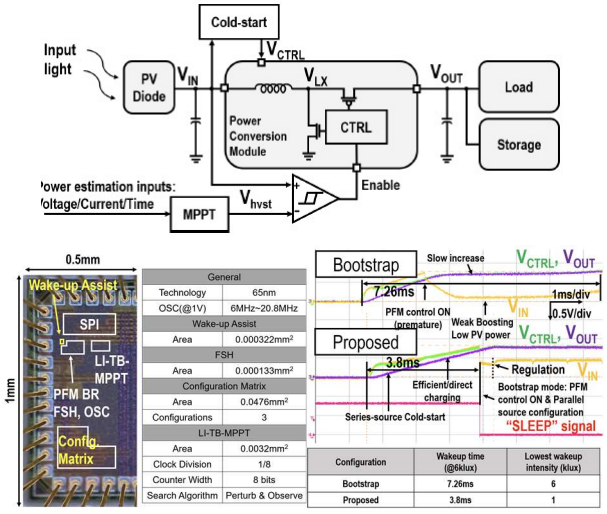



**Figure 2. The overall architecture, design summary, and measured waveform for wake-up of the PMU IC.**

**Keywords:** Integrated voltage regulator, power management, energy harvesting

## INDUSTRY INTERACTIONS

Intel

## MAJOR PAPERS/PATENTS

[1] E. Lee, N. Rahman, V. Chekuri, A. Singh and S. Mukhopadhyay, "A low power authentication IC for visible light based interrogation," accepted for publication in IEEE Transactions on Industrial Electronics (TIE).

[2] E. Lee, V. Chekuri, and S. Mukhopadhyay, "A PFM boost harvester with System-level Self-tuned Maximum Power Point Tracking," submitted to IEEE Transactions on Power Electronics (currently under revision).

# TASK 2712.027, GATE DRIVING TECHNIQUES AND CIRCUITS FOR AUTOMOTIVE-USE GAN POWER CIRCUITS

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## SIGNIFICANCE AND OBJECTIVES

The project aims to implement automotive-use, high step-down, DC-DC power conversion with high switching frequency, high power density, and high efficiency, using a double-step down (DSD) topology. The key is to develop a closed loop that prevents the two sub-converters from being simultaneously turned on. Phase current balancing control improves current distribution.

## TECHNICAL APPROACH

To achieve direct 48V/1V power conversion with a DSD topology, use of GaN HEMTs as power switches, a master slave adaptive ON-OFF time (AO$^2$T) control, and synchronous bootstrap circuits are proposed. The master slave adaptive AO$^2$T control improves transient response, avoids $T_{ON}$ overlapping, and enables adaptive phase synchronization with automatic phase current balancing. The integrated synchronous bootstrap circuits refresh the voltage across bootstrap capacitors periodically to stabilize the power rails of gate drivers.

## SUMMARY OF RESULTS

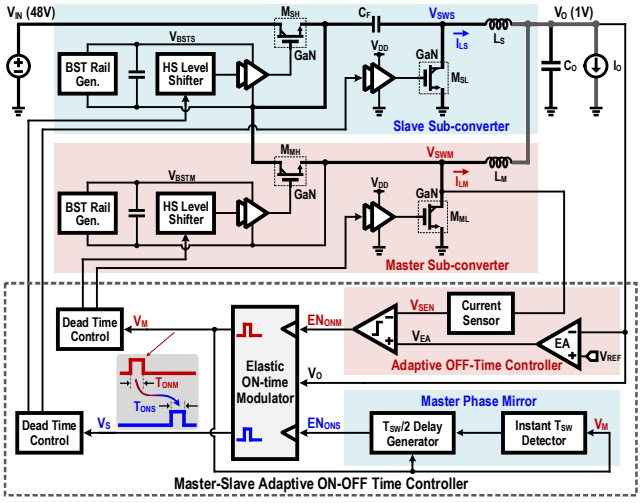


**Figure 1. Block diagram of DSD GaN power converter.**

The proposed GaN-based DSD power converter is shown in Fig. 1. It is divided into a master sub-converter and a slave sub-converter. To avoid the harmful ON-time ($T_{ON}$) overlap and current imbalance, a master-slave adaptive AO$^2$T control is employed with synchronous bootstrap circuits. The proposed master-slave AO$^2$T control facilitates clock-free phase synchronization and automatic phase current balancing without extra control circuits. With the proposed elastic on-time modulation scheme, the load transient response is greatly improved. In addition, the converter is designed to prevent cross-phase $T_{ON}$ overlap to improve reliability.

The design is implemented using a 180-nm HV BCD process. The active die area of the chip is 1.46mm$^2$. Four enhancement-mode GaN HEMTs are used as the power switches in the DSD power converter. It achieves 2MHz in each sub-converter for direct 48V/1V DC-DC power conversion and delivers the maximum load current of 1.5A. Fig. 2 shows the maximum efficiency for direct 48V/1V power conversion is 85.4%, 79% and 56.8% when the switching frequency of each sub-converter is 100kHz, 250kHz and 2MHz, respectively.

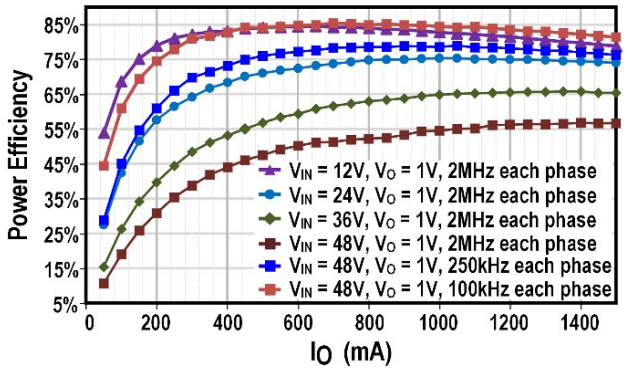


**Figure 2. Measured efficiency of DSD GaN power converter.**

**Keywords:** GaN Switch, direct 48V/1V power conversion, double step-down architecture

## INDUSTRY INTERACTIONS

Texas Instruments, NXP, IBM

## MAJOR PAPERS/PATENTS

[1] D. Yan and D. B. Ma, "An Automotive-Use Battery-to-Load GaN-Based Power Converter with Anti-Aliasing Multi-Rate Spread-Spectrum Modulation and In-Cycle ZVS Switching," *2020 Symposium on VLSI Circuits*, Honolulu, USA, Jun. 2020, pp. 1-2.

[2] D. Yan and D. B. Ma, "Fully On-Chip Pre-charge and Synchronous Bootstrap Circuits for Direct 48V/1V GaN-Based DSD Power Converters," SRC *TECHCON*, Austin, USA, Sept. 2020.

# TASK 2712.028, HIGH PERFORMANCE MICRO-SUPERCAPACITOR ON A CHIP BASED ON A HIERARCHICAL NETWORK OF NITROGEN DOPED CARBON NANOTUBE SHEETS SUPPORTED $MNO_2$ NANOPARTICLES

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## SIGNIFICANCE AND OBJECTIVES

This work is focused on demonstration of a 2D ultra flexible micro-supercapacitor (fMSC).

## TECHNICAL APPROACH

The current trend in the miniaturization of wearable electronics demands ultra-thin power/energy devices. High-performing fMSCs with a 2D form factor seems to be a viable approach to address this demand. This work emphasizes the electrochemical performance of a highly aligned array of carbon nanotube (HACNT) sheets for thin film fMSCs using a rapid, single step, and scalable plasma etching method.

## SUMMARY OF RESULTS

To study the device's flexibility, the electrochemical performance of the fMSCs was evaluated under various bending states (0°-180°) as shown in Fig. 1(a). Figs. 1(b) and 1(c) illustrate a slight increase in specific capacitance ($C_{sp}$) after bending under 30° followed by a stable behavior under higher bending states. The bending durability of the devices was evaluated via 10k cycles of bending under an angle of 180°. Our fMSCs exhibited excellent durability with no significant change in capacitance showing their outstanding flexion properties suitable for wearable electronics. (Figure 1d)

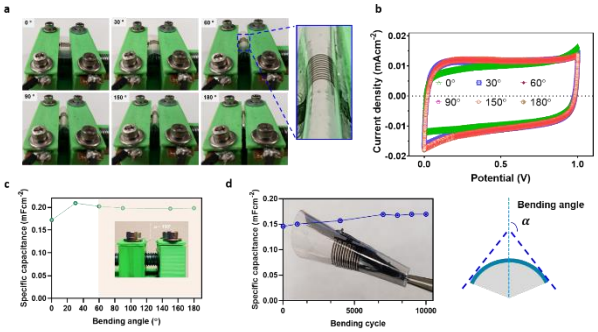


**Figure 1. (a) fMSC at different bending states, (b) CV curves at various bending angles, (c) Change in specific capacitance with bending angle (α), and (d) bending cycles under bending angle of 180° up to 10,000 cycles.**

To improve the performance of the fMSCs, we altered the electrode interspacing from 140 µm to 40 µm which improved $C_{sp}$ by a factor of 50X.

The impact on the energy and power density of these devices were also studied as presented in Figure 2(b). Finally, our fMSC performance in comparison to the most recent work is presented in Ragone plot in Figure 2(c). An optical image of devices (gap: 40 & 60 µm) is shown in Figure 2(d).

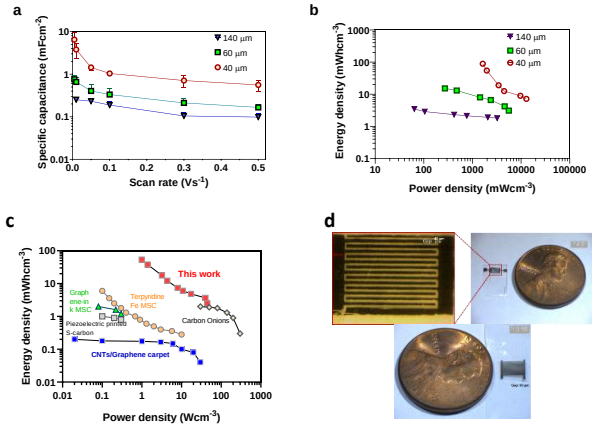


**Figure 2. (a) $C_{sp}$ of fMSCs (140, 60, and 40 µm) vs. scan rates from 5mVs$^{-1}$ to 500mVs$^{-1}$, (b) Ragone plot of the fMSCs, (c) Comparison of our device performance with MSCs based on carbon onion and graphene-ink, piezoelectric printed sucrose-carbon, CNT/graphene, terpyridine-Fe-based polymer base fMSC in a Ragone plot, (d) Digital image of fMSCs (40 µm and 60 µm gap).**

A high peak energy density of 54 mWhcm$^{-3}$ and a power density of 44.7 Wcm$^{-3}$ were obtained for our fMSC with a 40-µm gap, comparable to 3D MSC devices. Our fMCS shows superior performance in comparison to recently reported MSCs based on graphene ink, carbon onion, piezoelectric printed sucrose-carbon,CNTs/Graphene carpet and terpyridine-Fe-based polymer based fMSC.

**Keywords:** HACNT sheet, microsupercapacitor, all-solid-state, flexible, energy storage

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] B. Dousti, G.S. Lee, et al. Highly flexible all-solid-state planar microsupercapacitors for portable electronics, under review J. Power Sources.

[2] B. Dousti, Y.I. Choi, S. Cogan, and G.S. Lee, "A High Energy Density 2D Microsupercapacitor Based on an Interconnected…," ACS Applied Materials and Interfaces, 2020.

[3] Y. I. Choi, C. Chen, J. W. Park, and G.S. Lee, "Spinnable Carbon Nanotube Forest Synthesis in Nitrogen Environment," Diamond and Related materials, 2020.

# TASK 2810.002, SECURITY-AWARE DYNAMIC POWER MANAGEMENT FOR SYSTEM-ON-CHIPS

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## SIGNIFICANCE AND OBJECTIVES

The proposed research investigates the energy-security trade-offs associated with Dynamic Power Management (DPM). The proposed effort will develop a methodology to characterize security implications of DPM in SoCs and design circuit/system techniques to co-optimize security and energy efficiency of DPM.

## TECHNICAL APPROACH

This effort will pursue a cross-layer approach to understand the energy-security trade-offs in Dynamic Voltage Frequency Scaling (DVFS). We have designed power domains that are secure against power-/EM- side-channel analysis by leveraging the distributed integrated voltage regulators. We have investigated the energy-security trade-off at the chip level by focusing on the DVFS controller and algorithm.

## SUMMARY OF RESULTS

***DVFS as a Security Exploit [1]:*** Dynamic Voltage and Frequency Scaling (DVFS) plays an integral role in reducing the energy consumption of mobile devices, meeting the targeted performance requirements at the same time. We examine the security obliviousness of CPU Freq. in DVFS framework of Linux-kernel based systems. Since Linux-kernel based operating systems are present in a wide array of applications, the high-level CPU Freq policies are designed to be platform-independent. Using these policies, we present BiasP exploit, which restricts the allocation of CPU resources to a set of targeted applications degrading their performance.

***Trustworthy Hardware based Malware Detector (HMD) [2]***: The machine learning (ML) models used in HMDs are agnostic to the uncertainty that determine whether the model "knows what it knows," severely undermining their trustworthiness. We propose an ensemble-based approach that quantifies uncertainty in predictions made by ML models of an HMD when it encounters an unknown workload than the ones it was trained on. We test our approach on power management-based and performance counter-based HMDs.

***Securing IoT Devices using Dynamic Power Management [3]:*** We demonstrated Dynamic Voltage and Frequency Scaling (DVFS) states form a signature pertinent to an application, and its run-time variations comprise of features essential for securing IoT devices against malware attacks. We have demonstrated this proof of concept by performing experimental analysis on Snapdragon 820 mobile processor, hosting Android operating system (OS). We developed a supervised machine learning model for application classification and malware identification by extracting features from the DVFS states time-series. We also performed power measurements under different governors to evaluate power-security aware governor.

***Machine Learning in Wavelet Domain for Electromagnetic Emission Based Malware Analysis [4]:*** We have presented a signal processing and machine learning (ML) based methodology to leverage Electromagnetic (EM) emissions from an embedded device to remotely detect a malicious application running on the device and classify the application into a malware family. We have developed Fast Fourier Transform (FFT) based feature extraction followed by Support Vector Machine (SVM) and Random Forest (RF) based ML models to detect a malware. We further demonstrated the use of Discrete Wavelet Transform (DWT) based feature extraction from spectrograms of EM side-channel traces and perform ML on the extracted features to learn fine-grained patterns of malware families.

**Keywords:** Side-channel, EM emission, Dynamic Power Management, Machine Learning, Malware Detection

## INDUSTRY INTERACTIONS

Intel, IBM

## MAJOR PAPERS/PATENTS

[1] H. Kumar, et. al, "BiasP: A DVFS based Exploit to Undermine Resource Allocation Fairness in Linux Platforms," IEEE/ACM International Symposium on Low-Power Electronic Design (ISLPED), August 2020.

[2] H. Kumar, et. al., "Towards Improving the Trustworthiness of Hardware based Malware Detector using Online Uncertainty Estimation," Design Automation Conference (DAC), 2021.

[3] N. Chawla, et.al, "Securing IoT Devices using Dynamic Power Management: Machine Learning Approach," IEEE Internet of Things Journal.

[4] N. Chawla, et. al., "Machine Learning in Wavelet Domain for Electromagnetic Emission Based Malware Analysis," IEEE Transactions on Information Forensics and Security (TIFS), vol. 16, May 2021, pp. 3426-3441.

# TASK 2810.003, INTEGRATED VOLTAGE REGULATOR MANAGEMENT FOR SYSTEM-ON-CHIP ARCHITECTURES

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## SIGNIFICANCE AND OBJECTIVES

When achieving the high efficiency of modern sophisticated power delivery networks (PDNs), designers create many pathways for unintended interactions and expose various side-channel attacks. The efficiency, stability, as well as security of the PDNs, need to be systemically optimized and regions evaluated based on the simulation and hardware evaluation platform.

## TECHNICAL APPROACH

We propose PowerScout - a unified PDN modeling framework that can perform thorough side-channel vulnerability analysis by simulating a complete PDN system across multiple design layers and voltage domains. PowerScout attains a balance between security interpretability and simulation accuracy. Measurements from the platform based on a heterogeneous system composed at the board level help us verify the modeling accuracy and predictive power of our proposed modeling and simulation infrastructure, and to evaluate different run-time optimization algorithms and management strategies in a real system, thus lending more credibility to the infrastructure and optimization tools to be extended for studying future SoCs.

## SUMMARY OF RESULTS

With PowerScout validated, we evaluate fault injection attacks that use ring oscillator-based power virus (ROPVs). Our findings not only are consistent with those of previous works but also provide better interpretability. We first simulate the attack in PowerScout while sweeping the toggling frequency and varying the duty cycle. The attack space exploration for ROPVs is presented in Figure 1, where the heat map shows the minimum die voltage under different toggling frequencies and duty cycles. Generally, the toggling frequency and duty cycle do not have linear influences on the voltage drop. But when the toggling frequency ranges between 10KHz and 50KHz, the fault injection performance is linear to the toggling frequency. Moreover, there exists a most efficient toggling frequency which can induce the maximum voltage drop. Figure 1 (b) shows the minimum supply voltage versus toggling frequency when the duty cycle is 50%, and also shows the simulated PDN impedance. The resonant frequency of the PDN impedance is almost the same as the most efficient toggling frequency so that by using the resonant frequency and corresponding impedance from vulnerability analysis, we can effectively predict the maximum fault injection performance.

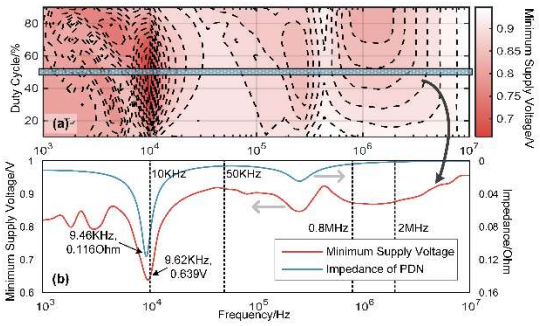


**Figure 1. (a) The minimum die voltage under different toggling frequencies and duty cycles, and (b) the PDN impedance compared to the minimum die voltage at 50% duty cycle.**

Figure 2 validates PowerScout by comparing results between the simulated and measured impedance profile of the hardware evaluation platform. The upper panel shows the comparison between the default configuration and the configuration of adding a chip. The lower part shows the results for the configuration of adding a resistor. We can accurately model the PDN at a frequency up to 100MHz. The cross-validation shows the correctness of the built PDN model.

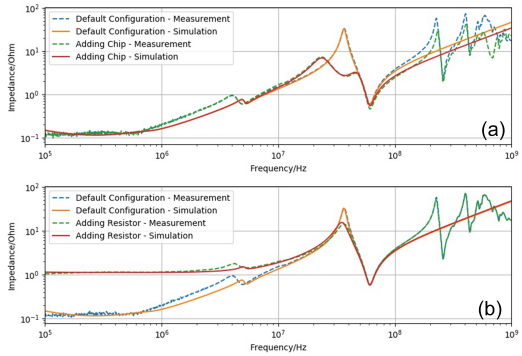


**Figure 2. The comparison between the PDN impedance profile measurement and the simulation results is based on the model built in PowerScout.**

**Keywords:** Integrated voltage regulator, DVFS, security

## INDUSTRY INTERACTIONS

Intel, IBM

## MAJOR PAPERS/PATENTS

[1] H. Zhu et al., "PowerScout: A Security-Oriented Power Delivery Network ModelingFramework for Cross-Domain Side-Channel Analysis," 2020 AsianHOST.

# TASK 2810.006, COMBATING UNPRECEDENTED EFFICIENCY, NOISE AND FREQUENCY CHALLENGES IN MODERN HIGH CURRENT INTEGRATED POWER CONVERTERS

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## SIGNIFICANCE AND OBJECTIVES

To suppress the EMI effectively in GaN power converter, a continuous random spread-spectrum-modulation (C-RSSM) scheme is developed. It employs a Markov-chain-based random clock generator to randomly modulate the switching frequency of the power converter in the analog domain. Thereby, the EMI spectra in the power converter are spread uniformly and continuously, attenuating the EMI noise considerably.

## TECHNICAL APPROACH

Based on a chaotic dynamic system, a Markov-chain-based random clock generator is built to implement the analog $f_{SW}$ modulation within a sideband of $\Delta f_C$ centered at $f_{SW0}$. Hence, it conducts SSM continuously and spreads the spurious noise at $f_{SW0}$ and its harmonics uniformly, achieving desirable C-RSSM. Compared to conventional discrete RSSM (D-RSSM), it effectively overcomes the finite frequency resolution issue, thus achieving a better performance in terms of EMI noise compression.

## SUMMARY OF RESULTS

By distributing the switching frequency within a certain sideband through spread-spectrum modulation (SSM) techniques, the EMI energy at the fundamental frequency and its harmonics are scattered to a lower level. For effective EMI suppression, it is highly preferable to accomplish C-RSSM. To serve this purpose, a Markov-chain-based random clock generator is designed to realize random $f_{SW}$ modulation in the analog domain. Beneficially, it conducts SSM continuously and spreads spurious noise uniformly.

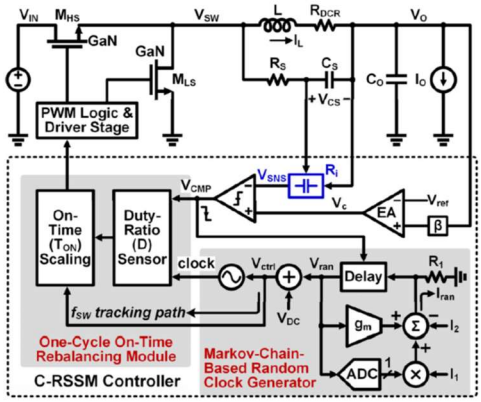


**Figure 1. Block diagram of the proposed Markov Chain based C-RSSM power converter.**

The system is designed as shown in Fig. 1. The Markov-chain-based random clock generator implements analog switching frequency modulation within a range around $f_{SW0}$, achieving a C-RSSM to spread the EMI noise uniformly. On the other hand, the one-cycle on-time rebalancing module prevents the $V_O$ from jittering induced by RSSM, balancing the EMI and voltage regulation performance of the converter.

A design prototype was designed and fabricated using a 0.18-µm HV CMOS process, with the die photo shown in Fig. 2. With ±10% modulation range of a nominal switching frequency of 8.3MHz, peak EMI is reduced from 66dBµV to 35dBµV at the fundamental frequency and from 62dBµV to 27dBµV at the 3rd order harmonic. The RSSM-induced output voltage jittering is also suppressed from 240mV to below 10mV.

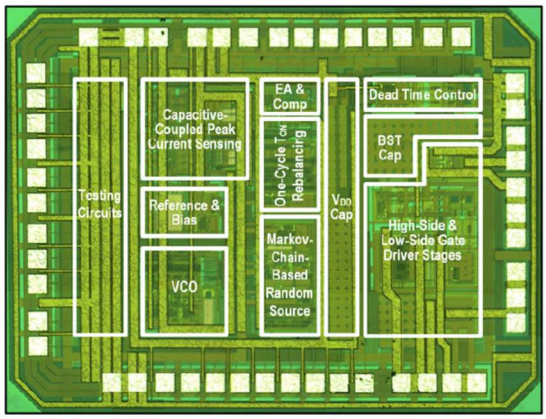


**Figure 2. Chip micrograph of the converter.**

**Keywords:** GaN, continuous RSSM, EMI noise

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] Y. Chen and D. Ma, "EMI-regulated GaN-based switching power converter with Markov continuous random spread-spectrum modulation and one-cycle on-time rebalancing," IEEE J. Solid-State Circuits (JSSC), vol. 54, no. 12, pp. 3306-3315, Dec. 2019.

[2] Y. Chen and D. Ma, "An 8.3MHz GaN power converter using Markov continuous RSSM for 35dBµV conducted EMI attenuation and one-cycle $T_{ON}$ rebalancing for 27.6dB $V_O$ jittering suppression," IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2019, pp. 250-251.

# TASK 2810.008, CIRCUIT TECHNIQUES FOR FAST START-UP OF CRYSTAL OSCILLATORS

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## SIGNIFICANCE AND OBJECTIVES

High-Q crystal oscillators (XOs) are notorious for being extremely slow to start up. Their long start-up time increases the average power consumption in duty-cycled systems such as Internet-of-Things. The objective of this work is to reduce the start-up time with minimal energy consumption.

## TECHNICAL APPROACH

Previously, we demonstrated an XO start-up technique that pre-energizes a high-Q resonator close to its steady-state energy using a low-Q "injection" oscillator for a precisely calculated, short duration (~100 cycles) [1]. The technique achieved 15x faster start up vs. the prior art. The short injection duration, which amounts to wideband signal injection, together with a PTAT injection drive makes it tolerate up to +/-6500ppm injection frequency errors from temperature and process variability. In this project, we are further enhancing our technique's tolerance to injection frequency errors and extending it to other oscillator topologies such as ultra-low power RTC XOs.

## SUMMARY OF RESULTS

We have developed a technique to automatically calibrate the injection oscillator frequency. Before each pre-energization instance, the ring injection oscillator is configured as a delay-line and its delay adjusted to match the period of the ringing step response of the crystal. Less than +/- 1000 ppm error is achieved in <10 cycles. Compared to our prior work [1], the technique eliminates the need for factory-time calibration and should be insensitive to injection oscillator frequency mismatch, temperature drift with minimal added startup time, and energy costs (see Table 1). A prototype IC has been fabricated and is currently being packaged and assembled for testing.

**Table 1: Comparison with the prior art.**

| | Startup time (cycles) | Startup Energy (nJ) | Calibration Required? |
|---|---|---|---|
| This Work | 123 | 14.32 | No |
| Our Prior Art [1] | 113 | 12 | Yes |
| J.B.Lechevallier, JSSC Aug 2019 | 360 | 4.4 | No |

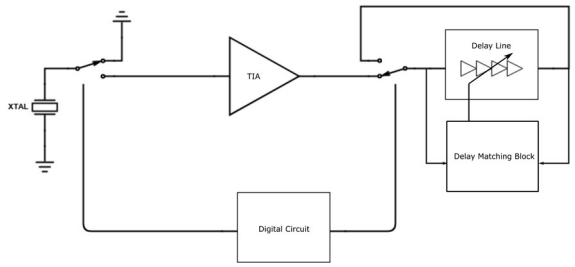


**Figure 1. Block diagram of auto calibration technique, consisting of a TIA to amplify the ringing response of the crystal, and a delay line to quickly match the period to the amplified signal.**

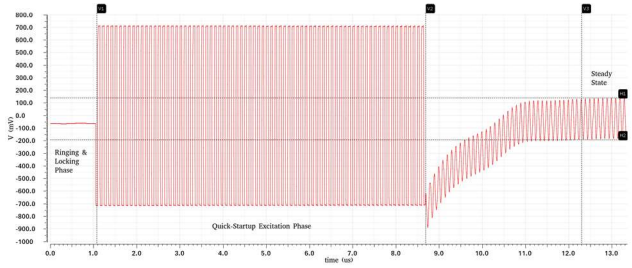


**Figure 2. Full system simulation showing crystal voltage: ringing and locking phase (0.1us – 1.1us), excitation phase (1.1us – 8.6us), and eventual steady state operation (after 12.4 us).**

**Keywords:** Start-up time, crystal oscillators, low power, re-configurable delay line, automatic calibration

## INDUSTRY INTERACTIONS

Intel

## MAJOR PAPERS/PATENTS

[1] H. Esmaeelzadeh, "A Quick Startup Technique for High-Q Oscillators Using Precisely Timed Energy Injection," JSSC 2018.

[2] H. Esmaeelzadeh, "Low-Energy Clock Generation for IoT Applications," Ph.D. Thesis, UCLA, 2019.

[3] H. Esmaeelzadeh, S. Pamarti, "A sub-nW 32-kHz Crystal Oscillator Architecture Based on a DC-Only Sustaining Amplifier," JSSC Dec 2019 (ISSC special issue).

[4] S. Pamarti et al, Ultra-low-power Oscillator with DC-Only Sustaining Amplifier, US 10,924,060 B2, granted Feb 16, 2021.

# TASK 2810.009, MIXED-SIGNAL BUILDING BLOCKS FOR ULTRA-LOW POWER WIRELESS SENSOR NODES

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## SIGNIFICANCE AND OBJECTIVES

This project develops novel and state-of-art performing ultra-low power mixed-signal circuits, suitable for IoT systems. This includes timekeeping circuits, amplifiers, CMOS-based sensors, and high voltage generation.

## TECHNICAL APPROACH

The most challenging ultra-low power circuit components are mixed-signal circuits such as timers, clock sources, sensing and interface circuits (e.g., temperature sensors and low-noise amplifiers). Some of these cannot be duty cycled (e.g., timers), while others require both low noise and low power (e.g., amplifiers), which are traditionally mutually exclusive. This work proposes new ULP designs for 1) crystal oscillator-based real-time clocks (RTCs), 2) temperature-compensated wakeup timers, 3) temperature sensors, 4) front-end low-noise amplifiers, and 5) on-chip high voltage generation.

## SUMMARY OF RESULTS

Capacitive MEMS sensors are fast becoming ubiquitous in many applications such as accelerometers and microphones, for their compact size, low temperature drift, and zero static current consumption. The capacitive MEMS sensors usually need dc-bias voltages to produce the sensing signal, and it is desired to use large bias voltages for better sensitivity. Voltage fluctuations on these bias voltages should be minimized to maintain a good signal-to-noise ratio. However, it remains difficult to design low power, fully integrated bias voltage generators that achieve both high voltage output (>20V) and low voltage fluctuations (<50mV). The challenge is exacerbated when considering that the generated voltages must be well-controlled to avoid interferences with the MEMS operation (e.g., electrostatic pull-in), which significantly increases the complexity and power consumption of the voltage generation circuit.

In this work, we propose a nW high voltage generator for ultra-low-power MEMS sensors. As shown in Fig. 1, the high voltage Dickson charge pumps (CPs) take 2V-4V power supply as input, and output 0 to ±30V programmable voltages through a positive ($V_{outp}$) and a negative ($V_{outn}$) electrode. The high voltage generator has a closed-loop scheme with its voltage output electrodes ($V_{outp}$, $V_{outn}$) separated from the voltage sampling electrodes ($V_{outp\text{-}pc}$, $V_{outn\text{-}pc}$) to reduce sampling ripples.

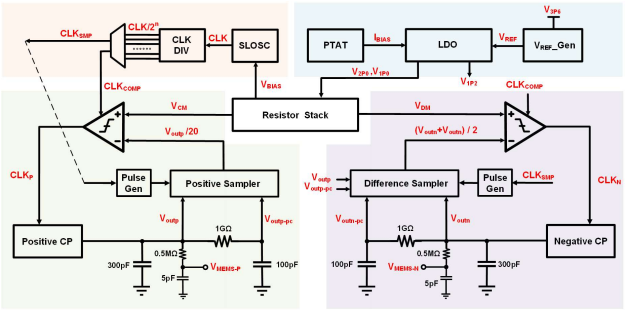


**Figure 1. Top-level diagram of the proposed ultra-low-power high voltage generator for MEMS sensing.**

To minimize the complexity and power overhead related to high voltage sampling (especially the negative voltage sampling), we present a novel structure that samples $V_{outp}$ and $V_{outp}$ + $V_{outn}$ and divides them down to compare with the desired "common-mode voltage $V_{CM}$" and the "voltage difference $V_{DM}$" between positive and negative output voltage. The comparator results the timing signals for the CPs that is usually highly duty-cycled with pure capacitive loads, greatly reducing the switching loss by the CPs. Other peripheral circuits, such as clock generation and reference voltage generation, are also implemented on chip. Altogether, the design achieves 40mV voltage variance at full-scale output while consuming 35.1nW active power.

**Table 1. Performance summary of test chip.**

| | | This work |
|---|---|---|
| Technology | | 0.18-µm HVBCD |
| Supply voltage [V] | | 2-4 |
| Maximum DC output | Positive [V] | 30 |
| | Negative [V] | -30 |
| Total Power [nW] | | 35.1 |
| Max Voltage Variant [mV] | | 40 |

**Keywords:** nano-watt, high voltage generation, MEMS sensor

## INDUSTRY INTERACTIONS

NXP

## MAJOR PAPERS/PATENTS

# TASK 2810.010, GS/S ADC BASED CYCLE-TO-CYCLE CLOSED-LOOP ADAPTIVE SMART DRIVER FOR HIGH-PERFORMANCE SIC/GAN POWER DEVICES

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## SIGNIFICANCE AND OBJECTIVES

As the input/output voltage ratio increases, buck/booster converters suffer from degraded power efficiency. The objective of this research is to demonstrate a 3-level buck converter using GaN switches that maximizes the power efficiency while utilizing a novel control algorithm based on general-regression-neural-network (GRNN) which allows for fast response time.

## TECHNICAL APPROACH

We propose a General-Regression-Neural-Network Based 5V-to-48V Three-Level Buck/Boost Power Converter with 40-dB PSRR and 90%-Efficiency for SSD Power Loss Protection. The new GRNN approach is proposed to eliminate the need for an error amplifier together with the feedback path and its associated compensation network, allowing for fast response time and reduced power consumption. The proposed power converter finds, in real-time, the relationship between the desired output voltage and multiple input variables, including the voltage across the storage capacitor, the voltage at the switching node, load current, and temperature.

## SUMMARY OF RESULTS

Figure 1 illustrates the proposed GRNN-based three-level GaN buck-boost power converter and supervised learning procedure. The GRNN predicts voltage $V_{PRE}$ used to produce the desired PWM duty cycle in real-time. Without the bandwidth limitation from the conventional feedback loop, theoretically, the proposed GRNN-based power converter can reduce the line response time by ~10x, thus mitigating the impact of line droops. In addition, three-level GaN-based buck/boost converters are employed to improve the energy efficiency since the three-level topology can halve the voltage stresses across the GaN switches. A fourth-order semi-physical formula consisting of multiplication and addition functions is chosen to accurately fit the predicted voltage VPRE to the ideal $V_{PRE}$ trajectory with respect to $V_{SC}$ (Fig. 1) at different $I_{LOAD}$ and temperature T.

The proposed converter is fabricated in 0.18-µm HV BCD process as shown in Figure 2. Four enhancement-mode GaN FET switches are employed as power switches to implement the three-level buck/boost converter. The proposed buck converter achieves a maximum power efficiency of 90.2% with a 12-V input. This neural-network based control scheme demonstrated excellent power efficiency, PSRR, and load regulation over a wide input range.

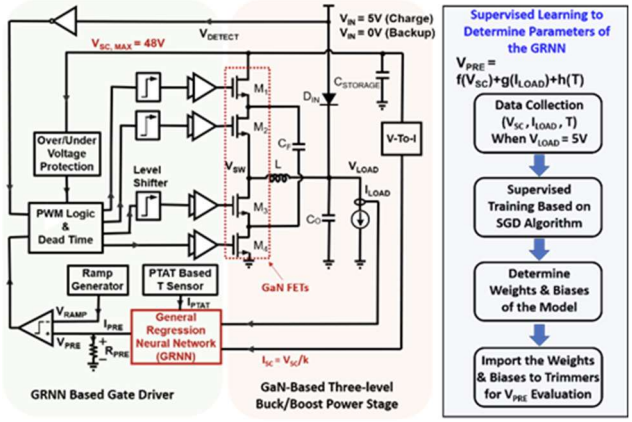


**Figure 1. Proposed GRNN-based three-level GaN buck-boost power converter and the supervised learning procedure to train the GRNN.**

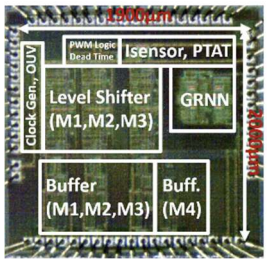


**Figure 2. Microphotograph of the proposed GRNN Based 5V-to-48V three-level buck/boost converter.**

**Keywords:** GaN driver, General-Regression-Neural-Network, machine learning, smart driver, 3-level buck

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] C. Yang, W. Chen, Y. Fan, W. Da, and P. Gui, "A 10MHz 40V VIN Slope-Reconfigurable Gaussian Gate Driven GaN DC-DC Converter…", IEEE RFIC 2020

[2] C. Yang, W. Chen, Y. Fan and P. Gui A General-Regression-Neural-Network Based 5V-to-48V Three-Level Buck/Boost…", IEEE CICC 2021

[3] C. Yang, W. Chen, Y. Fan and P. Gui, "Design and Characterization…", to appear in IEEE JSSC (minor revision)

# TASK 2810.011, MICRO-POWER ANALOG-TO-DIGITAL DATA CONVERTERS FOR SENSOR INTERFACES

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## SIGNIFICANCE AND OBJECTIVES

MEMS-based sensor systems have many applications in automotive electronics, IoT, and communication. Their interface circuits require data converters with high accuracy and power efficiency. Based on industry input, such a converter was designed and fabricated.

## TECHNICAL APPROACH

A novel active noise-shaping SAR ADC, based on a two-capacitor DAC, was designed as a high-accuracy digitally corrected circuit. To mitigate the effects of non-idealities noise filtering, correlated double sampling and correlated level shifting were used. To cancel the effects of mismatches and parasitic capacitors, the complete circuit used calibration with a novel bit-by-bit digital correction technique [1],[2]. The circuit diagram is shown in Fig. 1.

## SUMMARY OF RESULTS

The ADC was fabricated in 0.13-um CMOS technology. It achieved 85.1 dB DR, 82.6 dB SNDR, and 90.9 dB SFDR within a 2 kHz signal bandwidth with a 32-oversampling ratio (OSR). It consumes 40.8 μW power using a 1.6-V power supply. Calibration added 13 dBs to the SNDR. The die photo is illustrated in Fig. 2.

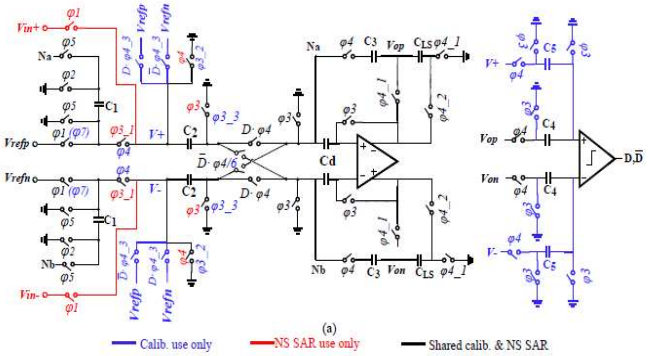


**Fig. 1. Circuit diagram of the active SAR ADC.**

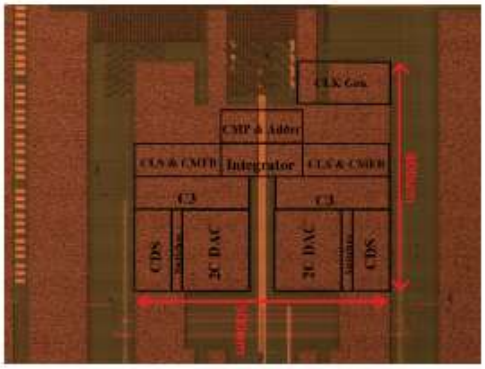


**Fig. 2 Die photo.**

In a related project, novel design techniques have been found for the cancellation of DAC nonlinearities [3], [4].

**Keywords:** Active noise-shaping SAR ADCS, ADCs for MEMS, high-accuracy ADCs, sensor interfaces

## INDUSTRY INTERACTIONS

Texas Instruments, NXP

## MAJOR PAPERS/PATENTS

[1] Shi, L., Zhang, Y. Wang, Y. Kareppagoudr and Temes, G.C., "A 13b ENOB Noise Shaping SAR ADC with a Two-Capacitor DAC," IEEE International Midwest Symposium on Circuits and Systems, Windsor, Ontario, Aug 5-8, 2018.

[2] L. Shi, E. Thaigarajan, R. Singh, E. Hancioglu, U. Moon and G. Temes, "Noise-Shaping SAR ADC Using a Two-Capacitor Digitally Calibrated DAC with 82.6 dB SNDR and 91 dB SFDR," IEEE Trans. on Circuits and Systems-I, vol. 68, to appear.

[3] J. Shakya and Temes, G.C., "Efficient Calibration of Feedback DAC in Delta-Sigma Modulators'" IEEE Trans. on Circuits and Systems-II, v. 67, May 2020, pp. 826-830.

[4] Payandehnia, P., He, T. and Temes, G.C., "Digital Correction of DAC Nonlinearity in Multi-Bit Feedback A/D Converters," (invited) IEEE Custom Integrated Circuits Conference, March 22-25, 2020, Boston, Mass.

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## SIGNIFICANCE AND OBJECTIVES

Battery fuel gauges usually employ a shunt-based Current-Sensing System (CSS). State-of-the-art CSSs consume µWs of power to achieve the required performance. However, many IoT or wearable applications require power consumption in the sub-µW range. This project aims to develop nano-power CSSs suitable for battery fuel gauges.

## TECHNICAL APPROACH

Continuous-Time Delta-Sigma Modulators (CTΔ∑Ms) is a good choice for this task. They have relaxed settling requirements and thus dissipate less power than discrete-time ∑ΔMs. However, due to resistor mismatch, achieving sufficient accuracy is quite challenging. Achieving accuracy and power efficiency is possible by combining a continuous-time front-end with a discrete-time modulator. Moreover, using a voltage reference with the same temperature dependence as the shunt prevents the need for a separate temperature sensor, which boosts the system's energy efficiency.

## SUMMARY OF RESULTS

The block diagram of the proposed current sensor is shown in Fig. 1. An ADC uses a temperature-dependent $V_{REF}$ to digitize the voltage $V_S$ across a shunt. $V_{REF} = V_{PTAT}+V_{CTAT}/\lambda$ where λ can be tuned to match the shunt's TC. Two types of shunts are used in this work: a 20 mΩ on-chip shunt based on four metal layers and a 3 mΩ PCB shunt.

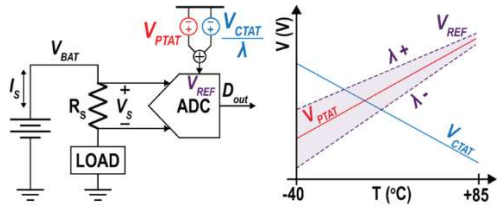


**Figure 1. System block diagram.**

Fig. 2 shows a single-ended block diagram of the fully differential readout circuit. It is based on a 1st order ΔΣ ADC, which has a uniform impulse response and a time-independent response to input pulses. Its continuous-time summing node consists of a capacitively-coupled instrumentation amplifier (CCIA), which allows the modulator to handle beyond-the-rail CM input voltages. Since the scaling factor λ is quite large, it is realized via two feedback paths. One via the CCIA consists of the $V_{PTAT}$-referenced FIR-DAC, and a second via the integrator comprises a $V_{CTAT}$-referenced 1-bit DAC. λ is then the product of the CCIA's gain (25x) and the ratio between $C_A$ and $C_B$.

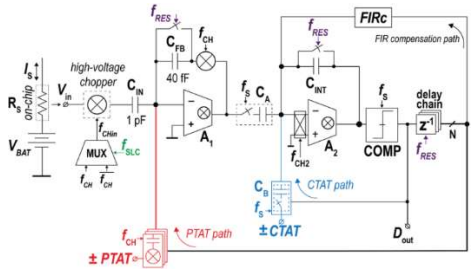


**Figure 2. Single-ended block diagram of the current sensor.**

The capacitive-coupled input uses a high voltage chopper that allows the circuit to sense common-mode input voltages in the range of -0.3V to 5V.

The current sensor is fabricated in a standard 0.18-µm CMOS process and draws 1.4 µA from a 1.8-V supply, of which the on-chip logic draws 600 nA. The decimator is implemented off-chip for flexibility. At a clock frequency of 32 kHz, the current sensor has a resolution of 5.4 $\mu V_{RMS}$ for a conversion time of 15.625 ms.

After a 25°C gain trim and a fixed λ = +500, the measured gain error with the on-chip shunt is less than 0.35% for ±2A currents from −40 to 85 ˚C . With the PCB shunt and λ = -50, this increases to 0.6% over a wider (±15A) current range.

The results mentioned in this report were published [1] at the 2021 Symposia on VLSI Technology and Circuits.

**Table 1. Comparison Table.**

| | This Work | | ISSCC 20 [1] | ISSCC 18 [2] | JSSC 17 [3] | | INA 260 [5] |
|---|---|---|---|---|---|---|---|
| $I_{SUPPLY}$ | 1.4 µA | | < 5 µA | 10.9 µA | 13 µA | | 310 µA |
| Gain Error | on-chip | ±0.35% | ±0.5%* | ±0.9% | on-chip | ±0.3%§ | ±0.5%* |
| | PCB trace | ±0.6% | | | lead-frame | ±0.3%§ | |
| $I_{RANGE}$ | on-chip | ±2A | ±1A | ±4A | on-chip | ±5A | ±10A |
| | PCB trace | ±15A | | | lead-frame | ±36A | |
| Shunt | on-chip | 20 mΩ | 50 mΩ* | 10 mΩ | on-chip | 10 mΩ | 2 mΩ* |
| | PCB trace | 3 mΩ | | | lead-frame | 260 µΩ | |
| Offset | on-chip | 25 µA | < 100 µA | 40 µA | on-chip | 4 µA | 5 mA |
| | PCB trace | 100 µA | | | lead-frame | 400 µA | |
| ICMR | -0.3 to 5 V | | 0 to 60 V | 0 to 25 V | 0 to 0.75 V | | 0 to 36 V |
| $V_{SUPPLY}$ | 1.8 V | | 1.7 to 60 V | 1.5 to 2 V | 1.3 to 1.7 V | | 2.7 to 5.5 V |
| $T_{RANGE}$ | -40 to 85°C | | -50 to 125°C | -40 to 85°C | -40 to 85°C | | -40 to 125°C |
| Tech. | 0.18 | | 0.18 BCD | 0.18 BCD | 0.13 | | |

**Keywords:** current-sensing, shunt-based, symposia on VLSI

## INDUSTRY INTERACTIONS

Texas Instruments, NXP

## MAJOR PAPERS/PATENTS

[1] R. Zamparette and K. Makinwa, “A ±2A/15A Current Sensor with 1.4 µA Supply Current…”, in Proc. Symposia on VLSI 2021.

# TASK 2810.032, DRIVR: A DIGITAL, RE-CONFIGURABLE, UNIFIED CLOCK-POWER (UNICAP) FABRIC FOR ENERGY-EFFICIENT SOCS

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## SIGNIFICANCE AND OBJECTIVES

Integrated Voltage Regulation (IVR) -- remains a critical technology for driving sustained efficiency in SoCs, offering buck converter efficiencies without additional bulky components. The objective of this effort is to devise a domain-scalable run-time programmable IVR fabric that drives and leverages advances in adaptive clocking and SIMO design (Fig. 1).

## TECHNICAL APPROACH

The design effort is organized into four thrusts: (1) Analyzing the effectiveness of UniCaP in designs with large insertion delay; (2) Demonstrate domain-scalable SIMO implementation, critical to providing the necessary flexibility required for a dynamically programmable IVR fabric; (3) Investigating optimal design-time allocation cross-bar switch allocation which connects modules to domains based on SoC usage profiles; and (4) Designing a tileable buck architecture and that can be configured at run-time either as a single-buck, a phase in a multi-phase buck, or a SIMO converter. The goal of the effort is to implement a test chip demonstration that incorporates all four efforts.

## SUMMARY OF RESULTS

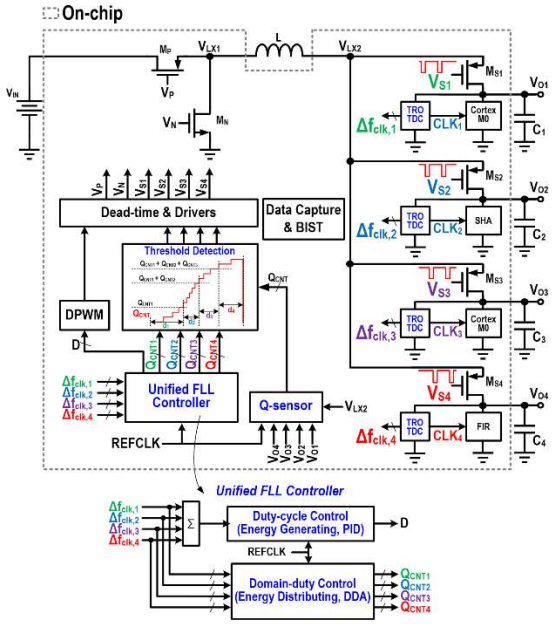


**Figure 1. Implemented SIMO-regulated SoC featuring UniCaP and Dynamic Droop Allocation (DDA) for concurrent domain control to address cross-regulation.**

Goals 1 and 2 of our technical approach have been accomplished – we recently successfully implemented a SIMO-regulated SoC that avoids the prohibitively large $V_{dd}$ margins required in prior implementations (Fig. 2). We are currently evaluating low-complexity run-time algorithms to concurrently determine per-domain $V_{dd}$ and domain allocation for DRIVR, and methodologies for determining partial crossbar connectivity.

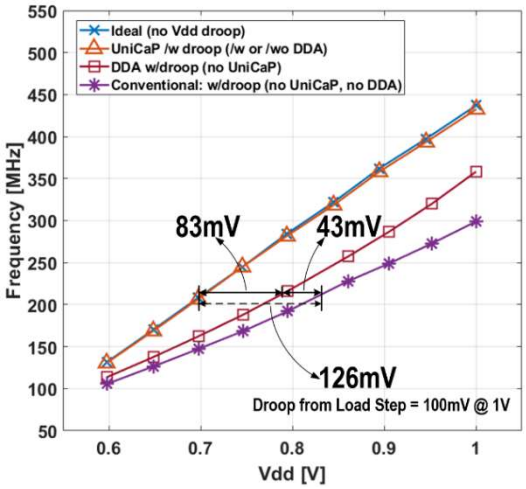


**Figure 2. Measured f-max data from the SIMO-regulated SoC demonstrating the effectiveness of the UniCap and DDA techniques.**

The SIMO effort has highlighted the need to address the severe voltage margins required for robust operation – only 40% of the energy delivered to the system is used to produce useful computing work -- before the technology can be considered for broader adoption in digital SoCs.

**Keywords:** UniCaP, SIMO, Configurable Voltage Regulation

## INDUSTRY INTERACTIONS

NXP, Intel, ARM

## MAJOR PAPERS/PATENTS

[1] Huang, C-H, et al., "A Single-Inductor 4-Output SoC with Dynamic Droop Allocation and Adaptive Clocking for Enhanced Performance and Energy Efficiency in 65nm CMOS," ISSCC 2021.

[2] Sun, X., et al., "UniCaP-2: Phase-Locked Adaptive Clocking with Rapid Clock Cycle Recovery in 65nm CMOS," VLSI Symposium 2020.

# TASK 2810.034, ALWAYS-ON KEYWORD SPOTTING BASED ON ANALOG-MIXED-SIGNAL COMPUTING HARDWARE

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## SIGNIFICANCE AND OBJECTIVES

The primary goal of the project is to create hardware-design knowledge and techniques on analog-mixed-signal (AMS) hardware for artificial intelligence (AI) and machine learning (ML) related computing. Specifically, we will create AMS hardware that can provide significant benefits in scaling power consumption in acoustic signal classification tasks.

## TECHNICAL APPROACH

We will conduct the planned research as follow. (i) We will design *new feature extraction AMS hardware that uses non-linear circuits*. (ii) We will develop the compact model of the non-linear AMS hardware, and by using the developed compact model, we will develop *a training model that can effectively tolerate the variability of AMS computing hardware*. (iii) We will design a matching back-end *classifier based on a deep neural network (DNN)*. We will develop the digital circuits to map the model at minimal leakage/power consumption. By combining the developed architecture/techniques, we will prototype one test chip for the AMS front end and another for the end-to-end multi-keyword recognition.

## SUMMARY OF RESULTS

In the last year from May/1/2020 to Apr/30/2021, we have designed, prototyped, and tested ultra-low-power keyword spotting (KWS) hardware and published the results in [1]. The key task was to design and tape out the new chip titled normalized acoustic feature extractor (NAFE). Recent KWS chips achieved very low power consumption down to ~500nW. But the edge devices usually work in a different environment, receiving various background noises. It is important to maintain a high accuracy across SNR levels and noise types including those that are not considered during training.

Most of the recent KWS chip designs adopt noise-dependent training, i.e., training for a specific signal-to-noise ratio (SNR) and noise type. For this reason, their accuracies tend to degrade for different SNR levels and noise types that are not targeted during training (Figs. 1(a), (b)).

To improve robustness, the noise-independent training could be used, which is to use the training data that includes all the possible SNR levels and noise types. But this approach is challenging for an ultra-low-power device since it demands a large neural network to learn all the possible features. A neural network of a fixed size has its memory capacity limit and reaches an accuracy plateau if it has to learn more than its limit (Fig. 1(b)).

In our NAFE chip, we leveraged the post-processing element from a biological acoustic system which is called divisive normalization (DN). It helps the biological system to maintain acoustic prediction accuracy even in varying noise conditions. Fig. 2 shows the overall architecture of the NAFE chip.

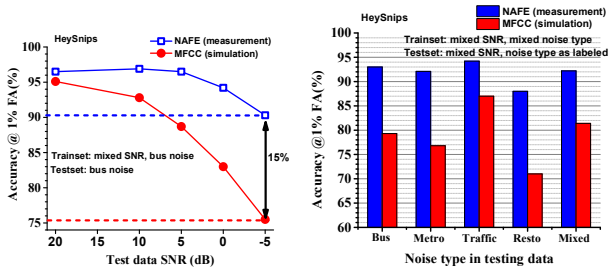


**Figure 1. Proposed KWS hardware achieves the high accuracy (left) across a wide range of SNR levels and (right) under noise scenarios that are not considered in training time**

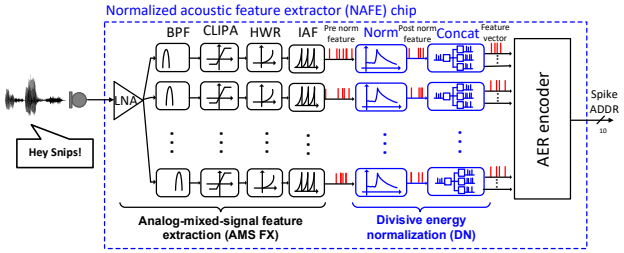


**Figure 2. The architecture of the NAFE chip**

We integrated the NAFE chip with the SNN chip [2] that we prototyped in the same technology at the board level and thus forming an end-to-end KWS system. Both chips are fully event-driven, so is the KWS system, which as a result consumes near-zero power when there are no significant input activities. At the highest activity, it consumes less than 500 nW.

**Keywords:** Keyword spotting, speech command recognition, AMS computing hardware, signal to feature conversion, deep neural networks

## INDUSTRY INTERACTIONS

Intel

## MAJOR PAPERS/PATENTS

[1] D. Wang, et al., "A Background-Noise- and Process-Variation-Tolerant 109-nW Acoustic…," ISSCC, 2021

[2] D. Wang, et al., "Always-On, Sub-300nW, Event-Driven Spiking Neural Network based on Spike-…,"ASSCC, 2020

# TASK 2810.035, COMPUTATIONALLY CONTROLLED INTEGRATED VOLTAGE REGULATORS

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## SIGNIFICANCE AND OBJECTIVES

The enhanced spatio-temporal control afforded by Integrated Voltage Regulation (IVR) in modern SoCs is critical to achieving efficiency, provided they can maintain or improve voltage droop despite reduced available decap. This effort examines computationally intensive IVR control strategies to improve the robustness and settling times of buck and LDO designs.

## TECHNICAL APPROACH

The design effort is organized into two key thrusts (1) Using "computational control" to achieve time-optimal transient response to random switching load current profiles typical of SoCs. (2) Addressing a key weakness in digital LDOs--their prohibitive Power Supply Rejection performance--to advance the state of the art in the transient response of digital LDOs. The main approach toward Thrust 1 will be to evaluate the use of Model Predictive Control (MPC) for a rapid transient response. This effort seeks to demonstrate the effectiveness, and the limits of more advanced control strategies on regulator design using test-chip demonstrations in 65-nm CMOS.

## SUMMARY OF RESULTS

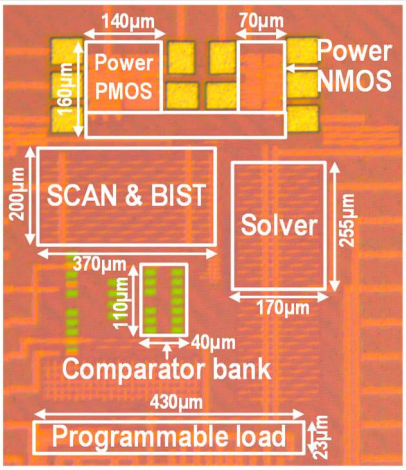


**Figure 1. MPC-buck test chip implemented in 65-nm CMOS. MPC allows time-optimal control to be achieved for the first time under random load current conditions.**

We have achieved our objective of demonstrating the effectiveness of computational control under tight latency constraints by demonstrating MPC for a buck regulator (Fig. 1). To meet the stringent sub-5ns latency imposed by the application, the regulator relies upon the MPC problem formulation from a problem of per-iteration constrained optimization (exceedingly computationally and latency intensive) to a much simpler problem of constraint satisfaction. The result is the first-ever time-optimal buck regulator under random loading conditions. Measurements show the superior settling-time performance of the system (Fig. 2). Notably, the MPC computations account for the non-linear operation of the buck under duty-cycle saturation conditions. Under duty-cycle saturation conditions, the MPC controller tracks not only the voltage error of the system, but also the *latent-charge* in the inductor that will be delivered to the system as the inductor current ramps back from its peak, higher-than-load-current value to match the load current. This calculation allows the system to achieve stable, time-optimal response under random loading conditions which are expected from an SoC. Such operation which cannot be accounted for by either existing ToC techniques or simple linear feedback PID control.

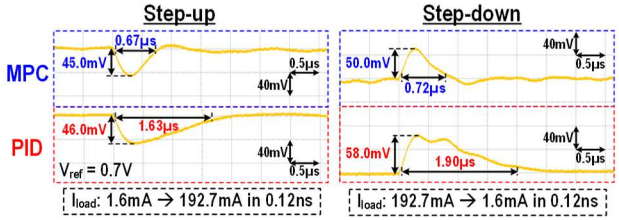


**Figure 2. Measured waveforms showing the voltage response of an MPC buck and a conventional, optimally tuned PID controller. The proposed approach provides near optimal settling time.**

We have also identified a mechanism that exploits computation to address both the non-linearity of Digital LDOs as well as their PSRR limitations. We are currently preparing a test-chip design to evaluate the effectiveness of the approach.

**Keywords:** Model-predictive control, Voltage Regulation

## INDUSTRY INTERACTIONS

Intel, NXP, ARM

## MAJOR PAPERS/PATENTS

[1] Sun, X., et al., "Model Predictive Control of an Integrated Buck Converter for Digital SoC Domains in 65nm CMOS," VLSI Symposium 2020.

# TASK 2810.039, DEVELOPMENT OF COMPACT AND LOW COST FULLY INTEGRATED DC-DC CONVERTER WITH RESONANT GATE DRIVE AND INTELLIGENT TRANSIENT RESPONSE

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## SIGNIFICANCE AND OBJECTIVES

Fully integrated DC-DC converters offer lower cost, lower form factors, and higher adaptability to the chip's real-time demands. During this year, we aim at developing circuit techniques such as resonant gate drive, autonomous resonant control, multi-core power train for fully integrated buck converter to achieve the state-of-art energy and area efficiency.

## TECHNICAL APPROACH

In this period, we have developed novel circuit techniques for a fully integrated buck converter. We have developed a concrete design methodology for on-chip inductor optimization with a 35% loss reduction. We have developed a series of novel circuit techniques to achieve optimal energy and area efficiency for buck converters including resonant gate drive techniques for reducing switching energy loss, associated automatic resonant tuning technique, CCM/DCM switching techniques, and multi-core power train techniques. The circuit techniques allow us to achieve the state-of-art energy efficiency, power density, and large dynamic range in a 65-nm prototype design which will be taped out in near future.

## SUMMARY OF RESULTS

We are focusing on circuit techniques for the fully integrated buck converters. By comparing 10 different topologies of inductors, we have arrived on a methodology that leads to optimal inductor design for on-chip buck converters. Details have been included in prior reports. In circuit design, we have developed a series of techniques to improve the efficiency of on-chip buck converters. Fig. 1 shows the power train schematic of the power core and the layout of the prototype buck converter test chip which includes 10 highly optimized power cores. The use of multiple smaller power cores allows use of more optimized small-size inductors to deliver higher output power while maintaining high scalability of the power level. The two-transistor stacked power train design allows use of core transistors at an IO input voltage level of 1.8V or above. As a result, we can significantly extend the input and output range of the design leading to a broader application space for the design.

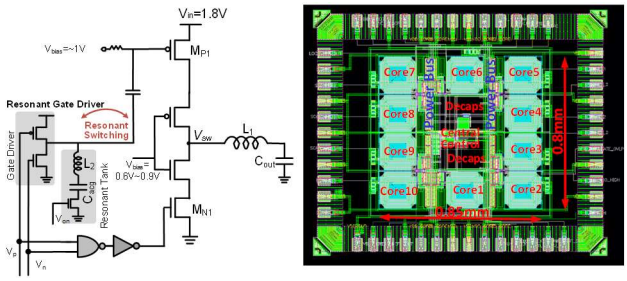


**Figure 1. Schematic of the power train of a single core and finished chip top layout with scalable 10 power cores.**

The power train adopts a resonant gate drive technique where a small resonant inductor is used to reduce switching power loss through resonance operation. This is particularly useful for high-speed converters at near 1GHz as in our design. The resonant operation brings 2~5% efficiency improvement with only 6% area overhead. To assist precise resonant control, a novel charge pump-based resonant tracking circuit is built to automatically adjust the timing of the resonant switches. In addition, DCM mode based on zero-crossing voltage detection is deployed to the design to further extend the dynamic range at low power mode. A complete inductor design methodology was also developed to achieve optimal inductor efficiency for fully integrated design.

Overall, by combining several novel circuit techniques, e.g., resonant gate drive, automatic resonant tracking, and a scalable architecture with multi-core power trains, we aim to achieve a high-power efficiency above 80% with a state-of-art power density above 1W/mm$^2$ for fully integrated power converters. A 65-nm test chip has been designed and is at the final stage of tape out. In the next project period, we will first prepare and perform chip testing and then explore system-level techniques for a transient response as described in the proposal.

**Keywords:** Fully integrated buck converter, resonant gate drive, automatic resonant control, CCM and DCM control, on-chip inductors

## INDUSTRY INTERACTIONS

Texas Instruments, IBM, Intel

## MAJOR PAPERS/PATENTS

# TASK 2810.040, HYBRID/RESONANT SC CONVERTERS WITH INTEGRATED LC RESONATOR FOR HIGH-DENSITY MONOLITHIC POWER DELIVERY

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## SIGNIFICANCE AND OBJECTIVES

Fully integrated power management is important for a variety of computing and communication applications but is difficult due to the limitations of on-chip passive components. This project explores a new direction using distributed LC-resonators in hybrid switched-capacitor architectures to manage high-frequency losses and expand efficiency and power density.

## TECHNICAL APPROACH

This work involves co-optimization of high-frequency DC-DC converters based on hybrid-resonant switched capacitor architectures and distributed planar-spiral LC resonators. A variety of analytical and numerical methods are used to model skin- and proximity-effect losses in planar magnetics which use capacitive dielectrics to ballast and homogenize current density. Several circuit topologies are under study spanning nominal 2:1 resonant converters as well as higher conversion ratios using Series-Parallel and Dickson architectures. Circuit design is completed in Cadence with a tapeout completed in March 2021; E&M simulation was completed in Sonnet and other tools.

## SUMMARY OF RESULTS

This work builds on past efforts in fully-integrated voltage regulation (FIVR), with specific aims to 1) improve passive component utilization through the use of electromagnetic ballasting, 2) leverage new architectures that benefit from high energy-density on-chip capacitors, and 3) explore new on-chip control, regulation, and timing optimization such as autotuned zero-current and voltage switching. A theoretical analysis was presented in Q4 2020 in IEEE COMPEL [1] which outlines certain design tradeoffs and optimization procedures, verified by EM simulation and measured data.

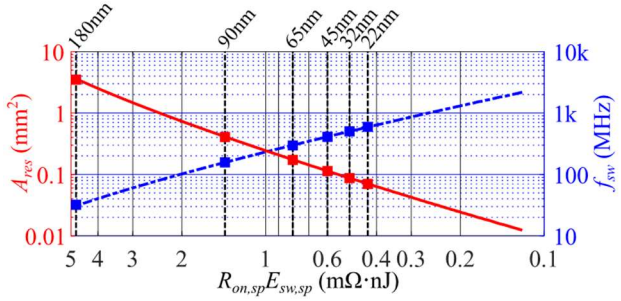


**Figure 1. Scaling analysis: required on-chip die area decreases significantly with advanced process technologies [1].**

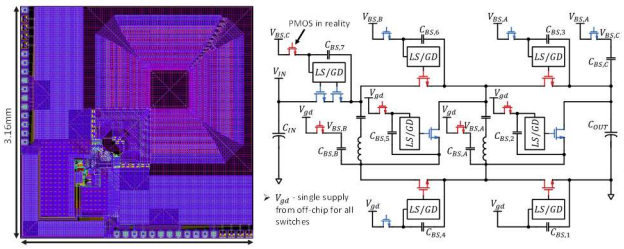


**Figure 2. March 2021 Tapeout: Cadence layout snapshot and high-level schematic with gate-drive/bootstrap scheme.**

Illustrated in Figure 1, Background theoretical studies showed that the concept presented here improves significantly with process technology. Overall, this demonstrates a solid roadmap to (90%+) efficiency at moderate-high power density (up to 1W/mm$^2$) with reasonable cost of an integrated solution.

A next-generation prototype tapeout was completed in March 2021 with expected sample delivery in July 2021. Shown in Figure 2, the design includes auto-tuned zero-current switching and variable output voltage regulation while operating between 40-60MHz and using fully-integrated passive components. The new design uses a nominally 3:1 series-parallel resonant switched capacitor converter, where the on-chip spiral magnetics use integrated ballasting to enforce uniform current density. The design required significant effort on the bootstrap and gate-drive scheme as well as fast instrumentation to sample output voltage and inductor current for feedback regulation. The design is implemented in 180-nm bulk CMOS, but the concepts should also be applicable in more advanced nodes.

**Keywords:** Power Management, DC-DC Converters

## INDUSTRY INTERACTIONS

NXP, Intel, Texas Instruments

## MAJOR PAPERS/PATENTS

[1] P. McLaughlin, et al., "Modeling and Design of Planar-Spiral Merged-LC Resonators in a Standard CMOS Process," IEEE COMPEL 2020.

[2] P. McLaughlin, et al., "A Fully Integrated Resonant Switched-Capacitor Converter with 85.5% Efficiency at 0.47W Using On-Chip Dual-Phase Merged-LC Resonator," ISSCC 2020.

[3] P.H. McLaughlin, et al., "A Monolithic Resonant Switched-Capacitor Voltage Regulator with Dual-Phase Merged-LC Resonator," JSCC 2020.

# TASK 2810.042, DIGITALLY ENHANCED HIGH EFFICIENCY, FAST SETTLING AUGMENTED DCDC CONVERTERS

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## SIGNIFICANCE AND OBJECTIVES

State-of-the-art digital loads impose challenging requirements for power-supply regulators to provide fast-transient currents. Fast-transient response improvement techniques utilizing auxiliary circuits have become popular due to their enhanced efficiency and design flexibility. Our goal is breaking the efficiency/dynamic-response/settling-time trade-off in conventional dcdc converters, by developing high-speed, digitally controlled augmented power stages with optimal load current control and settling time.

## TECHNICAL APPROACH

In the proposed augmented power converter topology, an auxiliary stage with a small inductor, high switching rate converter shares the load capacitor with the main stage providing fast settling under fast-load-transients. We will develop an observer-based load capacitor current estimator to control the auxiliary stage, having it work as a Current-Controlled-Current-Source. Given the specific supply-voltage regulation window, this system achieves a fully integrated solution that requires a smaller (3~4x) external capacitor size, which is significantly compatible and adequate for low-cost mass-production. For design, characterization, and validation of the proposed system, Arizona State University Connection One Research Labs will be used, which provides all necessary CAD/EDA design software/tools (Matlab, Cadence/Virtuoso) and test equipment for characterization.

## SUMMARY OF RESULTS

This project started in Feb 2020. During system-level design, different control schemes (PWM, hysteretic, Constant-On/Off-Time) and control modes (voltage mode, current mode, emulated current mode) for the main-stage have been analyzed in terms of settling speed and stability. Digital nonlinear controls (single-cycle, multi-cycle, or multiple-single-cycle correction) for the aux stage have been investigated. VerilogAMS models are used to build the transient detector and control logic. The system block diagram is shown in Figure1. The timings for digital control ($t_1$, $t_2$, $t_3$) are computed in an analog way for high cost/energy efficiency. The transistor-level schematic design is almost completed. The block-level layout is ready to start. The planned tape-out date is September 2021. The preliminary results of load transient response are shown in Figure 2.

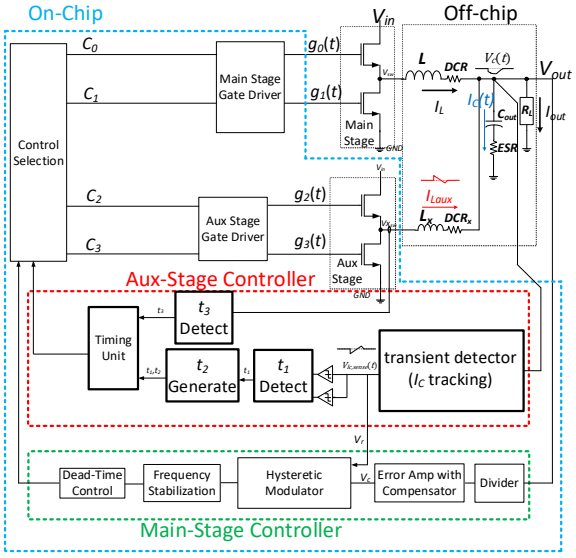


**Figure 1. Block Diagram of Augmented DCDC Buck Converter with Proposed Transient-Detector, Aux-Stage and Nonlinear Controller.**

From the comparison we can clearly see that the output voltage deviations under load current steps are reduced significantly.

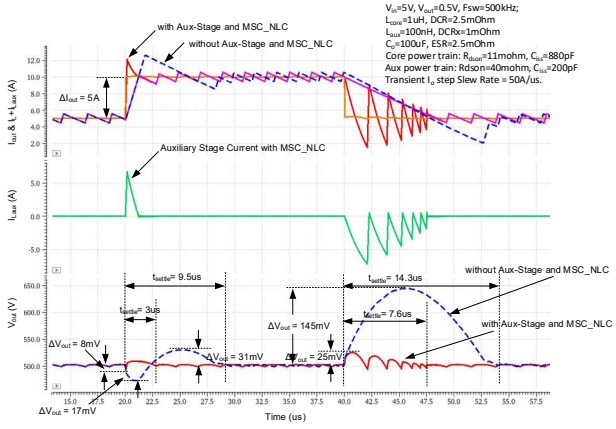


**Figure 2. Load Transient Response with and without the Aux-Stage and MSC_NLC.**

**Keywords:** augmented converter, fast transient detector, fast settling, high efficiency, digital nonlinear control

## INDUSTRY INTERACTIONS

NXP, Intel, IBM

## MAJOR PAPERS/PATENTS

# TASK 2810.049, 1-W BATTERY-CHARGING CMOS BUCK REGULATOR

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## SIGNIFICANCE AND OBJECTIVES

Charging batteries (in cell phones) with other batteries (battery banks) is the new normal. Volume and charge life are critical in this space. The objective of this research is to develop a small and power-efficient single-inductor voltage regulator that also charges and conditions a battery for maximum energy.

## TECHNICAL APPROACH

Charging dynamics in Lithium-Ion batteries are largely unaccounted for by conventional chargers, so they do not charge them maximally. The first step in this research is to study, test, and develop charging methods that expand usable energy storage. The second step is to develop an efficient power supply that charges a battery and supplies a load with one inductor. To preserve energy, power flow in all directions should be efficient: input-output, input–battery, and battery–output. The third step is to develop an efficient controller that supplies and regulates the output while charging and conditioning the battery for maximum energy.

## SUMMARY OF RESULTS

The charge-discharge tester in Fig. 1 was designed, simulated, built, debugged, and fully tested. $M_P$, $A_{GP}$, $A_{VP}$, $D_P$, and $R_P$'s set the charge current $i_C$. $M_N$, $A_{GN}$, $A_{VN}$, $D_N$, and $R_N$'s set the discharge current $i_D$. $R_{SH}$ monitors battery current $i_B$ and $R_{THERM}$ monitors battery temperature $T_B$.

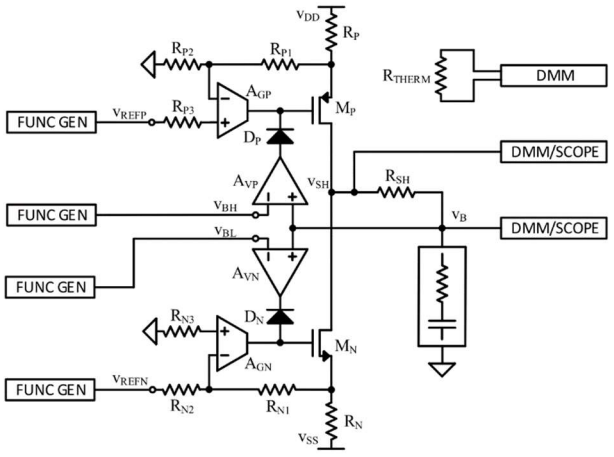


**Figure 1. Charge–discharge tester.**

Unique features of the tester are programmability, high bandwidth, and low distortion. $R_P$'s and $R_N$'s level-shift 5-V signals from the function generator to the ±12-V signals needed to bias $M_P$ and $M_N$. $R_{P3}$ and $R_{N3}$ cancel $A_{GP}$'s and $A_{GN}$'s input-current errors. $A_{GP}$, $R_P$'s, $A_{GN}$, and $R_N$'s close feedback loops that program $i_C$ and $i_D$. $A_{VP}$, $D_P$, $A_{VN}$, and $D_N$ disrupt $A_{GP}$'s and $A_{GN}$'s actions when $v_B$ reaches battery-high and -low targets $v_{BH}$ and $v_{BL}$.

The tester has been used to charge and discharge batteries with dc, sinusoidal, triangular, ramp, and pulse currents at different frequencies. In the five charge–discharge cycles in Fig. 2, steady $i_C$'s preconditioned $v_B$, sinusoidal $i_C$'s charged $v_B$, $v_B$ rested ("relaxed") across a fixed period, and steady $i_D$'s discharged $v_B$. Charge time was fixed, start-of-charge voltage was 3.8 V, and end-of-discharge voltage was 3.4 V. Experiments are on-going.

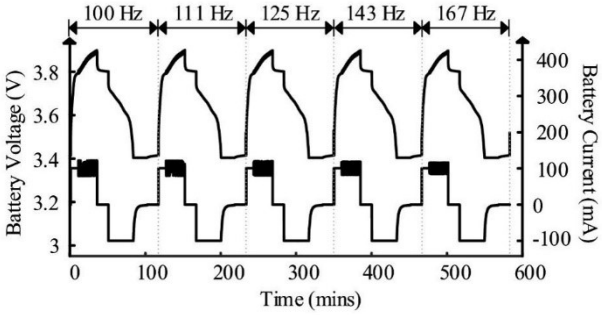


**Figure 2. Five measured charge–discharge cycles.**

The goals for 2020–2021 were to study the state of the art, develop test strategies, build a tester, and test batteries. The goals for 2021–2022 are to design, build, and test a CMOS power stage that can supply a load and condition and charge a battery with the maximum efficiency.

The feedback controller is next. The key here is to regulate the output and charge and condition a battery so it can hold the highest possible energy in the shortest possible time. In all, the fundamental advantages of this research will be higher energy (Watt–Hour) capacity, higher efficiency, smaller footprint, and lower cost.

**Keywords:** Li-ion charger, voltage regulator, efficiency

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

# TASK 2810.051, HIGH GAIN DC-DC CONVERTER FOR EV TRACTION SYSTEM

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## SIGNIFICANCE AND OBJECTIVES

Experimental validation of the proposed multi-input, high-conversion-ratio DC-DC converter for electric vehicle traction system involving low-voltage battery pack and variable DC link voltage. The proposed architecture increases safety, minimizes cell balancing issues in batteries, eliminates the need for an auxiliary DC-DC converter, and improves the overall efficiency of the system.

## TECHNICAL APPROACH

In EV traction systems, higher voltage motors offer improved efficiency and power density. Also, variable DC link voltage has been shown to improve the overall efficiency of the traction system. The proposed multi-input high conversion ratio converter (HCRC) can achieve high and variable voltage gain (4 to 20 times for a 4-phase converter) with a significant reduction in voltage and current stress across its devices. This enables the use of a 48V battery pack which significantly increases the overall safety. Each phase of HCRC is connected to a separate battery module whose charging-discharging can be independently controlled to achieve cell balancing easily.

## SUMMARY OF RESULTS

A scaled hardware prototype of a 4-phase multi-input HCRC is developed to verify the proposed concept as shown in Figure. 1. Due to the limited testing facility availability, the prototype is rated for 4 kW operating at 48 V input voltage. The output voltage can vary from 200 V to 800 V achieving a conversion ratio of 4 to 17 without any transient spikes in switch voltage or current. The converter has two zones of operation based on the duty ratio of operation. In Zone I (duty > 0.5), the converter has inherent current sharing and low device voltage stress which is not present in Zone II (duty < 0.5) operation.

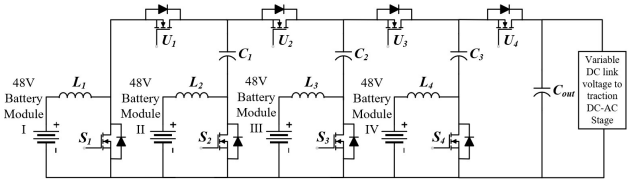


**Figure 1. Proposed 4-phase multi-input high conversion ratio converter for EV traction system.**

The hardware prototype is operated in dual-loop control with an inner current loop and outer voltage loop. The inner current loop regulates the current supplied by each input source while the voltage controller regulates the output voltage to the desired value. The converter can operate at both equal and un-equal current sharing among the different input phases over the whole range of operation with the output voltage regulated to the desired value. The converter has bi-directional power flow capability allowing it to operate in buck mode during regenerative braking in an electric vehicle. The converter operation in both boost and buck mode is verified experimentally through the hardware prototype.

The converter performance for different output voltage and power conditions in boost mode is presented in Table 1. As the converter has low voltage stress across the devices, 650-V SiC MOSFETs are selected which have low on-state resistance to minimize the conduction losses. The converter can achieve a peak efficiency of 98.24% at 48V to 400V, 2 kW. The converter has similar performance results in buck mode where it can achieve 98.16% efficiency for 400 V to 48 V operation at 2 kW, 50 kHz.

**Table 1. 4-phase HCRC performance in boost mode for 48 V input at 50 kHz switching frequency.**

| Output voltage | Output Power | Device Voltage Stress (Bottom / Top Switch) | Efficiency |
|---|---|---|---|
| 200 V | 1000 W | 200 V/ 145 V | 97.4 % |
| 400 V | 2000 W | 100 V/ 200 V | 98.24 % |
| 800 V | 4000 W | 200 V/ 400 V | 97.06 % |

The converter will be further optimized for power density by reducing the inductor size using interleaving among the different input phases which will reduce the input current ripple as well.

**Keywords:** DC-DC Converter, High Gain, Non-isolated boost, Variable DC link voltage, Electric Vehicle Traction System

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] J. Roy, A. Gupta, and R. Ayyanar, "Discontinuous Conduction Mode Analysis of High Gain Extended-Duty-Ratio Boost Converter," in IEEE Open Journal of the Industrial Electronics Society, vol. 2, pp. 372-387, 2021, DOI: 10.1109/OJIES.2021.3077982.

[2] A. Gupta, R. Ayyanar and S. Chakraborty, “Phase-Shedding Control Scheme for Wide Voltage Range Operation of Extended-Duty-Ratio Boost Converter,” Accepted to APEC 2021.

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## SIGNIFICANCE AND OBJECTIVES

With ever-growing electronic devices being employed in electric vehicles, electromagnetic interference (EMI) emission in modern automotive electronics has been record-high. The situation deteriorates further due to high dv/dt and di/dt transients, as more high-end power modules shift to adopt high-performance GaN power switches for faster and more efficient operation. The proposed techniques support effective EMI suppression and minimize switching power losses.

## TECHNICAL APPROACH

To regulate and suppress elevated EMI by automotive power ICs, spread-spectrum modulation (SSM) technique and circuit will be developed. By actively modulating switching frequencies of power circuits at multiple rates, the technique expects to shape EMI spectrum adaptively while accommodating in-cycle zero-voltage switching to accomplish a balanced EMI regulation and power control.

## SUMMARY OF RESULTS

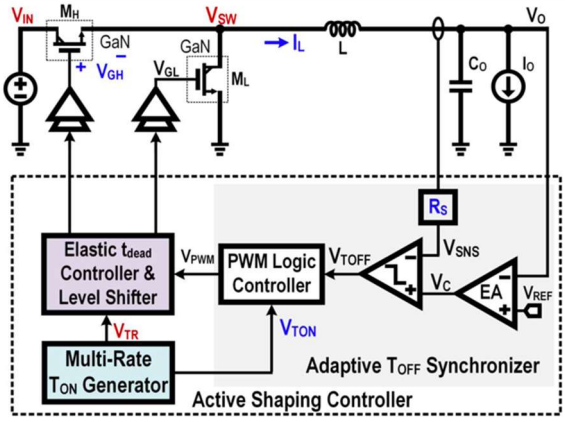


**Figure 1. Block diagram of the proposed GaN power converter.**

Fig. 1 shows the block diagram of the proposed GaN power converter. An anti-aliasing MR-SSM technique is incorporated through an active shaping controller for effective EMI reduction. To implement such, a multi-rate $T_{ON}$ generator is designed, which regulates the on-duty time ($T_{ON}$) with multiple coded rates. Compared to the classic FR-SSM, it successfully achieves a targeted redistribution of EMI energy by adapting the $f_{SW}$ modulation rate to the frequency range. Specifically, as shown in Figs. 2 and 3, a lower $f_{SW}$ is modulated with a faster rate, reducing its occurrence in the time domain. Thus, the EMI energy carried by such a frequency component and its corresponding harmonics is suppressed, eliminating the EMI power aliasing spikes, which are inevitable in the FR-SSM. Meanwhile, the off-duty time ($T_{OFF}$) is adaptively defined by an adaptive $T_{OFF}$ synchronizer. In response to a longer $T_{ON}$, $T_{OFF}$ is extended correspondingly while retaining a near-constant $T_{ON}/T_{OFF}$, and thus a near-constant $V_O$.

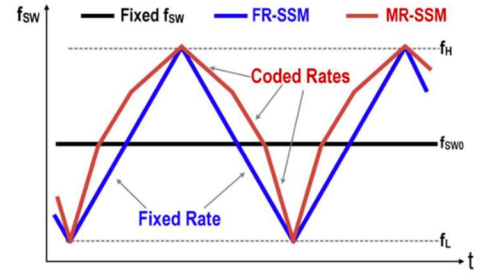


**Figure 2. Comparing MR-SSM to FR-SSM in time domain.**

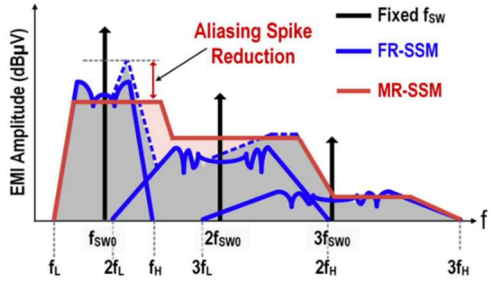


**Figure 3. Comparing MR-SSM to FR-SSM in frequency domain.**

On the other hand, as $f_{SW}$ varies continuously, ZVS operation is difficult to accomplish. Continuously varying peak and valley inductor currents induce extra switching and reverse conduction losses during switching deadtimes. Therefore, the elastic deadtime ($t_{dead}$) controller will be developed to realize in-cycle ZVS by predicting the expected inductor current.

**Keywords:** GaN, FR-SSM, EMI noise, IC security

## INDUSTRY INTERACTIONS

Texas Instruments, IBM, NXP

## MAJOR PAPERS/PATENTS

[1] D. Yan and D. B. Ma, "An Automotive-Use Battery-to-Load GaN-Based Power Converter with Anti-Aliasing Multi-Rate Spread-Spectrum Modulation and In-Cycle ZVS Switching," IEEE Symp. VLSI Circuits, Honolulu, HI, USA, Jun. 2020, pp. 1–2.

[2] D. Yan and D. B. Ma, "An Automotive-Use Battery-to-Load GaN-Based Switching Power Converter With Anti-Aliasing MR-SSM and In-Cycle Adaptive ZVS Techniques," IEEE Journal of Solid-State Circuits, Vol. 57, No. 4, pp. 1186-1196, Apr. 2021.

# TASK 2810.061, TWO-STAGE VERTICAL POWER DELIVERY AND MANAGEMENT FOR EFFICIENT HIGH-PERFORMANCE COMPUTING

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## SIGNIFICANCE AND OBJECTIVES

The project seeks to significantly improve the efficiency of power delivery from high-voltage busses to scaled-CMOS-compatible voltages (<1V) in a vertically and heterogeneously integrated architecture leveraging hybrid and switched-capacitor DC-DC converters. If successfully deployed, it can reduce the number of power pins to the chip by at least 2x and reduce thermal dissipation.

## TECHNICAL APPROACH

The new ambitious approach utilizes a 2-stage vertical power deliver and management (PDM) architecture with an optimal tapered current distribution, combining an integrated 4V-to-1V switched-capacitor voltage regulator (SCVR) stage located within the package substrate, underneath the processing die, along with a 20V/48V-to-4V hybrid voltage regulator module (HVRM) stage on the PCB. The SCVR is co-packaged with deep-trench capacitors where both SCVR and the integrated capacitor interposer dies can be thinned so that they can fit within the C4 bump height. The architecture enables ~2x reduction in package PDM pins with 4x to interconnect loss reduction; resulting in a ~1.5x increase in available data IO pins.

## SUMMARY OF RESULTS

The research team's efforts have been focused on detailed analysis, optimization, and power stage simulations of the two converter designs and Gen.1 designs of the converters with all detailed schematics and layout in the last 6 months.

In the SCVR design, the team also works with our industry partner, Murata, to co-design a package substrate with new integrated passive devices (iPDs) that can be isolated from each other to implement flying capacitors for the SCVR converter. Since this is a rare support and technology opportunity from our industry partner to demonstrate integration with iPDs, our research team applied an industry procedure of designing the pads and package integration in parallel with schematic design and completed package design even before our active silicon tape-out. This gives our Ph.D. students unique training in co-design of a package and an IC. The package substrate is now in fabrication and will be ready by our chip fab-out later this year.

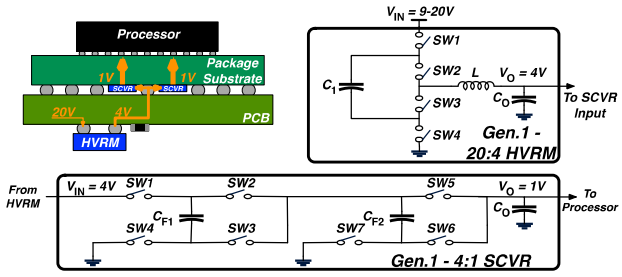


**Figure 1. Architecture of the two-stage vertical power delivery for Gen.1 specifications of 20V-to-1V conversion. Two converter designs are implemented on 65-nm (SCVR) and 180-nm (HVRM) processes.**

Regarding the two converter designs, multiple new circuit techniques have been introduced to improve their performances. The SCVR is implemented on a 65-nm process, while the HVRM in a 180-nm process, both will use flip-chip bumping to reduce parasitic resistances. In addition to the new efficient combination of two 2:1 SC converters in the topology, the SCVR employs a novel adaptive frequency control that optimally combines a PI control with a fast lower-bound control to achieve fast transient response, efficient steady-state regulation, as well as smooth transition between the two control modes across the load range. While these two modes of control are not new, utilization of both modes and achieving smooth transitions at any load point is a significant new contribution. The HVRM design exhibits multiple design advances, including a new design of voltage regulation loop with flying capacitor voltage balancer, a new soft-start startup mechanism, and new high-voltage level shifter circuits. The HVRM full design achieves 95% efficiency, while SCVR achieves 94%.

The two designs are at the top-level integration. In the next 6 months of the project, we will report the experiment results of the Gen.1 designs of the two converters and the system, as well as start designing the Gen.2 with more stringent specifications.

**Keywords:** vertical power delivery, power management, DC-DC converter, switched-capacitor, hybrid converter

## INDUSTRY INTERACTIONS

Texas Instruments, IBM, Intel, and NXP

## MAJOR PAPERS/PATENTS

# TASK 2810.065, POWER-EFFICIENT AND RELIABLE 48-V DC-DC CONVERTER WITH DIRECT SIGNAL-TO-FEATURE EXTRACTION AND DNN-ASSISTED MULTI-INPUT MULTIPLE-OUTPUT FEEDBACK CONTROL

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## SIGNIFICANCE AND OBJECTIVES

The goal of the project is to embed deep-neural-network (DNN) assisted digital feedback control systems for a 48V DC-DC converter for the data center application. The proposed control systems will enable two sought-after capabilities, namely the maximum PCE point tracking, and the in-field reliability diagnostics and remedy while consuming a small amount of hardware and energy.

## TECHNICAL APPROACH

We will develop mainly two features. First, we will design a digital DNN-assisted controller for tracking the maximum power conversion efficiency (PCE) point. It will take multiple inputs such as average load levels in the past and present monitoring windows. Then, it modulates several parameters such as duty cycle, switching frequency, dead zones, and switch widths. Second, we will develop long-term reliability diagnostics. We will focus on the long-term degradation of output capacitors and power switches. Capacitor aging, for example, induces an effective series resistance increase. To track them we will monitor the power spectral density of the output voltage. To reduce hardware overhead, we will recycle the hardware for the two features.

## SUMMARY OF RESULTS

We have first reviewed, compared the published 48V-to-1V converter topologies. Then, we have chosen and designed the 20-level series capacitor typology (Fig. 1). We augmented it with the gate width modulation technique to enable high PCE over a range of load current.

The multi-level series capacitor buck converter is chosen due to its lower power loss due to switch devices. By introducing series capacitors at each level, we can divide the converter with a high step-down ratio into multiple sub-converters with a lower step-down ratio. This allows each sub-converter to employ the *on-chip* power FETs which have superior figure-of-merits (FoM) than *off-chip* counterparts. This results in smaller conduction and switching loss and high PCE.

We chose the number of levels to be 20 to optimize the power loss while avoiding the short-circuit current in the high-side switches. Fewer levels would (i) increase the voltage tolerance requirement of switches, (ii) enlarge the current in each sub-converter, and (iii) require additional LDOs to regulate switch drivers' power supply. They all increase power loss. On the other hand, more levels would have a high risk of causing on-time overlapping in the high-side switches.

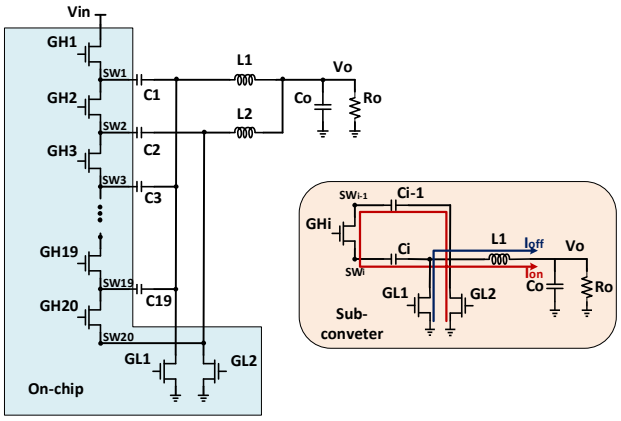


**Figure 1. (left) 20-level series-capacitor buck converter architecture; (right) A sub-converter for each level.**

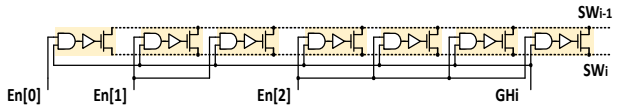


**Figure 2. Gate width modulation technique, one switch is divided into 7 segments.**

To keep a high PCE over a range of load current, we have investigated the trade-off between the conduction loss and driver loss at a different load level through the gate width modulation (Fig. 2). By controlling the enable bits, *En[2:0]*, we can increase the switch width at heavy load to reduce the conduction loss, while decreasing the switch width to reduce the driver loss at light load.

**Keywords:** Multi-level series capacitor buck converter, gate width modulation, power conversion efficiency (PCE)

## INDUSTRY INTERACTIONS

IBM, Intel, Texas Instruments

## MAJOR PAPERS/PATENTS

# TASK 2810.067, HIGHLY EFFICIENT EXTREME-CONVERSION-RATIO BUCK HYBRID CONVERTERS

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DEUKHYOUN HEO AND JANA DOPPA, WASHINGTON STATE UNIVERSITY

## SIGNIFICANCE AND OBJECTIVES

The overarching goal of this project is to design and demonstrate a high-performance energy-efficient voltage regulator with an extreme conversion ratio and high power density. The innovations in the circuit-level design will be complemented with a new machine learning-enabled optimization framework.

## TECHNICAL APPROACH

This research aims to develop: (a) a novel single-input-single-output (SISO) inductor-first hybrid buck converter with an extremely high conversion ratio, high efficiency, high power density, and full step-down conversion range; (b) a single-input-multi-output (SIMO) extreme-conversion-ratio hybrid converter that simultaneously produces a full range of output voltage, maintains high efficiency, high power density, low cross-regulation, and fast response; (c) a machine-learning (ML)-based framework to optimize the circuit parameters of SISO and SIMO inductor-first hybrid converters.

## SUMMARY OF RESULTS

We are investigating the system-level architecture of the SISO extremely high conversion ratio (EHCR) inductor-first hybrid (IFH) buck converter. The EHCR power stage is the crucial innovation in this research. In the initial design, an off-chip inductor and off-chip flying capacitors are employed to handle the high power requirement of the output and reduce the prototype cost arising due to the silicon area while considering the various performance trade-offs.

All other components, including power switches, drivers with a power supply generator, and a control feedback loop, are fully integrated on-chip and are designed using the TSMC 180-nm CMOS technology in Cadence virtuoso environment to keep a compact form-factor.

The operation principle of the EHCR power stage is presented in Fig. 1. The proposed power stage contains a power inductor and a reconfigurable switched-capacitor power stage (SCPS). When the conversion ratio is within the range between N and N+1, The node voltage of $V_x$ will be reconfigured to (N+1)x of $V_{out}$ in phase 1 and Nx of $V_{out}$ in phase 2. Thus, this power stage can achieve a steady-state by using a pulse width modulation (PWM) control method. Using the inductor voltage-second balance during the steady-state, the output voltage regulation is performed by the duty cycles of the control signals of the two phases. This power stage ensures the voltage across the inductor is consistently lower than the output voltage value. Thus, the inductor current ripple is minimized in any conversion ratio to reduce the AC switching loss.

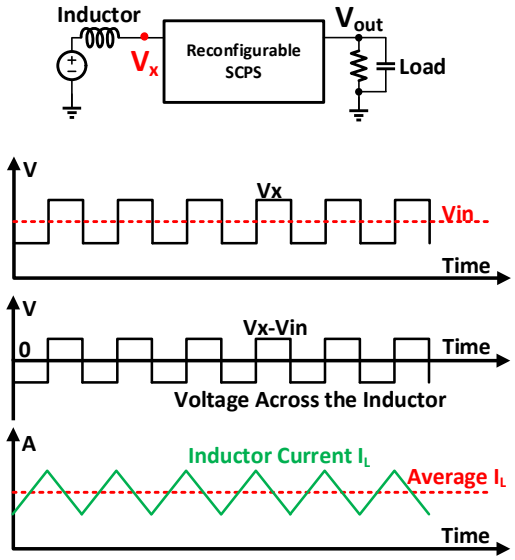


**Figure 1. Proposed high-conversion-ratio (HCR) inductor-first hybrid converter.**

We are now working on verifying the functionality and performance of the power stage. We are also developing the ML-based optimization framework at the same time. This new algorithm will be applied to optimize the parameters of the EHCR power stage after the verification. In the next few months, we will develop a new PWM feedback controller to minimize the hard-charging loss in the power stage. The designed SISO EHCR will be fabricated, and the measurement will be completed by mid 2022.

**Keywords:** extremely high conversion ratio, buck converter, hybrid topology, ML-optimization

## INDUSTRY INTERACTIONS

Intel

## MAJOR PAPERS/PATENTS

# TASK 2810.068, ACTIVE EMI FILTERING WITH SWITCH-MODE AMPLIFIER FOR HIGH EFFICIENCY

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## SIGNIFICANCE AND OBJECTIVES

EMI filters are necessary components of power converters. Passive filters are bulky and expensive, and typical active filters can consume unacceptably large powers. The objective of this research is an EMI filtering approach with a 10x smaller size than passive filters and 10x more efficiency than typical active filters.

## TECHNICAL APPROACH

We replace the linear amplifier universally used in active EMI filters with a GaN-based switch-mode amplifier for high efficiency. The amplifier switches at 31-100 MHz with a control bandwidth of 5+ MHz and is capable of filtering most of the EMI range with high (>90%) efficiency and small size. We further use innovative control techniques to achieve high loop gain (>>40 dB) over a relatively narrow bandwidth (~1 kHz - ~5 MHz).

## SUMMARY OF RESULTS

A complete design has been completed and simulated (full switching model, not small-signal equivalent). The switch-mode amplifier has a simulated efficiency of over 90% at 60 MHz switching frequency with a small size.

The control implementation is a particular challenge. The active EMI filter should have low gain at low frequency to avoid affecting the control of the power converter under test, especially for power factor correction applications with expected input voltage variations at harmonics of the line frequency. The filter should also have a high-frequency cutoff at about one-tenth to one-fifth of the amplifier switching frequency to ensure the validity of the amplifier small-signal model. Thus, the loop gain of the filter has a limited bandwidth (~500 Hz – 5 MHz) where gains greater than 0 dB are acceptable, and it is important to maximizing the gain (i.e., the filtering capability) over this frequency range while maintaining acceptable phase margin at the crossover frequencies. Considering Bode's gain-phase relationship, it is ordinarily difficult to achieve more than 20 dB/decade or 40 dB of total loop gain with a linear system.

The 40 dB gain limit can be overcome through the addition of a fractional-order filter, which uses repeated patterns of poles and zeros to approximately maintain an intermediate value of gain slope and phase compared to an ordinary pole or zero (for example, 45 degrees of phase and 30 dB/dec). A fractional-order differentiator is included in Figure 1 which allows the system to achieve a maximum of 60 dB of loop gain in the same bandwidth. This permits three orders of magnitude higher critical frequency for a passive filter (1000x smaller size) and one order of magnitude higher frequency than would be possible without the fractional-order filter.

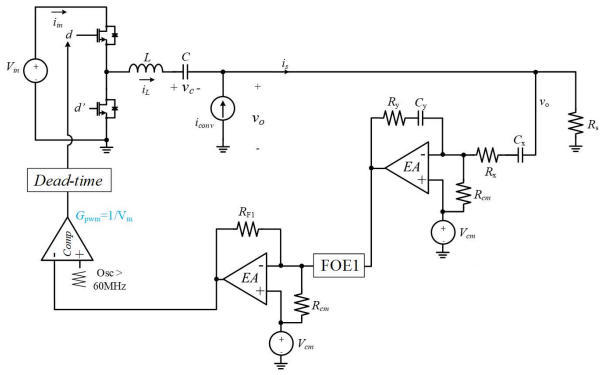


**Figure 1. The architecture uses a switch-mode amplifier (top left) to actively filter the ripple current from the power converter $i_{conv}$. In this version, a fractional-order filter helps achieve large gain over limited bandwidth.**

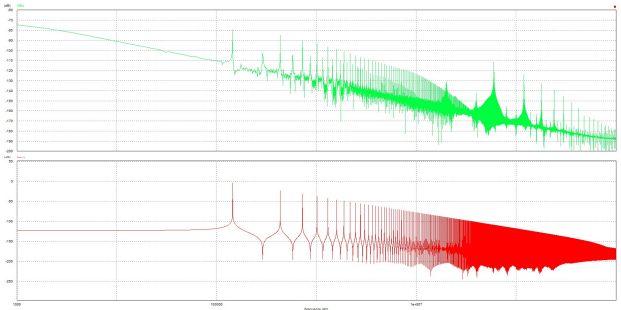

**Figure 2. A full switching simulation at 60 MHz shows the architecture achieving over 60 dB of current attenuation at the converter fundamental and important harmonics.**

**Keywords:** electromagnetic interference, EMI filter

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

# TASK 2810.072 AND 2810.073, AI/ML EDGE HARDWARE FOR ULTRA-RELIABLE WIRELESS NETWORKS

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## SIGNIFICANCE AND OBJECTIVES

In high-speed wireless communication systems, non-constant envelope modulation standards increase spectral efficiency which requires increased linearity. These are achieved currently using cumbersome offline digital pre-distortion techniques. An AI/ML time-domain neural network processor that uses area/energy efficient time-domain quantized neural networks will be developed and demonstrated for on-chip online *in-situ* calibration.

## TECHNICAL APPROACH

A time-domain MAC (TD-MAC) core for TD neural networks (TD-NN) uses medium-precision quantized NNs (QNNs). They use only digital cells and a single wire pair holds multiple "bits" using rail-to-rail voltages. The ever-finer time precision/resolution with CMOS scaling is exploited. QNN-based TD-NN techniques with 4-8 bit inputs/weights will be developed.

The basic block of the multi-bit TD-MAC is the digital-to-time converter (DTC). It has digital inputs (A,B) with relative delay $D_x$ and an $N_W$-bit weight $W$; it generates digital outputs (P,Q) with relative delay $D_y$ proportional to $W$. y is encoded as a Vernier pair to realize a signed DTC.

## SUMMARY OF RESULTS

The QNN TD-NN techniques will first be demonstrated in an eight-core 65-nm CMOS class-G SCPA (Figure 1). It is the first switched-capacitor power amplifier (SCPA) with eight efficiency peaks. The deepest one is at 24dB power back-off (PBO), and a 1.8X efficiency improvement is realized for *Wi-Fi 6* signals with +/- 6dB transmission power control (TPC) (Figure 2). Measurements of the first prototypes are underway including extensive linearity characterization using conventional static off-line digital pre-distortion (DPD) techniques.

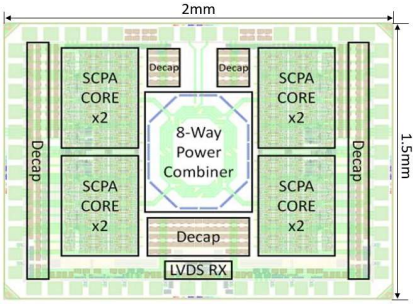


**Figure 1. Full chip layout of eight-core Class-G SCPA.**

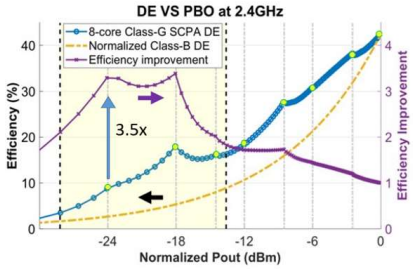


**Figure 2. Drain efficiency (post-layout simulation).**

However, its linearity (AM-PM distortion) is not good enough even with conventional static DPD to meet the EVM requirement for 1024 QAM OFDM signals (Figure 3). Time-domain measurements show that the dynamic nonlinearity is due to memory effects. Techniques are being developed to both sense and correct them.

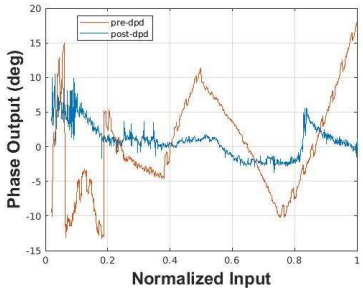


**Figure 3. Measured AM-PM distortion with and without DPD.**

In our proposed implementation, NX DTCs whose resolutions are scaled geometrically (Δ, 2Δ, 22Δ, 23Δ, …) are cascaded (Figure 4). We will develop and demonstrate this multiplying DTC concept for on-line static and dynamic linearity correction.

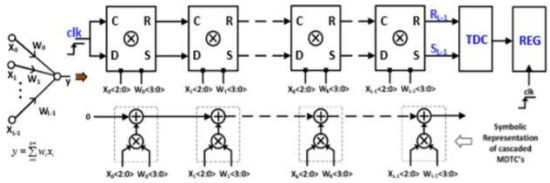


**Figure 4. Time-domain MAC that can be configured as a TD-NN.**

**Keywords:** Switched-capacitor power amplifier, digital pre-distortion, memory effects, time-domain neural networks

## INDUSTRY INTERACTIONS

Intel, NXP

## MAJOR PAPERS/PATENTS

# TASK 2810.075, HYBRID STEP-DOWN DC-DC CONVERTERS WITH LARGE CONVERSION RATIOS FOR 48V AUTOMOTIVE APPLICATIONS

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JIN LIU, THE UNIVERSITY OF TEXAS AT DALLAS

## SIGNIFICANCE AND OBJECTIVES

This research aims to develop innovative capacitor-assisted hybrid DC-DC converters to provide high power efficiency under large input-to-output voltage conversions in 48-V automotive applications. A systematic approach will also be developed to realize hybrid converters with a minimal number of low-voltage power FETs and passive components to improve the converter power density.

## TECHNICAL APPROACH

We investigate both flying-capacitor multi-level and switched-capacitor-assisted converter topologies to evaluate operation flexibility in different conditions, the requirements of voltage balancing and pre-charging of flying capacitors, the capability of providing high power density, and different power losses. We started with our recently reported converter topology: dual-path hybrid Dickson converter that can lower the required inductor current for a given output current. This not only decreases the inductor conduction loss but also improves the capability of delivering high output current for better power density.

## SUMMARY OF RESULTS

The proposed N:1 dual-path hybrid Dickson (DPHD) converter is shown in Fig. 1 below. It consists of one inductor, N+3 power switches, and N-1 flying capacitors, where N is an integer. All flying capacitors in the converter do not require to be balanced in the steady state nor be pre-charged in the start-up condition. Fig. 1 also shows that the SC network shares part of the output current, thereby reducing the required inductor current and its conduction loss. The efficiency would thus be improved.

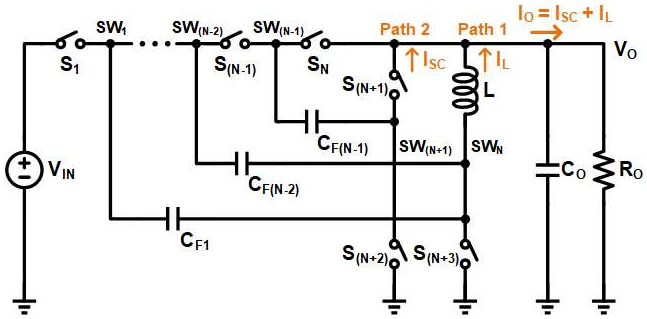


**Figure 1. The architecture of the proposed N:1 dual-path hybrid Dickson converter topology [1].**

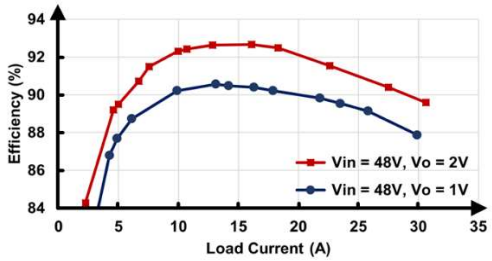


**Figure 2. Measured power efficiency of 7:1 converter.**

This converter topology was previously explored and reported for PoL applications, in which N is selected as 7 to generate the output voltage of 1-2V from the input voltage of 36-65V [1]. Ten 25-V MOSFETs were used as power switches in the DPHD converter prototype. The converter operates at 250kHz and delivers the load current $I_O$ up to 30A. Thanks to the proposed DPHD structure for sharing $I_O$, the value of inductor current is reduced by 17% compared to the conventional buck converter or other single-inductor hybrid converters. Fig. 2 presents the measured power efficiency of the DPHD converter at two output voltages of 1V and 2V under $V_{IN}$ of 48V. The peak power efficiencies of 92.7% and 90.6% are achieved with the input-to-output conversion ratios of 24 and 48, respectively. Compared to other state-of-the-art high-ratio non-isolated step-down converters, this DPHD converter supports the highest $I_O$, provides the highest power density of 451W/in$^3$, and achieves the competitive peak power efficiency.

Based on above promising results of the proposed DPHD converter, we are extending the research of this topology for automotive applications, in which the frequency is increased to the MHz range and the output voltage becomes 3-5V.

**Keywords: DC-DC converter, dual-path hybrid Dickson converter, high-conversion-ratio step-down converter, hybrid converter, non-isolated converter**

## INDUSTRY INTERACTIONS

Texas Instruments, Intel

## MAJOR PAPERS/PATENTS

[1] C. Chen et al., "A 92.7%-Efficiency 30A 48V-to-1V Dual-Path Hybrid Dickson Converter for PoL Applications," Accepted to 2021 ECCE, October 2021, Vancouver, Canada.

# TASK 2810.078, PROGRAMMABLE MIXED-SIGNAL ACCELERATOR FOR DNNS WITH DEPTHWISE SEPARABLE CONVOLUTION LAYERS

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## SIGNIFICANCE AND OBJECTIVES

Deep neural networks (DNNs) require massively parallel and energy-efficient multiply-accumulate (MAC) circuitry. In-memory computing (IMC) has shown potential but lacks efficient means for multi-bit compute. This work looks for a middle ground between IMC and standard digital processing by investigating the potential of multi-bit switched capacitor (SC) compute arrays.

## TECHNICAL APPROACH

The key ingredient of our approach is a processing element (PE) array that intersperses SC MAC circuitry with local SRAM kernel storage. The density of these circuits allows us to fully unroll and pipeline the operations of a modern DNN layer, featuring pointwise expansion, depthwise separable convolution, and a point-wise projection. This avoids storing the large expanded feature maps (~6x decrease in SRAM buffer size), eliminates accumulation buffers, as well as multiple loads of the same weights and input data. We target the implementation of MobileNetV2 to demonstrate the efficacy of this fabric.

## SUMMARY OF RESULTS

We have designed and simulated the first prototype of an M x N compute array and reported the results in [1]. Figure 1 shows a conceptual schematic. Each of the M kernels contains N-dimensional dot-product circuits with input activations d and weights w. The input activations are broadcast across the array to amortize memory access and to yield a full matrix-vector product. Each of the N MAC elements within a kernel performs a 4-bit multiplication with subsequent capacitive accumulation. The multiplications are performed similarly to a digital multiplier, which uses bitwise AND operations and a digital adder network to collect the partial products. Our mixed-signal design keeps the AND operations in the digital domain but sums the partial products through analog charge sharing on six analog wires ($V_{MAC}$).

The wire voltages are capacitively summed in the shown binary combiner block before digitization with an 8-bit SAR ADC (one per kernel). The final dot product result for each kernel is formed by charge sharing between all N MAC elements using the same $V_{MAC}$ wires. Thus, the analog charge sharing eliminates all digital partial product additions that would normally occur within multipliers and the accumulator hardware.

The weights are stored in a custom 6T SRAM inside each MAC element. The memory size per element can be chosen based on the application and the dimensions of the array. In this work, we use seven 4-bit weights per MAC element. Having dense memory right next to the product cells allows us to load the weights in a single clock cycle, reducing read energy and data movement. This increased read bandwidth avoids idling the compute when loading new weights in DNN layers that have small input dimensions but a large number of weights.

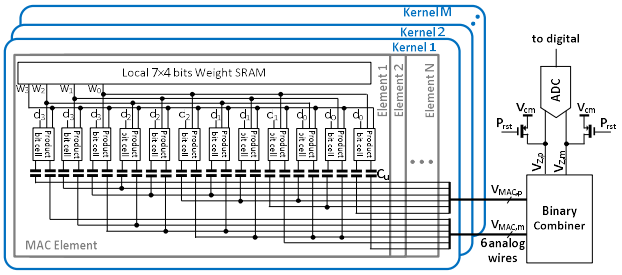



**Figure 1. Mixed-signal MAC array with binary combiner and local memory.**

Our first test chip will contain a 94 x 160 array and can perform all 4-bit MAC operations within only one clock cycle at 100 MHz. Post-layout simulations in 28-nm CMOS indicate an energy efficiency of 6.4 fJ/MAC and a compute density of 3.17 TOPS/mm$^2$. Compared to prior art, this work achieves higher energy efficiency than single-bit IMC configured for 4-bit arithmetic (~2.6x) as well as recent digital IMC realizations (~3.5x). The RMS MAC noise is <350 µV assuring <1% top-1 accuracy degradation for popular DNNs deployed on the ImageNet dataset.

**Keywords:** Deep neural networks, hardware accelerators, in-memory computing, mixed-signal integrated circuits, switched capacitor circuits

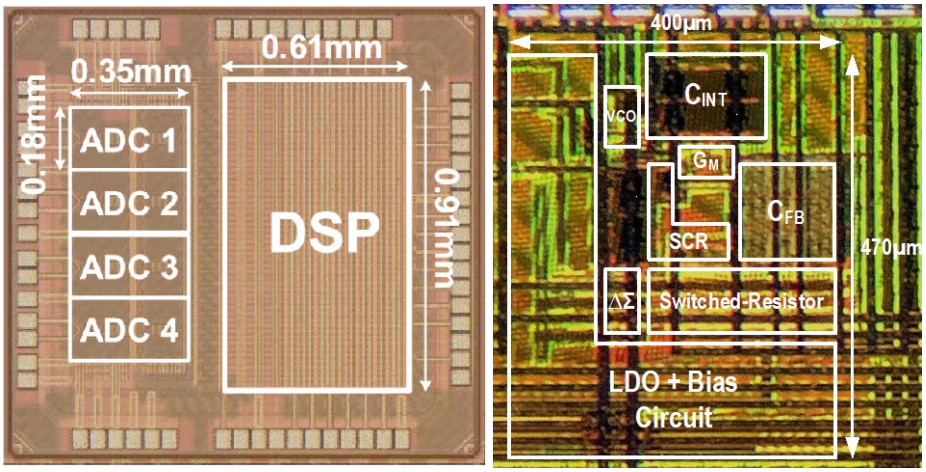
## INDUSTRY INTERACTIONS

Texas Instruments, IBM, NXP

## MAJOR PAPERS/PATENTS

[1] W.-H. Yu, M. Giordano, R. Doshi, M. Zhang, P.-I. Mak, R.P. Martins, and B. Murmann, “A 4-bit Mixed-Signal MAC Array with Swing Enhancement and Local Kernel Memory,” to appear at MWSCAS 2021.

# Fundamental Analog Thrust




| Category | Accomplishment |
|---|---|
| Fundamental Analog (Circuits) | A compact, low-power microphone-to-spectrogram beamforming frontend processor for speech recognition is demonstrated by bit-stream processing of the outputs generated by an array of sigma-delta modulators that digitize microphone outputs. The prototype beamformer fabricated in a 40-nm CMOS process occupies an active area of 0.89mm$^2$ and improves speech recognition accuracy in noisy conditions from 64% to 90%. (2810.060, M. Flynn, U. Michigan) |
| Fundamental Analog (Circuits) | The stability concerns that plague higher-order wideband continuous-time sigma-delta modulators are overcome using a Correlated Dual Loop SMASH (CDL-SMASH) architecture. The detrimental impact of scaling-induced circuit imperfections such as variations in RC time constant and finite amplifier gain are also mitigated, thus enabling robust high dynamic range wideband operation. Fabricated in a 65-nm CMOS process, the prototype CDL-SMASH-ADC achieves 73.4dB SNDR over 18.75MHz bandwidth while consuming only 18mW. (2712.014, N. Maghari, U. Florida) |
| Fundamental Analog (Circuits) | High accuracy RC oscillator-based frequency reference is demonstrated by precise and robust cancellation of the resistor temperature coefficient (TC) across the process. Using a parallel combination of switched-resistors that are digitally controlled by temperature-compensating pulse-density modulated sequences, the output frequency's first- and second-order TCs are suppressed. A prototype 100MHz frequency reference fabricated in a 65-nm CMOS process achieved an inaccuracy of 140ppm, 80ppm/V voltage sensitivity, 2.5ppm Allan deviation, and 1µW/MHz power efficiency. (2810.036, P. Hanumolu, UIUC) |

# TASK 2712.011, ROBUST RELIABLE AND PRACTICAL HIGH PERFORMANCE REFERENCES IN ADVANCED TECHNOLOGIES

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## SIGNIFICANCE AND OBJECTIVES

Objective is to develop circuits that express the bandgap voltage at the output with a single electrical trim at standard test temperature and to adapt all-electrical trim to an on-demand run-time trim without requiring external test equipment. Significance is in development of references with lower temperature dependence.

## TECHNICAL APPROACH

Our approach to the first objective is to revisit the issue of expressing the bandgap voltage at the output of a circuit directly rather than focusing on expressing the bandgap voltage only at an inflection temperature. Our approach to meet the second objective will be to identify what additional information can be obtained from the correlated reconfiguration of a circuit in which the bandgap voltage and temperature are tightly intertwined in the device characteristics and design variables. Two test chips will be designed to obtain experimental verification of the performance of the new precision reference circuits.

## SUMMARY OF RESULTS

Two new bandgap reference circuits have been developed that ideally express the bandgap voltage at the output. In contrast to existing approaches that provide curvature correction to partially correct for a nonlinear TlnT term that has been a nemesis for bandgap references for over 3 decades, these two new circuits are designed to eliminate the nonlinear TlnT term. These may be the first two circuits that express the bandgap voltage of silicon at the output. One is based upon a dc current bootstrapping approach and the second is based upon a dc voltage bootstrapping approach. A patent was obtained for the current bootstrapping approach.

The current bootstrapping circuit was fabricated in a 130-nm CMOS process. A Fluke Microbath Thermometer Calibrator was used to make measurements. Initial measured results were disappointing with the temperature dependence of the offset voltage of the operational amplifiers and the limited digital trim range limiting performance. The measured TC over an 80°C window was 14 ppm/°C. Though performance with this approach to the sub 1 ppm/°C range should be achievable, resources for refabricating and retesting were not available so the emphasis has been placed upon the voltage bootstrapping approach which should offer comparable performance.

The voltage bandgap expression circuit using a voltage bootstrap is shown in Fig. 1. The performance limitations are believed to be dominantly associated with the diode-connected substrate pnp transistors so only this part of the reference was fabricated in a 65-nm CMOS process to allow clear experimental delineation between limitations associated with the pnp devices and the remaining components that can be readily added by experienced designers with the required level of performance. The layout of the pnp transistor array is shown in Fig. 2. Experimental results with trim show 0.8 ppm/°C over 80°C range. Another bandgap expression circuit [2] has been designed. Simulations predict a TC of 0.7 ppm/°C over a 160°C range but experimental results are somewhat less impressive and appear to be flicker noise limited.

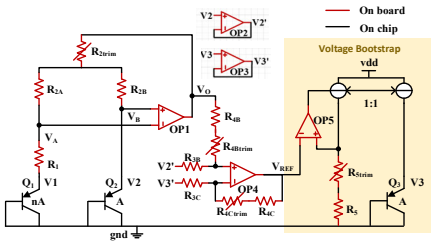


**Figure 1. Current Bootstrapped Bandgap Extractor Reference.**

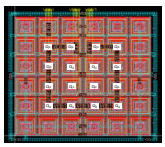

**Figure 2. Voltage Bootstrapped Bandgap Extractor Reference.**

**Keywords:** bandgap reference, diode model, curvature-compensation, voltage reference, bandgap separator

## INDUSTRY INTERACTIONS

Texas Instruments, Intel, NXP

## MAJOR PAPERS/PATENTS

[1] D. Chen and Z.Liu, US Pat. 10,359,801 "Voltage reference generator with linear and non-linear temperature dependency elimination," July 23, 2019.
[2] P. Ebenezer, V. Naganadhan, D. Chen, and R.L. Geiger, "Three-Junction Bandgap Circuit with Sub 1 ppm/°C Temperature Coefficient," IEEE Midwest Symposium on Circuits and Systems (MWSCAS), pp. 1-4, Aug. 2020.

# TASK 2712.014, LEVERAGING CMOS SCALING IN HIGH PERFORMANCE ADCS

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## SIGNIFICANCE AND OBJECTIVES

In the last year of this effort, we successfully debugged and refabricated the prototype IC of the proposed Continuous-Time (CT) Delta Sigma ADC called Correlated Dual Loop SMASH (CDL-SMASH). The measurement results validate the proposed architecture. Conference and journal publications are planned for 2021-22.

## TECHNICAL APPROACH

The goal is to leverage the properties of scaled CMOS to improve the performance of ADCs. In this effort, we have proposed three general solutions, two of which were reported in previous years including (1) digital correlated level shifting (D-CLS) pipelined ADC which alleviates the need for high opamp gain, and (2) leveraging parasitic capacitance in quantization in delta-sigma ADCs for excess loop delay (ELD) compensation. The third architecture (CDL-SMASH) allows high order noise shaping without stability constraints as well as high-speed operation.

## SUMMARY OF RESULTS

The proposed CDL SMASH not only preserves the advantages of SMASH structure and removes the need for direct quantization noise (QN) extraction but also simplifies the overall loop architecture. The CDL SMASH is essentially based on the original SMASH architecture but allows to adopt the low distortion structure similar to that of MASH with the help of an additional feedforward path while removing the feedback path in the cascaded loop as shown in Fig. 1. The overall noise transfer function (NTF) of CDL SMASH (NTFCDL) like SMASH shapes the quantization error of both Q1 and Q2.

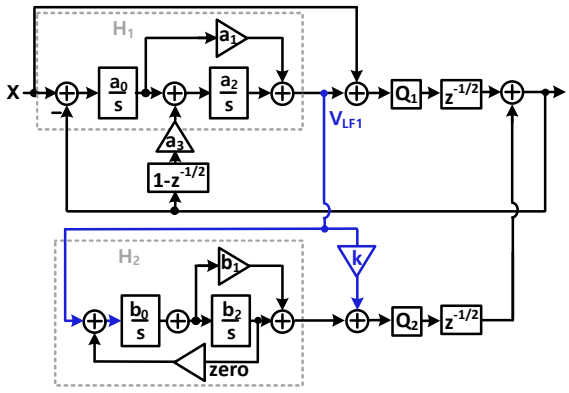


**Figure 1. Architecture level of the fabricated prototype CDL Delta-Sigma ADC.**

The key point for the CDL SMASH to operate properly is for the second loop (H2) to crudely follow the transfer function of the first loop (H1). This guaratees the stability of H2 and allows the CDL SMASH to have less sensitivity to RC mismatch, amplifier gain, and other circuit imperfections. While most of the characteristics follow the original SMASH structure, additional advantageous characteristics are found. First, further simplification of the SMASH is allowed which removes the feedback DAC from the output of Q2 to the input of H2. Second the overall timing is simplified allowing to use only complementary clock signals (CLK and CLKb for example) which enables allocation of more timing for quantizer operation and relaxation of the BW requirement of the integrators.

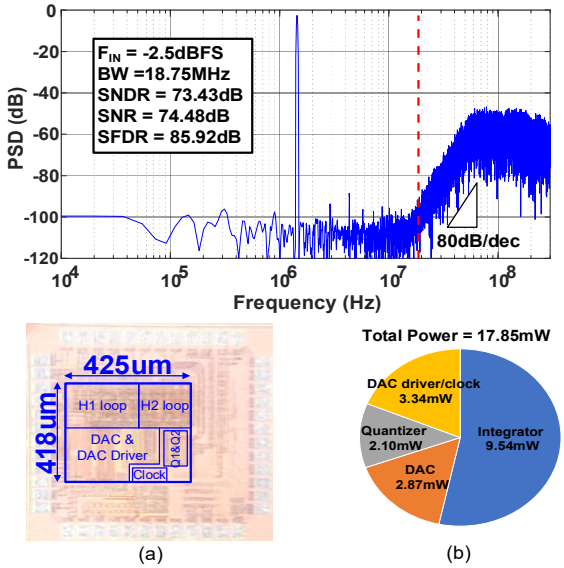


**Figure 2 (top) measured spectra (a) chip photo (b) power breakdown.**

**Table 1. Performance Summary.**

| Process | BW | SNDR | SNR | $FoM_{sndr}$ | $FoM_{DR}$ |
|---|---|---|---|---|---|
| 65nm UMC | 18.75M | 73.4 | 74.5 | 163.6 | 168.6 |

**Keywords:** Delta-Sigma, Multi-Loop, Noise Shaping, ADC

## INDUSTRY INTERACTIONS

Texas Instruments, INTEL, NXP

## MAJOR PAPERS/PATENTS

[1] B. Park. "Correlated Dual-Loop Delta-Sigma ADC," A-SSCC 2021.

# TASK 2712.025, REDUCTION OF LOW FREQUENCY NOISE IMPACT IN NANO-SCALE CMOS CIRCUITS

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## SIGNIFICANCE AND OBJECTIVES

This project is investigating approaches to incorporate an on-chip measurement capability and post-fabrication configurable minimum size transistor arrays to reduce the low frequency noise impact in RF and analog circuits. This approach may be more effective for reducing low frequency noise impact than increasing the transistor size.

## TECHNICAL APPROACH

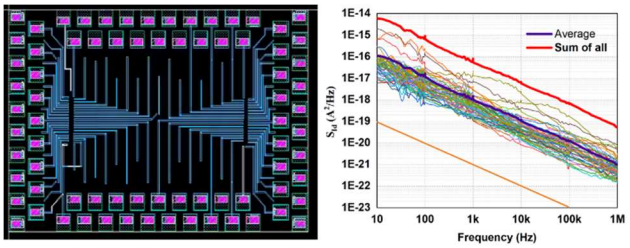
Using transistors with lower noise through post fabrication selection, and approaches for integrating a highly sensitive noise measurement circuit based on a frequency synthesizer commonly found in RF and millimeter wave transmitter and receiver will be investigated. Intelligent search algorithms will be applied to select the combinations with low frequency noise with the minimum number of measurements. Approaches to increase the operating frequency of VCO and the factors that limit the maximum operating frequency are being investigated. Lastly, the feasibility to extend this technique to other circuits is being investigated.

## SUMMARY OF RESULTS

The number of intended dopants and un-intended defects in a minimum sized device is reduced with technology scaling. One missing dopant or having an additional defect can dramatically increase or decrease the threshold voltage, current, and noise. A 4.3-GHz voltage controlled oscillator (VCO) that embraces the variability of nano-scale transistors to reduce its phase noise by taking advantage of reduced low frequency noise of some minimum sized transistors with fewer defects or traps through post-fabrication selection is reported [1].

The VCO fabricated in 65-nm CMOS uses a digitally addressable array of cross-coupled minimum-size NMOS transistor pairs for post-fabrication selection. An algorithm based on Hamming distance using the measurements of ~1,500 combinations was used to identify the combinations with low phase noise.

To make this technique practical, an affordable and sufficiently rapid on-chip measurement technique for the phase noise that can resolve noise below -130dBc/Hz for a 4.3-GHz carrier is being researched. An updated version of the PLL in 65-nm CMOS that has reduced phase noise and requires an ADC with a reduced dynamic range has been fabricated and is characterized. In addition, a 6.0-GHz down-converter in 65-nm CMOS, as well as a 12-GHz voltage controlled oscillator in the GF 22-nm FDSOI CMOS, have been fabricated and ultilized to demonstrate the applicability of this concept. Fig. 1(a) shows a layout of array containing 32 NMOS and 32 PMOS transistors (W=80 nm/L=20 nm) fabricated in the GF 22-nm FDSOI process. Fig. 1(b) shows the measured low frequency noise of NMOS transistors at $V_{GS}$=0.5 V and $V_{DS}$=0.5 V. The backgate bias voltage was 0 V.




(a) (b)

**Figure 1. (a) Layout of array of 32 NMOS and 32 PMOS transistors (W=80 nm/L=20 nm) fabricated in the GF 22-nm FDSOI process, and (b) measured low frequency noise of the NMOS transistors at $V_{GS}$=0.5 V and $V_{DS}$=0.5 V.**

The measured low frequency noise vary by ~2 orders of magnitude. The average noise is more than 10X higher than that for the transistor with the minimum noise. This variation is smaller than that is observed in 65-nm CMOS. However, these measurements show that there exist transistors with significantly reduced noise which can be selected post-fabrication to improve noise performance of circuits. Like that was observed in the measurements from the NMOS transistor array in 65-nm CMOS, there is a relatively smaller number of transistors with significantly higher noise that skew the average noise.

**Keywords:** low frequency noise, on-chip noise measurements, post-fabrication selection

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] A. Jha et al., "-197dBc/Hz FOM 4.3-GHz VCO Using an Addressable Array of Minimum-Sized NMOS Cross-Coupled Transistor Pairs in 65-nm CMOS," *IEEE Symposium on VLSI Circuits*, pp. 214-215, June 2016, Honolulu, Hi.

# TASK 2712.031, ADAPTIVE TRIMMING AND TESTING OF ANALOG/RF INTEGRATED CIRCUITS

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## SIGNIFICANCE AND OBJECTIVES

As part of the post-fabrication process, the optimum operating voltages ($V_{min}$) is searched to reduce the power consumption of each device. The device under study has four $V_{min}$ values. The goal is to adaptively identify the $V_{min}$ by speeding up the search without impact on yield.

## TECHNICAL APPROACH

We proposed two adaptive solutions, one at the wafer level to predict a single $V_{min}$ by taking advantage of the unique process signature per wafer expressed by the e-test vector. The second solution was to identify the $V_{min}$ associated with one speed by taking advantage of the correlation between the different $V_{min}$ values associated with different speeds of the device. We experimented with the prediction of search seed for linear speed at the wafer and die-level. Depending on the solution, features included for the adaptive solution were e-tests, multiprobe measurements, and a specific speed's $V_{min}$ value to predict the target $V_{min}$.

## SUMMARY OF RESULTS

An industrial dataset of more than 800 wafers with more than 500 devices was provided by a member company. For the first solution, the experiments seek to identify the cost savings and power consumption overhead for the linear search. Fig. 1 shows the percentage of cost savings achieved for each of the selected power consumption percentage bounds when a linear search is performed.

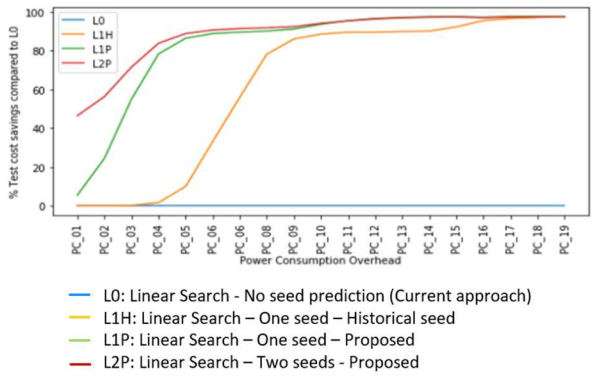


**Figure 1. Linear $V_{min}$ Search Savings.**

The L1H curve shows that the use of the historical $V_{start}$ value can achieve up to ~90% cost savings compared to the current static methodology (L0). Unfortunately, these savings start at the expense of 3-4% power consumption overhead and slowly ramp-up to 80% when there is more than 8% overhead. In comparison, our proposed method, that adapts both the $V_{start}$ and $V_{high}$, achieves ~50% savings at 1% overhead.

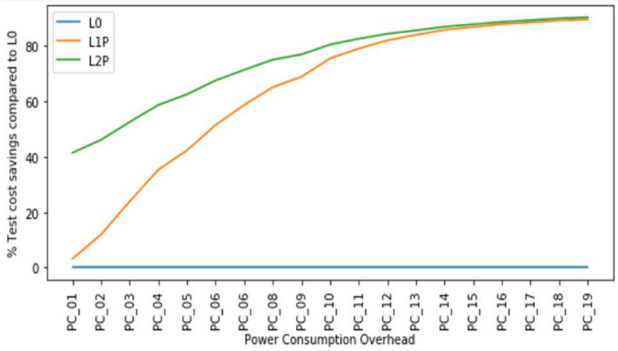


**Figure 2. Wafer-level $V_{min}$ Search Savings Compared to Current Approach L0.**

For the second adaptive solution, our focus was again on the adjustment of the starting search seed (L1P) as well as both the adjustment of the starting seed and highest possible search limit (L2P). From Figure 2, we can observe that at a power consumption overhead of 7%, an overall test cost savings of 60% is achieved.

We presented two adaptive, machine learning-based approaches to reduce the $V_{min}$ calibration costs, based on the e-test signature of a wafer and the correlation between different $V_{min}$ values. This is achieved by adjusting the $V_{min}$ search parameters to reduce the number of search steps without affecting the production yield. From the results, we were able to observe that there is still room for improvement in achieving cost savings.

**Keywords:** adaptive test, post-silicon calibration, machine learning, trimming

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] D. Neethirajan, C. Xanthopoulos, S. Boddikurapati, A. Nahar and Y. Makris, "Wafer-Level & Die-Level Adaptive Vmin Calibration Seed Forecasting using Inter-Vmin Correlation," (T-CAD Journal In preparation)

# TASK 2810.005, CIRCUIT DESIGN FOR ESD AND SUPPLY NOISE MITIGATION

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## SIGNIFICANCE AND OBJECTIVES

This project sought to develop (1) IC-level power distribution networks that promote power integrity even in the presence of power-on ESD, and (2) understand and mitigate latch-up that occurs in response to power-on ESD.

## TECHNICAL APPROACH

This work identifies ESD-induced reliability hazards, including latch-up, and evaluates solutions. There is a special emphasis on power-on ESD, e.g. from system-level discharges. Laboratory characterization of custom-designed test chips is the primary method used to investigate reliability hazards and evaluate proposed solutions. Power-on ESD induces supply noise and an effort is made to accurately measure the on-chip noise; board-level measurements are unsuitable because the package inductance decouples the noise signals at the board and chip levels. Therefore, the researchers develop and deploy on-chip noise sensors. Measurement results are interpreted with the aid of circuit and electromagnetic simulations.

## SUMMARY OF RESULTS

Power-on ESD, e.g. system-level ESD, induces noise on the chip ground bus, and ground noise may be converted to supply noise. This work found a strong positive correlation between the amplitude of the ESD-induced noise on the core power supply and the occurrence of bit flips in registers or memory cells. That study was carried out in the context of a semi-custom OpenMSP430 microcontroller test chip [1]. The on-chip supply noise was measured using supply noise monitor circuits.

This work established that internally regulated supplies reject the ESD-induced ground noise provided that there are no package pins connected to the regulated supply bus [2]. In the absence of an integrated voltage regulator, partial mitigation of the supply noise may be obtained by using separate ground busses for the IO circuits and the core logic. Those grounds cannot be completely isolated from one another due to component-level ESD requirements.

A previously unrecognized cause of transient latch-up (TLU) was identified for chip designs that have reverse body bias capability [3]. TLU is triggered by current injection at an IO pin, most notably from power-on ESD. The ampere-scale ESD current produces potential gradients across the ground net. Those gradients may cause the parasitic NPN devices associated with NMOS transistors in the circuit to turn on. Specifically, the NPN gets biased in the forward active region because the NMOS body voltage, which is driven by the regulator or charge pump circuit, is at a higher potential than the source, which is connected to the local VSS bus. The ground references for the transistor and for the regulator can differ by 1 V or more during ESD. The NPN base current provides the trigger for latch-up.

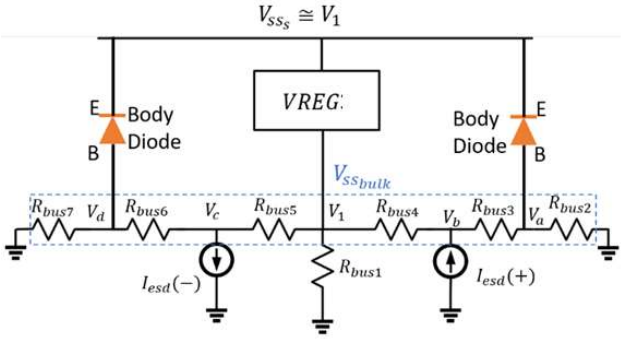


**Figure 1. Resistive model of an on-chip ground net, for a chip with reverse body bias capability. The figure illustrates how a positive bias on the base-emitter junction of the parasitic NPN may develop during ESD current injection. The resultant P-well current triggers on PNPN devices in the layout, resulting in latch-up.**

**Keywords:** ESD, power integrity, latch-up

## INDUSTRY INTERACTIONS

NXP, Texas Instruments, Intel

## MAJOR PAPERS/PATENTS

[1] S. Vora and E. Rosenbaum, "Analysis of system-level ESD-induced soft failures in a CMOS microcontroller," *IEEE Trans. EMC*, 62 (6), 2020.

[2] Y. Xiu and E. Rosenbaum, "Analysis and design of integrated voltage regulators for supply noise rejection during system-level ESD," IEEE Trans. CAS I, 67 (12), 2020.

[3] S. Vora et al., "Increased latch-up susceptibility of ICs using reverse body bias," *EOS/ESD Symp.*, 2020.

# TASK 2810.007, FULLY INTEGRATED PHASE NOISE CANCELLATION TECHNIQUES

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## SIGNIFICANCE AND OBJECTIVES

The overarching goal of our research has been the pursuit of low phase noise frequency synthesis using novel approaches, including phase noise cancellation and investigation of new PLL architectures.

## TECHNICAL APPROACH

While the project started with strategies to measure and cancel phase noise, the past two years have focused on new approaches to realize phase locked loops. A new architecture, based on a periodic excitation of an LC oscillator, has many similarities with injection locking, but has superior phase noise characteristics and no requirements on locking, making the design more robust over process corners and supply variations. On the other hand, envelope decay and non-linear tuning capacitors create frequency spurs that must be corrected. We proposed and demonstrated a mixed-signal approach to resolve these shortcomings. In the final year of the project, we also investigated sub-sampling PLL (SSPLL) architectures to realize low-phase noise mm-wave sources.

## SUMMARY OF RESULTS

Here we will focus on the last year of the project, which involved a new research thrust on SSPLL architectures. The motivation for using a divider-less architecture is that impact of divider and charge pump noise is reduced significantly, especially in PLL's that use a very large divide ratio. This is especially problematic at mm-wave PLL's that utilize XTAL oscillators at ~10 MHz and synthesize a VCO at frequencies > 10 GHz (M >1000).

The main issue in building a SSPLL is that it can lock to any integer of the XTAL within the tuning range of the VCO. To overcome this lock ambiguity, a frequency locked-loop (FLL) is often employed in parallel. In a traditional FLL, the transfer frequency of the FLL and PLL differ considerably in magnitude due to the presence of the frequency divider in the FLL, and designing a transfer function that is stable for both loops involves trade-offs, especially when the frequency division ratio is large. Typically, to meet the phase margin requirements, the power consumption of the combined FLL/sub-sampling PLL is very large. To break this trade-off, we have demonstrated a new architecture, shown in Fig. 1, wherein the charge pump and loop filter is modified to allow current injection into a new node, modifying the transfer function of the SSPLL compared to the FLL, and allowing a more favorable trade-off in the design.

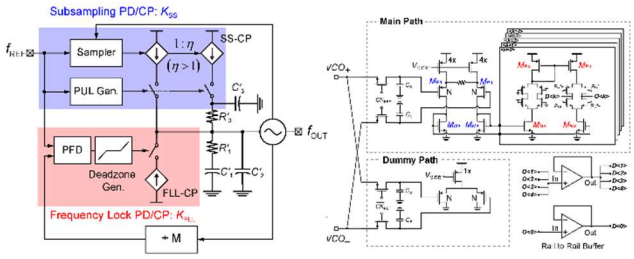


**Figure 1. The architecture for the proposed combined sub-sampling PLL/FLL and the circuit implementation of the split charge pump.**

A circuit implementation of the split charge pump is also shown in Fig. 1 (right). The efficacy of the proposed SS-CP/LF topology has been validated using a low power prototype M=480 SSPLL and a 14-GHz VCO. The prototype was fabricated in 28-nm CMOS as part of a larger system (sponsored by NSF), and the performance of the standalone PLL is shown in Fig. 2. The measured phase noise has an RMS integrated jitter of less than 155 fs (integrated from 1kHz-100 MHz). Spurs are measured below -62dBc and the overall -250dB figure-of-merit ($FOM_{JIT}$) for the PLL makes it the most competitive designs in literature when taking the large frequency division ratio into account.

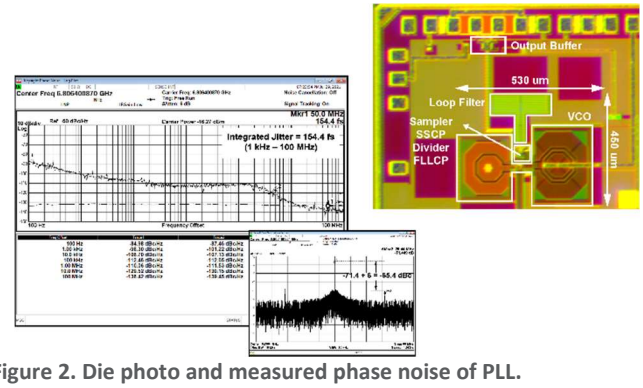


**Figure 2. Die photo and measured phase noise of PLL.**

**Keywords:** Sub-sampling PLL, low-phase noise, low jitter

## INDUSTRY INTERACTIONS

Texas Instruments, Intel

## MAJOR PAPERS/PATENTS

# TASK 2810.009, MIXED-SIGNAL BUILDING BLOCKS FOR ULTRA-LOW POWER WIRELESS SENSOR NODES

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## SIGNIFICANCE AND OBJECTIVES

This project develops novel and state-of-art performing ultra-low power mixed-signal circuits, suitable for IoT systems. This includes timekeeping circuits, amplifiers, CMOS-based sensors, and high voltage generation.

## TECHNICAL APPROACH

The most challenging ultra-low power circuit components are mixed-signal circuits such as timers, clock sources, sensing and interface circuits (e.g., temperature sensors and low-noise amplifiers). Some of these cannot be duty cycled (e.g., timers), while others require both low noise and low power (e.g., amplifiers), which are traditionally mutually exclusive. This work proposes new ULP designs for 1) crystal oscillator-based real-time clocks (RTCs), 2) temperature-compensated wakeup timers, 3) temperature sensors, 4) front-end low-noise amplifiers, and 5) on-chip high voltage generation.

## SUMMARY OF RESULTS

Capacitive MEMS sensors are fast becoming ubiquitous in many applications such as accelerometers and microphones, for their compact size, low temperature drift, and zero static current consumption. The capacitive MEMS sensors usually need dc-bias voltages to produce the sensing signal, and it is desired to use large bias voltages for better sensitivity. Voltage fluctuations on these bias voltages should be minimized to maintain a good signal-to-noise ratio. However, it remains difficult to design low power, fully integrated bias voltage generators that achieve both high voltage output (>20V) and low voltage fluctuations (<50mV). The challenge is exacerbated when considering that the generated voltages must be well-controlled to avoid interferences with the MEMS operation (e.g., electrostatic pull-in), which significantly increases the complexity and power consumption of the voltage generation circuit.

In this work, we propose a nW high voltage generator for ultra-low-power MEMS sensors. As shown in Fig. 1, the high voltage Dickson charge pumps (CPs) take 2V-4V power supply as input, and output 0 to ±30V programmable voltages through a positive ($V_{outp}$) and a negative ($V_{outn}$) electrode. The high voltage generator has a closed-loop scheme with its voltage output electrodes ($V_{outp}$, $V_{outn}$) separated from the voltage sampling electrodes ($V_{outp-pc}$, $V_{outn-pc}$) to reduce sampling ripples.

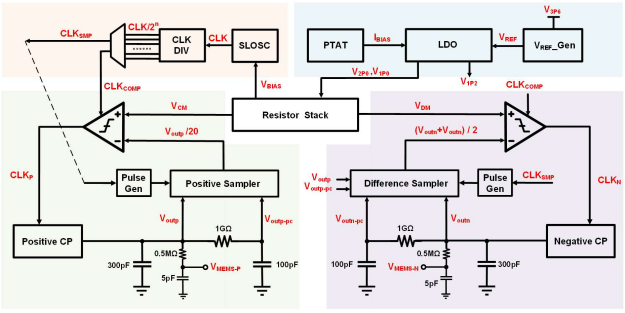


**Figure 1. Top-level diagram of the proposed ultra-low-power high voltage generator for MEMS sensing.**

To minimize the complexity and power overhead related to high voltage sampling (especially the negative voltage sampling), we present a novel structure that samples $V_{outp}$ and $V_{outp}$ + $V_{outn}$ and divides them down to compare with the desired "common-mode voltage $V_{CM}$" and the "voltage difference $V_{DM}$" between positive and negative output voltage. The comparator results the timing signals for the CPs that is usually highly duty-cycled with pure capacitive loads, greatly reducing the switching loss by the CPs. Other peripheral circuits, such as clock generation and reference voltage generation, are also implemented on chip. Altogether, the design achieves 40mV voltage variance at full-scale output while consuming 35.1nW active power.

**Table 1. Performance summary of test chip.**

| | | This work |
|---|---|---|
| Technology | | 0.18-µm HVBCD |
| Supply voltage [V] | | 2-4 |
| Maximum DC output | Positive [V] | 30 |
| | Negative [V] | -30 |
| Total Power [nW] | | 35.1 |
| Max Voltage Variant [mV] | | 40 |

**Keywords:** nano-watt, high voltage generation, MEMS sensor

## INDUSTRY INTERACTIONS

NXP

## MAJOR PAPERS/PATENTS

# TASK 2810.013, FREQUENCY-DOMAIN ADC-BASED SERIAL LINK RECEIVER ARCHITECTURES FOR 100+GB/S SERIAL LINKS

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SEBASTIAN HOYOS, TEXAS A&M UNIVERSITY

## SIGNIFICANCE AND OBJECTIVES

Clock jitter places fundamental performance limitations on common time-interleaved ADC architectures, necessitating clock generation and distribution circuitry that achieve rms jitter of a few hundred femtoseconds. The ADC-based high-speed serial link design techniques in this project aim to significantly improve jitter robustness and reduce ADC resolution and digital equalization complexity.

## TECHNICAL APPROACH

A new configurable frequency-domain ADC-based receiver serial link architecture is in development that can provide jitter robustness for baseband and coherent multi-tone modulation applications. The receiver utilizes ADCs with novel techniques to improve the configurable SAR sub-ADC speed and efficiency, including a design that utilizes reference pre-emphasis to enhance DAC settling and low-overhead reconfiguration logic to enable per-channel operation with a scalable resolution. Efficient digital reconstruction, equalization, and inter-channel interference filters for symbol detection are also in development.

## SUMMARY OF RESULTS

Figure 1 shows the proposed frequency-domain ADC-based receiver [1]. The input per-band CTLEs drive the front-end channels that have a mixer for down-conversion, resettable integrators, and an ADC for sampling and digitization. These digitized samples are then processed by the FIR filters in the DSP and their outputs are combined to either perform symbol estimation in PAM-4 baseband mode or to perform both inter-channel interference (ICI) and ISI cancellation in multi-tone mode. This architecture provides several benefits. First, the mixers perform self-equalization and provide some channel loss compensation, allowing for a reduction in digital equalization complexity. Second, high-frequency noise introduced by the mixers and CTLE is attenuated by the integrators. Finally, the inclusion of digital receive-side ICI cancellation filters in the proposed 128Gb/s system allows for a 50% improvement in relative channel spacing when compared against a previous 10Gb/s mixed-signal implementation.

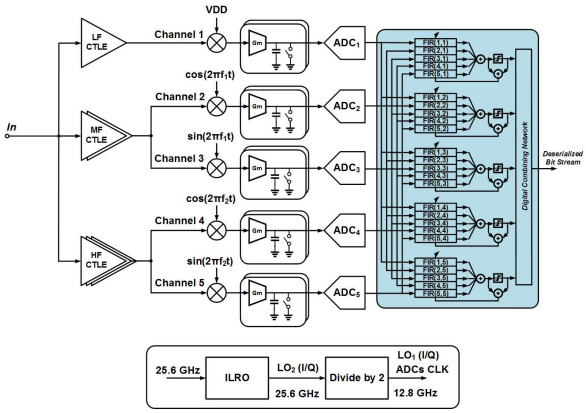


**Figure 1. Configurable frequency-domain ADC-based receiver.**

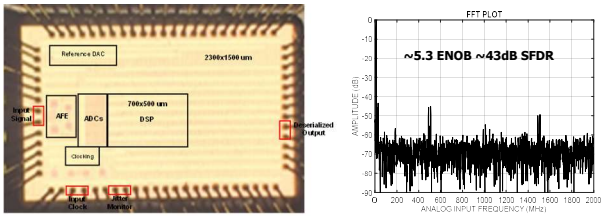


**Figure 2. 64Gb/s receiver prototype: (left) die photo and (right) initial low-frequency ADC characterization.**

Figure 2 shows an initial receiver prototype IC that was designed to operate at 64Gb/s. The analog front end (AFE) is placed close to the left-most input pads. The AFE includes the input CTLE bank, 5 mixers for the different bands, and 10 integrators, followed by the time-interleaved ADC bank which contains 20 channels in total. All the unit-ADCs are clustered to minimize routing from the integrator to the ADC sampler. This is followed by the DSP. Initial low-frequency characterization of the AFE and ADC, which is a 7b pipeline SAR architecture [2], shows that over 5b ENOB is achieved. The final 128Gb/s version with a higher bandwidth AFE and higher time-interleaved factor ADC is currently being fabricated.

**Keywords:** Analog-to-digital converter, frequency-interleaving, jitter, receiver, serial link

## INDUSTRY INTERACTIONS

Intel, Texas Instruments

## MAJOR PAPERS/PATENTS

[1] J. C. Gomez Diaz, et al., 2019 MWSCAS, August 2019, Dallas, TX.
[2] Y. Zhu, et al., 2020 CICC, March 2020, Virtual.

# TASK 2810.015, DEMONSTRATION OF 120-GBPS DIELECTRIC WAVEGUIDE COMMUNICATION USING FREQUENCY DIVISION MULTIPLEXING AND POLARIZATION DIVISION MULTIPLEXING

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## SIGNIFICANCE AND OBJECTIVES

This project in collaboration with the efforts on transitions and multiplexer/demultiplexer, and on low loss dielectric waveguides for operation at 100-400 GHz seeks to demonstrate 120-Gbps Polarization Division Multiplexing and Frequency Division Multiplexing (45-GHz bands around 180 and 315 GHz) communication over a 1-m long dielectric waveguide using CMOS circuits.

## TECHNICAL APPROACH

To excite waves at two different frequency bands with two different polarizations in a dielectric waveguide, transmitters for the 180 and 315-GHz bands will be used to drive a cross dipole. The receivers of two bands will be connected to one of the cross dipoles, while the second dipole will be terminated to reduce reflection. These receivers and transmitters will be used to demonstrate FDM operation. For PDM operation, the receiver will be rotated 90 degrees to pick up signals with the second polarization.

## SUMMARY OF RESULTS

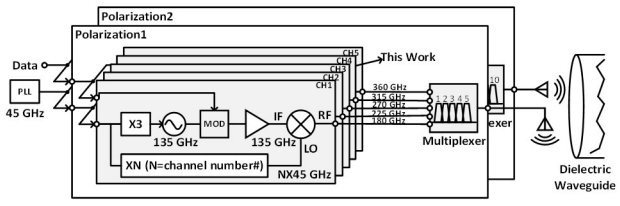


**Figure 1. Block diagram of transmitter supporting operation at 5 45-GHz frequency bands and two perpendicular polarizations.**

The dielectric waveguide communication system will eventually use five 45-GHz frequency bands spanning 157.5 to 382.5 GHz and two polarizations to implement a total of 10 30-Gbps channels for an aggregated data rate of 300 Gbps. The transmitter and receiver for the system are shown in Figs. 1 and 2. This project seeks to demonstrate 120-Gbps PDM and FDM electronic communication over a 1-m long dielectric waveguide using circuits fabricated in 65-nm CMOS. The 45-GHz bands around 180 and 315 GHz will be utilized for FDM. The transmitters and receivers connected through a diplexer or a combiner to a cross-dipole for the demonstration are shown in Fig. 3.

The 10-Gbps transmitters and receivers for the 180-GHz and 315-GHz bands have been experimentally demonstrated [1],[2]. These blocks have been integrated into dual-band transmitters and receivers including a diplexer and a feed. This dual-band transmitter and receiver circuits are assembled on a printed circuit board and connected using a ~2-mm long bond wire waveguide. The printed circuit board is being tested.

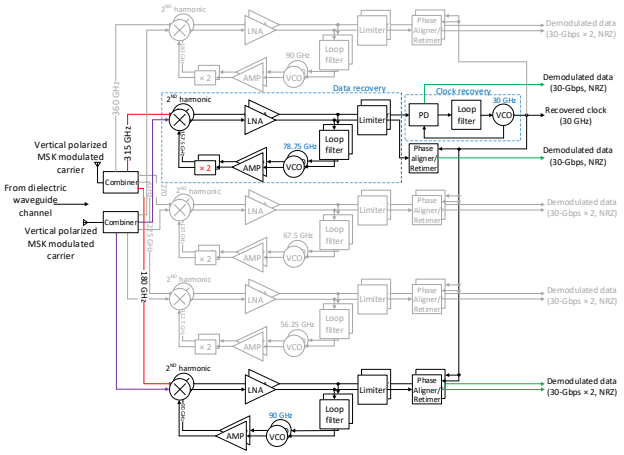


**Figure 2. Block diagram of receiver supporting operation at 5 45-GHz frequency bands and two perpendicular polarizations.**

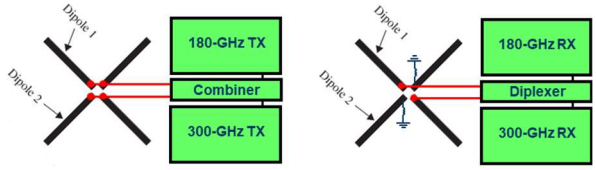


**Figure 3. TX and RX chains for PDM and FDM operation with cross-dipoles.**

**Keywords:** dielectric, waveguide, communication, millimeter waves

## INDUSTRY INTERACTIONS

Texas Instruments, Intel

## MAJOR PAPERS/PATENTS

[1] I. Momson, et al., "315-GHz Self-Synchronizing Minimum Shift Keying Receiver in 65-nm CMOS," *IEEE Symposium on VLSI Circuits*, June 2020.

[2] S. Dong, et al., "10-Gbps 180-GHz Phase-Locked-Loop Minimum Shift Keying Receiver," IEEE J. of Solid-State Circuits, vol. 56, no. 3, pp. 681-693, March 2021.

# TASK 2810.018, TRANSITION DESIGN FOR HIGH DATA RATE LINKS AT SUBMILLIMETER WAVE FREQUENCIES

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## SIGNIFICANCE AND OBJECTIVES

This research investigates techniques to connect millimeter wave transmit and receive integrated circuits (ICs) to a broadband dielectric waveguide using an on-chip dual-band cross-dipole antenna with a printed circuit board (PCB)-based quadruple ridge waveguide as the transition structure. The antennas and waveguide transition support two polarization states and operate at 180 and 315 GHz.

## TECHNICAL APPROACH

The approach involves using EM and circuit simulation tools to design the dual-band cross-dipole antenna that serves as the excitation for the RF signals coming from the integrated circuits. The transmit and receive ICs are separated by ideally a 1-meter-long broadband dielectric waveguide fabricated using Topas cyclic olefin copolymer (COC). To transition from an IC to a dielectric waveguide, a printed circuit board based metallic waveguide is designed that guides the energy. The waveguide is square includes a quadruple ridge to extend the bandwidth between 157.5 and 337.5 GHz. Upon completion of designing the individual elements, we performed an impedance and electromagnetic field matching optimization to improve the efficiency of the transitions.

## SUMMARY OF RESULTS

Figure 1 shows how the dual band crossed dipole antenna design evolves. Initially, individual dipoles operating at 180 GHz and 315 GHz are simulated separately in HFSS with two lumped port feeds. After optimizing the length, a single port is used to place the two designs in parallel. Another series of simulations are completed as the 180 GHz design is folded to reduce the overall antenna footprint. To excite two polarizations (horizontal and vertical), a second pair of parallel antennas is included that is rotated 90 degrees from the initial pair. As shown in Figure 1 (left), the antennas are 45 degrees from the center and appear as an "X".

The dual band antenna has been included in 5 separate tapeouts (generations) and has evolved in terms of the width and length of the dipole arms, the folding extension, the amount of ground metal keeps out area, and the length of the line feeding the antennas. After the 2nd generation design, the antenna S-parameters were used as a circuit block in Microwave Office and along with a circuit model representing the differential feed. This allowed for optimization of the feed outside of EM simulation to arrive at a solution more quickly. A planar balun is used to transition the single-ended input signal to differential. Also shown in Figure 1 is the most recent antenna design which includes a compensation inductive line to reduce the impact of parasitic capacitance due to the signal pad.

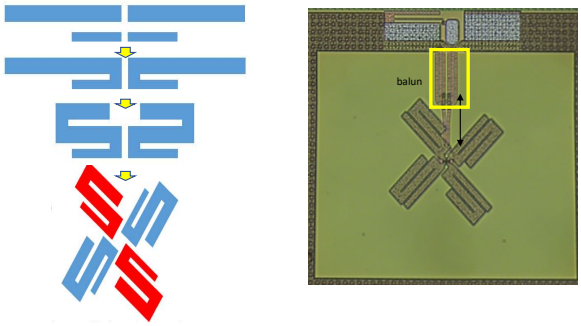


**Figure 1. Evolution of dual-band crossed dipole antenna. Two independent dipole antennas are connected in parallel. The lower frequency design is folded to reduce size. A second set of antennas is included and rotated 90 degrees from the initial set to provide vertical and horizontal polarization. Fabricated design with on-chip balun and inductance to reduce parasitic pad capacitance.**

Although the project concluded in June 2020, we are still working on the overall link demonstration. The two chips have been fabricated for transmit and receive. The antenna and the dielectric waveguides are currently under test.

**Keywords:** dual band dipole excitation, dielectric waveguide, transition, quadruple ridge waveguide

## INDUSTRY INTERACTIONS

Texas Instruments, IBM, NXP

## MAJOR PAPERS/PATENTS

[1] M. Mishra, et al., "Waveguide excitation using on-chip antenna for wireline data links," *2019 IEEE International COMCAS, Nov 2019, Tel Aviv Israel.*

[2] N. Aflakian, et al., "Low Loss Square Grid Dielectric Waveguide," *IEEE Texas Symposium on Wireless & Microwave Circuits and Systems*, May 2020, virtual presentation.

[3] N. M. Vijayakumar, R. Franklin, R. Henderson, "Multilayer Printed Circuit Board Square Waveguide in Ka Band," accepted for *URSI GASS 2021*.

# TASK 2810.019, DESIGN AUTOMATION FOR COVERAGE MANAGEMENT IN ANALOG AND MIXED SIGNAL SOCS

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## SIGNIFICANCE AND OBJECTIVES

The objective of this task is to design and implement CAD support for coverage management of AMS artifacts in mixed signal SoCs. Specific objectives include defining metrics for analog coverage, instrumenting analog coverage collection on standard simulation environments, and reasoning over coverage from IP level to SoC level.

## TECHNICAL APPROACH

We extend the syntax of coverpoints and covergroups from SystemVerilog coverage constructs such as range, levels, glitches. The CoveRT tool developed in this work automates coverage collection by embedding monitors synthesized from the coverage specification. The coverage is maintained in a database shared across the design hierarchy. CoveRT provides a query-based reasoning framework for specifying coverage targets, analyzing coverage gaps, and identifying coverage anomalies. We are currently looking at ML based approaches for reaching coverage corners, and information theoretic metrics for automatic separation of transients and glitches.

## SUMMARY OF RESULTS

The CoveRT tool is ready and under deployment at Texas Instruments. Multiple verification teams at TI have evaluated CoveRT on their existing designs as well as ones being designed. Results from some of the industrial designs are shown in Table 1. The table places a comparison between the traditional way of manually reviewing the waveforms with the CoveRT way of coverage management. CoveRT has proved to be quite impactful on these designs by not only bringing down the effort required but also improved the quality of verification by catching some design bugs which had escaped during the manual review process.

CoveRT also provides a coverage reasoning interface, which equips the user with the ability to construct and run queries on the coverage results database. Queries like incremental coverage, finding rarely hit bins, a comparative study between two sets of coverage results, etc., can be executed through this interface. A snapshot of the graphical interface of the same is shown in Figure 1.

To summarize, we believe that our contribution is rooted in the needs of the verification engineer as we have shown through our results how our offerings are enabling them to achieve higher quality results in a more time efficient fashion, thereby reducing time-to-market requirements.

**Table 1. Impact of CoveRT on industrial designs.**

| Circuit | Manual review | CoveRT approach | | Effort saving |
|---|---|---|---|---|
| SAR-ADC | Total 3H | Spec. creation | 1H | 33% |
| | | Runtime | 1H | |
| | | Total | 2H | |
| Class-D Audio Amp. | Total 12D | Spec. creation | 1.5D | 54% |
| | | Runtime | 4D | |
| | | Total | 5.5D | |
| RF MCU | Total 20D | Spec. creation | 4D | 75% |
| | | Runtime | 8H | |
| | | Total | ~5D | |
| Voltage Super--visor | Total 16D | Spec. creation | 1D | 69% |
| | | Runtime | 4D | |
| | | Total | 5D | |

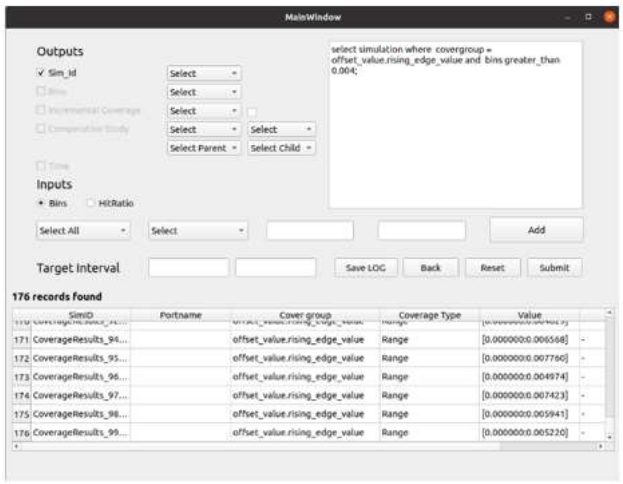


**Figure 1. The query management interface for AMS Coverage.**

**Keywords:** CAD for Analog and Mixed Signal, Coverage Management, Verification

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] S. Sanyal et al., "CoveRT: A Coverage Reporting Tool for Analog Mixed-Signal Designs," pp. 119-124, VLSID 2020.
[2] S. Sanyal et al., "The Notion of Cross Coverage in AMS Design Verification," pp. 217-222, ASP-DAC 2020.

# TASK 2810.020, ANALOG/MIXED-SIGNAL RF CIRCUIT TIME DOMAIN SENSITIVITY AND ITS APPLICATIONS

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## SIGNIFICANCE AND OBJECTIVES

Highly efficient simulation to produce a dictionary of catastrophic faults and parametric deviations for analog, mixed-signal, and radio frequency integrated circuits and systems. In contrast to the opacity of AI-ML approaches, this work is straightforward, transparent, understandable, and comprehensive.

## TECHNICAL APPROACH

Transient adjoint sensitivity is employed in a single simulation to estimate the worst-case and statistical effects of inserted catastrophic faults. Subsequently, such estimates can be tightened, and parametric drifts can be determined with very few additional such simulations.

## SUMMARY OF RESULTS

For obtaining sensitivity results, we make use of the generalized adjoint network extension of transient circuit simulation. With only one simulation, this leads to the sensitivity expression of Equation (1), where the $p_n$ represent parameters.

$$\delta_{Response_m} = \sum_{n=1}^{N} \frac{\partial f_m}{\partial p_n} . \Delta p_n \qquad (1)$$

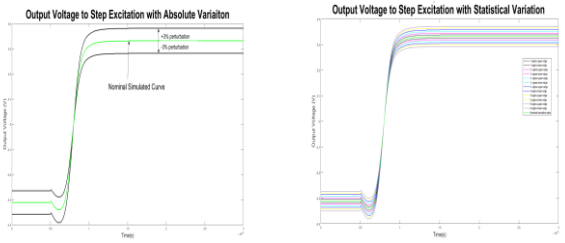


**Figure 1. Absolute and statistical manifold for a double-ended differential amplifier's output voltage response.**

The variation $\Delta p_n$ is given as tolerance in percent excursion for absolute variation and as $p_n \sim N(p_n, \sigma_n)^2$ for statistical variation. At the edges of the manifold, we calculate the possible observation of resistance faults as indicated by Equation (2). A sample for faults table for a double-ended differential amplifier of Figure 2 is shown in Table 1. Fault resistance values in Table 1 are derived from manifolds established using both absolute and statistical variations as shown in Figure 1.

$$G \text{ for a short} = \frac{\delta spec}{v_{nom} . \psi_{nom}}$$
$$R \text{ for an open} = \frac{\delta spec}{i_{nom} . \phi_{nom}} \qquad (2)$$

**Table 1. Faults generated with the resistance threshold data and the data for best strobe point locations.**

| Open Fault Location | $R_T$(Threshold) Absolute | $R_T$(Threshold) Statistical | Best Time to Observe (ns) |
|---|---|---|---|
| NM2S | 1.05e4 | 1.00e4 | 2.2241 |
| NM1D | 2.42e4 | 2.1e4 | 2.9954 |
| **Short Fault Location** | **$R_T$(Threshold) absolute** | **$R_T$(Threshold) Statistical** | **Best Time to Observe (ns)** |
| Net22 to gnd | 1.07e1 | 7.11e1 | 1.0531 |
| Net16 to Net22 | 0.44e2 | 0.65e2 | 3.3349 |

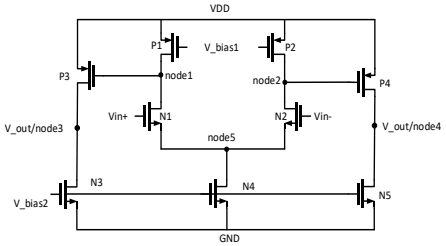


**Figure 2: Schematic for double ended differential Amplifier.**

**Keywords**: Transient Sensitivity, Adjoint Network, Fault Detection, Diagnosis

## INDUSTRY INTERACTIONS

NXP, Texas Instruments

## MAJOR PAPERS/PATENTS

[1] Zhengqi Gao and Ron Rohrer, "Efficient Non-Monte-Carlo Yield Estimation," accepted for publication in IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems.

# TASK 2810.028, ROBUST ATE MULTI-SITE HW DESIGN TO ENABLE EFFECTIVE ANALOG PERFORMANCE TESTING IN ANALOG-MIXED-SIGNAL (AMS) SOCS

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## SIGNIFICANCE AND OBJECTIVES

Mission-critical applications dictate demanding testing, significantly impacting time-to-market and manufacturing costs. Massively parallel multisite testing offers great improvements in throughput and test cost. This project will develop tools for automatically flagging excessive site-to-site (S2S) variations, identifying ATE hardware issues causing S2S variations, and enhancing multi-site ATE hardware robustness and effectiveness.

## TECHNICAL APPROACH

Existing volume probe/final-test data and ATE hardware files will be used to develop statistical signal processing and machine learning algorithms to automatically process the volume data and flag sites with issues. These results will enable the identification of sensitive components/nets in the ATE hardware. Targeted extraction/simulation will be run and additional GRR measurements will be taken to identify hardware root causes. Such learning will lead to improved test board hardware design that is robust to site-to-site variations. A framework for pre-fabrication verification, post-fabrication evaluation, and site-calibration, and adaptive test flow strategies will achieve robust and effective tests.

## SUMMARY OF RESULTS

The first year's results have been packaged and delivered to TI, the customer sponsor. The package includes three different algorithms for processing volume data and automatically identifying and flagging potential sites with issues. During the second year, we developed tools for automated extraction of analog sensitive Test Board Parameters; we applied the year-1 algorithms for site to site issue identification to a new product-test board in early ramping with a limited test volume data; we made improvements to the algorithms to make them more suitable for ramping products with light data; we used ordinal optimization and other methods to better estimate the true but unknown die distribution; we also developed the Systematic Hardware Error Identification and Calibration (SHEIC) method for massive multisite testing applications.

Figs 1 and 2 illustrate the basic idea of the SHEIC method and the corresponding coding flow chart. By applying the SHEIC method, ATE hardware systematic error-induced shifts in die parameters can be calibrated out, leading to more accurate die parameter measurement, reduced mis-trims, and better yields.

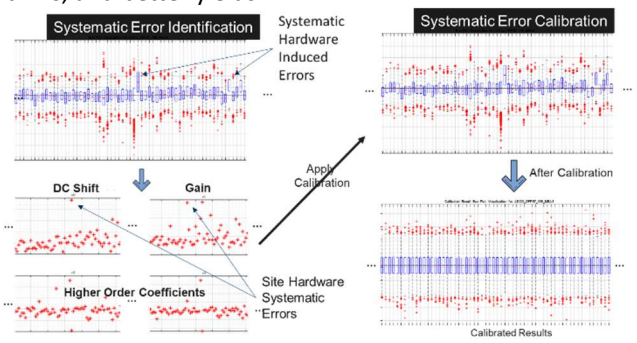


**Figure 1. SHEIC concept illustration.**

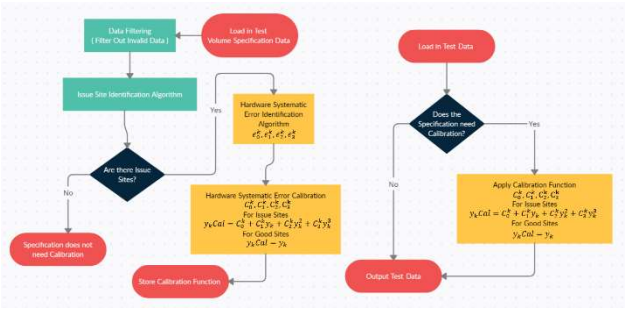


**Figure 2. SHEIC flow chart.**

**Future direction**: Improvement and validation to the Systematic Hardware Error Identification and Calibration method for improved test quality and yield; Development of a tool for automatic board parameter extraction and analysis for flagging or reducing potential S2S issues; Development of tools to help understand the root causes of site to site variations (SSV) so that future test board designs are robust to SSV.

**Keywords:** multi-site testing, test cost reduction, volume test data learning, ATE test hardware debug/design

## INDUSTRY INTERACTIONS

Texas Instruments, NXP

## MAJOR PAPERS/PATENTS

[1] P. Farayola, *et al*, "Quantile – Quantile Fitting Approach to Detect…," IEEE VTS, pp1-6, 2020.

[2] P. Farayola, *et al*, "Domain Transformation…," IEEE Trans. On Instr. and Meas., vol 70, pp1-12, 2021.

[3] I. Bruce, *et al*, "Ordinal Optimization Based Distribution Estimation For Multisite…," IEEE European Test Symposium, pp1-5, 2021.

# TASK 2810.029, 170GHZ – 260GHZ WIDEBAND PA AND LNA DESIGN IN SILICON

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## SIGNIFICANCE AND OBJECTIVES

We design a wideband power amplifier (PA) and a low-noise amplifier (LNA) operating in the 170-260 GHz band using a commercial silicon process. Both these blocks are critical components for future high-speed wireless communication links and high-resolution 3D-imaging radars.

## TECHNICAL APPROACH

A single-ended LNA was designed and taped out in a 130-nm SiGe process offered by IHP Microelectronics. An LNA was also taped out in a 22-nm FDSOI process offered by GlobalFoundries. A stagger tuned multi-stage design approach was adopted in both LNAs to obtain good noise performance and gain over a wide bandwidth. The entire layout is EM simulated and modeled to capture high-frequency effects accurately.

## SUMMARY OF RESULTS

The IHP SiGe-G2Cu process has transistors having $f_T/f_{max}$ of 300/450 GHz. It offers MIM caps having a density of 2fF/$\mu m^2$ and its copper backend enables the design of low-loss transmission line passives.

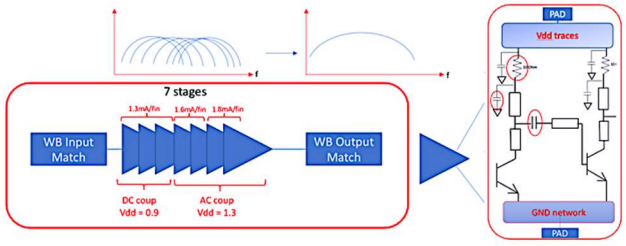


**Figure 1. The architecture of the 7-stage LNA.**

Fig. 1 shows the architecture of the 7 stage CE LNA. The stages are designed to peak at different frequencies to enhance the overall bandwidth of the LNA. The first three stages of the LNA are DC-biased to avoid the noise contribution of the low-Q MIM capacitor in the interstage matching networks at the operating frequencies. As shown, the initial stages are biased for optimum noise performance and the proceeding stages are biased for optimum gain performance.

Fig. 2 shows the measurement setup which was used to characterize the gain performance of the IHP LNA chip. A Keysight E8257D signal generator is connected to a Virginia Diodes WR5.1 frequency tripler to generate signals in the frequency band of interest. At the output side, an OML WR5 mixer is used to down convert the signal which is then captured using a Keysight 9030A PXA spectrum analyzer. The signal path is initially characterized using a 100-$\mu m$ on-chip transmission line. This is used as a reference for measuring gain. Figure 3 shows the gain vs frequency measurements. It suggests a wide-band behavior. The gain plot shows some measurement errors which can be resolved using a vector network analyzer.

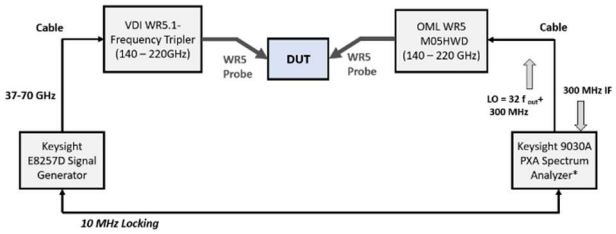


**Figure 2. Measurement setup for characterizing gain.**

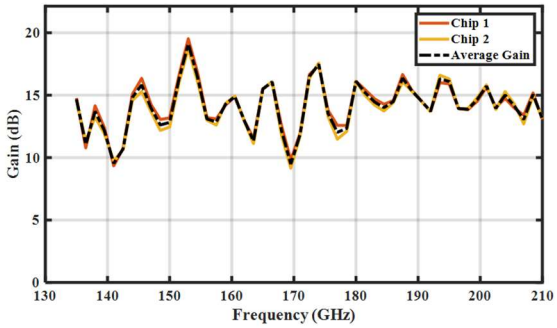


**Figure 3. Gain vs. frequency measurements of the iHP LNA chip.**

The GlobalFoundries 22-nm FDSOI process offers transistors with an $f_T/f_{max}$ of 244/347 GHz and a good $NF_{min}$ of 3.2 dB at 220 GHz. A stagger tuned approach, similar to Fig. 1 was adopted in this design to achieve broadband noise and gain performance.

In the coming months, we plan to perform noise figures and S-parameter measurements of the LNA. We also plan to characterize the small signal and large signal parameters of the PA chip and make the required modifications to the designs.

**Keywords:** LNA, PA Wideband, Silicon, SiGe BiCMOS

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

# TASK 2810.030, NEURAL NETWORK RECOGNITION & ON-CHIP ONLINE LEARNING WITH STT-MRAM

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## SIGNIFICANCE AND OBJECTIVES

Neuromorphic computing promises exceptional capabilities for artificial intelligence through highly efficient circuit structures mimicking the structure and functionality of the human brain. This project proposes the first experimental demonstration of a neural network system that leverages the stochastic switching of STT-MRAM devices to perform analog on-chip online learning and recognition.

## TECHNICAL APPROACH

We propose an STT-MRAM array with a novel analog CMOS weight-updating circuit. The stochastic switching of STT-MRAM can be used to provide the analog behavior necessary for neuromorphic computing. The circuit will perform an unsupervised learning rule based on spike-timing-dependent plasticity through which the relative timing of input and output neuron spikes determines the voltages applied to the synapses. This will be the first experimental demonstration of on-chip online learning and recognition with STT-MRAM, enabling high speed, low area, energy efficiency, and robustness. The chip will be demonstrated using an STT-MRAM array fabricated in a commercial process technology.

## SUMMARY OF RESULTS

This synchronous circuit design utilizing an unsupervised learning process has been demonstrated on the MNIST handwritten digit database via behavioral simulation and can be readily translated to a digital CMOS circuit that can be fabricated and experimentally demonstrated. The core of the on-chip unsupervised online learning system is shown in Fig. 1, with STT-MRAM synapses and leaky integrate-and-fire neurons implemented in CMOS. During each clock cycle, the input neurons generate input pulses to the MRAM array, and the output neurons integrate the current from the MRAM array. If a neuron fires, a learning pulse is generated during the next clock cycle and the neuron integration values are reset to zero; if no neuron fires, leaking occurs during the next clock cycle.

As shown in Fig. 2, the inference accuracy of the simulation increases as both the number of output neurons and the number of synapses sharing each pixel increase where it can reach a 90% accuracy to the MNIST handwritten digits. These results are comparable to simulations of unsupervised single-layer SNNs based on multilevel memristors evaluated with a similar size and methodology. However, those simulations do not account for the difficulties with attempting to precisely write and store memristor resistance states while this design does. The proposed binary STT-MRAM system with stochastic writing will be experimentally proven to provide higher accuracies than can be achieved with memristors and phase-change memory.

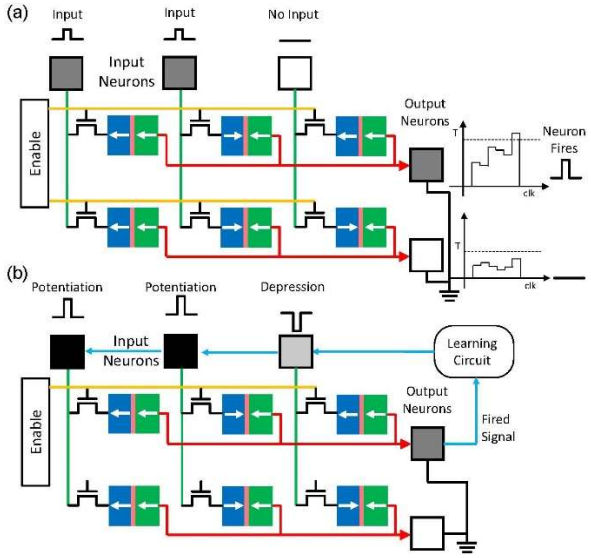


**Figure 1. STT-MRAM (a) inference and (b) learning circuits.**

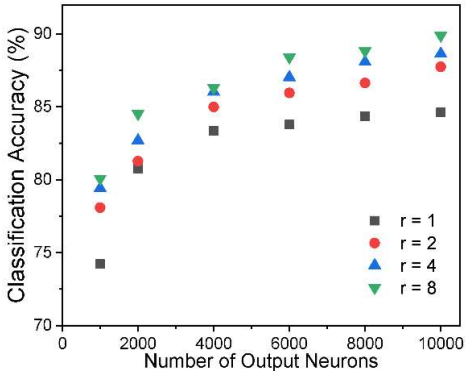


**Figure 2. MNIST accuracy as a function of output neuron count.**

**Keywords:** STT-MRAM, Neural Network, Online Learning, Unsupervised Learning, Artificial Intelligence

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] P. Zhou, J. A. Smith, L. Deremo, S. K. Heinrich-Barna, J. S. Friedman, "Synchronous Unsupervised STDP Learning with Stochastic STT-MRAM Switching," *GOMACTech* 2021.

# TASK 2810.031, DEVELOPMENT AND ASSESSMENT OF MACHINE LEARNING BASED ANALOG AND MIXED-SIGNAL VERIFICATION

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## SIGNIFICANCE AND OBJECTIVES

Due to the growing complexity and number of parametric variations in safety-critical analog and mixed-signal (AMS) circuits, rare failure detection in a high-dimensional PVT parameter space is one of the major challenges in AMS verification. We enable efficient AMS failure detection via a machine learning (ML) approach supported by dimension reduction.

## TECHNICAL APPROACH

Bayesian optimization (BO) has been demonstrated for sample-efficient rare failure prediction of AMS circuits. However, BO suffers from poor scalability with respect to the number of PVT parameters. We develop an ML-based nonlinear parameter reduction approach using a reversible residual network (RevNet) and gating architecture (ARGate) for learning important mapped features [2]. Specifically, we propose a new RevNet based auxiliary-model regulated gating architecture, called *Rev-Gate*, to utilize gating fusion weights for efficient dimension reduction (Figure 1). This allows for novel dimension embedding leveraging the RevNet and a Bayesian neural network (BNN) for mapping a low-dimensional internal representation back to the original high-dimensional parameter space and vice versa.

## SUMMARY OF RESULTS

As shown in Figure 1, during the pre-training phase, we make use of a RevNet to map the original high-dimensional parameter space (*x*) to a nonlinear mapped feature space (*r*) without any information loss. A subset of *r* parameters, i.e., *z*, are found to be critical using the ARGate network that computes the importance measure of each mapped feature. Finally, we operate BO based rare failure search in the reduced parameter space *z*, for much-improved scalability. Furthermore, for mapping a given *z* vector back to the original parameter space, we make use of a trained Bayesian neural network BNN, in a way such that additional simulation data collection can be acquired based on physically defined circuit parameters as part of the BO-based iterative search process.

We investigate the proposed dimension embedding in the BO framework for efficient rare failure detection via extensive experimental studies. We demonstrate that our proposed Rev-Gate architecture efficiently detects rare AMS failures with significantly less runtime and reduced simulation data usage compared to several related methods.

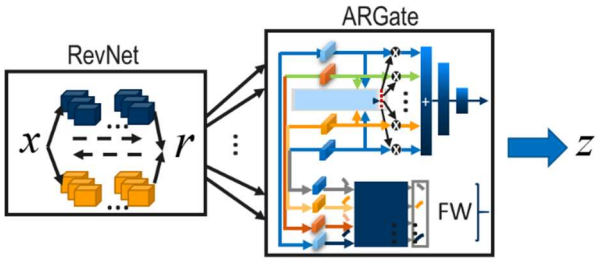


**Figure 1. Dimension reduction using a revisable neural network (RevNet) & feature importance learning (ARGate): mapping from a high-dimensional feature vector *x* to fewer features z.**

Table 1 compares several methods for failure detection of the quiescent current of a low-dropout voltage regulator (LDO): MC (Monte Carlo), EI/PI (BO using the standard EI/PI acquisition function), pBO/HDMO (our previously proposed BO methods), and Rev-Gate with BNN (this proposed approach). Our technique can find the first rare failure using a reasonable number of simulation samples within a few hours while all other methods fail.

**Table 1. Failure detection for quiescent current (spec = 11mA) of an LDO using several methods.**

| Method | # Sim | Worst Case | 1st Failure Hit | Runtime |
|---|---|---|---|---|
| MC | $330,000$ | 10.8mA | - | 47h45m |
| EI | $50_{init} + 750_{seq}$ | 7.1mA | - | 24h06m |
| PI | $50_{init} + 750_{seq}$ | 8.3mA | - | 23h43m |
| pBO | $50_{init} + 5 \times 150_{batch}$ | 10.5mA | - | 23h53m |
| HDBO | $50_{init} + 5 \times 150_{batch}$ | 10.1mA | - | 19h36m |
| **Rev-Gate with BNN** | $500_{training} + 50_{init} + 5 \times 50_{batch}$ | **11.6mA** | **621** | **3h32m** |

**Keywords:** Reversible neural networks, dimension reduction, Bayesian optimization, gating architecture, failure detection

## INDUSTRY INTERACTIONS

Texas Instruments, IBM, NXP, ARM, Intel

## MAJOR PAPERS/PATENTS

[1] H. Hu, et. al., "Advanced Outlier Detection Using Unsupervised Learning for Screening Potential Customer Returns," IEEE ITC'20.

[2] M.S. Shim, et. al., "Reversible Gating Architecture for Rare Failure Detection of Analog and Mixed-Signal Circuits," accepted to IEEE/ACM DAC'21.

[3] H. Hu, et. al., "Unsupervised Prediction of Rare Post-Silicon Defects using Neural Networks," SRC Techcon'20.

# TASK 2810.033, INTERLEAVED NOISE-SHAPING SAR ADCS FOR HIGH-SPEED AND HIGH-RESOLUTION

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## SIGNIFICANCE AND OBJECTIVES

This research will deliver an energy-efficient high-speed, high-resolution ADC architecture for high performance and emerging applications, including medical imaging, 4G/5G infrastructure, radar, production test, and defense. We will expand the bandwidth of our time-interleaved (TI) noise-shaping (NS) SAR architecture by an order of magnitude to extend SAR-ADC efficiency to high speed and high resolution.

## TECHNICAL APPROACH

Our new SAR-based architecture combines time-interleaving with noise-shaping, to break the tradeoff between speed and accuracy, and enable both high speed and high resolution. The target design space is unserved by state-of-the-art SAR ADCs. Different from conventional SAR and interleaved SAR converters, our approach provides both high resolution and high bandwidth. We expand our revolutionary new interleaved noise-shaping SAR ADC architecture to deliver an order-of-magnitude more bandwidth, as well as improved energy efficiency and enhanced robustness.

## SUMMARY OF RESULTS

The Noise-Shaping SAR (NS-SAR) is an emerging ADC architecture that offers both high resolution and high energy efficiency. State-of-the-art NS-SAR ADCs eliminate the need for op-amps, which relaxes design complexity and technology scaling issues. However, existing NS-SAR ADCs, with high FoM, are limited in bandwidth (typically in the MHz range). This makes NS-SAR ADCs unsuitable for applications that need bandwidths in the tens of MHz range, such as wireless communications. Traditionally, high-bandwidth, high-resolution applications utilize pipeline or continuous-time sigma-delta (CT-SD) ADCs, but these architectures are much more power-hungry than the NS-SAR.

We propose the new Hybrid-Loop (HL) DSM architecture (Figure 2), which combines the advantages of both CT and DT DSMs and eliminates the drawbacks. Moreover, a bandpass, time-interleaved noise-shaping (TINS) SAR quantizer further boosts the new architecture's performance. The prototype HL-DSM provides 68dB SNDR over a 100MHz BW for a quadrature input, without any calibration or tuning, while occupying only 0.09mm$^2$ and consuming 13mW at 1.6GS/s. The resulting 166dB FoMs show the potential of HL-DSM as a more robust and practical alternative to CT-DSM.

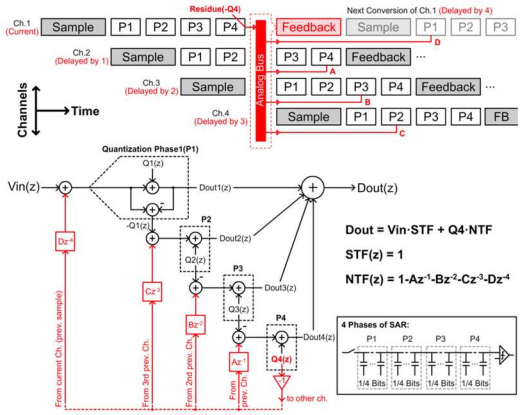


Figure 1. Interleaved noise-shaping architecture.

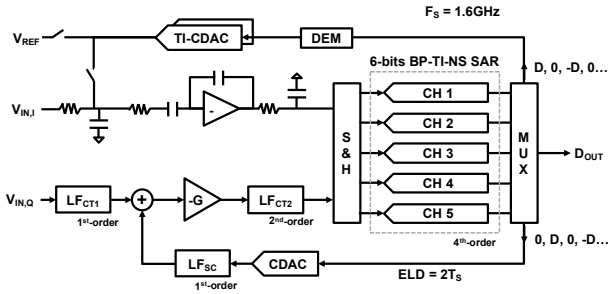


Figure 2. Hybrid CT DT Interleaved NS SAR.

**Keywords:** Sigma Delta, ADC, sensor, SAR, IoT

## INDUSTRY INTERACTIONS

Texas Instruments, Intel, ARM, NXP

## MAJOR PAPERS/PATENTS

[1] L. Jie, B. Zheng and M. P. Flynn, "A Calibration-Free Time-Interleaved Fourth-Order Noise-Shaping SAR ADC," in IEEE Journal of Solid-State Circuits, December 2019.

[2] L. Jie, B. Zheng and M. P. Flynn, "A 50MHz-Bandwidth 70.4dB-SNDR Calibration-Free Time-Interleaved 4th-Order Noise-Shaping SAR ADC," IEEE International Solid-State Circuits Conference, February 2019.

[3] L. Jie, H Chen, B. Zheng and M. P. Flynn, "A 4th order Cascaded-Noise-Shaping SAR ADC with 87dB SNDR over 100kHz Bandwidth," IEEE International Solid State Circuits Conference, February 2020.

[4] L. Jie, H Chen, B. Zheng and M. P. Flynn, "A 100MHz-BW 68dB-SNDR Tuning-Free Hybrid-Loop DSM with an Interleaved Bandpass Noise-Shaping SAR Quantizer" IEEE International Solid State Circuits Conference, February 2021.

# TASK 2810.036, HIGHLY STABLE INTEGRATED FREQUENCY REFERENCES

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## SIGNIFICANCE AND OBJECTIVES

Stable frequency references serve many time keeping functions. While quartz crystal-based references can achieve the desired electrical performance, they are bulky, expensive, power inefficient, and suffer from long start-up time. This task will develop novel architectures and circuit techniques that will overcome these drawbacks.

## TECHNICAL APPROACH

Frequency accuracy of integrated RC oscillators is limited by the temperature sensitivity of the reference resistor. We show the impact of resistor temperature coefficient on the accuracy of output frequency can be mitigated by using a parallel combination of multiple switched-resistors that are digitally-controlled by pulse-density modulated sequences. By trimming at three temperatures, second-order temperature compensation can be performed, which helps to achieve an inaccuracy of better than 150ppm at 100MHz output frequency and with 1µW/MHz power efficiency.

## SUMMARY OF RESULTS

A simplified block diagram of the proposed temperature compensated oscillator (TCO) is shown in Fig. 1. It is composed of a frequency-locked loop (FLL) that locks the period of a voltage-controlled ring oscillator (VCO) to a reference time constant ($1/F_{OUT} = 6R_{REF}C_R/126$). A voltage divider formed by a switched-capacitor resistor (SCR) and a reference resistor ($R_{REF}$) generates frequency-dependent voltage, $V_{FB}$, which is nominally equal to $V_{DD}/4$ when the switching frequency $F_{SW} = F_{OUT}/126$. The feedback loop is closed by driving the VCO with the integrated difference between $V_{FB}$, and a fixed reference voltage ($V_{REF}$) generated using a resistive voltage divider. Thanks to the large loop gain, $V_{FB} \approx V_{REF}$ and $F_{OUT} \approx 100$MHz in steady-state.

Off-state leakage current of PMOS switch in the SCR is steered away from reference capacitor $C_{FB}$ to the buffer output using a transmission gate ($TG_P$). PMOS transistor ($MP_S$) is added to prevent $C_R$ from being connected to the buffer output voltage. Because $MP_S$ source is connected to $V_{DD}/4$ and its drain is discharged to $V_{DD}/4$, $V_{DS}$ of $MP_S$ equals zero, thus significantly reducing its leakage. Similarly, NMOS transistor ($MN_S$) and transmission gate ($TG_N$) prevent off-state leakage current of NMOS switch ($MN_C$) from flowing into $C_{FB}$. Two parallel SCRs ($SCR_1$/$SCR_2$) with a relatively large $C_{FB}$ to $C_R$ ratio (100:1) operate in a ping-pong manner to reduce $V_{FB}$ voltage ripple, thereby linearizing the relationship between switching frequency and SCR conductance

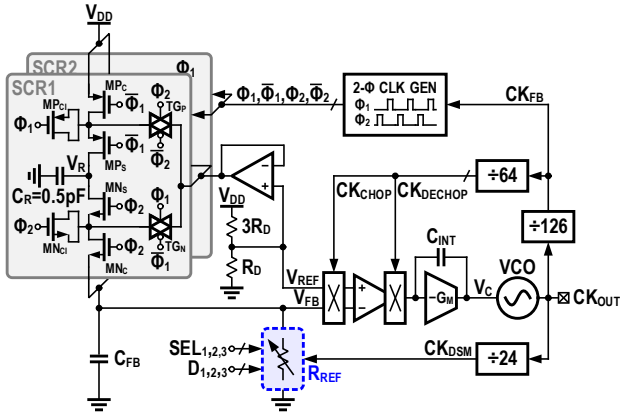


**Figure 1. Temperature compensated oscillator architecture.**

A prototype TCO was fabricated in a 65-nm CMOS process and packaged in a plastic QFN package. It occupies an active area of 0.19mm2 and draws 84.5µA from a 1.2V supply with on-chip LDOs generating 0.9V and 1.0V. D1/2/3 are determined for each sample by trimming at three temperatures (-35°C, 25°C, and 90°C) for FOUT = 100MHz. The frequency inaccuracy measured across 20 samples using R1 (189-kΩ negative TC p-poly resistor), R2 (positive TC 171-kΩ n-diffusion resistor), and R3 (208-kΩ positive TC p-diffusion resistor) is less than ±140ppm over -40°C to 95°C (2.1ppm/°C), which represents about 4x improvement over first-order compensated TCO. Measured supply sensitivity is 83ppm/V over a $V_{DD}$ range of 1.1 to 2.5V. Frequency inaccuracy is also measured with all positive TC resistors by replacing $R_1$ with a positive TC 289-kΩ n-poly resistor. The frequency inaccuracy for 20 samples is less than ±316ppm over -40°C to 95°C (4.7ppm/°C).

**Keywords:** switched resistor, frequency reference, temperature compensation.

## INDUSTRY INTERACTIONS

Texas Instruments, NXP, Intel

## MAJOR PAPERS/PATENTS

[1] K. -S. Park et al., "A second-order temperature compensated 1µW/MHz 100MHz RC oscillator with ±140ppm inaccuracy from -40°C to 95°C," 2021 IEEE Custom Integrated Circuits Conference (CICC), 2021

# TASK 2810.037, HIGH-PERFORMANCE RINGAMP-BASED ADCS

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## SIGNIFICANCE AND OBJECTIVES

Our research goal is to solidify ring amplifiers as a dominant means of closed-loop amplification in mixed-mode circuits through demonstration of performance improvements over traditional amplifiers. In this task, high-performance ring amplifier-based ADCs in FinFET technologies are explored, addressing the current need for high-speed applications in scalable CMOS.

## TECHNICAL APPROACH

For high-speed analog-to-digital converters utilizing pipelined architectures with residue amplification, two common methods to save power are the use of SAR ADCs as the sub-ADC and power-efficient amplifiers. Ring amplifiers are a good candidate to replace the traditional power-hungry residue amplifier blocks. Process scaling has become more important with the migration towards FinFET technologies, and maintaining performance with a supply voltage reduction in the presence of influences on silicon such as self-heating has become critical to address. Prototypes fabricated using 22-nm FinFETs will be used to demonstrate the performance capabilities of ring amplifier-based pipeline SAR ADCs.

## SUMMARY OF RESULTS

In this research, we are targeting the demonstration of a single-channel GS/s pipelined SAR ADC with future plans to look into reaching higher sample rates through time-interleaving.

The 12-bit hybrid (both active and passive) pipelined-SAR analog-to-digital converter aims to achieve high speed with a low-power three-stage structure. A non-binary 2-bit-per-cycle SAR ADC resolves the first 6-bits through three cycles of comparisons [1]. One bit of redundancy is used in these two bits per cycle SAR ADC to tolerate non-ideal factors. The use of non-binary decision levels introduces error correction and alleviates fluctuation of reference, comparator offset, and DAC settling time, therefore accelerating the conversion period of the first stage. The remaining residue then undergoes residue amplification using a ring amplifier. A dual-deadzone ring amplifier [2] with buffer stage enhancement inserted between Stage2 and Stage3 provides benefits for CMFB design as well as PVT stability. The proposed buffer enhanced ring amplifier achieves a much faster signal settling (for a given power) when compared with traditional op-amps. The ring amplifier performs a sufficiently accurate amplification in 400ps with a dynamic power consumption of 3mW. The back-end is comprised of a two-stage passive pipelined-SAR ADC with passive inter-stage charge-sharing and provides additional 9-bits with a significant speed advantage and minimal power, owing to the passively pipelined SAR structure. Custom 0.5fF per unit capacitor in the last two stages of SAR DACs achieve high speed SAR operation. Redundancy is distributed throughout the ADC and a total of 12-bits quantization level is provided as shown in Figure 1. Input buffering is provided with wide-swing and high-linearity, using a flipped source follower topology.

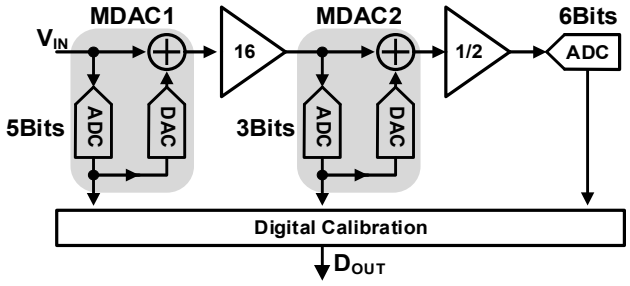


**Figure 1. The architecture for GS/s ADC.**

Preliminary simulation results of the ADC indicate a peak SNDR of 65dB in the 500MHz Nyquist bandwidth with 8mW of ADC core power consumption. The input buffer consumes an additional 6mW of power for a total system power of 14mW.

This chip has been taped out in a 22-nm FinFET technology. Into the future, we plan to move forward with the characterization of the single-channel RF ADC chip in the 22-nm FinFET technology and begin to explore the design of a time-interleaved ADC.

**Keywords:** pipeline SAR ADC, pvt stable ring amplifier, gigasample, FinFET, high speed

## INDUSTRY INTERACTIONS

NXP, Texas Instruments, Intel

## MAJOR PAPERS/PATENTS

[1] H. Hong, et al., “An 8.6 ENOB 900MS/s time-interleaved 2b/cycle SAR ADC with a 1b/cycle reconfiguration for resolution enhancement,” 2013 IEEE Int. Solid-State Circuits Conference (ISSCC), Feb 2013.

[2] A. ElShater et al., “A 10-mW 16-b 15-MS/s Two-Step SAR ADC With 95-dB DR Using Dual-Deadzone Ring Amplifier,” IEEE J. of Solid-State Circuits (JSSC), Dec 2019.

# TASK 2810.043, ANALOG OPTIMIZATION HYBRIDIZING DESIGNER'S INTENT AND MACHINE LEARNING

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## SIGNIFICANCE AND OBJECTIVES

Analog circuit design and optimization manifest as a critical phase in IC design, which still heavily rely on extensive and time-consuming manual designing by experienced experts. Building upon recent advances in machine learning, we develop a sample-efficient reinforcement learning (RL) algorithm and a design tool for automated high-quality analog sizing optimization.

## TECHNICAL APPROACH

Different from traditional applications of reinforcement learning, for analog circuit design, a smart and rapid search for high-quality design points is more desired than finding a globally optimal agent, which was a point not fully considered before. We present three techniques within the RL framework aiming at fast high-quality design point search in a data-efficient manner, as shown in Figure 1. Particularly, we explore smart non-uniform sampling, incorporate design knowledge from experienced designers into the critic network design to achieve a better reward evaluation with less data, and use the predictive power of the trained RL agent to identify high-quality design points [1].

## SUMMARY OF RESULTS

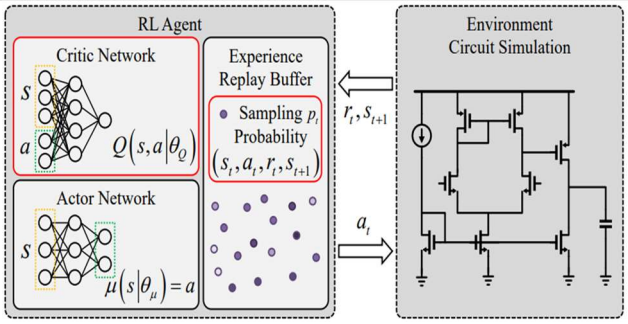


**Figure 1. Proposed reinforcement learning analog optimization.**

We develop a smart sampling technique, called *RL-NU*, to prioritize samples for exploitation over high-quality designs and exploration over poorly-trained regions of the design space in the RL training process, targeting better circuit optimization. We integrate circuit-specific design knowledge from design experience into the RL algorithm flow for achieving better design points faster, specifically via a two-stage critic network modeling technique called *RL-2SC*. Finally, we develop a local exploration method, called *RL*-TG, leveraging the prediction power of the critic network to search along the RL trajectory and achieve efficient circuit design. We demonstrate the effectiveness and efficiency of the proposed methods through extensive experiments with best circuit performance achieved in a data-efficient manner.

Figure 2 compares several methods on sizing optimization of hysteresis comparator for which the figure of merit (FOM) jointly considers gain, bandwidth, offset, and hysteresis. These methods are: Monte Carlo based sizing exploration, BO-EI/BO-POI (Bayesian optimization using EI/POI as the acquisition function), std-RL (standard DDPG RL algorithm), proposed RL-NU, proposed RL-2SC, proposed RL-TG, and the RL combining the features of RL-NU, RL-2SC, and RL-TG (labeled as "RL-proposed). As can be see, the proposed RL techniques, particularly "RL-proposed" can rapidly improve the FOM as more simulation samples are collected.

Future work will investigate sample-efficient RL based pareto-optimal multi-objective optimization and/or consider the impact of process variations.

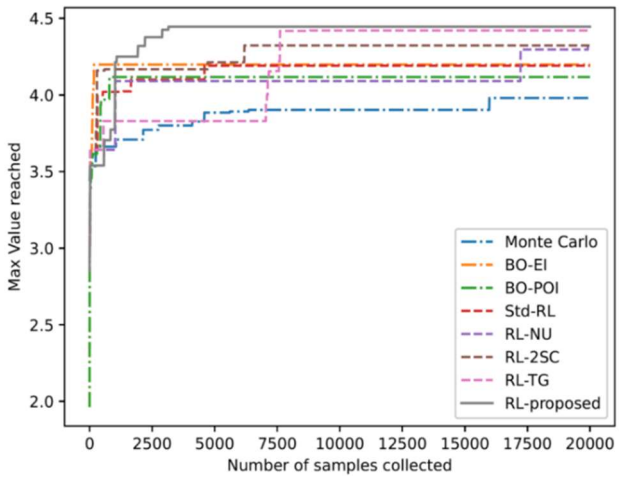


**Figure 2. Sizing optimization of a hysteresis comparator.**

**Keywords:** analog optimization, reinforcement learning, design knowledge, smart sampling, design productivity

## INDUSTRY INTERACTIONS

Texas Instruments, NXP, Intel

## MAJOR PAPERS/PATENTS

[1] Karthik Somayaji N.S., et. al., "Prioritized Reinforcement Learning for Analog Circuit Optimization with Design Knowledge," Accepted to IEEE/ACM DAC'21.

# TASK 2810.044, HIERARCHICAL CHARACTERIZATION AND CALIBRATION OF RF/ANALOG CIRCUITS USING LIGHTWEIGHT BUILT-IN SENSORS

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## SIGNIFICANCE AND OBJECTIVES

This project will explore a hierarchical calibration approach, including local calibration and system-level target setting, where information from built-in monitors is used to match the performance of individual blocks, as well as guarantee that the entire system functions in cohesion even if constraints or operating conditions change dynamically.

## TECHNICAL APPROACH

Figure 1 shows the proposed approach. Simple built-in sensors that measure current, DC voltages and RF power are used to set local circuit parameters, such as circuit bias or matching components, to optimize the performance with respect to given specifications. System-level calibration will rely on a statistical model (e.g., machine learning), whereas circuit-level calibration can be conducted with simplified mathematical models.

## SUMMARY OF RESULTS

Matching multiple paths is essential in multi-input/multi-output RF systems. Due to process variations, calibration of these paths is essential. However, in the field, the parameters may shift, causing mismatches and the part needs to be calibrated again. This is not feasible using traditional methods. Embedded components (e.g., power detectors) can be used to recalibrate the circuit in the field. An important aspect of using the power detectors for the built-in test is that it needs to include measurement set-up inaccuracies, such as noise, and mismatches between components, as well as imperfections such as the non-linear transfer curve of the monitors. Under these non-ideal conditions, the optimum design of the built-in components may differ from the theoretical optimum.

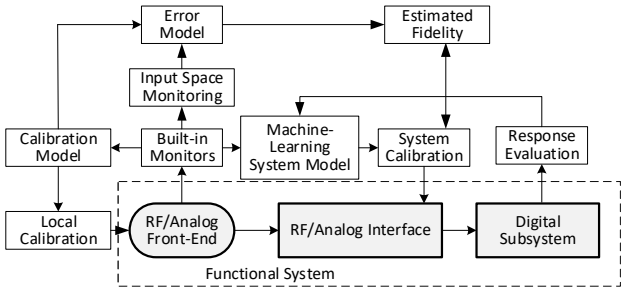


**Figure 1. Overview of the proposed approach.**

Thus, we need to develop a methodology to select the parameters of the test set-up such that highest accuracy can be attained with the given constraints on imperfections.

In BIST applications, the dynamic range of the power detectors is typically limited. Moreover, the incident power will be limited due to output power constraints as well as the gain of the coupler that routes the incident signal to the phase shifter. Thus, power limitations can be due to maximum input power of the device under test (DUT), linear region of the power detector, and noise floor. To accommodate this dynamic range, during BIST design, we need to limit the range of measured power in an interval.

Table 1 shows the optimization results, where N corresponds to the number of ports, where the number of power detectors is N - 2. K corresponds to the number of measurement components. In the (6; 2) configuration, every port has a companion and successive ports are separated by 90°.

**Table 1. Optimization of placement for power detectors based on design constraints.**

| N | K | Average Distance | |
|---|---|---|---|
| | | *g* | *Separation* ($\theta$) |
| $6^1$ | 2 | 0.71 | 90° |
| $8^1$ | 3 | 0.66 | 60° |
| $10^1$ | 4 | 0.62 | 45° |
| $6^2$ | 3 | 1.00 | 120° |
| $7^2$ | 4 | 1.00 | 90° |

**Keywords:** Analog BIST, Fault Simulation

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

# TASK 2810.052, TI PLM AS HOLOGRAM GENERATOR FOR HUD AND AR

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## SIGNIFICANCE AND OBJECTIVES

The goal of this effort is to use the Texas Instruments Phase Light Modulator (PLM) to create a holographic display for Augmented Reality (AR) and Head-up display (HUD) applications. This use of the PLM has the potential for a high impact in both the scientific and consumer electronic worlds.

## TECHNICAL APPROACH

Apply PLM-DLP (Digital Light Processor) laser beam steering technology for time-multiplexed monochromatic image transfer in free space. Evaluate FOV (Field of View), image resolution, and applicability for image transfer of 3D displays.

Update the Gerchberg–Saxton type algorithm software for the computation of the holographic pattern. Use the temporal multiplexing capability of the PLM to reduce the speckle noise. Use narrow bandwidth incoherent illumination to further reduce the speckle noise.

Develop a full-color holographic 3D display with large FOV and improved image quality using the PLM-DLP.

## SUMMARY OF RESULTS

[Task 1] The diffraction efficiency of a MEMS-based PLM with a nonlinear distribution of addressable phase levels was characterized for blazed grating. The nonlinear distribution of phase levels has a strong impact on the diffraction efficiency, which can be mitigated to an extent by how the ideal phase levels are mapped to the addressable states. When linearized, **the diffraction efficiency of the PLM increased by 15%** for the nominal wavelength.

At the tuned wavelength, the diffraction efficiency is maximum for a broad range of incidence angles in between [ − 45°, +45°]. This is a suitable range for most projection-based displays and could be improved for applications requiring a large field of views by cascading multiple devices. Additionally, increasing the mirror displacement range would be an effective strategy to increase the diffraction at longer wavelengths, such as the communication c-band, 1550 nm, and larger angles of incidence. As the wavelength increases above the tuned wavelength, the phase is under-modulated and the diffraction efficiency becomes narrower across angles of incidence. As the wavelength increases further, the peak efficiency decreases. On the other hand, when the wavelength is decreased below the tuned wavelength, the phase is overmodulated (>2π), and the peak diffraction efficiency shifts away from normal incidence. The further away from the tuned wavelength, the further the peaks shift. At 450 nm, the diffraction efficiency peaks are at ±41° with a peak-to-valley of 18%.

For wavelengths that are larger than the maximum mirror displacement, we also demonstrated that it is more favorable to scale the blaze profile—reducing the blaze angle but keeping the grating pitch, rather than truncating or wrapping the profile (keeping the blaze angle but changing the grating profile).

[Task 2] Pupil expansion using waveguide propagation and pupil replication has been a popular method of developing head-up displays and near-to-eye displays. During last year's research effort, we examined one of the limits of pupil replication, which involves projecting images at a finite distance through a single waveguide by holographic optical elements and seeing the image doubling artifact. A Zemax model and a demonstrator were developed to determine the cause of image doubling. A relationship between the designed outcoupled image distance of a waveguide, pupil size, optical path length, and angle of image doubling was established. In waveguide pupil replication, the internally propagating light should be close to collimated to mitigate image doubling. **We also found a solution to project the image at different distances**, which is an important factor for some applications, such as automotive head-up display and the seamless integration of augmented reality information with the natural environment.

**Keywords:** Augmented reality, phase modulator, 3D display, optics, holography

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] R.S. Ketchum; P.-A. Blanche, “Diffraction Efficiency Characteristics for MEMS-Based Phase-Only Spatial Light Modulator with Nonlinear Phase Distribution,” Photonics 2021, 8, 62.

[2] Craig T. Draper and Pierre-Alexandre Blanche, “Examining aberrations due to depth of field in holographic pupil replication waveguide systems,” Appl. Opt. 60, 1653-1659 (2021).

# TASK 2810.053, TI PLM TO ADVANCED LIDAR AND DISPLAY SYSTEMS

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## SIGNIFICANCE AND OBJECTIVES

Novel phase modulation scheme for TI-PLM (Phase Light Modulator) enabled PLM usable at infrared wavelength range, which is beyond the capability of the device at this point. This modulation scheme expands the application area of PLM from display at visible wavelength range to lidar and optical switch at infrared spectrum domain.

## TECHNICAL APPROACH

With polarization optics and Talbot self-imaging effect, the phase modulation depth of TI-PLM is doubled. At half of Talbot's distance of the given CGH periodic pattern displayed on PLM, a flat mirror is placed. This optical configuration forms an exact copy of the spatial phase profile on top of PLM pixels. In this manner, phase modulation depth is doubled. To effectively in-couple and out-couple light from the source to output beam polarization component is employed. The dual-phase modulation scheme is first modeled by fully vectorial electromagnetic simulation (RCWA: Rigorous Coupled Wave Analysis) and experimentally verified at a wavelength of 532nm and 1550nm.

## SUMMARY OF RESULTS

Figure 1 schematically shows the optical enhancement architecture. A vertically polarized (VP) and collimated light are deflected by a polarized beam splitter (PBS), followed by passing through a Quarter Wave Plate (QWP) that converts linear polarization (LP) to right circular polarization (RCP). Upon interaction of the RCP light with PLM, the spatial phase is modulated. PLM reflects and modulates the phase of light while changing the handedness of polarization from RHP to left-hand circular polarization (LCP). The 2nd interaction with QWP changes the polarization of light from LCP to horizontally polarized (HP) light. The mirror M1 is placed at half of the Talbot distance from the PLM as described later. The reflected light by M1 is an HP light, therefore it goes through the PBS and is converted to RCP by the 3rd interaction with QWP. Finally, the light is modulated by the PLM with the same phase modulation profile and reflected the direction along the incident laser beam via QWP and PBS. After the laser beam is doubly modulated, the laser beam diffracted towards the direction defined by the CGH pattern displayed on PLM. Figure 2 plots the prediction and experimental result of diffraction efficiency for laser beam steering as a function of wavelength.

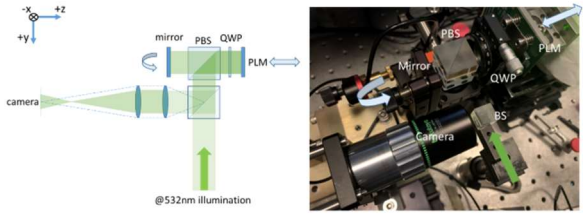


**Figure 1. Schematic and setup diagram of 532nm diffraction efficiency evaluation experiment for dual-phase modulation.**

The yellow curve shows the expected diffraction efficiency for dual-phase modulation. The gray curve shows predicted diffraction efficiency for conventional single-phase modulation. Green and red dots indicate experimentally measured diffraction efficiency for dual, and single modulation at 532nm and 1550nm, respectively. The prediction of diffraction efficiency includes loss of optical components as well as diffraction efficiency model for $0^{th}$ order as a function of wavelength. The crossing point of the yellow and gray curve shows wavelength above which dual modulation has higher efficiency. As seen from the graph, dual-phase modulation has higher efficiency above the wavelength of 900nm. In particular, at 1550nm dual-phase modulation improves diffraction efficiency by 100%.

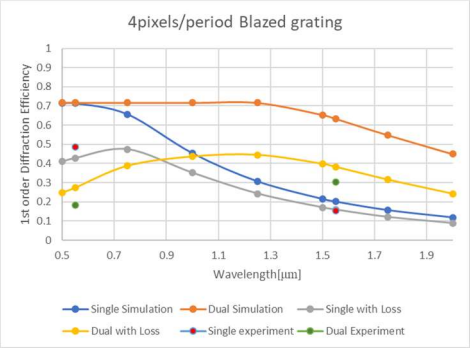


**Figure 2. Predicted and experimentally evaluated diffraction efficiency for laser beam steering as a function of wavelength.**

**Keywords:** Lidar, Holographic Display, Automotive Sensing, Beam steering, Automobiles

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] Y. Takashima, "Optical Enhancement of Phase Modulation Depth for a Phase Light Modulator" (UA21-201).

[2] Y. Takashima et al., "Review paper: imaging Lidar by Digital Micromirror Device," (Invited) Optical Review v. 27 (2020).

# TASK 2810.056, MILLIMETER WAVE PACKAGING RESEARCH-ANTENNA IN PACKAGE

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RASHAUNDA HENDERSON, MARK LEE, HONGBING LU, THE UNIVERSITY OF TEXAS AT DALLAS

## SIGNIFICANCE AND OBJECTIVES

Antenna in Package is a key enabler for future mmwave front-end modules. This project focuses on the design and characterization of antennas integrated on various packages incorporating antenna feeds, transmission lines, chip-package interconnections, and packaging materials that meet the mmwave and mechanical requirements over WR8 and WR5 frequency bands.

## TECHNICAL APPROACH

In Phase 1 (Aug'20-May'21) two package technologies and two antenna types were shortlisted from different packages, transmission lines, and antenna types. Package designs, antenna & feed designs, and preliminary simulations along with a high-frequency characterization of packaging materials and basic mechanical vibration models for the shortlisted packages were performed. Tools used include Ansys-HFSS for high-frequency simulations, Abaqus for vibration simulations, and free space spectrometry for materials characterization. This initial evaluation opens up into Phase 2 of the project with design optimization, test vehicles build on selected package prototypes and measurements along with vibration testing.

## SUMMARY OF RESULTS

Detailed package models were developed for Flip-Chip enhanced QFN (FCeQFN) package, Embedded Die enhanced QFN (EDeQFN) package, and Fanout Wafer Scale Package (FOWCSP). FOWCSP is used as a benchmark package. The two major types of antenna types shortlisted include slot bow tie and E-patch. Transmission lines used in the shortlisted packages feeding the suitable antennas include conductor-backed coplanar waveguide (CBCPW), grounded CPW (GCPW), microstrip, and stripline. The simulations were done to assess the performance over 90-140GHz (WR8) and 140-220GHz (WR5) frequency bands. The preliminary simulation results of slot bow-tie antenna integration in an FCeQFN are given in Figure 1. The mmwave characterization of some of the QFN and FOP WCSP package mold compounds showing the average dielectric constant (Dk) and dissipation factor (Df) over the WR5 band are summarized in Table 1.

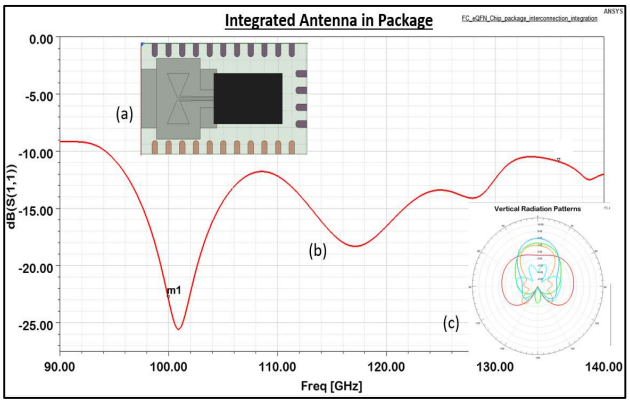


**Figure 1. Reflection loss and radiation pattern for a Slo Bow-Tie antenna fed by a CBCPW and integrated with a FCeQFN package. (a) Integrated package model, (b) Reflection Loss over WR8 band, (c) Vertical radiation pattern of the antenna.**

Material characterization in this frequency band for these packaging materials is relatively new. The preliminary measurement data has been sent to IEEE Trans on CPMT journal (Letters) for review in May 2021.

**Table 1. Measured Dk and Df values for some QFN and FOWCSP mold compounds.**

| Sample | Dk 180GHz | Df 180GHz | Comments |
|---|---|---|---|
| HC1 FOWCSP | 3.60 | 0.011 | Dispersionless |
| HC2 FOWCSP | 3.65 | 0.012 | Dispersionless |
| HC3 FOWCSP | 3.69 | 0.011 | Dispersionless |
| SC1 QFN | 3.63 | 0.009 | Dispersionless |
| SC2QFN | 3.62 | 0.009 | Dispersionless |
| HC3QFN | 3.60 | 0.012 | Dispersionless |

Optimization of package, transitions, and antenna designs, test vehicles/package structures prototyping, HF measurements, and mechanical integrity measurements are planned in Phase 2. The eQFN package has some novelty and the antenna integration approaches above 100GHz are innovative in this package.

**Keywords:** Enhanced QFN package, Planar antennas, Transmission lines, Chip-Package transitions, mmwave frequencies

## INDUSTRY INTERACTIONS

Texas Instruments, Intel, NXP

## MAJOR PAPERS/PATENTS

# TASK 2810.058, MACHINE LEARNING-BASED OVERKILL/UNDERKILL REDUCTION IN ANALOG/RF IC TESTING

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## SIGNIFICANCE AND OBJECTIVES

With the rising complexity of semiconductor devices, testing procedures have become complex and time-consuming. Depending on the nature of the test solution, some good chips will be discarded (overkill) or some defective chips being retained (underkill). We exploit machine learning-based solutions to develop a comprehensive yield management scheme.

## TECHNICAL APPROACH

For the problem of overkill, we propose a multivariate regression-based solution that predicts the values of empirically defined test measurements. We take advantage of the correlation among different test measurements and use the tests that are part of product specifications as predictors. For underkill, we use the devices probe test measurements across multiple insertions as predictors and train a one-class classifier to identify devices that may fail on-site and end up being a customer return. Due to the vastness of probe test measurements, we first subject them to agglomerative feature reduction and then employ the classifier.

## SUMMARY OF RESULTS

For overkill, an industrial dataset of 92,022 devices with measurements from 66 tests that are part of product specification and 241 tests that are empirically defined is utilized. The dataset was provided by Texas Instruments Inc. Out of the 92,022 devices, 9.6% of devices fall on our focus group which passes the product specification tests but fails tests that are empirically defined. We used the 87.21% of devices that pass both sets of tests as our predictors in our regression model to predict the 241 test measurements' values for the 9.6% of the devices.

**Table 1. Test Outcome after Regression.**

| | | Tests part of Product Specification | |
|---|---|---|---|
| | | **Pass** | **Fail** |
| **Empirically defined tests** | **Pass** | 80,261 **+ 7953** | **887** |
| | **Fail** | 726 | 2195 |

Based on Table 1, we can observe that before regression the 8,840 devices that fail empirically defined tests and pass all the tests that are product specification but were still discarded as fail. After regression and based on the predicted values, we were able to recover around 7,953 devices and move them back to the group where they pass both sets of tests. We are currently exploring ways to verify our results since there is no existing ground truth.

For underkill, an industrial dataset of 24,000 devices was provided by Texas Instruments Inc. The dataset consisted of 19 customer returns and each of these can be further classified into different fault-id. Due to the limited customer return data, we generate synthetic instances of customer returns to train the classifier for each fault ID.

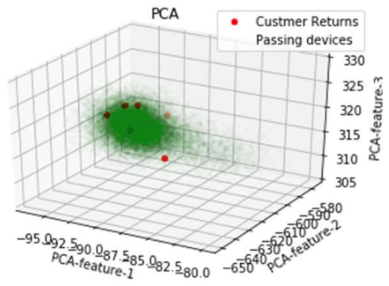


**Figure 1. Classification of customer returns for Fault ID 1.**

From the confusion matrix in Table 2, for fault-id 1, we get an accuracy of 90.7% for the classifier and this resulted in 81.56% of the customer returns being classified accurately. Similarly, results were observed for other fault IDs as well.

**Table 2. Confusion Matrix of Fault ID = 1 – Classification.**

| | **Customer Returns** | **Passing Devices** |
|---|---|---|
| **Customer Returns** | 6551 | 1481 |
| **Passing Devices** | 0 | 8011 |

We presented two adaptive, machine learning-based approaches to address the problems of overkill and underkill. We are working on verifying the results and exploring unsupervised learning solutions as well.

**Keywords:** adaptive test, post-silicon calibration, machine learning

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

[1] D. Neethirajan, V. A. Niranjan, D. Webster, A. Nahar and Y. Makris, "Machine Learning-Based Overkill Reduction through Inter-Probe Test Correlation." (Conference paper in preparation)

# TASK 2810.060, INTELLIGENT, LEARNING ADCS FOR THE POST FIGURE-OF-MERIT WORLD

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## SIGNIFICANCE AND OBJECTIVES

Although there has been tremendous progress in ADC performance, the research community has focused on energy efficiency, and in particular energy Figure of Merit (FoM). This research will redefine ADCs as information extraction tools, dramatically increasing their capability and utility in communication and sensing systems.

## TECHNICAL APPROACH

Existing sensor interfaces also create too much data and provide too little information. Machine learning approaches, such as feature extraction and classification, can overcome bandwidth and power limitations; however, traditional machine-learning methods are expensive. We propose a new class of intelligent and aware ADCs that directly extract information.

## SUMMARY OF RESULTS

Our bitstream processing approach embeds neural network processing directly at the delta-sigma bitstream output. Sophisticated processing, performed directly on delta-sigma bitstream output, removes the need for conventional power-hungry DSP. With embedded machine learning capabilities, the data bandwidth generated by the interface is reduced by orders of magnitude.

We use bitstream processing (BSP) to implement a bitstream neural network (BSNN) provides to add learning and classification capabilities within the ADC. In delta-sigma modulation, the combination of oversampling and noise shaping enables a high SNR modulator output with a single-bit (or low-resolution) quantizer. Conventionally, the low-resolution digital output of the delta-sigma modulator is low-pass filtered and decimated before further DSP. In the conventional approach, DSP is performed at a lower clock rate after decimation but at the cost of an increased word width. In BSP, on the other hand, the bitstream modulator output is directly processed to take advantage of the low word width. This approach was first proposed to realize a multiplier-less digital filter with a single-bit delta modulator output. A significant advantage of BSP is that it replaces large multipliers with simple MUXs. The need for decimation can be eliminated or significantly reduced.

Inspired by biology, many ASR schemes consider features of the time-varying frequency-dependent power domain (known as the spectrogram) to classify speech. In practical situations, environmental noise and interference from other speakers degrade the quality of the spectrogram features. Beamforming is an indispensable tool in hearing-aids, wireless communication, sonar, and ultrasound imaging to enhance the desired signal and reject interferers. Acoustic beamforming combines the outputs of multiple microphones to spatially filter the signal.


**Figure 1. Bitstream neural network processor directly operates on the bitstream.**

This work introduces a compact, low-power microphone-to-spectrogram beamforming frontend processor for speech recognition. Our approach harnesses the efficiency of an array of sigma-delta modulators digitizes eight microphone inputs. We take advantage of bitstream processing for beamforming and feature extraction. The prototype directly produces a Mel-frequency spectrogram output without the need for decimation filtering.

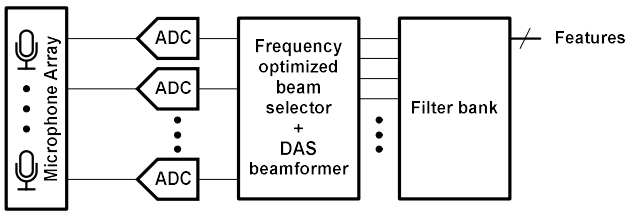


**Figure 2. Speech processing front end.**

**Keywords:** ADC, bitstream, modulator, spectrogram, beamforming

## INDUSTRY INTERACTIONS

NXP, Intel

## MAJOR PAPERS/PATENTS

[1] T. Kang, S. Lee, M. Haghigat, D. Abramson, and M. P. Flynn, "A 650¬µW 4-channel 83dBA-SNDR Speech Recognition Front-End with Adaptive Beamforming and Feature Extraction," IEEE Custom Integrated Circuits Conference (CICC), March 2021.

# TASK 2810.062, MULTI-CARRIER DAC-BASED TRANSMITTER ARCHITECTURES FOR 100+GB/S SERIAL LINKS

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## SIGNIFICANCE AND OBJECTIVES

Clock jitter places fundamental performance limitations on common wireline transmitters, necessitating clock generation and distribution circuitry that achieve rms jitter of a few hundred femtoseconds. The DAC-based transmitter design techniques in this project aim to significantly improve jitter robustness and reduce system equalization complexity.

## TECHNICAL APPROACH

A new multi-carrier DAC-based transmitter architecture is in development that is capable of providing jitter robustness for baseband and coherent multi-tone modulation applications. The transmitter utilizes novel techniques to improve the wireline polar transmitter speed and efficiency, including a high-speed injection-locked oscillator-based digital phase modulator and DAC-based FIR filtering in the segmented output driver. Efficient digital FIR filtering and linearization techniques, including a look-up table equalizer and an output stage pre-distortion DAC are also in development.

## SUMMARY OF RESULTS

Figure 1 shows the proposed multi-carrier DAC-based transmitter configured to transmit 128Gb/s with baseband (BB) PAM-4, mid-frequency band (MB) QAM-16, and high-frequency band (HB) QAM-16 modulations. 160 parallel bits at 800MHz drive the DSP and pass through FIR filters that are programmable from 1-8 taps. To achieve sufficient output stage linearity, the outputs of these filters are summed to generate a parallel 2b pre-distortion code. The output of the 800-MHz DSP is 3 parallel streams of 16 symbols that are represented with a 6b code, which represents the level of the BB PAM-4 signal and the amplitude of the MB and HB QAM-16 signals, a 4b phase code for the MB and HB QAM-16 signals, and the 2b pre-distortion code. This architecture provides several benefits. First, each channel is operating at an effective

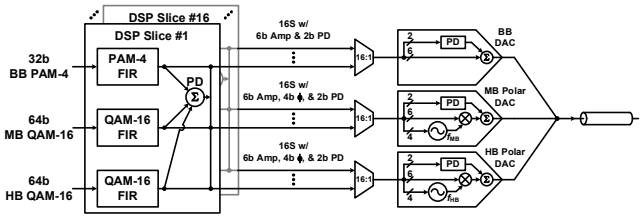


**Figure 1. Multi-carrier DAC-based transmitter.**

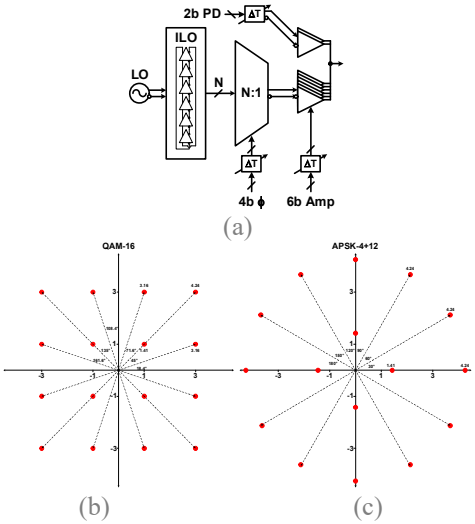


**Figure 2. (a) Digital polar output DAC. 16-point constellations: (b) QAM-16 and (c) APSK-4+12.**

12.8GS/s sampling/serialization rate, which is significantly lower than the 64GS/s sampling rate required for conventional PAM4 modulation, allowing for close to a 6X improvement in simulated rms jitter tolerance. Second, the up-conversion performed in the MB and HB channels perform mixer-baser self-equalization and provide channel loss compensation. Finally, the polar transmitter output stages provide the ability to support multiple 16-point constellations.

The proposed digital polar transmitter output stage used in both the MB and HB channels is shown in Figure 2. A given constellation point is realized by using the digital phase code to generate the desired phase from the high-speed phase modulator. This output phase passes to the output driver where it is scaled by the 6b amplitude control to realize the desired magnitude. The proposed polar architecture provides the flexibility to generate multiple 16-point constellations other than the conventional square QAM-16 constellation shown in Figure 2, which has three different output magnitudes. For example, the APSK-4+12 constellation allows all the outer 12 points to have the same maximum magnitude.

**Keywords:** Digital-to-analog converter, frequency-interleaving, jitter, transmitter, serial link

## INDUSTRY INTERACTIONS

Intel, NXP, Texas Instruments

## MAJOR PAPERS/PATENTS

# TASK 2810.063, ANALOG AND DIGITAL ASSIST TECHNIQUES TO IMPROVE MIXED-SIGNAL PERFORMANCE

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## SIGNIFICANCE AND OBJECTIVES

This task will develop new digital assist techniques for mixed-signal circuits in a range of applications, to improve density, energy efficiency, process scalability/portability, and other key performance metrics.

## TECHNICAL APPROACH

This project focuses on improving tradeoffs in state-of-the-art digitally-assisted analog circuits, identifying opportunities for new assist approaches, and broadly pushing forward the trend of digitizing conventionally analog heavy mixed-signal building blocks with an eye towards extreme scaling/density, ultra-low power design, or other metrics. We initially select three types of circuits to investigate: 1) digital LDOs, which are commonly in use today in advanced SoCs with multiple power domains; 2) low-power crystal oscillators for use in real-time clocks and other always-on timekeeping applications within IoT and ultra-low-power sensing systems; 3) time amplifiers for use in time-to-digital conversion, which find use in in-memory computing, on-chip calibration schemes, ADCs, and many other settings.

## SUMMARY OF RESULTS

Digital LDOs (DLDOs) are popular due to their process scalability and low-voltage operation. For high-performance applications with rapid power mode transitions (10s of mA/ns), conventional DLDOs require multi-GHz sampling rates and nF-range stabilizing output capacitors to reduce voltage droop, incurring large power and area overheads. Recently, analog-assisted (AA) DLDOs were introduced to circumvent this trade-off between power/output capacitance and transient response.

In this work, we propose to use a conventional DLDO-like structure to control the gate voltage of a single large output device (PMOS), as shown in Fig. 1. This output stage configuration stage is conceptually similar to a charge-pump-based LDO. In the proposed design, the PMOS is biased at weak inversion and its gate is coupled to $V_{OUT}$, allowing more than 2× conductance boost compared to previous AA-DLDOs. In addition, because the gate voltage of the PMOS is decoupled from the input voltage, fast transient response and droop performance can be obtained across a wide range ($V_{in}$=0.5-0.9V), facilitating the broad use of this design. Table 1 summarizes the measured performance. When the load current changes from 10mA to 60mA in 1ns, the measured voltage droop at $V_{OUT}$ is 110mV at $V_{IN}$ = 0.9V and $V_{IN}$ = 0.5V, which shows sub-fs speed FOM = ($C_{TOTAL}$·$V_{DROOP}$/$\Delta I_{LOAD}$)·($I_Q$/$I_{LOAD}$), representing state-of-the-art performance.

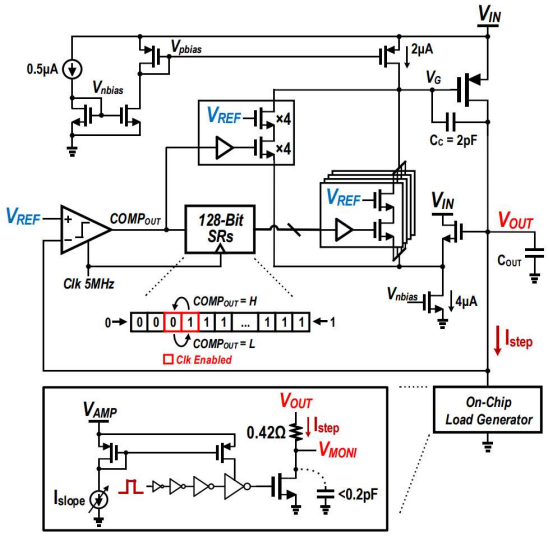


**Figure 1. Proposed digital LDO and on-chip load generator.**

**Table 1. Performance summary of the test chip.**

| | This work |
|---|---|
| Technology | 28nm |
| Supply voltage [V] | 0.5-0.9 |
| Output Voltage [V] | 0.45-0.85 |
| $I_{LOAD,MAX}$ [mA] | 100 |
| Area [mm$^2$] | 0.03 |
| $f_{CLK}$ [MHz] | 5 |
| $C_{TOTAL}$ [nF] | 0.002 |
| $I_Q$ [µA] | 5.9-8.2 |
| Droop [mV] | 110 |
| $\Delta I_{LOAD}$ @$t_{EDGE}$ | 50mA @1ns |
| FOM [fs] | 0.52-0.72 |

**Keywords:** digital LDO, voltage regulators

## INDUSTRY INTERACTIONS

NXP

## MAJOR PAPERS/PATENTS

# TASK 2810.071, ACCURATE COMPACT TEMPERATURE SENSORS FOR THERMAL MANAGEMENT OF HIGH-PERFORMANCE COMPUTING PLATFORMS

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## SIGNIFICANCE AND OBJECTIVES

The objective is to develop a strategy for designing very compact densely distributed temperature sensors that can be used for real-time power-thermal management with the accuracy needed for reliably managing the failure mechanisms inherent in silicon. Significance is in providing sensor output as a key input into a robust power/thermal management controller.

## TECHNICAL APPROACH

Very compact temperature sensors that can be widely dispersed at critical locations throughout an integrated circuit will be designed. Tentatively these compact sensors will be a single small MOS transistor or pairs of MOS transistors where the temperature is dependent upon the I-V characteristic of these devices. Located at a less-critical location where area requirements are also relaxed will be a Temperature Management Controller (TMC) that will extract temperature from many temperature sensors. The inter-relationship between the temperature of the TMC and the temperature at the remote temperature sensor locations will be managed through an appropriate calibration algorithm.

## SUMMARY OF RESULTS

The target thermal mask for the temperature sensors is shown in Fig. 1. In this figure, the absolute accuracy is 100 m°K over the critical temperature range from 75°C to 95°C but much more relaxed outside of this range. This should provide for managing the variation in the thermal-restricted mean time to failure (MTF) of an integrated circuit to approximately 10% of the target value.

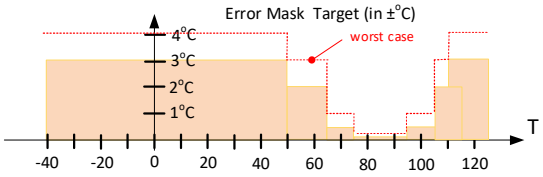


**Figure 1. Target thermal mask for temperature sensors.**

A simplified circuit diagram of a temperature sensor array is shown in Fig. 2. Though only analog signals are shown, the temperature output will be expressed in digital form. The TMC which is operating at temperature $T_1$ will provide bias currents from remote temperature sensors through a current MUX. Though conceptually a single transistor could be used to sense temperature, it can be shown that the temperature dependence of the bias current has a significant effect on the output voltage of single-transistor temperature sensors and invariably this will necessitate accurately measuring the temperature $T_1$ to obtain the temperature of the $k^{th}$ temperature sensor, $T_{2k}$. In contrast, it can be shown that with the two-transistor temperature sensor, the temperature at the $k^{th}$ sensor output can be approximately expressed as

$$T_k \approx a_k V_{OUT3k} + b_k V_{OUT4k} \qquad 1 < k < m$$

where $a_k$ and $b_k$ are nearly independent of the temperature $T_1$ of the TMC.

Preliminary simulation results of a temperature sensor based upon the basic structure of Fig. 2 designed in a 65-nm process show a temperature error of well under 100m°K in the 75°C to 95°C window and well under 1°C over a 100°C temperature range with a multi-temperature calibration. Ongoing efforts are focused on reducing the number of calibration temperature points.

Though the inverse Widlar bias generator circuit has been used to generate the bias currents, the bias currents are quite dependent upon the temperature $T_1$. Other bias current generators that are less temperature dependent will likely reduce the number of temperature measurements that are needed to calibrate the individual temperature sensors.

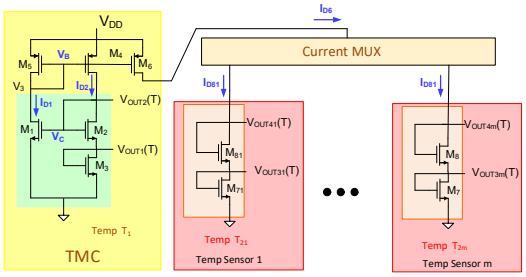


**Figure 2. Simplified schematic of temperature sensor array.**

**Keywords**: temperature sensor, thermal mask, power/thermal management, reliability

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

# TASK 2810.076, HIGH PRECISION POSITIONING TECHNIQUES BASED ON MULTIPLE TECHNOLOGIES AND FREQUENCY BANDS

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MURAT TORLAK, THE UNIVERSITY OF TEXAS AT DALLAS

## SIGNIFICANCE AND OBJECTIVES

Positioning solutions are gaining strong momentum in the IoT market, and new use cases require high accuracy. Our goal is to develop decimeter-level practical positioning algorithms for Bluetooth low energy (BLE) and WiFi systems and evaluate their performance in realistic multipath channel and interference conditions.

## TECHNICAL APPROACH

We adopt two-way ranging where access point and device exchange roles in transmitting and receiving a single tone and measuring magnitude and phase of channel response across multiple hopping frequencies. To overcome FFT resolution limitations due to limited bandwidth, measured channel frequency response data is extrapolated, smoothed, and fed to a super-resolution Multiple Signal Classification (MUSIC) algorithm to estimate time of flight (ToF) of the shortest propagation path. To enhance positioning accuracy, we use an antenna array and apply a spatial MUSIC algorithm to estimate the direction of arrival (DoA) of the shortest propagation path. Fusing ToF/DoA estimates improves positioning accuracy.

## SUMMARY OF RESULTS

We investigated signal processing techniques based on the MUSIC algorithm to improve ToF estimation beyond FFT resolution limits. These techniques overcome errors due to multipath and cases with a weak line-of-sight (LOS) propagation path. Our techniques for improved single antenna ToF estimation include the following enhancements to MUSIC: forward-backward (FB) correlation matrix averaging, eigenvector weighting, and minimum description length criteria to separate the signal and the noise subspaces. For multiple antennas at one or both devices, we combine correlation matrices across antennas before employing the MUSIC algorithm to estimate ToF.

We implemented a 75 MHz Bluetooth measurement testbed in the 2.4 GHz frequency band using two TI CC26X2R1 boards with up to four antennas per board. When using multiple antennas, the boards communicate in a 4x1 antenna configuration to obtain four spatially independent channel frequency response measurements per capture. Our measurements are taken in two outdoor parking lot environment scenarios: 1) LOS case with no obstructions between the two Bluetooth boards. 2) NLOS case with a person standing in front of one of the boards to block the LOS propagation path. As shown in Fig. 1, a total of 3840 measurements were taken for distances ranging from 1 meter to 8 meters in 1-meter increments. Each measurement distance has three trials with different placements of one of the boards.

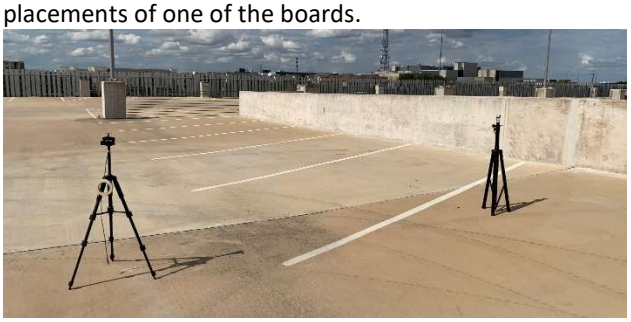

**Figure 1. Open space BLE measurement environment with a TI CC26X2R1 multi-antenna board mounted on each tripod.**

Fig. 2 depicts empirical cumulative density function (CDF) comparisons for single-antenna (SISO) ranging techniques of: FFT (IDFT), MUSIC, and forward-backward (FB) MUSIC. In the 4x1 antenna configuration (4-Ant.), we demonstrate further ranging accuracy improvement through correlation matrix combining across antennas.

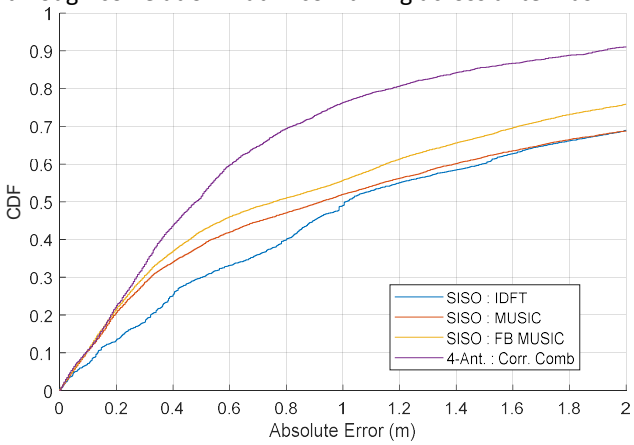


**Figure 2. Distance estimation performance for 1x1 (SISO) and 4x1 antenna configurations.**

For future work, we will investigate techniques that take advantage of multiple antennas in more challenging indoor multipath propagation environments.

**Keywords:** Positioning, BLE, WiFi, MUSIC, multipath

## INDUSTRY INTERACTIONS

Texas Instruments

## MAJOR PAPERS/PATENTS

## APPENDIX I PUBLICATIONS OF TXACE RESEARCHERS

# Conference Publications


[1] Sun, X., Boora, A., Pamula, R., Huang, C. -H., Peña-Colaiocco, D., and Sathe, V.S. (2020). UniCaP-2: Phase-Locked Adaptive Clocking with Rapid Clock Cycle Recovery in 65nm CMOS. *IEEE Symposium on VLSI Circuits, Honolulu, HI*, pp. 1-2, IEEE.

[2] Sun, X., Boora, A., Pamula, R., Huang, C. -H., Peña-Colaiocco, D., and Sathe, V.S. (2020). Model Predictive Control of an Integrated Buck Converter for Digital SoC Domains in 65nm CMOS. *IEEE Symposium on VLSI Circuits, Honolulu, HI*, pp. 1-2, IEEE.

[3] Ebenezer, P. S., Naganadhan, V., Chen, D., and Geiger, R. (2020). Three-Junction Bandgap Circuit with Sub 1 ppm/oC Temperature Coefficient. *IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS), Springfield, MA*, pp. 305-308, IEEE.

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[5] Tulsiram, A., and Eisenstadt, W.R. (2021). Design for Testability of Low Dropout Regulators. *IEEE 39th VLSI Test Symposium (VTS), San Diego, CA*, pp. 1-7, IEEE.

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[14] Zhu, H., Guo, X., Jin, Y., and Zhang, X. (2020) PowerScout: A Security-Oriented Power Delivery Network Modeling Framework for Cross-Domain Side-Channel Analysis. *Asian Hardware Oriented Security and Trust Symposium (AsianHOST), Kolkata, India*, pp. 1-6, IEEE.

[15] Vora, S., Stockinger, M., and Rosenbaum, E. (2020). Increased Latch-up Susceptibility of ICs Using Reverse Body Bias. 42nd Annual EOS/ESD Symposium (EOS/ESD), Reno, NV, pp. 1-10, IEEE.

[16] Yang, C., Chen, W., Fan, Y., and Gui, P. (2021). A General-Regression-Neural-Network Based 5V-to-48V Three-Level Buck/Boost Power Converter with 40dB PSRR 90%-Efficiency for SSD Power Loss Protection. *IEEE Custom Integrated Circuits Conference (CICC), Austin, TX*, pp. 1-2, IEEE.

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