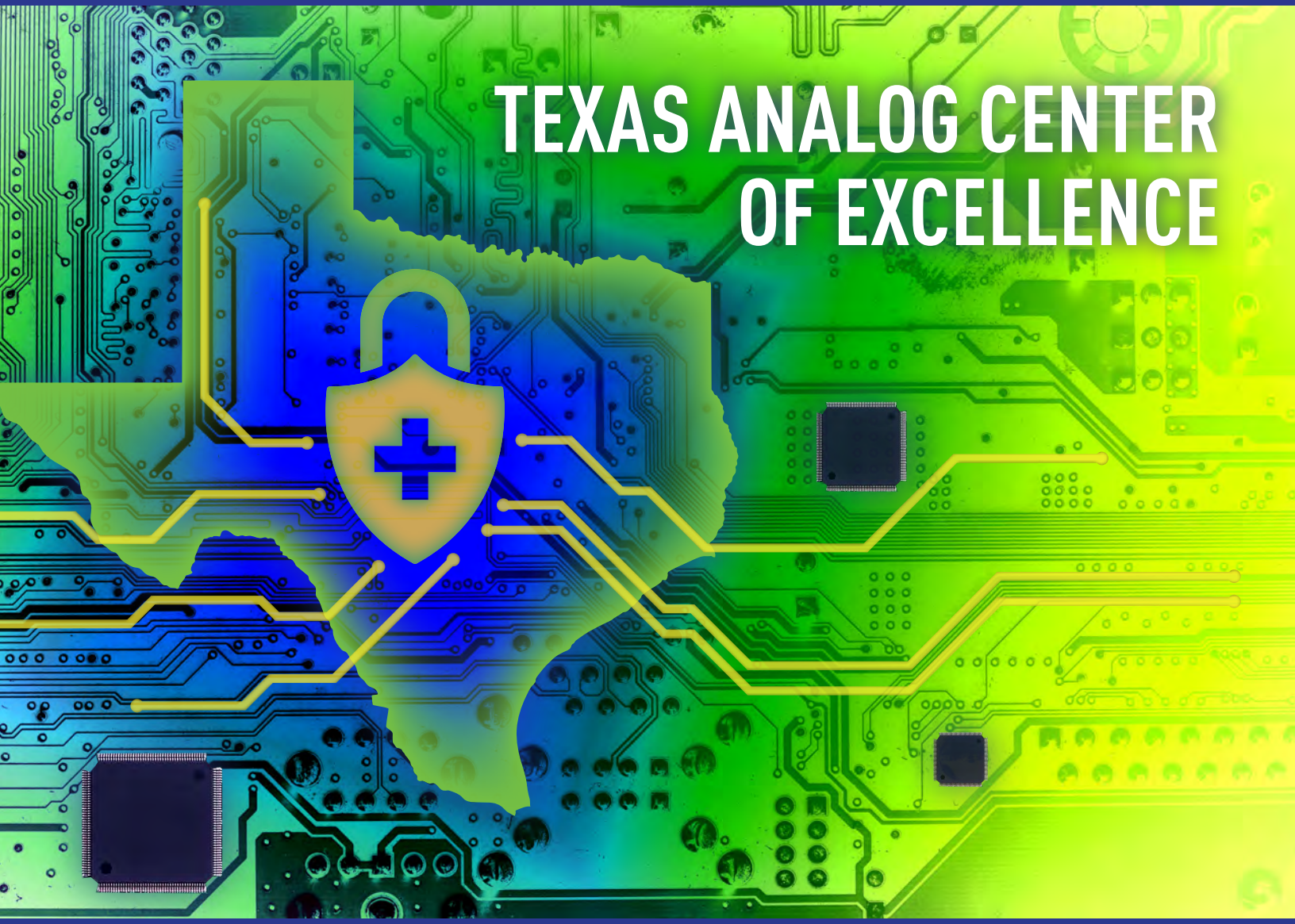
THE UNIVERSITY OF TEXAS AT DALLAS
ERIK JONSSON SCHOOL OF ENGINEERING AND COMPUTER SCIENCE



ANNUAL REPORT 2021 – 2022

Semiconductor Research Corporation

TxACE TEXAS ANALOG CENTER OF EXCELLENCE

TxACE MISSION

The Texas Analog Center of Excellence seeks to create fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, health care, and public safety and security.

TxACE THRUSTS

- *Safety, Security and Health Care*
- *Energy Efficiency*
- *Fundamental Analog Circuits*

TxACE 2021–2022 ANNUAL REPORT

The Texas Analog Center of Excellence (TxACE), located at the University of Texas at Dallas is the largest analog research center based in an academic institution. Analog and mixed signal integrated circuits engineering is both a major opportunity and challenge. Analog circuits are critical components of the majority of products for the $550+ billion per year integrated circuits industry, providing sensing, actuation, communication, power management and other functions. Digital integrated circuits such as microprocessors, logic circuits and memories are now integrating analog functions such as input/output circuits, phase locked loops, temperature sensors and power management circuits. It is also common to find microcontrollers with multiple analog-to-digital and digital-to-analog converters. These circuitries impact almost all aspect of modern life: safety security, health care, transportation, energy, entertainment and others.

Creation of advanced analog and mixed signal circuits and systems depends on the availability of engineering talent for analog research and development. TxACE was established to help translate the opportunity into economic benefits by overcoming the challenge and meeting the need through a collaboration of the state of Texas, Texas Instruments, the Semiconductor Research Corporation, the University of Texas System, and The University of Texas at Dallas.

The research tasks are organized into three research thrust areas: Safety, Security and Health Care, Energy Efficiency and Fundamental Analog. The scope of investigation extends from circuits operating at dc through terahertz, data converters that sample at a few samples/sec to 10's of Giga-samples/sec, AC-to-DC and DC-to-AC converters working at µW to Watts, energy harvesting circuits, sensors and many more. Significant improvements to existing mixed signal systems and new applications have been made and continued to be anticipated. Students who have been exposed to hands-on innovative research are forming the leading edge of analog talent flow into the industry. Close collaboration with and responsiveness to industry needs provide focus to the educational experience.

DIRECTOR'S MESSAGE

The Texas Analog Center of Excellence (TxACE) is leading analog research and education. Over the past year, TxACE researchers published 17 journal and 45 conference papers. We also filed 8 patent applications and 4 invention disclosures. 26 Ph.D., 5 M.S., and 1 B.S. students have completed their degree program.

Last year, the Center funded 70 research tasks led by 69 principal investigators at 28 institutions, including three international universities in India, Netherland and Taiwan. The Center supported 218 graduate and undergraduate students.

The Center is continuing to make impact to the industry and our way of life through its research accomplishments. There are always too many to list all here. A partial list includes demonstration of a 32.768-kHz temperature-compensated XO (TCXO) achieving an accuracy of ±4.2 ppm over a −20 °C to 85 °C with power consumption of 43 nW, a 150-kHz 300-W Active EMI Filter using a GaN switch-mode amplifier for high efficiency with a 32x lower volume than conventional LC filters, the first 48V-to-1V direct conversion DC-DC converter using a fully on-chip power NMOS transistors with competitive power efficiencies (87%) at switching frequency in the MHz range, online fault diagnosis/failure prognosis tools to warn failures of LDMOS integrated power IC's, and a digital in-memory computing chip (DIMC) using approximate arithmetic and approximation-aware training achieving 2219 TOPS/W.

I am also so pleased to share that InSilixa a company started by a former TxACE Health Care thrust leader made a successful exit. The company was founded to develop CMOS biochip devices for molecular diagnostics, specifically DNA/RNA testing, and was acquired by Danaher Corporation. Our research and researchers are indeed making differences.

The TxACE laboratory is continuing to help advance integrated circuit research by making its instruments and expertise available to researchers and our industrial partners all over the world.

I would like to thank UT Dallas, the University of Texas System, TI, and SRC, as well as many friends of TxACE all over the world for their generous support. Lastly, I would like to thank the students, principal investigators and staff for their efforts. I look forward to another year of working with the TxACE team to make our way of life better, safer and healthier through our research, education and innovation.

Kenneth K. O, Director TxACE
Texas Instruments Distinguished
University Chair Professor
The University of Texas at Dallas

BACKGROUND & VISION

The $550+ billion per year integrated circuits industry is evolving into an analog/digital mixed signal industry. Analog circuits are providing or supporting critical functions such as sensing, actuation, communication, power management and others. These circuits impact almost all aspect of modern life including safety, security, health care, transportation, energy, and entertainment. To lead this change, in particular to lead analog and mixed signal technology education, research, commercialization, manufacturing, and job creation, the Texas Analog Center of Excellence was announced by Texas Governor Rick Perry in October 2008 as a collaboration of the Semiconductor Research Corporation, state of Texas through its Texas Emerging Technology Fund, Texas Instruments Inc., University of Texas system and University of Texas at Dallas. The Center seeks to accomplish the objectives by creating fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, healthcare, and public safety and security as well as by improving the research and educational infrastructure.

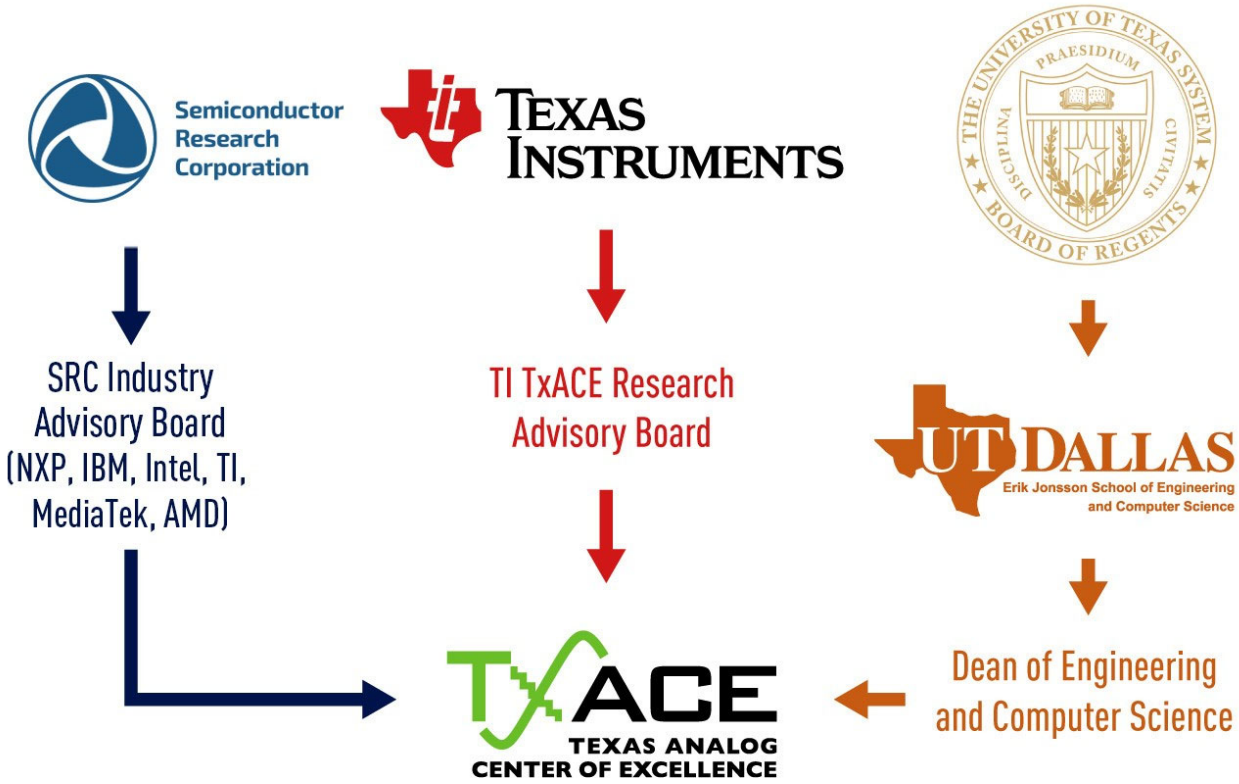


Figure 1. TxACE organization relative to the sponsoring collaboration.

CENTER ORGANIZATION

The Texas Analog Center of Excellence is guided by agreements established with the Center sponsors. Members of the industrial advisory boards identify the research needs and select research tasks in consultation with the Center leadership. Figure 1 diagrams the relationship of TxACE to the members of the sponsoring collaboration.

The internal organization of the Center is structured to flexibly perform the research mission while fully embracing the educational missions of the Universities.

Figure 2 shows the center management structure. The TxACE Director is Professor Kenneth O. The research is arranged into three thrusts that comply with the center mission: Safety, Security and Health Care, Energy Efficiency and Fundamental Analog Research. The third thrust consists of vital research that cuts across the first two research thrusts. The thrust leaders are Prof. Yiorgos Makris of the University of Texas at Dallas for safety, security and health care, and Prof. Ali Niknejad of the University of California, Berkeley for energy efficiency. The leader for fundamental analog is Prof. Pavan Hanumolu of University of Illinois, Urbana-Champaign. The thrust leaders along with Professor Dongsheng Ma of The University of Texas at Dallas form the executive committee. The committee, along with the director, forms the leadership team that works to improve the research productivity by increasing collaboration, better leveraging the diverse capabilities of principle investigators of the Center, and lowering research barriers. The leadership team also identifies new research opportunities for consideration by the Industrial Advisory Boards.

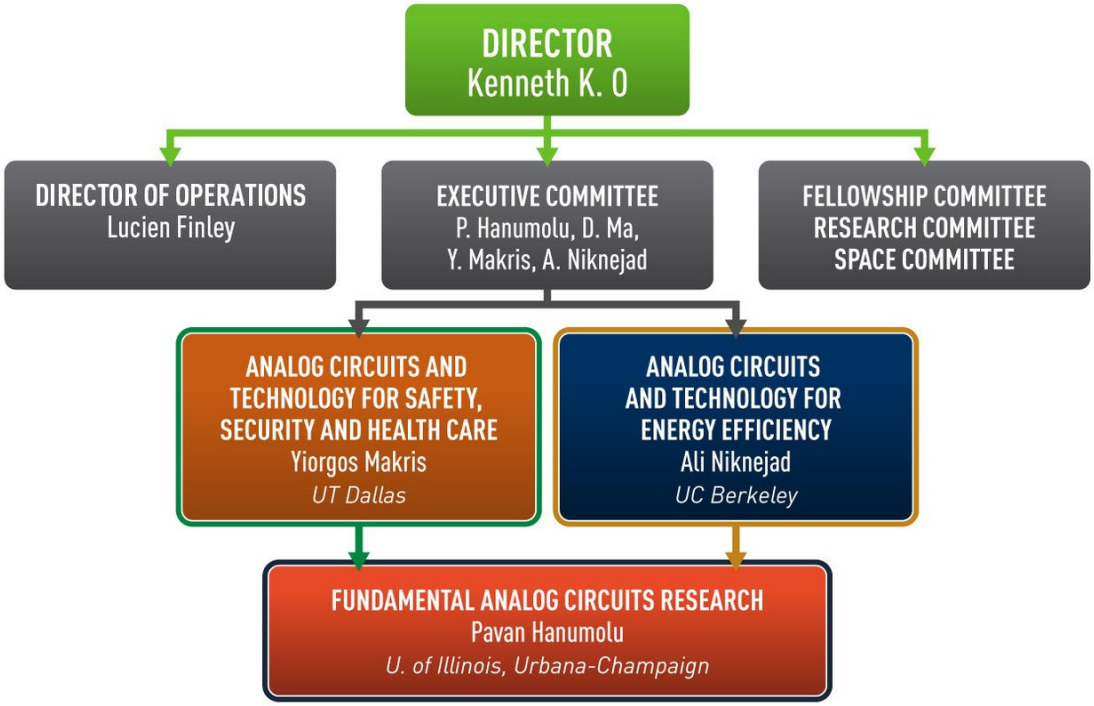


Figure 2. TxACE organization for management of research

SAFETY, SECURITY & HEALTH CARE

(Thrust leader: Yiorgos Makris, University of Texas at Dallas)

The Safety, Security, and Health care thrust focus on improving safety by mitigating various reliability threats in analog/RF devices, including ESD, supply noise, temperature stress/strain and electro-migration, as well as by developing effective machine learning-based design, verification and self-test solutions for mixed-signal automotive ICs. Particular emphasis has been placed on characterizing circuit aging, predicting failures and increasing lifetime of nano-scale CMOS circuits. This thrust also seeks to reduce the cost of millimeter wave imaging and on-vehicle radar technology for automotive safety by researching signal processing techniques that reduce system complexity and transmitter architecture that can efficiently adapt to changing antenna characteristics. Furthermore, this thrust is investigating methods for security aware dynamic power management and secure power IC design through EMI regulation. Additionally, this thrust includes research towards MEMS-based gas sensing, high-resolution TEM imaging-based reliability analysis of novel devices, and design of efficient temperature sensors for thermal performance characterization in power ICs as well as analog fault-injection, coverage estimation and diagnosis solutions for production test.

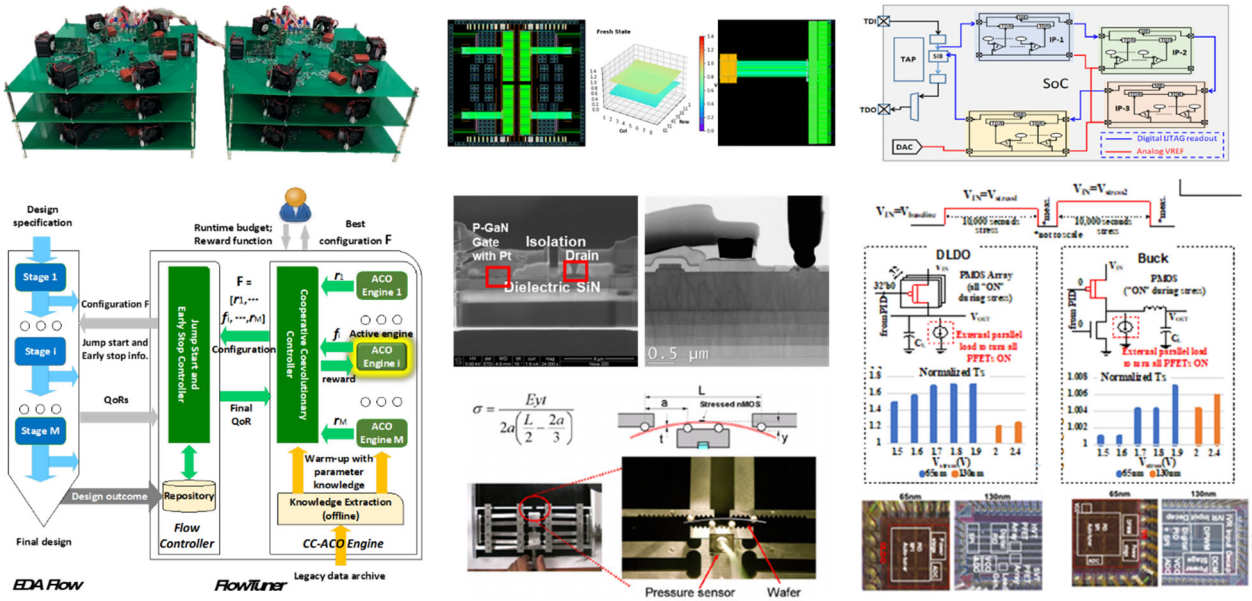


Figure 3. (Top left) Large scale dynamic testing setup for long-term reliability evaluation of LDMOS devices (B. Akin, University of Texas at Dallas), (Top middle) Power-grid EM chip with on-chip heaters and measured voltage maps (C. Kim, University of Michigan), (Top right) PCB for concurrent sampling of multi-node simultaneous analog measurements and IJTAG-compatible digital-like DfT for multiple analog IPs (D. Chen, University of Iowa), (Middle middle) Cross-sectional SEM image of a p-GaN gate device with drain and gate contact assembly for in-situ device biasing (M. Kim, University of Texas at Dallas), (Bottom left) Flow-Tuner: a multi-stage automatic tool for efficient and effective parameter tuning of VLSI design flows (J. Hu, Texas A&M University), (Bottom middle) Mechanical wafer-bending jig to strain silicon (S. Thompson, University of Florida), (Bottom right) NBTI measurements in IVR and DLDO test chips (S. Mukhopadhyay, Georgia Institute of Technology).

ENERGY EFFICIENCY

(Thrust leader: Ali Niknejad, UC Berkeley)

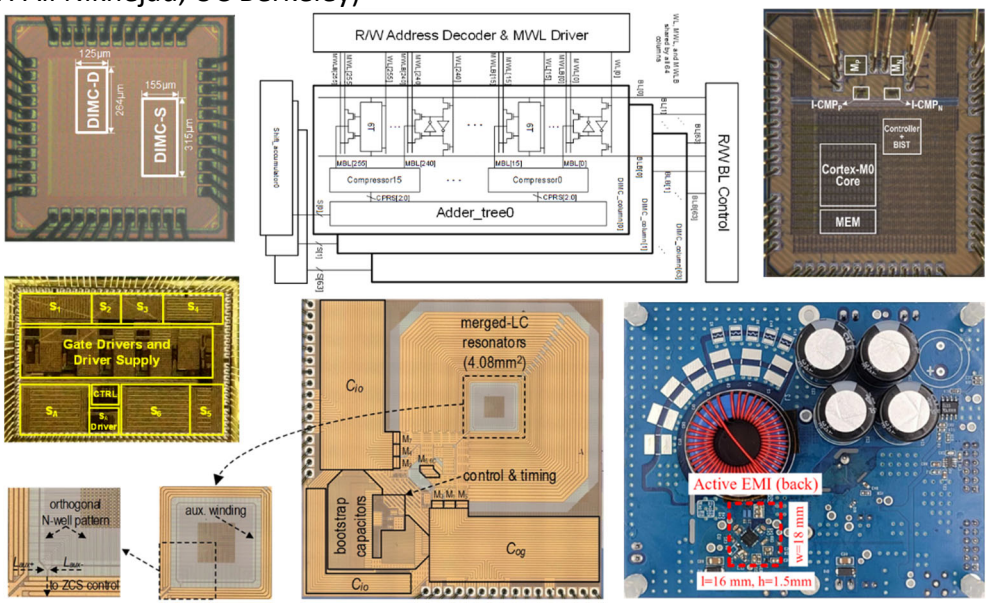


Figure 4. The TxACE Energy Efficiency thrust has diverse tasks ranging from advanced power management to digital and analog mixed-signal AI/ML for sensors and IoT systems, spanning a power range all the way from automotive kilowatts to always-on sensor systems consuming microwatts. (Top left) Demonstration of a fully digital in-memory computing chip (DIMC) achieving 2219 TOPS/W leveraging approximate arithmetic hardware to improve area and power efficiency, presented in *ISSCC* 2022 (M. Seok, Columbia University). (Top right) A regenerative breaking circuit that recycles charge to return stored domain charge into the battery instead of allowing it to leak away. The work is presented at *ISSCC* 2022 (V. Sathe, University of Washington). (Bottom left) A 2.5 – 5MHz 87% peak-efficiency 48V-to-1V integrated hybrid DC-DC converter adopting SC network with capacitor assisted dual inductor filtering presented at *ISSCC* 2022 (H. Lee, University of Texas at Dallas). (Bottom middle) A hybrid/resonant SC converter with integrated LC resonator for high-density monolithic power delivery demonstrates an integrated inductor/resonator to realize a fully integrated DC-DC power converter, presented at *ISSCC* 2022 (J. Stauth, Dartmouth). (Bottom right) A 150-kHz Active EMI Filter (AEF) using a GaN-based switch-mode amplifier. The total volume of the proposed AEF is 0.1in^3 which is equal to 1/32 of the volume of the size-optimized LC filter for the similar current attenuation (A. Hanson, U. of Texas at Austin).

The TxACE Energy and Efficiency thrust encompasses cross-cutting research tackling energy efficiency in electronic systems, spanning from advanced power management, all the way to the emerging fields of low power machine learning/AI for edge computing and applications to IoT sensor nodes. The power management research forms the foundation of the center and tackles important issues of efficiency in complex system applications, for example in digital multi-core systems that use single inductor multiple output (SIMO) DC-DC converters, addressing modeling and simulation and optimization of performance (transient response, EMI, security) using non-linear computational control, mixed-signal techniques, digital signal processing, and adaptive algorithms and design automation. This thrust investigates non-conventional hybrid architectures and integration strategies for applications in computing, large-ratio conversion from 48V down to 1V and below, EV traction, and charging applications. Many of the solutions employ mixed-signal techniques, exploiting advanced CMOS digital nodes alongside GaN power devices, and utilize novel scaling-friendly analog architectures to improve the control and expand the flexibility of the overall system.

FUNDAMENTAL ANALOG CIRCUITS RESEARCH

(Thrust leader: Pavan Hanumolu, U. of Illinois Urbana-Champaign)

The Fundamental Analog Circuits thrust focuses on cross-cutting research in analog and mixed-signal circuits, which impact all TxACE application areas (Energy Efficiency, Public Safety, Security, and Health Care). The research includes the design of various analog-to-digital converters, communication links, low-power crystal oscillators, I/O circuits, noise reduction techniques, new amplifier topologies suitable for use in nano-scale CMOS, development of CAD tools, and testing of integrated circuits.

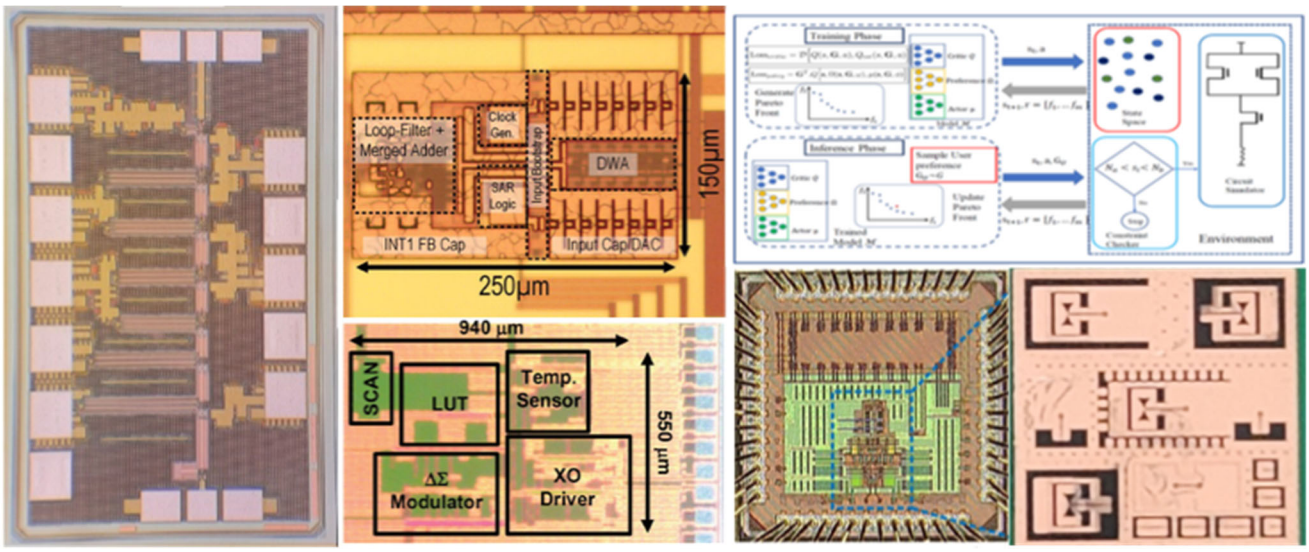


Figure 5. (Left) 170-260 GHz wideband low-noise amplifier (A. Babakhani, UCLA), (Top middle) wide dynamic range audio ADC (U. Moon, Oregon State University), (Top right) Sample-efficient reinforcement learning approach for analog circuit optimization (P. Li, UCSB), (Bottom middle) temperature-compensated nano-Watt crystal oscillator (D. Sylvester, University of Michigan), (Bottom middle right) Noise-shaping SAR ADC (M. Flynn, University of Michigan), (Bottom right) Slot bowtie antenna structures in QFN package (R. Henderson, UT Dallas).

TXACE ANALOG RESEARCH FACILITY

The centralized group of laboratories of the Texas Analog Center of Excellence dedicated to analog engineering research and training occupy a ~ 8000-ft^2 area on the 3rd floor of the Engineering and Computer Science North building (Figure 6). The facility includes RF and THz, Integrated System Design, Embedded Signal Processing, and Analog & Mixed Signal laboratories as well as CAD/Design laboratory structured to promote collaborative research**.** The unique instrumentation capability includes network analyses and linearity measurements up to 325 GHz, spectrum analysis up to 120 THz, and cryo-measurements down to 2^{o}K. The Center also added a pulsed multiple harmonic load and source pull measurement set up (up to 60 GHz for the third harmonic) and a 325-GHz antenna measurement set up. The close proximity of researchers in an open layout enables natural interaction and compels sharing of knowledge and instrumentation among the students and faculty. The TxACE analog research facility is one of the best equipped electronics laboratories. The laboratory is available for use by TxACE researchers and industrial partners all over the world.

Figure 6. TxACE Analog Research Facility

RESEARCH PROJECTS AND INVESTIGATORS

The Texas Analog Center of Excellence (TxACE) is the largest university analog technology center in the world. Table 1 lists the current principal investigators of the 70 tasks from 28 academic institutions funded by TxACE. Four universities (SMU, Texas A&M, UT Austin, UT Dallas) are from the state of Texas. 24 are from outside of Texas. Four (Delft University of Technology, Indian Institute of Tech. Kharagpur, National Taiwan University, and University of Toronto) (Figure 7) are from outside of the US. Of the 69 investigators, 21 are from Texas. During the past year, the Center supported 160 Ph.D., 32 M.S., and 26 B.S. students. 26 Ph.D., 5 M.S., and 1 B.S. degrees were awarded to the TxACE students.

Investigator	Institution	Investigator	Institution	Investigator	Institution
B. Akin	UT/Dallas	P. Hanumolu	UIUC	U. Moon	Oregon State U.
N. Al-Dhahir	UT/Dallas	R. Harjani	U. Minnesota	S. Mukhopadhyay	Georgia Tech.
D. Allstot	Oregon State U.	A. Hazra	Indian Institute of Tech. Kharagpur	B. Murmann	Stanford U.
R. Ayyanar	Arizona State U.	R. Henderson	UT/Dallas	F. Najm	U. Toronto
A. Babakhani	UC/Los Angeles	D. Heo	Washington State University	K. O	UT/Dallas
B. Bakkaloglu	Arizona State U.	S. Hoyos	TEES	S. Ozev	Arizona State U.
K. Basu	UT/Dallas	J. Hu	TEES	S. Palermo	TEES
D. Blaauw	U. Michigan	C. Huang	Iowa State U.	P. Pande	Washington State U.
P. Blanche	U. Arizona	T. Huang	National Taiwan U.	G. Rincón-Mora	Georgia Tech.
A. Chatterjee	Georgia Tech.	Y. Kaneda	U. Arizona	R. Rohrer	SMU
D. Chen	Iowa State U.	C. Kim	U. Minnesota	E. Rosenbaum	UIUC
Y. Chen	Duke U.	M. Kim	UT/Dallas	S. Sapatnekar	U. Minnesota
Y. Chiu	UT/Dallas	H. Le	UC/San Diego	V. Sathe	U. of Washington
P. Dasgupta	Indian Institute of Tech. Kharagpur	H. Lee	UT/Dallas	M. Seok	Columbia U.
J. Doppa	Washington State University	M. Lee	UT/Dallas	H. Shichijo	UT/Dallas
M. Flynn	U. Michigan	P. Li	UC/Santa Barbara	J. Stauth	Dartmouth College
J. Friedman	UT/Dallas	K. Lin	National Taiwan U.	D. Sylvester	U. Michigan
H. Fu	Iowa State U.	J. Liu	UT/Dallas	Y. Takashima	U. Arizona
I. Galton	UC/San Diego	H. Lu	UT/Dallas	S. Thompson	U. Florida
R. Geiger	Iowa State U.	D. Ma	UT/Dallas	M. Torlak	UT/Dallas
S. Gómez-Díaz	UC/Davis	K. Makinwa	Delft University	G. Trichopoulos	Arizona State U.

Investigator	Institution	Investigator	Institution	Investigator	Institution
J. Gu	Northwestern U.	Y. Makris	UT/Dallas	H. Wang	Georgia Tech.
A. Hanson	UT/Austin	P. Mercier	UC/San Diego	H. Wang	National Taiwan U.

Table 1. Principal Investigators (May 2021 through April 2022)

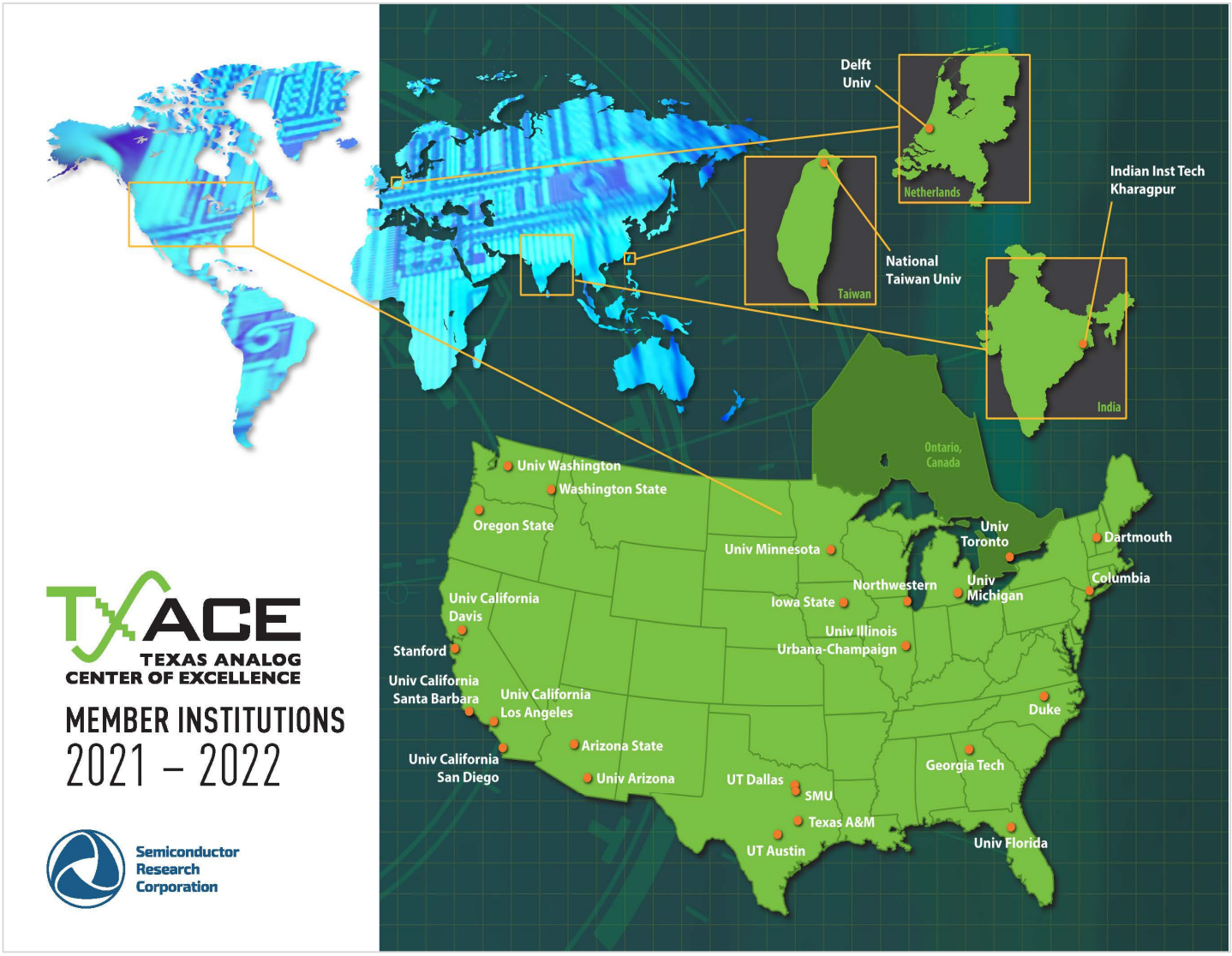


Figure 7. Member Institutions of Texas Analog Center of Excellence

SUMMARY OF RESEARCH PROJECTS

The 70 research projects funded through TxACE during 2021-2022 are listed in Table 2 below by the Semiconductor Research Corporation task identification number.

	Task	Thrust	Title	Task Leader	Institution
1	2712.029	SS	Novel Super-resolution and MIMO Techniques for Automotive and Emerging Radar Applications	Torlak, Murat	UT/Dallas
2	2810.012	EE	NPSense - Nano-Power Current Sensing	Makinwa, Kofi	Delft University
3	2810.019	FA	Design Automation for Coverage Management in Analog and Mixed-Signal SOCs	Dasgupta, Pallab Hazra, Aritra	Indian Institute of Tech. Kharagpur
4	2810.021	SS	A Collaborative Machine Learning Approach to Fast and High-Fidelity Design Prediction	Hu, Jiang Chen, Yiran	TEES and Duke University
5	2810.022	SS	A Collaborative Machine Learning Approach to Fast and High-Fidelity Design Prediction	Chen, Yiran Hu, Jiang	Duke University and TEES
6	2810.023	SS	Machine Learning Driven Automatic Mixed-Signal Design Verification-Validation for Automotive Applications	Chatterjee, Abhijit	Georgia Tech.
7	2810.025	SS	Machine Learning-Based Layout Analysis and Netlist Optimization for Defect Tolerance and Design Robustness to Process Imperfections and Variations	Makris, Yiorgos	UT/Dallas
8	2810.027	SS	Measurement and Modeling of Stress/Strain on Analog Transistor and Circuit Parameters	Thompson, Scott	University of Florida
9	2810.028	FA	Robust ATE Multi-Site HW Design to Enable Effective Analog Performance Testing in Analog-Mixed-Signal (AMS) SoCs	Chen, Degang	Iowa State University
10	2810.029	FA	170GHz – 260GHz Wideband PA and LNA Design in Silicon	Babakhani, Aydin	UCLA
11	2810.030	FA	Neural Network Recognition & On-Chip Online Learning with STT-MRAM	Friedman, Joseph	UT/Dallas
12	2810.031	FA	Development and Assessment of Machine Learning Based Analog and Mixed-Signal Verification	Li, Peng	UC/Santa Barbara

	Task	Thrust	Title	Task Leader	Institution
13	2810.032	EE	DRIVR: A Digital, Re-configurable, Unified Clock-Power (UniCaP) Fabric for Energy-Efficient SoCs	Sathe, Visvesh	University of Washington
14	2810.033	FA	Interleaved Noise-Shaping SAR ADCs for High-Speed and High-Resolution	Flynn, Michael	U. of Michigan
15	2810.034	EE	Always-on Keyword Spotting based on Analog-Mixed-Signal Computing Hardware	Seok, Mingoo	Columbia University
16	2810.035	EE	Computationally Controlled Integrated Voltage Regulators	Sathe, Visvesh	University of Washington
17	2810.036	FA	Highly Stable Integrated Frequency References	Hanumolu, Pavan	UIUC
18	2810.037	FA	High-performance Ringamp-based ADCs	Moon, Un-Ku	Oregon State University
19	2810.038	SS	Extreme Temperature Digital, Analog, and Mixed-Signal Circuits (ET-DAMS)	Kim, Chris	U. of Minnesota
20	2810.039	EE	Development of Compact and Low Cost Fully Integrated DC-DC Converter with Resonant Gate Drive and Intelligent Transient Response	Gu, Jie	Northwestern University
21	2810.040	EE	Hybrid/Resonant Sc Converters with Integrated Lc Resonator for High-Density Monolithic Power Delivery	Stauth, Jason	Dartmouth College
22	2810.041	SS	ESD Protection for IO Operating at 56 Gb/s and Beyond	Rosenbaum, Elyse	UIUC
23	2810.042	EE	Digitally Enhanced High Efficiency, Fast Settling Augmented DCDC Converters	Bakkaloglu, Bertan	Arizona State University
24	2810.043	FA	Analog Optimization Hybridizing Designer's Intent and Machine Learning	Li, Peng	UC/Santa Barbara
25	2810.044	FA	Hierarchical Characterization and Calibration of RF/Analog Circuits Using Lightweight Built-in Sensors	Ozev, Sule	Arizona State University
26	2810.046	SS	Generating Current Constraints for Electromigration Safety	Najm, Farid	University of Toronto

	Task	Thrust	Title	Task Leader	Institution
27	2810.047	SS	Architecture and DfT methods for improving life time reliability and functional safety of electronic circuits and systems out of application context	Chen, Degang	Iowa State University
28	2810.048	SS	Characterization and Mitigation of Electromigration Effects in Advanced Technology Nodes	Kim, Chris	U. of Minnesota
29	2810.049	EE	1-W Battery-Charging CMOS Buck Regulator	Rincón-Mora, Gabriel	Georgia Tech.
30	2810.050	SS	Integrating Metasurfaces and MEMS for Gas Sensing	Gómez-Díaz, Sebastian	UC Davis
31	2810.051	SS/EE	High Gain DC-DC Converter for EV Traction System	Ayyanar, Raja	Arizona State University
32	2810.052	FA	TI PLM as Hologram Generator for HUD (Head Up Display) and AR	Blanche, Pierre Kaneda, Yushi	University of Arizona
33	2810.053	FA	TI PLM to Advanced Lidar and Display Systems	Takashima, Yuzuru	University of Arizona
34	2810.054	SS	Reconfigurable AC Power Cycling Setup and Plug-in Condition Monitoring Tools for High Power IGBT and SiC Modules	Akin, Bilal	UT/Dallas
35	2810.055	SS/EE	EMI-Regulated Secure Automotive Power ICs	Ma, D. Brian	UT/Dallas
36	2810.056	FA	Millimeter Wave Packaging Research - Antenna in Package	Henderson, Rashaunda Lee, Mark Lu, Hongbing Lu	UT/Dallas
37	2810.057	SS	Reliability Study of E-mode GaN HEMT Devices by AC TDDB and High Resolution TEM	Kim, Moon Shichijo, Hishashi	UT/Dallas
38	2810.058	SS/FA	Machine Learning-Based Overkill/Underkill Reduction in Analog/RF IC Testing	Makris, Yiorgos	UT/Dallas
39	2810.059	SS/EE	Ultra-Low-Power Robust SAR ADC for PMCW Automotive RADAR	Chiu, Yun	UT/Dallas
40	2810.060	FA	Intelligent, Learning ADCs for the Post Figure-of-Merit World	Flynn, Michael	U. of Michigan

	Task	Thrust	Title	Task Leader	Institution
41	2810.061	EE	Two-Stage Vertical Power Delivery and Management for Efficient High-Performance Computing	Le, Hanh-Phuc Mercier, Patrick	UC/San Diego
42	2810.062	FA	Multi-Carrier DAC-Based Transmitter Architectures for 100+Gb/s Serial Links	Palermo, Samuel Hoyos, Sebastian	TEES
43	2810.063	FA	Analog and Digital Assist Techniques to Improve Mixed-Signal Performance	Sylvester, Dennis Blaauw, David	U. of Michigan
44	2810.064	SS	Characterization and Tolerance of Ageing in Integrated Voltage Regulators	Mukhopadhyay, Saibal	Georgia Tech
45	2810.065	EE/SS	Power-Efficient and Reliable 48-V DC-DC Converter with Direct Signal-to-Feature Extraction and DNN-Assisted Multi-Input Multiple-Output Feedback Control	Seok, Mingoo	Columbia University
46	2810.066	SS	Demonstrably Generalizable Compact Models of ESD Devices	Rosenbaum, Elyse	UIUC
47	2810.067	EE	Highly Efficient Extreme-Conversion-Ratio Buck Hybrid Converters	Pande, Partha Heo, Deukhyoun Doppa, Janardhan Rao	Washington State University
48	2810.068	EE	Active EMI Filtering with Switch-Mode Amplifier for High Efficiency	Hanson, Alex	UT Austin
49	2810.069	EE	A High-Mm-Wave-Yet-Wideband Linear Efficient Doherty Power Amplifier with Complex Device Neutralization, Multi-Drive Device Stacking, and Continuous-Mode Coupler-Based Doherty Load	Wang, Hua	Georgia Tech
50	2810.070	SS	Early and Late Life Failure Prediction Methods for Analog and Mixed-Signal Circuits	Kim, Chris	U. of Minnesota
51	2810.071	FA	Accurate Compact Temperature Sensors for Thermal Management of High Performance Computing Platforms	Geiger, Randall Chen, Degang	Iowa State University
52	2810.072	EE	AI/ML Edge Hardware for Ultra-reliable Wireless Networks	Allstot, David	Oregon State University
53	2810.073	EE	AI/ML Edge Hardware for Ultra-reliable Wireless Networks	Makris, Yiorgos	UT/Dallas
54	2810.074	SS	Thermal Performance Characterization and Degradation Monitoring of LDMOS based Integrated Power IC with On-Die Temperature Sensors	Akin, Bilal	UT/Dallas

	Task	Thrust	Title	Task Leader	Institution
55	2810.075	EE	Hybrid Step-Down DC-DC Converters with Large Conversion Ratios for 48V Automotive Applications	Lee, Hoi Liu, Jin	UT/Dallas
56	2810.076	FA	High Precision Positioning Techniques Based on Multiple Technologies and Frequency Bands	Al-Dhahir, Naofal Torlak, Murat	UT/Dallas
57	2810.077	SS	Increasing Lifetime of Nano-Scale CMOS Circuits	O, Kenneth	UT/Dallas
58	2810.078	EE	Programmable Mixed-Signal Accelerator for DNNs with Depthwise Separable Convolution Layers	Murmann, Boris	Stanford University
59	2810.079	EE	High-Power-Density In-Package SIMO Converters for Next-Generation Microprocessors	Huang, Cheng	Iowa State U.
60	2810.080	EE	Efficient and High-Density Fully In-Package GaN-Based High-Ratio DC-DC Converters	Huang, Cheng	Iowa State U.
61	2810.081	FA	Development of 70-95 GHz Terabit Beamformer	Wang, Huei	National Taiwan U.
62	2810.082	FA	Adaptive Digital Cancellation of Dynamic Error from Clock Skew, Component Mismatches, and ISI in High-Resolution RF DACs	Galton, Ian	UC/San Diego
63	2810.083	FA	Automated Layout of Analog Arrays in Advanced Technology Nodes	Sapatnekar, Sachin	U of Minnesota
64	2810.084	SS	Soft and hard analog fault detection, injection, coverage, diagnosis, and localization strategies suitable for production test and in-field test	Chen, Degang	Iowa State U.
65	2810.085	FA	Applications of Circuit Transient Sensitivity Simulation to Semiconductor Circuit Analysis and Design	Rohrer, Ronald	SMU
66	2810.086	SS	Machine Learning-based Functional Safety Improvement of AMS components in Automotive SoCs	Basu, Kanad	UT/Dallas
67	2810.087	EE	Grid Optimization and Silicon Validation for Chip Robustness	Najm, Farid	U. of Toronto
68	2810.088	EE	Grid Optimization and Silicon Validation for Chip Robustness	Kim, Chris	U of Minnesota

	Task	Thrust	Title	Task Leader	Institution
69	2810.089	SS	Techniques for Low-cost Design, Test, and Calibration of RF MIMO Systems	Ozev, Sule	Arizona State
70	2810.090	SS	Motor Health Monitoring	Akin, Bilal	UT/Dallas

Table 2: Funded research projects at TxACE by SRC task identification number (FA: Fundamental Analog, EE: Energy Efficiency, SS: Safety, Security and Health Care)

ACCOMPLISHMENTS

In the past year, TxACE has made significant research progress. Table 3 summarizes the number of publications and inventions resulting from the TxACE research during May 2021 to April 2022, while Table 4 lists the major research accomplishments for the Center during the period. The TxACE researchers have published 45 conference papers and 17 journal papers. The team also made 4 invention disclosure and filed 8 patent applications. The list of publications is included as Appendix I. Following the tabulation, brief summaries of each project are provided.

Table 3. TxACE number of publications (May 2021 through April 2022)

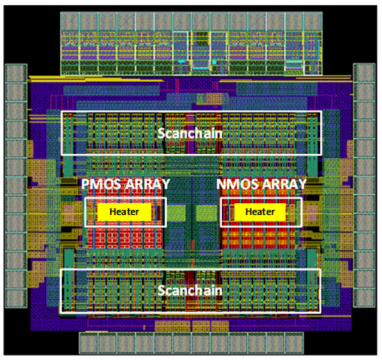
Conference Papers	Journal Papers	Invention Disclosures	Patents Filed	Patents Granted
45	17	4	8	0

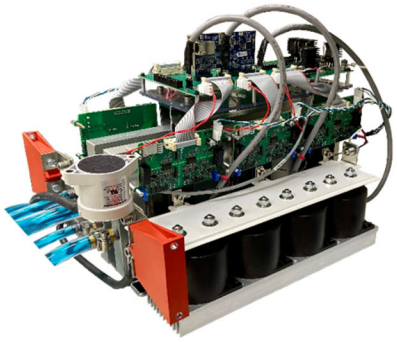
Table 4. Major TxACE Research Accomplishments (May 2021 through April 2022)

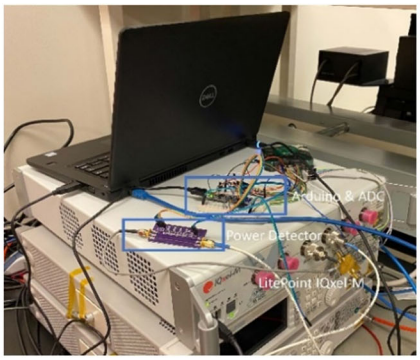
Category	Accomplishment
Energy Efficiency (Circuits)	A 2.5–5MHz 87% peak-efficiency 48V-to-1V integrated hybrid DC-DC converter adopting a switched capacitor network with capacitor assisted dual inductor filtering has been demonstrated. The converter using a fully on-chip power NMOS is the first to achieve 48V-to-1V direct conversion with competitive power efficiencies with switching frequency in the MHz range. (2810.075, H. Lee and J. Liu, UT Dallas)
Energy Efficiency (Circuits)	Computational control is used to guide the run-time optimization of low-power duty-cycled systems which are typically used in IoT and wearable applications. The principle of optimal "regenerative breaking" is utilized to return stored domain charge into the battery instead of allowing it to leak away. The proposed technique in a 65-nm CMOS prototype improves the *overall* system efficiency by ~2X, in duty-cycled domains that perform approximately 5k computations during active mode. (2810.035, V. Sathe, University of Washington, Seattle)
Energy Efficiency (Circuits)	A fully digital in-memory computing chip (DIMC) achieving 2219 TOPS/W is demonstrated. Full digital implementation mitigates the PVT variation issue. Approximate arithmetic hardware is utilized to improve area and power efficiency. Additionally, approximation-aware training and custom data format are utilized to minimize inference accuracy degradation due to approximation. (2810.34, M. Seok, Columbia University)
Energy Efficiency (Circuits)	A 150-kHz Active EMI Filter (AEF) using a GaN-based switch-mode amplifier for high efficiency with the input voltage, V_s=120V, the output voltage, V_o=400V and P_o=320W is demonstrated. The total volume of the proposed AEF is 0.1in^3 which is equal to 1/32 of the volume of the size-optimized LC filter for the similar current attenuation of ~65 dB. Furthermore, the power consumption is only 0.23W. This AEF with a smaller size and higher efficiency is a promising solution to replace the conventional passive LC filter and linear-mode AEF. (2810.68, A. Hanson, UT Austin)

Fundamental Analog (Circuits)	Wideband low noise amplifiers (LNAs) operating in the 170-260 GHz band are developed for future high-speed wireless communication links and imaging radars. Fabricated in a commercial 130-nm SiGe BiCMOS process, the LNA achieves a peak measured gain of 15.5 dB at 207 GHz, 3-dB bandwidth spanning the WR5 frequency range of 140-220 GHz (fractional bandwidth of 44%), a measured noise figure of 6.9 dB, 6.1 dB, and 8.2 dB at 150 GHz, 180 GHz, and 210 GHz, respectively. (2810.029, A. Babakhani, UCLA)
Fundamental Analog (Circuits)	A pulsed-injection driver and a delta-sigma dithered load capacitor is developed to lower power consumption and perform temperature compensation of crystal oscillators (XO), respectively. Implemented in 40-nm CMOS, the 32.768-kHz temperature-compensated XO (TCXO) achieves an accuracy of ±4.2 ppm over a −20 °C to 85 °C temperature range with three-point trimming and an Allan deviation floor of 34 ppb while consuming 43 nW, an 8× improvement over the state-of-the-art TCXOs. (2810.063, D. Sylvester, U. Michigan)
Safety, Security and Health Care (Circuits)	A method has been developed for reliable sub-threshold slope and V_t extraction at temperatures up to 200^{o}C, and the first ever map of measured temperature of a circuit area underneath an on-chip heater has been produced. The goal of this project is to understand the effects of extreme temperatures on variability and reliability of devices and circuits, through studies involving measurements from test chips with on-chip heaters and temperature sensors. (2810.038, C. Kim, U. Minnesota)
Safety, Security and Health Care (Systems)	Online fault diagnosis/failure prognosis tools to establish an early warning system for LDMOS integrated power IC have been developed and dominant aging mechanisms along with potential precursors (i.e., drain current) have been identified. This project investigates static & dynamic degradation and thermal performance of LDMOS using on-die temperature sensors under high voltage, high current, and high junction temperature condition to improve reliability of the warning system. (2810.054, B. Akin, UT Dallas)

Safety, Security and Health Care Thrust







Category	Accomplishment
Safety, Security and Health Care (Circuits)	A method has been developed for reliable sub-threshold slope and V_t extraction at temperatures up to 200°C, and the first ever map of measured temperature of a circuit area underneath an on-chip heater has been produced. The goal of this project is to understand the effects of extreme temperatures on variability and reliability of devices and circuits, through studies involving measurements from test chips with on-chip heaters and temperature sensors. (2810.038, C. Kim, U. Minnesota)
Safety, Security and Health Care (Systems)	Online fault diagnosis/failure prognosis tools to establish an early warning system for LDMOS integrated power IC have been developed and dominant aging mechanisms along with potential precursors (i.e., drain current) have been identified. This project investigates static & dynamic degradation and thermal performance of LDMOS using on-die temperature sensors under high voltage, high current, and high junction temperature condition to improve reliability of the warning system. (2810.054, B. Akin, UT Dallas)

TASK 2712.029, NOVEL SUPER-RESOLUTION AND MIMO TECHNIQUES FOR AUTOMOTIVE AND EMERGING RADAR APPLICATIONS

MURAT TORLAK, UNIVERSITY OF TEXAS AT DALLAS, TORLAK@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

Millimeter wave (mmWave) radar sensors provide contactless and highly accurate detection of motion and vital signs. We constructed a new lens-enabled multiple-input multiple-output (MIMO) system for vital signal detection. This report presents empirical results on vital signs detection algorithms and preliminary results on sleep monitoring with these sensors.

TECHNICAL APPROACH

We introduce a strategy to estimate vital signs (respiration and heart rates). In particular, talking and intermittent head movements complicate the heart rate detection problem. Our proposed method improves heart rate detection even during instances of small-scale motions. Additionally, we have conducted preliminary tests to understand the feasibility of mmWave radars for contactless sleep monitoring. This includes utilizing radar sensors' localizing sleep features in range, angle, and doppler domains to detect entry-exit times to bed and extracting Doppler features that can later be used in sleep stage classification. Preliminary tests were conducted using moving objects to emulate human sleep behavior.

SUMMARY OF RESULTS

There are two major issues in non-contact vital signs detection. The first is recognizing returns from a human subject and avoiding returns from static clutter in the environment. Such returns might cause attempts to detect vital signs within a spectral location where there are none. Two blocks, the Static Clutter Suppression, and Optimal Bins Selection block are placed to counteract this issue. The second issue is the spectral dominance of the respiration signal over the heart rate signal. This occurs because the displacement of the human body due to breathing is approximately an order of magnitude greater than the displacements due to the heart rate. The respiration rate and heart rate are also not perfect sinusoids, which results in their harmonics and intermodulation products appearing as artifacts in the extracted Doppler spectrum. As a result, there are checks placed in the algorithm to counter the impact of such artifacts. These checks are searching for heart rate values across multiple physical locations since the strength of artifacts is different at different locations. This is done by utilizing receive beamforming. The Generate Pseudo Spectrum, Respiration Artifact Correction, and Heart Rate Artifact Correction blocks in the algorithm help relieve the issues of erroneous artifacts. The Pseudo Spectrum is generated by counting the number of occurrences of a heart rate estimate at different range and angle locations. The Harmonic Product Spectrum algorithm is used to check for heart rate artifacts and find the correct fundamental frequency of heart rate.

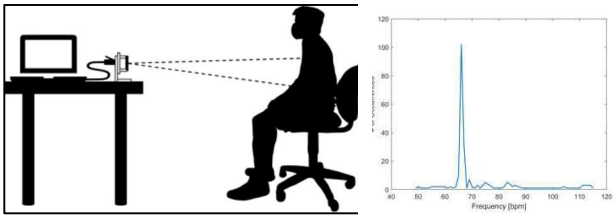


Figure 1. Left: Measurement setup with a mmWave radar. Right: Heart rate pseudo-spectrum (beats/min) demonstrating the heart rate extraction.

Two cases are analyzed for extracting the vital signs of a human subject. The first is a subject sitting in the boresight of the radar sensor at approximately 1-m away. This setup is shown in Fig. 1 (left). The second one is where the subject sits at around 4-m away and is not in the boresight of the sensor.

The problem with understanding sleep is the lack of reliable longitudinal data. The researchers have devised methods to detect when we fall asleep, wake up, and classify sleep stages in between. The gold-standard used in sleep medicine is Polysomnography (PSG). However, PSG requires subjects to visit sleep clinics which is costly and inconvenient. In this research, we investigated the ability of the mmWave radar sensor in detecting the presence of moving objects in a confined space and then track the frequency of oscillation of non-stationary signals across time. These form the backbone of sleep monitoring using radars, utilizing both the advantages of actigraphy and autonomic signal-based sleep monitoring approaches.

Keywords: mmWave, radar, vital sign monitoring, sleep monitoring

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] A. B. Baral and M. Torlak, "Joint Doppler Frequency and Direction of Arrival Estimation for TDM MIMO Automotive Radars," *IEEE Journal of Selected Topics in Signal Processing*, vol. 15, no. 4, pp. 980-995, June 2021.

TASK 2810.021, A COLLABORATIVE MACHINE LEARNING APPROACH TO FAST AND HIGH-FIDELITY DESIGN PREDICTION

JIANG HU, TEXAS A&M UNIVERSITY, JIANGHU@TAMU.EDU
YIRAN CHEN, DUKE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

This work proposes the first runtime on-chip power meter (OPM) that achieves a per-cycle temporal resolution in power prediction and < 1% area/power overhead without compromising accuracy, which is validated on high-performance, out-of-order industrial CPU designs. These unique features open up new applications in design and runtime power management beyond the capability of the prior art.

TECHNICAL APPROACH

We adopt a minimax concave penalty (MCP)-based feature selection algorithm to automatically select less than 0.05% of RTL signals in any given design as model inputs. The power model is integrated with an emulator-assisted flow to perform power estimations on millions-of-cycles benchmark for million-gate CPUs. Furthermore, the power model is synthesized and integrated into the microprocessor implementation as a runtime OPM.

SUMMARY OF RESULTS

Our work APOLLO is a unified RTL-level power modeling framework addressing both the design-time and runtime challenges within a consistent model structure, as shown in Figure 1. The centerpiece of it is a new power proxy selection technique based on minimax concave penalty (MCP) regression. It enables per-cycle power tracing for benchmarks executing over millions of CPU cycles. To the best of our knowledge, APOLLO is the first power monitoring technique with cycle accuracy and sub-1% area overhead. Moreover, the power proxy selection process in APOLLO is fully automated and thereby easily extensible to new designs and architectures.

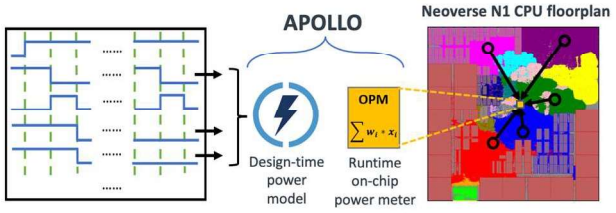


Figure 1. APOLLO provides a design-time power simulator and a runtime on-chip power meter (OPM) based on a consistent model. Neoverse™ N1 incorporating an OPM.

An APOLLO model with Q = 159 power proxies as input feature obtains NRMSE = 9.4% and R^2 = 0.95. Figure 2 illustrates prediction and label as power traces on the 15,000-cycle testing dataset, covering 12 handcrafted micro-benchmarks. The prediction overlaps well with the ground truth for distinctive patterns from different benchmarks.

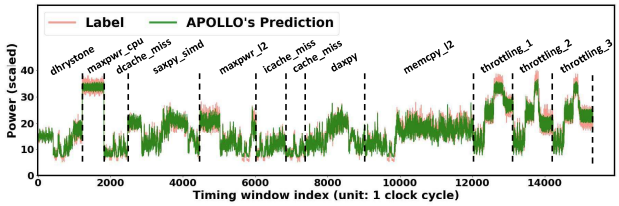


Figure 2. Evaluation of an APOLLO model with Q = 159.

Figure 3(a) shows the distributions of the power proxies selected from the CPU. There are 39 gated clock signals, which means APOLLO captures the major contributor, i.e., clock network, of the dynamic power consumption. The weights of the gated clock signals provide useful insights into the power-hungry clock gating structure. Figure 3(b) explores the area and accuracy trade-off in OPM design by varying the number of selected proxies Q and the number of bits B used for weight quantization. For an OPM with B = 10 and Q = 159, its total gate area is only 0.2% of the gate area of Neoverse N1. It has a latency of 2 cycles.

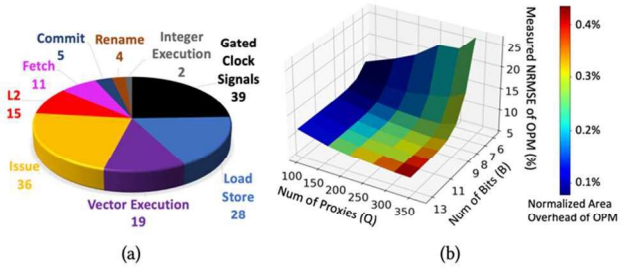


Figure 3. (a) Distribution of extracted power proxies. (b) Trade-off between the area overhead and accuracy of the OPM.

Keywords: power modeling, machine learning, voltage droop, commercial microprocessor, on-chip power meter

INDUSTRY INTERACTIONS

IBM, NXP, ARM

MAJOR PAPERS/PATENTS

[1] Zhiyao Xie, Xiaoqing Xu, Matt Walker, Joshua Knebel, Kumaraguru Palaniswamy, Nicolas Hebert, Jiang Hu, Huanrui Yang, Yiran Chen, Shidhartha Das, "APOLLO: An Automated Power Modeling Framework for Runtime Power Introspection in High-Volume Commercial Microprocessors." In *International Symposium on Microarchitecture (MICRO)*, 2021. **Best Paper Award.**

TASK 2810.022, A COLLABORATIVE MACHINE LEARNING APPROACH TO FAST AND HIGH-FIDELITY DESIGN PREDICTION

YIRAN CHEN, DUKE UNIVERSITY, YIRAN.CHEN@DUKE.EDU
JIANG HU, TEXAS A&M UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

This work proposes the first runtime on-chip power meter (OPM) that achieves a per-cycle temporal resolution for power prediction and < 1% area/power overhead without compromising accuracy. This is validated on high-performance, out-of-order industrial CPU designs. These unique features open up new applications in design and runtime power management.

TECHNICAL APPROACH

We adopt a minimax concave penalty (MCP)-based feature selection algorithm to automatically select less than 0.05% of RTL signals in any given design as model inputs. The power model is integrated with an emulator-assisted flow to perform power estimations on millions-of-cycles benchmark for million-gate CPUs. Furthermore, the power model is synthesized and integrated into the microprocessor implementation as a runtime OPM.

SUMMARY OF RESULTS

Our work APOLLO is a unified RTL-level power modeling framework addressing both the design-time and runtime challenges within a consistent model structure, as shown in Figure 1. The centerpiece of it is a new power proxy selection technique based on minimax concave penalty (MCP) regression. It enables per-cycle power tracing for benchmarks executing over millions of CPU cycles. To the best of our knowledge, APOLLO is the first power monitoring technique with cycle accuracy and sub-1% area overhead. Moreover, the power proxy selection process in APOLLO is fully automated and thereby easily adapted to new designs and architectures.

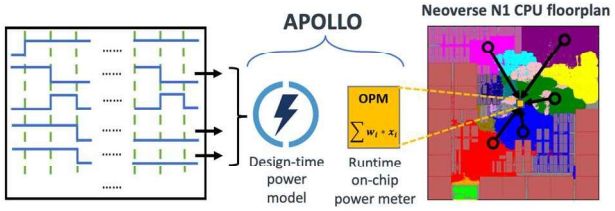


Figure 1. APOLLO provides a design-time power simulator and a runtime on-chip power meter (OPM) based on a consistent model. As an example, APOLLO has been used with a Neoverse™ N1 CPU.

An APOLLO model with Q = 159 power proxies as input features obtains NRMSE = 9.4% and R^2 = 0.95. Figure 2 illustrates prediction and label as power traces on the 15,000-cycle testing dataset, covering 12 handcrafted micro-benchmarks. The prediction overlaps well with distinctive patterns of the ground truth from different benchmarks.

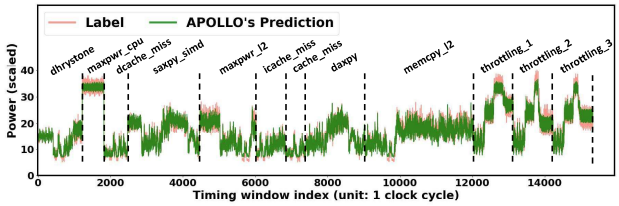


Figure 2. Evaluation of an APOLLO model with Q = 159.

Figure 3(a) shows the distributions of the power proxies selected from the CPU. There are 39 gated clock signals, which means APOLLO captures the major contributor, i.e., clock network, of the dynamic power consumption. The weights of the gated clock signals provide useful insights into the power-hungry clock gating structure. Figure 3(b) explores the area and accuracy trade-off in OPM design by varying the number of selected proxies Q and the number of bits B used for weight quantization. For an OPM with B = 10 and Q = 159, its total gate area is only 0.2% of the gate area of Neoverse N1. It has a latency of 2 cycles.

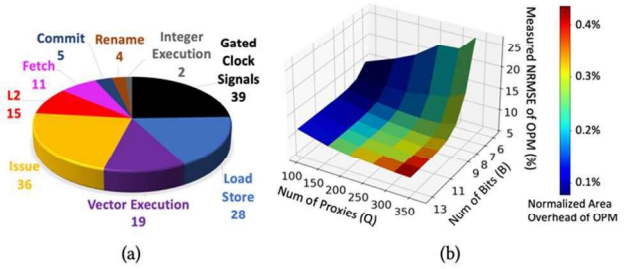


Figure 3. (a) Distribution of extracted power proxies. (b) Trade-off between the area overhead and accuracy of the OPM.

Keywords: power modeling, machine learning, voltage droop, commercial microprocessor, on-chip power meter

INDUSTRY INTERACTIONS

IBM, NXP, ARM

MAJOR PAPERS/PATENTS

[1] Zhiyao Xie, Xiaoqing Xu, Matt Walker, Joshua Knebel, Kumaraguru Palaniswamy, Nicolas Hebert, Jiang Hu, Huanrui Yang, Yiran Chen, Shidhartha Das, "APOLLO: An Automated Power Modeling Framework for Runtime Power Introspection in High-Volume Commercial Microprocessors." In *International Symposium on Microarchitecture (MICRO)*, 2021. **Best Paper Award.**

TASK 2810.023, MACHINE LEARNING DRIVEN AUTOMATIC MIXED-SIGNAL DESIGN VERIFICATION-VALIDATION FOR AUTOMOTIVE APPLICATIONS

ABIHIJIT CHATTERJEE, GEORGIA INSTITUTE OF TECHNOLOGY,
ABHIJIT.CHATTERJEE@ECE.GATECH.EDU

SIGNIFICANCE AND OBJECTIVES

The research will develop the next generation of pre- and post-silicon design model extraction and validation tools that will allow complex mixed-signal systems to be tested and debugged automatically and orders of magnitude more efficiently (speed, accuracy) than current techniques while providing diagnosis down to the physical level for quick design fixes.

TECHNICAL APPROACH

The proposed approach involves developing a frequency-based stimulus generation algorithm that exposes discrepancies between high-level AMS circuits and their silicon implementations. Such discrepancies occur because of design bugs in circuit modules. To diagnose, we perform multiple bug emulation experiments (BEEs). Kernels are placed across modules in the high-level model to replicate the buggy response. An error response clustering algorithm is then used to guide successive BEEs. The algorithm converges when minimum residual error across BEEs conducted cannot be reduced. The modules for that BEE are likely buggy modules. Results on multiple designs prove the viability of the proposed approach.

SUMMARY OF RESULTS

The key focus of this research is on post-silicon bug diagnosis: identifying circuit modules with buggy behaviors. Buggy module behaviors are defined as input-output transformations in hardware that are different from those predicted by pre-silicon simulation models by larger than a calibrated threshold. There may be multiple bugs in a module and multiple circuit modules may be buggy. Specific contributions are as follows: a novel frequency domain diagnostic test stimulus generation algorithm is developed that allows exposure of multiple design bugs using iterative bug behavior learning iterations. Therefore, multiple types of bug effects within each circuit module and across different modules are exposed by the test suite. This is particularly important for correct (multiple) bug diagnosis.

The use of a diverse set of design bug emulation experiments is proposed. Since there is limited observability in silicon, these experiments are performed on simulation models of the circuit to recreate the bug effects as observed on the circuit outputs in silicon by concurrently emulating the outputs of multiple circuit modules using dedicated machine learning kernels as opposed to sequential correction. We propose the use of a Gaussian Mixture Model (GMM) driven clustering to analyze data generated and used to guide the selection of future BEEs to arrive at a final diagnosis. An overview of the test generation algorithm and the selected diagnosis results on PLL and RF receivers is shown in Figure 1 and Figure 2, respectively.

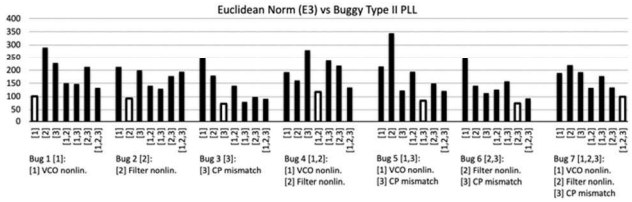


Figure 1. Diagnosis of seven different buggy PLLs with exhaustive BEEs

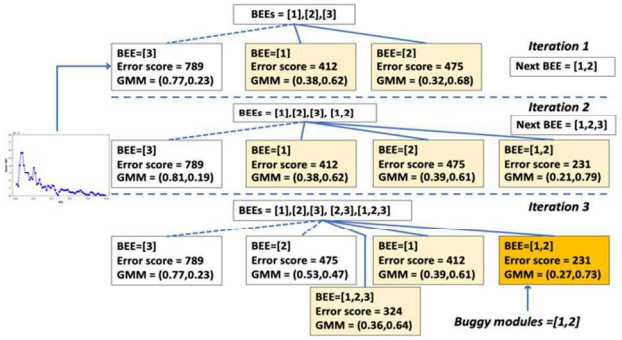


Figure 2. GMM-Guided diagnosis on a buggy receiver

Keywords: Analog/RF design validation, test generation, machine learning

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] J. Lei and A. Chatterjee, "ML-Assisted Bug Emulation Experiments for Post-Silicon Multi-Debug of AMS Circuits," ITC 2022

TASK 2810.025, MACHINE LEARNING-BASED LAYOUT ANALYSIS AND NETLIST OPTIMIZATION FOR DEFECT TOLERANCE AND DESIGN ROBUSTNESS TO PROCESS IMPERFECTIONS AND VARIATIONS

YIORGOS MAKRIS, UNIVERSITY OF TEXAS AT DALLAS, YIORGOS.MAKRIS@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

This task concentrates on improving yield and design robustness by presenting two parallel methods (i) detecting layout hotspots using improved Design Space Exploration (DSE) and (ii) synthesizing defect-tolerant structural netlists using enhanced library databases.

TECHNICAL APPROACH

We evaluate different feature extraction methods for detecting layout hotspots and train two machine learning algorithms (SVM and Decision Trees) to minimize the false negative rates during hotspot detection. In addition to this, we develop methodologies to enhance design synthesis by introducing defect tolerance metrics to library cells that use intelligence to guide synthesis toward generating robust structural netlists that can withstand delay variations and timing defects. We create "defect-aware" libraries that represents the defect-tolerance as delay penalties, thereby, biasing synthesis tool to pick robust cells for the critical paths of the design.

SUMMARY OF RESULTS

ML-based layout analysis: Using ICCAD '19 benchmarks for hotspot detection, we analyzed the effectiveness of 3 feature extraction methods to improve the accuracy of identifying hotspots. We also introduced feature specific weights to enable better convergence of the trained algorithms. The results of the 3 methods, a) density transform, b) co-ordinate transform, and c) fragment transform along with their weighted algorithmic versions are investigated. The results are tabulated in Table 1. We observed that adding weights to extracted features during training improves the results regardless of the feature extraction transformation. Fragment-based methods were performing better than density-based methods.

Defect-Aware netlist optimization: Fig. 1 shows the defect-aware synthesis flow where a benchmark RTL was synthesized using the original and the defect-aware (containing cell defectivity information from delay characterization) library databases, and the two functionally equivalent-structurally different netlists are compared for their defect tolerance using STA analysis.

Table 1. Feature Extraction Results for Hotspot Detection

FE method	Hotspots	Non-Hotspots	False Positives	False Negatives	Error
Density w/o weights	89.965 %	96.890 %	3.043 %	0.343 %	3.236 %
Density w weights	91.175 %	97.164 %	2.821 %	0.247 %	3.056 %
Co-ordinate w/o weights	89.472 %	97.059 %	2.878 %	0.223 %	3.101 %
Co-ordinate w weights	91.542 %	96.679 %	3.259 %	0.155 %	3.314 %
Fragment w/o weights	89.716 %	96.971 %	3.178 %	0.256 %	3.199 %
Fragment w weights	92.125 %	97.068 %	3.178 %	0.232 %	3.391 %

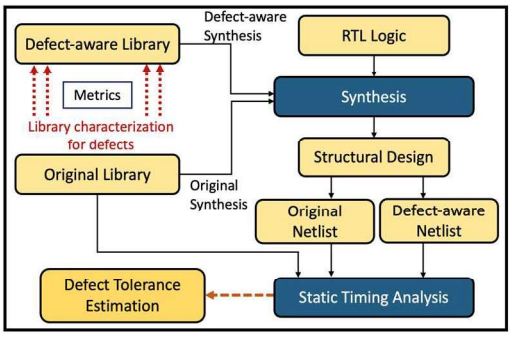


Figure 1. Defect Tolerant Design Overview

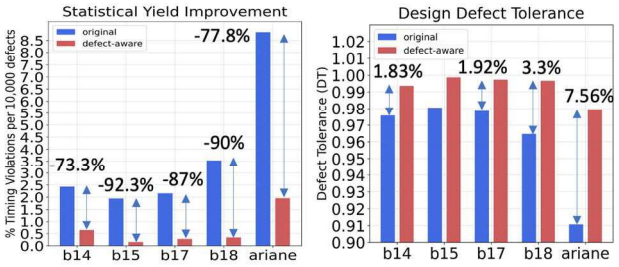


Figure 2. Defect Tolerance Improvement by Biasing Synthesis

For the 5 benchmark circuits shown in Fig. 2, we were able to achieve ~84% reduction in timing violations with ~4% improvement in design defect tolerance. Overhead of ~0.6% area and ~3% power with no performance impact.

Keywords: Defect-Tolerance, Yield, "Defect-Aware" Cell Libraries

INDUSTRY INTERACTIONS

Intel Corp.

MAJOR PAPERS/PATENTS

[1] S.S. Thiagarajan, S. Natarajan, Y. Makris, "A Defect Tolerance Framework for Improving Yield", DAC, 2022.

TASK 2810.027, MEASUREMENT AND MODELING OF STRESS/STRAIN ON ANALOG TRANSISTOR AND CIRCUIT PARAMETERS

SCOTT THOMPSON, UNIVERSITY OF FLORIDA, THOMPSON@ECE.UFL.EDU

SIGNIFICANCE AND OBJECTIVES

Packaging of electronic devices introduces compressive biaxial stress and variable vertical stress due to silicon particles in the epoxy. We show that due to the non-linear nature of the intrinsic carrier concentration, compressive biaxial stress (a common type in most commercial packages) is disadvantageous to bipolar device variability. Significantly improved matching could be obtained if transistors were packaged with tensile stress. PNP transistors are also shown to be less affected by packaging stress.

TECHNICAL APPROACH

The BJT matching due to packaging stress is modeled using device simulation. The BJT shift for analog transistors will be measured using a 4-point bending flexure wafer bending jig. Measurements and modeling are compared.

SUMMARY OF RESULTS

The goal is to develop a detailed understanding of packaging stress that results in voltage offset for a typical differential amplifier circuit (see Fig. 1).

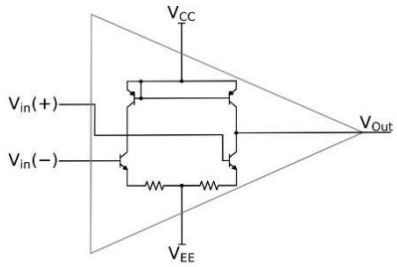


Figure 1. Example matching circuit.

Using wafer bending and simulations we show collector current due to stress can be approximated by a summation due to the change in intrinsic carrier concentration and mobility:

$$I_s = \frac{k_B T}{q}\frac{A}{W}\sigma^{Minority} = \frac{k_B T}{q}\frac{A}{W} * \frac{q}{N_{Majority}} n_i^2 \mu \quad (1)$$

$$\frac{\Delta I_c}{I_c} = \frac{\Delta I_s}{I_s} = \frac{\Delta(n_i^2\mu)}{n_i^2\mu} \approx \frac{\Delta\mu}{\mu} + \frac{\Delta n_i^2}{n_i^2} \quad (2)$$

We show that PNP (vs NPN) transistors are less sensitive to packaging stress. NPN and transistors with built-in global packaging compressive stress are more sensitive to silica filler particle stress. Transistors are less sensitive to package stress at room versus elevated temperature and high injection. Key data to support these are shown in Figs. 2-4.

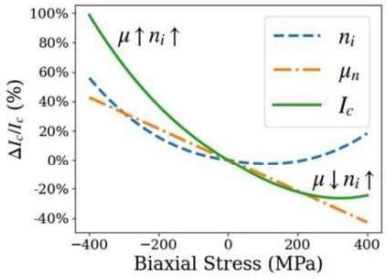


Figure 2. Change in collector current vs package stress.

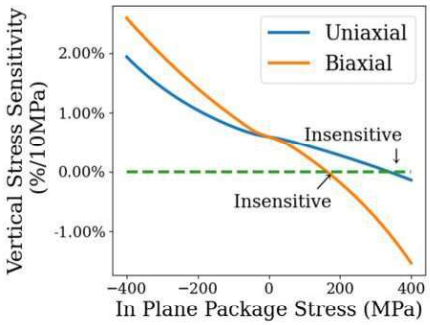


Figure 3. Built-in stress sensitivity versus package stress.

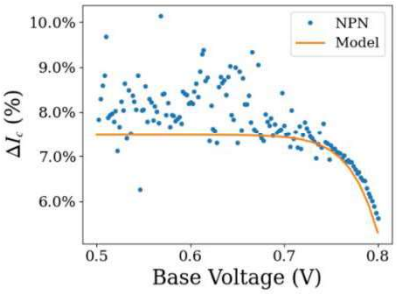


Figure 4. Change in I_C due to stress vs injection level.

Keywords: strained silicon, BJT matching, packaging stress

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] T. A. Weingartner, C. -H. Kuo, A. Thomas, S. E. Thompson and M. E. Law, "Negative Impact of Compressive Biaxial Stress on High Precision Bipolar Devices," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 11, no. 8, pp. 1310-1312, Aug. 2021, doi: 10.1109/TCPMT.2021.3095670.

TASK 2810.038, EXTREME TEMPERATURE DIGITAL, ANALOG, AND MIXED-SIGNAL CIRCUITS (ET-DAMS)

CHRIS H. KIM, UNIVERSITY OF MINNESOTA, CHRISKIM@UMN.EDU

SIGNIFICANCE AND OBJECTIVES

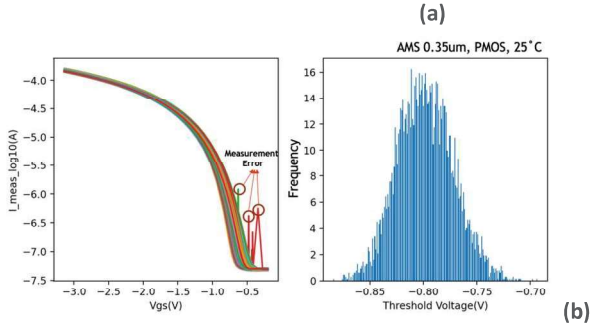
We have been focusing on the testing of the array-based, densely populated transistor characterization circuit in a 0.35-µm process that was taped out last year. Using the on-chip heater and M1 metal-based temperature sensor, we were able to collect statistical IV curve data from a large number of devices at temperatures over 200 °C.

TECHNICAL APPROACH

Testing software was developed for an array-based transistor characterization circuit to efficiently characterize transistor I-V behavior under extreme temperatures (i.e. >200°C). We have implemented a metal-based, small-sized on-chip heater to help us reach the target temperature using joule heating. In the past year, we successfully measured the I-V curves from 12,000+ PMOS and NMOS devices while the on-chip heater was controlled using an automatic temperature feedback loop. Additionally, we were able to measure for the first time the spatial temperature distribution of the transistor array over the entire heater area.

SUMMARY OF RESULTS

Figs. 1(a)-(d) show some of the test data we collected in 2022. The first figure shows the full chip layout of the 350-nm test chip we taped out last year showing the PMOS and NMOS array, a scan chain for addressing the devices, and peripheral circuits. Fig. 1(b) shows the I-V curve traces and the extracted threshold voltage of each device using a constant current V_t definition.



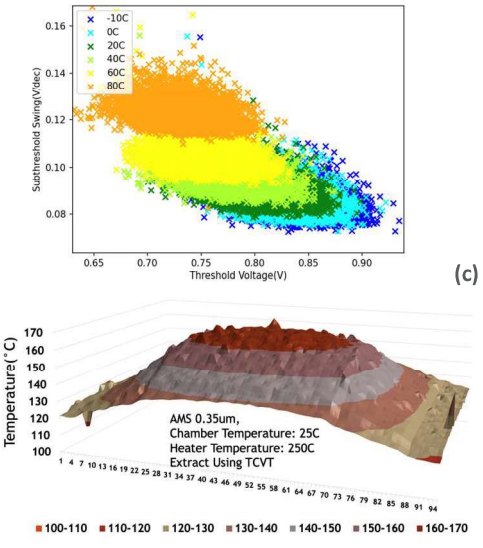


Figure 1. (a) Full chip layout of 350-nm device characterization array. (b) I-V curves and extracted threshold voltage from 6k+ PMOS devices. (c) Subthreshold swing and threshold voltage distributions at different measurement temperatures. (d) Device-under-test temperature underneath the heater showing spatial gradient.

The measurements and data analyses were fully automated with no manual intervention. The V_t distribution shows a Gaussian Bell curve with a sigma V_t of 50mV. Fig. 1(c) shows the sub-threshold slope and threshold voltage of individual devices measured at different temperatures showing the expected behavior for temperature sensitivity. Finally, Fig. 1(d) shows the measured temperature spatial map extracted from the individual I-V curves. As expected, the temperature peaks inside the on-chip heater region and quickly drops outside the heater.

Keywords: Device characterization array, on-chip heater, high-temperature operation, fully automated testing, spatial temperature gradient measurements

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] H. Yu, G. Park, and C.H. Kim, "Extreme Temperature Characterization of Amplifier Response Up to 300 Degrees Celsius Using Integrated Heaters and On-Chip Samplers", ESSCIRC, 2021.

TASK 2810.041, ESD PROTECTION FOR IO OPERATING AT 56 GB/S AND BEYOND

ELYSE ROSENBAUM, UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN, ELYSE@ILLINOIS.EDU

SIGNIFICANCE AND OBJECTIVES

The project objective is to develop a co-design methodology for ESD-protected high-speed receiver front-end circuits. This will enable a designer to achieve adequate component-level ESD protection while also meeting return loss specifications.

TECHNICAL APPROACH

A four-pronged technical approach has been developed. First, ESD hazards arising from a variety of bandwidth extension techniques are identified. The second step is to identify the V_{MAX} for each circuit topology under consideration, where V_{MAX} is the maximum tolerable voltage at the IO pin under ESD conditions. Third, the available protection devices are characterized using the metric I_{fail}/Capacitance and R_{on}·Capacitance. Finally, the performance and reliability of each candidate circuit are optimized through co-design. Much of the work is carried out using analysis and circuit simulation, but test chip fabrication and measurement will be used for proof of concept.

SUMMARY OF RESULTS

This work assumes CMOS technology and a conventional receiver architecture in which the first stage is a continuous time linear equalizer (CTLE). If a protection circuit shunts the ESD current away from the active circuit, the remaining threat to the active circuit is the higher-than-normal pad voltage. The pad voltage and thus the stress on the input transistor is largest for ESD events in which the current flows through the rail clamp circuit. The breakdown voltage of the input transistor can be maximized by optimally biasing the internal nodes of the front-end circuit. We developed bias control circuits for two different types of CTLE: (i) RC-degenerated differential amplifier topology (ACTLE) and (ii) inverter-based topology (ICTLE). The bias control circuits are activated by a signal from the rail clamp. CTLE test circuits were implemented in 55-nm CMOS. CTLE 1 does not include bias control, CTLE 2 includes bias control, and CTLE 3 includes bias control and uses smaller ESD protection devices than CTLEs 1 and 2. The expected performance of each is summarized in Table 1. The ESD simulation results contain some uncertainty because, in simulations, the node voltages are affected by I_{gate} but the PDK gate current model is not calibrated for the voltage range of interest.

Table 1. CTLE test circuits.

	ΔV_{stress} (V) @ 3 A CDM	ΔV_{stress} (V) @ 2 kV HBM	Return Loss (dB) @ 10 GHz
ACTLE 1	0 (Baseline)	0 (Baseline)	-8.99
ACTLE 2	-1.02	-0.35	-8.99
ACTLE 3	-0.84	-0.33	-10.45
ICTLE 1	0 (Baseline)	0.44	-9.36
ICTLE 2	-0.98	-0.78	-9.36
ICTLE 3	-0.75	-0.74	-12.46

We developed distributed ESD protection that utilizes the parasitic resistance of a bandwidth extension circuit based on a "tri-coil," a triply coupled inductor structure (Fig. 1), to reduce the gate voltage of input transistor of a wireline receiver. Three tri-coils with different secondary protection devices, D2, were implemented in 65-nm CMOS. A conventional T-coil is included for comparison. The inductors and coupling coefficients are optimized to maximize bandwidth and minimize return loss of tri-coil 1, while maintaining a small group delay variation. Tri-coils 2 and 3 are identical to tri-coil 1, except for the size of the D2 devices. The fabricated test structures will be evaluated by transmission line pulse (TLP) and S-parameter measurements. The expected results are listed in Table 2.

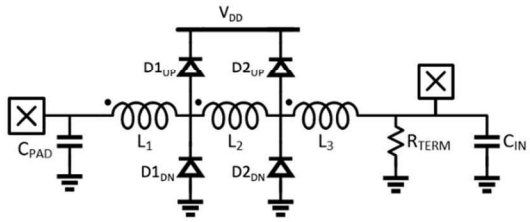


Figure 1. Tri-Coil and distributed ESD protection. C_{IN} represents the receiver input capacitance.

Table 2. Test structures and predicted performance.

Test Structure	D1 (μm)	D2 (μm)	BW (GHz)	RL (dB) @ 28 GHz	HBM	CDM
Tri-Coil 1	70	70	47	-7.3	2 kV	+++
Tri-Coil 2	70	46	50	-7.3	2 kV	++
Tri-Coil 3	70	23	36	-7.2	2 kV	++
T-Coil	140	-	46	-6.7	4 kV	+

Keywords: ESD, CDM, SerDes, bandwidth extension

INDUSTRY INTERACTIONS

Texas Instruments, NXP, AMD

MAJOR PAPERS/PATENTS

TASK 2810.046, GENERATING CURRENT CONSTRAINTS FOR ELECTROMIGRATION SAFETY

FARID N. NAJM, UNIVERSITY OF TORONTO, F.NAJM@UTORONTO.CA

SIGNIFICANCE AND OBJECTIVES

We focus on electromigration (EM) failures in the on-chip power grid and are developing tools to guarantee chip robustness in the face of EM degradation. Our goal is to provide techniques by which one can ensure EM reliability-by-design. The key advantage is improved accuracy and reduced conservatism.

TECHNICAL APPROACH

It is difficult to achieve EM sign-off on modern chip designs, due to the limitations of traditional empirical models that are built into existing tools. Modern physical EM models allow one to overcome these limitations, but are expensive to use, especially when doing EM simulation on large chip power grids. Instead of simulation, we will develop an "inverse approach": generate design-aware constraints on the circuit currents which, if guaranteed during chip design, would ensure EM safety for the desired lifetime. Since these constraints correspond to the specific design, this has the potential to improve accuracy and reduce pessimism.

SUMMARY OF RESULTS

Under previous tasks, using the Korhonen stress-based model for EM (1993), we developed a linear (LTI) system model that describes the time evolution of the stress vector as a function of line currents. We also used this to build a simulation engine for tracking the evolution of EM over time - the first practical *electromigration simulator*.

Last year, we discovered [1] that the relations between stress and flux in every interconnect tree metal line are identical to those between voltage and current in a specially designed electrical circuit (an RC network), as shown in Fig. 1. We call this an *equivalent circuit*, and it can be easily and automatically built for any given metal interconnect tree. If we solve the voltage-current problem for the equivalent circuit, then we have automatically solved the stress-flux problem for the interconnect tree. Node voltages in the equivalent circuit give the stresses in the metal network.

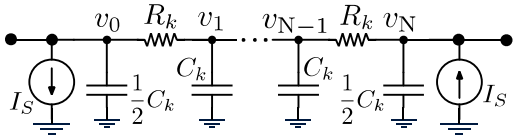


Figure 1. The equivalent circuit for a metal line.

We have used this equivalent circuit model to discover the closed-form analytical expression for the stress at all points in the interconnect tree for any given time t, in terms of the source currents applied to the tree, as

$$\sigma(t) = e^{At}\sigma_0 + (I - e^{At})G^{+}HMDM^{+}i.$$

this allows us to express the set (space) of safe DC current vectors that may be applied to the tree without violating the desired lifetime T for the tree, as captured by

$$(I - e^{AT})G^{+}HMDM^{+}i \leq \sigma_{\text{crit}} - e^{At}\sigma_0.$$

The computation of the matrix exponential e^{AT} is an expensive numerical operation and requires specialized algorithms that take into account the specific problem domain. The eigenvalues of the system matrix A are key to an efficient computation of the exponential. However, given the large sizes of modern interconnect trees, we may discover and maintain only a small fraction of the eigenvalues. Empirical tests indicate that finding and keeping the smallest eigenvalues is the way to go. The Arnoldi algorithm is the best-known method for finding the eigenvalues, but it generates the largest eigenvalues first. We will adapt the algorithm to our needs by performing an initial small shift to the system matrix then LU factorization for each eigenvalue to be kept, and so arrive at the approximation

$$e^{At} \approx \tilde{Q}e^{\tilde{H}t}\tilde{Q}^{*},$$

where $\tilde{Q}$ and $\tilde{H}$ are matrices generated by the algorithm, and $\tilde{Q}^{*}$ is the complex conjugate transpose of $\tilde{Q}$. The $\tilde{H}$ matrix is of much smaller size, and its exponential can be found more efficiently. Preliminary MATLAB results show very good accuracy, and the speedups are shown in Table 1.

Table 1. Speed-up results for a few test cases.

Case	Lines	Nodes	E-vals kept	Exact	Approx	Speedup
1	99	1891	99	5.79 s	0.24 s	24X
2	199	3891	199	40.3 s	1.4 s	34X
3	399	7891	399	206 s	15 s	14X

Keywords: integrated circuits, electromigration, stress, reliability, current constraints

INDUSTRY INTERACTIONS

NXP, Intel, Texas Instruments, Mentor-Siemens

MAJOR PAPERS/PATENTS

[1] F. N. Najm, "Equivalent circuits for electromigration," Microelectronics Reliability, August 2021.

TASK 2810.047, ARCHITECTURE AND DFT METHODS FOR IMPROVING LIFE TIME RELIABILITY AND FUNCTIONAL SAFETY OF ELECTRONIC CIRCUITS AND SYSTEMS OUT OF APPLICATION CONTEXT

DEGANG CHEN, IOWA STATE UNIVERSITY, DJCHEN@IASTATE.EDU

SIGNIFICANCE AND OBJECTIVES

Increasingly more ICs are deployed in mission-critical applications to improve performance, reduce accidents, and save lives. Stringent requirements on lifetime reliability and functional safety (LRFS) are imposed but methodologies are significantly lagging for analog circuits. This project develops cost-effective DfT methods for improving LRFS for analog and mixed-signal circuits.

TECHNICAL APPROACH

We will develop a DfT architecture and multilevel monitoring and healing solutions for ensuring lifetime reliability and functional safety. Digital DfT is assumed available to check our circuits. At power-on, we will use digital-like controls and detectors to verify all analog connectivity and topological correctness, which ensures the functionality of basic analog components. With intrinsic process matching, we then perform accurate AMS BIST and calibration. After that, various health and aging monitors will go online. A concurrent sampling strategy will enable simultaneous measurements of many health and safety conditions and will trigger recalibration and/or safety actions as necessary.

SUMMARY OF RESULTS

We have extended the digital-like DfT method for analog circuit fault detection and coverage, successfully applying it to a standard LDO defect detection. We have developed a wide-range temperature-to-digital converter design not requiring device model details. A test chip is under testing. We developed a digital strategy for checking all component connectivity inside a CDAC based SAR ADC, which enables structural test, defect detection, and defect localization. We developed a fast sensing method for multi-device NBTI aging detection and completed a test-chip design and fabrication.

We have developed a concurrent sampling strategy for simultaneous multi-analog-node online measurements. The method is incorporated with the digital-like DfT method and implemented with a PCB demo design. Figure 1 shows the PCB design to be fabricated and tested. We have also developed a method for simultaneous self-testing and self-calibration of both DAC and ADC in a single shot with no need for external instruments. Simulation results show accurate ADC and DAC testing, and calibration. Demonstration boards have been designed and submitted for fabrication, as shown in Figure 2.

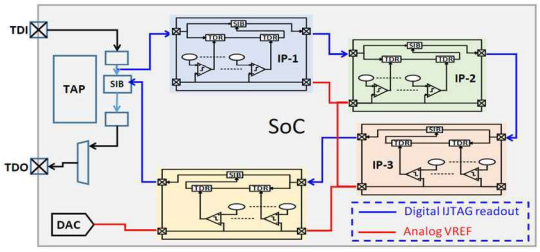


Figure 1. PCB design demonstrating concurrent sampling for multi-node simultaneous analog measurements and digital-like DfT for multiple analog IPs, compatible with IJTAG.

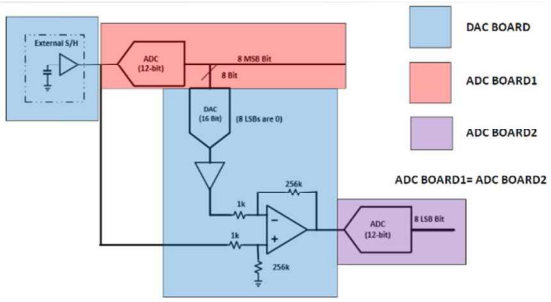


Figure 2. Test board design for simultaneous ADC and DAC co-self-testing, and self-calibration requiring no external instrumentation and targeting >= 20dB performance improvements for both the ADC and DAC.

Going forward, we will test and characterize the fabricated wide-range temperature to digital converter. We will take measurements of the fabricated built-in NBTI monitor. We will demonstrate the proposed DfT methods through PCB measurements and simulations. We will demonstrate the proposed simultaneous self-test and self-calibration of both ADC and DAC without external instrumentation.

Keywords: lifetime reliability and functional safety, power-on digital-like test for analog, built-in self-test and calibration for AMS, online health/aging monitors, online concurrent sampling of many nodes

INDUSTRY INTERACTIONS

Texas Instruments, NXP, Intel

MAJOR PAPERS/PATENTS

[1] Matthew Strong, et al, 2021 MWSCAS, pp. 1112–1115.
[2] Mona Ganji, et al, 2022 IEEE ISCAS.
[3] Marampally Saikiran, et al, 2022 IEEE ISCAS.
[4] Mona Ganji, et al, 2022 IEEE VTS.

TASK 2810.048, CHARACTERIZATION AND MITIGATION OF ELECTROMIGRATION EFFECTS IN ADVANCED TECHNOLOGY NODES

CHRIS H. KIM, UNIVERSITY OF MINNESOTA, CHRISKIM@UMN.EDU

SIGNIFICANCE AND OBJECTIVES

Electromigration (EM) is becoming one of the significant reliability issues in cutting-edge technologies due to higher current densities and increased Joule heating. In this work, we have taped out power grid structures in a 28-nm CMOS technology to collect massive statistical EM data from a realistic power grid.

TECHNICAL APPROACH

In 2021, our group taped out a 2mmx2mm test vehicle in a 28-nm CMOS technology capable of measuring EM-induced voltage degradation in realistic power grids. Four designs under test (DUT) with different via and metal-grid connections were implemented to compare the EM effects for various power grid configurations. Metal on-chip heaters located in the heating area were used to raise the die temperature (> 300°C) to accelerate the EM failure. Analog mux-based scanning circuits can monitor >1000 tapping nodes to track the voltage drop of quasi-loads and the power-grids' IR drop. We have successfully measured detailed power grid voltage degradation using our one-of-a-kind test chip setup.

SUMMARY OF RESULTS

Fig. 1 shows the DUT and full chip layout of the 28-nm EM test vehicle taped out in 2021. Each DUT includes two on-chip heaters for applying a 300°C+ stress temperature. Simultaneously, the analog mux-based scanning circuit, which is located away from the heating area, measures the 1024 voltages inside each power grid. Our group spent roughly 6 months developing the test code and improving the test efficiency and setup based on direct feedback from Siemens EDA. Now we have an excellent test setup that allows us to collect for the first time EM statistics from realistic power grids. A sample test data is shown in Fig. 2 where the local V_{DD} and GND voltages as well as the V_{DD}-GND voltage are plotted.

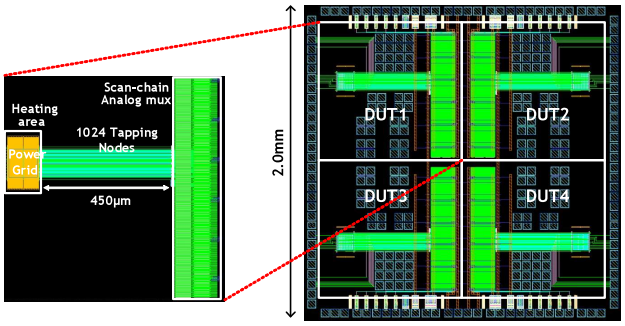


Figure 1. (Left) Proposed 28-nm EM test-vehicle including quasi power-grid, on-chip heater, and voltage scanning circuits. (Right) 2x2mm2 full-chip layout with four different DUT structures.

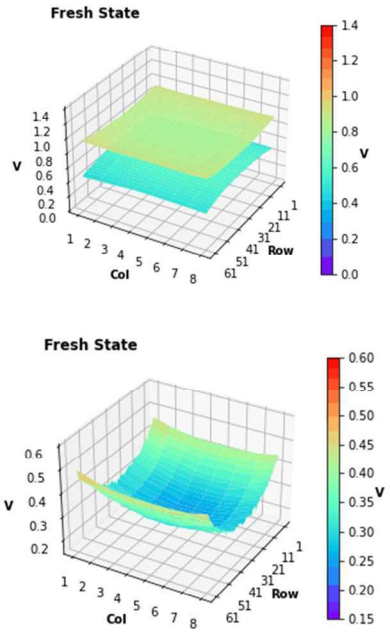


Figure 2. (Top) Measured V_{DD} and GND grid voltages under 340°C stress temperature and 100mA constant stress current. (Bottom) Measured V_{DD}-GND voltages (i.e., local supply voltage seen by circuits) showing gradual degradation with EM stress.

Keywords: Electromigration, power grid, lifetime, characterization, test structure

INDUSTRY INTERACTIONS

Mentor-Siemens, Intel, Texas Instruments

MAJOR PAPERS/PATENTS

[1] A. Kteyan, et al, "Novel Methodology for Temperature-Aware Electromigration Assessment in On-chip Power Grid: Simulations and Experimental Validation," International Reliability Physics Symposium (IRPS), 2022.

[2] V. Sukharev, et al, "Experimental Validation of a Novel Methodology for Electromigration Assessment in On-chip Power Grids," IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, 2021.

[3] N. Pande, et al, "Electromigration-Induced Bit-Error-Rate Degradation of Interconnect Signal Paths Characterized from a 16nm Test Chip," VLSI Technology Symposium, 2021.

TASK 2810.050, INTEGRATING METASURFACES AND MEMS FOR GAS SENSING

SEBASTIAN GÓMEZ DÍAZ, UNIVERSITY OF CALIFORNIA AT DAVIS, JSGOMEZ@UCDAVIS.EDU

SIGNIFICANCE AND OBJECTIVES

The goal is to demonstrate miniaturized infrared (IR) sensors operating at room temperature based on ultrathin metasurfaces (MTSs) integrated within a nanomechanical resonator system (NMEMS). The device will be optimized for gas sensing, an application whose value is expected to increase to $1B worldwide in 2023.

TECHNICAL APPROACH

By merging tailored electromagnetic (EM) and electromechanical resonances, a miniaturized and fast IR detector operating at room temperature will be demonstrated. This device exhibits superior performance to competing technologies in terms of speed, noise, and sensitivity over a relatively narrow band in the IR. The goal is to drastically improve the selectivity of the IR resonance by optimizing the MTS nanoresonators, aiming to achieve absorption responses with a full width half maximum (FWHM) below 0.3um. In the next step of the project, dozens of devices will be integrated within a chip to demonstrate a complete gas sensing system. For this purpose, each NMEMS resonator will be tailored to an IR spectral fingerprint of the targeted gas.

SUMMARY OF RESULTS

In collaboration with Texas Instruments, we have successfully designed, fabricated, and tested the first round of NMEMS. This complex fabrication process was delayed because of (i) COVID, and (ii) the sputtering tool at UC Berkeley was down for a few months. Our first prototype exhibit a loaded Q factor of ~900 (Fig. 1 - top). The inset depicts a contour mode resonator (CMR) device composed of 1µm of AlN with Pt electrodes. Using electron beam lithography (EBL) we fabricated a metasurface composed of 200-nm thick layer of AlN with unity absorption at desired wavelengths (Fig. 1 - bottom). Using EBL instead of optical lithography allows us to achieve a smaller resolution, which improves the metasurface FWHM and ultimately the NEP of the detector. Currently, we are in the last fabrication round of ~1000 NMEMS devices with integrated metasurfaces.

We also developed an automated electrical-infrared test bench to characterize the response of hundreds of sensors in terms of responsivity and noise (Fig. 2). It is composed of a blackbody radiator, chopper, lenses, motorized vacuum choke stage, microscope, and probe station – all controlled through MATLAB.

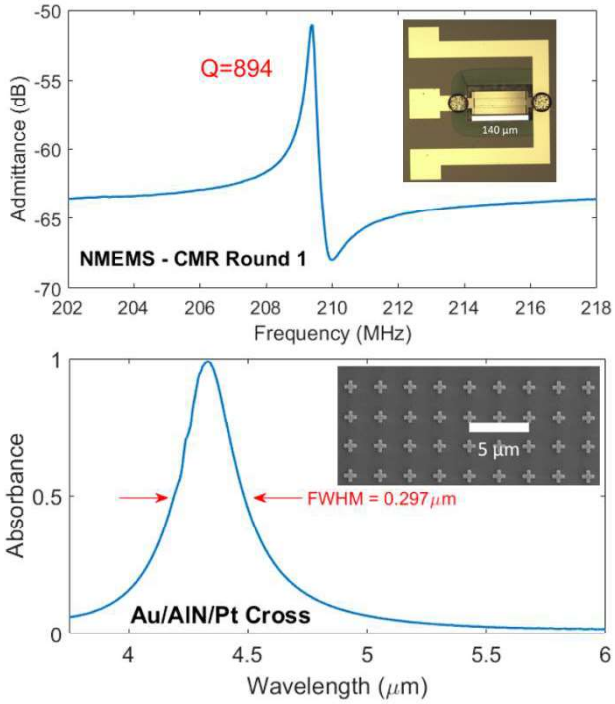


Figure 1. (Top) Frequency response for the first round of NMEMS with an inset of a microscopy image of the fabricated device. (Bottom) Measured absorbance of the metasurface array with an inset of an SEM image of the fabricated metasurfaces.

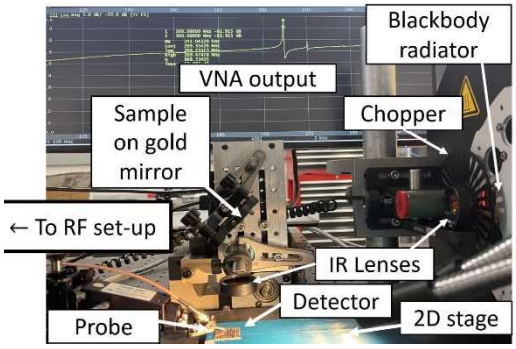


Figure 2. Experimental set-up to measure the responsivity and noise equivalent power of the proposed IR detector.

Keywords: NMEMS, ultrathin metasurfaces, IR sensors, gas sensing, AlN resonators

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

TASK 2810.051, HIGH GAIN DC-DC CONVERTER FOR EV TRACTION SYSTEM

RAJA AYYANAR, ARIZONA STATE UNIVERSITY, RAYYANAR@ASU.EDU

SIGNIFICANCE AND OBJECTIVES

Experimental validation of a multi-input, high-conversion-ratio DC-DC converter for electric vehicle traction systems involving a low-voltage battery pack and a variable DC link voltage is achieved. The proposed architecture increases safety, minimizes cell balancing issues in the battery, eliminates the need for an auxiliary DC-DC converter, and improves the overall efficiency of the system.

TECHNICAL APPROACH

In EV traction systems, higher voltage motors offer improved efficiency and power density. Variable DC link voltage improves the overall efficiency of the traction system. The proposed multi-input high conversion ratio converter (HCRC) can achieve high and variable voltage gain (4 to 20 times for a 4-phase converter) with a significant reduction in voltage and current stress across its devices. This enables use of a 48-V battery pack which significantly increases the overall safety. Each phase of HCRC is connected to a separate battery module whose charging-discharging can be independently controlled to achieve cell balancing easily.

SUMMARY OF RESULTS

Figure 1 shows one of the configurations of the proposed architecture for 48V to >800V variable DC link conversion. A scaled hardware prototype of a 4-phase multi-input HCRC is developed to verify the proposed concept. The prototype is rated for 4kW (each module) operating at 48-V input. The output voltage can vary from 200V to 800V achieving a conversion ratio of 4 to 17 without any transient spikes in switch voltage or current.

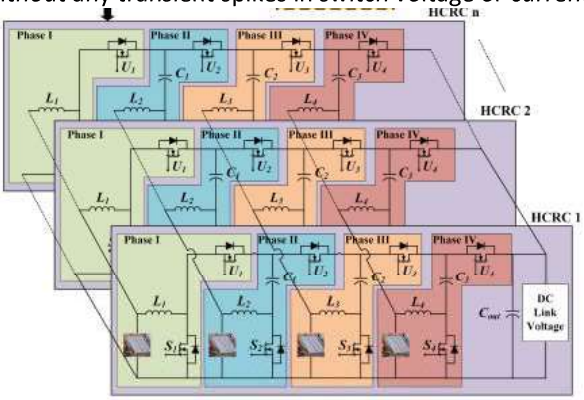


Figure 1. One of the configurations of the proposed 4-phase multi-input high conversion ratio converter for EV traction systems.

Multiple possible configurations of HCRC in parallel have been derived and verified in simulation and hardware experiments. The configurations include interleaved and non-interleaved connections of HCRC with different battery modules. A sample design of the proposed architecture corresponding to the Chevrolet Bolt battery pack has also been published.

The HCRC operation is verified experimentally through a scaled hardware prototype for both interleaved and non-interleaved configurations. The hardware prototype is operated in dual-loop control with an inner current loop and an outer voltage loop. The inner current loop regulates the current supplied by each input source while the voltage controller regulates the output voltage to the desired value. The converter can operate at both equal and unequal current sharing among the different input phases over the whole range of operation with the output voltage regulated to the desired value. The converter has bi-directional power flow capability allowing it to operate in buck mode during regenerative braking in an electric vehicle. The converter operation in both boost and buck mode is verified experimentally using the hardware prototype.

As the converter has low voltage stress across the devices, 650 -V SiC MOSFETs are selected which have low on-state resistance to minimize the conduction losses. The converter can achieve a peak efficiency of 98.36% at 400V, 2-kW output with a switching frequency of 50 kHz. The converter has similar performance results in buck mode with 98.16% efficiency for 400V to 48V operation at 2kW. With interleaved configuration, the net inductor size reduces by 55% with a slight increase of overall efficiency.

Keywords: DC-DC Converter, High Gain, Non-isolated boost, Variable DC link, EV Traction

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] A. Gupta, R. Ayyanar and S. Chakraborty, "Novel Electric Vehicle Traction Architecture with 48 V Battery and Multi-Input, High Conversion Ratio Converter for High and Variable DC-Link Voltage," in IEEE Open Journal of Vehicular Technology, pp. 448-470, 2021.

[2] A. Gupta, R. Ayyanar and S. Chakraborty, "Soft-Switching Mechanism for a High-Gain, Interleaved Hybrid Boost Converter," in IEEE Journal of Emerging and Selected Topics in Ind. Electronics, pp. 420-430, Oct. 2021.

TASK 2810.054, RECONFIGURABLE AC POWER CYCLING SETUP AND PLUG-IN CONDITION MONITORING TOOLS FOR HIGH POWER IGBT AND SIC MODULES

BILAL AKIN, THE UNIVERSITY OF TEXAS AT DALLAS, BILAL.AKIN@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

Automotive manufacturers are moving towards Silicon Carbide MOSFET-based inverters. Reliability assessment and condition monitoring solutions become crucial to address safety concerns. AC power cycling is the most realistic reliability test. This research investigates the suitable precursors for SiC device condition monitoring circuits, lifetime models, and remaining useful lifetime estimation.

TECHNICAL APPROACH

For this purpose, a 200-kVA AC cycling setup is built and tested. Utilizing TI UCC5870 gate driver IC's, three condition monitoring (CM) circuits are designed (i) threshold voltage, (ii) body diode voltage, and (iii) on-resistance measurement. The CM circuits in the board can cover all three main aging mechanisms: package, gate oxide, and body diode aging. Also, the power stage of the AC power cycling setup has been completed. Full test setup, sensing circuits, and protection features have been debugged and calibrated at full current. Lastly, closed-loop control is implemented for current control and junction temperature measurements.

SUMMARY OF RESULTS

Different precursors and their condition monitoring circuits are evaluated. Based on this evaluation, a gate driver board is developed for condition monitoring purposes to determine the state of health of the devices in real applications (see Fig. 1). The proposed circuits are integrated into DESAT (Desaturation) protection to decrease the number of components.

A new precursor (transconductance) has been identified, and a new daughter board has been designed and fabricated. A new technique is also proposed to measure transconductance and threshold voltage without using high bandwidth current sensors (Fig. 2).

Fig. 3 shows the fabricated high power density setup for AC power cycling (ACPC). A software function is developed for flexible control and communication of ACPC. An out-of-order sampling technique is developed to decrease the acquisition burden and measurement error.

Figure 1. Second version of gate driver board with embedded condition monitoring systems for different aging mechanisms.

Figure 2. Transconductance daughter Board.

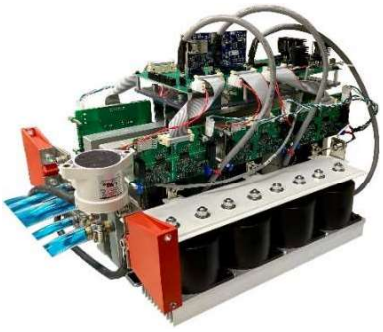


Figure 3. AC power cycling test setup.

Keywords: SiC MOSFETs, AC power cycling, performance degradation, condition monitoring, reliability

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] "Investigation and On-Board Detection of Gate-Open Failure in SiC MOSFETs," in IEEE Transactions on Power Electronics, vol. 37, no. 4, pp. 4658-4671, April 2022.

[2] "A method for reliable on-board detection of gate-open faults in power semiconductor switches", Patent, UTD 21010.

D. BRIAN MA, THE UNIVERSITY OF TEXAS AT DALLAS, BRIAN.MA@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

Today EMI remains a critical design challenge in power electronic circuits. With ever-growing deployment of electronic devices, electromagnetic interference (EMI) emission in modern automotive electronics is record-high. The situation deteriorates further due to high *dv/dt* and *di/dt* transients, as more high-end power modules shift to adopt high-performance GaN power switches for faster and more efficient operation. The proposed techniques support effective EMI suppression and minimize switching power losses.

TECHNICAL APPROACH

To suppress EMI in switching power circuits effectively, passive EMI filters, shielding, PCB, and packaging innovations can be applied. However, these approaches often come at the significant expenses of system volume, PCB real estate, and cost. Alternatively, EMI can be mitigated using compact, cost-effective, active circuit techniques, especially if a power circuit is naturally equipped with sensing mechanisms and feedback control loops, which are highly adaptive to variable conditions. Hence, our focus is on active circuit techniques for EMI suppression.

SUMMARY OF RESULTS

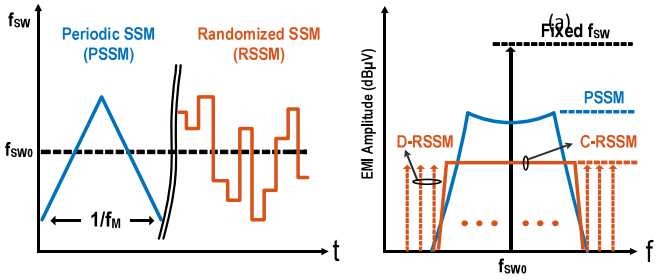


Figure 1. Comparison of EMI modulation between PSSM and RSSM schemes [1].

In a PWM control switching of a power circuit, power switches are controlled at a fixed switching frequency f_{SW}. Therefore, its EMI spectrum is distributed as spurious peaks at f_{SW} and harmonics. The modulation scheme, on the other hand, would redistribute EMI energy into a broader frequency range so that spurious EMI peaks are suppressed. A popular frequency modulation scheme is periodic SSM, in which the frequency modulation follows a periodic pattern. The periodic SSM is easy to implement in a circuit and has low power and cost overhead. However, it is not as effective for EMI suppression as random SSM (RSSM), as shown in Fig. 1.

On the other hand, EM spectrum presented by a power converter itself can also be vulnerable to another type of side-channel attack (SCA) – power SCA. Hence, the modulation scheme should also be enciphered to improve security. This leads to the need to randomize the switching frequency of the converter. To implement the RSSM in circuits, a Markov-chain-based continuous RSSM is designed. Theoretically, if the modulation follows the piecewise linear one-dimensional (PL1D) map in Fig. 2(a), the state transitions of sequence $\{V_{ran}[n]\}$ in Fig. 2(b) provide an unpredictable random output. Moreover, the state transition from $V_{ran}[n]$ to $V_{ran}[n+1]$ is in an analog manner, suggesting that the set of V_{ran} is continuous. Hence, the Markov-chain-based random clock generator possesses infinite number of states, overcoming the limitation of digital RSSM implementations. Fig. 3 demonstrates that a highly randomized f_{SW} pattern is achieved within a low modulation range of 10%, avoiding potential conflicts with the effort to mitigate anti-aliasing.

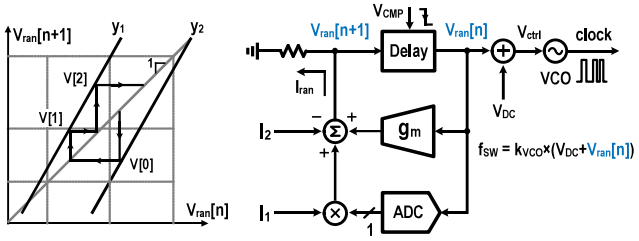


Figure 2. (a) PL1D map of Markov-chain random voltage source, (b) block diagram of Markov-chain C-RSSM.

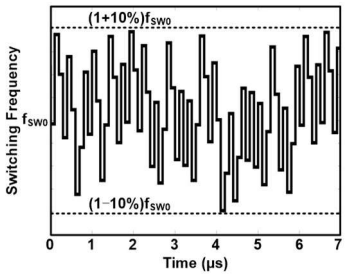


Figure 3. Markov-Chain generated randomized f_{SW}.

Keywords: RSSM, EMI, EM SCA

INDUSTRY INTERACTIONS

Texas Instruments, IBM, NXP

MAJOR PAPERS/PATENTS

[1] D. Ma, D. Yan, L. Du, "Active Conducted EMI Suppression in GaN Switching Power Circuits," IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium, pp. 1-6, Monterey CA, Dec. 2021.

TASK 2810.057, RELIABILITY STUDY OF E-MODE GAN HEMT DEVICES BY AC TDDB AND HIGH-RESOLUTION TEM

MOON KIM, UNIVERSITY OF TEXAS AT DALLAS, MOONKIM@UTDALLAS.EDU
HISASHI SHICHIJO, UNIVERSITY OF TEXAS AT DALLAS

SIGNIFICANCE AND OBJECTIVES

E-Mode GaN HEMTs are studied for their gate reliability to expand their use in power devices. The gate controls 2-DEG channel formation in AlGaN/GaN channel. This work examines reliability through AC voltage pulse stressing, effects of stress to gate characteristics of p-GaN E-mode GaN HEMT, and in-situ STEM with biasing.

TECHNICAL APPROACH

Commercially available p-GaN E-mode GaN HEMTs were characterized for their electrical and physical characteristics. Electrical measurements include AC pulse stress to induce breakdown in the gate and gate I_G-V_G characteristics. Failed devices were subjected to a detailed physical analysis. Physical characterization of the devices before and after the breakdown is performed with high-resolution electron microscopy techniques. In-situ electrical biasing samples with a gate-drain structure are made using FIB and e-chip. The in-situ sample was electrically biased and imaged in real-time in a STEM.

SUMMARY OF RESULTS

E-mode GaN HEMTs with p-GaN gate were subjected to the voltage pulse stress at 8 V with a 3.2-ms on-off pulse cycle. As seen in Figure 1, the recorded I_G shows a quick increase in the gate current to a step-like increases with time (Fig. 1(a)). The gate characteristics of the devices show a multi-stage gate leakage pattern. First is the increase in the gate current at a higher gate voltage, second is the increased gate leakage at a lower voltage, and finally, the complete failure of the gate (Fig. 1(b)). This indicates the degradation at the AlGaN/GaN interface, metal/p-GaN junction, and fusion of the gate stack.

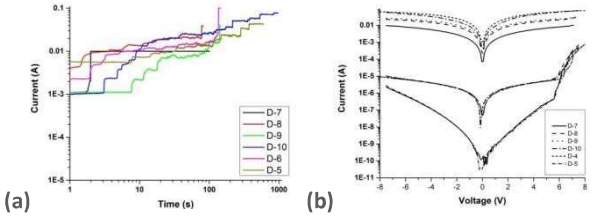


Figure 1. (a) AC voltage pulse stress data and (b) Gate characteristics of E-mode GaN HEMTs.

It was seen that the device started leaking as soon as the pulse stress commenced. To study the early-stage leakage, the device was pulse stressed for a specific time, and the gate leakage was measured after intervals. The early-stage leakage shows recovery 24-48 hrs after the stress is stopped. The leakage is attributed to the charge accumulation in the p-GaN region. To check the accumulation, we recorded I_D-V_G, where we observe that holes are accumulated in the p-GaN region. After the pulse stress is stopped, the charge homogenizes, and the device recovers (Figure 2).

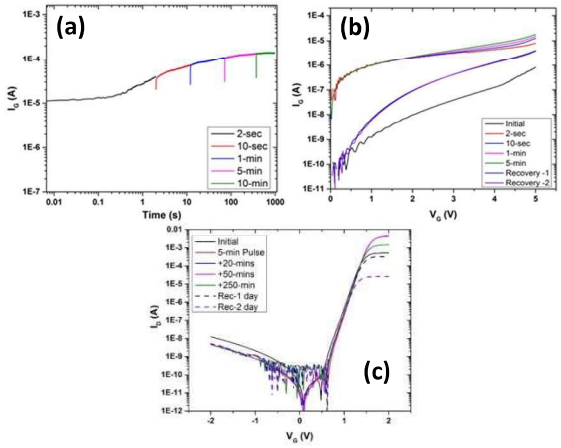


Figure 2. (a) Pulse stress data at 6 V, (b) Gate characteristics, and (c) Drain characteristics.

A new in-situ electrical biasing sample preparation is developed for two-terminal biasing in TEM. The in-situ test sample has drain and gate contacts, with Pt used as connecting leads. Figure 3 shows a sample and biasing data for the sample.

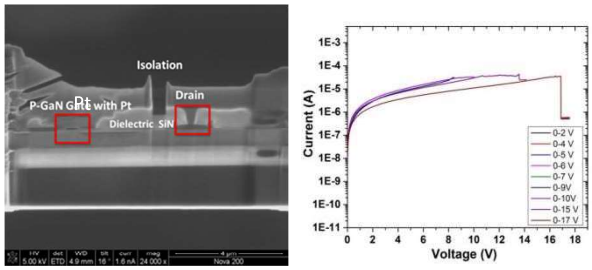


Figure 3. SEM images of the new two-terminal sample preparation for in-situ STEM electrical biasing of E-mode GaN HEMTs (left) and biasing data (right).

Keywords: E-mode GaN HEMT device, Reliability, in-situ TEM probing

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

TASK 2810.058, MACHINE LEARNING-BASED OVERKILL/UNDERKILL REDUCTION IN ANALOG/RF IC TESTING

YIORGOS MAKRIS, UNIVERSITY OF TEXAS AT DALLAS, YIORGOS.MAKRIS@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

With the rising complexity of semiconductor devices, the testing procedures have become complex and time-consuming. Depending on the nature of the test solution, some good chips will get discarded (overkill) or some defective chips being retained (underkill). We exploit machine learning-based solutions to develop a comprehensive yield management scheme.

TECHNICAL APPROACH

For the problem of overkill, we propose a three-step approach that predicts the values of auxiliary tests using multivariate regression models, clusters that predicted the actual outcomes of auxiliary tests, and finally combine the two outcomes along with a proximity-based metric to decide on the devices to recover. For underkill, we use the probe test measurements of devices across multiple insertions to train a Gaussian mixture model to identify devices that have a higher probability of failure on-site and become a customer return. Due to the vastness of probe test measurements, we perform feature space exploration to extract signatures from customer returns.

SUMMARY OF RESULTS

For mitigating overkill, an industrial dataset of 92,022 devices with measurements from 66 specification tests and 241 auxiliary tests is utilized. Out of the 92,022 devices, 9.6% of devices fall into our focus group which passes the specification tests but fails one or more auxiliary tests. We used the 87.21% of devices that passed both sets of tests as predictors in the regression model to predict the failing auxiliary test measurements for the 9.6% of the devices.

Table 1. Test Outcome after Regression.

		Specification Tests	
		Pass	**Fail**
Auxiliary Tests	**Pass**	80261 + **8235**	**605**
	Fail	726	2195

Based on Table 1, we can observe that by predicting failing auxiliary test measurements we were able to recover 8,235 devices but there is no ground truth to verify our results. Using these predicted outcomes and actual outcomes of the auxiliary tests for the devices under test, we cluster them to address the sub-optimally defined test limits. Combining the both results, we get three buckets of devices. In one of these buckets, the two outcomes diverge, and we use a proximity-based metric to decide. Using this approach, we were able to recover 81.6% of devices from our focus group.

For mitigating underkill, an industrial dataset of 24,000 devices was utilized. These are collected from 19 wafers. The dataset consisted of 19 customer returns (one for each wafer) and each of these can be further broadly classified into different fault-id on return analysis. As a first step, we perform feature space exploration to generate a hyperspace that can separate the distribution of faulty devices from nominal devices, using the differential in probe test measurements across hot and room temperature insertions. Any abnormal variation in device measurements across the insertions is indicative of a failure.

Due to the gaussian nature of test measurements across a wafer, we perform unsupervised Gaussian mixture model clustering. The clusters whose gaussian mean are further from the means of the nominal devices have a higher probability of failure as shown using the heat map in Figure 1. The customer return devices are outliers coming from different corners of the distribution.

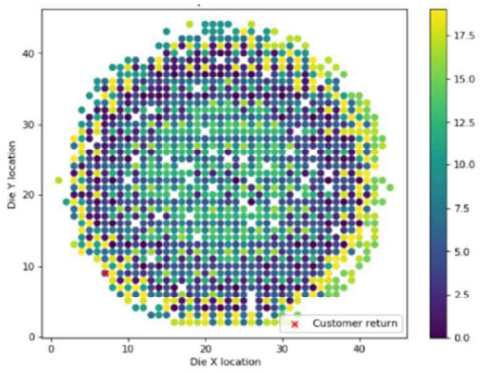


Figure 1. Wafer heat maps of GMM clusters.

Keywords: yield recovery, machine learning, adaptive testing

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] D. Neethirajan, V. A. Niranjan, R. Willis, D. Webster, A. Nahar, and Y. Makris, “Machine Learning-Based Overkill Reduction through Inter-Test Correlation,” IEEE VLSI Test Symposium (VTS), 2022.

TASK 2810.059, ULTRA-LOW-POWER ROBUST SAR ADC FOR PMCW AUTOMOTIVE RADAR

YUN CHIU, UNIVERSITY OF TEXAS AT DALLAS, CHIU.YUN@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

A study on the feasibility of using an elastic S/H (ESH) technique for bottom plate sampling is presented. We find that distortion at the summing node can be corrected, allowing for an improved sampling structure wherein the summing-node switch size is greatly reduced. This new guideline can be applied equally to SAR, pipelined SAR, as well as conventional pipelined ADCs.

TECHNICAL APPROACH

The feasibility of treating the post-sampling summing-node voltage as a dynamic "offset" of the preamplifier was tested using a behavioral simulation of a 10-bit SAR ADC. Two methods of removing the "offset" voltage were tested and found to be effective. Distortion contributions from the sampling and/or summing-node switches before and after the correction was tested using a nonlinear switch model. The behavior was analyzed in a simplified sampling circuit, then the functionality of ESH given finite driver impedance and parasitic capacitance was checked.

SUMMARY OF RESULTS

A schematic of a bottom plate sampling circuit is shown in Figure 1 below with C_x for preamp offset removal.

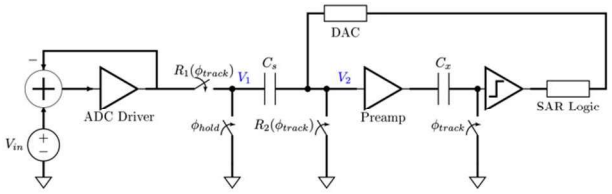


Figure 1. Bottom-plate sampling circuit in a SAR ADC with preamp "offset" removal to correct summing-node swing.

To correct for swing or distortion at the summing node V_2, we can treat V_2 swing as a 'dynamic' offset voltage – dynamic because of its signal-dependent nature – of the preamp (i.e. one that will vary from sample to sample). Therefore, the existing techniques used to remove offset can be used to remove the swing at the summing node. Both an output storage technique (Figure 1) or an input storage technique (where the offset storage is at the input of the preamp) was effective, although the output storage technique is likely the better design.

The dominant nonlinearity in a bootstrapped switch such as the sampling switch R_1 or summing node switch R_2 arises from a variation on which side of the switch is the source or the drain, which depends on whether the input is rising or falling. The nonlinearity at V_1 is dominated by R_1 and at V_2 by R_2. Without ESH, the sampled voltage is $V_1 - V_2$, meaning that the nonlinearity from both switches contribute equally. With ESH, the sampled voltage is just V_1, meaning only the distortion from R_1 contributes.

If a nonlinear switch resistance is scaled by a factor of K (meaning the switch is K times smaller), then the swing across the switch is K times larger, resulting in K^2 as much distortion. Therefore, if $R_2 = KR_1$, then the improvement to THD when correcting the summing node is a factor of $K^2 + 1$. Figure 2 below shows that this means we can correct for nearly all of the distortion caused by R_2 and are only limited by the distortion caused by R_1.

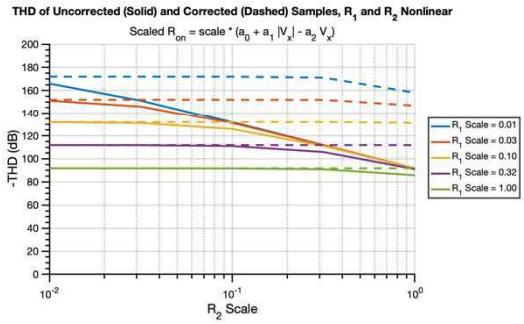


Figure 2. THD of sampled voltage with varying sizes of R_1 and R_2 with or without summing-node correction.

We verified that given finite switch and C_S parasitic capacitances, and finite ADC driver output impedance and bandwidth, the summing node switch can still be made smaller. The smaller switch would aid in improving the feedback factor during residue amplification and summing node attenuation during the SAR bit cycles, both helping with the power efficiency. We also found that for a given switch size, a lower driver G_m is needed to achieve the same THD.

In the following year, the plan is to verify these results with transistor circuits. We plan to do design and layout of a 10b 1Gs/s SAR ADC in a 65-nm CMOS process to verify the benefits of ESH in silicon.

Keywords: Elastic S/H (ESH), THD, switch nonlinearity, summing-node swing, summing-node distortion

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

TASK 2810.064, CHARACTERIZATION AND TOLERANCE OF AGEING IN INTEGRATED VOLTAGE REGULATORS

SAIBAL MUKHOPADHYAY, GEORGIA INSTITUTE OF TECHNOLOGY, SAIBAL@ECE.GATECH.EDU

SIGNIFICANCE AND OBJECTIVES

The project will develop circuit techniques and design methodologies to model, characterize and tolerate ageing in integrated voltage regulators, including on-chip inductive buck and digital low dropout regulators, used in modern SoCs.

TECHNICAL APPROACH

The objectives of this research are to (1) analyze the effects of ageing in IVRs, (2) design a test-circuit to efficiently characterize ageing in IVRs, (3) estimate ageing-induced design margin for IVR and develop circuit techniques to tolerate ageing, and (4) explore on-line tuning for tolerating ageing in IVRs. We will focus on high-frequency inductive buck regulators and DLDOs, both with digital voltage-mode control topologies.

SUMMARY OF RESULTS

We have developed a simulation methodology to analyze the effects of HCI (Hot carrier injection) on transient performance and efficiency of a digitally controlled IVR designed in 65-nm CMOS (Fig. 1). The proposed simulation methods coupled device level aging models with circuit level simulations of individual components of an IVR, and finally, combine them to study the closed-loop performance of an IVR using a Simulink model. The mixed-mode simulation allows analyzing the aging effect under various operating conditions of an IVR, without the need for computationally prohibitive closed-loop circuit simulations. It can be extended as a generic method for other systems like low-dropout regulators.

We have used the developed simulation framework to characterize the effects of HCI on the components of IVRs, namely, Analog to digital converter (ADC), Digital proportional-integral-derivative (PID) controller, power stage, and gate drivers. The effects on these individual components are coupled to characterize the impact of HCI on the transient response and efficiency of the entire IVR. Moreover, we showed that the simulation methodology can be adapted to study various aging mechanisms. A comparative analysis between HCI and NBTI induced aging of IVR is presented. Finally, the simulation framework is adapted to analyze the impact of package parasitic on the HCI and NBTI induced degradation of the IVR (Fig. 2).

Simulations are performed with an IVR designed in a 65-nm CMOS technology. It is observed that HCI-induced degradation leads to a longer settling time from output current change to output voltage stabilization, and a larger first droop after output current change during a load transient and reduced efficiency. As expected, HCI effect increases while down-converting (and operating with) a higher input voltage. A higher switching frequency (i.e., higher bandwidth) of IVR also increases the HCI-induced degradation. We further observe that HCI leads to a higher degradation in transient performance compared to NBTI. Finally, the analysis shows that the parasitic impedance of associated with the C4 bumps (or bond-wires) of a package impacts aging-induced degradation. In particular, a parasitic inductance near the IVR's input aggravates NBTI while parasitic capacitance near the IVR's output aggravates HCI effects.

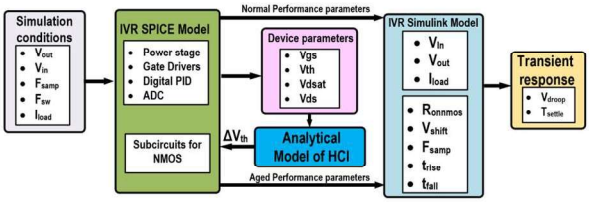


Figure 1. IVR Ageing simulation framework.

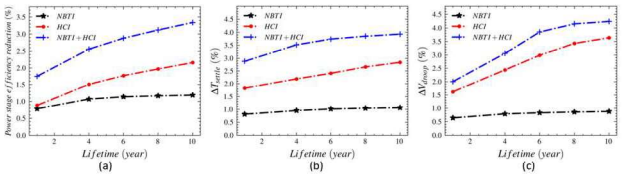


Figure 2. Simulation of HCI and NBTI effect on (a) power stage efficiency reduction, (b) degradation of settling time, T_{settle}, (c) degradation of first voltage droop, V_{droop} over 10-year lifetime.

Keywords: Integrated voltage regulator, ageing

INDUSTRY INTERACTIONS

Intel, IBM, NXP

MAJOR PAPERS/PATENTS

[1] S. Zhang, et.al., "Analysis of the Effect of Hot Carrier Injection in An Integrated Inductive Voltage Regulator," IEEE/ACM ISLPED 2022.

TASK 2810.065, POWER-EFFICIENT AND RELIABLE 48-V DC-DC CONVERTER WITH DIRECT SIGNAL-TO-FEATURE EXTRACTION AND DNN-ASSISTED MULTI-INPUT MULTIPLE-OUTPUT FEEDBACK CONTROL

MINGOO SEOK, COLUMBIA UNIVERSITY, MGSEOK@EE.COLUMBIA.EDU

SIGNIFICANCE AND OBJECTIVES

The goal of this project is to design the sensing and control circuit for a 48-V DC-DC converter for the data center application. The proposed sensing and control system will be able to measure the real-time power converter efficiency (PCE), track the maximum PCE point and enhance the reliability of the converter.

TECHNICAL APPROACH

We designed three key features to improve the DC-DC converter PCE and reliability. First, we developed a sensing circuit to sample the converter input and output current and calculate the real-time PCE. Then, we designed a digital controller to track the maximum PCE point by modulating the gate width of power switches. We also designed a roaming circuit that functions at a steady-state, which divides the stress on power switches equally on each switched segment, thus improving the reliability of the converter.

SUMMARY OF RESULTS

We designed a prototype of the DC-DC converter. We are going to verify the PCE tracking and reliability enhancing function using the prototype.

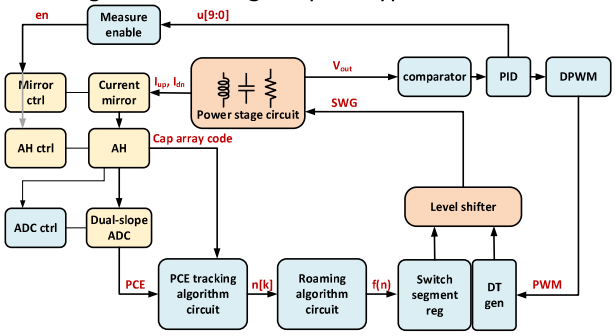


Figure 1. Block diagram of the DC-DC converter shows the signal flow in control loops. The blue blocks use 1.8-V V_{DD}, the yellow blocks use 5-V V_{DD}, and the red blocks are high-voltage blocks.

Figure 1 shows a block diagram of the DC-DC converter with sensing and control circuits. It has two control loops on the periphery of the power stage circuit. One is for stability contro and the other is for PCE tracking and reliability enhancements.

The voltage mode PWM control ensures the stability of the power stage. It includes a comparator, proportional–integral–derivative controller (PID), digital PWM signal generator (DPWM), deadtime generator (DT gen), and level shifter. The comparator first digitizes V_{out} and sends the digital value to the PID controller. DPWM transfers the PID output control code into the a PWM control signal. Then, the DT gen introduces a deadtime between high-side and low-side switches and sends the control signal to each power switch through the level shifter.

The second control loop performs PCE measurement, maximum PCE point tracking, and roaming algorithm. It includes a current mirror, accumulate-and-hold (AH) circuit, dual-slope ADC and their control circuit, PCE tracking algorithm circuit, and roaming algorithm circuit. When the PID output stays unchanged for a long enough time, we say the power stage circuit is in a steady state. Then, the measure enables the circuit to activate the current mirror to sample the converter input and output current. AH circuit accumulates the mirrored current and converts them into voltages. These voltage values represent the input and output power of the converter. Afterward, a dual-slope ADC calculates the ratio between two voltages to get the real-time PCE measurement. The PCE tracking algorithm circuit performs dynamic gate width modulation in the DC-DC converter and compares the measured PCE in the past and present monitoring window. It then uses gradient descent algorithms to track the maximum PCE point. Afterward, the roaming algorithm circuit equalizes the stress to the power switch segments by equally distributing the turn-on period among the switch segments. By doing so, we can mitigate the aging effect of the power switch and enhance the reliability of the converter. The switch segment register synchronizes the roaming output with the PWM control signal and applies control signals to each power switch through the level shifter.

Keywords: PCE tracking, gate width modulation, PCE measurement, reliability

INDUSTRY INTERACTIONS

Texas Instruments, IBM, Intel

MAJOR PAPERS/PATENTS

[1] Z. Wang et al., “Review, Survey, and Benchmark of Recent Digital LDO Voltage Regulators,” (Invited) 2022 CICC, April 2022, Newport Beach, CA, USA.

TASK 2810.066, DEMONSTRABLY GENERALIZABLE COMPACT MODELS OF ESD DEVICES

ELYSE ROSENBAUM, UNIVERSITY OF ILLINOIS, URBANA-CHAMPAIGN, ELYSE@ILLINOIS.EDU

SIGNIFICANCE AND OBJECTIVES

This project will develop methodologies for creating charge-based compact models of ESD protection devices and verifying that the model correctly represents the device's response to arbitrary stimuli. This will allow designers to use simulation to create protection circuits that can protect I/O pins in advanced nodes without compromising signal integrity.

TECHNICAL APPROACH

Using a charge-based approach, compact models suitable for transient and AC analysis will be developed. Dual-purpose devices, e.g., MOSFETs, are used both in functional circuits and on-chip protection networks. We will demonstrate ESD shell models that do not compromise the accuracy of AC and transient simulations of normal operating conditions. Transient models of ESD devices are validated using waveforms that are different from those used for parameter extraction. Package models suitable for CDM-ESD simulations will be created.

SUMMARY OF RESULTS

Previously, we demonstrated a non-quasi static model of the CMOS P-well ESD diode, which properly represents the long tail of the reverse recovery current transient. Recently, that model was extended to the N-well ESD diode. The N-well diode must be represented as a PNP, due to the N-well to P-substrate junction. We start with a modified SPICE Gummel-Poon model and then use the NQS diode model to represent the base-emitter junction and the stored charge in the base. The model is illustrated in Fig. 1 and selected model equations that highlight the NQS nature of the model are given in Table 1. The NQS formulation requires that high-level injection (HLI) be represented differently from the SGP model. HLI is encapsulated in the model equation that computes the variable I_F as a function of the voltage across the emitter-base junction.

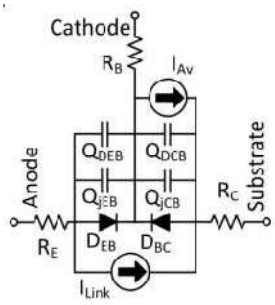


Figure 1. Schematic representation of N-well ESD diode model.

The model accurately represents the high-current pulse I-V characteristic, shown in Fig. 2(a), without significant impact to the fit at low current levels (Fig. 2(b)). The peak amplitude of the forward and reverse recovery transients is well represented in the simulation shown in Fig. 3, but the duration of the transients is not captured precisely. We are investigating whether the (small) error can be eliminated by modifying the parameter optimization procedure, which is based on that used for the P-well diode, or if the equations relating to the base charge need to be changed to reflect the physical differences between P-well and N-well diodes.

Table 1. Selected model equations.

$Q_E = I_F \tau_F$
$0 = \frac{dQ_{EB}}{dt} + \frac{Q_{EB}}{\tau_F} - i_{DF}$
$i_{DF} = \frac{Q_E - Q_{EB}}{T_{MF}}$
$i_{Link} = i_{DF} - I_R$
$i_{DEB} = \frac{i_{DF}}{\beta_F}$

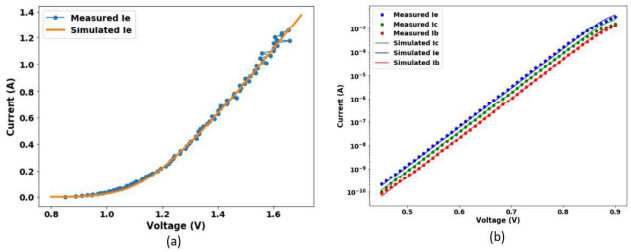


Figure 2. (a) TLP I-V, measured and simulated, and (b) Low current DC I-V, measured and simulated for N-well diodes.

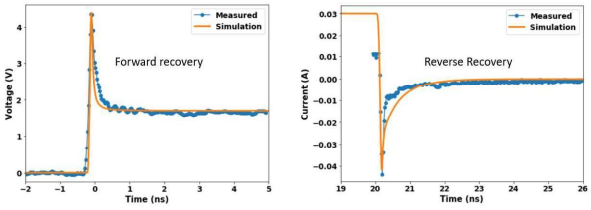


Figure 3. Measured and simulated forward and reverse recovery transients for the N-well diodes.

Keywords: ESD, compact models, circuit simulation

INDUSTRY INTERACTIONS

NXP, Texas Instruments, AMD

MAJOR PAPERS/PATENTS

[1] S. Huang and E. Rosenbaum, "Compact model of ESD diode suitable for sub-nanosecond switching transients," in Proc. *2021 IRPS*.

TASK 2810.070, EARLY AND LATE LIFE FAILURE PREDICTION METHODS FOR ANALOG AND MIXED-SIGNAL CIRCUITS

CHRIS H. KIM, UNIVERSITY OF MINNESOTA, CHRISKIM@UMN.EDU

SIGNIFICANCE AND OBJECTIVES

The main goal of this task is to develop a synthesizable odometer IP for effectively monitoring long-term aging in a real IC product. In collaboration with our industry sponsors, we have demonstrated a synthesized version of the silicon odometer aging sensor in 65-nm CMOS for measuring frequency degradation caused by device aging.

TECHNICAL APPROACH

Our previous silicon odometer circuit based on the beat frequency (BF) detection technique was implemented fully in structural and behavioral Verilog. The synthesizable design involves no manual layout and gives the flexibility to port the design to any technology. The design includes produce-friendly features such as a calibration-free power supply, a Verilog module for enabling the circuit to come out of the dead zone, along with a technique to remove glitches in ring oscillators during startup.

SUMMARY OF RESULTS

Three-ring oscillators (ROSCs) composed of INV, NAND, and NOR gates were implemented in register-transfer-logic (RTL). The new odometer has product level features such as calibration-free operation, automatic frequency dead zone escape, and start-up glitch removal. The odometer Verilog code was synthesized and automatically placed and routed using standard ASIC design tools. The original silicon odometer included frequency trimming circuits that allows tuning of the initial ring oscillator frequencies. In the new RTL based design, the frequency trimming circuitry was removed which makes the overall design attractive for product chips. The measured data from a prototype implemented in a 65-nm CMOS technology, with a daisy chain of 12 odometers, is presented in Fig. 2, for INV, NAND, and NOR ROSCs. Frequency shifts were measured at different voltages (1.2V, 1.5V, and 1.8V) and temperatures (-40°C, 27°C, and 100°C). Unlike our past odometer designs, the supply voltage of the synthesizable odometer remains the same during both stress and measurement modes. The data show more degradation in NOR than NAND and INV, because of the NBTI impact to the stacked PMOS devices in the NOR gate. Interestingly, due to malfunction in the hardware, 1.8V-100°C data shows stress interruption at ~10,000s. Consistent with the previous reports, the degradation quickly goes back to the original trend line after the stress is active again.

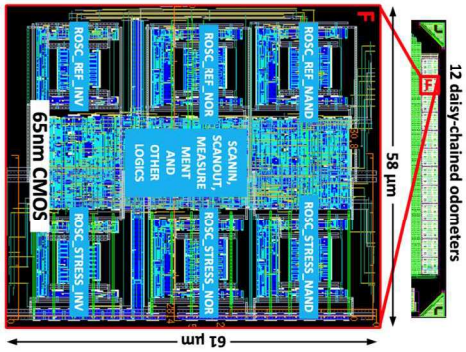


Figure 1. Odometer chain and single odometer instance in 65-nm CMOS.

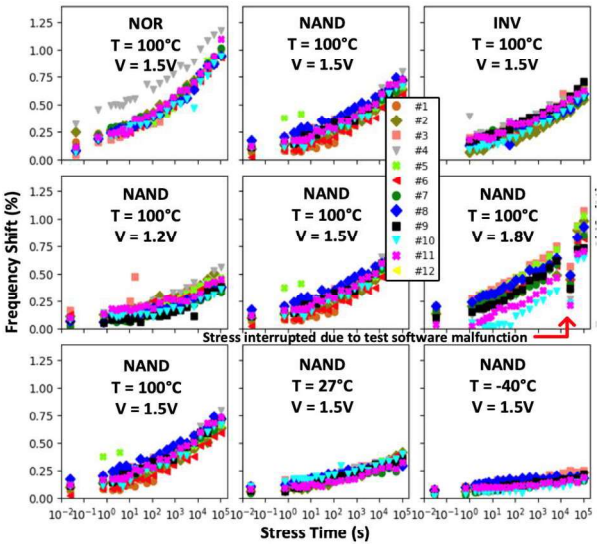


Figure 2. Frequency shift measurements at different gates under different voltage and temperature settings.

Keywords: Silicon odometer, synthesizable, Verilog, automatic place and route, 22-nm test chip

INDUSTRY INTERACTIONS

NXP, Intel

MAJOR PAPERS/PATENTS

[1] T. Islam, J. Kim, D. Tipple, M. Nelson, R. Jin, A. Jarrar, and C.H. Kim, "A Calibration-Free Synthesizable Odometer Featuring Automatic Frequency Dead Zone Escape and Start-up Glitch Removal," International Reliability Physics Symposium (IRPS), 2022.

TASK 2810.074, THERMAL PERFORMANCE CHARACTERIZATION AND DEGRADATION MONITORING OF LDMOS BASED INTEGRATED POWER IC WITH ON-DIE TEMPERATURE SENSORS

BILAL AKIN, UNIVERSITY OF TEXAS AT DALLAS, BILAL.AKIN@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

Lateral Diffused MOS (LDMOS) devices are widely used in power integration applications. With the unprecedented increase in current density and switching speed, stress caused by voltage overshoots become harsher, which leads to avalanche breakdown. Therefore, it is necessary to investigate the LDMOS devices' robustness against repetitive avalanche breakdown.

TECHNICAL APPROACH

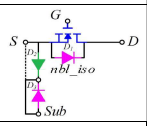
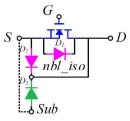
A large-scale test setup is implemented to simultaneously stress multiple devices for time reduction and convincing test results. Based on the modular design, the system is capable of easy expansion and measurement. The symmetrical design guarantees equal pulse widths among distributed modules in the motherboard. Customized isolated LDMOS devices are designed to investigate the effect of the isolation well connection and width over the ruggedness against avalanche breakdown.

SUMMARY OF RESULTS

Three types of switches with 20-V rated voltage are designed with the connection and parameters listed in TABLE I. The solid lines are implemented inside the chip via metal stacks, and the dashed line is connected through traces on the PCB board, which allows measuring one diode separately as marked in green color, namely, D2 for SW1s, and D3 for SW2s and SW3s. Due to the importance of a large dataset in reliability studies and validation of power devices, a large-scale test setup for stressing the Devices Under Test (DUTs) is necessary. Besides, it significantly reduces the testing time when several DUTs can be simultaneously stressed. A highly flexible current pulse generator (CPG) that excludes stress caused by the bus voltage is used as an electrical stress block.

The daughter board interface and one electrical stress generators (ESG) board with six submodules are implemented and illustrated in Fig. 1. A hexagonal shape is utilized to attain an equal pulse width for each of the submodules. Using the avalanche test setup, repetitive current strikes stressed the different types of LDMOS devices. A pulse width of 10 ns is selected to degrade the devices caused by the avalanche breakdown for a minimum temperature swing. This pulse also mimics an avalanche resulting from the voltage ringing during the hard switching turn-off in real applications. The key electrical parameters, including the threshold voltage (V_{th}), the body diode forward voltage (V_f), the on-state resistance ($R_{ds,on}$), and the drain-source leakage current (I_{dss}) are periodically measured over the cycles with a Keysight B1506A curve tracer. Experimental results validated the effectiveness of a symmetrical design for equal stress for each module. Customized LDMOS devices with different isolation well connections and widths reveal that the isolated well spreads the avalanche stress into a wider region and improves the robustness of devices. On the other hand, though a larger distance between the isolation n-well and substrate enhances the corresponding diode ruggedness, the device lifetime under avalanche breakdown depends on the weakest point of the devices.

Table 1. Specification of LDMOS devices.

Item	SW1	SW2	SW3
Connection			
HVNW to Sub	3µm	3µm	30µm

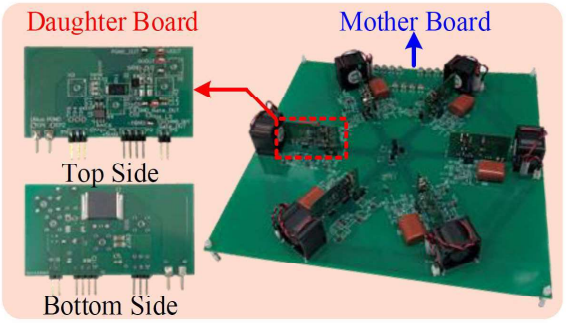


Figure 1. Hardware of one ESG board and interface to the daughterboard.

Keywords: LDMOS, reliability, avalanche breakdown, degradation mechanisms, aging precursor

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] C. Xu et al., "Performance Degradation of Automotive Power MOSFETs Under Repetitive Avalanche Breakdown Test," in *IEEE Trans. Transportation Electrification.*

TASK 2810.077, INCREASING LIFETIME OF NANO-SCALE CMOS CIRCUITS

KENNETH K. O, UNIVERSITY OF TEXAS AT DALLAS, K.K.O@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

This research seeks to increase lifetime and enable circuit operation closer to the reliability limit to improve performance. To reduce complexity and cost approaches to estimate the noise degradation using surrogate sensors will be investigated. This research may provide a step toward a framework for predicting time to failure.

TECHNICAL APPROACH

Noting that the aging of nano-scale transistors is highly variable and noise is one of the most sensitive parameters to transistor aging, this research will investigate the feasibility of increasing the lifetime of circuits by monitoring noise performance degradation and intelligent circuit reconfiguration. More specifically, PLL's and downconverters using arrays of near minimum size transistors that can be used for post fabrication selection of a subset to reduce noise will be utilized. The feasibility of replacing the transistors with increased noise due to aging with fresher transistors that have lower noise to recover the circuit noise performance will be evaluated.

SUMMARY OF RESULTS

This research effort involving collaboration with Prof. Y. Makris of UT Dallas and Prof. C. Kim of U. of Minnesota is experimentally evaluating the initial feasibility to increase lifetime by replacing the degraded devices with low noise devices that are not aged. An existing 4-GHz PLL (Fig. 1) using a VCO utilizing 64 pairs of cross-coupled pairs with a width of 250 nm and a length of 60 nm has been stressed using high DC voltage. The PLL is fabricated in 65-nm CMOS. Arbitrary combinations of 64 pairs can be selected for stressing and for VCO operation. The degradation of DC current on individual cells as well as the noise performance of the entire circuits are being characterized.

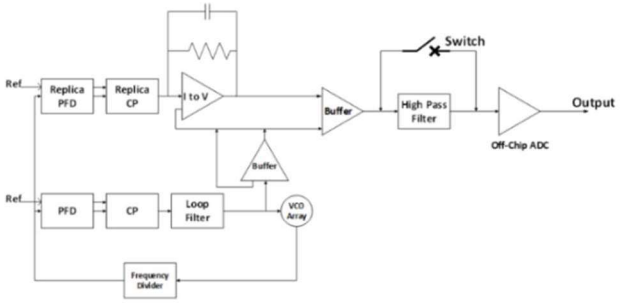


Figure 1. PLL with an on-chip phase noise measurement circuit that will be used for initial stress and heal experiments to investigate the feasibility of improving lifetime.

Fig. 2 shows the DC characteristics of 8 pairs of transistors before and after stressing at V_{DD} of 1.7 V for 24 hours. The drain current is reduced by ~12% on average. The measurement of the phase noise of VCO using these pairs as a subset however did not show any phase noise degradation after the stress. In addition to the DC stress, the PLL is being AC stressed. The circuit level degradation will be correlated with the low frequency noise degradation of individual cells. The sensitivity of the degradation of these circuits to current, supply voltage, temperature and others will be investigated.

An existing design of down-converter using an array of transistors will be refined to improve its performance. Printed circuit boards including a microcontroller and an ADC, which automate the monitoring of the degradation of down converter and the measurement circuits will be constructed and utilized for collection of history of stress over time from a large number of samples as possible during normal operation and accelerated stress testing. The data will be used to develop a machine learning model for the dependence of noise performance degradation on surrogate measurements (e.g. peak and average current, voltage, temperature and others) to define aging monitoring strategies that are more straightforward and lower cost.

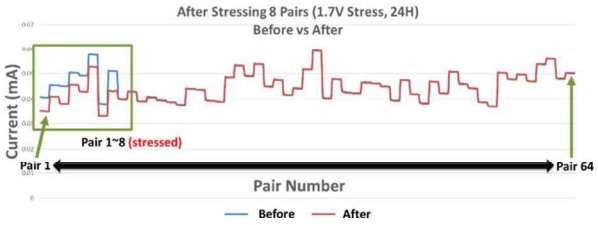


Figure 2. DC current of 64-cross coupled pairs (diode connected at DC) after stressing 8 pairs at V_{DD}=1.7 for 24 hours.

Keywords: PLL, downconverter, noise measurements, post-aging selection, lifetime

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] P. Yelleswarapu, A. Jha, R. Willis, Y. Makris, and K. K. O, "Phase Noise Reduction in LC VCO's Using an Array of Cross-Coupled Nano-Scale MOSFETs and Intelligent Post-Fabrication Selection," Accepted to IEEE Transactions on Microwave Theories and Techniques.

TASK 2810.084, SOFT AND HARD ANALOG FAULT DETECTION, INJECTION, COVERAGE, DIAGNOSIS, AND LOCALIZATION STRATEGIES SUITABLE FOR PRODUCTION TEST AND IN-FIELD TEST

DEGANG CHEN, IOWA STATE UNIVERSITY, DJCHEN@IASTATE.EDU

SIGNIFICANCE AND OBJECTIVES

Mission critical applications demand extreme reliability, mandating high electronic fault coverage. Analog circuits account for a tiny portion of transistors but a major portion of failures. This project develops cost-effective strategies for detecting soft and hard analog faults for both production and in-field testing, targeting significantly enhanced reliability and robustness.

TECHNICAL APPROACH

We will work with industry liaisons to identify the most relevant AMS-IP blocks as research vehicles. Digital-like detectors and injectors will be inserted to boost structural observability and controllability so that high defect coverage becomes possible from the digital detectors, making specification simulation unnecessary. Instead, DC parametric sweep is utilized for coverage evaluation, dramatically reducing coverage simulation time and allowing all single-defect injections evaluated for accurate coverage. Soft defects are modeled as device parametric changes or as open/shorts in sub-unit components. Detector output codes and injector input control codes will be analyzed to determine the defect location and type for diagnosis.

SUMMARY OF RESULTS

Figure 1 illustrates the proposed research. The circuit under test is a fast-transient LDO, consisting of a transient-enhanced power stage, an error amplifier with slew rate enhancement, and a bias block with reference generation. The pink gates are digital-like detectors. The two blue transistors and switches in the error amplifier are an example of digital control injections. In this case, they are used for intentional offset injections. The area overhead for the detectors and injectors is <4%. Insertion of the detectors and injector does not influence the LDO performance beyond the tolerance due to inherent local random mismatches. A single DC parametric sweep will activate all modeled defects one by one under the single defect assumption. Because of the DC nature, the coverage simulation time is very short. No LDO specification simulation is needed. Better than 95% true coverage was achieved. Because of the digital nature, the detectors and the injectors can be tested for defects using standard digital test methods. The combination of the detector output and the injector input can be used to determine the type of the simulated defect and the block where it occurred.

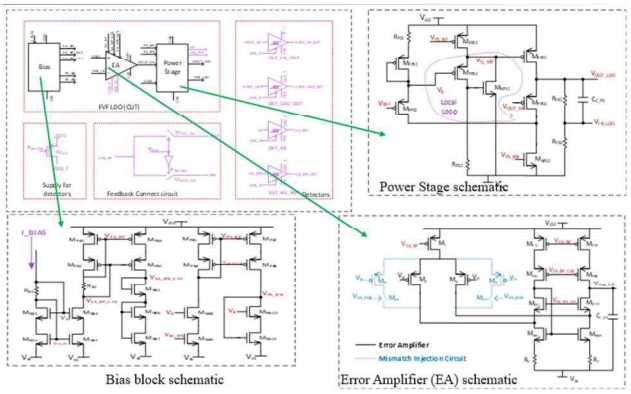


Figure 1. Analog defect detection and control injection for a fast transient LDO, achieving >95% defect coverage with <4% area overhead and no performance degradation to the original LDO.

The project plan is illustrated in Figure 2. Major anticipated results include:

- Hard and soft analog defect detection with minimal insertion impact, utilizing existing digital circuitry for mixed-signal components, and/or inserting digital-like detectors for purely analog components.
- Detection/injection code analysis algorithms for fault diagnosis and localization.
- Digitally controlled fault injection of targeted types at targeted locations for efficient silicon validation.

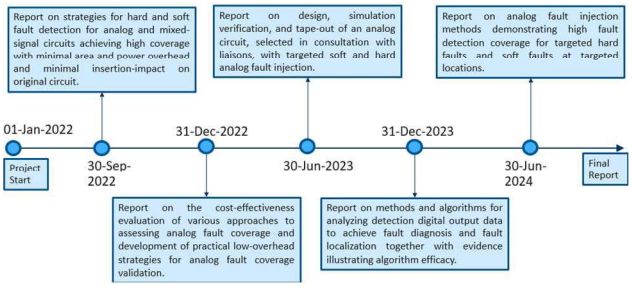


Figure 2. Project progress plan.

Keywords: Hard and soft defect detection, analog defect coverage, defect diagnosis and localization, in-field test

INDUSTRY INTERACTIONS

Texas Instruments, IBM, NXP, Intel, Mentor-Siemens

MAJOR PAPERS/PATENTS

TASK 2810.086, MACHINE LEARNING-BASED FUNCTIONAL SAFETY IMPROVEMENT OF AMS COMPONENTS IN AUTOMOTIVE SOCS

KANAD BASU, UNIVERSITY OF TEXAS AT DALLAS, KANAD.BASU@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

We propose a data-driven anomaly detection framework along with a signal selection technique for AMS Functional Safety (FuSa). Towards this end, we have developed an unsupervised learning-based framework that performs early anomaly detection in AMS circuits constituting automotive Systems-on-Chips (SoCs), which furnishes up to 100% accuracy.

TECHNICAL APPROACH

With the proliferation of safety-critical applications in the automotive domain, it is imperative to guarantee the FuSa of automotive systems. To this end, we propose a novel unsupervised learning-based early anomaly detection pertaining to AMS circuits. Our approach involves anomaly injection in various circuit locations and components to develop a training dataset encompassing a wide range of anomalous scenarios, feature extraction from observation signals, and a novel centroid selection algorithm to facilitate anomaly detection, which is tailored for detecting anomalies in AMS circuits. Furthermore, time series-based analysis is proposed to improve and expedite anomaly detection performance.

SUMMARY OF RESULTS

The overview of the proposed anomaly detection framework is illustrated in Figure 1. To ensure that the experimental setup is more relevant to the current scope and state-of-the-art systems, we have evaluated our solution using a case study of two AMS circuits commonly present in modern automotive systems-on-chips, namely bandgap voltage reference circuit and operational amplifier circuit. Moreover, four clustering algorithms have been considered: (1) k-means, (2) Gaussian Mixture Model (GMM), (3) Balanced Iterative Reducing and Clustering using Hierarchies (BIRCH), and (4) Spectral clustering. We have selected these algorithms due to proficiency in identifying outliers, robustness and scalability with an increase in data dimensionality.

From our analysis, we can infer that GMM outperforms the other algorithm in most experiments, furnishing anomaly detection accuracy up to 100% in certain scenarios. Furthermore, the centroid selection algorithm augments detection performance by up to 5% in the case of the operational amplifier circuit. Moreover, incorporating a time series-based approach improves the accuracy by up to 6.3% for the voltage reference circuit, while furnishing an accuracy of 88% for the operational amplifier circuit. Furthermore, by leveraging the temporal characteristics of the anomaly data associated with AMS circuits, we can identify anomalies early, by observing just 20% of the time period of the signal, furnishing 5X faster anomaly detection than the non-time series approach.

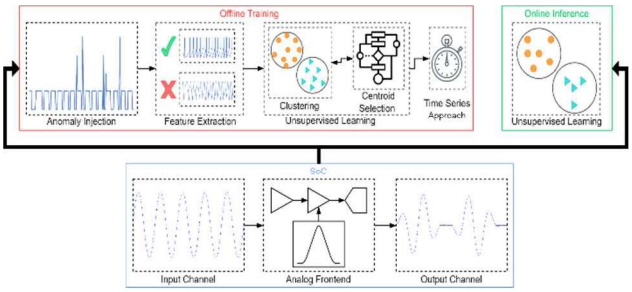


Figure 1. Overview of the proposed unsupervised learning-based anomaly detection framework.

The proposed approach, to the best of our knowledge, is the first unsupervised learning-based anomaly detection framework for AMS components of automotive SoCs. We propose a novel centroid selection algorithm to identify the ideal cluster centroids and in turn facilitate high fidelity anomaly detection. Furthermore, we propose a time series-based analysis to expedite anomaly detection by reducing the latency by 5X.

Keywords: Functional safety, unsupervised machine learning, centroid selection, time series-based approach

INDUSTRY INTERACTIONS

Intel, NXP, Texas Instruments

MAJOR PAPERS/PATENTS

TASK 2810.089, TECHNIQUES FOR LOW-COST DESIGN, TEST, AND CALIBRATION OF RF MIMO SYSTEMS

SULE OZEV, ARIZONA STATE UNIVERSITY, SULE.OZEV@ASU.EDU
GEORGIOS TRICHOPOULOS, ARIZONA STATE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

This project aims to achieve the goal of lowering the overall production cost of RF MIMO systems by developing techniques for antenna/radome design, judicious insertion of built-in self-test (BIST) and calibration components, and system level test development without requiring far-field testing.

TECHNICAL APPROACH

The proposed approach includes two phases of optimization. In Phase 1, we will develop a system level model that includes imperfections of the RF front-end as well as the antenna and radome. This system-level model will be used to determine what information can be extracted by using only mission-mode signals and what information is needed to achieve the calibration levels that satisfy system-level requirements. The second phase of optimization is to explore the design space of antenna/radome and BIST components to help identify the best solution for the target determined in Phase – 1.

SUMMARY OF RESULTS

To demonstrate how complex parameters can be de-embedded and the minimum amount of BIST components necessary can be determined, we focus on the mismatch parameters of IQ transceivers in the loop-back mode, as shown in Figure 1. Of particular concern are the phase and gain mismatches, which add up in the loop-back mode.

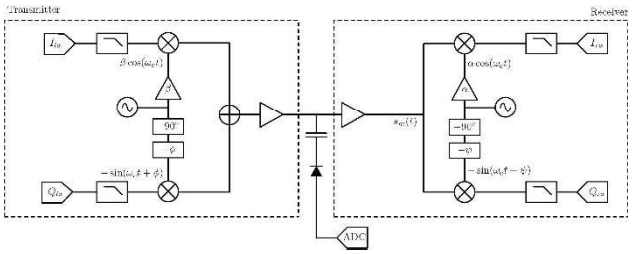


Figure 1. A transceiver in loop-back mode.

Using loop-back as a BIST approach has many advantages as negates the need for an RF signal source, which is difficult to integrate and rely on. However, the major drawback of using any kind of loop-back has been the inability to separate the transmitter imbalances from the receiver imbalances, as both contribute to the distortion linearly. The first step in solving this problem is to construct a model from baseband TX to baseband RX that includes the hardware imperfections. Then, we can identify baseband TX inputs that can provide as many linearly independent equations as possible. For instance, changing the phase of the baseband symbols adds more information, but changing simply the amplitude does not. With this input-output model, we can also easily see that regardless of the baseband input, several variables appear together, which cannot be separated without changing the structure of the system. This is where BIST is needed. To separate the unknown transmitter imbalances from the receiver imbalances, we utilize a simple power detector before the quadrature signals are separated in the mixer. This power detector enables us to normalize the received signal power, thereby eliminating the effect of the amplitude modulation due to transmitter imbalances. Since the transmitter's absolute phase is meaningless from the receiver's perspective, eliminating the amplitude variation enables us to separate the two imbalances. Hence, by analyzing what information is needed and determining the minimum effort BIST solution to extract this information, we can achieve a low-cost design that satisfies the calibration requirements.

This approach has been demonstrated using off-the-shelf components for power detection and a programmable RF test equipment as the device under test (DUT). Both TX and RX gain imbalances are swept from 0.6 to 1.6 with 0.2 steps and for each gain imbalance, the phase imbalances are swept from -10° to +10° with 5° steps, generating a data set for a diverse DUT samples. We used the TX to generate eight and sixteen equally spaced phase modulated symbols with TX impairments. The standard deviation of the error in IQ gain imbalance extraction is 0.013 and the standard deviation of the error in IQ phase imbalance extraction is 0.44°. These results are generally better compared to what has been reported in prior work while requiring far less overhead. Moreover, since this method requires no specialized test stimuli and can work with different transmitters, it can be used in the field in the background to monitor performance shifts or degradation.

Keywords: mm-wave, radar, 5G, BIST

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

TASK 2810.090, MOTOR HEALTH MONITORING

BILAL AKIN, UNIVERSITY OF TEXAS AT DALLAS, BILAL.AKIN@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

Cooling fans are one of the most critical parts of electronic systems. Bearing failure is a major failure mode caused by poor lubrication, moisture, and contamination. To avoid unexpected interruptions, we aim to propose a method to diagnose bearing faults in advance and provide an early warning signal months before a possible failure.

TECHNICAL APPROACH

This study is aimed to detect the incipient bearing faults in cooling fan motors at an early stage through motor current analysis to prevent costly shutdowns and safety issues. The main motivation behind this is to increase reliability and reduce the economic losses due to bearing failures. Typically, the commercial vibration-based bearing fault detection methods are destructive and require sensor installation on the motor. Motor current signature analysis is a condition monitoring method widely used to diagnose mechanical and electrical problems. The proposed method primarily uses thecooling fan motor current for fault detection.

SUMMARY OF RESULTS

Task 1: A modular test bench is being developed to evaluate various parameters like current, back emf, etc. of fan motors that have major bearing issues. For this purpose, several fan motors will artificially be modified to mimic common bearing faults (i.e. lubrication issues, debris and others) and the current waveforms will be recorded. Signal features will be compared to healthy versions. The tests will be repeated at different speed levels for all motors to have a comprehensive training database that includes all possible operating points. A detailed report will be presented including setup, comprehensive fault characterization of motors, key patterns, and signatures.

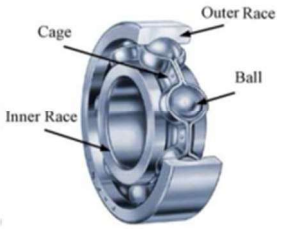


Figure 1. Bearing structure.

Task 2: The collected data will be analyzed. Pre-processed data sets will be used to understand the fault characterization of small fan motors, and common signatures and patterns will be used as key parameters of detection algorithms. In the next step, various algorithms including machine learning using time domain and frequency domain signatures will be evaluated, and the most promising ones will be identified as reliable software library for fault detection. A report and software library will be shared including all tested algorithms and their comparative performances.

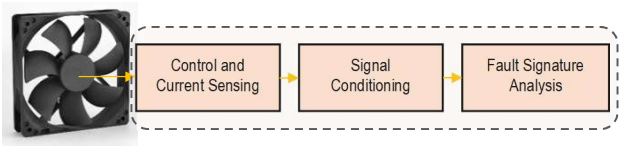


Figure 2. Fault detection prototype and concept.

Task 3: In this step, we will work on the fine-tuning and optimization of the algorithms, eliminating the effects of external vibrations or disturbances. We will also make sure that the proposed algorithms are not limited to the test motors but work with any small fan motors at any power/speed level (universal). A detailed report on testing, fine-tuning, optimization, and universalization of the proposed solutions will be shared.

Table 1. Timeline.

Timeline	Year1		Year2	
Task 1				
Task 2				
Task 3				

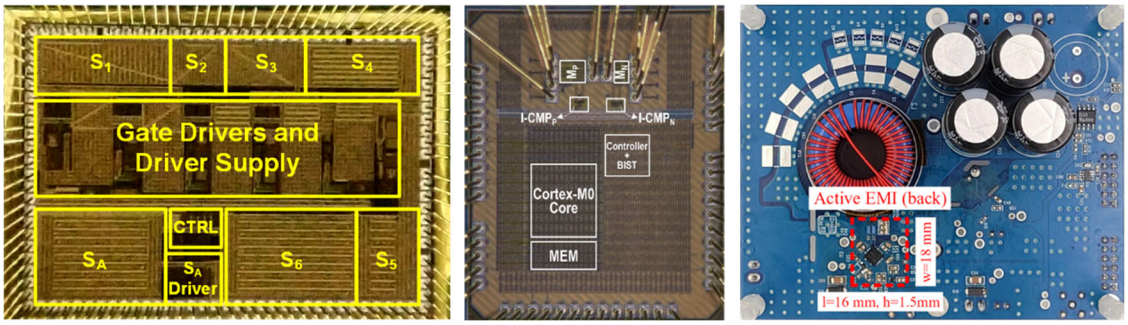
Keywords: Fan motors, bearing fault, time domain analysis, frequency domain analysis, machine learning

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

Energy Efficiency Thrust



Category	Accomplishment
Energy Efficiency (Circuits)	A 2.5–5MHz 87% peak-efficiency 48V-to-1V integrated hybrid DC-DC converter adopting a switched capacitor network with capacitor assisted dual inductor filtering has been demonstrated. The converter using a fully on-chip power NMOS is the first to achieve 48V-to-1V direct conversion with competitive power efficiencies with switching frequency in the MHz range. (2810.075, H. Lee and J. Liu, UT Dallas)
Energy Efficiency (Circuits)	Computational control is used to guide the run-time optimization of low-power duty-cycled systems which are typically used in IoT and wearable applications. The principle of optimal "regenerative breaking" is utilized to return stored domain charge into the battery instead of allowing it to leak away. The proposed technique in a 65-nm CMOS prototype improves the *overall* system efficiency by ~2X, in duty-cycled domains that perform approximately 5k computations during active mode. (2810.035, V. Sathe, University of Washington, Seattle)
Energy Efficiency (Circuits)	A 150-kHz Active EMI Filter (AEF) using a GaN-based switch-mode amplifier for high efficiency with the input voltage, V_s=120V, the output voltage, V_o=400V and P_o=320W is demonstrated. The filter achieves current attenuation of 65dB . The total volume of the proposed AEF is 0.1in^3 which is equal to 1/32 of the volume of the size-optimized LC filter for the similar current attenuation. This AEF with a smaller size and higher efficiency is a promising solution to replace the passive LC filter and linear-mode AEF. (2810.068, A. Hanson, U. of Texas at Austin)
Energy Efficiency (Circuits)	A fully digital in-memory computing chip (DIMC) achieving 2219 TOPS/W and 2569F^2/b is demonstrated. Full digital implementation mitigates the PVT variation issue. Approximate arithmetic hardware is utilized to improve area and power efficiency. Additionally, approximation-aware training and custom data format are utilized to minimize inference accuracy degradation due to approximation. (2810.034, M. Seok, Columbia University)

TASK 2810.012, NPSENSE – NANO-POWER CURRENT SENSING

KOFI A. A. MAKINWA, TU DELFT, K.A.A.MAKINWA@TUDELFT.NL

SIGNIFICANCE AND OBJECTIVES

Battery fuel gauges usually employ a shunt-based Current-Sensing System (CSS). State-of-the-art CSSs consume µWs of power to achieve the required performance. However, many IoT or wearable applications require power consumption in the sub-µW range. This project aims to develop nano-power CSSs suitable for battery fuel gauges.

TECHNICAL APPROACH

Continuous-Time Delta-Sigma Modulators (CTΔ∑Ms) is a good choice for this task since they have relaxed settling requirements and thus dissipate less power than discrete-time ∑ΔMs. Using a VCO as a phase quantizer instead of a typical continuous-time integrator allows multi-bit quantization and lower supply voltage, which improves energy efficiency. Further reduction in power consumption can be achieved by designing a voltage reference responsible for the shunt temperature dependence compensation, avoiding the necessity of a temperature sensor.

SUMMARY OF RESULTS

The block diagram of the proposed current sensor is shown in Fig. 1. An ADC uses a temperature-dependent V_{REF} to digitize the voltage V_S across a shunt. $V_{REF} = V_{PTAT}+V_{CTAT}/\lambda$ where λ can be tuned to match the shunt's TC. Two different shunt types are used in this work: a 10 mΩ on-chip shunt based on four metal layers, and a 300 µΩ on-package shunt.

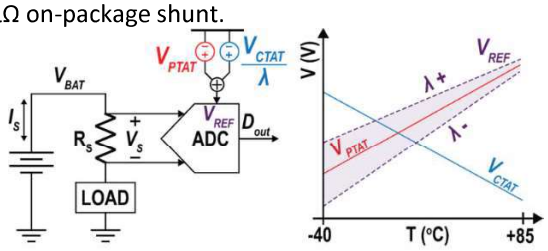


Figure 1. System block diagram.

The V_{CTAT}/λ portion of the voltage reference is obtained by inserting a CTAT resistor in series with a DTMOS based V_{PTAT} voltage generator, Fig. 2. DTMOS transistors were chosen instead of BJTs to allow low supply voltage (<1V) operation.

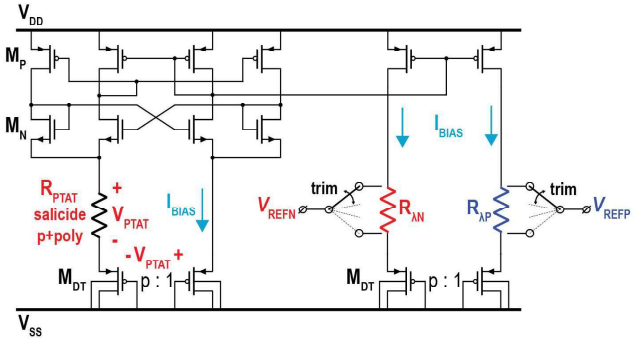


Figure 2. Voltage reference generation.

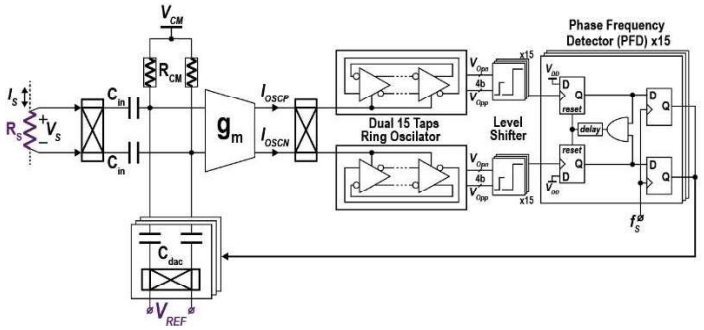


Figure 3. Architecture of the current sensor.

Fig. 3 shows a block diagram of the readout circuit. It is based on a 1st order ΔΣ ADC which has a uniform impulse response and a time-independent response to input pulses. The loop filter is a g_m + CCO with pseudo differential phase quantization. The phase quantization turns the g_m + CCO into an integrator with a multi-bit quantization which improves the SQNR of the overall system and, more importantly, reduces the error signals into the loop filter. This allows the use of an open-loop g_m stage in the summing node of the ΔΣ ADC. The circuit is capacitively coupled, allowing high ICMR (15 V in this design) while the circuit operates by a low supply voltage (<1V).

The circuit is in tape out phase and the expected performance is summarized in Table 1.

Table 1. Comparison Table.

	This Work		Zamparette VLSI 21		Xu SSCL 18		Vroonhoven ISSCC 20
PSUPPLY	600 nW		2.5 µW		24.5 µW		< 8.5 µW
Gain Error	on-chip	±0.3%	on-chip	±0.35%	PCB Trace	±0.35%	±0.5%*
	on-package	±0.3%	PCB trace	±0.6%			
IRANGE	on-chip	± 1 A	on-chip	±2A	PCB Trace	±12A	±1A
	on-package	± 30 A	PCB trace	±15A			
Shunt	on-chip	10 mΩ	*on-chip*	20 mΩ	PCB Trace	1 mΩ	50 mΩ*
	on-package	300 µΩ	PCB trace	3 mΩ			
Offset	on-chip	< 50 µA	on-chip	25 µA	PCB Trace	40 µA	< 100 µA
	Package	< 5 mA	PCB trace	100 µA			
ICMR	15 V		5 V		25 V		60 V
VSUPPLY	< 1.0 V		1.8 V		1.8 V		1.7 to 60 V
Res.	4.5 µVRMS		5.4 µVRMS		1.5 µVRMS		-
TCONV	3 ms		15 ms		2 ms		-
FOM°	176 dB		149 dB		162 dB		-
Tech.	0.18		0.18		0.18 BCD		0.18 BCD

° FOM = Dynamic Range +10log (Bandwidth/Power)

* Uses a custom/off-chip low-TCR shunt

§ Uses an extra ADC for temperature sensing allied to an extensive calibration.

Keywords: current sensing, VCO based, multibit, low-power

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

[1] R. Zamparette and K. Makinwa, "A ±2A/15A Current Sensor with 1.4 µA Supply Current and ±0.35%/0.6% Gain Error From −40 to 85 °C using an Analog Temperature-Compensation Scheme," in IEEE Symposia on VLSI 2021.

TASK 2810.032, DRIVR: A DIGITAL, RE-CONFIGURABLE, UNIFIED CLOCK-POWER (UNICAP) FABRIC FOR ENERGY-EFFICIENT SOCS

VISVESH S. SATHE, UNIVERSITY OF WASHINGTON, SEATTLE, SATHE@UW.EDU

SIGNIFICANCE AND OBJECTIVES

Integrated Voltage Regulation (IVR) -- remains a critical technology for driving sustained efficiency in SoCs, offering buck converter efficiencies without additional bulky components. The objective of this effort is to devise a domain-scalable run-time programmable IVR fabric that drives and leverages advances in adaptive clocking and SIMO design (Fig. 1).

TECHNICAL APPROACH

The design effort is organized into four thrusts (1) analyzing the effectiveness of UniCaP in designs with large insertion delay; (2) Demonstrate domain-scalable SIMO implementation, critical to providing the necessary flexibility required for a dynamically programmable IVR fabric; (3) Investigating optimal design-time cross-bar switch allocation which connects modules to domains based on SoC usage profiles; and (4) Designing a tileable buck architecture and that can be configured at run-time either as a single-buck, a phase in a multi-phase buck, or a SIMO converter. The goal of the effort is to implement a test chip demonstration that incorporates all four efforts.

SUMMARY OF RESULTS

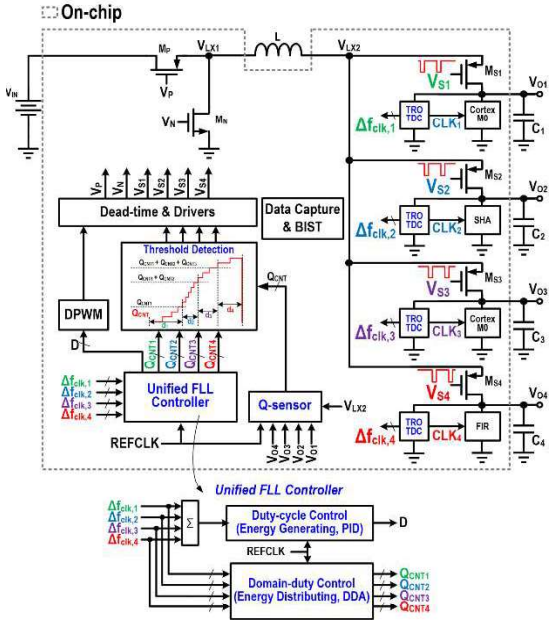


Figure 1. Implemented SIMO-regulated SoC featuring UniCaP and Dynamic Droop Allocation (DDA) for concurrent domain control to address cross-regulation.

Goals 1 and 2 of our technical approach have been accomplished – we recently successfully implemented a SIMO-regulated SoC that avoids the prohibitively large V_{DD} margins required in prior implementations (Fig. 2). We have also developed mechanisms to enable "hot-swapping" load modules across voltage domains.

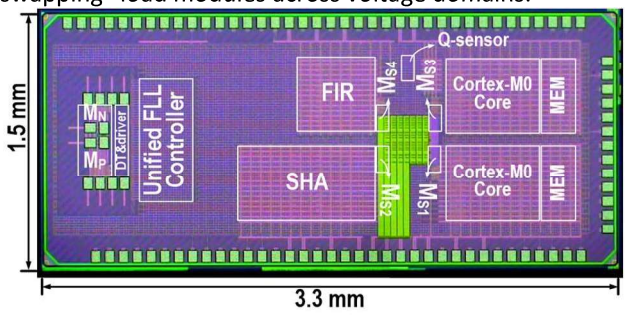


Figure 2. Die photograph of the implemented low-V_{DD} droop margin SIMO regulated SoC consisting of two processor and two accelerator domains.

We are currently working toward the design of a silicon prototype of the proposed DRIVR fabric. The design will feature two configurable buck tiles, and four load domains. The tiles can be configured to operate either as two buck voltage domains, a single two-phase buck domain or a buck-SIMO regulator pair. Similarly, load modules can be configured to be connected to each domain using a configurable power switch. The power switch can be configured as a low-resistance header switch, a digital LDO, or the access device of a SIMO design.

Keywords: UniCaP, SIMO, Configurable Voltage Regulation

INDUSTRY INTERACTIONS

NXP, Intel, ARM

MAJOR PAPERS/PATENTS

[1] Huang, C-H et al., "A Single-Inductor 4-Output SoC with Dynamic Droop Allocation and Adaptive Clocking for Enhanced Performance and Energy Efficiency in 65nm CMOS," ISSCC 2021.

[2] Sun, X. et al., "*UniCaP-2: Phase-Locked Adaptive Clocking with Rapid Clock Cycle Recovery in 65nm CMOS*," VLSI Symposium 2020.

TASK 2810.034, ALWAYS-ON KEYWORD SPOTTING BASED ON ANALOG-MIXED-SIGNAL COMPUTING HARDWARE

MINGOO SEOK, COLUMBIA UNIVERSITY, MGSEOK@EE.COLUMBIA.EDU

SIGNIFICANCE AND OBJECTIVES

The primary goal of the project is to create hardware-design knowledge and techniques on analog-mixed-signal (AMS) hardware for artificial intelligence (AI) and machine learning (ML) related computing. Specifically, we will create AMS hardware that can significantly benefit scaling power consumption in acoustic signal classification tasks.

TECHNICAL APPROACH

We will conduct the planned research as follows: (i) We will design *new feature extraction AMS hardware that uses non-linear circuits*. (ii) We will develop a compact model of the non-linear AMS hardware, and by using the developed compact model, we will develop *a training model that can effectively tolerate the variability of AMS computing hardware*. (iii) We will design a matching back-end *classifier based on a deep neural network (DNN)*. We will develop the digital circuits to map the model at minimal leakage/power consumption. By combining the developed architecture/techniques, we will prototype one test chip for the AMS front end and another for the end-to-end multi-keyword recognition systems.

SUMMARY OF RESULTS

Last year, we have designed, prototyped, and tested energy- and area-efficient digital in-memory-computing hardware and published the results in [1]. The key task was to design and tape out a digital in-memory-computing (DIMC) macro based on approximate arithmetic hardware.

In-memory-computing (IMC) SRAM architecture has gained significant attention as it achieved high energy efficiency for computing a convolutional neural network (CNN) model. Most of the recent works, including our past works, have investigated the use of analog-mixed-signal (AMS) hardware in the IMC SRAM architecture.

AMS IMC hardware has achieved high area and energy efficiency. However, the computation results of AMS hardware vary across process, voltage, and temperature (PVT) variations, limiting the computing precision and ultimately the inference accuracy of a CNN. We reconfirmed, through simulation of a capacitor-based IMC SRAM macro that computes 256-d binary dot products. The AMS computing hardware has a significant root-mean-square error (RMSE) of 22.5% across the worst-case voltage, temperature (Fig. 1 top left) and 3-sigma process variations. Instead, *digital* IMC (DIMC) hardware can virtually eliminate the variability, but digital circuits require more devices than AMS counterparts for an arithmetic function, often resulting in poor area efficiency.

In [1], we leveraged approximate arithmetic hardware to improve area and power efficiency and present two versions of digital IMC macros with different levels of approximation. Fig. 2 shows the architecture of DIMC.

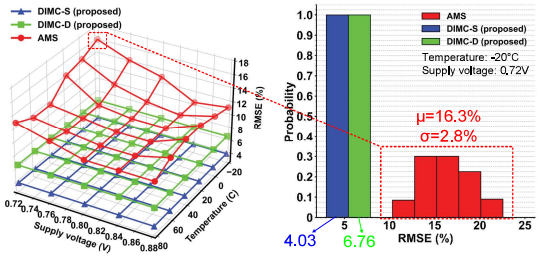


Figure 1. Proposed DIMC hardware achieves the low RMSE (left) across a wide range of temperature, supply voltage, and (right) process variation compared with an AMS IMC.

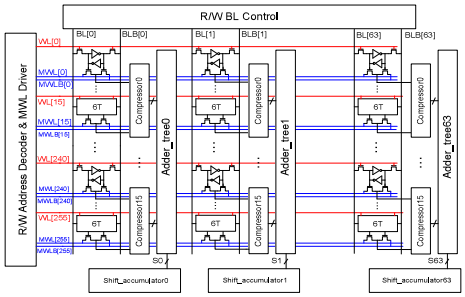


Figure 2. Architecture of the DIMC chip.

To compensate the error caused by approximate arithmetic hardware, we leveraged an approximation-aware training method and a custom data format. DIMC-D (DIMC-S) achieves CIFAR-10 accuracy of 87.0% (90.4%). We measured two macros at 0.5V–1.1V at 25°C. DIMC-D (DIMC-S) achieves the maximum energy-efficiency of 2219 TOPS/W (990 TOPS/W).

Keywords: IMC hardware, digital computing hardware, approximate arithmetic hardware, convolutional deep neural networks

INDUSTRY INTERACTIONS

Intel

MAJOR PAPERS/PATENTS

[1] D. Wang, et al., "DIMC: 2219 TOPS/W, 2569 F^2/bit, Digital In-Memory-Computing Macro…," ISSCC, 2022.

TASK 2810.035, COMPUTATIONALLY CONTROLLED INTEGRATED VOLTAGE REGULATORS

VISVESH S. SATHE, UNIVERSITY OF WASHINGTON, SEATTLE, SATHE@UW.EDU

SIGNIFICANCE AND OBJECTIVES

The enhanced spatio-temporal control afforded by Integrated Voltage Regulation (IVR) in modern SoCs is critical to achieving efficiency, provided they can maintain or improve voltage droop despite reduced available decap. This effort examines computationally intensive IVR control strategies to improve the robustness and settling times of buck and LDO designs.

TECHNICAL APPROACH

The design effort is organized into two key thrusts: (1) Using "computational control" to achieve time-optimal transient response to random switching load current profiles typical of SoCs, and (2) Addressing a key weakness in digital LDOs – their prohibitive Power Supply Rejection performance – to advance the state of the art in the transient response of digital LDOs. The main approach toward Thrust 1 will be to evaluate the use of Model Predictive Control (MPC) for a rapid transient response. This effort seeks to demonstrate the effectiveness, and the limits of more advanced control strategies on regulator design through test-chip demonstrations using 65-nm CMOS.

SUMMARY OF RESULTS

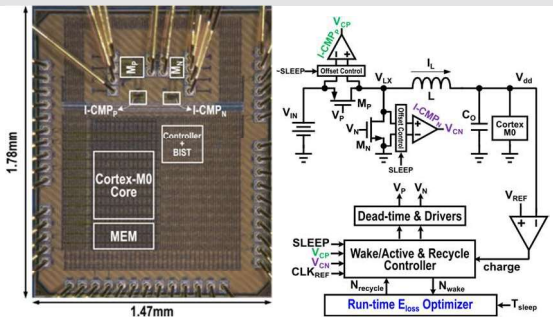


Figure 1. Autonomous "Regenerative Breaking" SoC, computationally determines the optimum amount of energy recovery from the load domain (C_0).

We have already realized our objective of demonstrating the effectiveness of computational control under tight latency constraints by demonstrating MPC for a buck regulator in 2021. In consultation with our liaisons, we have determined from our simulations that computational approaches to low-PSRR digital LDO have not proven to offer sufficient value in large part due to the need for aggressive over-sampling of V_{in}. We have instead continued our efforts on computationally controlled IVR but in the context of run-time optimization of low-power SoCs. In particular, we have demonstrated regenerative breaking, a technique that recovers the energy that is otherwise wasted in the load capacitance of duty cycled systems during their transition to steady state Sleep mode (Fig. 1).

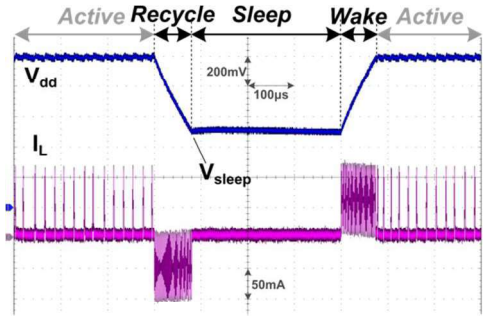


Figure 2. Measured waveforms showing the operation of regenerative breaking. Before entering *Sleep* mode, the design enters a *Recycle* phase, where energy stored in C_0 is recycled into the supply to save energy.

Fig. 2 shows measured waveforms of our proposed approach. The proposed technique is shown to improve the *overall* system efficiency by nearly 2X, in duty-cycled domains that perform approximately 5k computations during *Active* mode. These savings are reflected in measured energy dissipation data shown in Fig. 3.

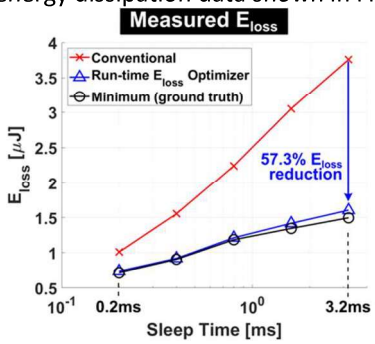


Figure 3. The proposed computationally guided autonomous "Regenerative Breaking" SoC (blue) enables operation near the optimum (black) efficiencies that are significantly better than that of conventional (red) approaches.

Keywords: Model-predictive control, Voltage Regulation

INDUSTRY INTERACTIONS

Intel, NXP, ARM

MAJOR PAPERS/PATENTS

[1] Huang, C-H et al., "Energy Minimization of Duty-Cycled Systems Through Optimal Stored-Energy Recycling from Idle Domains," ISSCC, vol. 65, pp. 222-224. IEEE, 2022.

TASK 2810.039, DEVELOPMENT OF COMPACT AND LOW COST FULLY INTEGRATED DC-DC CONVERTER WITH RESONANT GATE DRIVE AND INTELLIGENT TRANSIENT RESPONSE

JIE GU, NORTHWESTERN UNIVERSITY, JGU@NORTHWESTERN.EDU

SIGNIFICANCE AND OBJECTIVES

Fast and intelligent transient response is a critical specification for fully integrated voltage regulators. In this project, we seek to develop an intelligent transient response technique for a fully integrated DC-DC converter using novel machine learning techniques and event-based control rendering enhanced power efficiency and fast transient response for use in microprocessors.

TECHNICAL APPROACH

In this project, we incorporate modern machine learning techniques to realize intelligent transient responses for fully integrated buck converters. Two novel techniques are developed. First, a linear regression-based machine learning technique is used as a real-time feedforward control method to regulate load transients from a CPU on a chip. The model is trained based on real-time operational features, e.g., Opcode from CPU, and simulated CPU's transient current profile. Second, to overcome the false prediction of the machine learning technique, event-based droop control is developed as a "safety net" to maintain the output voltage within the acceptable voltage range of the CPU.

SUMMARY OF RESULTS

For the first time, we utilized a real-time machine learning technique to learn the relationship between supply droop and CPU's operating condition. The predicted voltage from the machine learning core is used to modify the PWM control signal of the buck converter, which in our case runs at 0.8~1GHz similar to the speed of the CPU implemented on the chip. A 65-nm test chip for the demonstration of the technique has been taped out in May 2022. Fig. 1(a) shows the architecture of the key modules in the test chip. Fig. 1(b) shows the layout of the test chip with a total dimension of 1.9mm by 2.0mm. A RISC-V CPU is implemented as both the current load and prediction target of our machine learning controller. A smaller version of a previous buck converter is implemented to provide adequate regulation of the output voltage between 0.9V to 1.2V from a 1.8V input voltage. A linear regression-based machine learning model is trained using simulation from ASIC design and Analog Mixed-signal design, which captures the relationship between CPU's current consumption and CPU's internal signals, e.g., Opcode. The machine learning core proactively generates prediction of CPU's current consumption 2 cycles later. The prediction result is sent back to the buck converter and combined with real-time measured supply voltage to deliver "feedforward" regulation to the incoming current surge.

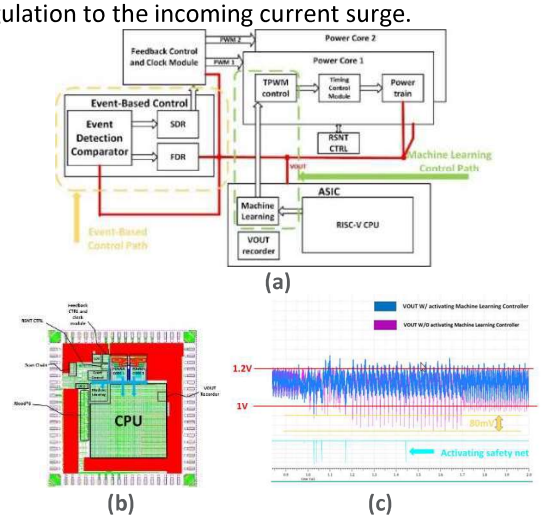


Figure 1. (a) Architecture of the test chip; (b) Layout of the test chip; (c) Simulated Vout w/ or w/o machine learning controller.

To deal with the inaccuracy of machine learning prediction, an event-based control scheme is also developed serving as "safety net" for V_{min} and V_{max} requirement of the CPU. In the event-based control module, a number of fast comparators are used to detect supply voltage value at the output. Two regulation modules, i.e., fast droop response (FDR) and slow droop response (SDR) are developed to provide regulation to either cycle-by-cycle fast current transient or slower but larger current load change from the CPU. As shown in Fig. 1(b), after activating the machine learning prediction and event based "safety net," an 80-mV improvement on supply transient variation is observed. The chip is expected back in the summer of 2022.

Keywords: fast transient response of regulator, machine learning, event-based feedback control, RISC-V CPU

INDUSTRY INTERACTIONS

Texas Instruments, IBM, Intel

MAJOR PAPERS/PATENTS

TASK 2810.040, HYBRID/RESONANT SC CONVERTERS WITH INTEGRATED LC RESONATOR FOR HIGH-DENSITY MONOLITHIC POWER DELIVERY

JASON T. STAUTH, DARTMOUTH COLLEGE, JASON.T.STAUTH@DARTMOUTH.EDU

SIGNIFICANCE AND OBJECTIVES

Fully-integrated power management is important for a variety of computing and communication applications but is difficult due to the limitations of on-chip passive components. This project explores a new direction using distributed LC-resonators in hybrid switched capacitor architectures to mitigate high-frequency losses and improve efficiency and power density.

TECHNICAL APPROACH

This work involves co-optimization of high-frequency DC-DC converters based on hybrid-resonant switched capacitor architectures and distributed planar-spiral LC resonators. A variety of analytical and numerical methods are used to model skin- and proximity-effect losses in planar magnetics which use capacitive dielectrics to ballast and homogenize current density. Several circuit topologies are under study spanning nominal 2:1 resonant converter as well as higher conversion ratios using Series-Parallel and Dickson architectures. The project involves integrated circuit design with tapeouts completed in Cadence, and electromagnetic design using Sonnet and Maxwell. Key deliverables include circuit architectures and blocks, electromagnetic models, and component optimization methods.

SUMMARY OF RESULTS

This work builds on the past efforts in fully-integrated voltage regulation (FIVR), with specific aims to 1) improve passive component utilization through the use of electromagnetic ballasting, 2) leverage new architectures that benefit from high energy-density on-chip capacitors, and 3) explore new on-chip control, regulation, and timing optimization such as autotuned zero-current and voltage switching. A theoretical analysis was presented in [2] which outlines certain design tradeoffs and optimization procedures, verified by EM simulation and measured data. A prototype tapeout was completed in March 2021

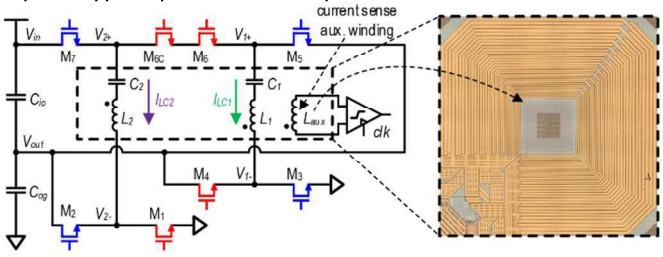


Figure 1. Scaling analysis: required on-chip die area decreases significantly with advanced process technologies, from [1].

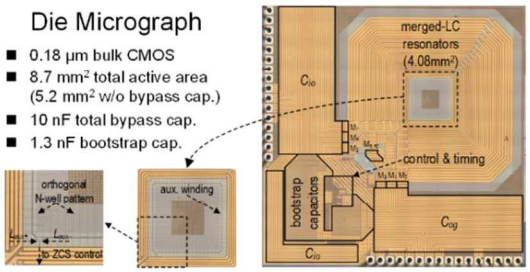


Figure 2. Feb 2022 ISSCC Prototype: Die Micrograph.

(highlighted in Figs. 1 & 2). This tapeout comprised a nominally 3:1 hybrid Dickson converter. A paper detailing the design was published at ISSCC 2022 [1].

The 3:1 Dickson converter used the merged-LC concept, demonstrating a fully integrated resonator and operating at ~30MHz. The design achieved peak efficiency of >78% with voltage conversion from 3.7V to 1.2V with no off-chip components. Regulation used a dynamic off-time control scheme to demonstrate fast transient response (<50mV over/undershoot @40mA, 12.5µs load step). An integrated zero-current detection and regulation scheme used an on-chip auxiliary winding to directly measure magnetic field in the merged resonator. This scheme was able to accurately auto-tune the zero-current switching state with low power overhead. New gate driving and bootstrapping circuits were designed to drive floating power devices accurately and with low latency at 30-50MHz. The design was implemented in 180-nm bulk CMOS, but the concepts should also be applicable to more advanced nodes.

Keywords: Power Management, DC-DC Converters

INDUSTRY INTERACTIONS

NXP, Intel, Texas Instruments

MAJOR PAPERS/PATENTS

[1] P. H. McLaughlin et al., "A Monolithic 3:1 Resonant Dickson Converter with Variable Regulation and Magnetic-Based Zero-Current Detection and Autotuning," ISSCC 2022.
[2] P. McLaughlin, et al., "Modeling and Design of Planar-Spiral Merged-LC Resonators in a Standard CMOS Process," IEEE COMPEL 2020.
[3] P. McLaughlin, et al., "A Fully Integrated Resonant Switched-Capacitor Converter with 85.5% Efficiency at 0.47W Using On-Chip Dual-Phase Merged-LC Resonator," ISSCC 2020.

TASK 2810.042, DIGITALLY ENHANCED HIGH EFFICIENCY, FAST SETTLING AUGMENTED DCDC CONVERTERS

BERTAN BAKKALOGLU, ARIZONA STATE UNIVERSITY, BERTAN.BAKKALOGLU@ASU.EDU

SIGNIFICANCE AND OBJECTIVES

State-of-the-art digital loads impose challenging requirements for power-supply regulators to provide fast-transient currents. Fast-transient response improvement techniques utilizing auxiliary circuits become popular due to their enhanced efficiency and design flexibility. Our goal is to break the efficiency/dynamic-response/settling-time trade-off in conventional DC-DC converters, by developing high-speed, digitally controlled augmented power stages with optimal load current control and settling time.

TECHNICAL APPROACH

In the proposed augmented power converter topology, an auxiliary stage with a small inductor, and a high switching rate converter share the load capacitor with the main stage providing fast settling under fast-load-transients. We will develop an observer-based load capacitor current estimator to control the auxiliary stage, having it work as a Current-Controlled-Current-Source. Given the specific supply-voltage regulation window, this system achieves an integrated solution that requires a smaller (3~4x) external capacitor size that lowers cost.

SUMMARY OF RESULTS

During system-level design, different control schemes (PWM, hysteretic, Constant-On/Off-Time) and control modes (voltage mode, current mode, emulated current mode) for the main stage have been analyzed in terms of settling speed and stability. Digital nonlinear controls (single-cycle, multi-cycle, or multiple-single-cycle correction) for the aux stage have been investigated. VerilogAMS models are used to build the transient detector and control logic. The timings for digital control (t_1, t_2, t_3) are computed in an analog way for high cost/energy efficiency. Transistor-level schematic design is completed. The full layout is completed. The final GDS file is lvs/drc passed and ready for fabrication. Post-layout simulations are done and compared with the pre-simulation results. Layout parasitics are well under control. The buck converter die top layout view is shown below. The die size is 2.5mm x 3mm.

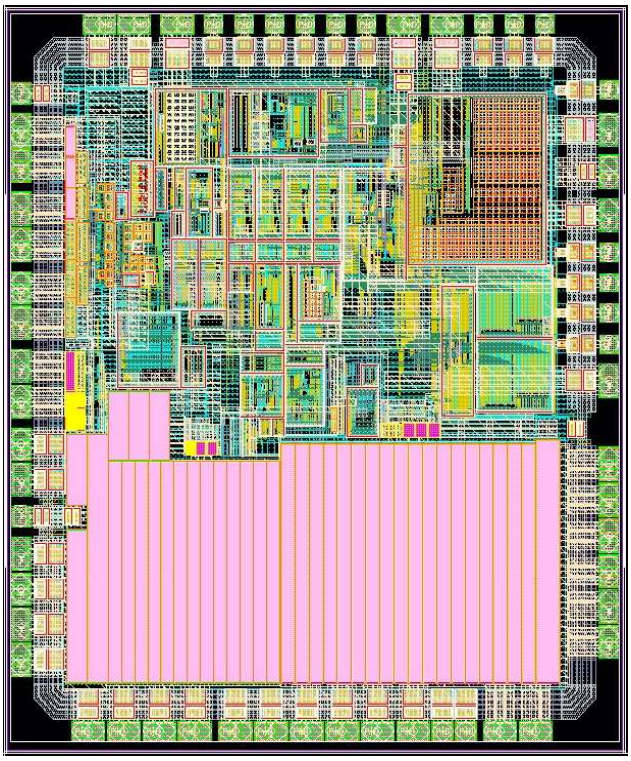


Figure 1. Final layout view of the buck_converter_die_top.

Load transient of 5A step-up/down load current is applied to check the transient response. The results are summarized below in Table 1.

Table 1. Load Transient Response results summary.

	ΔV_{out} (+5A/-5A)	t_{settle} (+5A/-5A)
w/o msc_nlc	48mV/145mV	9.5us/14.3us
w/ msc_nlc	12mV/35mV	3us/7.6us
w/ msc_nlc and brake-diode	12mV/28mV	3us/4us

Keywords: augmented converter, fast transient detector, fast settling, high efficiency, digital nonlinear control

INDUSTRY INTERACTIONS

NXP, Intel, IBM

MAJOR PAPERS/PATENTS

TASK 2810.049, 1-W BATTERY-CHARGING CMOS BUCK REGULATOR

GABRIEL A. RINCÓN-MORA, GEORGIA TECH, RINCON-MORA@GATECH.EDU

SIGNIFICANCE AND OBJECTIVES

Charging batteries (in cell phones) with other batteries (battery banks) is the new normal. Volume and charge life are critical in this space. The objective of this research is to develop a small and power-efficient single-inductor voltage regulator that also charges and conditions a battery for maximum energy.

TECHNICAL APPROACH

Charging dynamics in Lithium-Ion batteries are largely unaccounted for by conventional chargers, so they do not charge them maximally. The first step in this research is to study, test, and develop charging methods that expand usable energy storage. The second step is to develop an efficient power supply that charges a battery and supplies a load with one inductor. To preserve energy, power flow in all directions should be efficient: input-output, input–battery, and battery–output. The third step is to develop an efficient controller that supplies and regulates the output while charging and conditioning the battery for maximum energy.

SUMMARY OF RESULTS

Experiments on optimal charge current profiles are completed. Three Li-ion batteries are tested using the battery tester in [1]. The charge current profile is varied while the discharge current profile is controlled. The investigated charge current profile is an ac ripple superimposed on a dc current. The parameters varied are the dc current amplitude $i_{B(DC)}$, ac ripple shape (sine/square/triangle), frequency f_{AC}, amplitude $i_{B(AC)}$, and application region (pre-condition/main charge).

The performance of charge profiles is indicated by energy efficiency change $\Delta\eta_E$, which is the percentage efficiency increase relative to a DC current charge. Across over 400 charge-discharge cycles, no significant improvement is observed by varying the ac ripple. Figure 1 shows the results for Panasonic NCR18650B when the applied ac ripple is sinusoidal (left) and square (right). The resulting $\Delta\eta_E$ is less than ±0.1%. It can be concluded that ac ripples in charge current have negligible effects on the battery's usable energy.

Therefore, i_B does not need to be regulated when it does not exceed the maximum limit. A single-inductor battery-charging/sourced voltage regulator is proposed as shown in Fig. 2, which enables the battery to be connected in series with the output when M_{BO} is on. As current is supplied to the load, the battery is automatically charged.

The power stage can be configured as a buck/buck–boost to deliver power in all directions efficiently: v_I to v_O, v_I to v_B, v_I to (v_B + v_O), and v_B to v_O. The advantage of this power stage includes reduced control complexity, higher efficiency, smaller footprint, and lower cost. The power stage is currently being designed, simulated, and implemented. Design of the feedback controller, which regulates v_O and charges the battery, will follow.

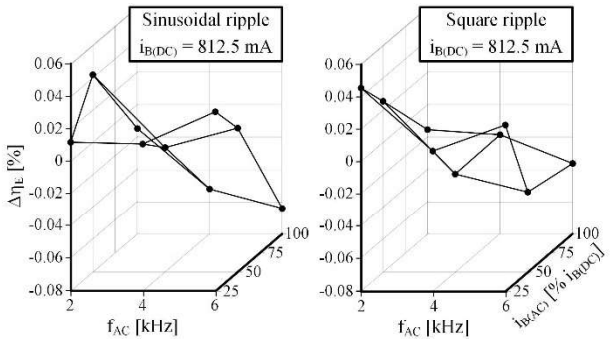


Figure 1. Effect of i_B ripple on the battery's usable energy.

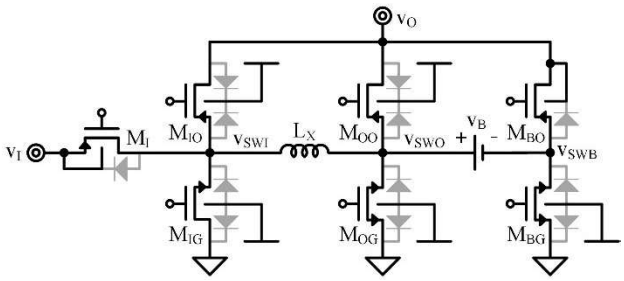


Figure 2. Single-inductor battery-charging voltage regulator.

Keywords: Li-ion charger, voltage regulator, efficiency

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] Q. Zhi, G. A. Rincón-Mora and P. Gu, "Autonomous and Programmable 12-W 10-kHz Single-Cell Li-Ion Battery Tester," accepted to *IEEE TIM*.

TASK 2810.051, HIGH GAIN DC-DC CONVERTER FOR EV TRACTION SYSTEM

RAJA AYYANAR, ARIZONA STATE UNIVERSITY, RAYYANAR@ASU.EDU

SIGNIFICANCE AND OBJECTIVES

Experimental validation of a multi-input, high-conversion-ratio DC-DC converter for electric vehicle traction systems involving a low-voltage battery pack and a variable DC link voltage is achieved. The proposed architecture increases safety, minimizes cell balancing issues in the battery, eliminates the need for an auxiliary DC-DC converter, and improves the overall efficiency of the system.

TECHNICAL APPROACH

In EV traction systems, higher voltage motors offer improved efficiency and power density. Variable DC link voltage improves the overall efficiency of the traction system. The proposed multi-input high conversion ratio converter (HCRC) can achieve high and variable voltage gain (4 to 20 times for a 4-phase converter) with a significant reduction in voltage and current stress across its devices. This enables use of a 48-V battery pack which significantly increases the overall safety. Each phase of HCRC is connected to a separate battery module whose charging-discharging can be independently controlled to achieve cell balancing easily.

SUMMARY OF RESULTS

Figure 1 shows one of the configurations of the proposed architecture for 48V to >800V variable DC link conversion. A scaled hardware prototype of a 4-phase multi-input HCRC is developed to verify the proposed concept. The prototype is rated for 4kW (each module) operating at 48-V input. The output voltage can vary from 200V to 800V achieving a conversion ratio of 4 to 17 without any transient spikes in switch voltage or current.

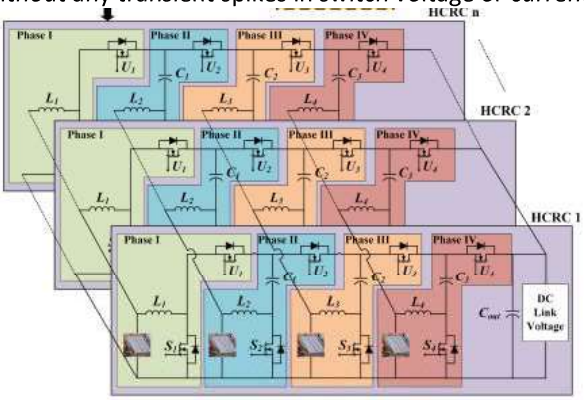


Figure 1. One of the configurations of the proposed 4-phase multi-input high conversion ratio converter for EV traction systems.

Multiple possible configurations of HCRC in parallel have been derived and verified in simulation and hardware experiments. The configurations include interleaved and non-interleaved connections of HCRC with different battery modules. A sample design of the proposed architecture corresponding to the Chevrolet Bolt battery pack has also been published.

The HCRC operation is verified experimentally through a scaled hardware prototype for both interleaved and non-interleaved configurations. The hardware prototype is operated in dual-loop control with an inner current loop and an outer voltage loop. The inner current loop regulates the current supplied by each input source while the voltage controller regulates the output voltage to the desired value. The converter can operate at both equal and unequal current sharing among the different input phases over the whole range of operation with the output voltage regulated to the desired value. The converter has bi-directional power flow capability allowing it to operate in buck mode during regenerative braking in an electric vehicle. The converter operation in both boost and buck mode is verified experimentally using the hardware prototype.

As the converter has low voltage stress across the devices, 650 -V SiC MOSFETs are selected which have low on-state resistance to minimize the conduction losses. The converter can achieve a peak efficiency of 98.36% at 400V, 2-kW output with a switching frequency of 50 kHz. The converter has similar performance results in buck mode with 98.16% efficiency for 400V to 48V operation at 2kW. With interleaved configuration, the net inductor size reduces by 55% with a slight increase of overall efficiency.

Keywords: DC-DC Converter, High Gain, Non-isolated boost, Variable DC link, EV Traction

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] A. Gupta, R. Ayyanar and S. Chakraborty, "Novel Electric Vehicle Traction Architecture with 48 V Battery and Multi-Input, High Conversion Ratio Converter for High and Variable DC-Link Voltage," in IEEE Open Journal of Vehicular Technology, pp. 448-470, 2021.

[2] A. Gupta, R. Ayyanar and S. Chakraborty, "Soft-Switching Mechanism for a High-Gain, Interleaved Hybrid Boost Converter," in IEEE Journal of Emerging and Selected Topics in Ind. Electronics, pp. 420-430, Oct. 2021.

TASK 2810.055, EMI-REGULATED SECURE AUTOMOTIVE POWER ICS

D. BRIAN MA, THE UNIVERSITY OF TEXAS AT DALLAS, BRIAN.MA@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

Today EMI remains a critical design challenge in power electronic circuits. With ever-growing deployment of electronic devices, electromagnetic interference (EMI) emission in modern automotive electronics is record-high. The situation deteriorates further due to high *dv/dt* and *di/dt* transients, as more high-end power modules shift to adopt high-performance GaN power switches for faster and more efficient operation. The proposed techniques support effective EMI suppression and minimize switching power losses.

TECHNICAL APPROACH

To suppress EMI in switching power circuits effectively, passive EMI filters, shielding, PCB, and packaging innovations can be applied. However, these approaches often come at the significant expenses of system volume, PCB real estate, and cost. Alternatively, EMI can be mitigated using compact, cost-effective, active circuit techniques, especially if a power circuit is naturally equipped with sensing mechanisms and feedback control loops, which are highly adaptive to variable conditions. Hence, our focus is on active circuit techniques for EMI suppression.

SUMMARY OF RESULTS

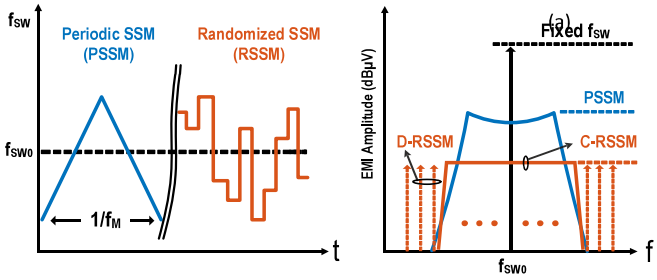


Figure 1. Comparison of EMI modulation between PSSM and RSSM schemes [1].

In a PWM control switching of a power circuit, power switches are controlled at a fixed switching frequency f_{SW}. Therefore, its EMI spectrum is distributed as spurious peaks at f_{SW} and harmonics. The modulation scheme, on the other hand, would redistribute EMI energy into a broader frequency range so that spurious EMI peaks are suppressed. A popular frequency modulation scheme is periodic SSM, in which the frequency modulation follows a periodic pattern. The periodic SSM is easy to implement in a circuit and has low power and cost overhead. However, it is not as effective for EMI suppression as random SSM (RSSM), as shown in Fig. 1.

On the other hand, EM spectrum presented by a power converter itself can also be vulnerable to another type of side-channel attack (SCA) – power SCA. Hence, the modulation scheme should also be enciphered to improve security. This leads to the need to randomize the switching frequency of the converter. To implement the RSSM in circuits, a Markov-chain-based continuous RSSM is designed. Theoretically, if the modulation follows the piecewise linear one-dimensional (PL1D) map in Fig. 2(a), the state transitions of sequence $\{V_{ran}[n]\}$ in Fig. 2(b) provide an unpredictable random output. Moreover, the state transition from $V_{ran}[n]$ to $V_{ran}[n+1]$ is in an analog manner, suggesting that the set of V_{ran} is continuous. Hence, the Markov-chain-based random clock generator possesses infinite number of states, overcoming the limitation of digital RSSM implementations. Fig. 3 demonstrates that a highly randomized f_{SW} pattern is achieved within a low modulation range of 10%, avoiding potential conflicts with the effort to mitigate anti-aliasing.

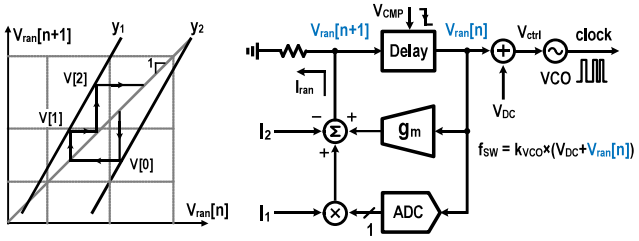


Figure 2. (a) PL1D map of Markov-chain random voltage source, (b) block diagram of Markov-chain C-RSSM.

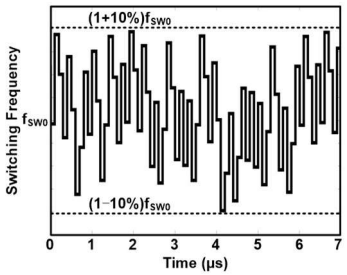


Figure 3. Markov-Chain generated randomized f_{SW}.

Keywords: RSSM, EMI, EM SCA

INDUSTRY INTERACTIONS

Texas Instruments, IBM, NXP

MAJOR PAPERS/PATENTS

[1] D. Ma, D. Yan, L. Du, "Active Conducted EMI Suppression in GaN Switching Power Circuits," IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium, pp. 1-6, Monterey CA, Dec. 2021.

TASK 2810.059, ULTRA-LOW-POWER ROBUST SAR ADC FOR PMCW AUTOMOTIVE RADAR

YUN CHIU, UNIVERSITY OF TEXAS AT DALLAS, CHIU.YUN@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

A study on the feasibility of using an elastic S/H (ESH) technique for bottom plate sampling is presented. We find that distortion at the summing node can be corrected, allowing for an improved sampling structure wherein the summing-node switch size is greatly reduced. This new guideline can be applied equally to SAR, pipelined SAR, as well as conventional pipelined ADCs.

TECHNICAL APPROACH

The feasibility of treating the post-sampling summing-node voltage as a dynamic "offset" of the preamplifier was tested using a behavioral simulation of a 10-bit SAR ADC. Two methods of removing the "offset" voltage were tested and found to be effective. Distortion contributions from the sampling and/or summing-node switches before and after the correction was tested using a nonlinear switch model. The behavior was analyzed in a simplified sampling circuit, then the functionality of ESH given finite driver impedance and parasitic capacitance was checked.

SUMMARY OF RESULTS

A schematic of a bottom plate sampling circuit is shown in Figure 1 below with C_x for preamp offset removal.

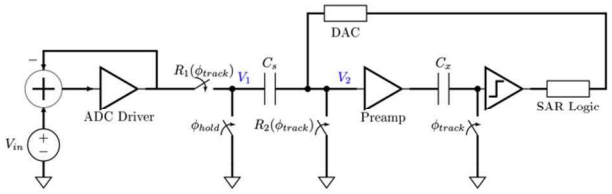


Figure 1. Bottom-plate sampling circuit in a SAR ADC with preamp "offset" removal to correct summing-node swing.

To correct for swing or distortion at the summing node V_2, we can treat V_2 swing as a 'dynamic' offset voltage – dynamic because of its signal-dependent nature – of the preamp (i.e. one that will vary from sample to sample). Therefore, the existing techniques used to remove offset can be used to remove the swing at the summing node. Both an output storage technique (Figure 1) or an input storage technique (where the offset storage is at the input of the preamp) was effective, although the output storage technique is likely the better design.

The dominant nonlinearity in a bootstrapped switch such as the sampling switch R_1 or summing node switch R_2 arises from a variation on which side of the switch is the source or the drain, which depends on whether the input is rising or falling. The nonlinearity at V_1 is dominated by R_1 and at V_2 by R_2. Without ESH, the sampled voltage is $V_1 - V_2$, meaning that the nonlinearity from both switches contribute equally. With ESH, the sampled voltage is just V_1, meaning only the distortion from R_1 contributes.

If a nonlinear switch resistance is scaled by a factor of K (meaning the switch is K times smaller), then the swing across the switch is K times larger, resulting in K^2 as much distortion. Therefore, if $R_2 = KR_1$, then the improvement to THD when correcting the summing node is a factor of $K^2 + 1$. Figure 2 below shows that this means we can correct for nearly all of the distortion caused by R_2 and are only limited by the distortion caused by R_1.

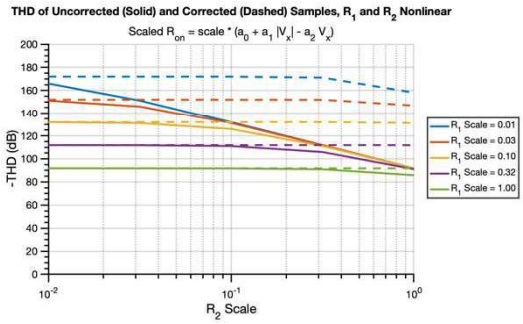


Figure 2. THD of sampled voltage with varying sizes of R_1 and R_2 with or without summing-node correction.

We verified that given finite switch and C_S parasitic capacitances, and finite ADC driver output impedance and bandwidth, the summing node switch can still be made smaller. The smaller switch would aid in improving the feedback factor during residue amplification and summing node attenuation during the SAR bit cycles, both helping with the power efficiency. We also found that for a given switch size, a lower driver G_m is needed to achieve the same THD.

In the following year, the plan is to verify these results with transistor circuits. We plan to do design and layout of a 10b 1Gs/s SAR ADC in a 65-nm CMOS process to verify the benefits of ESH in silicon.

Keywords: Elastic S/H (ESH), THD, switch nonlinearity, summing-node swing, summing-node distortion

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

TASK 2810.061, TWO-STAGE VERTICAL POWER DELIVERY AND MANAGEMENT FOR EFFICIENT HIGH-PERFORMANCE COMPUTING

HANH-PHUC LE, UNIVERSITY OF CALIFORNIA, SAN DIEGO, HANHPHUC@UCSD.EDU
PATRICK MERCIER, UNIVERSITY OF CALIFORNIA, SAN DIEGO

SIGNIFICANCE AND OBJECTIVES

The project seeks to significantly improve the efficiency of power delivery from high-voltage busses to scaled-CMOS-compatible voltages (<1V) in a vertically and heterogeneously integrated architecture leveraging hybrid and switched-capacitor DC-DC converters. Successfully deployed can reduce the number of power pins to the chip by at least 2x and reduce thermal dissipation.

TECHNICAL APPROACH

The new ambitious approach utilizes a 2-stage vertical PDM architecture with an optimal tapered current distribution, combining an integrated 4V-to-1V switched-capacitor voltage regulator (SCVR) stage located within the package substrate, underneath the processing die, along with a 20V/48V-to-4V hybrid voltage regulator module (HVRM) stage on a PCB. The SCVR is co-packaged with deep-trench capacitors where both SCVR and the integrated capacitor interposer dies can be thinned so that they can fit within a C4 bump height. The architecture enables ~2x reduction in package PDM pins and a 4x interconnect loss reduction resulting in a ~1.5x increase in available data IO pins.

SUMMARY OF RESULTS

After efforts in a detailed analysis, optimization, and power stage simulations of the two converter designs from 09/2020 to 12/2020, the year 2021 has been utilized to design the Gen 1 versions. Multiple new circuit techniques have been introduced to improve their performance. The SCVR and HVRM were implemented with a 65-nm and 180-nm CMOS process, respectively. Both will use flip-chip bumping to reduce parasitic resistances and inductances. In addition to a new efficient combination of two 2:1 SC converters in the topology, the SCVR employs a novel adaptive frequency control that optimally combines a PI control with a fast lower-bound control to achieve fast transient response, efficient steady-state regulation, as well as a smooth transition between the two control modes across the load range. While these two modes of control are not new, the utilization of both modes and achieving smooth transitions at any load point to achieve both high efficiency in steady state and fast transient response is a significant new contribution. The HVRM design features multiple design advances, including a new design of a voltage regulation loop with a flying capacitor voltage balancer, a new soft-start startup mechanism, and new high-voltage level shifter circuits. The HVRM full design achieves 95% efficiency, while SCVR achieves 94%.

In the SCVR design, the team also works with our industry partner, Murata, to co-design a package substrate with new integrated passive devices (iPDs) isolated from each other to implement flying capacitors for the SCVR converter.

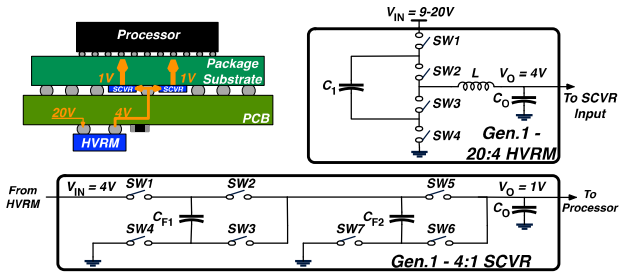


Figure 1. Architecture of the two-stage vertical power delivery module with Gen.1 specifications of 20V-to-1V conversion. Two converter designs are implemented in 65-nm (SCVR) and 180-nm (HVRM) CMOS processes.

The designs were taped out in January 2022. The fabricated chips of the designs have been received and are in assembly for testing. The iPD package substrate is already in the second generation with the same footprint for integration but updated with a better capacitor technology with 1μF/mm^2 density that is verified in measurement.

Keywords: vertical power delivery, power management, DC-DC converter, switched-capacitor, hybrid converter

INDUSTRY INTERACTIONS

Texas Instruments, IBM, Intel, NXP

MAJOR PAPERS/PATENTS

TASK 2810.065, POWER-EFFICIENT AND RELIABLE 48-V DC-DC CONVERTER WITH DIRECT SIGNAL-TO-FEATURE EXTRACTION AND DNN-ASSISTED MULTI-INPUT MULTIPLE-OUTPUT FEEDBACK CONTROL

MINGOO SEOK, COLUMBIA UNIVERSITY, MGSEOK@EE.COLUMBIA.EDU

SIGNIFICANCE AND OBJECTIVES

The goal of this project is to design the sensing and control circuit for a 48-V DC-DC converter for the data center application. The proposed sensing and control system will be able to measure the real-time power converter efficiency (PCE), track the maximum PCE point and enhance the reliability of the converter.

TECHNICAL APPROACH

We designed three key features to improve the DC-DC converter PCE and reliability. First, we developed a sensing circuit to sample the converter input and output current and calculate the real-time PCE. Then, we designed a digital controller to track the maximum PCE point by modulating the gate width of power switches. We also designed a roaming circuit that functions at a steady-state, which divides the stress on power switches equally on each switched segment, thus improving the reliability of the converter.

SUMMARY OF RESULTS

We designed a prototype of the DC-DC converter. We are going to verify the PCE tracking and reliability enhancing function using the prototype.

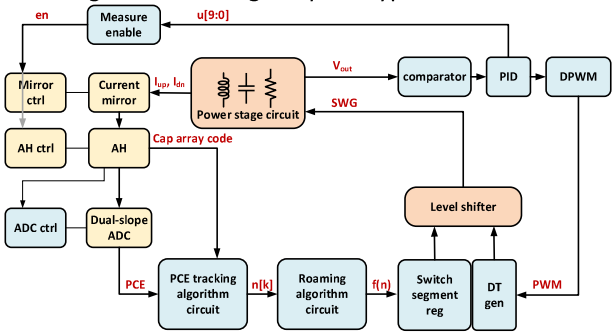


Figure 1. Block diagram of the DC-DC converter shows the signal flow in control loops. The blue blocks use 1.8-V V_{DD}, the yellow blocks use 5-V V_{DD}, and the red blocks are high-voltage blocks.

Figure 1 shows a block diagram of the DC-DC converter with sensing and control circuits. It has two control loops on the periphery of the power stage circuit. One is for stability contro and the other is for PCE tracking and reliability enhancements.

The voltage mode PWM control ensures the stability of the power stage. It includes a comparator, proportional–integral–derivative controller (PID), digital PWM signal generator (DPWM), deadtime generator (DT gen), and level shifter. The comparator first digitizes V_{out} and sends the digital value to the PID controller. DPWM transfers the PID output control code into the a PWM control signal. Then, the DT gen introduces a deadtime between high-side and low-side switches and sends the control signal to each power switch through the level shifter.

The second control loop performs PCE measurement, maximum PCE point tracking, and roaming algorithm. It includes a current mirror, accumulate-and-hold (AH) circuit, dual-slope ADC and their control circuit, PCE tracking algorithm circuit, and roaming algorithm circuit. When the PID output stays unchanged for a long enough time, we say the power stage circuit is in a steady state. Then, the measure enables the circuit to activate the current mirror to sample the converter input and output current. AH circuit accumulates the mirrored current and converts them into voltages. These voltage values represent the input and output power of the converter. Afterward, a dual-slope ADC calculates the ratio between two voltages to get the real-time PCE measurement. The PCE tracking algorithm circuit performs dynamic gate width modulation in the DC-DC converter and compares the measured PCE in the past and present monitoring window. It then uses gradient descent algorithms to track the maximum PCE point. Afterward, the roaming algorithm circuit equalizes the stress to the power switch segments by equally distributing the turn-on period among the switch segments. By doing so, we can mitigate the aging effect of the power switch and enhance the reliability of the converter. The switch segment register synchronizes the roaming output with the PWM control signal and applies control signals to each power switch through the level shifter.

Keywords: PCE tracking, gate width modulation, PCE measurement, reliability

INDUSTRY INTERACTIONS

Texas Instruments, IBM, Intel

MAJOR PAPERS/PATENTS

[1] Z. Wang et al., “Review, Survey, and Benchmark of Recent Digital LDO Voltage Regulators,” (Invited) 2022 CICC, April 2022, Newport Beach, CA, USA.

TASK 2810.067, HIGHLY EFFICIENT EXTREME-CONVERSION-RATIO BUCK HYBRID CONVERTERS

PARTHA PANDE, WASHINGTON STATE UNIVERSITY, PANDE@WSU.EDU
DEUKHYOUN HEO AND JANA DOPPA, WASHINGTON STATE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

This project aims to design and demonstrate an extremely high conversion ratio (HCR) high-performance, energy-efficient voltage regulator, and a new machine learning (ML)-enabled optimization framework.

TECHNICAL APPROACH

This research aims to develop: (a) a novel high-efficiency single-input-single-output (SISO) HCR hybrid buck converter; (b) a single-input-multi-output (SIMO) HCR hybrid converter with low cross-regulation and fast response; (c) an ML-based framework to optimize the circuit parameters of SISO and SIMO inductor-first hybrid converters.

SUMMARY OF RESULTS

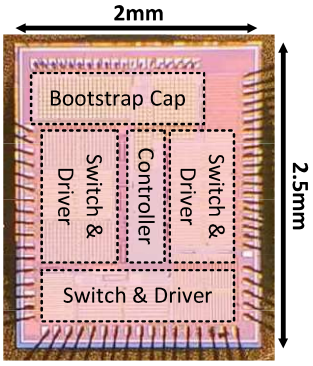


Figure 1. Fabricated chip-die photo

We have developed a SISO HCR inductor-first hybrid (IFH) buck converter. In the post-layout simulation, a peak efficiency of 94% is achieved at 120-mA load current with a 650-mV output voltage, 5.5-V input voltage, and maximum HCR of 9. The settling time of load transient response is less than 20 µs with an overshoot of less than 10% of the output voltage. The proposed HCR converter is fabricated in a 180-nm CMOS process with an area of 2×2.5mm^2 including test pads. The fabricated chip die-photo is illustrated in Fig. 1. The chip is being tested.

In the first five months of 2022, we were investigating the SIMO HCR IFH converter, aiming for reduced inductor conduction loss, and higher efficiency with a larger conversion ratio. The initial simulation result of the power stage is shown in Fig. 2. The proposed power stage can generate a 0.49-V and 0.9-V output with a 12-V input voltage using a conventional 180-nm CMOS technology. We will develop a new pulse width modulation (PWM) feedback controller in the next few months to minimize the hard-charging loss and cross-regulation in the power stage. The SIMO HCR design will be fabricated in late 2022.

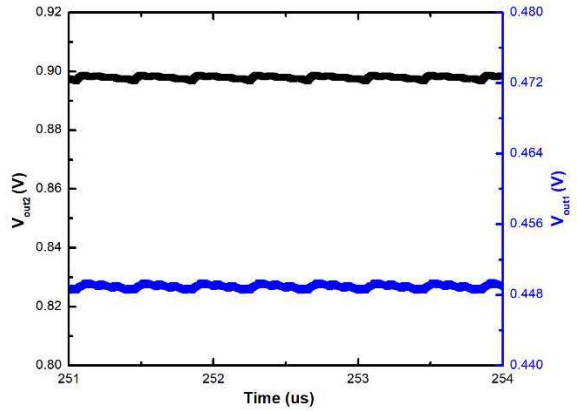


Figure 2. Simulated SIMO converter outputs of 448mV and V_{out2} at 900 mV.

We propose a novel and efficient information-theoretic approach referred to as Preference-Aware Constrained Multi-Objective Bayesian Optimization (PAC-MOO) for optimizing circuit configurations. The experimental results demonstrate that our information-theoretic algorithm PAC-MOO without any preferences outperforms baseline methods by finding a high-quality Pareto set of circuit designs (measured in terms of hypervolume indicator) in fewer circuit simulations.

Keywords: extremely high conversion ratio, buck converter, hybrid topology, ML-optimization, single-inductor-multi-output

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] "An Inductor-First Single-Inductor Multiple-Output Hybrid DC-DC Converter With Integrated Flying Capacitor for SoC Applications," accepted by TCAS-1 journal and ISICAS2022.

TASK 2810.068, ACTIVE EMI FILTERING WITH SWITCH-MODE AMPLIFIER FOR HIGH EFFICIENCY

ALEX HANSON, THE UNIVERSITY OF TEXAS AT AUSTIN, AJHANSON@UTEXAS.EDU

SIGNIFICANCE AND OBJECTIVES

EMI filters are necessary components of power converters. Passive filters are bulky and expensive, and typical active filters can consume unacceptably large powers. The objective of this research is an EMI filtering approach with a 10x smaller size than passive filters and 10x more efficiency than typical active filters.

TECHNICAL APPROACH

We replace the linear amplifier universally used in active EMI filters (AEF) with a GaN-based switch-mode amplifier for high efficiency. The AEF amplifier operates at the same switching frequency and simply uses the controlled gate signals directly from the main DC-DC boost converter. The AC ripple current from the boost converter can be almost filtered out (remains only small high-frequency harmonics) by simply matching the ratios of V_g/L with V_o/L_o. By making the AEF supply V_g hundreds of times smaller than the output voltage of the boost converter V_o, the size of L is made over hundreds of times smaller than the size of the boost inductor L_o. As a result, the AEF volume is much smaller than a passive LC filter with a similar current attenuation. This approach does not require any sensing, feedback and compensation circuits, and it also does not interfere with the closed-loop controller of the boost converter which is advantageous compared with the prior high-frequency switch-mode AEFs.

SUMMARY OF RESULTS

A complete design has been completed as shown in Figure 1. A 150-kHz prototype of the proposed AEF is shown in Figure 2 with the input voltage V_s=120V, V_o=400V, and P_o=320W. We also built another 120-W prototype switching at a higher frequency of 1MHz, which is a more attractive frequency range due to the very fast deployment of wide-bandgap devices, i.e. GaN, SiC, for smaller size and higher efficiency.

The total volume of the proposed AEF is 0.1in^3 which is much smaller and equal to 1/32 of the volume of the size-optimized LC filter for the similar current attenuation. It filters large ripple current from the boost converters achieving significantly high current attenuation of 65dB and 38dB at the switching frequencies of 150kHz and 1MHz, respectively. Furthermore, it consumes very low power of only 0.23W and 0.3W for the 150-kHz, 320W and 1-MHz, 120-W prototypes which demonstrate the proposed AEF with a smaller size and higher efficiency is a promising solution to replace the conventional passive LC filter and linear-mode AEF.

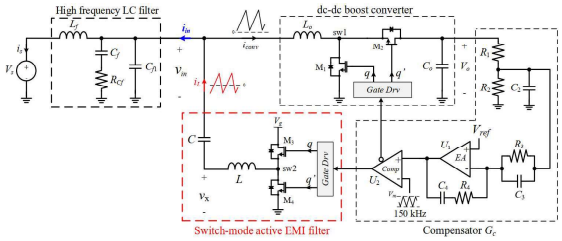


Figure 1. Overall configuration of the synchronously switch-mode active EMI filtering using GaN devices for higher efficiency and smaller size.

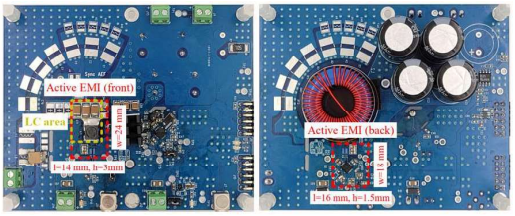


Figure 2. Two prototypes are built, (left) one at a low frequency of 150 kHz for 320-W output power, and (right) one at a higher switching frequency of 1 MHz for 120-W output power.

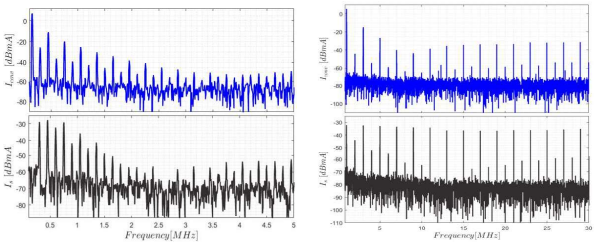


Figure 3. Experimental results show that the proposed AEF achieves very high current attenuation of 65 dB (left) and 38 dB (right) at 150kHz and 1MHz.

Keywords: electromagnetic interference, active EMI filter

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Nguyen, D. T., Hanson, A. J., "Active EMI Filter with Switch-Mode Amplifier for High Efficiency," Applied Power Electronics Conference (APEC) 2022, IEEE.

[2] Alex J. Hanson, Duy T. Nguyen, "Synchronous Switch-mode Active Electromagnetic Interference Cancellation Circuit and Method," US Patent App. 63/307,565, Feb 2022.

TASK 2810.069, A HIGH-MM-WAVE-YET-WIDEBAND LINEAR EFFICIENT DOHERTY POWER AMPLIFIER WITH COMPLEX DEVICE NEUTRALIZATION, MULTI-DRIVE DEVICE STACKING, AND CONTINUOUS-MODE COUPLER-BASED DOHERTY LOAD ARCHITECTURE

HUA WANG, GEORGIA INSTITUTE OF TECHNOLOGY, HUA.WANG@ECE.GATECH.EDU

SIGNIFICANCE AND OBJECTIVES

Sub-THz systems operating in D-band frequency, have gained increasing interest. Due to the higher free space path loss, the gain requirements of the transmitter are higher. However, native devices experience degraded power gain when operating close to the device f_{max}. Therefore, boosting the power gain of the PA becomes an essential task.

TECHNICAL APPROACH

Close to the device f_{max}, the power gain decreases. Traditional capacitive neutralization enhances device gain to its unilateral gain over a large bandwidth, but the inductive routing parasitics drastically degrades its performance at sub-THz frequencies. Therefore, we propose a new sub-THz differential complex neutralization network to attain a wideband device gain boosting. Essentially, we leverage and engineer the routing inductive parasitics with the neutralization capacitors to form a high-order neutralization network that enables wideband gain boosting. Moreover, an in-house design automation program has been developed to maximize the device Gain-BW at sub-THz frequencies.

SUMMARY OF RESULTS

The proposed power amplifier with complex neutralization is shown in Figure 1. Furthermore, we used this PA as a unit cell for a multi-way power combined power amplifier topology. An example design of 4-way combining PA is shown in Figure 2. The complex neutralization technique is used within each unit to boost the power gain at the D-band frequency range. The input power is split at the input and combined at the output using $\lambda/4$ transmission lines. We propose a coupler- based low-loss output matching network.

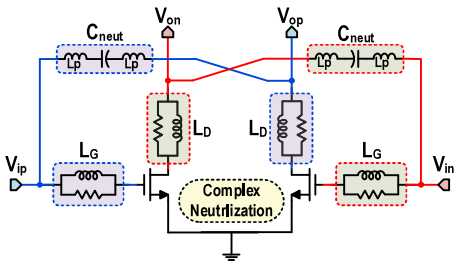


Figure 1. Proposed differential complex neutralization network using CMOS devices.

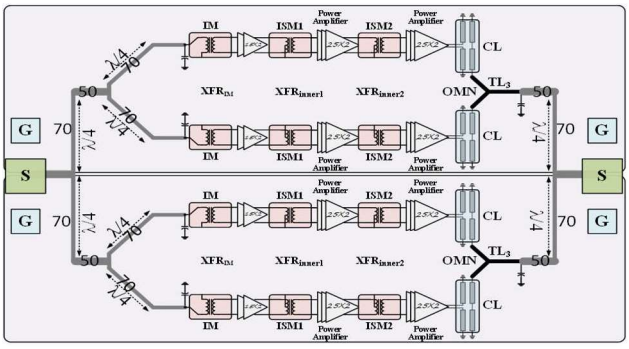


Figure 2. 4-way power combined power amplifier using three-stage PA unit cell.

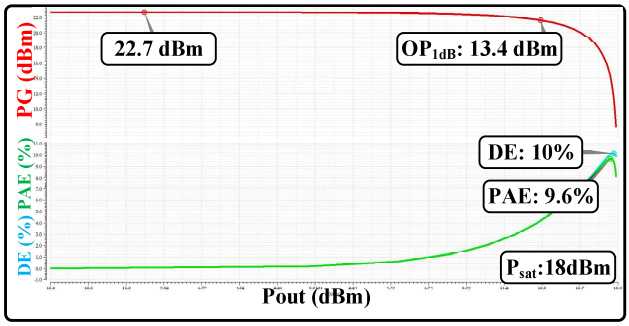


Figure 3. Large signal PA simulation results with 3D EM simulated models.

As a preliminary study, we designed a high gain 4-Way 140-150GHz PA with our proposed complex neutralized in 45nm CMOS SOI. As depicted in Figure 3, the system achieves more than 22dB power gain at a frequency of 145GHz. The saturation output power is almost 18dBm. The 1-dB compression point is 13.4dBm. Moreover, the power added efficiency is 9.6% with a chip area of 2.3mm×1.1mm.

Going forward, we will apply the proposed complex neutralization within a cascode amplifier to enhance the gain and achieve higher output power.

Keywords: Power amplifier, gain boosting, embedding network, capacitor neutralization, transmission line

INDUSTRY INTERACTIONS

Texas Instruments, Intel, NXP, MediaTek

MAJOR PAPERS/PATENTS

TASK 2810.072 AND 2810.073, AI/ML EDGE HARDWARE FOR ULTRA-RELIABLE WIRELESS NETWORKS

DAVID J. ALLSTOT, OREGON STATE UNIVERSITY, ALLSTOTD@OREGONSTATE.EDU
YIORGOS MAKRIS, UNIVERSITY OF TEXAS AT DALLAS

SIGNIFICANCE AND OBJECTIVES

The overall objective of this project is to develop area- and power-efficient on-chip real-time digital predistortion (DPD) techniques for state-of-the-art RF transmitters using energy-efficient switched-capacitor power amplifiers (SCPA). Data from several advanced SCPA architectures is being used to develop machine-learning-based static and dynamic DPD.

TECHNICAL APPROACH

The major goals described above are being addressed using an efficient sparse neural network digital predistortion technique. The proposed implementation comprises a time-domain MAC (TD-MAC) core for sparse TD neural networks (TD-NN) that uses a medium-precision quantized NNs (QNNs). As only digital cells are used, the ever-finer time precision/resolution with CMOS scaling is exploited. QNN-based TD-NN techniques with 4-8-bit inputs and coefficient weights are being developed.

The basic circuit block is the digital-to-time converter (DTC). It has digital inputs (A,B) with a relative delay D_x and an N_W-bit weight W. it generates digital outputs (P,Q) with a relative delay D_y proportional to W.

SUMMARY OF RESULTS

During this phase of the project, we have designed, implemented, and tested a CMOS SCPA that can be reconfigured for either a symmetric (SMO) or asymmetric multi-level outphasing (AMO) operating mode. In addition to providing state-of-the-art measured results for linearity and adjacent-channel performance, this design will also motivate the demonstration of reconfigurable on-chip real-time DPD techniques.

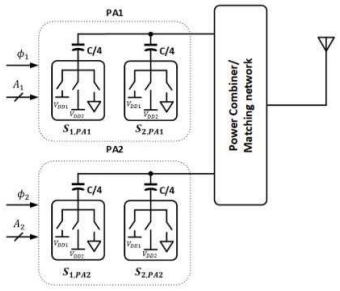


Figure 1. The reconfigurable outphasing SCPA architecture.

The proposed outphasing PA uses an architecture with a switched-capacitor power amplifier as sub-PAs (PA1 and PA2). The output of the sub-PAs is combined using a power combiner as shown in Figure 2.

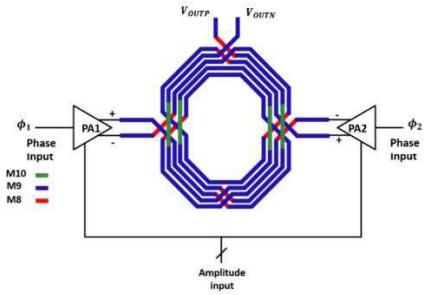


Figure 2. The layout of the 4-way power combiner.

The amplitudes of the sub-PAs are controlled using digital inputs A_1 and A_2. This means that A_1 and A_2 are the digital inputs that decide the number of capacitors in the SCPA switching between the supply voltage and ground. On the other hand, the phase of the sub-PAs (ϕ_{s1} and ϕ_{s2}) are the phases of the clock inputs to each sub-PAs. The clock is generated by a phase modulator.

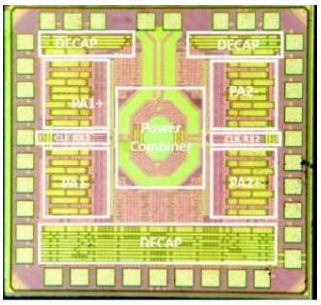


Figure 3. Die photo.

A 64-QAM signal carrier signal with a bandwidth of 400KHz is used for the SMO dynamic measurement. The measured EVM is -25dB and ACLR is -24dBc.

Keywords: Digital Predistortion, Switched-Capacitor Power Amplifier, Machine Learning, Neural Networks

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] B. Qiao, et al., "I/Q-sharing Switched-capacitor power amplifier with baseband harmonic-rejection and Wilkinson Combiner," *IEEE ISCAS*, 2021, pp. 1-4.
[2] A.V. Kayyil, et al., "Linearity improvement techniques for CMOS switched-capacitor power amplifiers," *IEEE ISCAS*, 2021, pp. 1-4.
[3] B. Qiao, et al., "An eight-core class-G switched-capacitor power amplifier with eight power backoff efficiency peaks," *IEEE RFIC Symp.*, 2022, pp. 1-4.

TASK 2810.075, HYBRID STEP-DOWN DC-DC CONVERTER WITH LARGE CONVERSION RATIOS FOR 48-V AUTOMOTIVE APPLICATIONS

HOI LEE, UNIVERSITY OF TEXAS AT DALLAS, HOILEE@UTDALLAS.EDU
JIN LIU, UNIVERSITY OF TEXAS AT DALLAS

SIGNIFICANCE AND OBJECTIVES

This research aims to develop innovative capacitor-assisted hybrid DC-DC converters to provide high power efficiency under large input-to-output voltage conversions in 48-V automotive applications. A systematic approach will also be developed to realize hybrid converters with a minimal number of low-voltage power FETs and passive components to improve the converter power density.

TECHNICAL APPROACH

We investigated both flying-capacitor multi-level and switched-capacitor-assisted converter topologies to evaluate operation flexibility in different conditions; the requirements of voltage balancing and pre-charging of flying capacitors; the capability of providing high power density; and different power losses. We developed a new technique, capacitor-assisted dual-inductor filtering to combine with common SC architectures for reducing the output-to-input conversion ratio. The minimum on-time of the power switches can be expanded such that the converter can operate in the MHz range with high efficiency. All flying capacitors do not require voltage balancing in the steady state, thereby reducing the controller design complexity.

SUMMARY OF RESULTS

The proposed 3:1 Ladder-based capacitor-assisted dual-inductor (CADI) converter is shown in Fig. 1 below. It consists of two inductors, six power switches, and three flying capacitors. The minimum input-to-output conversion ratio (CR) achieves D/5, which helps expand the minimum on-time of power switches by 10 times as compared with the conventional buck converter. All flying capacitors in the converter do not require balancing in the steady state. Both switching-node voltage swings and the flying capacitor voltages are reduced to lower the converter switching loss and improve the converter reliability.

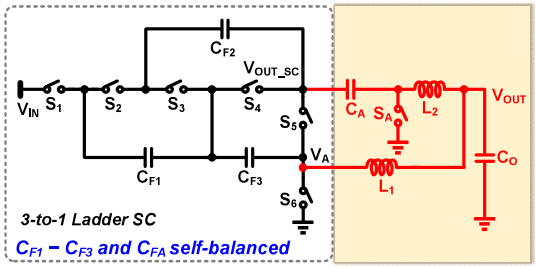


Figure 1. The architecture of the proposed 3:1 Ladder-based CADI converter [1].

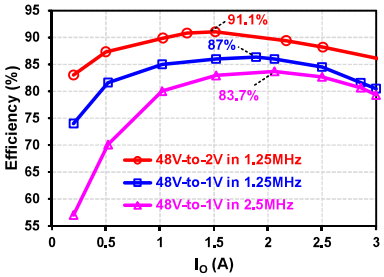


Figure 2. The measured power efficiency of the proposed converter.

The proposed converter was implemented in a 0.18-μm HV CMOS process. It can provide direct voltage conversion to generate an output voltage of 0.8 – 2V from an input voltage range of 36V – 55V with a maximum switching frequency of 2.5MHz [1]. All six power switches are fully integrated on die by using LDMOS transistors. The converter delivers the load current I_O up to 3A. Thanks to the proposed converter topology, the minimum on-time of the power switches are 80ns at 1.25MHz and 40ns at 2.5MHz for 48-V-to-1-V conversion. Fig. 2 represents the measured power efficiency of the proposed converter. The peak power efficiencies are 91% at 1.25MHz for 48V-to-2V conversion, 87% at 1.25MHz for 48V-to-1V conversion, and 83.7% at 2.5MHz for 48V-to-1V conversion. To our best knowledge, the proposed converter using fully on-chip power NMOS is the first to achieve 48-V-to-1-V or to-2-V direct conversion with competitive power efficiencies in the MHz range.

Based on these excellent results of the proposed converter, we are exploring different techniques to further increase the output current.

Keywords: DC-DC converter, capacitor-assisted dual inductor filtering, high-conversion-ratio step-down converter, hybrid converter, non-isolated converter

INDUSTRY INTERACTIONS

Texas Instruments, Intel, NXP

MAJOR PAPERS/PATENTS

[1] C. Chen et al., "A 2.5 – 5MHz 87% peak efficiency 48V-to-1V integrated hybrid DC-DC converter adopting Ladder SC network with capacitor assisted dual inductor filtering," in 2022 ISSCC, Feb. 2022, San Francisco, CA.

TASK 2810.078, PROGRAMMABLE MIXED-SIGNAL ACCELERATOR FOR DNNS WITH DEPTHWISE SEPARABLE CONVOLUTION LAYERS

BORIS MURMANN, STANFORD UNIVERSITY, MURMANN@STANFORD.EDU

SIGNIFICANCE AND OBJECTIVES

Deep neural networks (DNNs) require massively parallel and energy-efficient multiply-accumulate (MAC) circuitry. In-memory computing (IMC) has shown potential but lacks efficient means for multi-bit compute. This work looks for a middle ground between IMC and standard digital processing by investigating both mixed-signal (MS) multi-bit switched capacitor (SC) compute arrays and fully digital IMC approaches. The goals are to (1) compare the performance of MS and fully digital approaches and (2) see how overheads at the processor level affect the performance gains of IMC for both approaches.

TECHNICAL APPROACH

Our hardware is built to efficiently run bottleneck layers, which are used in modern DNNs like MobilenetV2 (MBNetV2) that target Tiny-ML applications. The key ingredient of our MS approach is a processing element (PE) array that intersperses SC accumulation circuitry with local SRAM kernel storage and digital multipliers. We also designed a fully digital version that uses the same local SRAM kernel storage but does all accumulation in the digital domain. The density of these circuits allows us to fully unroll and pipeline the operations of a bottleneck layer to (1) reduce the activation memory needed, (2) eliminate accumulation buffers and (3) eliminate repeat weight and activation accesses.

SUMMARY OF RESULTS

We have designed and simulated a prototype of an NxM MS compute array and reported the results in [1], [2]. We have also taped-out and measured a test-chip with a 160x96 array and 52kB of local memory in TSMC 28-nm CMOS to validate our energy and noise results. Figure 1 shows a conceptual schematic. Each of the M kernels contains N-dimensional dot-product circuits with input activations d and weights w. Each of the N elements in a kernel compute a 4-bit MAC with a digital AND operation and an analog accumulation operation using charge sharing on six wires (V_{MAC}). The wire voltages are capacitively summed in the shown binary combiner block before digitization with an 8-bit SAR ADC (one per kernel). All weights are stored in custom local memories with 6-T bit cells. The proximity of memory to compute eliminates the need for expensive readout circuitry.

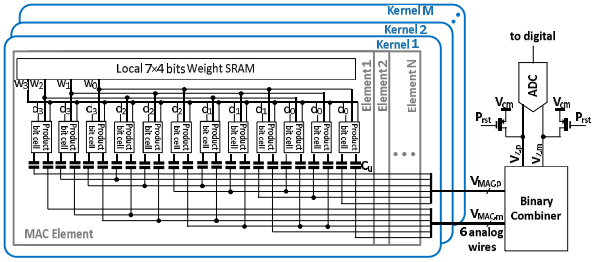


Figure 1. MS MAC array with binary combiner and local memory.

Post-layout simulations in 28 nm CMOS demonstrate an energy efficiency of 6.4 fJ/4b-MAC and a compute density of 3.17 TOPS/mm^2. Compared to the prior art, this work achieves higher energy efficiency than single-bit IMC configured for 4-bit arithmetic (~2.6x) as well as recent digital IMC realizations (~3.5x). The RMS MAC noise is <350 µV assuring <1% top-1 accuracy degradation for popular DNNs deployed on the ImageNet dataset.

Digital compute does not face the same precision limits as analog compute, so we can target 8-bit MACs. Quantization results on a small MBNetV2 (<60kB) for several Tiny-ML applications have shown that 8-bit quantization results in better accuracy than 4-bit quantization for the same network size, motivating the use of digital compute. We have designed and simulated a kernel for a fully digital IMC approach that uses the same type of local memories as the MS approach but uses 8-bit bit-serial multiplications with a digital adder tree and accumulator. By using aggressive supply voltage scaling and custom low-power full adders and flip flops we can achieve less than 30 fJ/8b-MAC in post-layout simulations.

Keywords: Deep neural networks, hardware accelerators, in-memory computing, mixed-signal integrated circuits, switched capacitor circuits

INDUSTRY INTERACTIONS

TI, IBM, NXP

MAJOR PAPERS/PATENTS

[1] W.-H. Yu et al., "A 4-bit Mixed-Signal MAC Array with Swing Enhancement and Local Kernel Memory," 2021 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), 2021.

[2] W.-H. Yu, et al. “Single-Conversion Multi-bit Mixed-Signal In-Memory Computing Array Featuring Binary Combiner,” to appear in TCAS-I Special Issue, 2022.

TASK 2810.079, HIGH-POWER-DENSITY IN-PACKAGE SIMO CONVERTERS FOR NEXT-GENERATION MICROPROCESSORS

CHENG HUANG, IOWA STATE UNIVERSITY, CHENGH@IASTATE.EDU

SIGNIFICANCE AND OBJECTIVES

SIMO allows multiple voltage rails to share the same inductor, thus reducing the use of bulky and expensive inductors. However, it has significant limitations of self-cross-regulation, smaller power capacity, and the capability to handle fast and large current steps. This project aims to address these limitations and achieve higher efficiency.

TECHNICAL APPROACH

Three different techniques are developed. Firstly, dual sampling frequency voltage mode hysteretic control is developed to eliminate small-signal bandwidth limitation with intrinsic stability. The dual sampling frequency techniques eliminate any free-wheel switches, which removes the reductant current in the inductor thus improving the power efficiency. Secondly, individual digital LDO for each output is developed to break the large-signal limitation and reduce the output voltage droops to support faster and larger load steps. Lastly, bootstrap drivers and switches are developed to boost the V_{GS} of the output selection switches to be $V_{DD} + V_O$, which extends the output range and improves power efficiency.

SUMMARY OF RESULTS

We have finished the circuit design in a TSMC 180-nm process. Figure 1 shows the system diagram of the proposed SIMO converter with two outputs for prototyping, which includes the techniques discussed above. The power inductor used is a 1-µH 0603 inductor. To verify the dual sampling frequency hysteretic control, we verified in simulations for different scenarios at steady states and transients. While the inductor charge/discharge control is synchronized at a higher frequency, the output power distribution control is synchronized at 1/8 of the clock frequency and rotated between the two outputs. The simulation results verify that with the proposed control technique, the converter can operate properly without the free-wheel switch, which improves the power efficiency.

The proposed hybrid digital LDOs are also verified in simulations at different conditions. First, we design the hybrid digital LDO with a conventional buck converter and verify that the operation can be smoothly switched between the digital LDO and the buck converter under different loading and LDO current strength conditions. In the buck configuration, for 1.2-V output voltage with a 10-µF output capacitor, when the load current steps up from 50mA to 1A in 1 ns, the output voltage droop are reduced from 78mV to 18mV by the digital LDO. Then we implement the digital LDOs in the SIMO converter. For the case when VO_2 is 0.9V, IO_2 is 450mA, VO_1 is 1.2V and IO_1 is stepped up from 50mA to 1.05A in 1 ns (1A/1ns), the voltage droops for VO_1 and VO_2 are both kept within 60mV. The transient simulation results discussed above demonstrate that the proposed digital LDO can significantly reduce the voltage droops for faster and larger current transient steps. In addition, we also verified the function of the proposed bootstrapped topology for a wide output voltage range from 0.6V to 1.5V and compared the efficiency for the cases with/without bootstrap techniques. While keeping VO_2 to be 0.9V, IO_2 to be 450mA, VO_1 to be 1.2V, and varying IO_1 from 50mA to 1.05A, we observe a 25% efficiency improvement. The chip is ready for tape-out (Fig. 2).

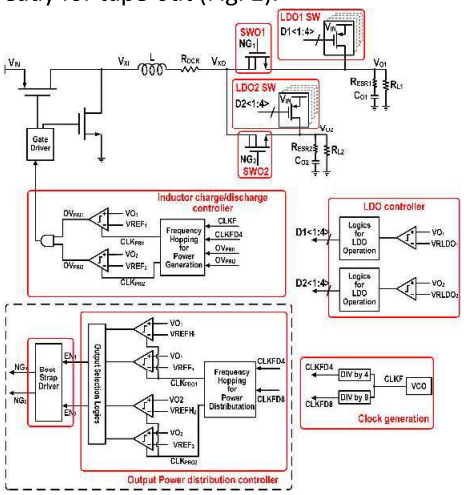


Figure 1. System diagram of the proposed SIMO converter.

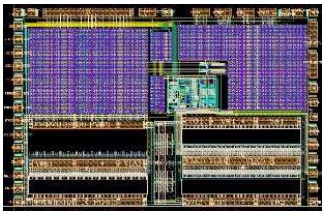


Figure 2. Chip layout in a TSMC 180-nm process.

Keywords: single-inductor multiple-output, voltage-mode, hysteretic control, digital LDO, bootstrapping

INDUSTRY INTERACTIONS

Texas Instruments, IBM, NXP

MAJOR PAPERS/PATENTS

TASK 2810.080, EFFICIENT AND HIGH-DENSITY FULLY IN-PACKAGE GAN-BASED HIGH-RATIO DC-DC CONVERTERS

CHENG HUANG, IOWA STATE UNIVERSITY, CHENGH@IASTATE.EDU
HOUQIANG FU, IOWA STATE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

Three-level and double step-down (DSD) converters are widely used for high-ratio step-down conversion. The current objective is to study and compare different topologies and then develop new topologies for better performance in a smaller form-factor.

TECHNICAL APPROACH

A 3-level two-phase (3L2P) topology is chosen for a fair comparison with DSD as the 3L2P topology has the same number of interleaved inductors as DSD. A comprehensive comparison is made between DSD and 3L2P topologies with carefully controlled conditions i.e. the same voltage and current ripples, same chip-area budget with the same number and sizes of inductors and capacitors. The comparison is made first by analyzing the differences in frequency required in each topology for a given ripple and then comparing the switching and conduction loss of each. The simulations are then carried out at different frequencies, loading conditions, and conversion ratios to verify the analysis in Cadence with 180-nm 55V BCD and 200V GaN processes [1]. We have also derived the control-to-output transfer functions using state-space-average for comparison.

SUMMARY OF RESULTS

Based on the analysis and verification results, the switching waveforms are identical when 3L2P is switched at half the frequency of DSD, while DSD can achieve better efficiency even with a smaller chip area. Moreover, when both DSD and 3L2P have the same total area and DSD is switched at 2X the frequency of 3L2P, 3L2P has the conduction loss and switching loss of 4X and 0.5X that of DSD, respectively. The simulation results (Fig. 1(a)) comparing the two topologies at 10-A loading current and different conversion ratios using the integrated power stage in the BCD process show that DSD stands better in every case (the DSD converter is switching at 2X the frequency of the 3L2P one for the same voltage and current ripples).

Further efficiency improvements are observed when using the integrated GaN process (provided by IMEC) for the power stage. Although GaN fabrication will cost more, it is worth considering given the efficiency benefits achieved for each device. For instance, a 48-V-to-1-V 2.5-A loading current GaN DSD occupying an area of 1mm^2 is 93% efficient when switched at 200kHz, which increases to 98% for 48V-to-2V. The simulation results for GaN are shown in Fig. 1(b) with 550-kHz DSD switching frequency and different output voltages at varying loading conditions. Again, GaN DSD has a higher efficiency in each case, and is a better design choice to achieve an efficient direct down-conversion, especially for very high down-conversion ratios such as 48V-to-1V.

In addition, a new switch-tank-based direct-down-conversion topology is being developed at the board level for prototyping. Basic operations, such as output voltage conversion ratio and resonant capacitor charging (Fig. 2) have been verified, but some issues related to the bootstrap high-side drivers need to be resolved.

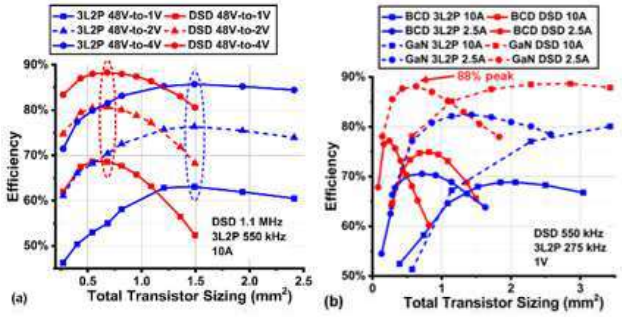


Figure 1. Efficiency comparison at different conditions.

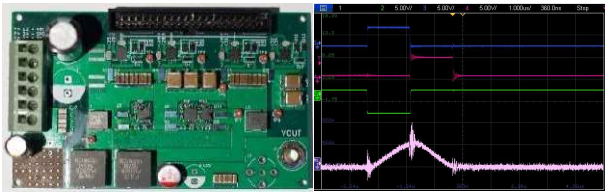


Figure 2. PCB of the 3-phase switched-tank converter and verified resonant charging of the flying capacitor (pink) with control signals for phase 1, phase 2, and phase 3.

Keywords: high-ratio, hybrid, 3-level converter, double-step-down converter, GaN, switched tank converter

INDUSTRY INTERACTIONS

Texas Instruments, IBM, Intel

MAJOR PAPERS/PATENTS

[1] M. R. Khan, et al., "Analytical Comparison of 2-Phase 3-Level and Double-Step-Down…," accepted in ECCE 2022.

TASK 2810.087, GRID OPTIMIZATION AND SILICON VALIDATION FOR CHIP ROBUSTNESS

FARID N. NAJM, UNIVERSITY OF TORONTO, F.NAJM@UTORONTO.CA
CHRIS H. KIM, UNIVERSITY OF MINNESOTA

SIGNIFICANCE AND OBJECTIVES

On-chip power grid design and sizing can have a direct impact on the supply voltage, circuit timing, and functionality. As the chip ages, even a well-designed grid degrades over time and causes voltage drop violations. We develop methods for grid optimization and design that guarantee grid robustness under electromigration (EM).

TECHNICAL APPROACH

Our previous work on grid optimization [1] provided a method for grid fixing by varying the widths of metal lines, to be used once an EM-induced voltage drop violation has been found. In this work, we will build on that work and address the one bottleneck identified in [1], namely that the objective function computation is slow. We do this by introducing novel model reductions in the lines and in the trees to speed up the simulation and tackle large grids.

SUMMARY OF RESULTS

Under previous tasks, using the Korhonen stress-based model for EM (1993), we developed a linear (LTI) system model that describes the time evolution of the stress vector as a function of line currents. We also used this to build a simulation engine for tracking the evolution of EM over time - the first practical *electromigration simulator*.

Last year, we discovered [2] that the relations between stress and flux in every interconnect tree metal line are identical to those between voltage and current in a specially designed electrical circuit (an RC network), as shown in Fig. 1. We call this an *equivalent circuit*, and it can be easily and automatically built for any given metal interconnect tree. If we solve the voltage-current problem for the equivalent circuit, then we have automatically solved the stress-flux problem for the interconnect tree. Node voltages in the equivalent circuit give the stresses in the metal network.

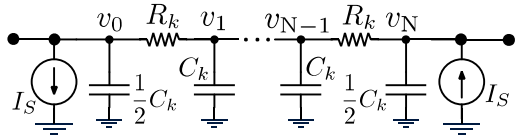


Figure 1. The equivalent circuit for a metal line.

This model, with 20 segments, is the standard model for RC transmission lines but, given the slow dynamics of EM-induced stress evolution, we have found that this model can be drastically reduced in size, with no significant loss of accuracy. This reduction does not require any EDA effort and is pre-determined upfront based on the reduced circuit shown in Fig. 2.

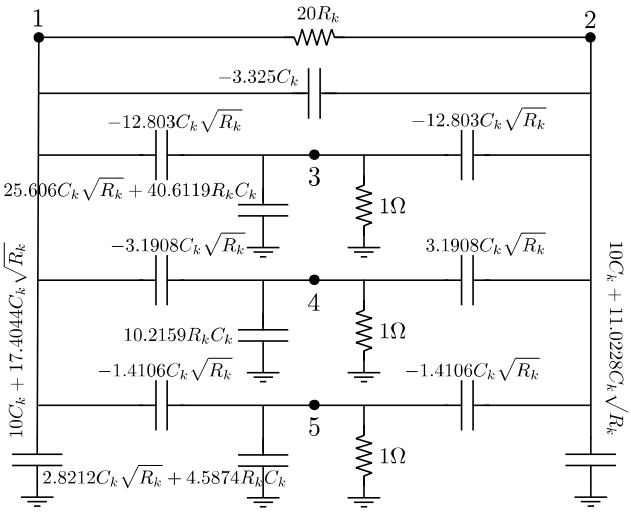


Figure 2. The reduced circuit for a metal line.

This year, we incorporated this model into our stress simulation engine which computes the grid lifetime, as the objective function, to replace the previous engine in [1]. The node count per line is reduced by about 4X. A tree with one million nodes now takes only 2 minutes to simulate, compared to 8 minutes previously.

Simulation of whole grids, which contain large numbers of trees, show an overall speedup of 2-3X. For example, a grid with 3.2 million junctions, which takes 2.15 hours to simulate with the full model, simulates in 52 minutes with the reduced model (a 2.5X speedup). A grid with 4.1 million junctions takes 1.3 hours to simulate with the full model but only 37 minutes with the reduced model (a 2.2X speedup). These improvements should contribute similar speedups in the overall runtime of the optimization.

Keywords: integrated circuits, electromigration, stress, reliability, optimization, reduced-order model

INDUSTRY INTERACTIONS

Intel, NXP, Texas Instruments, Mentor-Siemens

MAJOR PAPERS/PATENTS

[1] Z. Moudallal, V. Sukharev, and F. N. Najm, "Power grid fixing for electromigration-induced voltage failures," International Conf. on Computer-Aided Design, Nov 2019.
[2] F. N. Najm, “Equivalent circuits for electromigration,” Microelectronics Reliability, August 2021.

TASK 2810.088, GRID OPTIMIZATION AND SILICON VALIDATION FOR CHIP ROBUSTNESS

CHRIS H. KIM, UNIVERSITY OF MINNESOTA, CHRISKIM@UMN.EDU
FARID NAJM, UNIVERSITY OF TORONTO

SIGNIFICANCE AND OBJECTIVES

This project will experimentally validate the power/ground (p/g) grid optimization techniques in custom built silicon ICs. This work addresses the lack of hardware data which is arguably the most pressing issue when it comes to developing EM models. Another important focus is to demonstrate how to incorporate the optimization methodology into a standard ASIC design flow.

TECHNICAL APPROACH

We will leverage the circuit-based EM characterization experience to design standard and optimized p/g grids on the same silicon die and compare the measured EM lifetimes and IR drop maps with the simulation results. The focus of this project will be on the optimization of the grid, rather than the characterization of an existing standard grid, and on how the optimization framework could be incorporated into design flows.

SUMMARY OF RESULTS

Our experimental work will leverage the previous 65-nm and 28-nm CMOS power-grid test chips where thousands of local V_{DD} and GND voltages can be monitored while the grid undergoes EM stress. Fig. 1 shows a 9x9 pseudo power grid chip with three connection points to IO pads. Using this dedicated test vehicle, we were able to study the impact of temperature gradient on the power grid lifetime. Using the power grid structure with different metal widths, we will experimentally verify the effectiveness of increasing the metal width on reducing the IR noise and increasing the EM lifetime. Our group has been developing a testing program that will allow the stress and measurement to be performed under the same elevated temperature. We have also developed a new temperature control program that uses the temperature of on-chip metal sensors instead of the previous heater temperature-based feedback. Another improvement we have been making is controlling the power of the two on-chip heaters separately so that we can achieve a uniform temperature distribution while eliminating multi-variable feedback issues. We are getting close to collecting IR drop and EM data from power grids with different metal widths and the number of metal stripes. In addition to the experimental work, we have been familiarizing ourselves with the various power grid configuration options available in the place-and-route tool. As shown in Fig. 2, we have generated different power grids to understand the design tradeoffs.

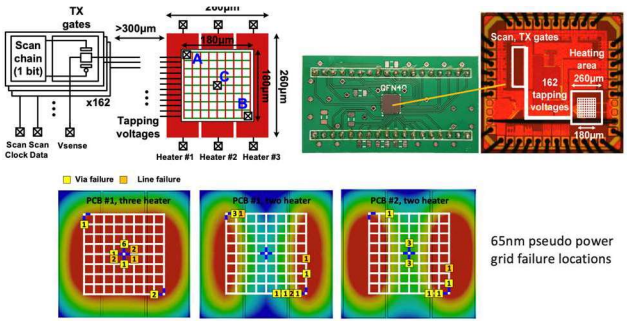


Figure 1. Previous power grid EM test vehicle that will be leveraged in this work.

Figure 2. Power grid design options in place and route tool. Around 100 power grid parameters ranging from metal width, metal stripes, power rings, etc., can be configured in the physical design flow.

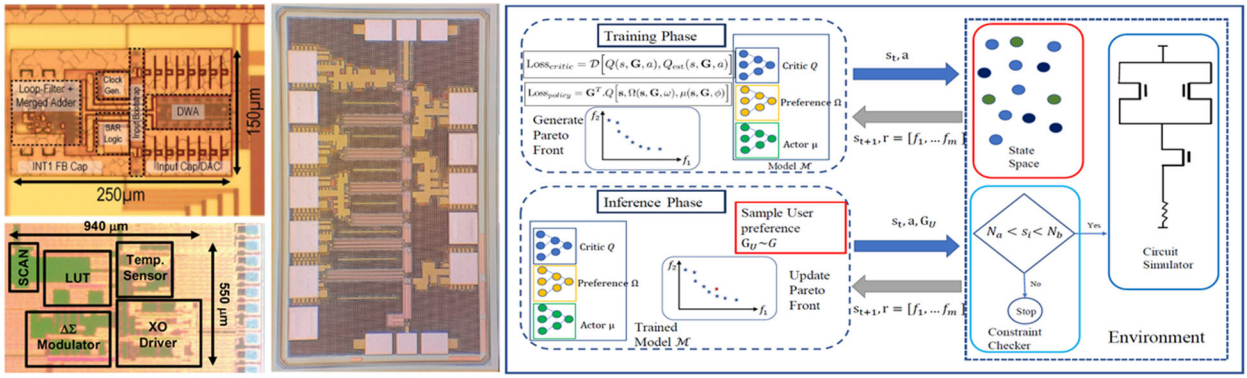
Keywords: Power grid, IR noise, electromigration lifetime, silicon validation, physical design

INDUSTRY INTERACTIONS

Intel, NXP, Texas Instruments, Mentor-Siemens

MAJOR PAPERS/PATENTS

Fundamental Analog Thrust



Category	Accomplishment
Fundamental Analog (Circuits)	Wideband low noise amplifiers (LNAs) operating in the 170-260 GHz band are developed for future high-speed wireless communication links and imaging radars. Fabricated in a commercial 130-nm SiGe BiCMOS process, the LNA achieves a peak measured gain of 15.5 dB at 207 GHz, 3-dB bandwidth spanning the WR5 frequency range of 140-220 GHz (fractional bandwidth of 44%), a measured noise figure of 6.9 dB, 6.1 dB, and 8.2 dB at 150 GHz, 180 GHz, and 210 GHz, respectively. (2810.029, A. Babakhani, UCLA)
Fundamental Analog (Circuits)	A pulsed-injection driver and a delta-sigma dithered load capacitor is developed to lower power consumption and perform temperature compensation of crystal oscillators (XO), respectively. Implemented in 40-nm CMOS, the 32.768-kHz temperature-compensated XO (TCXO) achieves an accuracy of ±4.2 ppm over a −20 °C to 85 °C temperature range with three-point trimming and an Allan deviation floor of 34 ppb while consuming 43 nW, an 8× improvement over the state-of-the-art TCXOs. (2810.063, D. Sylvester, U. Michigan)
Fundamental Analog (Circuits)	A newly-developed pseudo-pseudo-differential (PPD) technique for reducing flicker noise in single-ended circuits is employed in a high-resolution discrete-time single-loop delta-sigma ADC to improve dynamic range. Utilizing a single-ended ring-amplifier-based integrator and the PPD technique, the fabricated ADC consumes 203.5μW and achieves a 108.8 dB dynamic range within a compact area of 0.0375 mm^2 in 180-nm CMOS. (2810.037, U. Moon, Oregon State University)

TASK 2810.019, DESIGN AUTOMATION FOR COVERAGE MANAGEMENT IN ANALOG AND MIXED-SIGNAL SOCS

PALLAB DASGUPTA, INDIAN INSTITUTE OF TECHNOLOGY KHARAGPUR,
PALLAB@CSE.IITKGP.AC.IN
ARITRA HAZRA, INDIAN INSTITUTE OF TECHNOLOGY KHARAGPUR

SIGNIFICANCE AND OBJECTIVES

The objective of this task is to design and implement CAD support for coverage management of AMS artifacts in mixed signal SoCs. Specific objectives include defining metrics for analog coverage, instrumenting analog coverage collection on standard simulation environments, and reasoning over coverage from IP level to SoC level.

TECHNICAL APPROACH

We propose novel metrics for identifying glitches and levels in an analog waveform. Our metrics hold the ability to adaptively identify glitches and levels depending on the scope of the signal that is presented to it. We also propose coverage artifacts for a periodic signal. We have also developed a sequence-based approach for computing these artifacts that can carry out the computations even when the reference value of periodicity is unknown or when the reference changes with time. Finally, our SMT-based methodology for selecting simulation runs from a set of statistical simulations at the IP level has been beneficial in increasing coverage at the SoC level.

SUMMARY OF RESULTS

Each of our methodologies has been verified on industrial circuits. Figure 1 shows the result of glitch and level identification metrics on a waveform from an industrial circuit. Our algorithm for identifying coverage

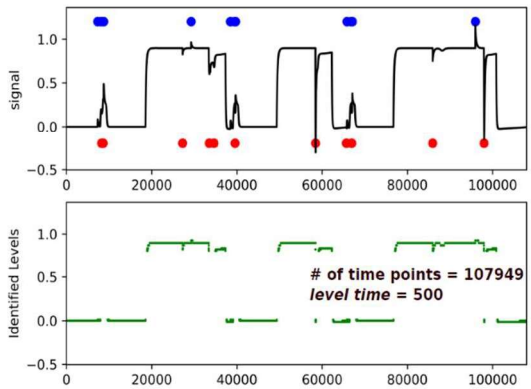


Figure 1. Blue and Red dots show time points of overshoots and undershoot respectively. Green lines are the identified levels.

artifacts on periodic signals was verified using waveforms from a DCO. Figure 2 demonstrates the results for the same. Table 1 shows the impact of the proposed approach in increasing the coverage of two signals at module level simulations of an LDO.

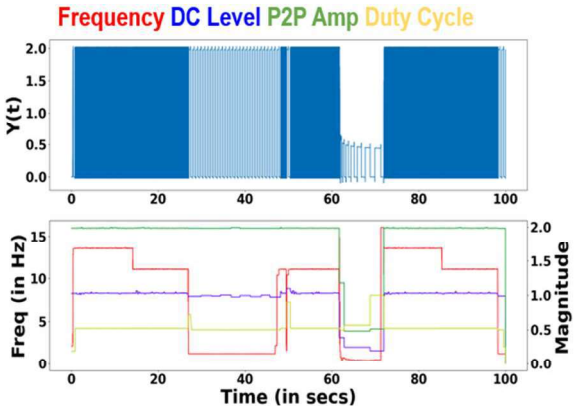


Figure 2. Tracking periodic artifacts of a DCO output.

Table 1. Increase in coverage at the module level.

Category	Signal	min value	max value
Baseline sims.: Nominal, weak, strong, skewn, skewp process	ldo_1v8	1.79	1.81
	ld0_3v0	2.4	3.001
2 Monte Carlo corners identified by the proposed methodology	ldo_1v8	1.73	1.86
	ld0_3v0	2.4	3.016

Keywords: Coverage Management, Analog & Mixed Signal, System-on-Chip, Glitch and Level, Periodic Signal

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] S. Sanyal et al., "The CoveRT Approach for Coverage Management in Analog and Mixed Signal Integrated Circuits," IEEE Transactions on CAD, March 2022.
[2] A. Chakraborty et al., "Tracking Coverage Artefacts for Periodic Signals using Sequence-based Abstractions," IEEE VLSI Design Conf., Feb 2022.
[3] S. Sanyal "Glitch and Level Detection Algorithms for Analog Mixed-Signal Verification Coverage Management," [Poster], IEEE/ACM Design Automation Conference, 2021.
[4] S. Sanyal, et al. "METRICS FOR IDENTIFYING GLITCHES AND LEVELS IN MIXED-SIGNAL WAVEFORMS." US Provisional Patent, 63/285,652, filed December 3, 2021.

TASK 2810.028, ROBUST ATE MULTI-SITE HW DESIGN TO ENABLE EFFECTIVE ANALOG PERFORMANCE TESTING IN ANALOG-MIXED SIGNAL (AMS) SOCS

DEGANG CHEN, IOWA STATE UNIVERSITY, DJCHEN@IASTATE.EDU

SIGNIFICANCE AND OBJECTIVES

Mission-critical applications dictate demanding testing, significantly impacting time-to-market and manufacturing costs. Massively parallel multisite testing offers great improvements in throughput and test cost. This project will develop tools for automatically flagging excessive site-to-site variations, identifying/correcting ATE hardware issues causing s2s variations, and enhancing multi-site ATE hardware robustness and effectiveness.

TECHNICAL APPROACH

Existing volume probe/final-test data and ATE hardware files will be used to develop statistical signal processing and machine learning algorithms to automatically process the volume data and flag the issue sites and specifications. These results will enable the identification of sensitive components/nets in the ATE hardware. Targeted extraction/simulation will be run and additional GRR measurements will be taken to identify hardware root causes. Such learning will lead to improved test board hardware design that is robust to site-to-site variations. A framework for pre-fabrication verification, post-fabrication evaluation, and site-calibration, and adaptive test flow strategies will improve robustness and effectiveness of tests.

SUMMARY OF RESULTS

Multisite systematic hardware error identification and calibration are extensively investigated. The L-moments method, which was developed in year two was improved. Three new calibration algorithms: the Least Squares approach, the Optimal Order approach, and the Neural Network approach are proposed. To evaluate the performance of these, the consistency of the algorithms for measurement calibration was studied and more test data from Texas Instruments were obtained for extensive validation. When the hardware systematic errors are identified and corrected, more accurate die specifications can be extracted from the raw measurement data. We proposed a principal component analysis method for issue site detection and extended the cross-correlation approach to the issue site detection method developed in year one by including derived boundary conditions. Tools to extract board parameters were further explored and developed. Finally, there was an extensive study on the root causes of site-to-site variation, and findings were documented.

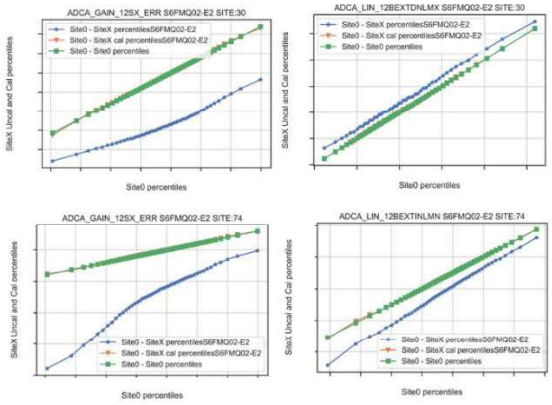


Figure 1. Hardware error correction effects for issue sites and good sites: blue is before, orange is after, and green is desired.

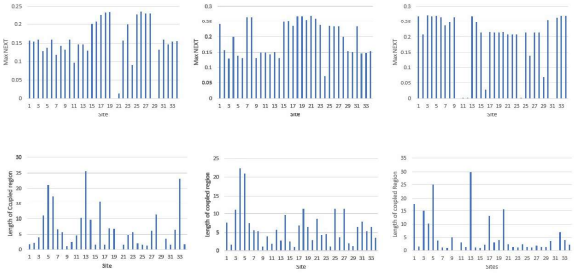


Figure 2. Example board analysis results showing near-end crosstalk and length of coupling region for some critical nets.

Keywords: Multi-site testing, test cost reduction, site-to-site variations, volume test data learning, ATE test hardware debug/design

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

[1] Farayola, et al, "The Least-Squares Approach to Systematic Error Identification and Calibration in Semiconductor Multisite Testing," 2022 IEEE 40th VLSI Test Symposium (VTS), 2022, pp. 1-6.

[2] Steenhoek, et al, “Graph Theory Approach for Multi-site ATE Board Parameter Extraction,” 2022 IEEE European Test Symposium (ETS).

[3] Farayola, et al, "Optimal Order Polynomial Transformation for Calibrating Systematic Errors in Multisite Testing," 2022 IEEE International Test Conference (ITC).

TASK 2810.029, 170GHz – 260GHz WIDEBAND PA AND LNA DESIGN IN SILICON

AYDIN BABAKHANI, THE UNIVERSITY OF CALIFORNIA AT LOS ANGELES
AYDINBABAKHANI@UCLA.EDU

SIGNIFICANCE AND OBJECTIVES

Wideband power amplifier (PA) and a low-noise amplifier (LNA) operating in the 170-260 GHz band using a commercial silicon process are critical components for future high-speed wireless communication links and high-resolution 3D-imaging radars.

TECHNICAL APPROACH

A single-ended LNA, taped out in a 130-nm SiGe process of IHP Microelectronics, was characterized with VNA measurements, and Y-factor noise figure measurements. A single-ended PA, taped out in a 130-nm SiGe process of IHP Microelectronics was characterized using VNA, and large-signal power measurements.

SUMMARY OF RESULTS

The LNA was fabricated in a 130-nm SiGe BiCMOS process. The DC power consumption is 46 mW. Fig. 1 shows the measured S-parameters. The LNA shows a peak measured gain of 15.5 dB at 207 GHz. The measured 3-dB bandwidth covers the entire WR5 frequency range from 140-220 GHz (fractional bandwidth of 44%). The Y-factor method is used for characterizing the noise performance of the amplifier. A VDI WR5 noise source, with a calibrated excess noise ratio (ENR), is used at the input. Fig. 2 shows the noise figure measured across four chips. A record noise figure of 6.9 dB, 6.1 dB, and 8.2 dB is measured at 150 GHz, 180 GHz, and 210 GHz, respectively.

The proposed PA was fabricated in a 130-nm SiGe BiCMOS process. A VNA setup is used for measuring the S-parameters in the WR5 band (140-220 GHz) and a WR8 VNA a VDI tripler is used at frequencies below 140 GHz (Fig. 3).

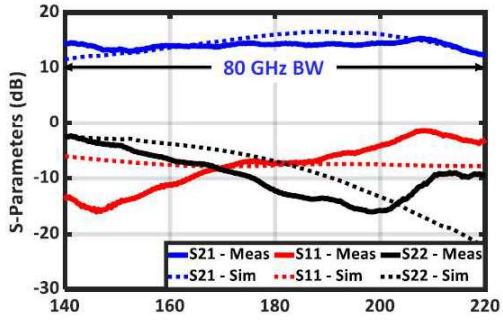


Figure 1. Measured small signal S-parameters of the LNA. Measurement results show a 3-dB bandwidth of 80 GHz.

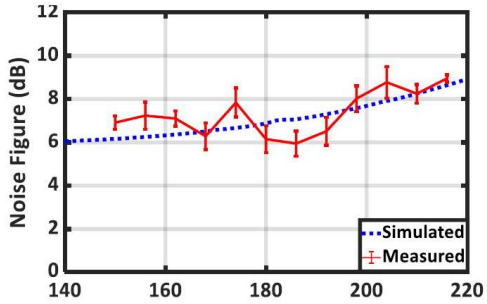


Figure 2. Noise figure measurements using the Y-factor technique.

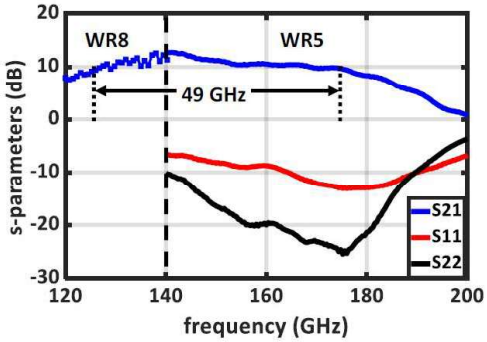


Figure 3. Measured small signal S-parameters of the PA. Measurement results show a 3-dB bandwidth of 49 GHz.

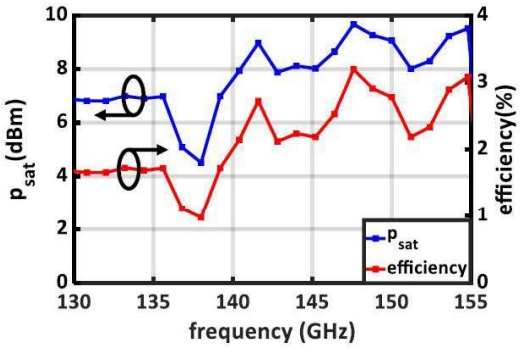


Figure 4. Measured saturation power and efficiency of the PA.

Keywords: LNA, PA, Wideband, Noise Figure, SiGe

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

TASK 2810.030, NEURAL NETWORK RECOGNITION & ON-CHIP ONLINE LEARNING WITH STT-MRAM

JOSEPH FRIEDMAN, UNIVERSITY OF TEXAS AT DALLAS, JOSEPH.FRIEDMAN@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

One of the primary hardware costs incurred by artificially-intelligent neural networks is due to vector-matrix multiplication (VMM), which is generally performed with floating-point binary numbers and computed exactly with cumbersome multiplication computations which scale with the number of entries in the matrix; *i.e.* $O(N^2)$.

TECHNICAL APPROACH

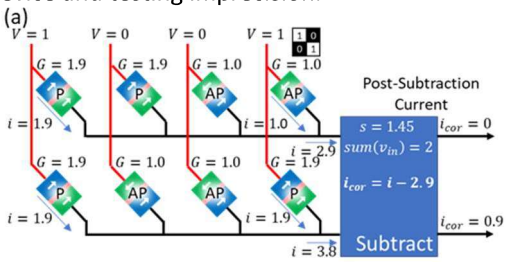
Most research in this area has focused on cross-bars composed of memristors and phase change memory (PCM). However, these devices suffer from several major challenges, including imprecise writing, weight drifting over time, limited endurance, and compatibility challenges with modern CMOS processes. Magnetic tunnel junctions (MTJs) provide solutions to the limitations of memristors and PCM, but only exhibit binary resistance states. Furthermore, it was recently proposed that stochastic MTJ switching should enable analog neuromorphic behaviors.

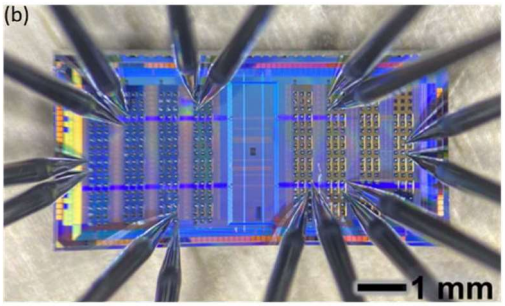
SUMMARY OF RESULTS

Our experiment demonstrates a 4x2 neuromorphic VMM accelerator, with eight two-terminal MTJ synapses as shown in Figs. 1(a)-(b). The four input voltages are provided by four power supplies (PS) and the two output currents are read by a source measuring unit (SMU). Each MTJ needs two probes to connect the top and bottom electrodes individually, thereby requiring a total of 16 probes for this 4x2 neuromorphic network.

To evaluate the functionality of the proposed system, we tested the system on the two-pixel by two-pixel supervised image classification task shown in Fig. 1(c). In this task, four input pixels are fed into the network, which is tasked with recognizing two target images. The network must calculate the Hamming distance between the input and target images, to which a threshold may be applied to identify images that are identical or sufficiently similar to the target image. The synapses in the network were trained offline to weights of either parallel (P) or anti-parallel (AP) MTJ resistance states.

Output currents normalized by the average AP state current are presented in Fig. 1(c). The output current variations result primarily due to power supply voltage variation and differences in probe connectivity. Significantly decreased variation is expected for future neuromorphic networks with MTJ arrays directly integrated with peripheral CMOS circuits. Fig. 1(c) includes the post-subtraction results of the normalized current. By setting proper thresholds, the post-subtraction results can be categorized into five distinct bins. These post-subtraction currents show high fidelity to the expected VMM results, demonstrating robustness to the device and testing imprecision.





(c)

Input Vector					Hamming Distance from Target		Normalized Output Current		Post-Subtraction Current		Expected VMM Output	
P1	P2	P3	P4		O1	O2	O1	O2	O1	O2	O1	O2
0	0	0	0		2	2	0.00	0.00	0.00	0.00	0	0
0	0	0	1		3	1	0.99	1.84	-0.45	0.40	-0.45	0.45
0	0	1	0		3	3	1.04	1.08	-0.40	-0.36	-0.45	-0.45
0	0	1	1		4	2	2.02	2.92	-0.86	0.04	-0.9	0
0	1	0	0		1	3	1.95	0.89	0.51	-0.55	0.45	-0.45
0	1	0	1		2	2	2.94	2.74	0.06	-0.14	0	0
0	1	1	0		2	4	3.00	1.95	0.12	-0.93	0	-0.9
0	1	1	1		3	3	3.97	3.80	-0.35	-0.52	-0.45	-0.45
1	0	0	0		1	1	1.87	1.98	0.43	0.54	0.45	0.45
1	0	0	1		2	0	2.84	3.81	-0.04	0.93	0	0.9
1	0	1	0		2	2	2.89	3.03	0.01	0.15	0	0
1	0	1	1		3	1	3.79	4.86	-0.53	0.54	-0.45	0.45
1	1	0	0		0	2	3.76	2.86	0.88	-0.02	0.9	0
1	1	0	1		1	1	4.74	4.75	0.42	0.43	0.45	0.45
1	1	1	0		1	3	4.63	3.87	0.31	-0.45	0.45	-0.45
1	1	1	1		2	2	5.73	5.57	-0.03	-0.19	0	0

Figure 1. Experimental setup and testing results.

Keywords: STT-MRAM, MTJ, Binarized Neural Network, Vector-Matrix Multiplication, Image Recognition

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] P. Zhou, J. S. Friedman, "Experimental Demonstration of Neuromorphic Network with STT MTJ Synapses," *GOMAC,* 2022.

[2] P. Zhou, J. S. Friedman, *IEEE International Electron Devices Meeting - MRAM Poster Session*, 2021.

TASK 2810.031, DEVELOPMENT AND ASSESSMENT OF MACHINE LEARNING BASED ANALOG AND MIXED-SIGNAL VERIFICATION

PENG LI, THE UNIVERSITY OF CALIFORNIA AT SANTA BARBARA, LIP@UCSB.EDU

SIGNIFICANCE AND OBJECTIVES

Wafer map pattern recognition is instrumental for detecting systemic manufacturing process issues for circuits. Labeling cost renders it impossible to leverage unlabeled data in conventional machine learning based wafer map pattern prediction. To mitigate this, a contrastive learning framework for semi-supervised learning and prediction of wafer map patterns is proposed.

TECHNICAL APPROACH

Our framework incorporates an encoder to learn good representation for wafer maps in an unsupervised manner, and a supervised head to recognize wafer map patterns [1]. In particular, contrastive learning is applied for the unsupervised encoder representation learning supported by augmented data generated by different transformations (views) of wafer maps. A set of transformations to effectively generate similar variants of each original pattern is identified. Furthermore, a novel rotation-twist transformation is proposed to augment wafer map data by rotating each given wafer map for which the angle of rotation is a smooth function of the radius.

SUMMARY OF RESULTS

A domain-specific application of contrastive learning for wafer pattern recognition is proposed. This general contrastive learning paradigm is shown in Figure 1. While the existing contrastive learning techniques have primarily focused on conventional image recognition and natural language processing tasks, the unique characteristics of the wafer pattern recognition task present new challenges and opportunities. First, the relevance of the transformations proposed in the literature is investigated. They act as a mechanism for data augmentation, and identify a near-optimal subset of transformations that are well-suited for meaningful characterization of similarities and dissimilarities of practical wafer pattern data. A set of transforms to effectively discover similarities among samples of the same wafer map pattern is identified. In addition, a novel twist transform is proposed through a smooth rotation at different radii to extract wafer map pattern similarity.

Experimental results demonstrate that the proposed semi-supervised learning framework greatly improves recognition accuracy compared to traditional supervised methods, and the rotation-twist transformation further enhances the recognition accuracy in both semi-supervised and supervised tasks.

As an example, Table 1 reports the wafer pattern recognition results of several methods based on the well-known WM-811K wafer map dataset. As can be seen, contrastive learning incorporating the proposed rotation-twist transformation achieve the highest performance at three different levels of labeled data availability when compared with other methods including the contrastive learning approach SimCLR developed for general image recognition tasks.

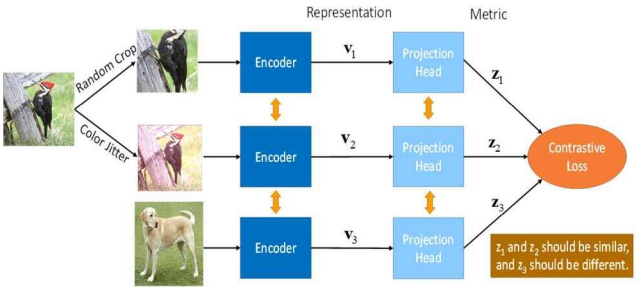


Figure 1. Semi-supervised learning based on contrastive learning.

Table 1. Results of wafer pattern recognition as a function of the percentage of available labelled data.

Methods	Label Percentage 1%	Label Percentage 5%	Label Percentage 20%
SVM	48.07%	46.99%	55.40%
CNN	64.87%	66.10%	77.90%
SimCLR	72.35%	72.05%	78.30%
CL+PT	72.42%	73.90%	80.23%
CL+PT+RoTwist	**73.27%**	**75.54%**	**82.19%**

Keywords: Manufacturing failures, wafer pattern recognition, semi-supervised learning, contrastive learning

INDUSTRY INTERACTIONS

NXP, Intel

MAJOR PAPERS/PATENTS

[1] H. Hu, et. al., "Semi-supervised Wafer Map Pattern Recognition using Domain-Specific Data Augmentation and Contrastive Learning," IEEE ITC'21.

[2] M.S. Shim, et. al., "Reversible Gating Architecture for Rare Failure Detection of Analog and Mixed-Signal Circuits," accepted to IEEE/ACM DAC'21.

TASK 2810.033, INTERLEAVED NOISE-SHAPING SAR ADCS FOR HIGH-SPEED AND HIGH-RESOLUTION

MICHAEL P. FLYNN, UNIVERSITY OF MICHIGAN, MPFLYNN@UMICH.EDU

SIGNIFICANCE AND OBJECTIVES

This research will deliver an energy-efficient high-speed, high-resolution ADC architecture for high-performance and emerging applications, including medical imaging, 4G/5G infrastructure, radar, production test, and defense. We will expand the bandwidth of our time-interleaved (TI) noise-shaping (NS) SAR architecture by an order of magnitude to extend SAR-ADC efficiency to high speed and high resolution.

TECHNICAL APPROACH

Our new SAR-based architecture combines time-interleaving with noise-shaping, to break the tradeoff between speed and accuracy, and enable both high speed and high resolution. The target design space is unserved by state-of-the-art SAR ADCs. Different from conventional SAR and interleaved SAR converters, our approach provides both high resolution and high bandwidth. We expand our revolutionary new interleaved noise-shaping SAR ADC architecture to deliver an order-of-magnitude more bandwidth, as well as improved energy efficiency.

SUMMARY OF RESULTS

The Noise-Shaping SAR (NS-SAR) is an emerging ADC architecture that offers both high resolution and high energy efficiency. State-of-the-art NS-SAR ADCs eliminate the need for op-amps, which relaxes design complexity and technology scaling issues. However, existing NS-SAR ADCs, with high FoM, are limited in bandwidth (typically in the MHz range). This makes NS-SAR ADCs unsuitable for applications that need bandwidths in the tens of MHz range, such as wireless communications. Traditionally, high-bandwidth, high-resolution applications utilize pipeline or continuous-time sigma-delta (CT-$\Sigma\Delta$) ADCs, but these architectures are much more power hungry than the NS-SAR.

Combining a CT DSM with an NS quantizer (QTZ) provides excellent efficiency, robust operation, and the benefits of a CT input. Nevertheless, existing CT ADCs with NS QTZs are limited in resolution and bandwidth. Conventional methods for increasing resolution and bandwidth are challenging: (1) The usable time for the QTZ is limited; (2) Increasing QTZ resolution reduces the NS QTZ sampling rate; (3) The loading of the NS QTZ limits the performance of the CT frontend, and (4) Increasing the CT loop-filter order can cause excessive out- of-band gain. This work tackles the speed-resolution bottleneck of the NS QTZ to address these challenges. Introducing a delay in the NS QTZ feedback loop enables complete parallelization of the NS QTZ operations (Figure 1). The extra time from parallelization greatly relaxes loop filtering and residue integration and enables a high (6-bit) QTZ resolution. Furthermore, the extra time in the feedback loop permits DWA (Data Weight Averaging) to eliminate the need for calibration. The prototype comprises a 2nd order CT frontend and a fully interleaved 1st order NS QTZ.

A new Hybrid-Loop (HL) DSM architecture (Figure 2), which combines the advantages of both CT and DT DSMs and eliminates the drawbacks is proposed. A bandpass, time-interleaved noise-shaping (TINS) SAR quantizer further boosts the performance. The prototype HL-DSM provides 68dB SNDR over a 100MHz BW for a quadrature input, without any calibration or tuning, while occupying only 0.09mm^2 and consuming 13mW at 1.6GS/s. The resulting 166dB FoMs show the potential of HL-DSM as a more robust and practical alternative to CT-DSM.

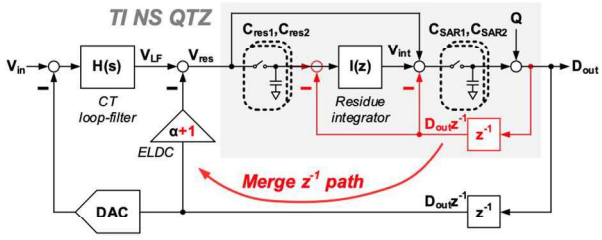


Figure 1. CT SDM with new TI NS QTZ merges ELD paths.

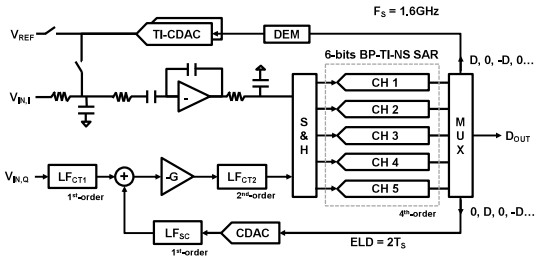


Figure 2. Hybrid CT DT Interleaved NS SAR.

Keywords: Sigma Delta, ADC, sensor, SAR, IoT

INDUSTRY INTERACTIONS

Texas Instruments, Intel, ARM, NXP

MAJOR PAPERS/PATENTS

[1] L. Jie, H. -W. Chen, B. Zheng, and M. P. Flynn, "A Hybrid-Loop Structure and Interleaved Noise-Shaped Quantizer for a Robust 100-MHz BW and 69-dB DR DSM," in IEEE Journal of Solid-State Circuits, vol. 56, no. 12, pp. 3681-3693, Dec. 2021.

TASK 2810.036, HIGHLY STABLE INTEGRATED FREQUENCY REFERENCES

PAVAN KUMAR HANUMOLU, UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN,
HANUMOLU@ILLINOIS.EDU

SIGNIFICANCE AND OBJECTIVES

On-chip RC oscillators are getting popular as clock references due to their low power, small area, and cost-efficiency. However, poor frequency accuracy has limited their usage to systems tolerating ~1% inaccuracy. The objective is to achieve <±250ppm frequency accuracy at low power making it suitable for real-time clock sources.

TECHNICAL APPROACH

We use a method for precise and robust cancellation of the resistor temperature coefficient (TC) using a parallel combination of three switched-resistors (SRs) that are digitally controlled by pulse-density modulated sequences. For excellent temperature stability, we propose a low-leakage switched-capacitor resistor (SCR) and the second-order compensation scheme which is independent of the sign of resistor TC.

SUMMARY OF RESULTS

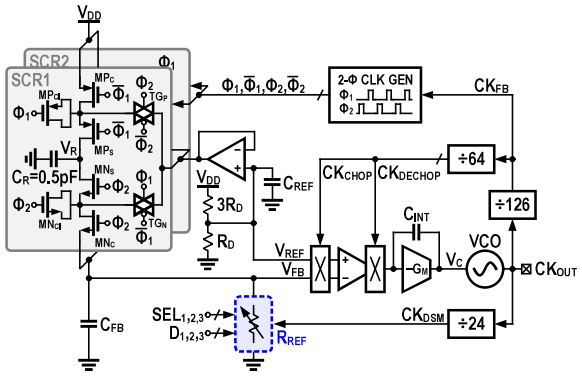


Figure 1. Proposed TCO architecture.

A proposed temperature compensated oscillator is shown in Fig. 1. It is composed of a frequency-locked loop that locks the period of a voltage-controlled ring oscillator (VCO) to a reference time constant ($1/F_{OUT} = 6R_{REF}C_R/126$). A voltage divider formed by an SCR and a reference resistor (R_{REF}) generates frequency-dependent voltage, V_{FB}. The feedback loop is closed by driving the VCO with the integrated difference between V_{FB}, and a fixed reference voltage (V_{REF}). Thanks to the large loop gain, $V_{FB} \approx V_{REF}$ and $F_{OUT} \approx 100$MHz in steady-state. The accuracy of F_{OUT} over temperature and supply variations is largely dictated by SCR and R_{REF}. In Fig. 1, the off-state leakage current of the PMOS switch (M_{PC}) is steered away from C_{FB} to the buffer output using a transmission gate (TG_P). A PMOS transistor (M_{PS}) is added to prevent C_R from being connected to the buffer output voltage. Because M_{PS} source is connected to $V_{DD}/4$ and its drain is discharged to $V_{DD}/4$, V_{DS} of M_{PS} equals zero, thus significantly reducing its leakage.

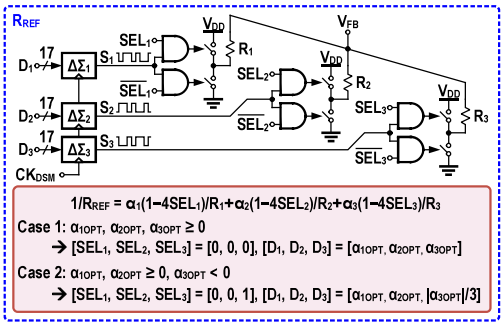


Figure 2. Reference resistor schematic.

Fig. 2 shows the details of the reference resistor. R_{REF} is implemented using three SRs, R_1, R_2, and R_3, that are controlled by sequences, $S_1/S_2/S_3$ generated by three ΔΣ modulators. Each resistor can be either connected to ground or V_{DD} using low-leakage switches controlled by select signals $SEL_1/SEL_2/SEL_3$. This programmability eliminates the need for resistors with opposite TCs.

A prototype was fabricated in a 65-nm CMOS process and packaged in a plastic QFN package. It occupies an area of 0.19mm^2 and draws 84.5µA from a 1.2V supply. The measured frequency accuracy for 20 samples after three-point trim using p-poly, n-diffusion, and p-diffusion resistors is less than ±140ppm over -40°C to 95°C (2.1ppm/°C). The supply sensitivity is 83ppm/V over a V_{DD} range of 1.1 to 2.5V. The obtained optimum alphas after three-point trim from twenty samples using p-poly resistor, n-diffusion resistor, and p-diffusion resistor have strong correlation. A scatterplot shows strong correlation with a correlation coefficient, R^2 of 0.94. When a single-point trim at room temperature (RT) is performed by leveraging the strong correlation among alphas, a frequency inaccuracy of 587 ppm from -40 ◦C to 95 ◦C (8.7 ppm/◦C) is achieved.

Keywords: Switched capacitor, switched resistor, Delta–sigma modulator, pulse density modulation, RC oscillator

INDUSTRY INTERACTIONS

NXP, Texas Instruments

MAJOR PAPERS/PATENTS

[1] K.-S. Park et al., “A second-order temperature compensated 1µW/MHz 100MHz RC oscillator with ±140ppm inaccuracy from −40°C to 95°C,” in 2021 CICC, April 2021.

TASK 2810.037, HIGH-PERFORMANCE RINGAMP-BASED ADCS

UN-KU MOON, OREGON STATE UNIVERSITY, MOON@EECS.OREGONSTATE.EDU

SIGNIFICANCE AND OBJECTIVES

Our research goal is to solidify ring amplifiers as a dominant means of closed-loop precision amplification and fast integration in mixed-mode circuits through the demonstration of performance improvements over traditional amplifiers. In this task, high-performance ring amplifier-based ADCs in FinFET technology are explored, addressing the current need for high-speed and high-resolution applications in scalable CMOS.

TECHNICAL APPROACH

Instead of utilizing single loop noise shaping successive-approximation (NSSAR) ADC, this report demonstrates a proposed architecture of multi-stage noise-shaping (MASH) structure with NSSAR ADCs. The proposed intrinsically stable 4th order MASH NSSAR ADC not only takes advantage of sharp noise shaping but also benefits from hardware reuse. With an ultra-low oversampling ratio (OSR), the MASH NSSAR is realized in a 22-nm FinFET process with a 0.9V supply. The noise leakage introduced by the analog and digital mismatch has minor effects on the performance of the whole ADC. PVT stable ring amplifiers that can achieve high-speed precision amplification and fast integration are also incorporated. With 50MHz bandwidth (OSR=3), the topology can yield ~78-dB SNDR.

SUMMARY OF RESULTS

The intrinsically stable 4th order MASH is shown in Fig. 1. Stage1 uses an error feedback (EF) structure. Gain (32X) variation of the amplifier under process, voltage, and temperature (PVT) can greatly deteriorate the noise transfer function (NTF). Previous work utilized an open loop dynamic opamp with complex digital calibration to achieve acceptable results. The proposed ring amplifier working in closed loop operation with a gain of 32 can replace the open loop opamp to provide a precise and PVT stable gain. The 1/16 gain coefficient in the feedback path of the stage1 is generated by capacitor charge sharing.

The stage1 feedback opamp is reused to provide inter-stage gain onto the next stage. Quantization noise from the stage1 SAR is amplified by the residue amplifier and sent to the second stage. Due to the large precise inter-stage gain, stage2 works with reduced accuracy, and low power consumption noise shaping circuits. In stage2, the filter is realized by a low gain but fast settling ring amplifier with much lower power and a simpler structure.

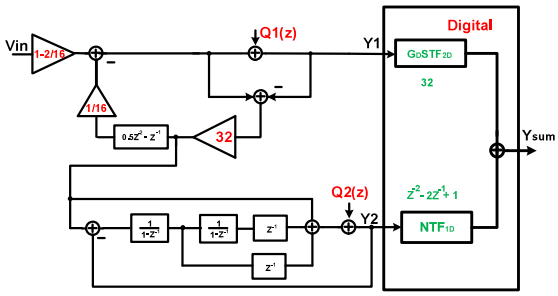


Figure 1. Topology of the proposed architecture.

Noise leakage issues have also been analyzed. Under a reasonable mismatch range, there is no need for digital calibration. The design has been implemented in a 22-nm process. The simulation results show that, with ultra-low OSR (3), ~78-dB SNDR can be achieved, as summarized in Table 1. The anticipated power consumption is 6.7mW. In the proposed MASH topology, it can efficiently reach high speed, when compared to a discrete-time MASH delta-sigma ADC which requires large power consumption due to the multiplicity of integrators. Our proposed structure also avoids the unavoidable complex digital calibration in high-speed continuous-time MASH delta-sigma ADCs. This structure presents the best-to-date low-OSR architecture, combined with speed, calibration simplicity (i.e., can be avoided), and power consumption.

Table 1. 50M bandwidth with a corner.

Corner	tt	ss	ff
Temp (°C)	25	100	-40
SQNR(dB)	77.6	70.5	75.5

Keywords: MASH, noise shaping SAR, ultra-low-OSR, high resolution, ring amplifier

INDUSTRY INTERACTIONS

Texas Instruments, NXP, Intel

MAJOR PAPERS/PATENTS

[1] C.Y. Lee *et. al.*, "A 0.0375mm^2 203.5uW 108.8dB DR DT single-loop DSM audio ADC using a single-ended ring-amplifier-based integrator in 180nm CMOS," *IEEE Int. Solid-State Circuits Conf.*, Feb. 2022.

[2] H. Hu *et al.*, "Passive third order continuous-time ΔΣ modulator with Q enhancement technique," *IEEE Int. Symp. Circuits Syst.*, May 2022.

[3] H. Hu *et al.*, "Ultra-Low OSR calibration free MASH noise shaping SAR ADC," *IEEE Int. Symp. Circuit Syst.*, May 2022.

TASK 2810.043, ANALOG OPTIMIZATION HYBRIDIZING DESIGNER'S INTENT AND MACHINE LEARNING

PENG LI, THE UNIVERSITY OF CALIFORNIA AT SANTA BARBARA, LIP@UCSB.EDU

SIGNIFICANCE AND OBJECTIVES

Analog circuit design and optimization manifest as a critical phase in IC design, which still heavily relies on extensive and time-consuming manual designing by experienced experts. Building upon recent advances in machine learning, we develop a sample-efficient reinforcement learning (RL) algorithm and a design tool for automated Pareto-optimal analog sizing optimization.

TECHNICAL APPROACH

Analog circuit optimization and design present a unique set of challenges. With embedded and edge devices on the rise, the need for faster optimization procedures is increasing. Furthermore, many applications require a designer to optimize for multiple competing objectives which poses a crucial challenge. Motivated by these practical aspects, we propose a novel method to tackle multi-objective optimization for analog circuit design in continuous action spaces using reinforcement learning. In particular, we propose: (i) To extrapolate current techniques in Multi-Objective Reinforcement Learning (MORL) to continuous state and action spaces. (ii) We provide a dynamically tunable trained model to query user-defined preferences in multi-objective optimization in the analog circuit design context [1].

SUMMARY OF RESULTS

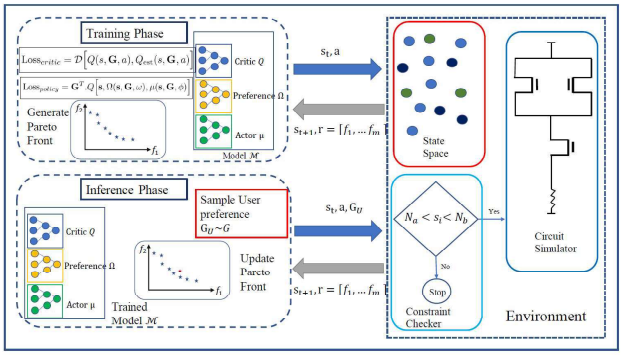


Figure 1. Proposed reinforcement learning for multi-objective analog design optimization.

Figure 1 illustrates the proposed reinforcement learning (RL) approach for multi-objective analog optimization [1]. Specifically, we propose a sample-efficient and easy-to-train, multi-objective reinforcement learning (MORL) algorithm to form a well approximated Pareto set of the analog circuit, where the actions of the RL agent (fine-tuned sizing solutions) are continuous valued. Next, we use the predictive power of the trained RL agent to demonstrate that the RL agent supports querying the analog circuit for user-defined / custom preferences among objectives to be optimized for. Our work presents a model to query for unseen design points in the training process, based on the designer's choice and helps augment the current Pareto set. We demonstrate through extensive experiments, the effectiveness of using the proposed RL algorithm for blackbox multi-objective analog circuit optimization. We illustrate the performance improvements of our algorithm over previous methods.

Figure 2 compares several methods on optimization of the gain and bandwidth of a two-stage differential amplifier. We compare our method (RL-train) with genetic algorithm (NSGA-II), Monte-Carlo sampling, and Bayesian optimization (BO). As can be seen, RL-train produces the best overall Pareto front among all these four methods. Future work will investigate sample-efficient RL based analog design optimization while considering the impacts of process variations.

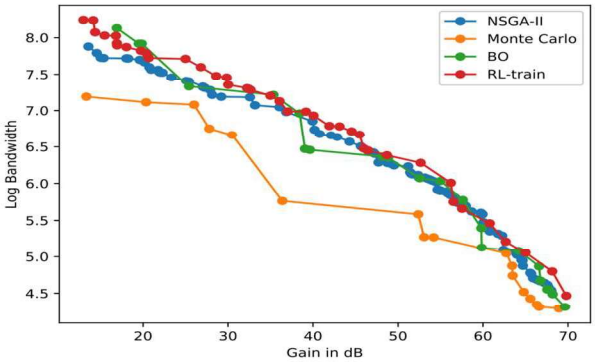


Figure 2. Optimization of a two-stage amplifier.

Keywords: analog optimization, reinforcement learning, multi-objective optimization, design productivity

INDUSTRY INTERACTIONS

NXP, Intel

MAJOR PAPERS/PATENTS

TASK 2810.044, HIERARCHICAL CHARACTERIZATION AND CALIBRATION OF RF/ANALOG CIRCUITS USING LIGHTWEIGHT BUILT-IN SENSORS

SULE OZEV, ARIZONA STATE UNIVERSITY, SULE.OZEV@ASU.EDU

SIGNIFICANCE AND OBJECTIVES

This project will explore a hierarchical calibration approach, including local calibration and system-level target setting, where information from built-in monitors is used to match the performance of individual blocks, as well as to guarantee that the entire system functions in cohesion even if constraints or operating conditions change dynamically.

TECHNICAL APPROACH

Simple built-in sensors that measure current, DC voltages, and RF power are used to set local circuit parameters, such as circuit bias or matching components, to optimize the performance for given specifications. System-level calibration will rely on a statistical model (e.g., machine learning), whereas circuit-level calibration can be conducted with simplified mathematical models.

SUMMARY OF RESULTS

Since direct measurement of the incident and reflected test signals requires a high-overhead RF interface, mismatch information is indirectly measured using multiple low-overhead sensors such as power detectors. These detectors are strategically placed in different parts of the circuit to maximize measurement sensitivity. S_{11} measurement approaches can be generalized as six-port network analyzers. A six-port network analyzer consists of a passive network with at least four ports for the power detectors, one port for the load, and one port for the signal source. Existing methods aim at directly determining the matching parameter and they require external calibration, which makes them unsuitable for a BIST application. Our work solves the necessity of calibration by referencing all measurements to a small set of parameters and conducting measurements in two steps. In each step reflection coefficient of one load is measured. Since each measurement is referenced to the same parameters, these measurements can be used to assess the mismatch amount of the two loads and gives information on how both loads compare to each other. We also fabricated and tested the design example. The measurements confirm that this method can be used for mismatch detection and return loss estimation.

As can be seen in Figure 2, the proposed heuristic tuning approach significantly improves S_{11} as compared to its value before tuning. The proposed heuristic tuning approach also provides very close results to the traditional tuning approach that requires an external RF instrument.

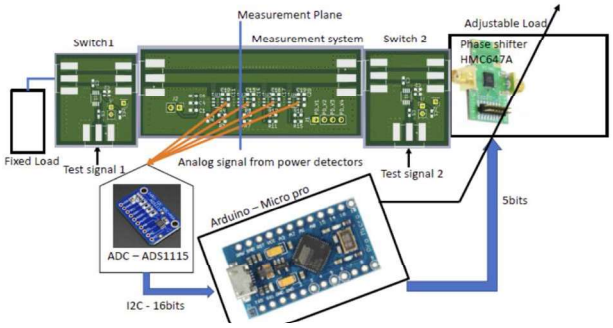


Figure 1. Experimental Set-up.

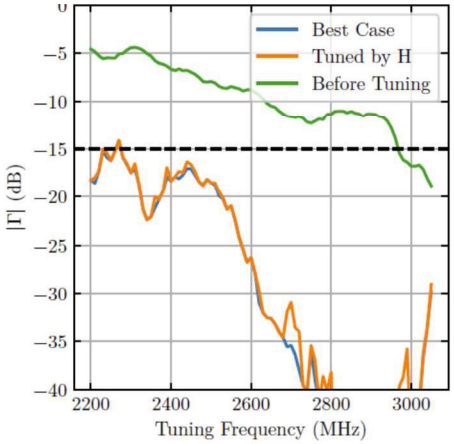


Figure 2. Tuning results with proposed approach.

Keywords: RF BIST, cascade, automotive radar, tuning

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

[1] Avci, Muslum Emir, Sule Ozev, and YB Chethan Kumar. "Fast RF Mismatch Calibration Using Built-in Detectors." In 2022 IEEE 40th VLSI Test Symposium (VTS), pp. 1-7. IEEE, 2022.

TASK 2810.052, TI PLM AS HOLOGRAM GENERATOR FOR HUD AND AR

PIERRE-ALEXANDRE BLANCHE, UNIVERSITY OF ARIZONA,
PABLANCHE@OPTICS.ARIZONA.EDU

SIGNIFICANCE AND OBJECTIVES

The goal of this effort is to use the Texas Instruments PLM to create a holographic display for AR and HUD applications. The use of the Texas Instruments PLM has the potential for high impact to both the scientific and consumer electronic worlds.

TECHNICAL APPROACH

This task is applying the PLM-DLP laser beam steering technology for time-multiplexed monochromatic image transfer in free space and evaluating field of view (FOV), image resolution, and applicability to image transfer of 3D displays. This task will also update the Gerchberg–Saxton type algorithm software for the computation of the holographic pattern, use the temporal multiplexing capability of the PLM to reduce the speckle noise and use narrow bandwidth incoherent illumination to further reduce the speckle noise. Lastly, this task will develop a full-color holographic 3D display with large FOV and improved image quality using the PLM-DLP.

SUMMARY OF RESULTS

Computer-generated holograms (CGHs) used for AR/VR displays typically have poor image quality compared to numerical reconstructions. The primary cause of these discrepancies can be attributed to over-idealized wave propagation used for CGH generation. This problem is often exacerbated when the image is projected through a more complex optical system like a holographic waveguide combiner. Direct camera feedback during hologram optimization has been shown to significantly improve image quality for CGHs projected in free space. Here we demonstrate the use of camera feedback optimization for improving the image quality of CGHs projected through holographic waveguide combiners. Machine learning can be applied to adjust the numerical propagation method to better match physical propagation through the system without the need for camera feedback. This method corrects for various optical aberrations, beam profiles, and phase nonlinearities in the display. Further image improvement is made by leveraging high-speed MEMS-based phase light modulators for time multiplexing CGHs to reduce speckles.

We implemented a camera in the loop (CITL) algorithm that dramatically improved the image resolution of our computer-generated holograms (CGH). Figure 1 presents some of the holographic images captured in our setup. Target image, numerical image reconstruction, and camera feedback image are all used in each iteration to optimize the phase pattern of the CGHs. The camera feedback image is compared to numerical reconstruction to determine differences between the optical system and numeric calculations. This algorithm can correct for the discrepancy between the light propagation model and the actual setup. Even the optical aberrations introduced in the setup can be taken care of. However, this image quality improvement comes at the cost of a significantly increased computation time. The algorithm also requires a camera in the optical system, and good mechanical stability.

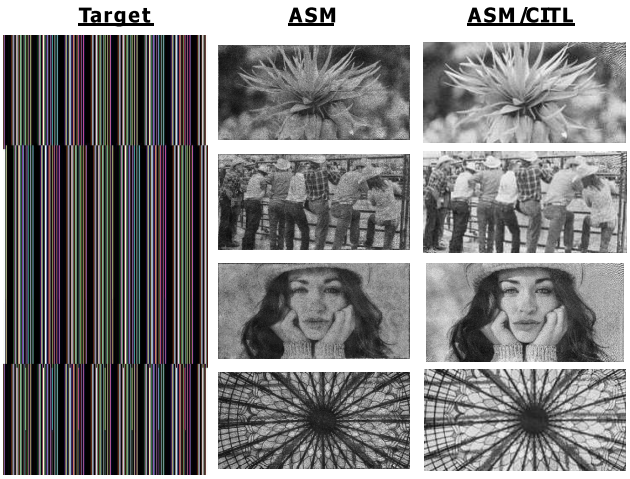


Figure 1. Holographic image comparison between the original target, physical model propagation (ASM), and camera in the look (ASM/CITL) optimization.

The operation takes on the order of 5 minutes. To improve the CGH calculation speed, we are implementing a neural network algorithm that is trained using the CITL phase hologram. Since the CITL images have a much better resolution than the images obtained using the ASM method, we are expecting better results with this new neural network. Early results have shown that neural network hologram generation is order of magnitude faster than both ASM and CITL.

Keywords: computer generated hologram, holographic display, phase light modulator

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

TASK 2810.053, TI PLM TO ADVANCED LIDAR AND DISPLAY SYSTEMS

YUZURU TAKASHIMA, UNIVERSITY OF ARIZONA, YTAKASHIMA@OPTICS.ARIZONA.EDU

SIGNIFICANCE AND OBJECTIVES

Texas Instrument Phase Light Modulator (TI PLM) and Digital Micromirror Device (DMD) enable control of the light in a very fast and flexible manner, and are a key enabler of automotive and consumer optical devices such as lidar, head-up display, headlight, augmented reality (AR) display being used with advanced optoelectronics and cameras.

TECHNICAL APPROACH

We have unlocked unexplored capabilities of PLM and DMD for lidar and AR display by synchronous pulse illumination to PLM and DMD. For lidar, the light recycling concept turned PLM for visible light into a high-efficiency infrared beam steering device. An efficient equalization algorithm generates a computer-generated hologram (CGH) that makes PLM into a foveated beam steerer that captures both near and far objects simultaneously. A new solid-state lidar optical architecture with DMD and PLM expands the field of view (FOV) by a factor of 10. For AR display, a wide FOV image is displayed via an optical waveguide, by employing wavelength and polarization multiplexing.

SUMMARY OF RESULTS

PLM for infrared lidar beam steerer: TI-PLM is a very fast and flexible light modulation device with a kHz refresh rate which enables fast laser beam steering, intelligent lighting, and high-fidelity holographic display for automotive and AR applications. The current generation of PLM for visible light suffers from a low diffraction efficiency (15%) in infrared (IR) at 1.55um for lidar applications. Also, limited field of view (of several degrees) and undesired diffraction orders are major challenges for both lidar and AR displays. A new concept, self-pixel matching increased the diffraction efficiency at IR by a factor of 2 (from 15% to 30%, Fig. 1).

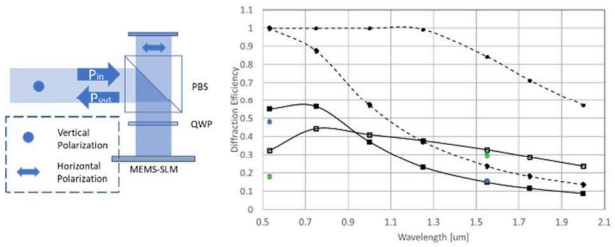


Figure 1. Optical architecture for IR beam steering (left) and diffraction efficiency as a function of wavelength (right).

TI-PLM as a sub-wavelength pixel equivalent phased array for lidar and AR display: The field of view (FOV) is limited by λ/d which λ is a wavelength and d is a pixel period. PLM and DMD have a pixel period of $d >> \lambda$, that limits FOV up to several degrees, and produce side-lobes. Sub-wavelength optical phased array is expected to solve the problem, though challenges such as scaling up to a $100mm^2$ device area is elusive. A new optical architecture employing the PLM and DMD increased the FOV from several degrees to 50 degrees, which is equivalent to a pixel period of $d = 0.5\lambda$ (Fig. 2). The optical reduction of the pixel period of a large area PLM opened a pathway to all-MEMS beam steering for lidar, and foveated and high-resolution display for AR by using COTs devices.

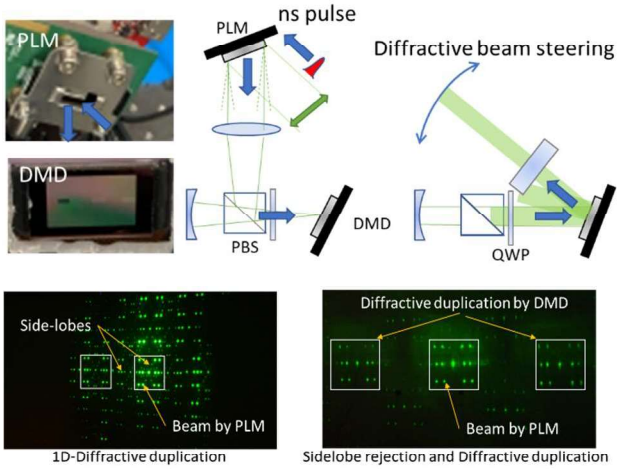


Figure 2. Optical architecture for the IR beam steering (top) and wide FOV and side-lobe free beam pattern (bottom).

Keywords: lidar, AR display, beam steering, image steering, CGH

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Z. Dong et al., "Optical enhancement of diffraction efficiency of Texas Instrument Phase Light Modulator by Talbot imaging-based pixel matching for infrared lidar beam steering," SPIE, Emerging Digital Micromirror Device Based Systems and Applications XIV, 2022.

[2] X. Deng et al., "Solid-state beam steering with adaptive side lobe rejection and enhanced angular throw of MEMS phase SLM by angular spatial and phase combined modulation," SPIE, Emerging Digital Micromirror Device Based Systems and Applications XIV, 2022.

TASK 2810.056, MILLIMETER WAVE PACKAGING RESEARCH-ANTENNA IN PACKAGE

RASHAUNDA HENDERSON, UNIVERSITY OF TEXAS AT DALLAS, RMH072000@UTDALLAS.EDU
MARK LEE AND HONGBING LU, UNIVERSITY OF TEXAS AT DALLAS

SIGNIFICANCE AND OBJECTIVES

Antenna in package (AiP) is a key enabler for future millimeter-wave front-end modules. This research project focuses on the design and characterization of antennas integrated into various package types incorporating the proper antenna feeds, transmission lines and chip-to-package interconnects along with packaging materials. The goal is to meet the mm-wave and mechanical requirements over the WR8 and WR5 frequency bands.

TECHNICAL APPROACH

Phase 2 of this project has resulted in down-selecting antennas and package technologies to be implemented in two test vehicles/package prototype structures. Through electromagnetic (EM) simulations, optimized antenna designs, transmission lines, and transition structures were developed. Unique methods have been incorporated to characterize the antennas for input impedance and radiation patterns operating at WR8 and WR5 bands, 90-140 GHz and 140-220 GHz. Mechanical vibration testing of AiPs has been conducted for the development of a failure analysis model. Commercially available packaging mold compounds and laminates have been characterized at room and elevated temperatures, to extract dielectric properties for accurate EM simulation.

SUMMARY OF RESULTS

Antenna-in-package (AiP) simulations of slot bowtie antennas have been conducted using Ansys HFSS. Included in the design of the coplanar waveguide (CPW) fed standalone antenna, is the optimization of a transition from a silicon IC within an enhanced quad flat pad with no leads (QFN) package. Figure 1 shows the cross-section including the IC and copper rod solder bumps to transition an RF signal from the chip to the packaged antenna. Surface roughness and the properties of the over mold material are included in the EM simulation.

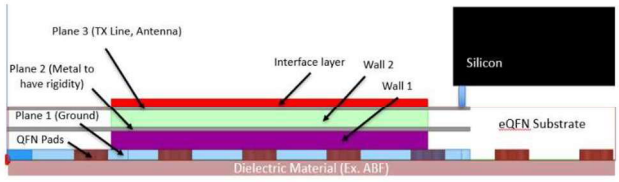


Figure 1. Flip-chip enhanced QFN package test vehicle cross-section.

Liquid crystal polymer (LCP) compounds have been characterized to provide precise dielectric properties in the WR5 band. This data is useful to accurately model the performance of packaged antennas. Extensive material characterization of commercially supplied LCP premolds has been conducted using free-space techniques. Phase-sensitive transmission scattering parameter measurements (S_{21}) have been made using a 2-port vector network analyzer and WR5 rectangular waveguide components [1]. Table 1 summarizes the performance of Sumitomo Chemical (SC), RTP Company (RTP), and Celanese Corporation (CC) products.

Table 1. Average D_k and D_f values of liquid crystal polymer materials were measured at room temperature.

Sample	Average Dk (180 GHz)	Average Df (180 GHz)	Dispersive (Dk or Df)
SC1	3.05±0.01	0.0133±0.001	Df
SC2	4.07±0.01	0.0176±0.001	Df
SC3	2.85±0.12	0.0146±0.001	Df
RTP	4.52±0.08	0.0201±0.002	Non-dispersive
CC1	2.45±0.04	0.0440±0.002	Dk
CC2	2.20±0.02	0.0356±0.001	Dk

Test vehicle 1 includes ground-signal-ground (GSG) structures for traditional probe characterization and novel waveguide-to-board transitions to isolate the antenna under test from the RF signal and minimize parasitic radiation.

Keywords: Enhanced QFN package, planar antennas, transmission line, chip-package transitions

INDUSTRY INTERACTIONS

Texas Instruments, Intel, NXP

MAJOR PAPERS/PATENTS

[1] M. P. McGarry, M. K. Iyer, M. Lee, "Broadband Millimeter-Wave Dielectric Properties of Liquid Crystal Polymer Materials," IEEE Trans. Compon. Packag. Technol., vol. 12, no. 1, Jan. 2022, pp. 192-194.
[2] A. N. Jogalekar, O. Medina, R. M. Henderson, M. Iyer, "Slot Bow-Tie Antenna Integration in an Enhanced Flip-Chip QFN Package for WR8 and WR5 Band Applications," IEEE MTT-S International Microwave and RF Conference (IMaRC) 2021, Dec. 2021.

TASK 2810.058, MACHINE LEARNING-BASED OVERKILL/UNDERKILL REDUCTION IN ANALOG/RF IC TESTING

YIORGOS MAKRIS, UNIVERSITY OF TEXAS AT DALLAS, YIORGOS.MAKRIS@UTDALLAS.EDU

SIGNIFICANCE AND OBJECTIVES

With the rising complexity of semiconductor devices, the testing procedures have become complex and time-consuming. Depending on the nature of the test solution, some good chips will get discarded (overkill) or some defective chips being retained (underkill). We exploit machine learning-based solutions to develop a comprehensive yield management scheme.

TECHNICAL APPROACH

For the problem of overkill, we propose a three-step approach that predicts the values of auxiliary tests using multivariate regression models, clusters that predicted the actual outcomes of auxiliary tests, and finally combine the two outcomes along with a proximity-based metric to decide on the devices to recover. For underkill, we use the probe test measurements of devices across multiple insertions to train a Gaussian mixture model to identify devices that have a higher probability of failure on-site and become a customer return. Due to the vastness of probe test measurements, we perform feature space exploration to extract signatures from customer returns.

SUMMARY OF RESULTS

For mitigating overkill, an industrial dataset of 92,022 devices with measurements from 66 specification tests and 241 auxiliary tests is utilized. Out of the 92,022 devices, 9.6% of devices fall into our focus group which passes the specification tests but fails one or more auxiliary tests. We used the 87.21% of devices that passed both sets of tests as predictors in the regression model to predict the failing auxiliary test measurements for the 9.6% of the devices.

Table 1. Test Outcome after Regression.

		Specification Tests	
		Pass	**Fail**
Auxiliary Tests	**Pass**	80261 + **8235**	**605**
	Fail	726	2195

Based on Table 1, we can observe that by predicting failing auxiliary test measurements we were able to recover 8,235 devices but there is no ground truth to verify our results. Using these predicted outcomes and actual outcomes of the auxiliary tests for the devices under test, we cluster them to address the sub-optimally defined test limits. Combining the both results, we get three buckets of devices. In one of these buckets, the two outcomes diverge, and we use a proximity-based metric to decide. Using this approach, we were able to recover 81.6% of devices from our focus group.

For mitigating underkill, an industrial dataset of 24,000 devices was utilized. These are collected from 19 wafers. The dataset consisted of 19 customer returns (one for each wafer) and each of these can be further broadly classified into different fault-id on return analysis. As a first step, we perform feature space exploration to generate a hyperspace that can separate the distribution of faulty devices from nominal devices, using the differential in probe test measurements across hot and room temperature insertions. Any abnormal variation in device measurements across the insertions is indicative of a failure.

Due to the gaussian nature of test measurements across a wafer, we perform unsupervised Gaussian mixture model clustering. The clusters whose gaussian mean are further from the means of the nominal devices have a higher probability of failure as shown using the heat map in Figure 1. The customer return devices are outliers coming from different corners of the distribution.

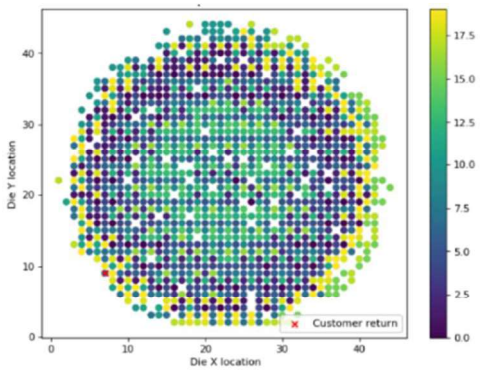


Figure 1. Wafer heat maps of GMM clusters.

Keywords: yield recovery, machine learning, adaptive testing

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] D. Neethirajan, V. A. Niranjan, R. Willis, D. Webster, A. Nahar, and Y. Makris, “Machine Learning-Based Overkill Reduction through Inter-Test Correlation,” IEEE VLSI Test Symposium (VTS), 2022.

TASK 2810.060 INTELLIGENT LEARNING ADCS FOR THE POST FIGURE OF MERIT WORLD

MICHAEL FLYNN, UNIVERSITY OF MICHIGAN, MPFLYNN@UMICH.EDU

SIGNIFICANCE AND OBJECTIVES

Although there has been tremendous progress in ADC performance, the research community has focused on energy efficiency, and in particular energy Figure of Merit (FoM). This research will redefine ADCs as information extraction tools, dramatically increasing their capability and utility in communication and sensing systems.

TECHNICAL APPROACH

Existing sensor interfaces also create too much data and provide too little information. Machine learning approaches, such as feature extraction and classification, can overcome bandwidth and power limitations; however, traditional machine-learning methods are expensive. We propose a new class of intelligent and aware ADCs that directly extract information.

SUMMARY OF RESULTS

Our bitstream processing approach embeds neural-network processing directly at the delta-sigma bitstream output. Sophisticated processing, performed directly on delta-sigma bitstream output, removes the need for conventional power-hungry DSP. With embedded machine learning capabilities, the data bandwidth generated by the interface is reduced by orders of magnitude.

We use bitstream processing (BSP) to implement a bitstream neural network (BSNN) provides to add learning and classification capabilities within the ADC. In delta-sigma modulation, the combination of oversampling and noise shaping enables a high SNR modulator output with a single-bit (or low-resolution) quantizer. Conventionally, the low-resolution digital output of the delta-sigma modulator is low-pass filtered and decimated before further DSP. In the conventional approach, DSP is performed at a lower clock rate after decimation but at the cost of an increased word width. In BSP, on the other hand, the bitstream modulator output is directly processed to take advantage of the low word width. This approach was first proposed in to realize a multiplier-less digital filter with a single-bit delta modulator output. A significant advantage of BSP is that it replaces large multipliers with simple MUXs. The need for decimation can be eliminated or significantly reduced.

Our ASR (Automatic Speech Recognition) frontend system (Fig. 1) addresses the problems of conventional ABF (Analog Beam Forming) with: (1) Low DSP power consumption (3x lower than state-of-art ABF [4]) thanks to an innovative greedy blocking matrix (GBM) with simple calculations and a reduced-sample-rate ADC; (2) Automatic Direction of Arrival (DOA) error compensation with a Delay and Sum (DAS) tracking beamformer (DTDAS) aided by the GBM, (3) A multi-mode hybrid ADC architecture adapts to signal conditions and consumes an order-of-magnitude less power than the state-of-art; and (4) Multi-mode beamforming takes advantage of high signal SNR to reduce power consumption by up to 46%.

Our speech-processing frontend connects to four microphones and outputs frequency- domain speech features (Fig 1). After digitization by the multi-mode ADC array, the DTDAS beamformer corrects speaker-direction estimate errors by appropriately time- aligning the ADC outputs. DTDAS generates an enhanced target signal OUTDAS and outputs correctly aligned ADC outputs, x1-4. Next, the GBM removes the target signal from x1-4 to generate a residual noise-dominant signal, y1-4. Then, an FIR-based multiple-input canceller (MC) cancels the noise in OUTDAS to produce a clean beamformer output, OUTGABF. Finally, a feature extractor generates 40 log-Mel frequency energy features for speech recognition. A mode controller estimates target power and noise power floor from the output of the feature extractor. The mode controller controls greedy adaptive beamformer (GABF) coefficient adaptation, beamformer mode, and ADC mode.

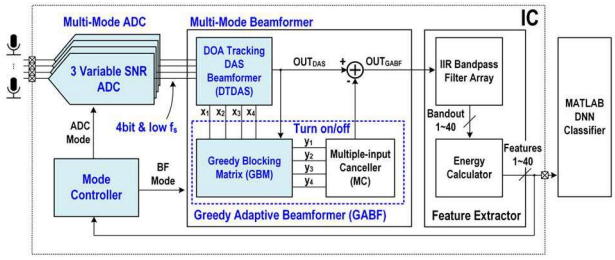


Figure 1. Multi- mode automatic speech frontend end with Greedy Adaptive Beamformer.

Keywords: ADC, bitstream, modulator, spectrogram, beamforming

INDUSTRY INTERACTIONS

NXP, Intel, Analog Devices

MAJOR PAPERS/PATENTS

[1] T. Kang, S. Lee, S. Song, M. R. Haghighat, M. P. Flynn, " A Multimode 157µW 4-Channel 80dBA-SNDR Speech-Recognition Frontend with Self-DOA Correction Adaptive Beamformer" ISSCC, Feb 2022.

TASK 2810.062, MULTI-CARRIER DAC-BASED TRANSMITTER ARCHITECTURES FOR 100+GB/S SERIAL LINKS

SAMUEL PALERMO, TEXAS A&M UNIVERSITY, SPALERMO@ECE.TAMU.EDU
SEBASTIAN HOYOS, TEXAS A&M UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

Clock jitter places fundamental performance limitations on common wireline transmitters, necessitating clock generation and distribution circuitry that achieve rms jitter of a few hundred femtoseconds. The DAC-based transmitter design techniques in this project aim to significantly improve jitter robustness and reduce system equalization complexity.

TECHNICAL APPROACH

A new multi-carrier DAC-based transmitter architecture is in development that is capable of providing jitter robustness for baseband and coherent multi-tone modulation applications. The transmitter utilizes novel techniques to improve the wireline polar transmitter speed and efficiency, including a high-speed injection-locked oscillator-based digital phase modulator and DAC-based FIR filtering in the segmented output driver. Efficient digital FIR filtering and linearization techniques, including a look-up table equalizer and an output stage predistortion DAC are also in development.

SUMMARY OF RESULTS

Figure 1 shows the proposed multi-carrier DAC-based transmitter configured to transmit 128Gb/s with baseband (BB) PAM-4, mid-frequency band (MB) QAM-16, and high-frequency band (HB) QAM-16 modulations. 160 parallel bits at 800MHz drive the DSP and pass-through FIR filters that are programmable from 1-8 taps. To achieve sufficient output stage linearity, the outputs of these filters are summed to generate a parallel 2b predistortion code. The output of the 800MHz DSP is 3 parallel streams of 16 symbols that are represented with a 6b code, which represents the level of the BB PAM-4 signal and the amplitude of the MB and HB QAM-16 signals, a 4b phase code for the MB and HB QAM-16 signals, and the 2b predistortion code. This architecture provides several benefits. First, each channel is operating

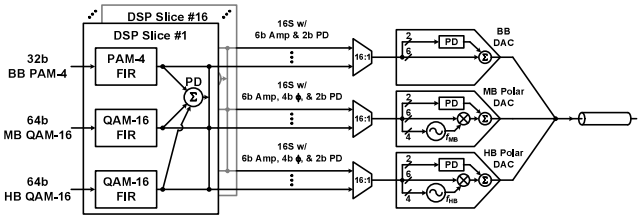


Figure 1. Multi-carrier DAC-based transmitter.

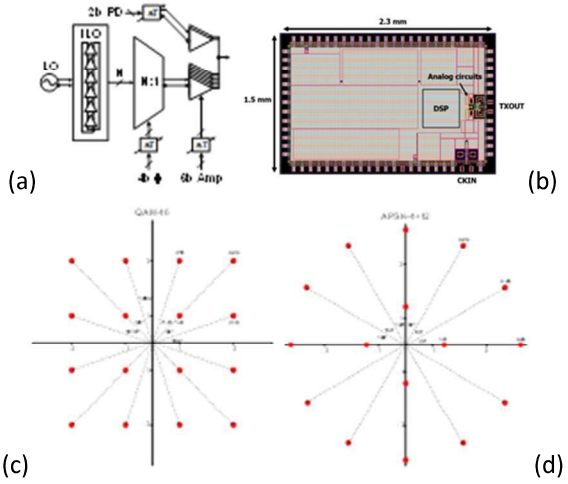


Figure 2. (a) Digital polar output DAC. (b) 64Gb/s TX chip layout in 22nm FinFET. 16-point constellations: (c) QAM-16 and (d) APSK-4+12.

at an effective 12.8GS/s sampling/serialization rate, which is significantly lower than the 64GS/s sampling rate required for conventional PAM4 modulation, allowing for close to a 6X improvement in simulated rms jitter tolerance. Second, the up-conversion performed in the MB and HB channels performs mixer-based self-equalization and provides channel loss compensation. Finally, the polar transmitter output stages provide the ability to support multiple 16-point constellations.

The proposed digital polar transmitter output stage used in both the MB and HB channels is shown in Figure 2. A given constellation point is realized by using the digital phase code to generate the desired phase from the high-speed phase modulator. This output phase passes to the output driver where it is scaled by the 6b amplitude control to realize the desired magnitude. The proposed polar architecture provides the flexibility to generate multiple 16-point constellations other than the conventional square QAM-16 constellation shown in Figure 2, which has three different output magnitudes. A 64Gb/s transmitter prototype has been taped-out in February 2022 in a 22nm FinFET process.

Keywords: Digital-to-analog converter, frequency-interleaving, jitter, transmitter, serial link

INDUSTRY INTERACTIONS

Intel, NXP, Texas Instruments

MAJOR PAPERS/PATENTS

TASK 2810.063, ANALOG AND DIGITAL ASSIST TECHNIQUES TO IMPROVE MIXED-SIGNAL PERFORMANCE

DENNIS SYLVESTER, UNIVERSITY OF MICHIGAN, DMCS@UMICH.EDU
DAVID BLAAUW, UNIVERSITY OF MICHIGAN

SIGNIFICANCE AND OBJECTIVES

This task will develop new digital assist techniques for mixed-signal circuits in a range of applications, to improve density, energy efficiency, process scalability/portability, and other key performance metrics.

TECHNICAL APPROACH

This project focuses on improving tradeoffs in state-of-the-art digitally-assisted analog circuits, identifying opportunities for new assist approaches, and broadly pushing forward the trend of digitizing conventionally analog heavy mixed-signal building blocks with an eye towards extreme scaling/density, ultra-low power design, or other metrics. We initially select three types of circuits to investigate: 1) digital LDOs; 2) low-power crystal oscillators for use in real-time clocks and other always-on timekeeping applications within IoT and ultra-low power sensing systems; 3) time amplifiers for use in the time-to-digital conversion.

SUMMARY OF RESULTS

A real time clock (RTC) is essential in battery-operated IoT sensors as they cannot afford to keep time through frequent communication with devices with accurate time references. Since an RTC is always on, its power consumption must be much lower than other components that can be duty cycled. Moreover, timing uncertainty yields longer radio on-time during synchronization, incurring high energy penalties, and hence, RTC accuracy must be high. To meet these needs, several ultra-low power (ULP) 32-kHz oscillators have been proposed. Previous sub-10nW oscillators use a pulsed-injection driver that directly replenishes the energy of the XO load capacitors. Unfortunately, frequency accuracy across temperatures exceeds 100ppm. Other works on temperature-compensated XOs and MEMS oscillators show frequency error < ±5ppm but consume > 300nW. The motivation of this work is to investigate the feasibility of a 32-kHz temperature-compensated XO with < 50nW power and < ±5ppm frequency error.

In particulare, an ultralow-power (ULP) temperature-compensated crystal oscillator (TCXO) with a pulsed-injection XO driver for IoT applications is being investigated. Temperature compensation is achieved by changing the load capacitance (C_L) between two values using a delta-sigma modulator. The complex modulation profile across temperature is approximated as piecewise linear elements that is selected by a coarse temperature sensor. This avoids the power and area of fine-grain look-up tables (LUTs) or a polynomial engine used in prior works. The proposed pulsed-injection XO driver that directly replenishes the energy of the C_L sustains the XO oscillation for the two different C_L states. Implemented in 40-nm CMOS, the proposed 32.768-kHz TCXO achieves an ±4.2 ppm accuracy from −20°C to 85°C with three-point trimming and 34-ppb Allan deviation floor while consuming 43 nW, which is ~8× better than recent state-of-the-art TCXOs.

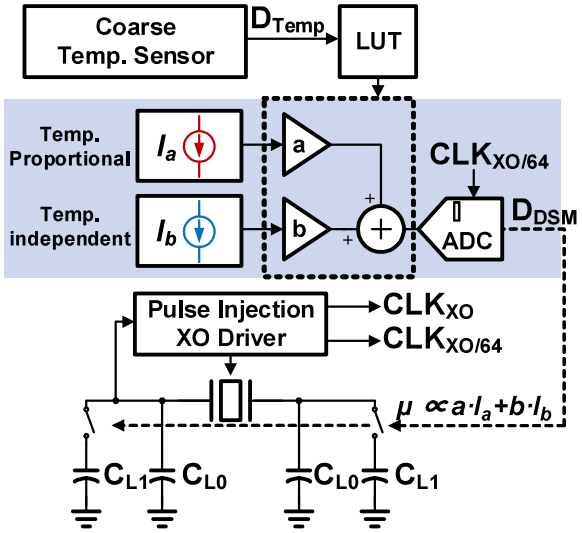
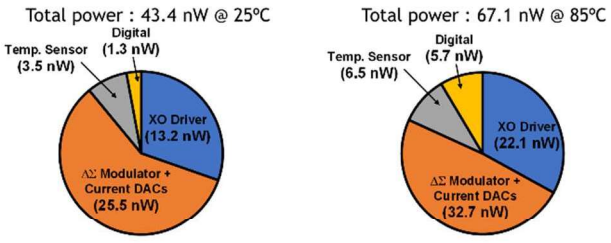


Figure 1. Proposed TCXO architecture.

Table 1. Power breakdown of TCXO at two temperatures.



Keywords: Crystal oscillators, frequency reference, temperature compensation

INDUSTRY INTERACTIONS

NXP

MAJOR PAPERS/PATENTS

TASK 2810.071, ACCURATE COMPACT TEMPERATURE SENSORS FOR THERMAL MANAGEMENT OF HIGH-PERFORMANCE COMPUTING PLATFORMS

RANDALL GEIGER, IOWA STATE UNIVERSITY, RLGEIGER@IASTATE.EDU
DEGANG CHEN, IOWA STATE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

The objective is to develop a strategy for designing compact densely distributed temperature sensors for real-time power-thermal management with the accuracy needed for reliably managing failure mechanisms inherent in silicon IC's. Significance is in providing sensor output as a key input into a robust power/thermal management controller.

TECHNICAL APPROACH

Compact temperature sensors that can be widely dispersed at critical locations throughout an integrated circuit will be designed. Tentatively these sensors will be a single small MOS transistor or pairs of MOS transistors where the temperature is embedded in the I-V characteristic of these devices. Located at a less-critical location where area requirements are relaxed will be a Temperature Management Controller (TMC) that extracts temperature data from an array of temperature sensors. The inter-relationship between the temperature of the TMC and at remote temperature sensor locations will be managed with an appropriate calibration algorithm.

SUMMARY OF RESULTS

The target performance of the compact temperature sensors is absolute accuracy of 100mK over the critical temperature window from 75°C to 95°C with accuracy rapidly reducing to 3°C below 50°C. This should enable management of the variation in the thermal-restricted mean time to failure (MTTF) of an integrated circuit to approximately 10% of a target MTTF value.

Two very compact temperature sensors are shown in Fig. 1. For the circuit on the left, the temperature T can ideally be determined from V_{OUTA} and V_{OUTB} independent of the current I_X. And for the circuit on the right, T can be

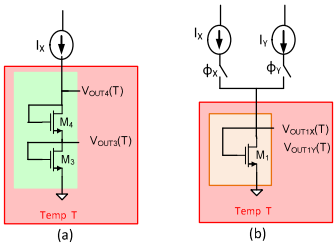


Figure 1. Compact Correlated Temperature Sensors.

ideally determined from V_{OUTX} and V_{OUTY} independent of the currents I_X and I_Y provided the current ratio I_X/I_Y is known. Thus, the temperature dependence of the biasing currents that are remotely generated in the TMC is of little concern.

A temperature sensor was designed in an ON 0.5-µm CMOS process using the circuit in Fig. 1(a) and a basic untrimmed Banba circuit for the current generator in the TMC. 100 Monte Carlo simulations were run over a wide range of temperatures for the current generator. Linearity correction of the temperature sensor was modeled by the equation $\hat{T} = a_0 + a_1 V_{0UT3} + a_2 V_{0UT4} + a_3 V_{0UT3} V_{0UT4}$. Ten of the Monte Carlo samples were used for a batch calibration to obtain $<a_0,a_1,a_2,a_3>$. Then each of the 100 samples was calibrated for slope and offset errors (m,b) with the measurement at two temperatures with the estimated temperature sensor temperature given by $\hat{\hat{T}} = m\hat{T} + b$. Monte Carlo simulation results of the maximum error in the 75°C to 95°C temperature window are shown in Fig. 2. The maximum error in the 100 samples was under 50mK.

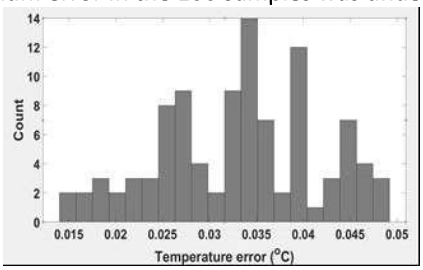


Figure 2. Monte Carlo Simulation of Temperature Error.

A partially-integrated sensor fabricated in the 0.5-µm CMOS process was tested using a discrete current generator. Four sensors were characterized. One was used for batch nonlinearity calibration and then a 2-point slope and offset calibration was used for all four sensors. The maximum measured error for the four circuits was 30mK over the 75°C to 95°C range and 350mK over the -10°C to 100°C range.

Keywords: temperature sensor, thermal mask, power/thermal management, reliability

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

Patent Disclosure: Dec 2021 "Compact Temperature Sensors for Power/Thermal Management."

TASK 2810.076, HIGH PRECISION POSITIONING TECHNIQUES BASED ON MULTIPLE TECHNOLOGIES AND FREQUENCY BANDS

NAOFAL AL-DHAHIR, UNIVERSITY OF TEXAS AT DALLAS, ALDHAHIR@UTDALLAS.EDU
MURAT TORLAK, UNIVERSITY OF TEXAS AT DALLAS

SIGNIFICANCE AND OBJECTIVES

High accuracy ranging techniques are essential for accurate localization in IoT applications. Bluetooth 5.1 is a popular candidate for ranging due to its low power consumption. However, multipath interference severely degrades ranging performance. We aim to achieve low complexity decimeter level ranging accuracy using Bluetooth systems in challenging real-world multipath scenarios.

TECHNICAL APPROACH

To achieve decimeter level ranging accuracy in challenging multipath environments, we proposed enhanced super-resolution Multiple Signal Classification (MUSIC) estimators. The enhancements include forward-backward (FB) averaging, virtual bandwidth extrapolation (BWE), and multiple antenna processing with both individual antenna processing (IAP) and summed antenna processing (SAP). To lower computational complexity without losing ranging accuracy, we proposed an enhanced sparsity aware range estimator utilizing a greedy orthogonal matching pursuit algorithm. We proposed MUSIC complexity reduction techniques such as the Lanczos algorithm and pseudospectrum computation using signal subspace. To demonstrate ranging performance, we collected real-world Bluetooth data in line of sight (LOS) and non-line of sight (NLOS) multipath for different ranges and multi-antenna configurations.

SUMMARY OF RESULTS

For our collected Bluetooth data in LOS and NLOS multipath environments for a range up to 7m, the enhanced MUSIC estimator with forward-backward averaging, bandwidth extrapolation, and multi-antenna processing showed a root mean square error (RMSE) performance of 61cm, while the conventional MUSIC estimator with a single antenna achieved RMSE of 1.52m. The sparse estimator achieved a similar RMSE performance of 64cm with much lower complexity (1.43 times faster) than enhanced MUSIC. For collected LOS and NLOS data, the enhanced MUSIC estimator's RMSE is 49cm (sparse estimator RMSE is 53cm) and 66cm (sparse RMSE is 67cm), respectively. The MUSIC estimator without any enhancements achieved RMSE of 1.25m for LOS and 1.74m for NLOS multipath scenarios, respectively. Figures 1-3 compare the empirical cumulative distribution function (ECDF) performance of all investigated range estimators.

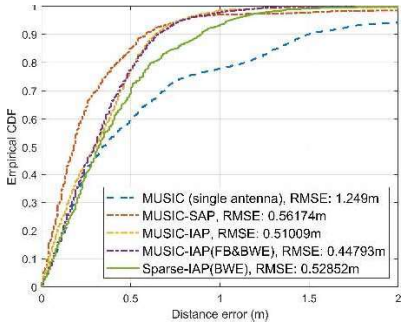


Figure 1. ECDF of range estimators in LOS multipath.

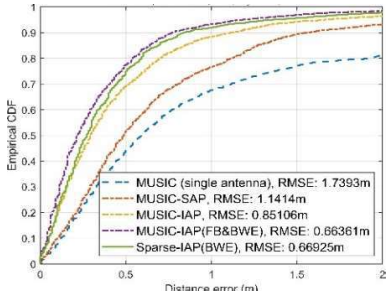


Figure 2. ECDF of range estimators in NLOS multipath.

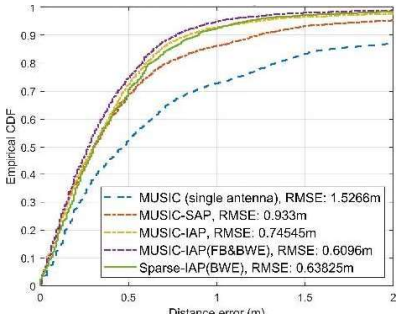


Figure 3. ECDF of range estimator in LOS and NLOS multipath.

Keywords: Bluetooth, Ranging, Multipath, Decimeter, IoT

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

[1] S.N. Shoudha, J. P. Van Marter, S. Helwa, A. G. Dabak, M. Torlak, and N. Al-Dhahir. "Reduced-Complexity Decimeter-Level Bluetooth Ranging in Multipath Environments," IEEE Access Journal, pp.38335-38350, 2022.

TASK 2810.081, DEVELOPMENT OF 70-95 GHZ TERABIT BEAMFORMER

HUEI WANG, NATIONAL TAIWAN UNIVERSITY, HUEIWANG@NTU.EDU.TW
TIAN-WEI HUANG AND KUN-YOU LIN, NATIONAL TAIWAN UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

We propose to develop a 70-95 GHz beamformer for extremely high-speed communication applications, possibly for B5G/6G systems. The proposed beamformer can provide a 25-GHz bandwidth (30% fractional bandwidth), which covers three point-to-point bands at E-band/W-band. Our brick-type array has three features: easy expansion, easy spacing, and easy assembly.

TECHNICAL APPROACH

We have successfully developed a Ka-band 32-element brick-type (vertical) phased-array beamformer shown in Figure 1. [1]. Compared with the traditional planar array, NTU vertical array can significantly reduce the length of RF signal routings, especially for 1024 elements or more. Another design challenge is the board-to-board spacing of a half-wavelength at the millimeter-wave carrier frequency (less than 2mm for the W-band). An InFO (integrated fan-in and fan-out) process will be utilized for the stack integration. We will also incorporate advanced CMOS or SOI technologies to enhance the RF performance and lower DC power consumption.

SUMMARY OF RESULTS

Figure 1(Right) is the block diagram of the proposed 70-95 GHz brick-type (vertical) phased-array beamformer, including an up/down converter, bi-directional PA-LNA, and bi-directional phase shifter.

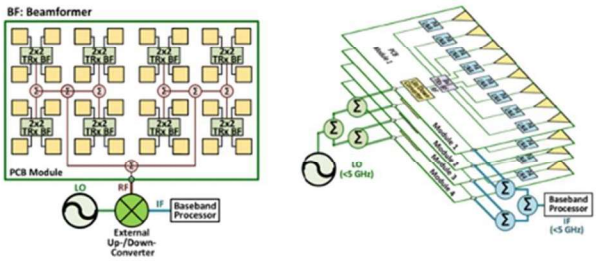


Figure 1. Traditional phased array with patch antennas, and brick-type phased array with end-fire antennas.

Based on our published bi-directional PA-LNA [2], we designed a W-band bi-directional PA-LNA in Figure 2, which demonstrates 19-dB Gain, 13.9dBm P_{sat}, and 6.4-dB NF at 85GHz. In [3], the one-directional E-band VGA measured 5.5-dB NF at 76–86 GHz with a minimum NF of 4.8 dB at 78 GHz. A 65% fractional bandwidth PA in [4] and a 30% fractional bandwidth LNA in [5] are developed for Ka-band/V-band.

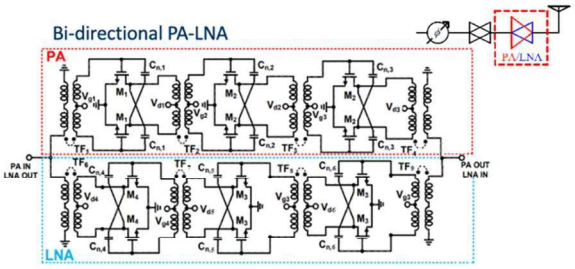


Figure 2. Schematic of W-band Bi-directional PA-LNA.

We have also designed W-band sub-harmonic up/down converter with 20-dB conversion gain and a bi-directional phase shifter with 5-bit control. In [6], a 70-dB high-isolation antenna array is developed at 24 GHz. In [7], a two-stage LC ladder is used to realize a 90% fractional bandwidth power divider (about 26GHz bandwidth) for a 5G millimeter-wave beamformer. These form a sound foundation for proposed research to realize the 70-95GHz beamformer.

Keywords: Beamformer, Phased Array, Bi-directional, W-band, CMOS

INDUSTRY INTERACTIONS

MediaTek

MAJOR PAPERS/PATENTS

[1] C. Chen et al., "38-GHz Phased Array Transmitter and Receiver Based on Scalable Phased Array Modules with Endfire Antenna Arrays for 5G MMW Data Links," *IEEE TMTT*, Jan. 2021.
[2] T. Chiu et al., "A Ka-Band Transformer-Based Switchless Bidirectional PA-LNA in 90-nm CMOS Process," 2021 *IEEE/MTT-S IMS*, Atlanta, GA, USA.
[3] Y. Wang et al., "An E-Band High-Performance Variable Gain Low Noise Amplifier for Wireless Communications in 90-nm CMOS Process," *IEEE MWCL*, Mar. 2022.
[4] T. Huang et al., "A 19.7–38.9-GHz Ultrabroadband PA With Phase Linearization for 5G in 28-nm CMOS Process," *IEEE MWCL*, Apr. 2022.
[5] M. Li et al., "A 50–67-GHz Ultralow-Power LNA Using Double-Transformer-Coupling Technique and Self-Resonant Matching in 90-nm CMOS," *MWCL*, Jan. 2022.
[6] L. Chang et al., "A Duplexing Hybrid Slot Antenna Design with High Isolation for Short-Range Radar Detection and Identification Applications at 24 GHz Band," *IEEE TAP*, Apr. 2022.
[7] Y. Chang et al., "Wideband Reconfigurable Power Divider/Combiner in 40-nm CMOS for 5G mmW Beamforming System," *IEEE TMTT*, Feb. 2022.

TASK 2810.082, ADAPTIVE DIGITAL CANCELLATION OF DYNAMIC ERROR FROM CLOCK SKEW, COMPONENT MISMATCHES, AND ISI IN HIGH-RESOLUTION RF DACS

IAN GALTON, UNIVERSITY OF CALIFORNIA, SAN DIEGO, GALTON@UCSD.EDU

SIGNIFICANCE AND OBJECTIVES

The project will develop digital calibration techniques that adaptively measure and cancel both static and dynamic errors from clock skew, component mismatches and ISI in current-steering RF DACs, and will experimentally validate via two 22-nm CMOS DAC ICs that enable DAC performance beyond the state-of-the-art.

TECHNICAL APPROACH

The project consists of three parts. Part 1 will develop a high-speed current-steering 3-GHz DAC IC with a target worst-case Nyquist-band SNDR of 72 dB enabled by a new subsampling mismatch-noise cancellation (MNC) technique. RZ signaling will be used to prevent ISI from limiting the DAC's performance. Part 2 will develop a subsampling inter-symbol interference cancellation (ISIC) technique, and Part 3 will develop a second-generation version of the Part 1 DAC IC that includes both the subsampling MNC and ISIC techniques. The ISIC technique eliminates the need for RZ signaling, which will enable a doubling of the sample rate to 6 GHz without degrading the SNDR of DAC.

SUMMARY OF RESULTS

Our first task is to design a first-generation 22-nm 3 GS/s CMOS RF DAC IC with a target Nyquist-band SNDR of 72 dB enabled by MNC and RZ signaling. We have made good progress on the system and circuit-level design and are on track to complete the task by the due date.

Keywords: DAC, current-steering, ISI, mismatch-cancellation, ISI-cancellation

INDUSTRY INTERACTIONS

NXP, MediaTek

MAJOR PAPERS/PATENTS

TASK 2810.083, AUTOMATED LAYOUT OF ANALOG ARRAYS IN ADVANCED TECHNOLOGY NODES

SACHIN S. SAPATNEKAR, UNIVERSITY OF MINNESOTA, SACHIN@UMN.EDU
RAMESH HARJANI, UNIVERSITY OF MINNESOTA

SIGNIFICANCE AND OBJECTIVES

This project automatically synthesizes high-quality layouts for analog circuit arrays. This involves (1) optimal design of array components considering parasitics, layout-dependent effects, process variations, temperature, electromigration, and voltage drops, and (2) optimal building block selection in circuits for performance/variability, exploring tradeoffs at the building block level.

TECHNICAL APPROACH

The design of array structures requires consideration of potentially conflicting factors: matching and resilience to systematic/random process variations, compact layout, low-parasitic routing, and thermal, electromigration, and IR drop constraints on wires that can degrade performance. These array structures are embedded into larger circuits, and the performance constraints on the array depend on the type of circuit and its usage in the larger system. The project will develop modeling techniques to capture these constraints and use them to build optimal arrays that balance the requirements of these performance requirements with matching constraints, using approaches such as common-centroid (CC) or interdigitated layout.

SUMMARY OF RESULTS

A common centroid (CC) layout is an integral method for ensuring matching in capacitive arrays in analog circuits. We will develop fast constructive procedures for CC placement and routing for binary-weighted capacitors in charge-sharing digital to analog converters (DACs). Traditional methods focus on the impact of mismatch on metrics such as the integral nonlinearity (INL) and differential nonlinearity (DNL) of the DAC and attempt to distribute capacitors in the array to achieve good levels of dispersion, increasing correlation between capacitance variations and therefore reducing mismatch. However, a traditional "chessboard" approach results in scattered structures that require a large number of "bends" in the wires used to connect them. In FinFET technologies with severe wire/via resistances, where wires are required to change layers to change directions, this results in a large number of vias. The high via resistances result in high RC delays, greatly degrading the 3-dB bandwidth for the capacitor.

We develop a set of approaches to place and route a CC capacitor array that optimizes for switching speed, measured by the 3-dB frequency. A balance between 3-dB frequency and DAC INL/DNL is investigated by trading off via counts with dispersion using (1) a spiral layout, shown in Fig. 1(a) and (2) block chessboard approaches, shown in Fig. 1(b) that use larger blocks (the size of the block is tunable) to reduce the number of vias particularly for the longest wires associated with the largest capacitors.

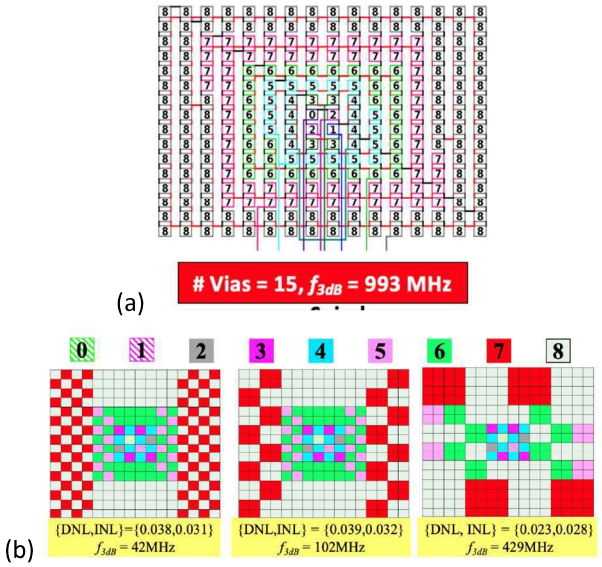


Figure 1. Common-centroid capacitor layouts for an 8-bit DAC using the proposed (a) spiral approach and (b) block chessboard layouts at various granularities.

CPU run times for both the spiral method and for each block chessboard are similar and are under 3s for 6-, 8-, and 10-bit DAC arrays. Because these methods are constructive, they are much faster than stochastic CC optimization, while providing excellent quality of results.

Keywords: Common-centroid, capacitor arrays, digital-to-analog converters, matching, 3dB frequency

INDUSTRY INTERACTIONS

Intel, NXP

MAJOR PAPERS/PATENTS

[1] N. Karmokar, A. K. Sharma, J. Poojary, M. Madhusudan, R. Harjani, and S. S. Sapatnekar, "Constructive Common-Centroid Placement and Routing for Binary-Weighted Capacitor Arrays," Proceedings of Design, Automation and Test in Europe, 2022.

TASK 2810.085, APPLICATIONS OF CIRCUIT TRANSIENT SENSITIVITY SIMULATION TO SEMICONDUCTOR CIRCUIT ANALYSIS AND DESIGN

RON ROHRER, SMU, RROHRER@SMU.EDU

SIGNIFICANCE AND OBJECTIVES

Apply adjoint sensitivity to reduce the number of circuit simulations entailed for analog integrated circuit fault analysis and yield estimation.

TECHNICAL APPROACH

Circuit simulation provides b (the number of branches) and n (the number of nodes) pieces of information. Adding adjoint sensitivity to the mix provides p (the number of parameters) times that. Extrapolation and interpolation among this enriched data set replaces the expensive blind groping of Monte Carlo simulation. The results of this research are expected to be on par with the task leader's prior contributions which touch virtually every integrated circuit designed and manufactured.

SUMMARY OF RESULTS

Time domain transient adjoint sensitivity provides the first order partial derivatives of all responses concerning all parameters, both process, and design.

The simulation flow has been optimized to support relatively large time step sizes and hypothetical parameter changes without requiring excessive additional computation. Comprehensive error analysis defines the difference between tedious incremental sensitivity (gold standard) and adjoint sensitivity estimation. Time domain adjoint sensitivity is potentially applicable to any type of integrated circuit including VLSI.

Reasonably accurate estimations for Fault Analysis and Yield Analysis are explored in terms of a small number of time domain adjoint sensitivity simulations.

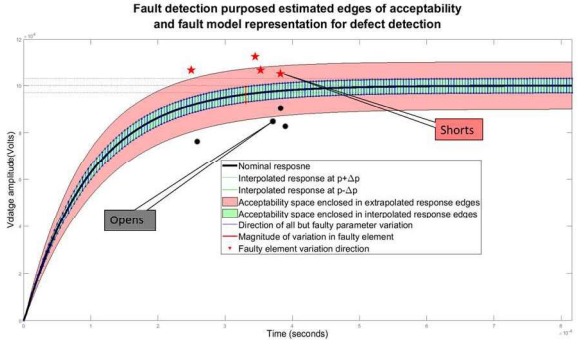


Figure. 1 Acceptability edge and fault detection for an Opamp circuit.

Traditionally, fault analysis has required many repeated simulation runs with different model changes for all fault locations (shorts/opens) to obtain all of the potential faulty responses. Instead of conducting design of experiments for analog faults, we have shown that faults can be considered as parameter variations that change the functionality of the circuit. In this research, faults in analog circuits are represented as those resistance models that cause the violation of circuit specifications. Fig. 1 indicates the fault detection scheme for an operational amplifier circuit.

Another application is non-Monte-Carlo Yield estimation [1]. If the circuit performance can be approximated with a multivariate gaussian distribution, sensitivities of all the random variables provide an estimation of the performance distribution. This approach provides a yield estimation that is very close to that of tedious Monte-Carlo: Fig. 2. Only normal distributions have been employed so far. More general parameter distributions are to be addressed in future work.

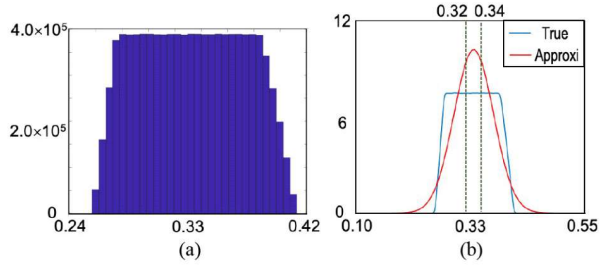


Figure 2. The performance distribution obtained by Monte-Carlo (a) and that obtained by sensitivity-estimation (b).

Future work will focus on exploring the application of fault analysis in terms of industry standard circuit examples. Circuit hierarchy and time domain noise analysis will also be addressed.

Keywords: adjoint sensitivity, yield estimation, fault analysis

INDUSTRY INTERACTIONS

Texas Instruments, NXP

MAJOR PAPERS/PATENTS

[1] Zhengqi Gao and Ron Rohrer, "Efficient Non-Monte Carlo Yield Estimation," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 41, Issue 5, Pages 1222-1235, May 2022.

APPENDIX I PUBLICATIONS OF TXACE RESEARCHERS

Conference Publications

[1] Zamparette, R. and Makinwa, K. (2021). A ±2A/15A Current Sensor with 1.4 µA Supply Current and ±0.35%/0.6% Gain Error From −40 to 85°C using an Analog Temperature-Compensation Scheme. *2021 Symposium on VLSI Circuits, Kyoto, Japan*, pp. 1-2, IEEE.

[2] Chakraborty, A., Sanyal, S., Dasgupta, P., Hazra, A., Morrison, S., Surendran, S. and Balasubramanian, L. (2022). Tracking Coverage Artefacts for Periodic Signals using Sequence-based Abstractions. *2022 35th International Conference on VLSI Design and 2022 21st International Conference on Embedded Systems (VLSID), Bangalore, India*, pp. 132-137, IEEE.

[3] Xie, Z., Xu, X., Walker, M., Knebel, J., Palaniswamy, K., Hebert, N., Hu, J., Yang, H., Chen, Y. and Das, S. (2021). APOLLO: An Automated Power Modeling Framework for Runtime Power Introspection in High-Volume Commercial Microprocessors. *International Symposium on Microarchitecture, Athens, Greece*, pp. 1-14, IEEE/ACM.

[4] Chang, C., Pan, J., Zhang, T., Xie, Z., Hu, J., Qi, W., Lin, CW., Liang, R., Mitra, J., Fallon, E. and Chen, Y. (2021). Automatic Routability Predictor Development Using Neural Architecture Search. *International Conference On Computer Aided Design (ICCAD), Munich, Germany*, pp. 1-9, IEEE/ACM.

[5] Liang, R., Jung, J., Xiang, H., Reddy, L., Lvov, A., Hu, J. and Nam, G.-J. (2021). FlowTuner: A Multi-Stage EDA Flow Tuner Exploiting Parameter Knowledge Transfer. *International Conference On Computer Aided Design (ICCAD), Munich, Germany*, pp. 1-9, IEEE/ACM.

[6] Farayola, P.O., Bruce, I., Chaganti, S.K., Sheikh, A., Ravi, S. and D. Chen. (2022). The Least-Squares Approach to Systematic Error Identification and Calibration in Semiconductor Multisite Testing. *2022 IEEE 40th VLSI Test Symposium (VTS), San Diego, CA*, pp. 1-7, IEEE.

[7] Zhou, P., Smith, J., Deremo, L., Heinrich-Barna, S. and Friedman, J. (2021). Synchronous Unsupervised STDP Learning with Stochastic STT-MRAM Switching. *IEEE International Conference on Rebooting Computing*, IEEE.

[8] Zhou, P., Edwards, A., Mancoff, F., Houssameddine, D., Aggarwal, S. and Friedman, J. (2021). Experimental Demonstration of Neuromorphic Network with STT MTJ Synapses. *IEEE International Electron Devices Meeting - MRAM Poster Session, San Francisco, CA*, IEEE.

[9] Zhou, P., Smith, J., Deremo, L., Heinrich-Barna, S. and Friedman, J. (2022). Synchronous Unsupervised STDP Learning with Stochastic STT-MRAM Switching. *Joint IEEE International Magnetics Conference & Conference on Magnetism and Magnetic Materials, New Orleans, LA*, IEEE.

[10] Zhou, P., Smith, J., Deremo, L., Heinrich-Barna, S. and Friedman, J. (2022). Synchronous Unsupervised STDP Learning with Stochastic STT-MRAM Switching. *APS March Meeting, Chicago, IL*, IEEE.

[11] Zhou, P., Edwards, A., Mancoff, F., Houssameddine, D., Aggarwal, S. and Friedman, J. (2022). Experimental Demonstration of Neuromorphic Network with STT MTJ Synapses. *Government Microcircuit Applications & Critical Technology Conference, Miami, Florida*, US DoD.

[12] Hu, H., He, C. and Li, P. (2021). Semi-supervised Wafer Map Pattern Recognition using Domain-Specific Data Augmentation and Contrastive Learning. *2021 IEEE International Test Conference (ITC), Anaheim, CA*, pp. 113-122, IEEE.

[13] Shim, M.S., Hu, H., and Li, P. (2021). Reversible Gating Architecture for Rare Failure Detection of Analog and Mixed-Signal Circuits. *2021 58th ACM/IEEE Design Automation Conference (DAC), San Francisco, CA*, pp. 901-906, IEEE/ACM.

[14] Wang, D., Lin, C., Chen, G., Knag, P., Krishnamurthy, R. and Seok, M. (2022). DIMC: 2219TOPS/W 2569F2/b Digital In-Memory Computing Macro in 28nm Based on Approximate Arithmetic Hardware. *2022 IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, CA*, pp. 266-268.

[15] Lee, C.Y. and Moon, U.-K. (2022). A 0.0375mm^2 203.5µW 108.8dB DR DT Single-Loop DSM Audio ADC Using a Single-Ended Ring-Amplifier-Based Integrator in 180nm CMOS. *2022 IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, CA*, pp. 412-414, IEEE.

[16] Yu, H., Park, G. and Kim, C. (2021). Extreme Temperature Characterization of Amplifier Response up to 300 Degrees Celsius Using Integrated Heaters and On-chip Samplers. *ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC), Grenoble, France*, pp. 411-414, IEEE.

[17] McLaughlin, P., Datta, K. and Stauth, J.T. (2022). A Monolithic 3:1 Resonant Dickson Converter with Variable Regulation and Magnetic-Based Zero-Current Detection and Autotuning. *2022 IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, CA*, pp. 304-306, IEEE.

[18] Karthik Somayaji, N.S., Hu, H. and Li, P. (2021). Prioritized Reinforcement Learning for Analog Circuit Optimization With Design Knowledge. *2021 58th ACM/IEEE Design Automation Conference (DAC), San Francisco, CA*, pp. 1231-1236, IEEE/ACM.

[19] Avci, M.E., Ozev, S. and Chethan Kumar, Y.B. (2022). Fast RF Mismatch Calibration Using Built-in Detectors. *2022 IEEE 40th VLSI Test Symposium (VTS), San Diego, CA*, pp. 1-7, IEEE.

[20] Strong, M., Bhatheja, K., Yang, R. and Chen, D. (2021). A Simple Monitor for Tracking NBTI in Integrated Systems. *2021 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), Lansing, MI*, pp. 1112-1115, IEEE.

[21] Ganji, M., Saikiran, M. and Chen, D. (2022). All Digital Low-Overhead SAR ADC Built-In Self-Test for Fault Detection and Diagnosis. *2022 IEEE 40th VLSI Test Symposium (VTS), San Diego, CA*, pp. 1-7, IEEE.

[22] Kteyan, A., Sukharev, V. and Kim, C.H. (2022). Novel methodology for temperature-aware electromigration assessment in on-chip power grid: simulations and experimental validation (Invited). *2022 IEEE International Reliability Physics Symposium (IRPS), Dallas, TX*, pp. 8C.1-1-8C.1-10, IEEE.

[23] Pande, N., Zhou, C., Lin, M.H., Fung, R., Wong, R., Wen, S. and Kim, C.H. (2021). Electromigration-Induced Bit-Error-Rate Degradation of Interconnect Signal Paths Characterized from a 16nm Test Chip. *2021 Symposium on VLSI Technology, Kyoto, Japan*, pp. 1-2, IEEE.

[24] Blanche, P. and Ketchum, R. S. (2021). Texas Instruments Phase Light Modulator for Holography. *OSA Imaging and Applied Optics Congress 2021*, OSA Technical Digest (Optica Publishing Group, 2021).

[25] Blanche, P. and Draper, C. (2021). Curved Holographic Waveguide Combiner for HUD and AR Display. *OSA Imaging and Applied Optics Congress 2021*, OSA Technical Digest (Optica Publishing Group, 2021).

[26] Blanche, P. and Draper, C. (2021). Curved waveguide combiner for HUD/AR. *SPIE Optical Engineering + Applications, San Diego, CA*, SPIE.

[27] Luo, C., Guan, J., Deng, X. and Takashima, Y. (2021). Analysis of diffraction efficiency of TI-PLM and its potential in beam steering. *SPIE Optical Engineering + Applications, San Diego, CA*, SPIE.

[28] Ma, D.B., Yan, D. and Du, L. (2021). Active Conducted EMI Suppression in GaN Switching Power Circuits. *2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), Monterey, CA*, pp. 1-6, IEEE.

[29] Jogalekar, A., Medina, O., Blanchard, A., Henderson, R., Iyer, M., Tang, T., Murugan, R. and Ali, H. (2021). Slot Bow-Tie Antenna Integration in an Enhanced Flip-Chip QFN Package for WR8 and WR5 Band Applications. *2021 IEEE MTT-S International Microwave and RF Conference (IMARC), Kanpur, India*, pp. 1-4, IEEE.

[30] Neethirajan, D., Niranjan, V.A., Willis, R., Webster, D., Nahar, A. and Makris, Y. (2022). Machine Learning-Based Overkill Reduction through Inter-Test Correlation. *2022 IEEE 40th VLSI Test Symposium (VTS), San Diego, CA*, pp. 1-7, IEEE.

[31] Kang, T., Lee, S., Song, S., Haghighat, M.R. and Flynn, M.P. (2022). A Multimode 157µW 4-Channel 80dBA-SNDR Speech-Recognition Frontend With Self-DOA Correction Adaptive Beamformer. *2022 IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, CA*, pp. 500-502, IEEE.

[32] Wang, Z., Kim, S., Bowmann, K. and Seok, M. (2022). Review, Survey, and Benchmark of Recent Digital LDO Voltage Regulators. *2022 IEEE Custom Integrated Circuits Conference (CICC), Newport Beach, CA*, pp. 1-8, IEEE.

[33] Nguyen, D.T., Macias, E. and Hanson, A.J. (2022). Active EMI Filter with Switch-Mode Amplifier for High Efficiency. *2022 IEEE Applied Power Electronics Conference and Exposition (APEC), Houston, TX*, pp. 443-450, IEEE.

[34] Islam, T., Kim, J., Tipple, D., Nelson, M., Jin, R., Jarrar, A., and Kim, C.H. (2022). A Calibration-Free Synthesizable Odometer Featuring Automatic Frequency Dead Zone Escape and Start-up Glitch Removal. *2022 IEEE International Reliability Physics Symposium (IRPS), Dallas, TX*, pp. P2-1-P2-6, IEEE.

[35] Qiao, B., Kayyil, A.V., Walling, J.S. and Allstot, D.J. (2021). I/Q-Sharing Switched-Capacitor Power Amplifier with Baseband Harmonic-Rejection and Wilkinson Combiner. *2021 IEEE International Symposium on Circuits and Systems (ISCAS), Daegu, Korea*, pp. 1-4, IEEE.

[36] Kayyil, A.V., Qiao, B. and Allstot, D.J. (2021). Linearity Improvement Techniques for CMOS Switched-Capacitor Power Amplifiers. *2021 IEEE International Symposium on Circuits and Systems (ISCAS), Daegu, Korea*, pp. 1-5, IEEE.

[37] Liu, J. and Allstot, D.J. (2021). Compressed Sensing Σ-Δ Modulators and Recovery Algorithm for Multi-Channel Bio-Signal Acquisition. *2021 IEEE International Symposium on Circuits and Systems (ISCAS), Daegu, Korea*, pp. 1-4, IEEE.

[38] Liu, J. and Allstot, D.J. (2021). A Switched-Capacitor Closed-Loop Integration Sampling Front-End for Peripheral Nerve Recording. *2021 IEEE Biomedical Circuits and Systems Conference (BioCAS), Berlin, Germany*, pp. 1-4, IEEE.

[39] Allstot, D.J., Moon, U.-K. and Temes, G.C. (2022). Switched-Capacitor Circuits (Invited). *2022 IEEE Custom Integrated Circuits Conference (CICC), Newport Beach, CA*, pp. 1-8, IEEE.

[40] Xu, C., Yang, F. and Akin, B. (2021). Design of AC Power Cycling Test Setup for GaN HEMTs' Reliability Assessments. *2021 IEEE 13th International Symposium on Diagnostics for Electrical Machines, Power Electronics and Drives (SDEMPED), Dallas, TX*, pp. 471-476, IEEE.

[41] Chen, C., Liu, J. and Lee, H. (2022). A 2.5-5MHz 87% Peak Efficiency 48V-to-1V Integrated Hybrid DC-DC Converter Adopting Ladder SC Network with Capacitor-Assisted Dual-Inductor Filtering. *2022 IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, CA*, pp. 234-236, IEEE.

[42] Yu, W.-H., Giordano, M., Doshi, R., Zhang, M., Mak, P.-I., Martins, R.P. and Murmann, B. (2021). A 4-bit Mixed-Signal MAC Array with Swing Enhancement and Local Kernel Memory. *2021 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), Lansing, MI*, pp. 326-329, IEEE.

[43] Karmokar, N., Sharma, A.K., Poojary, J., Madhusudan, M., Harjani, R. and Sapatnekar, S.S. (2022). Constructive Common-Centroid Placement and Routing for Binary-Weighted Capacitor Arrays. *2022 Design, Automation & Test in Europe Conference & Exhibition (DATE), Antwerp, Belgium*, pp. 166-171, IEEE.

[44] Karthik Somayaji, N.S., Hu, H. and Li, P. (2021). Non-global Policy Reinforcement Learning for Analog Circuit Optimization. *SRC Techcon, Austin, TX*, SRC.

[45] Takashima, Y. (2021). Preface: Enablers for DX (Digital Transformation), can AR display and automotive lidar be next optical data storage industry? *New Orleans Academy of Ophthalmology 71st Annual Symposium, New Orleans, LA*, NOAO.

Journal Publications

[1] Baral, A. B. and Torlak, M. (2021). Joint Doppler Frequency and Direction of Arrival Estimation for TDM MIMO Automotive Radars. *IEEE Journal of Selected Topics in Signal Processing*, **vol.** 15, **no.** 4, **pp.** 980-995.

[2] Smith, J. W. and Torlak, M. (2022). Efficient 3-D Near-Field MIMO-SAR Imaging for Irregular Scanning Geometries. *IEEE Access*, **vol.** 10, **pp.** 10283-10294.

[3] Weingartner, T.A., Kuo, C.-H., Thomas, A., Thompson, S.E. and Law, M.E. (2021). Negative Impact of Compressive Biaxial Stress on High Precision Bipolar Devices. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **vol.** 11, **no.** 8, **pp.** 1310-1312.

[4] Huang, C.H., Chen, Y., Sun, X., Mandal, A., Pamula, V.R., Kurd, N. and Sathe, V.S. (2022). Improving SIMO-Regulated Digital SoC Energy Efficiencies Through Adaptive Clocking and Concurrent Domain Control. *IEEE Journal of Solid-State Circuits*, **vol.** 57, **no.** 1, **pp.** 90-102.

[5] Jie, L., Tang, X., Liu, J., Shen, L., Li, S., Sun, N. and Flynn, M.P. (2021). An Overview of Noise-Shaping SAR ADC: From Fundamentals to the Frontier. *IEEE Open Journal of the Solid-State Circuits Society*, **vol.** 1, **pp.** 149-161.

[6] Jie, L., Chen, H.-W., Zheng, B. and Flynn, M.P. (2021). A Hybrid-Loop Structure and Interleaved Noise-Shaped Quantizer for a Robust 100-MHz BW and 69-dB DR DSM. *IEEE Journal of Solid-State Circuits*, **vol.** 56, **no.** 12, **pp.** 3681-3693.

[7] Najm, F. N. (2021). Equivalent circuits for electromigration. *Microelectronics Reliability*, **vol.** 123, **pp.** 114200.

[8] Zhi, Q., Rincón-Mora, G.A. and Gu, P. (2022). Autonomous and Programmable 12-W 10-kHz Single-Cell Li-Ion Battery Tester. *IEEE Transactions on Instrumentation and Measurement*, **vol.** 71, **pp.** 1-8.

[9] Gupta, A., Ayyanar, R. and Chakraborty, S. (2021). Novel Electric Vehicle Traction Architecture With 48 V Battery and Multi-Input, High Conversion Ratio Converter for High and Variable DC-Link Voltage. *IEEE Open Journal of Vehicular Technology*, **vol.** 2, **pp.** 448-470.

[10] Gupta, A., Ayyanar, R. and Chakraborty, S. (2021). Soft-Switching Mechanism for a High-Gain, Interleaved Hybrid Boost Converter. *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, **vol.** 2, **no.** 4, **pp.** 420-430.

[11] Blanche, P. and Draper, C. (2022). Holographic curved waveguide combiner for HUD/AR with 1-D pupil expansion. *Optics Express*, **vol.** 30, **pp.** 2503-2516.

[12] Vankayalapati, B.T., Pu, S., Yang, F., Farhadi, M., Gurusamy, V. and Akin, B. (2022). Investigation and On-Board Detection of Gate-Open Failure in SiC MOSFETs. *IEEE Transactions on Power Electronics*, **vol.** 37, **no.** 4, **pp.** 4658-4671.

[13] Pu, S., Yang, F., Vankalayapati, B. and Akin, B. (2022). Aging Mechanisms and Accelerated Lifetime Tests for SiC MOSFETs: An Overview. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, **vol.** 10, **no.** 1, **pp.** 1232-1254.

[14] McGarry, M., Iyer, M. and Lee, M. (2022). Broadband Millimeter-Wave Dielectric Properties of Liquid Crystal Polymer Materials. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **vol.** 12, **no.** 1, **pp.** 192-194.

[15] Kang, T., Lee, S., Haghighat, M., Abramson, D. and Flynn, M.P. (2021). A 650-µW 4-Channel 83-dBA-SNDR Speech Recognition Front-End With Adaptive Beamforming and Feature Extraction. *IEEE Solid-State Circuits Letters*, **vol.** 4, **pp.** 158-161.

[16] Park, S., Seol, J.-H., Xu, L., Cho, S., Sylvester, D. and Blaauw, D. (2022). A 43 nW, 32 kHz, ±4.2 ppm Piecewise Linear Temperature-Compensated Crystal Oscillator With ΔΣ-Modulated Load Capacitance. *IEEE Journal of Solid-State Circuits*, **vol.** 57, **no.** 4, **pp.** 1175-1186.

[17] Shoudha, S., Van Marter, J., Helwa, S., Dabak, A., Torlak, M. and Al-Dhahir, N. (2022). Reduced-Complexity Decimeter-Level Bluetooth Ranging in Multipath Environments. *IEEE Access*, **vol.** 10, **pp.** 38335-38350.

Contact TxACE

To become a TxACE partner, please contact:

Kenneth K. O, Director
972-883-5556

To discuss our core facilities in Dallas and how to obtain access to them and to receive future TxACE requests for proposals, please contact:

Lucien Finley
lucien.finley@utdallas.edu
972-883-5553

TxACE is based at The University of Texas at Dallas. We are located in the Engineering and Computer Science North building, ECSN 3.302.

Texas Analog Center of Excellence
The University of Texas at Dallas, EC37
800 West Campbell Road
Richardson, Texas 75080

centers.utdallas.edu/txace

Semiconductor Research Corporation

TxACE TEXAS ANALOG CENTER OF EXCELLENCE