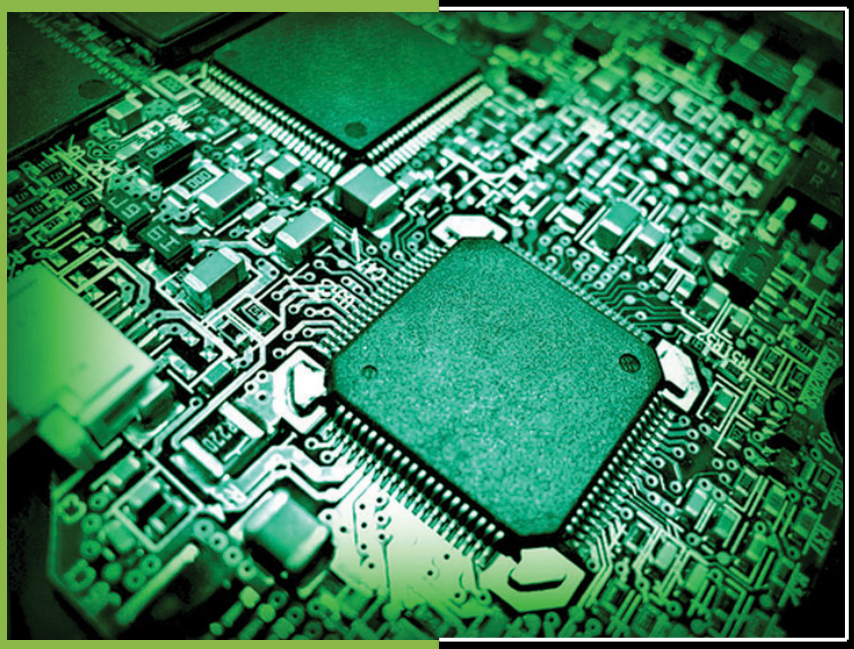
TEXAS ANALOG CENTER OF EXCELLENCE

ANNUAL REPORT 2009 – 2010



SRC

TxACE
TEXAS ANALOG
CENTER OF EXCELLENCE

OUR MISSION

The Texas Analog Center of Excellence seeks to create fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, health care, and public safety and security.

OUR RESEARCH THRUSTS

- Safety & Security
- Health Care
- Energy Efficiency
- Fundamental Analog Circuits Research

TxACE 2009-2010 ANNUAL REPORT

Analog and mixed signal integrated circuits engineering is both a major opportunity and a major challenge. It is an opportunity because of the increasing importance of analog integrated circuits in electronic systems and the emergence of new applications. It is a challenge because of the inherent difficulty of the art. The creation of advanced wireless technology and sophisticated sensing and imaging devices depends on the availability of engineering talent for analog research and development. The Texas Analog Center of Excellence (TxACE) was established to help overcome the challenges and translate these opportunities into economic benefits for the participants and society. Support for TxACE has been provided through a collaboration of the State of Texas, Texas Instruments, the Semiconductor Research Corporation, the University of Texas System and the University of Texas at Dallas.

As the second year of TxACE operation closed, the center has much to be proud of. An ambitious research program is in place and beginning to yield results. The research tasks are being organized into four research thrust areas: Healthcare, Safety and Security, Energy Efficiency and Fundamental Analog. The scope of investigation extends from circuits operating at DC through terahertz, data converters that sample at tens of mega-samples/sec to tens of giga-samples/sec, AC-to-DC and DC-to-DC converters working at microwatts to watts, energy harvesting circuits, protein and DNA sensors and many more. Significant improvement on existing mixed signal systems and exciting new applications based on this circuit research are anticipated.

Graduate students who have been exposed to hands-on innovative research are forming the leading edge of a flow of analog talent into industry. Close collaboration with and responsiveness to industry needs provides focus to the educational experience. TxACE researchers and engineers are ready to perform. Located at The University of Texas at Dallas, TxACE has rapidly grown from a concept to a dynamic working reality. On the basis of the number of principal investigators and funding, it is now the largest analog center in the world. **Figure 1** shows the location of academic institutions including three international universities. A

significant portion of the program involves Texas Universities and Texas industry in order to enhance the local economy.

The new TxACE analog laboratory just coming online provides a working environment that promotes collaboration among researchers. The laboratory includes capabilities for device and circuit characterization at high frequencies well beyond that used in present day commercial electronics, opening up the door for novel circuit research for new applications and markets.

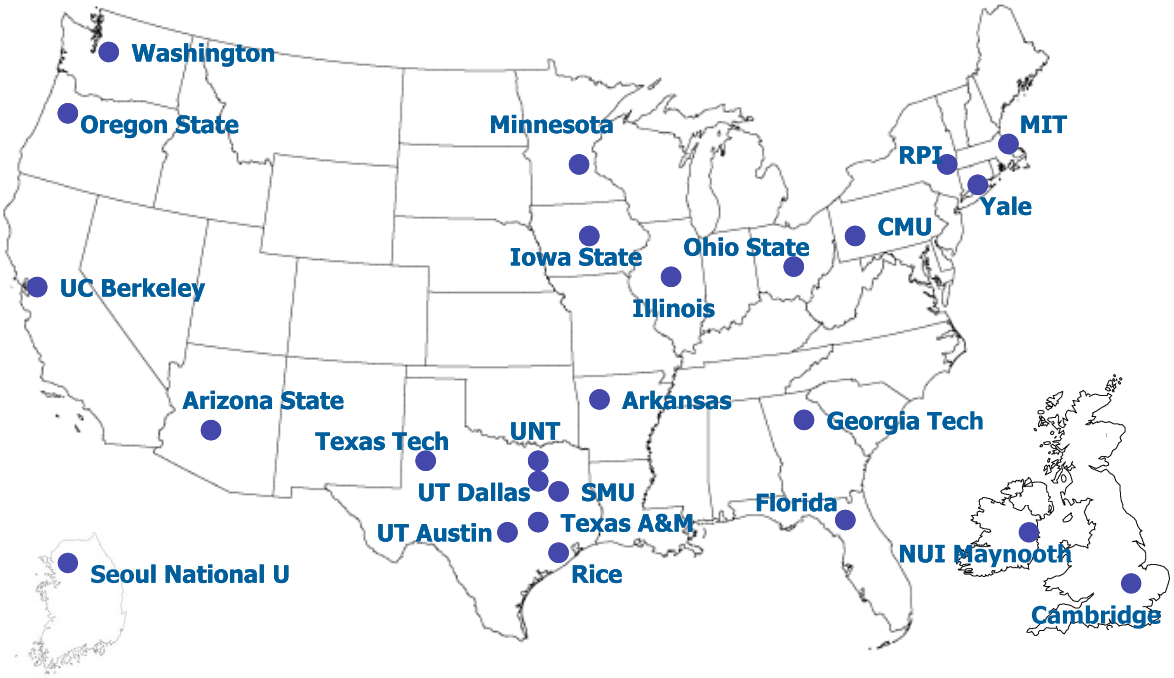


Figure 1: TxACE Member institutions

DIRECTOR'S MESSAGE

This second year of TxACE operation has matured and focused all facets of the center. Our objective is to lead analog research and education that can create new economic opportunities by improving analog and mixed signal technology, education, research and manufacturing. We are pleased to see our efforts beginning to show results. A flow of graduating analog engineering talent has been established and is entering the workplace. Individual research efforts herald the entry of innovative products into the marketplace. The process of technology transfer is underway.

At the close of the 2009-2010 period construction of TxACE laboratories and design facilities was completed, and the equipment is being installed. TxACE high frequency circuit characterization tools will help lower a critical barrier for advancing millimeter and sub-millimeter integrated circuit technology. These capabilities are a global asset, and plans are being formulated to provide access to the laboratories to TxACE members and others in a collaborative framework.

The research and organizational structure of the center has been defined. Additionally, critical leadership positions have been filled. We are grateful to those who have stepped up to serve.

TxACE is now an international center that is the largest for analog research in the world on the basis of funding and the number of principal investigators (68 principal investigators from 26 academic institutions). A majority of the leading analog researchers in the United States are participating in the center. Seven schools (Rice, SMU, Texas A&M, Texas Tech, The University of North Texas, UT Austin, UT Dallas) are from Texas. Three (Seoul National University, Cambridge University, National University of Ireland, Maynooth) are from outside the United States.

Presently the center supports 73 graduate students (49 from Texas universities and 24 from outside of Texas). During the past year nine PhD and three MS degrees were awarded to TxACE students.

Despite being in existence for only two years, as documented in this report, TxACE can report significant achievements. This of course could not have happened without the support of TxACE's principal investigators and students as well as the support of the State of Texas, UT Dallas, Texas Instruments Inc. and Semiconductor Research Corp. I am proud of the TxACE team, and I am looking forward to a new year with greater research accomplishments and impact.

Kenneth K. O, Director TxACE
Texas Instruments Distinguished Chair
The University of Texas at Dallas

MESSAGE FROM UT DALLAS

Analog technology has existed in the shadow of digital technology for far too long, but the Texas Analog Center of Excellence is succeeding in changing that.

It is doing so through both research and education.

The research component speaks for itself: More than $10 million in funding for directed research tasks performed by 68 principal investigators at 26 academic institutions. But the education component is equally important.

The majority of electrical engineering students have long specialized in digital electronics, but as the use of digital has grown, the need for analog of course has grown. But analog is growing at several times the rate of digital, and as a result analog engineers are in great demand.

Many engineers find analog more rewarding to work with than digital, and TxACE is helping to convey the excitement of analog technology to students. The numbers alone are impressive: TxACE projects have so far involved nearly 100 students in four countries.

But what those students mean for the future is more important still. They are the ones who will become analog engineers in industry, developing technology that will improve our lives in myriad ways. And they will pass along their enthusiasm for analog engineering to the next generation of students and engineers.

TxACE is to be congratulated for an outstanding start, and I look forward to seeing what great technology, students and engineers it produces in the years ahead.

Mark W. Spong
Dean, Erik Jonsson School of Engineering and Computer Science
Lars Magnus Ericsson Chair in Electrical Engineering
Excellence in Education Chair
The University of Texas at Dallas

MESSAGE FROM SEMICONDUCTOR RESEARCH CORPORATION

The Texas Analog Center of Excellence has made strong progress since its creation just two years ago.

Under the direction of Kenneth K. O, TxACE has quickly become an influential resource for analog research and development, coordinating and supporting work that directly contributes to addressing the world's needs in key areas, including health care, energy, and safety and security.

But that's just the beginning.

- With the creation of a core laboratory facility, TxACE's influence will grow, and it will complement its distributed research approach with centralized resources available to researchers from various institutions using a collaborative framework.
- With TxACE's demonstrated success at bringing a methodical approach to analog research, we fully expect funding support for TxACE to expand in years ahead.
- As research continues, I am confident we will soon begin seeing real-world applications of TxACE-generated technology all around us.

Two years ago, Texas Gov. Rick Perry hailed TxACE as the sort of investment that is essential to strengthen growing industries and bolster the economy. TxACE has exceeded expectations, and I'm confident there is more to come from the growing number of researchers whose combined talents TxACE has succeeded in harnessing.

Larry W. Sumney, President and CEO
Semiconductor Research Corporation

BACKGROUND & VISION

For the past 20 years semiconductor electronics was dominated by digital logic. This led to the digital revolution that we are all familiar with, affecting things from computational power to high-definition digital television. For the next 20 years, analog and mixed signal semiconductor technology is expected to drive progress as electronics continues to bridge the gap between the analog real world and the digital information infrastructure. In just the period from 2005 to 2007, the analog semiconductor market grew from $30 billion to $50 billion! High performance analog technology is a unique segment of the semiconductor electronics business. It requires special skills in both design and process that reside in the United States.

To lead this change, in particular to lead analog technology education, research, commercialization, manufacturing and job creation, the Texas Analog Center of Excellence was formally announced by Texas Gov. Rick Perry in October 2008 as a $16 million collaboration of the Semiconductor Research Corp., the State of Texas through its Texas Emerging Technology Fund, Texas Instruments, Inc., The University of Texas System and UT Dallas (see **Figure 2**). The center seeks to accomplish these objectives by creating fundamental analog, mixed signal and RF design innovations in integrated circuits and systems that improve energy efficiency, health care, and public safety and security.

CENTER ORGANIZATION

The Texas Analog Center of Excellence is guided by agreements established with the center sponsors.The advisory boards identify the research needs and select research tasks in consultation with the center leadership. **Figure 2** diagrams the relationship of TxACE to the members of the sponsoring collaboration.

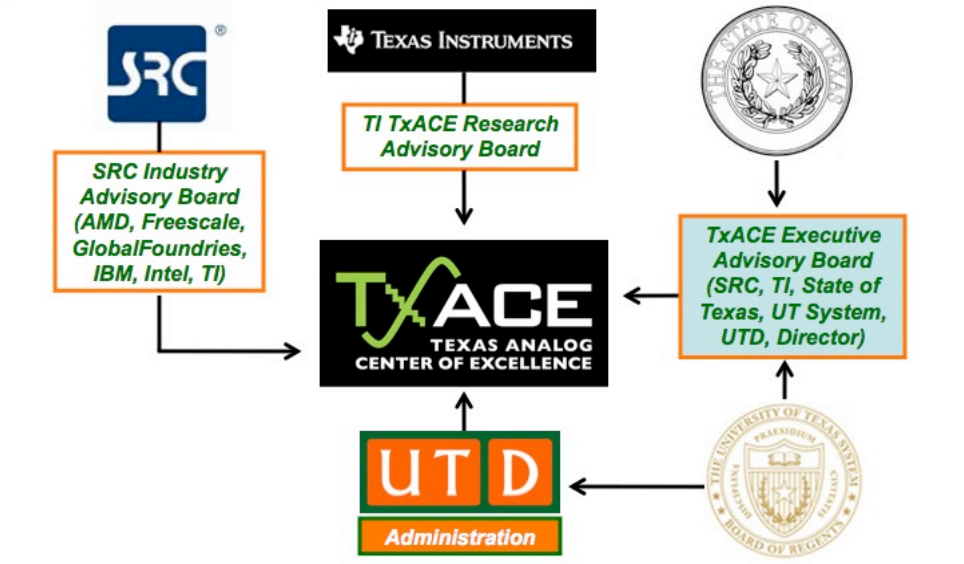


Figure 2: TxACE organization relative to the sponsoring collaboration

The internal organization of the center is structured to flexibly perform the research mission while not detracting from the educational missions of the University. **Figure 3** identifies the elements of the organization. The TxACE Director is Kenneth K. O and the Associate Director is Eric Vogel. The center research is arranged into four thrusts that comply with the mission of the Center: Safety and Security, Health Care, Energy Efficiency and Fundamental Analog Circuits. The last thrust consists of vital research that cuts across more than one of the first three research thrusts. The thrust leaders are Brian Floyd of North Carolina State University for the safety and security thrust, Ramesh Harjani of the University of Minnesota for the health care thrust, Dongsheng Ma of UT Dallas for the energy efficiency thrust and David Allstot of the University of Washington for the fundamental analog research thrust. The thrust leaders and Yun Chiu of UT Dallas form the executive committee. The committee along with the director

and associate director form the leadership team which works to improve the research productivity of center by increasing collaboration, better leveraging the diverse capabilities of principle investigators of the center, and lowering research barriers. The leadership team also identifies new research opportunities for consideration by the advisory boards.

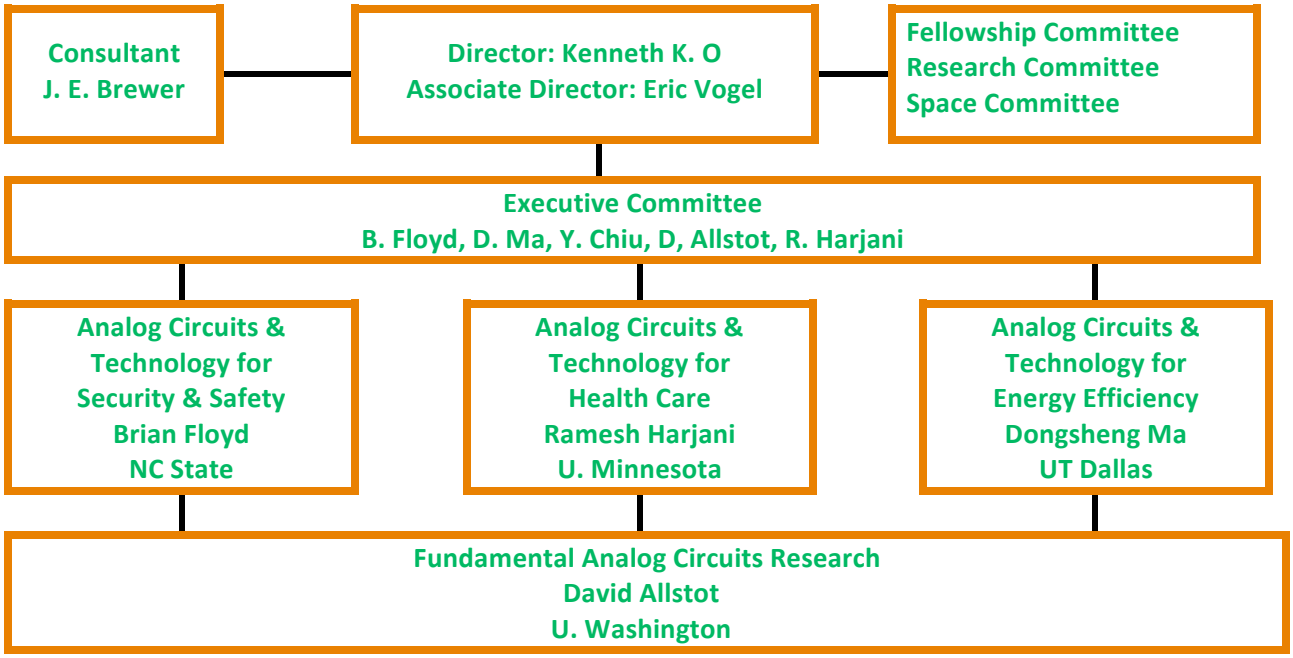


Figure 3: TxACE organization for management of research

PUBLIC SAFETY AND SECURITY

(Thrust leader: Brian Floyd, NC State)

TxACE has awarded nearly $1.5 million to researchers to develop analog technology that enhances public safety and security. The projects are intended to: 1) Enable a new generation of devices that can scan for harmful substances by researching 200-300-GHz silicon ICs for use in spectrometers and 2) Significantly reduce the cost of in-vehicle radar technology to improve automotive safety by researching circuit techniques that can improve manufacturing and lower test and packaging costs.

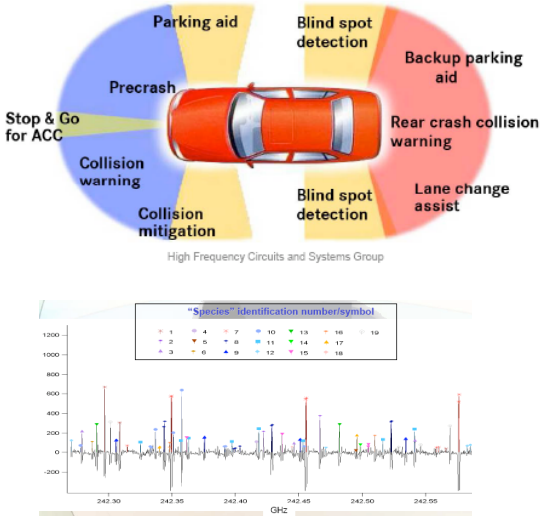


Figure 4: Millimeter wave radar to improve automobile safety and rotational spectrum around 300 GHz.

HEALTH CARE

(Thrust leader: Ramesh Harjani, University of Minnesota)

Analog and RF integrated circuit technology is the essential interface enabling the power, speed and miniaturization of modern digital microelectronics to be brought to bear on an array of medical issues, including medical imaging, patient monitoring, laboratory analyses, bio-sensing and new therapeutic devices. TxACE is working to identify and support analog circuit research challenges that have the potential to enable important health-related applications.

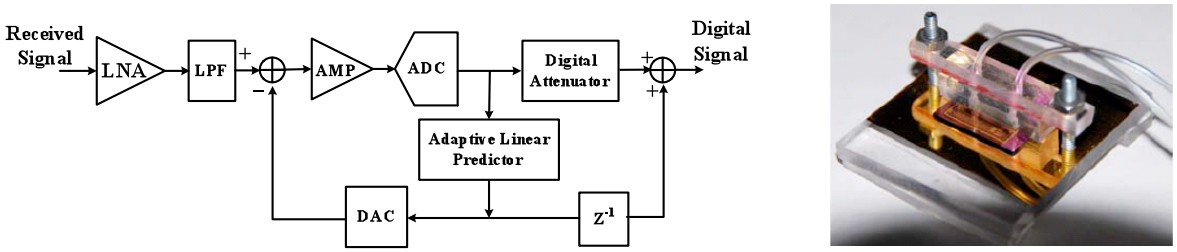
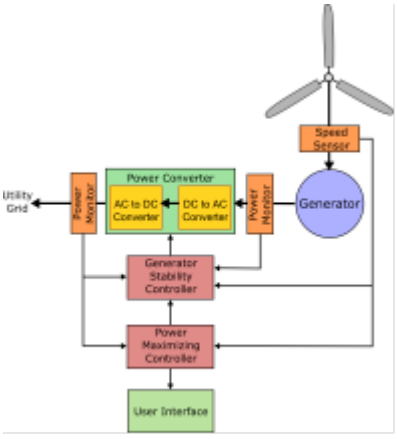


Figure 5: Receiver for ultrasound imaging based on adaptive data prediction with improved dynamic range (left). Micro-fluidic system for detecting protein markers using nanowire transistors (right).

ENERGY EFFICIENCY

(Thrust leader: Dongsheng Ma, UT Dallas)

TxACE is committed to alleviate the global energy problem by improving the energy efficiency of electronic systems as well as by developing analog technologies that can make energy generation more efficient. The center is also working to energize and power long-lasting in-situ microscale devices such as wireless microsensors, biomedical implants and portable microelectronics.



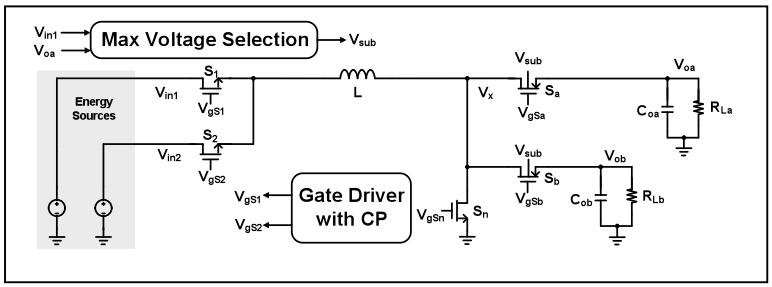


Figure 6: Electric generation system using wind (left). Single inductor multiple input and multiple output DC-DC converter (above).

FUNDAMENTAL ANALOG CIRCUITS RESEARCH

(Thrust leader: David Allstot, University of Washington)

Research in this thrust focuses on cross-cutting areas in analog circuits which impact all of the TxACE application areas (Energy Efficiency, Health Care, Public Safety and Security).

Fundamental analog circuits' research is crucial for the design of analog-to-digital converters and communication links, the development of CAD tools, and testing of high-speed circuits.

TXACE ANALOG RESEARCH FACILITY

UT Dallas has prepared a ~7,500 ft^2 area on the 3rd floor of the Engineering and Computer Science North building to form an enhanced centralized group of laboratories dedicated to analog engineering research and research training.

Figure 7 is a 3D sketch of the facility, which was completed in August 2010, and is currently being brought online. The facility includes RF and THz, Integrated System Design, Embedded Signal Processing, and Analog & Mixed Signal laboratories as well as a CAD/Design laboratory structured to promote collaborative research**.** **Figure 7** presents the facility floor plan showing the dimensions of each laboratory.

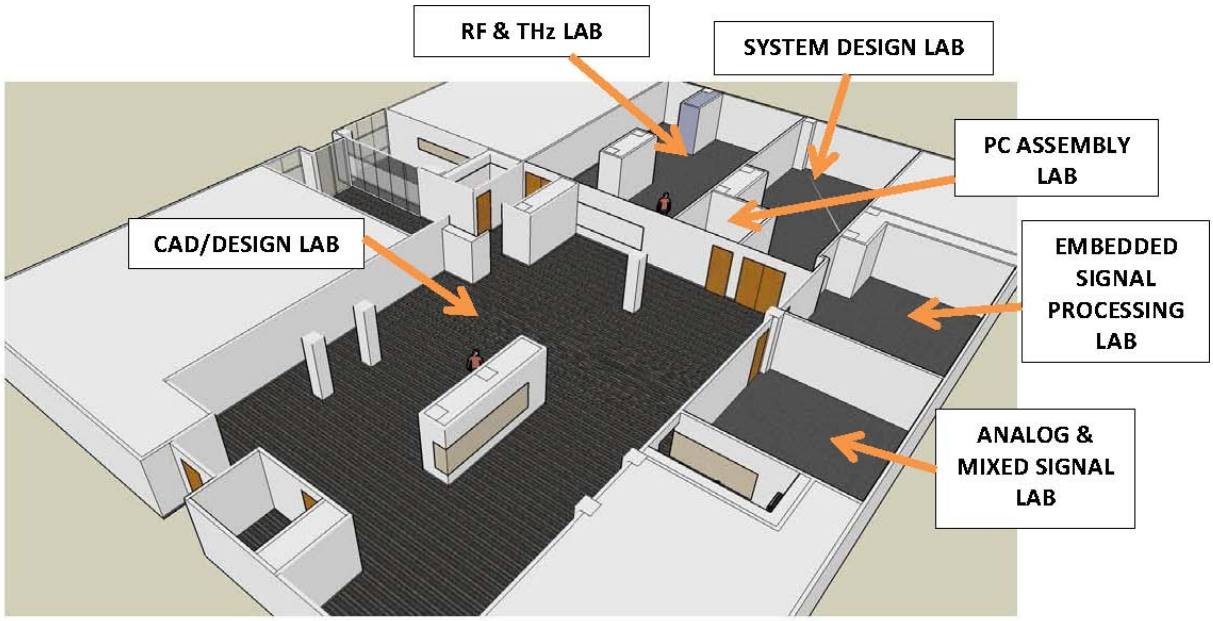


Figure 7: TxACE research facility

The close proximity of researchers in an open layout enables natural interaction and compels sharing of knowledge and instrumentation among the students and faculty. The TxACE analog research facility is one of the best equipped university-based electronics laboratories in the state, and the RF and THz laboratory will be one of the best in the nation.

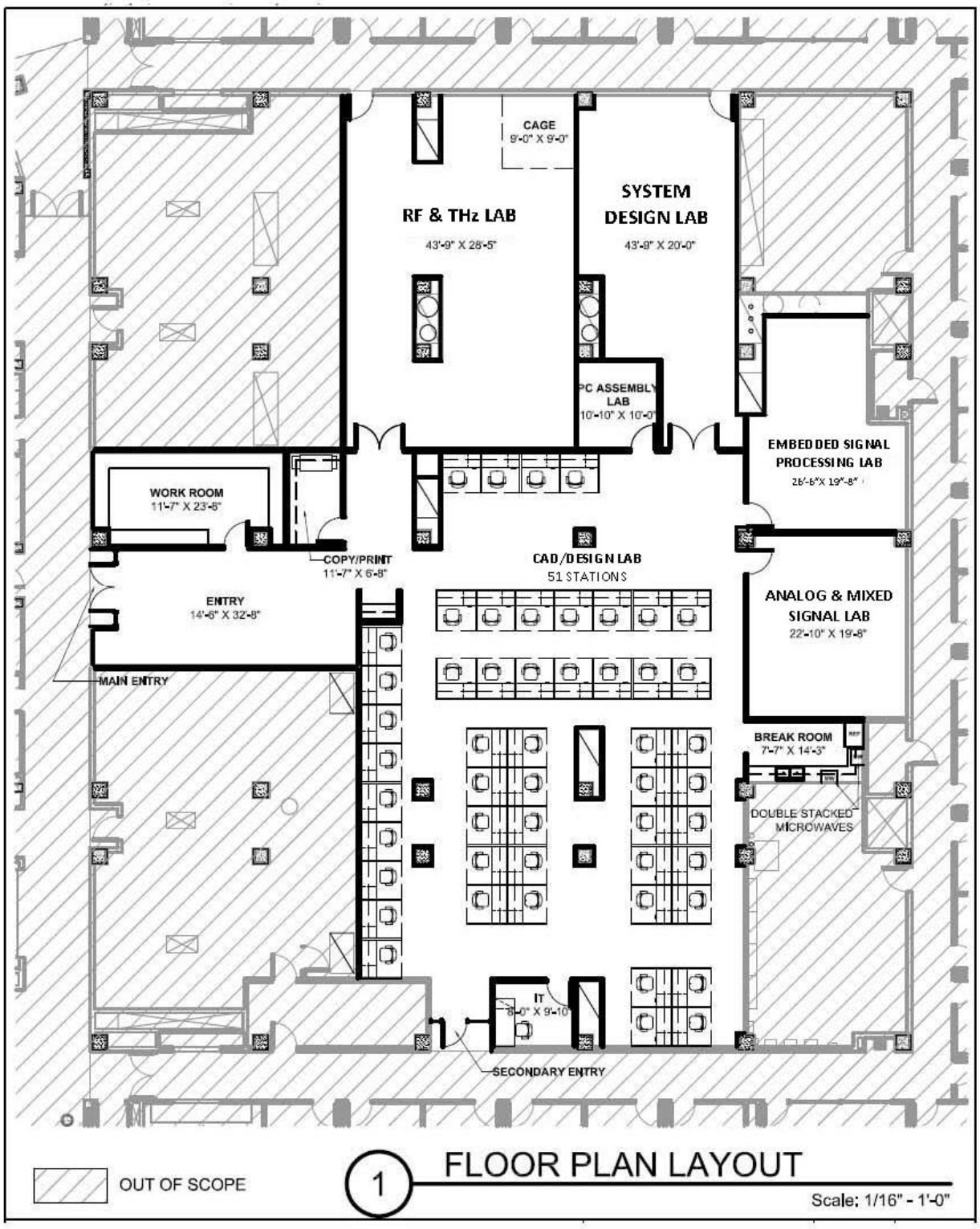


Figure 8: TxACE research facility floor plan

RESEARCH PROJECTS AND INVESTIGATORS

During 2009-2010 TxACE grew to be the largest analog technology center in the world on the basis of funding and the number of principal investigators. **Table 1** lists the names of the 68 principal investigators from 26 academic institutions with directed research tasks funded by TxACE. Seven schools (Rice, SMU, Texas A&M, Texas Tech, University of North Texas, UT Austin, UT Dallas) are in Texas. Nineteen are outside Texas. Three (Seoul National University, Cambridge University, National University of Ireland, Maynooth) are outside the U.S. Of the 68 investigators, 35 are from Texas. The center supports 73 graduate students and during the past year nine PhD and three MS degrees were awarded to TxACE students.

Table 1: Principal and co-principal investigators of TxACE during reporting period

Investigator	Institution	Investigator	Institution	Investigator	Institution
David Allstot	U Washington	Mona Hella	Rennselaer	Un-Ku Moon	Oregon State
Bertan Bakkaloglu	Arizona State	Rashaunda Henderson	UT Dallas	Tamal Mukherjee	Carnegie Mellon
Poras Balsara	UT Dallas	Sebastian Hoyos	Texas A&M	Won Namgoong	UT Dallas
Bhaskar Banerjee	UT Dallas	Roozbeh Jafari	UT Dallas	Ken O	UT Dallas
Leonidas Bleris	UT Dallas	Aydin Ilker Karsilayan	Texas A&M	Vojin Oklobdzija	UT Dallas
Andrew Blanchard	UT Dallas	Sayfe Kiaei	Arizona State	Sule Ozev	Arizona State
Shawn Blanton	Carnegie Mellon	Jaeha Kim	Seoul Nat'l U	Sam Palermo	Texas A&M
Joe Brewer	U Florida	Elias Kougianos	U North Texas	Larry Pileggi	Carnegie Mellon
Choong-Yul Cha	UT Dallas	Farinaz Koushanfar	Rice	John Ringwood	NUI Maynooth
Abhijit Chatterjee	Georgia Tech	Hoi Lee	UT Dallas	Elyse Rosenbaum	U Illinois, Urbana-Champaign
Degang Chen	Iowa State	Changzhi Li	Texas Tech	Jaijeet Roychowdhury	UC Berkeley
Frank De Lucia	Ohio State	Donald Yu-Chun Lie	Texas Tech	Rob Rutenbar	Carnegie Mellon
William Eisenstadt	U Florida	Peng Li	Texas A&M	Mohammad Saquib	UT Dallas
Kamran Entesari	Texas A&M	Xin Li	Carnegie Mellon	Carl Sechen	UT Dallas
Brian L. Evans	UT Austin	Jin Liu	UT Dallas	Naresh Shanbhag	U Illinois, Urbana-Champaign
Terri Fiez	Oregon State	Dongsheng Ma	U Arizona	Michael Shur	Rennselaer
Randy Geiger	Iowa State	H.A. Mantooth	U Arkansas	Jose Silva-Martinez	Texas A&M
Ranjit Gharpurey	UT Austin	Yiorgos Makris	Yale	V. Stojanovic	MIT
Ping Gui	SMU	Jose Silva-Martinez	Texas A&M	Murat Torlak	UT Dallas
Pavan Kumar Hanumolu	Oregon State	Kartikeya Mayaram	Oregon State	Eric Vogel	UT Dallas
Ramesh Harjani	U Minnesota	Richard McMahon	Cambridge	Xi-Cheng Zhang	Rennselaer
Arjang Hassibi	UT Austin	Kathleen Melde	U Arizona	Dian Zhou	UT Dallas
Robert Heath	UT Austin	Saraju Mohanty	U North Texas		

SUMMARIES OF RESEARCH PROJECTS, ACCOMPLISHMENTS AND PUBLICATIONS

The 66 research projects funded through TxACE during 2009-2010 are listed in **Table 2** below by Semiconductor Research Corp. task identification number. Despite being in existence for only two years, TxACE is making significant research progress. **Table 3** lists the major research accomplishments for the center from Sept. 1, 2009, to Aug. 31, 2010, while **Table 4** summarizes the number of publications and inventions resulting from TxACE research during the period. Following the tabulations, brief summaries of each project are provided.

Table 2: Funded research projects at TxACE by SRC task identification number

#	Task	Task Title	PI	Institution
1	1836.002	Adaptive High Dynamic Range Equalizer and Automatic Skew Compensation for High-Speed Data Communications	Liu, Jin	UT Dallas
2	1836.003	Temperature Compensated, High Common Mode Range, Cu-Trace Based Current Shunt Monitors	Bakkaloglu, Bertan	Arizona State
3	1836.004	Robust Design of Low Power Small Area Data Converters in Low Voltage Digital Processes	Geiger, Randall	Iowa State
4	1836.005	Design and Implementation of a Large-N Low-Jitter Digitally-Controlled Oscillator (DCO)-based Frequency Multiplier	Gui, Ping	SMU
5	1836.006	Multi-Core and Distributed Parallel Simulation for Design and Verification of Custom Digital and Analog ICs	Li, Peng	Texas A&M
6	1836.007	Novel Instruction Set Architecture Designs for Programmable Multiple Standard Radio Processors	Oklobdzija, Vojin	UT Dallas
7	1836.008	Digital Assisted Millimeter-Wave CMOS Circuits	O, Kenneth	UT Dallas
8	1836.011	Power Minimization and Yield Optimization in Digital IC's	Sechen, Carl	UT Dallas
9	1836.012	Structural Fault Modeling, Testing, and Defect Level Estimation for Analog/RF Circuits	Ozev, Sule	Arizona State
10	1836.013	Wideband Receiver Architectures in Digital Deep Submicron CMOS	Hoyos, Sebastian	Texas A&M
11	1836.014	Digital Phase-Locking Circuits for Clock Generation and Data Recovery in High-Speed Frequency Multiplier Communication Links	Hanumolu, Pavan Kumar	Oregon State
12	1836.015	Software-Defined Digital Multiple-Output DC-DC Converter for Dynamic Thermal Management	Ma, Brian	UT Dallas
13	1836.016	Bridging the Synthesis Gap from Circuits to Systems for Scaled Mixed-Signal Silicon	Mukherjee, Tamal	Carnegie Mellon
14	1836.017	Performance-Oriented DVS-Compatible Single-Inductor Multiple-Output Power Converters	Ma, Brian	UT Dallas
15	1836.018	Transistor Sizing and Voltage Scaling for Minimal Energy at Fixed Performance	Oklobdzija, Vojin	UT Dallas
16	1836.019	Digitally-Enhanced Energy-Efficient High-Speed I/O Links	Shanbhag, Naresh	U Illinois Urbana-Champaign
17	1836.020	Low-Complexity High-Performance Analog-to-Digital Converters in Submicron CMOS	Moon, Un-Ku	Oregon State
18	1836.021	CAD Algorithms and Tools for Fast and Accurate PLL Design in the Presence of Variability	Roychowdhury, Jaijeet	UC Berkeley
19	1836.022	High-Speed MIMO Signaling Techniques for Single-Ended Parallel I/O	Harjani, Ramesh	U Minnesota

Table 2: continued

#	Task	Task Title	PI	Institution
20	1836.023	Fast Algorithms for SPICE-Level Simulation of Large Structured Circuits	Roychowdhury, Jaijeet	UC Berkeley
21	1836.024	MIMO at the Cell Edge for High Bandwidth Communication in Interference Limited Cellular Systems	Heath, Robert	UT Austin
22	1836.025	Ultra Low Power ADCs for Wireless Communications	Fiez, Terri	Oregon State
23	1836.026	Automatic RF Impedance Correction Circuits for SoC RF/Mixed-Signal ATE Test	Eisenstadt, William R	U Florida
24	1836.027	Automatic RF Impedance Correction Circuits for SoC RF/Mixed-Signal ATE Test	Melde, Kathleen	U Arizona
25	1836.028	Tools and Algorithms for Behavioral Model Generation of Analog/Mixed-Signal Circuits	Mantooth, Homer Alan	U Arkansas
26	1836.029	Statistical Analysis of Parametric Measurements and its Applications in Analog/RF Test	Makris, Yiorgos	Yale
27	1836.030	Fast PVT-Tolerant Physical Design of RF IC Components	Mohanty, Saraju	UNT
28	1836.031	Variation Tolerant Analog Design based on Generalized Kharitonov/Lyapunov Theory	Zhou, Dian	UT Dallas
29	1836.032	Millimeter Wave Phase-Locked Loop Design with Enhanced Tolerance to Process and Temperature Variation	Gharpurey, Ranjit	UT Austin
30	1836.033	MIMO Radar for Pixel Reduction in mm-Wave Imaging	Saquib, Mohammad	UT Dallas
31	1836.034	77-81 GHz CMOS Transceiver with Built-In Self Test and Healing	Banerjee, Bhaskar	UT Dallas
32	1836.035	Development of CMOS Sub-Terahertz Receivers for Spectrometers	Banerjee, Bhaskar	UT Dallas
33	1836.036	Signal Generation for 200-300 GHz Spectrometer	O, Kenneth	UT Dallas
34	1836.037	Development of Antenna and Chip Interface Systems for Millimeter Wave and Sub-Millimeter Wave Applications	Henderson, Rashaunda	UT Dallas
35	1836.038	A Hybrid 14-bit Analog-to-Digital Converter for Broadband Applications	Silva-Martinez, Jose	Texas A&M
36	1836.039	UxIDs: Unclonable Mixed-Signal Integrated Circuits Identification	Koushanfar, Farinaz	Rice
37	1836.040	Energy-Efficient CMOS 10GS/s 6-bit ADC with Embedded Equalization	Palermo, Sam	Texas A&M
38	1836.041	A High-Efficiency Single-Inductor Multiple-Input Multiple-Output Integrated DC/DC Converter for Energy-Harvesting Applications	Lee, Hoi	UT Dallas
39	1836.042	Adaptive Data Prediction Based Receiver for Power-Efficient High-Resolution Ultrasound Imaging Systems	Ma, Brian	UT Dallas
40	1836.043	High-Voltage Amplifier Technology	Gui, Ping	SMU
41	1836.044	Statistical Models and Methods for Design and Test of Non-Digital Components	Li, Xin	Carnegie Mellon
42	1836.045	Frequency Channelized ADC for Wide Bandwidth Systems	Namgoong, Won	UT Dallas
43	1836.046	Reconfigurable Antenna Interface for Low-Power Wireless Sensor Nodes	Allstot, David	U Washington
44	1836.047	Integration of Millimeter Wave Antennas Using System in Package Techniques	Henderson, Rashaunda	UT Dallas
45	1836.048	Millimeter and Submillimeter Gas Sensors: System Architectures for CMOS Devices	De Lucia, Frank	Ohio State
46	1836.049	On-Chip Current-Sensing Techniques for Switching DC/DC Converters	Lee, Hoi	UT Dallas

Table 2: continued

#	Task	Task Title	PI	Institution
47	1836.050	Feed-Forward Multi-Phase Clock Generation	Liu, Jin	UT Dallas
48	1836.052	An Ultra-low Power Signal Processing with Smart Analog-enabled Pre-Conditioning Stage for Inertial Sensing Applications	Jafari, R.& Namgoong, W.	UT Dallas
49	1836.053	High-Efficiency Highly-Integrated LED Driver Systems for Solid-State Lighting Applications	Lee, Hoi & Zhou, Dian	UT Dallas
50	1836.054	Silicon Based Beamforming Arrays for Millimeter Wave Systems	Torlak, Murat	UT Dallas
51	1836.055	SPICE Models and Analog Circuits for Nanoscale Silicon Chemical- and Biological-Sensors	Vogel, Eric	UT Dallas
52	1836.057	High Accuracy All-CMOS Temperature Sensor with Low-Voltage Low-Power Subthreshold MOSFETs Front-End and Performance-Enhancement Techniques	Li, Changzhi	Texas Tech
53	1836.058	Hierarchical Model Checking for practical Analog/Mixed-Signal Design Verification	Li, Peng & Liu, Jin	Texas A&M
54	1836.060	Design Techniques for Scalable, Sub-1mW/Gbps Serial I/O Transceivers	Palermo, Sam	Texas A&M
55	1836.061	Analog Computing in Human Cells	Bleris, Leonidas	UT Dallas
56	1836.062	System-Level Models and Design of Power Delivery networks with On-Chip Voltage Regulators	Li, Peng	Texas A&M
57	1836.063	Power line Communications for Enabling Smart Grid Applications	Evans, Brian L.	UT Austin
58	1836.064	Ultra-Low-Power Analog Front-End IC Design for Implantable Cardioverter Defibrillator	Lie, Donald Yu-Chun	Texas Tech
59	1836.065	Energy Efficient Comparator Elements for A/D Converters and High-Speed I/Os	Oklobdzija, Vojin	UT Dallas
60	1836.066	A Fully-Integrated CMOS Platform for Microwave-Based Label-Free DNA Sensing	Entesari, Kamran	Texas A&M
61	1836.067	Characterization of CMOS Basic Building Blocks for Sub-THz Wideband Transmitters	Hella, Mona	Rensselaer
62	1836.068	Global Convergence Analysis of Mixed-Signal Systems	Kim, Jaeha	Seoul Nat'l U
63	1836.069	Electronic Systems for Small-Scale Wind Turbines	McMahon, Richard	Cambridge
64	1836.070	Optimum Control of Power converters	Ringwood, John	NUI Maynooth
65	1836.071	Design of Photovoltaic (PV) Power Harvesting CMOS Ics	Hassibi, Arjang	UT Austin
66	1836.072	Low Cost Test of High Speed Signals	Chatterjee, Abhijit	GA Tech

Table 3: TxACE Research Accomplishments September 2009 through August 2010

Category	Accomplishment
Circuits	Demonstrated a tunable 60-GHz tuned amplifier using variable inductors in 45-nm CMOS. (1836.008-1836.10, PIs: K. O, University of Texas, Dallas, J. Brewer, University of Florida
Circuits	Demonstrated a tool that lowers dynamic power of digital integrated circuits by more than 35% and lowers leakage power by more than 70%, compared to that generated using state-of-the-art EDA tools. (1836.011, PI: C. Sechen, University of Texas, Dallas)
Circuits	Demonstrated a supply-regulated PLL architecture that eliminates the tradeoff between supply noise rejection and oscillator phase noise suppression. The PLL is the first to employ bandwidth tracking and achieves the highest supply noise immunity, best power efficiency and low jitter. (1836.014, PI: P. Hanumolu, Oregon State University)
Circuits	Demonstrated a DC-DC power conversion system with software-defined control schemes. The system utilizes an all-digital temperature sensor with high resolution and low static power consumption. (1836.015, PI: D. Ma, University of Texas, Dallas (Formerly of University of Arizona)
Circuits	Demonstrated a digital SIMO step-up/down power converter for DVS-enabled multicore systems. An adaptive freewheel switching control mechanism is demonstrated for cross regulation suppression. (1836.017, PI: D. Ma, University of Texas, Dallas (Formerly of University of Arizona))
Circuits	By exploring energy-delay trade-offs in algorithm, recurrence, wiring, and circuit topology, developed the most energy efficient 64-bit adder (EZO-S2). (1836.018, PI: P. V. Oklobdjiza, University of Texas, Dallas)
Circuits	Developed a BER-aware 3-b ADC architecture with shaping gain > 30dB that has 10^6 X lower BER than a conventional 4-b ADC, and 50% savings in power consumption for flash converters. (1836.019, PIs: N. Shanbhag and E. Rosenbaum, University of Illinois, Urbana Champaign)
Circuits	Demonstrated a ΔΣ ADC that uses an auxiliary quantizer to significantly raise the maximum input stable range. Demonstrated a low complexity synthesizable all-digital domino logic based ADC. (1836.020, PI: U. Moon, Oregon State University)
Circuits	Developed a MIMO architecture for reducing far end cross talk with reduced power and area. Achieved reliable signal integrity with narrow channel spacing, increasing data throughput. (1836.022, PI: R. Harjani, University of Minnesota)

Table 3: Continued

Category	Accomplishment
Circuits	Showed uncoordinated interference in MIMO communication proposed for the latest cellular standard causes the goodput gain to decay doubly exponentially with feedback delay. Proposed rate backoff at the transmitter maximizes the achievable ergodic goodput. (1836.024, PI: R. Heath, University of Texas, Austin)
Circuits	A broadband planar bowtie antenna with 55% bandwidth has been achieved. (1836.037, PIs: R. Henderson, A. Blanchard, University of Texas, Dallas)
Circuits	A single inductor dual-input dual-output (SIDIDO) boost converter is developed for energy harvesting applications. A switching-time-aware pulse-frequency modulation control scheme is proposed to enable the converter to achieve the peak power efficiency of 89% over the load current range from 0.1mW to 16mW. (1836.041, PI: H. Lee, University of Texas, Dallas)
Circuits	Demonstrated an adaptive data prediction based ultrasound receiver with ~27-30 dB higher output dynamic range while using a lower resolution ADC (10 bit instead of 12bit). (1836.042 D. Ma, University of Texas, Dallas (Formerly of University of Arizona))
Circuits	Using current mode control in a buck regulator, reduced (2-5 x) off-chip inductor size to 1 mH and reduced chip size by ~5 to 10X. The regulator incorporates dynamically-biased shunt feedback in both peak and valley current sensors for improving the sensing speed to 2.5MHz. (1836.049, PI: H. Lee, University of Texas, Dallas)
Circuits	Created equivalent circuit model and understood impact of back-gate bias on silicon on insulator based nanowire sensor operation. (1836.055, PI: E. Vogel, University of Texas, Dallas)
CAD & Test	Developed multi-algorithm parallel circuit simulation techniques using 8 threads that speed up run time by more than 10X over serial single algorithms. (1836.006, PI: Peng Li, Texas A&M)
CAD & Test	Developed variability-enabled nonlinear phase models for PLLs that enable accurate simulation of PLL dynamics orders of magnitude faster than comparable alternatives. (1836.021, PI: J. Roychowdhury, University of California, Berkeley)

Table 3: Continued

Category	Accomplishment
CAD & Test	Developed the hierarchical Differential Algebraic Equation (HDAE) formulation core for enabling multilevel algorithms that reduces memory usage and speeds up simulation. The HDAE core has been used to enable multilevel DC, AC, transient and harmonic balance analyses. (1836.023, PI: J. Roychowdhury, University of California, Berkeley)
CAD & Test	Demonstrated a new automatic match circuit tuner using square split ring resonators (SSRR) that is 2.5x smaller in size. (1836.026, PI: K. Melde, University of Arizona)
CAD & Test	Showed that by employing the NSGA-II genetic algorithm as a heuristic basis for feature selection, latent correlations between kerf/inline parameters and module final test parameters can be uncovered. (1836.029, PI: Y. Makris, Yale University)
CAD & Test	Developed a unified statistical analysis engine for SRAM performance, yield, reliability and testability that uses a novel Gibbs sampling algorithm to improve the accuracy and speed of analysis. Demonstrated 3~10x runtime speedup over other state-of-the-art CAD techniques without any accuracy loss. (1836.044, PI: X. Li, Carnegie Mellon University)

Table 4: TxACE number of publications during the reporting period

Conference Papers	Journal Papers	Invention Disclosures
62	13	2

TASK ID# 1836.003: TEMP. COMPENSATED, HIGH COMMON MODE RANGE, CU-TRACE BASED CURRENT SHUNT MONITOR AMPLIFIER

BERTAN BAKKALOGLU, ARIZONA STATE UNIVERSITY, bertan.bakkaloglu@asu.edu
SAYFE KIAEI, ARIZONA STATE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

A current shunt monitor that accurately amplifies 10mV range voltages across a sense resistor, in the presence of large common-mode voltage up to 26V is presented. The design was completed and fabricated in 0.7um CMOS process with less than 10uV of input offset and 1uV/$\sqrt[2]{Hz}$ of flicker noise. CMRR over 120dB is also achieved.

TECHNICAL APPROACH

Instead of using external sensing resistor in the current path, existing PCB Cu-trace is used as sensing resistors for cost reduction by eliminating high accuracy external components. Better internal resistive matching and equal resistance variation over all the process corners and temperatures achieved by designing Input sensing (R_S) and gain (R_G) resistors in ratio, $\frac{R_G}{R_S} = 50$. A switching current mode FIR filter is used to cancel chopping ripple in current domain instead of using conventional voltage mode ripple reduction techniques.

SUMMARY OF RESULTS

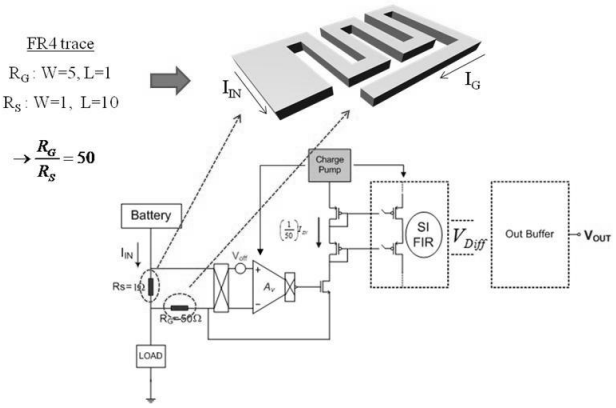


Figure 1: Matched input resistors on an FR4 trace.

The patterning of proposed Cu-Trace resistors is shown in Figure 1. Input chopping technique is applied to fulfill less than 10uV of input referred offset requirement. Since chopping technique causes ripple due to the switching, there needs to be a function that can suppress down the ripple at chopping frequency harmonics. A switching current mode FIR filter which samples and averages the two different phase chopped input signals while reducing the chopping ripples with its first order hold sinc^2 function is implemented. The switching current mode (SI) FIR filter not only reduce down the ripple by its second order notching mechanism, but also recovers original offset-free DC input current by averaging the offset-containing input signals. The following first order hold sinc^2 function as in eq. (1) is realized in the circuit in Figure 2.

$$\left|\frac{1-e^{-sT}}{s}\right|^2 = T\frac{\left|sin\left(\frac{wT}{2}\right)\right|^2}{\left|\frac{wT}{2}\right|^2} = Tsinc^2\left(\frac{wT}{2}\right) \quad (1)$$

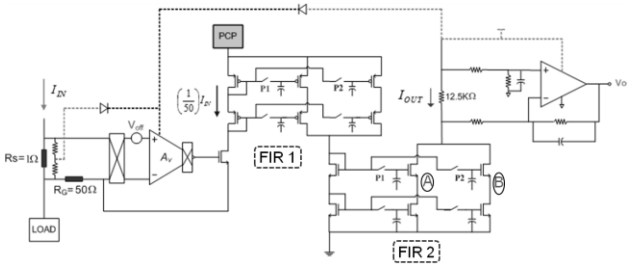


Figure 2: Detailed diagram of first order hold sinc^2 FIR.

Overall, the presented instrumentation amplifier has clear rail to rail operation with less than 10uV input referred offset and CMRR of 120 dB. The device has been fabricated with 0.7 um AMIS (ON Semiconductor) I2T100 process.

Table 1: specifications of the design

Input voltage (V)	Offset (uV)	CMRR (dB)	Input noise (V/$\sqrt{Hz}$)
0 ~ 26	10	120	1u

Keywords: Chopper stabilizers, flicker noise, Instrumentation amplifier, CMRR, ripple/residue reduction

INDUSTRY INTERACTIONS

Texas Instruments Tucson HPA (High Performance Analog) and Freescale Inc. Tempe, AZ work closely with ASU scientists

MAJOR PAPERS/PATENTS

[1] H.S. Yeom, B. Bakkaloglu, "High Common Mode Range, Cu-Trace Based Current Shunt Monitor Amplifier," (Invited) SRC 2010 TECHCON, September, 2010, Austin, Texas.

TASK ID# 1836.004, ROBUST DESIGN OF LOW POWER SMALL AREA DATA CONVERTERS IN LOW VOLTAGE DIGITAL PROCESSES

RANDALL GEIGER, IOWA STATE UNIVERSITY, rlgeiger@iastate.edu
DEGANG CHEN, IOWA STATE UNIVERSITY, djchen@iastate.edu

SIGNIFICANCE AND OBJECTIVES

The objective is to develop a method for practical on-chip testing of ADCs (BIST) and to use test results to enhance ADC performance through BIST-based calibration. This offers potential for reducing die area and power while enhancing parametric performance and reliability of systems that employ embedded data converters.

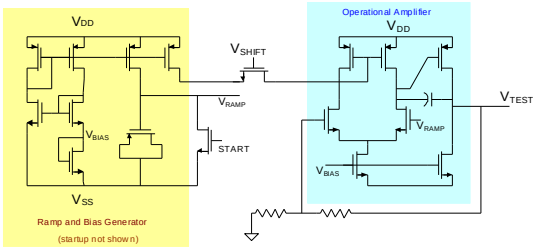
TECHNICAL APPROACH

Initially methods of testing ADCs will be developed that do not require precision test equipment but that provide reliable parametric test performance. Emphasis will be placed on approaches where excitation and measurement circuitry can be placed on-chip with minimal area overhead. Preliminary results for linearity testing have been obtained but for a practical BIST approach, all critical parametric parameters of an ADC must be testable. In this work emphasis is placed both upon reducing the size of the test circuitry and on extending previous results to include other parametric parameters such as spectral performance, gain, and offset parameters.

SUMMARY OF RESULTS

A comparison of several different algorithms that can provide INL and DNL test results without requiring precise or known signal generators has been made. This comparison has been restricted to testing strategies based upon the Functionally Related Excitation (FRE) method of on-chip testing. This comparison shows that there are not significant differences in parametric performance between the different test approaches that have been published but some offer reductions in hardware complexity.

Methods of generating the test signals have been investigated. Emphasis has been placed upon circuits that can generate a sufficiently constant shift and on methods for using a series of faster-rising ramps that do not have correlation of break points from one ramp signal to the next. Results show that simple shift generators that exploit the offset voltage in an operational amplifier that results from a switchable asymmetry are adequate for INL testing of ADCs with resolution up to 18 bits. The concept is illustrated in the following figure where the mismatch in bias current of the differential inputs is controlled by V_{SHIFT}.



Keywords: BIST, Analog-BIST, SEIR, Self-calibration

STUDENTS

Jingbo Duan, Bharath Vasan, and Siva Sudani

INDUSTRY INTERACTIONS

Texas Instruments, Liaisons: Irene Deng, Steve Howard

MAJOR PAPERS/PATENTS

[1] Duan J. et al., "Cost Effective Signal Generators for ADC BIST", ISCAS, 2009.

[2] Duan J. et al., "Stimulus Generator for SEIR Method Based ADC BIST", NAECON 2009.

[3] Vasan, B. et al, "Signal generators for cost effective BIST of ADCs", ECCTD 2009.

[4] Duan, J. "Chip Implementation of Low Overhead ADC BIST", TECHON 2009.

[5] Duan, J. et al., "Phase Control of Triangular Stimulus for ADC BIST", ISCAS, 2010.

[6] Duan, J. et .al., "INL Based Spectral Performance Estimation for ADC BIST", ISCAS 2010.

[7] Vasan, B. et al. ,"Linearity testing of ADCs using low linearity stimulus and Kalman filtering", ISCAS 2010.

[8] Duan, J. et al., "A New Method for Estimating Spectral Performance of ADC from INL", ITC 2010 (to appear).

[9] Vasan, et al "Linearity testing of ADCs using imprecise sinusoidal excitations", NAECON 2010.

[10] Duan, J. et al., "Sensorless Temperature Measurement Based on ADC Input Noise Measurement", NAECON 2010.

[11] Duan, J.,"Phase Control of Triangular Stimulus for ADC BIST",TECHON 2010.

TASK ID# 1836.005, A LARGE-N LOW-JITTER DIGITALLY-CONTROLLED OSCILLATOR (DCO)-BASED FREQUENCY MULTIPLIER

PING GUI, SOUTHERN METHODIST UNIVERSITY, pgui@smu.edu

SIGNIFICANCE AND OBJECTIVES

Conventional PLL-based frequency multiplier becomes not feasible when the multiplication ratio N is very large ($N \geq 1000$). This project seeks to design a digital frequency multiplier that is able to handle such a large N with very low jitter. This approach employs minimum analog complexity, and is easily transferable across technologies.

TECHNICAL APPROACH

The proposed frequency multiplier utilizes a Flying-Adder-based Digital Controlled Oscillator (FA-DCO) and a frequency-to-digital converter (FDC) in a unique configuration. By employing both an FDC and a DFC, frequencies are represented in the digital or software domain. Digital or software processing can be utilized to produce the desired relationship $f_{out} = N \cdot f_{in}$, where the multiplication ratio N can be either an integer or a real number. This frequency multiplier is capable of generating a large range of frequencies instantaneously. Additionally, a digital modulation technique is introduced and implemented in this architecture to reshape the clock spectrum for electromagnetic interference (EMI) reduction.

SUMMARY OF RESULTS

We have designed and implemented the FA-DFC-based frequency synthesizer structure (show in Fig. 1) capable of generating a low-jitter high-frequency output clock from a noisy low-frequency input and providing a range of available frequencies [1]. Silicon measurement results have demonstrated the following features of this frequency multiplier: 1) the input clock frequency can be very low, even in Hz range, and the multiplication ratio N can be very large ($N \geq 1000$); 2) the jitter associated with the input will not propagate to the output; 3) the output clock can follow instantly with the change in input clock frequency or the multiplication ratio; 4) digital modulation circuits are shown capable of spreading the clock spectrum or reducing the spurious frequencies. In addition, we have also completed a thorough mathematical analysis on the effects of the FA-based clock on embedded systems such as DACs [2-3]. A Redundant Signed-Binary-Addition-Based Digital-to-Frequency converter is also proposed and implemented to eliminate the speed bottleneck of the FA-DCO [4]. Moreover, a new DCO architecture which employs both sigma-delta Fractional-N and the Flying-Adder synthesizer is proposed and implemented to improve the jitter performance of the FA-DCO [5].

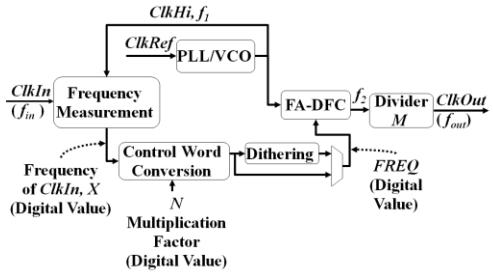


Figure 1: The block diagram of the FA-DFC-based frequency generator capable of handling large multiplication ratio N.

Keywords: Frequency Multiplier, Fractional-N, Flying-Adder, Jitter, Spread Spectrum, Sigma Delta

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] W. Chen, P. Gui and L. Xiu, "A Low-Jitter Large-N Frequency Multiplier", SRC TECHCON, 2008.

[2] P. Gui, Z. Gao, C. W. Huang, L. Xiu, " The Effects of Flying-Adder Clocks on Digital-to-Analog Converters", *IEEE Transaction on Circuits and Systems II* in Vol. 57, No. 1, pp.1-5, 2010.

[3] L. Xiu, C. W. Huang, P. Gui, " The Analysis of Harmonic Energy Distribution Portfolio For Digital-to-Frequency Converter", To appear in *IEEE Transactions on Instrumentation and Measurement*, Vol. 59, No. 4, 2010.

[4] W. Chen, M.A. Thornton, and P. Gui, "A Redundant Signed Binary Addition Based Digital-to-Frequency Converter", *IEE Electronics Letters*, vol. 45, no. 2, pp. 824-826, July 2009.

[5] C-W Huang, P. Gui, " A 250 MHz-4 GHz Sigma-Delta Fractional-N Frequency Synthesizer with Adjustable Duty Cycle", Proceedings of *International Symposium on Circuits and System (ISCAS),* 2010.

TASK ID# 1836.006, MULTI-CORE & DISTRIBUTED PARALLEL SIMULATION FOR DESIGN AND VERIFICATION OF CUSTOM DIGITAL AND ANALOG ICS

PENG LI, TEXAS A&M UNIVERSITY, pli@tamu.edu

SIGNIFICANCE AND OBJECTIVES

Transistor-level circuit simulation is a fundamental, yet computationally intensive, design and verification enabler for wide ranges of digital and analog circuits. We address the significant simulation challenge by developing novel parallel simulation paradigms on multi-core and distributed computing platforms.

TECHNICAL APPROACH

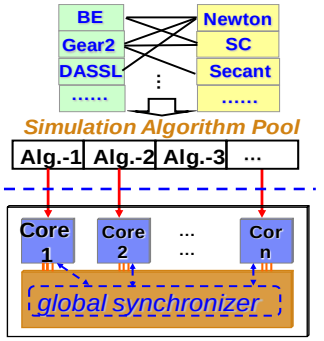
Novel parallel computing paradigms are developed to exploit rich simulation application level parallelisms. These approaches are designed to minimize inter-processor communication overhead, achieve good scalability, and simplify parallel programming implementation. We not only develop intra-algorithm but also unconventional inter-algorithm parallel approaches. In the latter, multiple simulation algorithms are launched for a single simulation task. The goal is to create orthogonal opportunities such that massively parallel machines can be well utilized. Furthermore, we develop parallel performance models to facilitate static and runtime simulation code optimization.

SUMMARY OF RESULTS

We develop novel algorithms that complement conventional parallelization approaches and allow for efficient use of parallel hardware.

For harmonic balance based steady-state and envelope following analysis, we have developed a robust hierarchical preconditioner. It not only leads to fast convergence for strongly nonlinear problems but also is naturally parallelizable by construction. In the time domain, we have demonstrated a coarse-grained approach, *Waveform Pipelining*, for transient simulation. Transient responses at multiple time points are computed in parallel by exploiting multi-step numerical integration methods and predictive computing at future time points while guaranteeing the simulation convergence and accuracy. In a different perspective, by exploiting the recently developed telescopic numerical integration method, we have leveraged stable explicit numerical integration for parallel simulation. With a multi-level integration scheme, this approach addresses the known stability limitations of existing explicit integration methods and facilitates natural parallelization. The same basic principle has also been extended to a novel bi-directional parallel simulation approach for digital timing and steady-state analysis.

With an increased parallelization granularity, we have developed a multi-algorithm parallel circuit simulation (MAPS) framework. Unlike most existing approaches, MAPS exploits inter-algorithm parallelisms by launching multiple simulation algorithms in parallel for a given simulation task (Fig. 1 left). By properly synchronizing these algorithms on-the-fly, we exploit the diversity in simulation algorithms to achieve significant speedups over a standard serial single-algorithm reference, which employs backward Euler numerical integration and Newton iterative method (Fig. 1 right). The coarse grained nature of MAPS leads to simple parallel implementation and reuse of existing simulation codes.



Circuit	4-thread MAPS speedup	8-thread HMAPS speedup
Logic 1	7.39x	9.98x
Logic 2	13.0x	23.12x
Clock 1	10.60x	6.29x
Clock 2	19.36x	37.89x
Clock 3	19.19x	39.69x
LNA+Mixer	7.22x	7.16x

Figure 1: left: multi-algorithm parallel circuit simulation; right: runtime speedups over a single-algorithm reference.

In the following year, we will develop parallel performance modeling approaches that allow for static and runtime optimization of MAPS.

Keywords: Circuit simulation, parallelization, transient analysis, steady-state analysis, parallel code optimization.

INDUSTRY INTERACTIONS

Texas Instruments, Intel, AMD, Freescale

MAJOR PAPERS/PATENTS

[1] X. Ye, W. Dong, P. Li and S. Nassif, IEEE/ACM ICCAD'09.

[2] W. Dong and P. Li, IEEE TCAD'09.

[3] W. Dong and P. Li, IEEE/ACM ICCAD'09.

[4] X. Ye and P. Li, IEEE/ACM DAC'10.

TASK ID# 1836.007, SOFTWARE DEFINED/RECONFIGURABLE MULTI-MODE SERIAL LINK CONTROLLER ARCHITECTURE

VOJIN G. OKLOBDZIJA, UNIVERSITY OF TEXAS AT DALLAS, vojin@acsel-lab.com
PORAS T. BALSARA, UNIVERSITY OF TEXAS AT DALLAS

SIGNIFICANCE AND OBJECTIVES

This work introduces a novel Multi-mode Serial Link Controller (MMSLC) for logic physical layer (PHY) and data link layer (DLL) of USB 3.0, PCIe 2.0 and SATA 3.0. This architecture may accommodate multiple revisions of existing protocols and also for standards with similar protocol stacks, the approach may be extended across different communication protocols.

TECHNICAL APPROACH

Our purpose is to define a feasible approach towards an efficient and reconfigurable controller that can be utilized by multiple protocols when implementing their logic PHY and DLL functions. This framework is designed to exploit the similarities amongst multiple serial-link protocols to achieve flexibility in implementation and reduction in power. The framework is divided in 3 groups- 1) configurable circuit, 2) programmable accelerator and 3) event processor, each with distinct functionalities and speeds of operation.

SUMMARY OF RESULTS

For a given functionality, our analysis indicates the necessity of introducing dedicated functional components as well as the possibility of sharing these across protocols. Based on similarity and throughput features, we define an entire architecture as shown in Figure 1, which contains UP-PHY and CRC modules implemented as configurable circuits, Framer and Deframer as programmable accelerators, and a microcontroller with event queue forming an event processor. An internal control bus is used by the processor to set-up configurable/programmable peripherals at initialization.

Group 1: The logic UP-PHY defines functions for processing bit streams including serialization/ deserialization, clock tolerance, encoding/decoding and scrambling/ descrambling.

Group 2: The framing/deframing module is a major part of DLL, which is responsible for constructing and extracting frames exchanged with logic PHY. So, data input and output rate is about 500M symbols per second (Sps) in USB 3.0 and PCIe 2.0 and 600M Sps in SATA 3.0.

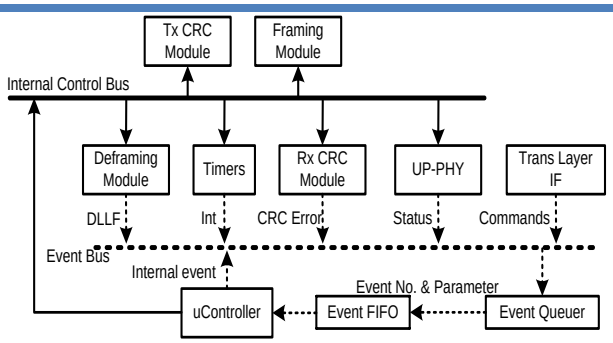


Figure 1: Overview of the MMSLC architecture

Group 3: Our estimation of DLL in protocols also indicates the need of an embedded processor for event handling. These events will result in terrible context-switching overhead, as if using typical interrupt mechanism, when we take into account the high event frequency and large number of events. A complete context switching will cost almost 15 instruction cycles which occupies 60% of an average event handler. So we use a 2-phase event queuing mechanism to prevent processor from responding directly to an event.

The RTL model was synthesized in Synopsys using 90nm standard cell library to estimate the area of the circuit as well as to verify if the speed can meet the protocol's requirement. The results show that this architecture is capable of achieving the high-speed requirements of around 500MHz symbol rate for serial link protocols and realize area reduction over conventional link controllers running each protocol individually.

Furthermore, we are working towards broadening this work to achieve improved energy efficiency in MMSLC architecture.

Keywords: link controller, reconfigurable architecture, serial-link protocols, communication standards

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Lei Wang, Vishal Nawathe, Pawankumar Hegde et al., "Design of a Link-Controller architecture for Multiple Serial Link Protocols Energy-Efficient", IEEE SOCC 2010, Las Vegas, Nevada, USA, 27-29 September 2010.

TASK ID# 1836.008, DIGITAL ASSISTED MM-WAVE CMOS CIRCUITS

J. E. BREWER, UF, jebrewer@ufl.edu
K.K.O, UTD, k.k.o@utdallas.edu

SIGNIFICANCE AND OBJECTIVES

To improve yield and shorten time to market of millimeter wave CMOS circuits, this task is Investigating the feasibility of incorporating digitally-controlled built-in tuning in millimeter wave circuits that mitigates the impact of process variations, modeling uncertainty of passive and active components.

TECHNICAL APPROACH

Detectors placed at the input and output of front-end amplifiers and mixer outputs of an RF transceiver can be used for measurements needed for tuning/calibrating the receiver and transmitter. The key challenges for realizing a digital assisted system operating at millimeter wave frequencies are (1) inexpensively injecting test signals, (2) incorporating tuning elements which do not add significant parasitics and degrade circuit performance, and (3) realizing high impedance broadband detectors with sufficient dynamic range. This effort will understand these challenges, and the limitations in the context of a 77-GHz reconfigurable low noise and power amplifiers fabricated in 45-nm CMOS.

SUMMARY OF RESULTS

Test structures of tunable components including variable capacitors, inductors, and loads have been simulated and fabricated in 45-nm CMOS. The variable inductor has the maximum to minimum inductance ratio of ~1.8. A tunable 77-81 GHz low noise amplifier in Figure 1 has been fabricated. The four stage amplifier includes four tunable inductors that can tune the inter-stage matching. The center frequency gain can be tuned from 76 to 82 GHz, while that for the output matching can be tuned from 70-81 GHz. The amplifier achieves peak gain greater than 15 dB and minimum noise figure of ~8 dB.

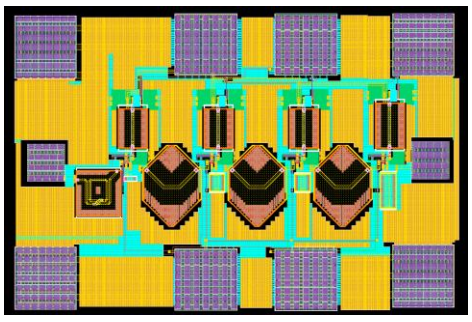


Figure 1: 77-81 GHz tunable low noise amplifier.

Test structures of diode detectors are also fabricated in the same process technology. The insertion of high impedance detector introduces around ~0.2-dB loss at 77 GHz. The detector as shown in Figure 2 also includes low pass filters and a chopper stabilized amplifier. The rms diode detector has dynamic range greater than 50 dB.

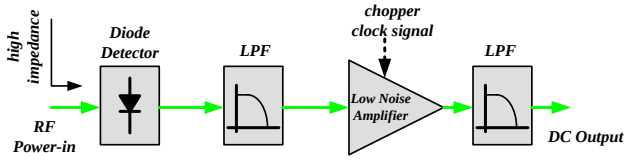


Figure 2: Diode detector and amplification circuits

The test structures and circuits are being characterized. A tunable power amplifier is being designed. Based on the measurements, the LNA and detector will be redesigned and integrated. Detectors will also be integrated into the power amplifier. Lastly, techniques for tuning a set of circuit parameters, including gain, linearity, and noise performance will be investigated.

Keywords: tunable, mm-wave, low noise amplifier, power amplifier.

INDUSTRY INTERACTIONS

Texas Instruments and Freescale

MAJOR PAPERS/PATENTS

[1] N. Zhang and K. K. O, "W-Band Pulsed Radar Receiver in Low Cost CMOS," Accepted to 2010 CICC.

[2] C. Mao et al., "Diodes in CMOS for Millimeter and Sub-Millimeter Wave Circuits," **(Invited)** 2010 Intl. Sym. on VLSI Tech., Systems and Applications, April, 2010, Hsinchu, Taiwan.

[3] C. Mao and K. K. O, "60-GHz Hybrid Transmit/Receive Switch Using p-n Diode and MOS Transistors," 2009 Symposium on VLSI Circuits, pp. 248-249, June 2009, Kyoto, Japan.

[4] N. Zhang et al., "CMOS Freq. Gen. Syst for W-Band Radar," 2009 Symp. on VLSI Circs., pp.126-127, June 2009, Kyoto, Japan.

[5] C. Mao et al., "65/130 GHz diode frequency doubler in 0.13-mm CMO," IEEE JSSC, vol. 44, no. 5, pp. 1531-1538, May 2009.

TASK ID# 1836.011, POWER MINIMIZATION AND YIELD OPTIMIZATION IN DIGITAL ICS

CARL SECHEN, UNIVERSITY OF TEXAS-DALLAS, carl.sechen@utdallas.edu

SIGNIFICANCE AND OBJECTIVES

We address power minimization given a delay target in a synthesized digital logic block. To that end, we engineered a reduced cell library along with our optimal cell size selection algorithms that combine to achieve power reductions on large, contemporary industrial circuits.

TECHNICAL APPROACH

Tools have been produced that lower dynamic power by more than 35% on actual industrial digital circuits, and which lower leakage power by more than 70%, compared to state-of-the-art EDA tools. The tools select the optimal cell size and the optimal Vt among the options available in a cell library. The contents of a power-optimal physical cell library have been identified, and the contents of a (rather different) power-optimal synthesis cell library have been determined. The physical cell library (only 8 gate types) is dramatically smaller than those currently used in industry, while achieving much lower dynamic and leakage power for industrial circuits.

SUMMARY OF RESULTS

We demonstrated that optimal cell size selection, including optimized threshold voltage selection, along with a new discrete cell size mapping algorithm enable substantial reductions in total power and leakage power for industrial digital blocks compared to leading synthesis tools. We were further able to engineer a highly power efficient cell library composed of far fewer cells than is common in commercial libraries, including functional content, drive strengths and beta ratios. The size selection algorithms in conjunction with the reduced library size enable this combination of library and tools to efficiently handle the large layout partitions used in contemporary ASICs, which typically have 500k to 2 million sizeable cells.

Our approach includes nearly globally optimal cell size selection from options in a standard cell library, as well as nearly optimal Vt selection among options available in the cell library. We have also developed precise static timing analysis, accurate to spice and more accurate than the leading commercial static timing analyzer. Our tools handle commercial multi-million gate designs today. We have also developed the most power efficient standard cell library that consists of only 8 combinational gate types in addition to flip-flops.

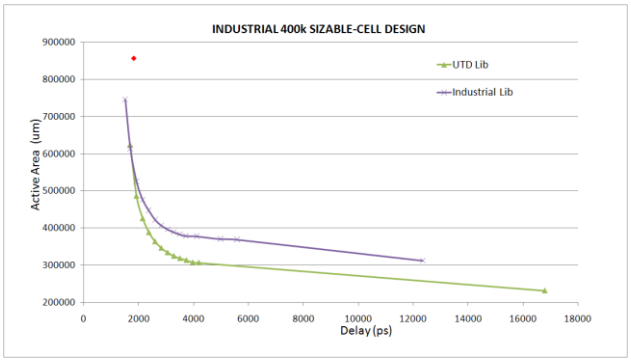


Figure 1: A typical result is shown above for a 2010 multi-million gate industrial design in 40nm. The red dot is the best result produced by the leading commercial synthesis tool. Active area, immediately proportional to dynamic power, was reduced by more than 2X (for the same delay) and the UTD optimal cell library (using only 8 types of gates) reduced dynamic power by 20% over a leading commercial cell library. Leakage power was reduced by 80% versus the leading commercial synthesis tool for the same delay.

Keywords: Gate sizing, gate size selection, threshold voltage selection, power minimization, optimal cell libraries.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] M. Rahman, H. Tennakoon, and C. Sechen, “Near Optimal Power Efficiency Through Gate Sizing”, Proc. Austin Conf. on Integrated Circuits and Systems (ACISC), Oct. 26-27, 2009, Austin, TX.

[2] R. Afonso, M. Rahman, H. Tennakoon, and C. Sechen, “Power Efficient Standard Cell Library Design”, Proc. IEEE Dallas Circuits and Systems Society Workshop, Oct. 4-5, 2009, Dallas, TX.

[3] H. Tennakoon and C. Sechen, “Non-convex Gate Delay Modeling and Delay Optimization,” IEEE Trans. on Computer-Aided Design, Vol. 27, No. 9, September 2008, pp. 1583-1594.

[4] Several patents are planned for late 2010.

TASK ID# 1836.012, STRUCTURAL FAULT MODELING, TESTING, AND DEFECT LEVEL ESTIMATION FOR ANALOG/RF CIRCUITS

SULE OZEV, ARIZONA STATE UNIVERSITY sule.ozev@asu.edu

SIGNIFICANCE AND OBJECTIVES

In order to provide an alternative to specification-based testing, various test and built-in-test techniques have been proposed. However, there is a lack of a mechanism to predict the test quality This project aims at (a) fault modeling, (b) test development based on these models, (c) estimating the overall test quality.

TECHNICAL APPROACH

Fault models are based on continuous behavior of defects. A statistical framework is developed to evaluate and define tests based on the continuous fault models together with process variations. The process variation model includes both within-die and die-to-die components. For test development, both specifications and other parameters are considered. These tests can be evaluated with respect to their fault coverage. Based on statistical analysis, each test has a certain probability of detecting deviations in a given parameter. By collecting this statistical information over many parameters, an overall fault coverage metric can be calculated and used to select tests.

SUMMARY OF RESULTS

First, parametrizable defect models have been generated using 3D electromagnetic simulations. Various defect sizes have been simulated for known defect types, such as missing vias, pinhole defects, etc. A library of faults based on defect size has been generated. Probability of a defect decreases with its size. Using this information, and the defect simulation based on size, each circuit can be evaluated using transistor-level simulations.

Two issues make these simulations quite challenging. First, with process variations, each fault simulation becomes a statistical simulation, making it computationally very expensive. Second, such fault simulation also requires the knowledge of absolute defect probability, which is generally not available.

We aim at resolving these issues with novel approaches. Inductive fault analysis tries to obtain defect probabilities. However, accuracy is typically limited. We take a unique approach where we decouple the inductive fault analysis from the absolute defect probability. Inductive fault analysis is used to obtain a relative probability distribution for each fault. For example, a break in a thick metal line is much less likely than a break in a thin metal line. Then, we use initial characterization data, in conjunction with outlier analysis to determine a baseline defectivity level. Combined with relative fault probabilities, this defectivity level is used to approximate the defect probability.

In order to solve the tractability problem, we develop a hierarchical fault simulation methodology. First, we attack the problem of high number of simulations by classifying fault responses with respect to how far they lay from the specification or pass/fail limits. This first cut eliminates a large number of faults from more extensive simulations as their responses are immediately classifiable as pass or fail. For the remaining faults, we take advantage of the layered nature of process variations. For die-to-die variations, we have only a small number of parameters, and can afford to use enumerative techniques, such as Taguchi's method. For within-die variations, the number of parameters is large. However, variations are smaller. We conduct a more detailed characterization of these faults. Table I shows the speed-up we can achieve when compared with Monte-Carlo simulations alone for an LNA circuit.

TABLE I: Speed-up in fault simulations when compared with Monte-Carlo analysis

# Simulations		DPPM Error	
MC	Proposed	MC	Proposed
100K	3K	0	0.4

Keywords: fault modeling, analog testing, test development, fault simulation, test quality

INDUSTRY INTERACTIONS

Texas Instruments, Intel, IBM, Freescale

MAJOR PAPERS/PATENTS

"Accurate Multi-Specification DPPM Estimation Using Layered Sampling Based Simulation", ISQED 2010.

"Defect-Based Test Optimization for Analog/RF Circuits for Near-Zero DPPM Applications", ICCD 2009.

TASK ID# 1836.013, WIDEBAND RECEIVER ARCHITECTURES IN DIGITAL DEEP SUBMICRON CMOS

SEBASTIAN HOYOS, TEXAS A&M UNIVERSITY, COLLEGE STATION, hoyos@ece.tamu.edu
JOSE SILVA-MARTINEZ, TEXAS A&M UNIVERSITY, COLLEGE STATION

SIGNIFICANCE AND OBJECTIVES

Provide innovative solutions to achieve high performance, flexibility, and low power consumption required in ΔΣ analog-to-digital converters (ADCs) for multi-standard receivers. Apply the proposed system- and circuit-level techniques to the design of a low power ΔΣ ADC. Implementation of a CMOS chip prototype for the ADC and obtain experimental measurements to demonstrate the potential of the proposed solutions.

TECHNICAL APPROACH

The main approach is to achieve the required flexibility in multi-standard RF receivers by exploiting the enormous momentum in digital signal processors (DSPs). Particularly, the incoming signal at the receiver input is to be digitized as early as possible while filtering operations and channel selection are performed in the digital domain. In this context, continuous-time ΔΣ modulators show up as an attractive option for the ADC implementation. Continuous-time ΔΣ structures offer amenability for operating at a high speeds with lower power consumption, compared to discrete-time implementations, inherent anti-aliasing, and robustness to sampling errors, Furthermore, digital filtering achieved by the digital decimator filter following the ΔΣ modulator can be used for channel selection.

SUMMARY OF RESULTS

The block-diagram of the continuous-time ΔΣ ADC structure is shown in Fig. 1.

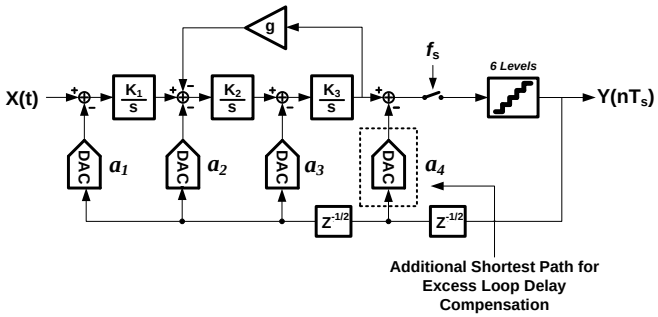


Figure 1: Third-order continuous-time ΔΣ modulator with 6 levels quantizer and sampling frequency, *fs*=450 MHZ.

The modulator is arranged in a cascade-of-resonators feedback (CRFB) structure for two main reasons. First, to provide inherent low-pass filtering along the signal path from modulator input to modulator output so that to attenuate out-of-band (OOB) interferes, accompanied by the desired signal at the modulator input. OOB blockers can overload the loop quantizer and/or saturate loop filter and hence drive the ADC unstable. Second, to achieve adequate suppression for sampling images. Particularly, having the cascade of all the loop integrators in the signal path provide adequate suppression for wideband images by aggressive inherent anti-aliasing filtering.

There are two main challenges for that ADC to achieve the required performance within a multi-standard receiver:

1. Pulse width jitter associated with the clock of the feedback digital-to-analog converters.
2. Tolerance to OOB blockers in terms of loop filter linearity and noise folding.

Solutions to these two critical problems are being addressed by the ongoing research effort in this project.

Keywords: ΔΣ modulator, ADC, blocker-tolerance, clock-jitter, continuous-time

INDUSTRIAL LIAISONS

Venkatesh Srivinisan, Texas Instruments Inc., Dallas TX

PARTICIPATING STUDENTS

Ramy Ahmed, PhD student, Texas A&M University, College Station TX

MAJOR PAPERS/PATENTS

[1] R. Ahmed, S. Hoyos, and J. Silva-Martinez, "Hybrid Clock-Jitter Error Shaping Technique for Feedback Digital-to-Analog Converters (DACs) in Continuous-Time Sigma-Delta Modulators," SRC TECHCON 2010 Proceedings, Paper/Poster Number: 14.3, to appear September 2010.

[2] R. Saad and S. Hoyos, "Sensitivity of single-bit continuous-time analogue-to-digital converters to out-of-band blockers," IET Electronics Letters, vol. 46, no. 12, pp.826-828, June 2010.

[3] R. Saad, S. Hoyos, and J. Silva-Martinez, "Novel Hybrid Clock-Jitter Tolerant Error Shaping Feedback DAC," SRC/GRC Patent Program, approved for patent application, June 2010.

TASK ID# 1836.014: DIGITAL PHASE-LOCKING CIRCUITS FOR CLOCK GENERATION & DATA RECOVERY IN HIGH-SPEED COMM. LINKS

PAVAN KUMAR HANUMOLU, OREGON STATE UNIVERSITY, hanumolu@ece.orst.edu
KARTI MAYARAM, OREGON STATE UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

Phase-locked loops (PLLs) are essential building blocks in all digital, analog, and radio frequency integrated circuits. The main objective of this work is to design robust, scalable, low-power, low-noise PLLs that are immune to supply noise in deep submicron CMOS processes.

TECHNICAL APPROACH

The approach is based on co-optimizing the PLL system and its circuits simultaneously to achieve the best power efficiency and low-jitter performance. To this end, a split-tuned supply-regulated PLL architecture is invented to overcome the tradeoff between the power, noise, and supply-noise immunity of conventional PLLs. An all-digital PLL architecture that obviates the need for a high resolution time-to-digital converter is proposed to improve the noise, power, and operating range of conventional digital PLLs by nearly an order of magnitude. Low power digital signal processing is used to alleviate the accuracy requirements of analog circuits.

SUMMARY OF RESULTS

The proposed supply-regulated PLL employs a split-tuned architecture to decouple the tradeoff between supply-noise rejection performance and power consumption. The prototype PLL, incorporating a novel regulator, is fabricated in a 0.18um digital CMOS process and operates from 0.5 to 2.5GHz. At 1.5GHz, the proposed PLL achieves a worst-case noise sensitivity of -28dB (0.5rad/V), an improvement of 20dB over conventional solutions, while consuming 2.2mA from a 1.8V supply.

Supply-noise significantly affects the jitter performance of ring oscillator-based PLLs. While the focus of much of the prior art is on supply-noise in oscillators, this work illustrates that supply-noise in other building blocks also contribute significantly to PLL output jitter. Our design employs a split-tuned PLL architecture wherein the power supply of the building blocks is derived from the regulated power supply of the VCO. The prototype PLL fabricated in a 0.18um digital CMOS process occupies 0.18mm^2 and consumes only 3.3mW, from a 1.8V supply, of which 0.54mW is consumed in the regulators, while operating at 1.5GHz. The PLL achieves 33ps and 41ps peak-to-peak jitter with no supply noise and with 100mV peak-to-peak supply noise, respectively.

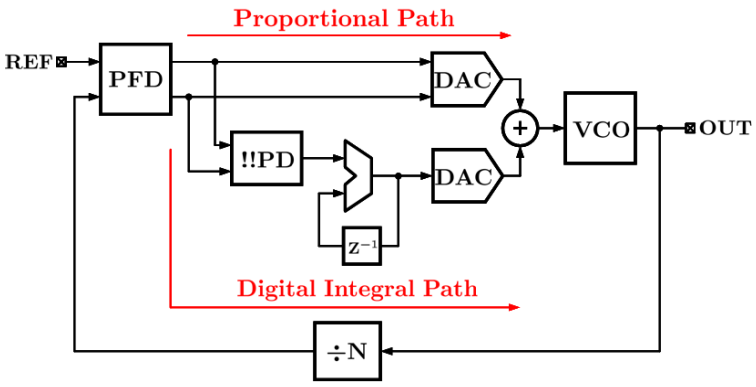


Figure 1: Simplified block diagram of the proposed digital PLL.

The proposed digital PLL employs a linear proportional path, a double integral path, bandwidth and tuning range tracking, and a novel delta-sigma digital to analog converter to achieve low jitter, wide operating range and low power. The prototype digital PLL fabricated in a 90nm CMOS process operates from 0.7GHz to 3.5GHz. At 2.5GHz, the digital PLL consumes only 1.6mW power from a 1V supply and achieves 1.6ps and 11.6ps of long-term r.m.s and peak jitter, respectively.

Keywords: PLL, regulator, jitter, delta-sigma, loop filter.

INDUSTRY INTERACTIONS

Texas Instruments, Intel, IBM

MAJOR PAPERS/PATENTS

[1] A. Arakali et al., "A 0.5-to-2.5GHz supply-regulated PLL with noise sensitivity of -28dB," *IEEE Custom Int. Circuits Conf.*, pp. 443-446, Sep. 2008.

[2] A. Arakali et al., "Supply-noise mitigation techniques in phase-locked loops," *IEEE European Solid-State Circuits Conf.*, pp. 374-377, Sep. 2008.

[3] A. Arakali et al., "Low-power supply-regulation techniques for ring oscillators in phase-locked loops using a split-tuned architecture," *IEEE J. Solid-State Circuits*, pp. 2169-2181, Aug. 2009.

[4] W. Yin et al., "A 1.6mW 1.6ps-rms-Jitter 2.5GHz digital PLL with 0.7-to-3.5GHz frequency range in 90nm CMOS," *IEEE Custom Int. Circuits Conf.*, Sep. 2010.

[5] A. Arakali et al., "Analysis and Design Techniques for Supply-Noise Mitigation in Phase-Locked Loops," *IEEE Trans. Circuits Syst. I.* (to appear)

TASK ID# 1836.015, SOFTWARE-DEFINED DIGITAL MULTIPLE-OUTPUT DC-DC CONVERTER FOR DYNAMIC THERMAL MANAGEMENT

DONGSHENG MA, THE UNIVERSITY OF TEXAS AT DALLAS, dma@email.arizona.edu

SIGNIFICANCE AND OBJECTIVES

Power dissipation is identified as a Grand Challenge by ITRS, due to aggressive transistor scaling techniques and increasing on-chip operating frequencies. Therefore, modern computing systems urgently require techniques such as dynamic voltage scaling (DVS) and dynamic thermal management (DTM). Hence, this research involves the development of an integrated DC-DC power conversion system for power-efficient SoCs and embedded applications.

TECHNICAL APPROACH

As the enabling technology for adaptive power and thermal management, this research proposes a powerful and cost-effective single-inductor multiple-output (SIMO) DC-DC power converter design. The system design explores joint system optimization through power/thermal control algorithms, sensing techniques, multi-direction power flow control, and converter architectures.

The research explores the use of software-defined digital control algorithms that can be integrated within microprocessors. This enables an autonomous and power-aware design, while maintaining compatibility with future semiconductor technologies.

On-chip temperature tracking and thermal management techniques that are compatible with the proposed SIMO DC-DC power conversion system also ensure joint power- and thermal-efficient operation.

SUMMARY OF RESULTS

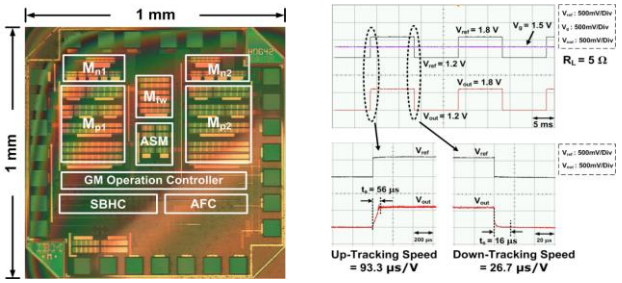


Figure 1. Chip photo and DVS measurement results of a DC-DC power conversion system using software-defined digital control schemes.

Figure 1 illustrates the prototype of a DC-DC power conversion system, based on a 'design-for-system' approach. The converter employs several software-defined control schemes to reconfigure the system architecture on-the-fly, based on the instant load power demands, supply voltages and processor workloads.

Various digital control algorithms are investigated to ensure optimal system operation during all conditions of start-up, steady state and DVS/load transient. The software-based controller also enables its integration with microprocessors, leading to a power-aware SoC design. Such an implementation allows the hardware-based power management module to fully exploit the abundance of software-based resources.

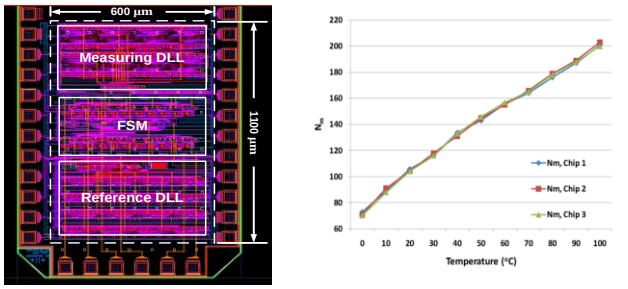


Figure 2. Layout and measurement results of the all-digital temperature sensor.

To achieve both power and thermal-efficient operation, Figure 2 illustrates an all-digital temperature sensor. The introduction of the sensor provides the dual features of thermal protection and thermal compensation. Accurate on-chip temperature tracking improves system robustness, by preventing local hotspots. The synergetic closed-loop operation with the DC-DC power converter enables thermal compensation, by which fast reference-tracking converters can provide optimal supply voltages at the operating temperatures.

Keywords: Dynamic voltage scaling, power management, on-line power sensing, single-inductor multiple-output (SIMO) converter, software-defined control schemes.

INDUSTRY INTERACTIONS

Texas Instruments Inc., Intel Corp.

MAJOR PAPERS/PATENTS

[1] Y. Zhang, et al., *IEEE ECCE,* Sept. 2010.
[2] Y. Zhang, et al., *ASP JOLPE*, (submitted on Jul. 2010).
[3] R. Bondade, et al., *IEEE ISCAS,* pp. 617-620. May 2010.
[4] D. Ma, et al., *IEEE CAS Magazine,* pp. 14-30. Mar. 2010.
[5] C. Zheng, et al., *IEEE ISSCC*, pp. 204-205, Feb. 2010.
[6] R. Bondade, et al., *ACM TODAES,* (submitted on Feb. 2010).
[7] F. Luo, et al., *IEEE ISLPED*, pp. 319-322, Aug. 2009

1836.016 BRIDGING THE SYNTHESIS GAP FROM CIRCUITS TO SYSTEMS FOR SCALED MIXED-SIGNAL SILICON

T. MUKHERJEE, CARNEGIE MELLON UNIVERSITY, tamal@ece.cmu.edu
R. A. RUTENBAR, CARNEGIE MELLON UNIVERSITY rutenbar@ece.cmu.edu

SIGNIFICANCE AND OBJECTIVES

Develop novel methodology and unified numerical optimization methods that will allow us to reuse existing designer-derived verification and exploration models, but re-purpose these for use in system-level parameter optimization.

TECHNICAL APPROACH

We "co-optimize" the system as a set of small circuit level tasks, married to a few large (but efficient) analytical system-level models. The hybrid synthesis strategy has three key novel features: (1) we strive to reuse (i.e., to respect) the existing models used by practicing system designers; (2) we optimally leverage existing cell-level optimization tools; (3) we can bring first-order statistical optimization into the same framework, by extracting statistical tradeoff models from key circuits, and inserting these into the system-level design problem.

SUMMARY OF RESULTS

Over the last year we have integrated our Stochastic Pijavskij Tunneling (SPT) algorithm into an evolutionary framework as shown in Figure 1. The original stochastic approach finds the global minimum through a few deep searches. The evolutionary approach uses a population of partial solutions. Each Pijavskij tunnel (PT) performs a shallow search and updates the population. Essentially this leads to many many shallow PT searches.

The evolutionary Pijavskij tunneling (EPT) was applied to our standard benchmark, a proprietary Freescale design of a 3rd order continuous time sigma-delta with 4-bit quantizer. Freescale's challenge was to take the Matlab modulator model and optimize SNR to "at least 80 dB".

Assuming an ideal op-amp in the $\Sigma\Delta$ model, with SPT, we achieved 74 dB with 1400 simulation runs after year 1, and about 84 dB with about 4200 simulation runs in year 2 of this project. The EPT optimizer uses approximately one day per run, and all 10 runs in a sample EPT has good results. All 10 runs exceed 80 dB SNR, with the best of the runs resulting in about 85 dB. The randomness in the population and the search direction choices in EPT contributes to the variation in the EPT results. This demonstrates successful system synthesis, and sets the stage for the system-circuit interface.

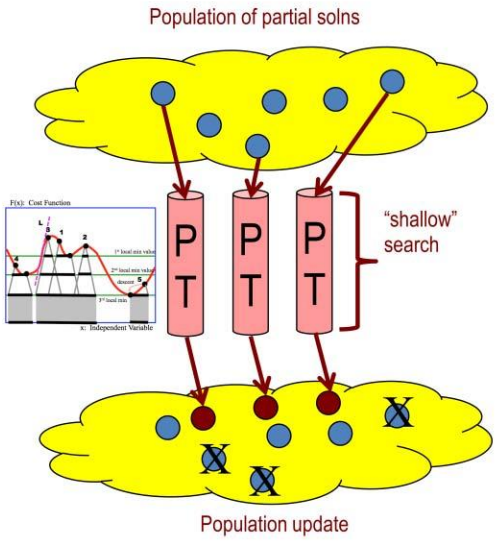


Figure 1: Evolutionary Pijavsky Tunneling Framework.

To link more accurately model the op-amp within EPTl, we use Pareto optimal fronts. Pareto fronts capture the boundary, in the objective performance space, of the best possible designs. Extracting Pareto fronts have been done with an evolutionary/genetic search and with deterministic search approaches in the past. In this work we've tried both approaches, but favor the deterministic approaches, called Normal Boundary Intersection (NBI) as they are the most straightforward to implement in today's synthesis tools. NBI requires the lowest feasible designs in each performance direction, draws a chord between them, and searches normal to the chord to find the Pareto points. In our approach EPT runs provides the lowest feasible design points. A 3D Pareto surface of the gain, bandwidth and power performance metrics were extracted from a Cadence NeoCircuit run on an op-amp, after the initial boundary points were obtained with multiple EPT runs. This Pareto model was then added as a new constraint in the EPT formulation, for course-grid optimization. The best design point from this stage was used for fine-grid optimization by tunneling in each design dimension within a ±10% range

Keywords: optimization, synthesis, Pijavskij, Pareto

INDUSTRY INTERACTIONS

Freescale, Texas Instruments, IB

TASK ID# 1836.017, PERFORMANCE-ORIENTED DVS-COMPATIBLE SINGLE-INDUCTOR MULTIPLE-OUTPUT POWER CONVERTERS

DONGSHENG MA, THE UNIVERSITY OF ARIZONA, dma@email.arizona.edu

SIGNIFICANCE AND OBJECTIVES

Advanced power management techniques are urgently required due to the exponentially increasing power dissipation in modern VLSI systems. The objective of this project is to develop a DVS-compatible single-inductor multiple-output (SIMO) power converter with improved cross regulation, line/load transient response and on-chip supply switching noise.

TECHNICAL APPROACH

To avoid cross regulation and minimize the response time, power demands from all loads should be instantly monitored and accurately measured. An on-line CMOS power meter is developed based on on-line current and voltage sensing techniques to accurately measure the instantaneous static and dynamic power of the whole system. A digital multi-mode control scheme is also proposed to dynamically change the switching actions of power devices according to different load conditions, leading to low switching noise. Moreover, an adaptive global/local power allocation technique is proposed to minimize duty-ratio errors and maintain optimal regulation at different operation scenarios.

SUMMARY OF RESULTS

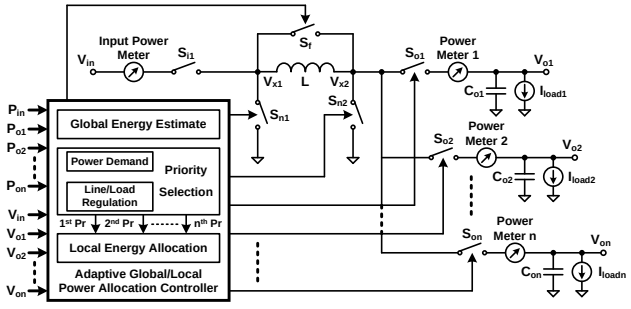


Figure 1: System architecture of the proposed SIMO converter with on-line CMOS power meter.

The architecture of the proposed SIMO converter with on-line power meter is shown in Figure 1. By accurately monitoring the power demand of each sub-converter, the global power can be estimated and allocated accordingly, thereby minimizing duty-ratio errors which cause cross regulation. Moreover, the operation scheme is dynamically controlled based on the instantaneous load conditions. As illustrated in Figure 2, the inductor is charged once (Fig. 2(a)) or multiple times (Fig. 2(b)) in each switching cycle, in light or heavy load conditions. The power delivery to certain sub-converter can also be skipped in unbalanced load condition (Fig. 2(c)) or enhanced by auxiliary power source in load transient scenario (Fig. 2(d)).

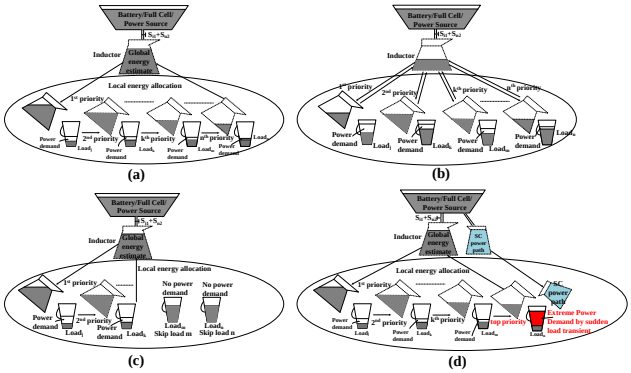


Figure 2: Adaptive global/local power allocation at different regulation scenarios.

The future work involves the design of a SIMO converter with an auxiliary path to accelerate the load transient response. Paralleled with the SIMO converter, the auxiliary path provides an instantaneous current to satisfy the sudden load increase, thereby significantly improving the load transient response.

Keywords: dynamic voltage scaling, global/local power allocation, multi-mode control, on-line power meter, single-inductor multiple-output (SIMO) converter.

INDUSTRY INTERACTIONS

Texas Instruments, Intel.

MAJOR PAPERS/PATENTS

[1] Y. Zhang, et al., *IEEE ECCE,* Sept. 2010.

[2] Y. Zhang, et al., *ASP JOLPE*, (submitted on Jul. 2010).

[3] F. Luo, et al., *IEEE TIE*, pp. 2151-2160, June 2010.

[4] C. Zheng, et al., *IEEE JSSC*, (submitted on Jun. 2010)

[5] R. Bondade, et al., *IEEE ISCAS,* pp. 617-620. May 2010.

[6] D. Ma, et al., *ICS Magazine,* pp. 14-30. Mar. 2010.

[7] Y. Zhang, et al., *IEEE APEC*, pp. 204-208, Feb. 2010.

[8] C. Zheng, et al., *IEEE ISSCC*, pp. 204-205, Feb. 2010.

[9] R. Bondade, et al., *ACM TODAES,* (submitted on Feb. 2010).

[10] F. Luo, et al., *IEEE ISLPED*, pp. 319-322, Aug. 2009.

TASK ID# 1836.018, TRANSISTOR SIZING AND VOLTAGE SCALING FOR MINIMAL ENERGY AT FIXED PERFORMANCE

VOJIN G. OKLOBDZIJA, UNIVERSITY OF TEXAS AT DALLAS, vojin@acsel-lab.com
PORAS T. BALSARA, UNIVERSITY OF TEXAS AT DALLAS

SIGNIFICANCE AND OBJECTIVES

This task will create enabling technologies for developing low-power digital systems, from fully customized to synthesized designs, in three key areas: design methodology for minimum energy system optimization, low-power building blocks, and low-power standard cell libraries.

TECHNICAL APPROACH

In this task, we aim to use power as the primary constraint on digital system design, and to develop methodology for designing digital systems and the key enabling technologies of the lowest-power basic building blocks and standard cell libraries. The methodology will provide design parameters (voltage, thresholds and transistor sizing) resulting in minimal power consumption without a performance penalty. By balancing design time and validation complexity with energy-efficient circuit optimization, considerable improvements in power and performance are expected.

SUMMARY OF RESULTS

The developed energy-efficient design techniques are applied to high-performance adders and multipliers that are the basic building blocks in many applications. By taking advantage of possible energy-delay trade-offs on various levels; algorithm, recurrence, wire delay and energy, circuit sizing and circuit topology, we developed 64-bit adder *(EZO-S2)* which operates at the highest achievable speed using up to order of magnitude less energy over leading CMOS implementations (Figure 1). We also generated the energy-delay characteristics of proposed and existing adders across all technology nodes. The results showed that the given methodologies lead to best design at all technology nodes.

Using developed sizing method, Booth and Non-Booth multipliers are comparatively analyzed in energy and delay space. Non-Booth multiplier is found to be 10% faster than Booth multiplier at the same energy budget. To improve the energy efficiency of the multipliers, novel 3:2 and 4:2 compressors are developed. We were able to reduce the energy consumption by 20% at same speed by employing the improved compressors.

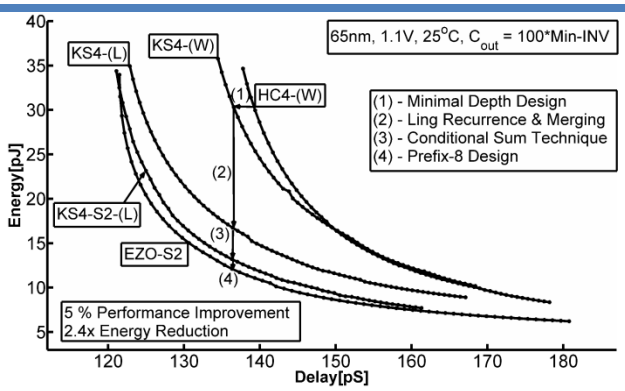


Figure 1: Comparison of Representative 64-bit Compound Domino CMOS Adders at 65nm Technology. By exploring energy-delay trade-offs in algorithm, recurrence, wiring, and circuit topology resulted in the most energy efficient 64-bit adder (EZO-S2).

Another accomplishment is the development of a quick circuit sizing method to explore the energy-delay space. The method is able to size digital circuits for minimum energy under a delay constraint. The method is evaluated on adder circuits in 65nm CMOS technology in terms of sizing accuracy and runtime. In comparison with the convex optimization based optimal method, proposed method has 300x runtime improvement for a circuit with 2000 gates with a sizing accuracy within 10% of optimal solution-. The method is able to reflect architectural trade-offs in functional units enabling quick selection for the optimum architecture.

Keywords: Energy-Efficient Design, Energy-Delay Estimation, Circuit Sizing, Arithmetic and Logic Structures

INDUSTRY INTERACTIONS

Intel, IBM

MAJOR PAPERS/PATENTS

[1] Zeydel et al., "Energy-Efficient Design Methodologies: High-Performance VLSI Adders," Solid-State Circuits, IEEE Journal of , vol.45, no.6, pp.1220-1233, June 2010.

[2] Baran et al., “Energy Efficient Implementation of Parallel CMOS Multipliers with Improved Compressors,” ISLPED 2010, Austin, TX, USA, 18-20 August 2010.

[3] Aktan et al., “A Quick Method for Energy Optimized Gate Sizing of Digital Circuits,” PATMOS 2010, Grenoble, France, 7-10 September 2010.

TASK ID# 1836.019, DIGITALLY ENHANCED ENERGY-EFFICIENT HIGH-SPEED I/O LINKS

NARESH SHANBHAG, UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN shanbhag@illinois.edu
ELYSE ROSENBAUM, UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN

SIGNIFICANCE AND OBJECTIVES

Design of high-speed and low-power analog mixed-signal circuits in nanoscale CMOS is made challenging due to a number of issues such as reduced supply voltage. These problems are exemplified in multi-Gb/s I/O links, whose prevalence in modern electronic systems motivates us to seek cost-effective solutions.

TECHNICAL APPROACH

The goal of this project is to exploit the capability of DSP and ECC to reduce power in high-speed I/O links. I/O link specific ECC will be explored in terms of BER, latency, encoder and decoder architectures. BER-optimal rather than SFDR-optimal ADC architectures will be developed. Ultra low-power DSP techniques such as algorithmic noise-tolerance will be employed to design low-power I/O link equalizers. System-level techniques will be developed to power-optimally budget ECC coding and ADC shaping gains across the power-hungry blocks in the link. An ESD-protected multi-Gb/s I/O link embodying some of these ideas will be implemented.

SUMMARY OF RESULTS

We have shown [1] via system optimization that short (block length = 63-to-255) BCH codes in a 20-in FR4 link carrying 10-Gb/s data results in: 1) an 18-mW/Gb/s savings in the ADC; 2) a 1-mW/Gb/s reduction in transmit driver power; 3) up to 6× improvement intransmit jitter tolerance; and 4) a 25- to 40-mV improvement in comparator offset tolerance with 3× smaller swing. These results indicate that ECC is effective in designing robust, low-power high-speed I/O links.

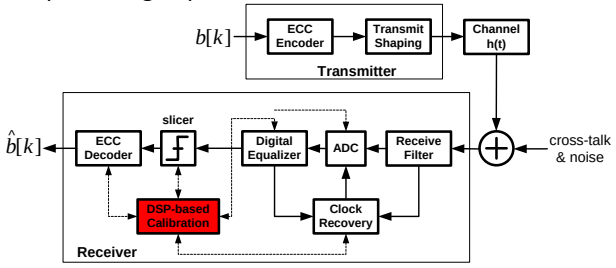


Figure 1: Overview of a systems-aware mixed-signal high-speed I/O link.

For ECC-based links with a DFE, we have shown that for a fixed code-rate: 1) the BER of a random error correcting code reduces monotonically with block-length, 2) there exists a BER-optimum block-length for a burst error-correcting code. This work clearly shows the interplay between equalization and ECC. For ADC-based high-speed I/O links, we have shown [3] that a BER-aware ADC, where the ADC reference levels are chosen based on channel output statistics, provides the following advantages in a 20-in FR4 link carrying 10-Gb/s data: 1) the ADC shaping gain is > 30dB at a BER=10^{-15} for a 3-b ADC, and 2) a 3-b BER optimal ADC gives 6 orders-of-magnitude reduction in BER over a 4-b conventional ADC at an SNR of 32 dB. This corresponds to a shaping gain of 3dB at a BER=10^{-15}, and a power savings of 50% in the ADC.

A receiver test chip was designed in a low-power 90-nm CMOS technology to demonstrate a g_m-boosted negative capacitance circuit for input port bandwidth extension. The g_m-boosted circuit leverages the inherent gain of the receive amplifier to improve the circuit's ability to negate the capacitive parastics at the input port of the receiver.

Our next year plans include: 1) report the test results of an ECC-based 6 Gb/s low-power transceiver, 1) implement a 4-b BER-aware ADC for a 4 Gb/s I/O link in a 90nm CMOS process, and demonstrate its benefits via measured results, 2) develop additional BER-aware ADC topologies including time-interleaved ones, and 3) explore integrated ADC-equalizer receiver architectures.

Keywords: high-speed I/O, DSP, ESD, ECC, low-power

INDUSTRY INTERACTIONS

Texas Instruments, Intel, AMD, IBM

MAJOR PAPERS/PATENTS

[1]R. Narasimha, and N. R. Shanbhag, "Design of energy-efficient high-speed links via forward error-correction (FEC)," IEEE TCAS-II, May 2010.

[2]R. L. Narasimha, N. Warke, and N. Shanbhag, "Impact of DFE Error Propagation in FEC-based high-speed I/O links," GLOBECOM, 2009.

[3]R. Narasimha, N. R. Shanbhag, and A. C. Singer, "BER-aware adaptive ADC-equalizer receiver for communication links," IEEE SiPS 2010.

TASK ID# 1836.020, LOW-COMPLEXITY HIGH PERFORMANCE ANALOG-TO-DIGITAL CONVERTERS IN SUBMICRON CMOS

UN-KU MOON, OREGON STATE UNIVERSITY, moon@eecs.oregonstate.edu

SIGNIFICANCE AND OBJECTIVES

The reduced supply and intrinsic gain prevalent in submicron CMOS technologies limit the achieved performance in analog-to-digital converters in those technologies. The techniques presented in this summary offer ways to obtain increased signal swing, lower design cost and higher effective op-amp gain while maintaining low power operation and small area.

TECHNICAL APPROACH

The power- and area-saving techniques are implemented in three separate prototype ICs. The first prototype is a single-loop ΔΣ ADC that employs an auxiliary quantizer to process the quantization error of the main quantizer. This allows the loop to process larger input signals, and thus increases SQNR [1]. The second uses cascade of digital-like domino logic cells whose propagation delay is input signal dependent to realize a compact ADC whose digital code is a count of triggered cells, and is amenable to synthesis. Finally, an improved CLS technique allows the use of simple low-gain op-amps in a low power ADC.

SUMMARY OF RESULTS

The extended dynamic range technique is used to design a 3rd order modulator in 0.18μm CMOS. The design uses a 3-level main quantizer, a 9-level auxiliary quantizer and 30dB open-loop opamp gain. Measurement results included in Fig. 1 shows that at 1.2V power supply and reference, the input signal can go over +5dBFS without any stability issues, achieving 75dB SNDR and 77.2dB dynamic range at OSR of 16.

The domino logic cell shown in Fig. 2 is cascaded to design an all-digital pseudo-differential ADC in 0.18μm CMOS. The test chip achieves over 5.4b ENOB up 50MS/s at 1.3V supply. The domino cell was implemented as a digital cell with supply pitch matching that of the standard cell library to allow synthesis.

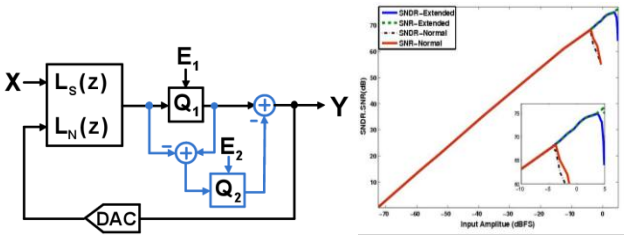


Figure 1: The extended dynamic range ΔΣ ADC & DR plot.

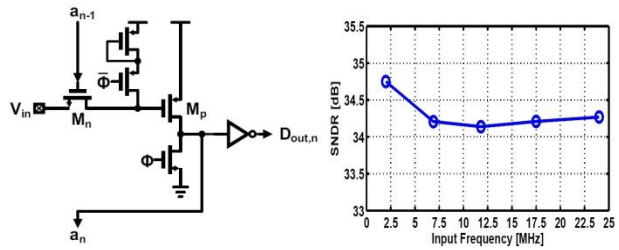


Figure 2: A single "domino" cell and the SNDR plot of the ADC.

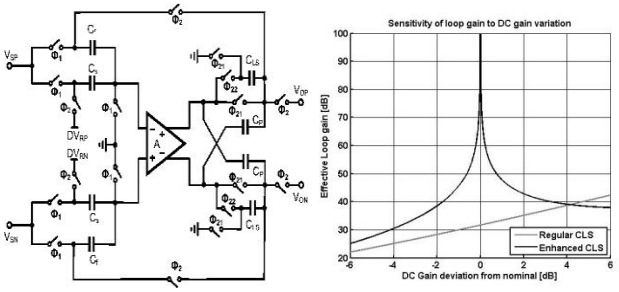


Figure 3: The improved CLS MDAC and its effective loop gain.

The improved CLS is used to design a 10bit pipelined ADC with four 2.5bit stages and a 2bit flash. Each of the MDACs uses a simple single-stage op-amp with 32dB open-loop gain. The ADC is expected to achieve an SNDR of 54dB SFDR of about 70dB while consuming 6.0mW from a 1.2V supply.

Table 1: Performance Summary

	VDD	ENOB	BW	Power	Area
Chip 1	1.2V	12.2b	2.5MHz	4.9mW	.85mm^2
Chip 2	1.3V	5.4b	25MHz	.43mW	.094mm^2
Chip 3	1.2V	9.0b	20MHz	6.0mW	1.0mm^2

From Table 1, all the test chips achieve low power wide-band operation at low supply voltages. Higher energy efficiency could be achieved by further optimization.

Keywords: extended dynamic range, domino logic, correlated level shifting, synthesizable

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] N. Maghari *et al.*, "A +5dbFS Third-Order Extended Dynamic Range Single-Loop ΔΣ Modulator," (Accepted) 2010 CICC.

TASK ID# 1836.021, CAD ALGORITHMS AND TOOLS FOR FAST AND ACCURATE PLL DESIGN IN THE PRESENCE OF VARIABILITY

JAIJEET ROYCHOWDHURY, UC BERKELEY, jr@berkeley.edu

SIGNIFICANCE AND OBJECTIVES

PLLs and SRAMs suffer disproportionately from several difficult-to-debug post-fabrication issues. Their functionality/performance problems often critically limit overall system function and time to market. We have been developing novel simulation methods (variability-enabled macromodelling and nonstationary noise analysis) to help close the gap to first-pass-correct design of these systems.

TECHNICAL APPROACH

We have been attacking the PLL/SRAM variability and noise simulation problem with three research prongs:

1) variability-enabled nonlinear phase macromodelling (for PLLs). Our technique incorporates parameter variability into nonlinear time-shifted PPV macromodels of oscillators and establishes efficient computational and analytical methods for using these variability-aware macromodels
2) non-Monte-Carlo yield analysis (for PLLs and SRAMs). Our methods find success/failure boundaries in parameter space quickly and adaptively
3) fully nonstationary accounting of Random Telegraph Noise (RTS) (for SRAMs and PLLs). Our RTS simulation technique accounts correctly for changing trap firing statistics due to varying gate bias using Markov uniformisation.

SUMMARY OF RESULTS

Our work on variability-enabled PLL macromodels and non-Monte-Carlo yield analysis has been covered in previous reports.

Random Telegraph Signal (RTS) noise is a major performance detractor in PLLs and SRAMs. Over the last year, we have been developing algorithms and CAD tools that enable (a) accurate prediction of RTS-induced transient failures in PLLs/SRAMs, and (b) accurate characterization/compact-modeling of non-stationary large-signal modulated RTS for RF circuits.

We model RTS at the trap level using non-stationary Markov chains with bias-dependent (i.e, time-varying) propensities. So far, this model has been simulated via a Monte-Carlo technique called Markov Uniformisation, which exactly preserves the stochastic properties of non-stationary trap activity, yielding accurate time-domain RTS traces. This enables us to obtain RTS characterizations for arbitrary bias conditions. We have validated our method by showing excellent agreement with analytically known results.

Over the next year, our plan is to devise and validate techniques for co-simulation of RTS noise with nonlinear circuits, in particular SRAMs and PLLs.

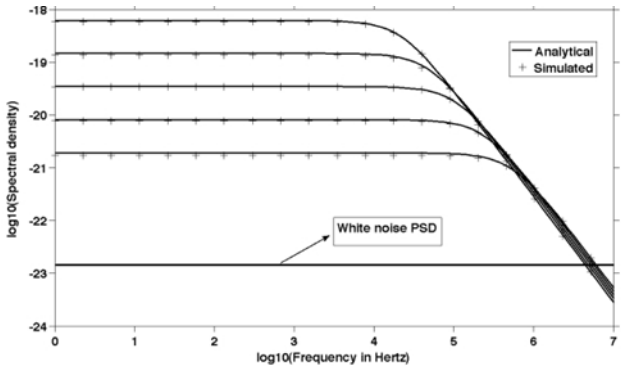


Figure 1: RTS noise: comparison of simulated vs analytical spectra for a DC swept gate voltage

Keywords: PLL, SRAM, variability, yield, Random Telegraph Noise, jitter, read-access-time, write-access-time.

INDUSTRY INTERACTIONS

Intel; IBM; Freescale; TI; AMD; Cadence

MAJOR PAPERS/PATENTS

1. (**invited book chapter**) C. Gu, J. Roychowdhury, "Computing Probabilistic Hypervolumes", in *Extreme Statistics in Nanoscale Memory Design*, Springer, 2010.
2. (**best paper**) C. Gu and J. Roychowdhury, "An Efficient, Fully [...]", Proc. ASPDAC, 2008.
3. Z. Wang and J. Roychowdhury, "Obtaining Frequency Sensitivities [...]", Proc. CICC, 2007.
4. S. Srivastava andJ. Roychowdhury, "Rapid Estimation of [SRAM failure]", Proc. CICC, 2007.

TASK ID# 1836.022, "HIGH-SPEED MIMO SIGNALING TECHNIQUES FOR SINGLE-ENDED PARALLEL I/O"

RAMESH HARJANI, UNIVERSITY OF MINNESOTA, harjani@umn.edu

SIGNIFICANCE AND OBJECTIVES

Processor-memory I/O bandwidth is often the performance bottleneck in high-performance computing. The goal of the task is to develop efficient MIMO techniques to improve multi-Gbps NRZ signaling by reducing crosstalk noise. This allows serial links to be placed closer together while operating at higher speeds for a higher data throughput within a given board area.

TECHNICAL APPROACH

Chip-to-chip I/O signaling has relatively time-invariant channels where simplified MIMO techniques can be used. The parallel decomposition of the MIMO channels can be obtained by manipulating the channel input and output using transmit precoding and receiver shaping. New I/O architectures will be explored. Considerations for low-power implementations and performance/complexity tradeoffs will be analyzed.

SUMMARY OF RESULTS

The technique not only cancels the cross-talk energy from adjacent lines but reutilizes the crosstalk energy that had been transferred to the adjacent line to increase SNR.

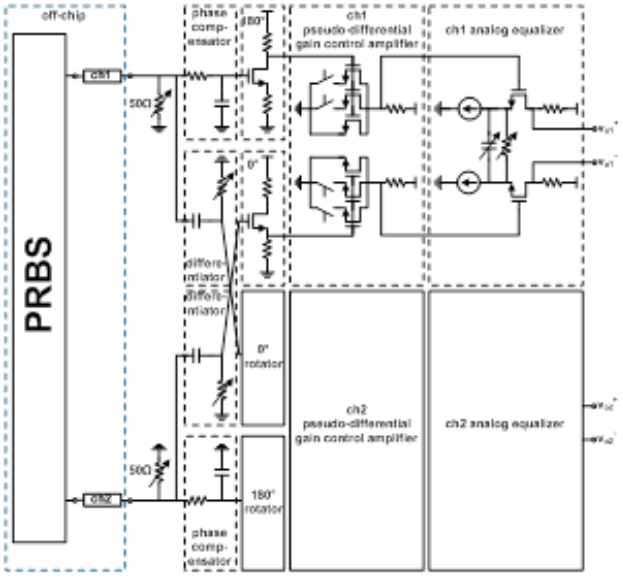


Figure 1: Low power and low complexity implementation of MIMO algorithm

After transmitting 5Gb/s NRZ signals, $X_1(\omega)$, $X_2(\omega)$ into the far-end crosstalk (FEXT) channels, the adjacent received signal output, $Y_2(\omega)$, is differentiated ($j\omega$) and added to the current channel signal, $Y_1(\omega)$, with the appropriate gain (β). $Z_1(\omega)$ and $Z_1(\omega)$ are the equalized signals. If β is matched to τ_F, the FEXT signal is canceled, zeroing out of the non-diagonal terms in the matrix.

$$\begin{bmatrix} Y_1(\omega) \\ Y_2(\omega) \end{bmatrix} = \begin{bmatrix} H(\omega) & -j\omega\tau_F H(\omega) \\ -j\omega\tau_F H(\omega) & H(\omega) \end{bmatrix} \begin{bmatrix} X_1(\omega) \\ X_2(\omega) \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} Z_1(\omega) \\ Z_2(\omega) \end{bmatrix} = \begin{bmatrix} 1 & j\omega\beta \\ j\omega\beta & 1 \end{bmatrix} \begin{bmatrix} Y_1(\omega) \\ Y_2(\omega) \end{bmatrix} = \begin{bmatrix} (1+\beta\tau_F\omega^2)H(\omega) & j\omega(\beta-\tau_F)H(\omega) \\ j\omega(\beta-\tau_F)H(\omega) & (1+\beta\tau_F\omega^2)H(\omega) \end{bmatrix} \begin{bmatrix} X_1(\omega) \\ X_2(\omega) \end{bmatrix}$$

$$= \begin{bmatrix} (1+\tau_F^2\omega^2)H(\omega) & 0 \\ 0 & (1+\tau_F^2\omega^2)H(\omega) \end{bmatrix} \begin{bmatrix} X_1(\omega) \\ X_2(\omega) \end{bmatrix} \quad \text{if } \beta = \tau_F \quad (2)$$

The diagonal values have an additional term $\tau_F^2\omega^2$. This second derivative of the signal boosts high frequency gain by τ_F^2 and reduces channel ISI.

A prototype circuit that implements the MIMO algorithm as suggested in Fig. 1 using passive differentiators, 180◦ phase rotators, wide-band variable gain amplifiers and analog equalizers. 16" FR4 lines with 240mil and 120mil spacing, corresponding to 2× and 1× channel widths, were used to demonstrate the circuit's dynamic range on various FEXT gains. The measurement results are summarized in the below table.

Table 1: Measurement results

Data Rate (Gb/s)	Line Spacing (mil)	$Jitter_{pp}$ (ps)	Vertical Eye (mV/mV)	$Jitter_{pp}$ /eye-improve
5	240 (2W)	81/40.2%UI 54/27%UI	314/815 38.5% 223/447 49.9%	13.2%↓ /11.4%↑
5	120 (1W)	170/85%UI 36/18%UI	60/821 7.3% 306/467 65.5%	67%↓ /58.2%↑

In the following year, a crosstalk cancellation solution for four-lanes will be accomplished. In the multi-lane design, the crosstalk from two independent adjacent channels should be utilized at the same time.

Keywords: MIMO XTC, Continuous-time XTC, Far-end crosstalk (FEXT), ISI, Equalization

INDUSTRY INTERACTIONS

Intel and AMD

MAJOR PAPERS/PATENTS

[1] T. Oh and R. Harjani, "A 5Gb/s 2x2 MIMO Crosstalk Cancellation Scheme for High-Speed I/Os," 2010 CICC.

[2] M. R. Ahmadi and R. Harjani, IEEE Custom Integrated Circuits Conference, Sept 2009.

[3] T. Oh and R. Harjani, "Continuous-time 2x2 MIMO Crosstalk Cancellation Architecture for High-speed I/O," IP disclosure

TASK ID# 1836.023, FAST ALGORITHMS FOR SPICE-LEVEL SIMULATION OF LARGE STRUCTURED CIRCUITS

JAIJEET ROYCHOWDHURY, UC BERKELEY, jr@berkeley.edu

SIGNIFICANCE AND OBJECTIVES

Increasing simulation speed while retaining SPICE-level accuracy is a top priority in analog, mixed-signal, RF and high-speed design. This project aims to set up an open and public base of fast algorithms that SRC companies can take advantage of within their internal simulators.

TECHNICAL APPROACH

Our approach uses structured nonlinear differential equation formulations capable of representing hierarchy. This feature (the HDAE) is crucial for enabling a slew of fast simulation approaches that can exploit hierarchy and isomorphism for improved speed. HDAEs enable general and convenient use of the multilevel Newton-Raphson algorithm, which confers benefits in terms of memory/cache usage and convergence robustness. Different analyses (including hierarchical DC, transient and harmonic balance) benefit from HDAE-based multilevel Newton-Raphson. Our HDAE-based framework constitutes an open core using which SRC companies can explore different fast simulation techniques. Existing fast simulation engines, such as HSIM and nanosim, are highly proprietary.

SUMMARY OF RESULTS

Technical accomplishments: We have developed and prototyped the hierarchical DAE formulation core for enabling multilevel algorithms. The HDAE core has been used to enable multilevel DC, AC, transient and harmonic balance analyses. The net impact of HDAE-enabled multilevel algorithms is lower memory usage and more robust convergence, with related speed improvements. Table 1 provides a summary of performances.

Number of stages	Simulation Time (s)		Memory Usage (MB)	
	Flattened	Multilevel	Flattened	Multilevel
5	3.06	5.95	0.0451	0.101
10	7.47	6.04	0.209	0.294
15	21.6	13.9	1.78	1.35
25	245	25.9	65.1	6.24
30	N/A	72.1	N/A	15.5

Table 1: Flat vs HDAE hierarchical: performance

The HDAE-enabled multilevel algorithms were validated on several example circuits, including: cross-coupled LC digitally-controlled voltage-controlled oscillator; a flash ADC; and chains of inverters. The techniques were also validated on a new device model for carbon nanotube FETs (CNFETs) developed by Philip Wong (Stanford). The CNFET model involves a large number of internal nodes and variables (30 for the N-type, 38 for P-type) which makes it well suited to benefit from hierarchical/multilevel simulation techniques.

Constrained funding for this project (a total of $100K over 3 years) precluded exploration of isomorphism-related directions for speed-up and open-source release. However, the PI remains committed to this important direction and intends to continue making further progress.

Student training: Three students have been trained as part of this project: Bin Cheng and Xiaolue Lai (both graduated from the University of Minnesota) and Michael Lorek (first-year student at UC Berkeley).

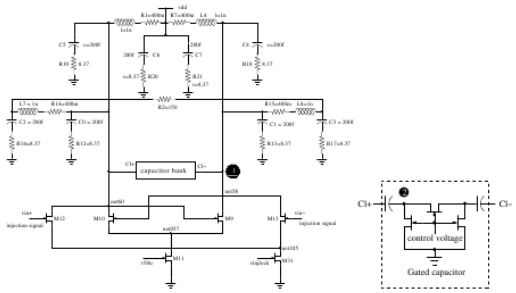


Figure 1: Cross-coupled LC DCO with capacitor bank.

Keywords: fast simulation, hierarchical DAE, ADC, VCO

INDUSTRY INTERACTIONS

Texas Instruments, Intel, AMD, Freescale

MAJOR PAPERS/PATENTS

[1] B. Cheng and J. Roychowdhury, "A General Formulation for Hierarchical Multilevel Simulation", Technical Report, University of Minnesota.

TASK ID# 1836.024, REINVENTING MIMO FOR HIGH-BANDWIDTH COMMUNICATION IN INTERFERENCE LIMITED CELLULAR SYSTEMS

ROBERT W. HEATH JR. THE UNIVERSITY OF TEXAS AT AUSTIN, rheath@ece.utexas.edu

SIGNIFICANCE AND OBJECTIVES

The research deals broadly with discovering the practical implications of limited feedback MIMO (multiple-input-multiple-output), in interference limited cellular systems. Throughput and outage performance limits are derived along with rate adaptation algorithms for approaching those limits. Both uncoordinated other-cell interference and ad-hoc cross-tier interference are considered.

TECHNICAL APPROACH

The research deals broadly with performance limits and practical algorithms for interference limited cellular systems with multiple antenna-equipped subscribers. Goodput is used to capture the mismatch in channel state information between the subscribers and the base station for limited feedback beamforming, with extensions to cross-tier interference. Interference nulling strategies are proposed to mitigate the effect of interference while rate backoff is analyzed to improve channel state mismatch robustness. Performance tradeoffs are also derived in terms of range and density of femtocells. The analyses provide design insights for next generation cellular networks.

SUMMARY OF RESULTS

Uncoordinated other cell interference and feedback delay cause a mismatch in channel state information between the transmitter and the receiver. This mismatch leads to a packet outage. By only considering the fraction of successful transmissions over the channel – goodput – we show that the gain in ergodic achievable rate from having delayed feedback decreases exponentially with the feedback delay. This exponential rate of decay doubles in the presence of other cell interference, when compared to noise-limited scenarios, for low to moderate delay values. This analysis was carried out for both limited feedback beamforming and precoded spatial multiplexing. The analysis also proves that the decay rate of the goodput decreases when the codebook quantization size increases and the Doppler shift in the temporally correlated channel decreases. Zero forcing (ZF) interference nulling at the mobile station restores the decay rate of the closed loop MIMO throughput gain at the expense of a rate loss due to the projection power loss of the ZF receiver.

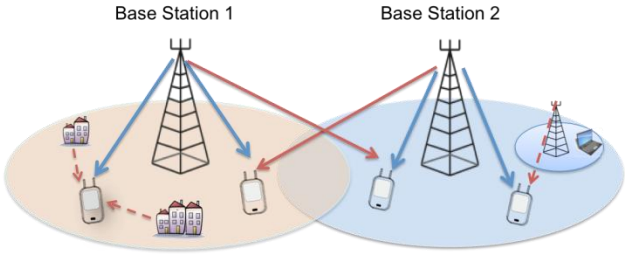


Figure 1: Limited feedback MIMO for interference limited cellular systems subject to both other cell and cross-tier interference

Heterogeneous cellular networks, which employ femtocells to increase spatial reuse, also introduce additional sources of interference. The analysis is extended to account for cross-tier interference from femtocells. Closed form expressions for the probability of outage and the maximum femtocell contention density are derived as a function of the distance from the receiver to the base station, the Doppler shift in the channel and the feedback delay. Rate adaptation through rate backoff optimization to maximize the ergodic goodput is proposed, and is shown to combat the effects of interference. It is shown that rate backoff doubles the goodput achieved by the limited feedback system.

Keywords: MIMO, limited feedback, cellular systems, interference, feedback delay, femtocells, rate backoff, goodput.

INDUSTRY INTERACTIONS

Texas Instruments.

MAJOR PAPERS/PATENTS

[1] S. Akoum, R. W. Heath, Jr. “Limited feedback for temporally correlated MIMO channels with other cell interference” (accepted) *IEEE Trans. Signal Processing*, October 2010.

[2] S. Akoum, R. W. Heath, Jr. “Limited feedback beamforming for temporally correlated MIMO channels with other cell interference” *Proc. of IEEE Int. Conf. on Acoustics, Speech and Signal Process.*, March 2010.

[3] S. Akoum, R.W. Heath, Jr., “Rate adaptation for goodput maximization on the downlink of a two-tier network,” to be submitted to *IEEE Trans. Wireless Comm.*, August 2010.

TASK ID# 1836.026, AUTOMATIC RF IMPEDANCE CORRECTION CIRCUITS FOR SOC RF/MIXED SIGNAL ATE TEST

WILLIAM R EISENSTADT, UNIVERSITY OF FLORIDA, wre@tec.ufl.edu

SIGNIFICANCE AND OBJECTIVES

This research program develops, in collaboration with University of Arizona, a compact Automatic Match Control (AMC) circuit that dynamically sets the bandwidth or the impedance match of RF ports of a socketed DUT under ATE-based test.

TECHNICAL APPROACH

The AMC closed-loop control system was developed as part of the impedance estimation and multistate reflectometers system in 2008. The impedance estimation and control algorithms have been developed in early 2009 and the fabrication and usage of the prototype AMC control system the second half of 2009. Recently, this system has been used to evaluate the new meta-material compact AMC circuits developed at the University of Arizona as reported in the 2009 Annual review presentation and novel on-chip solutions for impedance and bandwidth control are under fabrication.

SUMMARY OF RESULTS

The published results include the impedance control and work shown below.

Impedance matching is an important factor that impairs radio frequency (RF) test and antenna efficiency. An AMC system is introduced to adaptively correct the device under test (DUT) impedance mismatch. The matching control system consists of a five-stub microstrip filter and three varactors. It employs a greedy algorithm to determine the varactor bias for impedance matching. Our experimental results demonstrate the feasibility of the automatic matching control circuit over a frequency range of 2.5 to 4.5 GHz.

As shown in Fig. 1, the proposed automatic matching control system which consists of a reconfigurable tuner, a network analyzer, a host computer, and a microcontroller. In the current implementation, the tuner is directly connected to the network analyzer. Various antenna mismatches were simulated by an automatic load-pull system. The automatic matching is performed by a closed-loop feedback operation as follows. First, the network analyzer measures the reflected signal (S_{11} parameter).

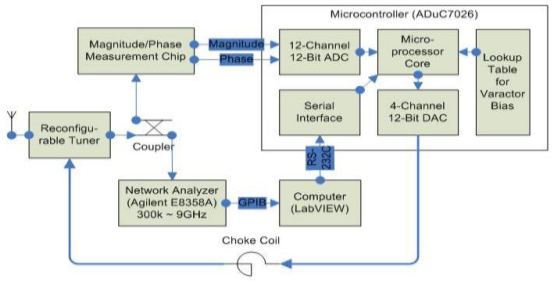


Figure 1: Automatic Match Control System Diagram

Second, the host computer calculates the available bandwidth. Last, the algorithm searches for the varactor bias for broadband impedance match and the microcontroller sets the varactor bias. The above procedures are repeated until the algorithm search converges to the optimal bias.

The measurement results showed that the greedy search algorithm could find the optimal bias for the matching tuner, but the matching tuner did not show the good tunability against large mismatches, $|\Gamma| > 0.14$. Currently we are working on improving the tuner's tunability against large mismatch.

Keywords: RF test, microwave matching, mixed-signal test, wireless test

INDUSTRY INTERACTIONS

Freescale, Intel.

MAJOR PAPERS/PATENTS

[1] J. Kim, "Automated Matching Control System Using Load Estimation and Microwave Characterization," Univ. of FL, Ph.D. Dissertation, 1-Dec-2008; (Pub P050421).

[2]. Coupler and Coupler-Free Load Estimation Methods for Automatic Impedance Matching; J. Kim, and W. Eisenstadt; 20-Nov-2008; (Pub P050403);

[3]. Automatic Matching Control System for Loadboard Test; J. Kim et.al., 6-Mar-2008; (SRC Pub P024320); Univ. of FL; WTW'2008, San Diego, CA., April 27, 2008, 4 pages.

[4]. J. Kim, et. al., "Automatic Matching Control System for Loadboard Test," 7-May-2008; (SRC Pub P023108);

[5]. "Load Impedance Estimation for Automatic Impedance Matching Control Circuits; J. Kim and W. Eisenstadt," 10-Jun-2008; (SRC Pub P023491 SRC TECHCON, Austin TX, Sept 15-16 2008.

TASK ID# 1836.027, AUTOMATIC RF IMPEDANCE CORRECTION CIRCUITS FOR SOC RF/MIXED SIGNAL ATE TEST

KATHLEEN L. MELDE, UNIVERSITY OF ARIZONA, melde@ece.arizona.edu

SIGNIFICANCE AND OBJECTIVES

This research program develops, in collaboration with University of Florida, a compact Automatic Match Control (AMC) circuit that dynamically sets the bandwidth or the impedance match of RF ports of a socketed DUT under ATE-based test.

TECHNICAL APPROACH

A closed-loop AMC system was demonstrated in 2008. The AMC (or SDMC, for software-defined match control) involves an RF impedance tuner and a control block to adaptively adjust the tuner settings. The recent research has focused on creating and demonstrating a compact tuner. The new design involves using highly coupled square split ring resonators (SSRRs). The size of the SSRR tuner is 0.32 x0.44 in^2. The approach uses vertical interconnects to create the bias circuitry. Detailed RF measurements are underway.

SUMMARY OF RESULTS

The published results include methods to reduce the size of the RF tuner and work shown below. Impedance matching is an important factor that impairs radio frequency (RF) test and antenna efficiency. The SDMC is a microstrip circuit with tuning diodes that are adjusted to tune the input impedance of the antenna and to select a targeted frequency range of operation. It is both an antenna impedance tuner and tunable filter. The work in [2] discusses the design approach for the system and presents simulated and measured results. The results show that the combined antenna and SDMC can be tuned to operate at many worldwide frequency ranges even when the individual antenna (a planar inverted F antenna) is not specifically matched to the frequencies.

Fig. 1 shows a reconfigurable tuner connected to an antenna. Project 1836.026 discusses the integration of the control system and decision making algorithm. The integrated SDMC shows an excellent range of tuning to various target frequencies of operation. The results show that the integrated design can achieve good tuning performance at frequencies that are beyond the primary design frequencies of the antenna or the tuner. Many different frequency standards could be achieved in one circuit. This avoids have to package several different antennas for different standards on a single device. The SDMC can also be used for new wireless standards after the system is designed and fabricated. The SSRR is a type

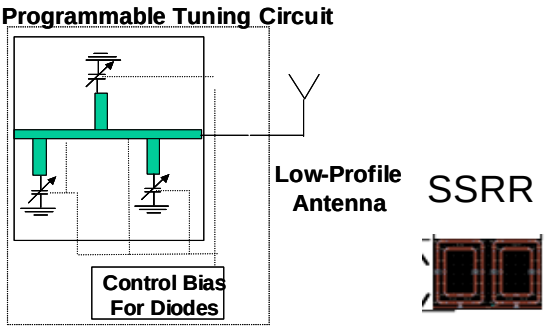


Fig. 1: Automatic Match Control Diagram and SSRR

of band pass filter that uses highly electromagnetically coupled transmission line structures with two coupled rings. The coupled rings are electrically small resonators of coupled LC elements. Varactor diodes are placed at the open ends of each coupled ring. The use of SDMCs with SSRRs requires innovative approaches in order to integrate and isolate the diode bias control circuits. This approach uses vertical interconnects are used to create the bias circuits by designing a multilayer structure with ground, square ring resonator and bias layers. Measurements of the SSRR tuner are underway.

Keywords: Reconfigurable filter, software-defined radio, multi-band antenna, tunable filter

INDUSTRY INTERACTIONS

Freescale, Intel.

MAJOR PAPERS/PATENTS

[1] H. Park, "Frequency Reconfigurable Tuner with Three Stubs Resonator and Split Ring Resonator," Univ. of AZ, M.S. Thesis, 1-Aug-2010;

[2] K. L. Melde, H-J. Park, H-S. Yeh, B. Fankem, Z. Zhou and W. R. Eisenstadt, "Software Defined Match Control Circuit Integrated with a Planar Inverted F Antenna," to appear in IEEE Trans. on Antennas and Propagation, 2010. (SRC Pub: P055283)

[3]. H-J. Park, K. L. Melde, and W. R. Eisenstadt, " Design of Compact Adaptive RF Matching Circuits using; Square Split Ring Resonators," IEEE Intl. Symposium on Antennas and Propagation Digest, Toronto, Ontario, Canda., July 11, 2010, 4 pages. (SRC Pub: P055282)

[4] H-J. Park and K. L. Melde, "Development of a Compact Varactor Loaded Tuner for Automatic Match Control," Techon, June 15, 2009 (SRC Pub: P052489)

TASK ID# 1836.028, TOOLS AND ALGORITHMS FOR BEHAVIORAL MODEL GENERATION OF ANALOG/MIXED-SIGNAL CIRCUITS

H. ALAN MANTOOTH, UNIVERSITY OF ARKANSAS, mantooth@uark.edu

SIGNIFICANCE AND OBJECTIVES

Manually creating circuit behavioral models can take a long time. This research is focused on the synthesis of models and subsequent full-chip or system verification. The objective is to develop algorithms and tools for extracting behavioral models from the circuit level for linear and switching regulators.

TECHNICAL APPROACH

The proposed approach accepts user inputs for modeling information and analyzes the circuit configurations based on the circuit netlist. Extended signal path tracing (SPT) for feed forward and feedback paths, model topology formulation (MTF) and other algorithms are utilized to build a hybrid model topology (combination of simplified circuit and tabulated models). Table extraction is applied to characterize the model to match the original circuit. The algorithms are expected to generate adaptive model topologies for different circuits and implement the model in a hardware description language (Verilog-A).

SUMMARY OF RESULTS

Phase I of this project mainly focused on modeling Low Dropout (LDO) voltage regulator circuits. Several modeling methodologies were investigated, three model topologies were proposed, and the corresponding models were tested. Among the three models, the hybrid model build upon the combination of the table-based method and circuit simplification algorithms demonstrated decent simulation improvement as compared to the original circuit, and the algorithms can be implemented automatically. Fig. 1 shows the model topology of the hybrid model (AVdd: Input Power Source, Vout: Regulated Output). On the left side bias blocks are table-based models and the right side structure including the feedback block is the extracted core circuit structure. The transient simulation waveforms of the model are shown in Fig. 2 comparing to the simulation of the original LDO circuit, and the accuracy of the model is quite well. The simulation time comparison is listed in Table 1. Using tables (Table) or piecewise linear functions (PWL) to represent the bias blocks in Fig. 1 respectively, the comparison shows that there is no big difference for the speed-up of these two expressions, and both of them can achieve 6X to 9X simulation speed improvement.

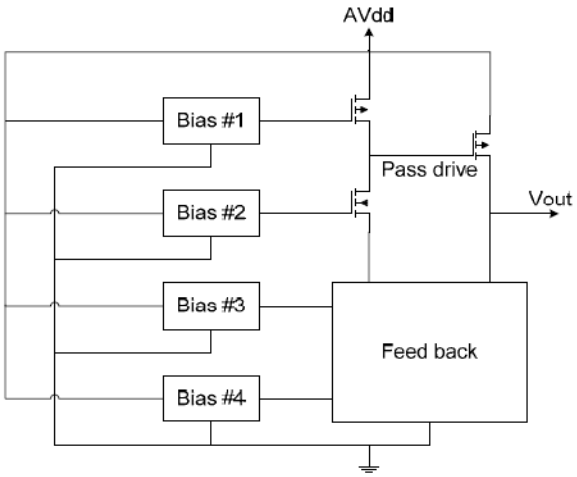


Fig. 1. Hybrid model topology for an LDO circuit.

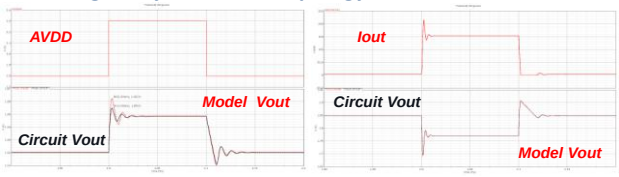


Fig. 2. Hybrid model performance (a) Line regulation, (b) Load regulation

Table 1 - DC/AC Simulation time comparison Figure (unit: sec)

Test Bench	Table	PWL	Circuit	Table Spee dup	PWL speed up
DC AVdd	30m	30m	250m	8.3	8.3
DC RLoad	30m	30m	280m	9.3	9.3
AC (1-100kHz)	20m	20m	170m	8.5	8.5
TR AVdd	220m	200m	1.17	5.3	5.9
TR RLoad	100m	90m	550m	5.5	6.1

Keywords: Model, Automation, SPT, MTF, LDO

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

In preparation

TASK ID# 1836.029, STATISTICAL ANALYSIS OF PARAMETRIC MEASUREMENTS AND ITS APPLICATIONS IN ANALOG/RF TEST

YIORGOS MAKRIS, YALE UNIVERSITY, yiorgos.makris@yale.edu
CONSULTANT: PETROS DRINEAS, RENSSELAER POLYTECHNIC INSTITUTE drinep@rpi.edu

SIGNIFICANCE AND OBJECTIVES

The key objective of this project is the development of an expert system employing advanced statistical analysis to assist in devising cost-effective strategies for analog/RF specification test compaction, measurement correlation identification, parametric failure diagnosis, yield and test quality learning, and adaptive test.

TECHNICAL APPROACH

Statistical analysis and machine learning methods, such as regression, support vector machines (SVMs) and neural classifiers (NCs), are used to analyze the parametric measurements from a statistically significant set of chips and learn correlations. Feature selection algorithms are used to select a measurement subset that carries sufficient information to address the problem at hand. Initially, these methods are demonstrated within the context of analog/RF specification test compaction. Other relevant applications include identification of trends across RF and DC measurements, yield analysis, and exploration of the test quality vs. cost trade-off through guard-banding. Ultimately, these methods will be enhanced to account for process variations.

SUMMARY OF RESULTS

Within the area of classification-based specification test compaction, our work has taken several directions. In [1], we developed techniques for improving prediction of device pass/fail labels by introducing guard-bands in regions of the performance hyperspace where prediction accuracy is uncertain. Thus, we can tag misclassification suspect devices for retest under the full specification test suite to improve overall test accuracy. In [2] we addressed a more challenging problem by limiting the retained performances to only non-RF performances. By making this reduction, cost is dramatically decreased. We approached this problem using an Ontogenic Neural Network (ONN) classifier in conjunction with a Genetic Algorithm (GA). Additionally, we devised a cost model to evaluate the relationship between test cost and quality.

In [3, 4] we investigated correlation-based specification test compaction. Using MARS, a multivariate regression algorithm, we leverage correlations existing in analog test data to predict untested RF performances from a retained set of low-cost non-RF performances. While this process is well-understood, our work developed a guard-banding technique for improving prediction accuracy. This "confidence estimation" technique employs an SVM to learn regions of prediction uncertainty and associate guard-bands with those regions, in order to explore the cost trade-off between number of retested devices and test quality. A comparison to the prior art methods of defect filtering and guard banding is shown in Figure 1.

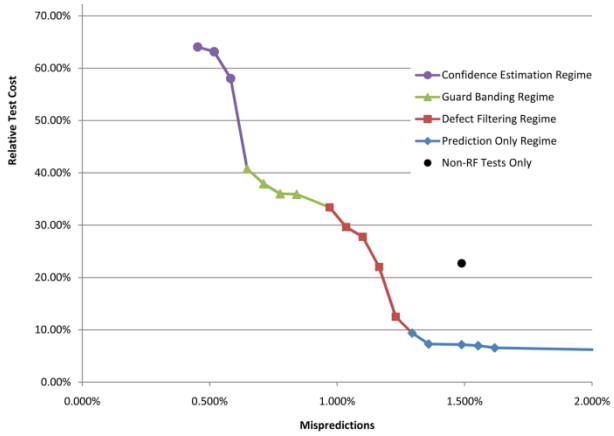


Figure 1: Comparison of various guard-banding schemes for analog/RF specification test compaction

We have also developed an adaptive test scheme to counteract the impact of process variations and ATE drifts on the accuracy of specification test compaction.

INDUSTRY INTERACTIONS

IBM (Mustapha Slamani and Alberto Valdes-Garcia), Texas Instruments (Friedrich Taenzler, John Carulli and Ken Butler), Intel (Prashant Goteti)

MAJOR PAPERS/PATENTS

[1] H-G. Stratigopoulos et al, "Error Moderation in Low-Cost Machine Learning-Based Analog/RF Testing," IEEE TCAD, 2008

[2] H-G. Stratigopoulos et al, "RF Specification Test Compaction using Learning Machines," IEEE TVLSI, 2010

[3] N. Kupp et al, "On Boosting the Accuracy of Non-RF to RF Correlation-Based Specification Test Compaction," JETTA, 2009

[4] N. Kupp et al. "Confidence Estimation in Non-RF to RF Correlation-Based Specification Test Compaction," ETS 2008

TASK ID# 1836.030, FAST PVT-TOLERANT PHYSICAL DESIGN OF RF IC COMPONENTS

SARAJU P. MOHANTY, UNIVERSITY OF NORTH TEXAS, saraju.mohanty@unt.edu
ELIAS KOUGIANOS, UNIVERSITY OF NORTH TEXAS, eliask@unt.edu

SIGNIFICANCE AND OBJECTIVES

PVT variability makes it hard to achieve "safe" designs in nanoscale CMOS technologies and also reduces yield. However, no major attempts have been made to address these for RFICs due to increased complexity and bottlenecks of analog simulation. We investigate fast physical design and optimization techniques for RF ICs such that the resulting designs are PVT tolerant.

TECHNICAL APPROACH

To have a process-variation robust design accounting for parasitics, power, and temperature, we investigate a new "PVT tolerant RF IC design flow". In a standard RF IC design flow, multiple iterations between the front-end circuit design and back-end layout are required to achieve parasitic closure. Such a manual approach requires X number of iterations. The proposed design flow is to reduce the number of manual iterations to 1, by performing the X number of iterations on a parasitic parameterized netlist instead of the layout. Hence, **this novel flow reduces the X number of manual iterations required for parasitic closure, to 1 manual iteration**.

SUMMARY OF RESULTS

The effects of PVT variation on the performance of RF IC components is analyzed. A current-starved VCO circuit is used as a case study. The physical design of the VCO is performed using a 90*nm* CMOS PDK. The simulations were performed on the full-blown (RLCK) parasitic-extracted netlist of the VCO. A total of 1000 Monte Carlo runs are performed to analyze the effect of the variations on the center-frequency of the VCO. The statistical distribution of the center frequency is studied.

It is shown through simulations that parasitics, process, voltage and temperature have a drastic effect on the performance (center frequency) of the VCO. The 5 parameters considered for process-voltage variation are as follows: (1) *VDD*: Supply voltage, (2) *VThn*: NMOS threshold voltage, (3) *VThp*: PMOS threshold voltage, (4) *Toxn*: NMOS gate oxide thickness, (5) *Toxp*: PMOS gate oxide thickness. Each of these process parameters is assumed to have a Gaussian distribution with mean taken as the nominal value specified in the process design kit, and a standard deviation of 10% of the mean is assumed. A correlation coefficient (cc) of 0.9 is assumed between *Toxn* and *Toxp*. The VCO is subjected to temperatures of 27°C, 50°C, 75°C, 100°C and 125°C. After full-extraction, a 22% degradation in the center frequency is observed between the preliminary physical design and target frequency. Furthermore, a 50% discrepancy is observed between the preliminary physical design and target frequency when the VCO is subjected to *worst case* PVT. **The flow achieved 16.4% power (including leakage) minimization with 10% degradation in center frequency compared to the target frequency, in the presence of *worst-case* variations**.

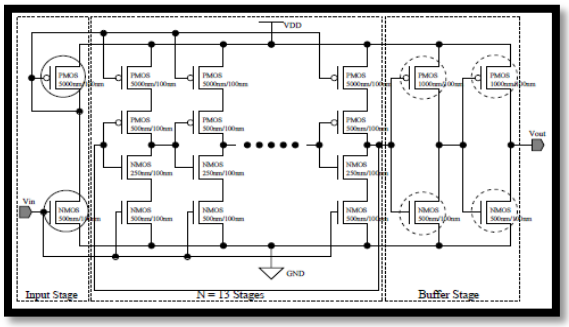


Figure 1: VCO Circuit with Dual-Threshold Voltage.

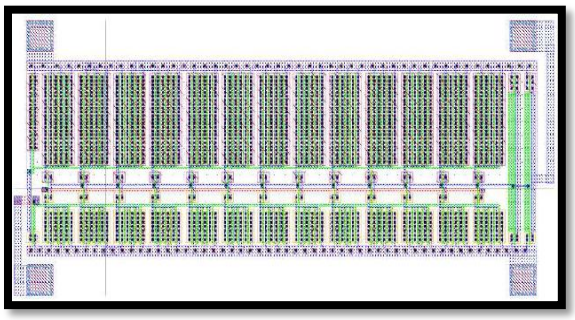


Figure 2: P4VT Optimal Dual-Threshold VCO Layout.

Keywords: Process Variation, Parasitic Effects, Temperature Effects, Nanoscale CMOS, RF Circuits

INDUSTRY INTERACTIONS

Priyadarsan Patra, Intel Corporation

MAJOR PAPERS/PATENTS

[1] S. P. Mohanty, D. Ghai, and E. Kougianos, "A P4VT (Power-Performance-Process-Parasitic-Voltage - Temperature) Aware Dual-*VTh Nano-CMOS VCO", in Proceedings of the 23rd IEEE International Conference on VLSI Design (ICVD)*, pp. 99-104, 2010.

TASK ID# 1836.031, VARIATION TOLERANCE ANALOG DESIGN BASED ON GENERALIZED KHARITONOV/LYAPUNOV THEORY

DIAN ZHOU, UNIVERSITY OF TEXAS AT DALLAS

SIGNIFICANCE AND OBJECTIVES

In today's VLSI technology, the manufactured fluctuations are unavoidable. We propose an efficient method, in spirit of the Kharitonov's theorem, to compute the likely performance range of linear analog circuit with process variations. This approach reduces the computational burden to evaluation of at most 48 critical transfer functions.

TECHNICAL APPROACH

The geometrical properties of Kharitonov's theorem state that phase and magnitude response of a family of interval polynomials are bounded by four Kharitonov polynomials in this family. Assume the behavior of a linear analog circuit is governed by an interval transfer function which is the ratio of two families of interval polynomials. Therefore the magnitude and phase response of the interval transfer function can be calculated from the overall combinations of eight Kharitonov polynomials for the numerator and denominator interval polynomial families.

SUMMARY OF RESULTS

The envelop of 48 critical Kharitonov-type transfer functions can yield variation range of magnitude response, whereas 16 critical Kharitonov-type transfer functions are sufficient to calculate the variation range of phase response. Take a RAFFC three-stage amplifier as example, and the derived transfer function is:

$$A_v(s)=\frac{-1-s\dfrac{C_{C1}}{g_{mb}}}{\dfrac{1}{A}(1+\dfrac{s}{\omega_{P1}})[1+s\dfrac{C_{C1}+C_L}{g_{m3}C_{C1}}C_{C2}+s^2\dfrac{C_{C2}C_L}{g_{mb}g_{m3}}]}$$

where $A=g_{m1}r_{01}g_{m2}r_{02}g_{m3}r_{03}$, $\omega_{p1}=1/C_{C1}r_{01}g_{m2}r_{02}g_{m3}r_{03}$. Assume there is ±10% tolerance level to every parameter. Fugure.1 (a) and (c) display the envelop of magnitude and phase response of RAFFC circuit which is calculated from 48 and 16 Kharitonov-type critical transfer functions. Figure.1 (b) and (d) show the envelop and 500 Monte Carlo samples when every parameter is sampled randomly from its variation range. It is obvious that the samples are well enclosed by the envelops. The simulation of 500 samples spends 2.47h, but underestimates the variation range. The magnitude and phase envelop yields the exact bounds within 15.2354s and 11.1191s respectively. From the envelops, we can also tell that the gain of RAFFC circuit may vary from 106dB to 118dB, whereas the variation range of phase margin lies within [45.5°, 178°].

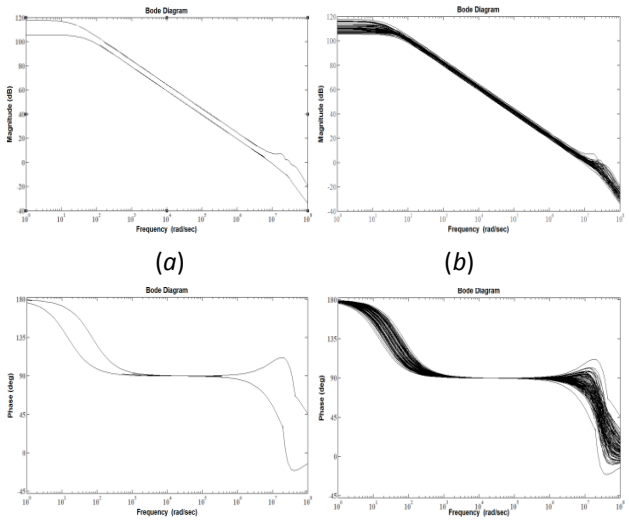


Figure.1 (a) The envelop of magnitude response; (b) The envelop and 500 Monte Carlo samples of magnitude response; (c) The envelop of phase response; (d) The envelop and 500 Monte Carlo samples of phase response

Next step, we will extend the proposed approach to other interested performance metrics and nonlinear circuits. We will also study the Lyapunov theory, and apply it in the robust analysis of VLSI circuits in the time domain.

Keywords: Kharitonov's theorem, interval polynomial, gain, phase margin.

INDUSTRY INTERACTIONS

Texas Instruments, Intel

MAJOR PAPERS/PATENTS

[1] L. Qian et al., "Worst Case Analysis of Linear Analog Circuit Performance Based on Kharitonov's Rectangle," (Submitted) 2010 ICSICT.

[2] L. Qian et al, "Performance Robustness Analysis of VLSI Circuits with Process Variations Based on Kharitonov's Theorem," (Submitted) 2010 DCAS.

TASK ID# 1836.032, MILLIMETER-WAVE PHASE-LOCKED LOOP DESIGN WITH ENHANCED TOLERANCE TO PROCESS & TEMPERATURE VARIATION

RANJIT GHARPUREY, UNIVERSITY OF TEXAS AT AUSTIN, ranjitg@mail.utexas.edu

SIGNIFICANCE AND OBJECTIVES

A key challenge to the manufacturability and robustness of designs at mm-wave frequencies arises from process and temperature (P&T) induced variations. This research focuses on the design of a phase-locked loop (PLL) based mm-wave frequency synthesizer for 77 GHz RADAR applications that is robust to such variations.

TECHNICAL APPROACH

The impact of process and temperature variations on PLL circuits will be investigated and critical sensitivities will be identified through simulation. Circuit and architectural solutions to minimize changes in critical performance metrics, and prevent catastrophic failures due to such variations will be implemented. Techniques that can provide adequate frequency span of circuits, such as oscillators and dividers, in order to compensate for process variations, without compromising the phase noise of the synthesizer will be investigated. Circuit techniques for controlling the gain and amplitude response of the phase detector and inter-stage buffers will be explored. The compensation techniques will be optimized for ensuring minimal power and area overhead.

SUMMARY OF RESULTS

Key effects of process and temperature variations on critical circuits employed in the PLL have been studied in simulation during the first year of the project.

A significant impact of process variation is on the center frequency of the oscillator, and the operating frequency of the high-frequency dividers used in the PLL. It is important to ensure that these circuits have sufficient frequency span, so as to accommodate the frequency spread caused by variations and the frequency range required by the system.

Ensuring tunability over a wide frequency span presents a significant challenge at mm-wave frequencies. This is due to the high sensitivity of these designs to parasitics, such as those introduced by devices and interconnects used for increasing the tuning range. In addition, a large tuning range often comes at the expense of degraded phase noise in oscillators. This tradeoff is observed in multiple design approaches used for extending frequency range, e.g., switched capacitors for coarse tuning in an oscillator. In this work, we target a frequency range of over 10% around the nominal center frequency of 60 GHz, to compensate for process variation. This span needs to be achieved without degrading phase noise across the full frequency range.

Multiple oscillators with offset center frequencies can be used to avoid the above trade-off. However this can be expensive due to a large area penalty, in addition to suffering from additional routing parasitics, and uncertainty arising from these. A technique that allows for dual-mode oscillator operation in order to achieve wide frequency span of the oscillator, ideally without the above trade-off between phase noise and tuning range, is proposed for this work. The design approach uses the technique proposed in [1][2] (Fig. 1), wherein, instead of switching passive elements within the tank, the active core is reconfigured around it, so as to allow dual mode operation.

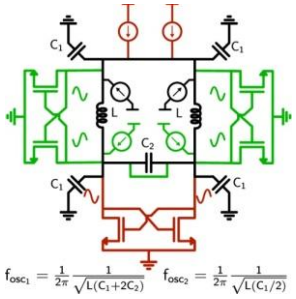


Fig. 1: Active core reconfiguration for dual-mode operation [1] with tank capacitor modification

As the second part of the work, the impact of temperature variations on performance metrics of key circuits within the PLL has been studied. Techniques to compensate for these variations are being investigated.

Keywords: Frequency synthesis, phase-locked loop, variability, voltage-controlled oscillator, mm-wave design

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] R. Gharpurey *et al.*, A Single-Tank Dual-Band Reconfigurable Oscillator, VLSI Symp. 2006, pp. 176-177

[2] S. Agarwal *et al.*, A Dual-mode Wide-band CMOS Oscillator, IEEE DCAS Workshop, 2009, 64-66

TASK ID# 1836.033, MIMO RADAR FOR PIXEL REDUCTION IN MM-WAVE IMAGING

MOHAMMAD SAQUIB, UNIVERSITY OF TEXAS AT DALLAS, saquib@utdallas.edu

SIGNIFICANCE AND OBJECTIVES

Millimeter wave (mm-wave) radar technology is a highly potential candidate for many safety and health care applications. In an effort to achieving a higher level of precision and affordability of such systems, multiple-input-multiple-output (MIMO) radar technologies and smart image processing techniques are incorporated into the mm-wave framework in this project.

TECHNICAL APPROACH

The transceiver design for the MIMO radar mm-wave imaging system involves waveform design, antenna array design, and image processing techniques. Novel transmitted waveforms with good correlation properties are devised within the frequency range of interest (200-300 GHz) with hardware complexity and battery power constraints. Since sparse MIMO antennas have better resolution than uniform linear array antennas, antenna array design are addressed as well. Adaptive image reconstruction and pixel reduction methods are developed and implemented so that the desired image resolution can be obtained with the minimum number of antennas, which in turn reduces the hardware complexity and cost.

SUMMARY OF RESULTS

In an effort towards lowering the transceiver cost of an mm-wave imaging system, a framework has been established for developing a complete system that will improve image resolution. Significant progress has been made in designing optimal mm-wave transmit waveforms with good autocorrelation properties, and devising adaptive receive filters.

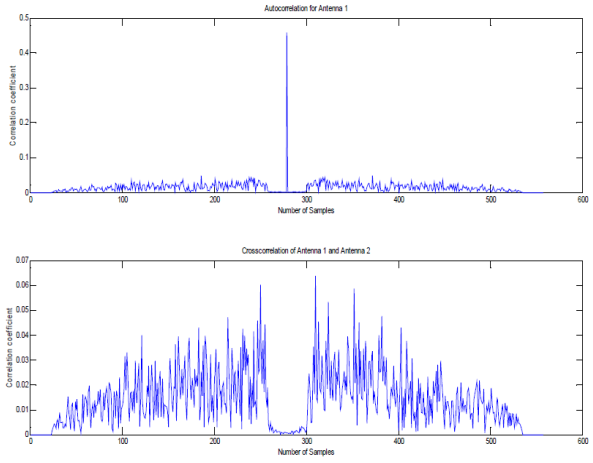


Figure 1: Autocorrelation (top) and cross-correlation (bottom) properties of transmit waveforms.

(1) The initial transmitter structure is proposed in this report taking into account the properties of MIMO radar imaging as well as that of mm-waves. An iterative algorithm is used in obtaining the constant modulus transmit signals that have close-to-orthogonal properties (shown in Fig 1). Although orthogonality is desired in MIMO radar applications in general, it is not usually feasible practically. The proposed waveforms are not strictly orthogonal but have good auto and cross-correlation properties. The waveforms are constant modulus, and it is possible to generate a high number of samples (almost 1000) using this algorithm.

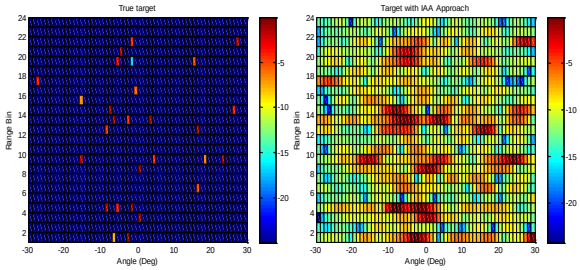


Figure 2: (left) True target positions, with different reflectivity indices; (right) spotlight SAR image obtained through Iterative Adaptive Approach with a MIMO array

(2) When an MIMO radar transmits simultaneous signals, the reflected signals from the scatterers are overlapped, and added with high levels of noise and strong clutter. Efficient adaptive receive filters are required to extract the targets. An iterative adaptive approach has been employed in this context (results shown in Fig 2) to estimate the reflectivity indices of the targets. Further adaptive techniques are in the process of design and exploration, with a goal to obtain the optimal receive performance.

Keywords: millimeter wave (mm-wave) radar, MIMO antenna array, constant modulus waveform, iterative adaptive approach, target resolution.

INDUSTRY INTERACTIONS

Texas Instruments.

1836.034: 77-81 GHZ CMOS TRANSCEIVER WITH BUILT-IN SELF-TEST AND HEALING

BHASKAR BANERJEE, UNIVERSITY OF TEXAS AT DALLAS, bhaskar.banerjee@utdallas.edu

SIGNIFICANCE AND OBJECTIVES

The objective of this project is to develop integrated millimeter-wave transceiver in CMOS, with built-in self-test (BIST) capabilities that will minimize the testing cost and enable the development of low-cost, affordable millimeter-wave radios for 77 GHz automotive radar applications. In addition to one time calibration, the receiver will be capable of correcting for variations in circuit performance by monitoring the circuit blocks in regular intervals and compensating for errors.

TECHNICAL APPROACH

In this task, the PI proposes to develop an integrated transceiver with built in self-test and healing for 77 GHz automotive radar applications, using highly scaled CMOS technology. To reduce the costs associated with detailed performance testing to ascertain 'good' and 'bad' ICs, we propose to employ an on-chip built-in loopback test methodology. In the loopback mode, the test signal is sent from the baseband, which travels through the transmit chain, and 'loops' through and enters the receive chain and comes back to the baseband. The loopback path is typically created using an on-chip CMOS switch.

Fig. 1 shows the overall system schematic with the loopback path. The main circuit blocks in the transceiver are a tunable low-noise amplifier (LNA), active mixers, tunable IF amplifier and a tunable power amplifier.

To successfully implement the BIST at millimeter wave frequencies, the loopback path must be implemented with minimum insertion loss and maximum isolation. Since this is a pulsed RADAR system, the transmitter and the receiver are not operational simultaneously. This allows us to use an SPST switch to complete the loopback path. During the calibration and compensation mode, the loopback SPST switch is closed and the transmitter is programmed to transmit lower power, so as to not saturate the receive path, and the signal is fed back into the receiver. By varying the gain steps of individual blocks, namely the LNA, the IF amplifier, etc. it is possible to estimate and correct for errors in the transceiver operation.

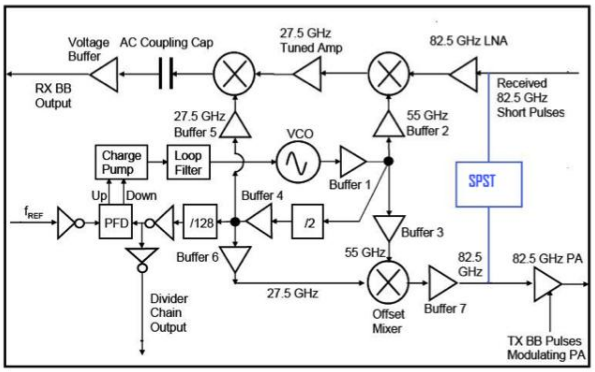


Fig. 1. A simple schematic of the pulsed automotive RADAR transceiver with Built-in Self Test (BIST).

SUMMARY OF RESULTS

A complete system overview and link budget analysis for 77-81 GHz RADAR has been performed to ascertain the required performance from the circuits. Table 1 shows the specification requirements of the system.

Table 2. System Specifications for Long Range Radar

Parameter	Value
Signal Band-width	170 MHz
Information Band-width	436 kHz
Required SNR	10 - 10log4 = 4 dB
Receiver Sensitivity	-104 dBm
Tx Power	15.0 dBm
Tx Antenna Gain	14.5 dBi
Path Loss	-141 dB
Rx Antenna Gain	14.5 dBi
Receiver Sensitivity	-104 dBm

Keywords: BIST, Self-healing, Automotive Radar, millimeter-wave, CMOS.

INDUSTRY INTERACTIONS

Texas Instruments

1836.035: DEVELOPMENT OF CMOS SUB-TERAHERTZ RECEIVERS FOR SPECTROMETERS

BHASKAR BANERJEE, UNIVERSITY OF TEXAS AT DALLAS, bhaskar.banerjee@utdallas.edu

SIGNIFICANCE AND OBJECTIVES

Sub-terahertz (THz) frequency bands of the electromagnetic spectrum find many uses in short range radars, spectrometers for detection of chemicals, and detection of concealed weapons. The objective of this project is to develop a receiver of a sub-terahertz spectrometer (180 – 300 GHz) using CMOS integrated circuit technologies that wirelessly detects chemicals for medical, security and safety applications.

TECHNICAL APPROACH

To cover the entire proposed spectrometer band of 180 – 300 GHz, the receiver will be split-up into six sub-bands, covering 20 GHz bands each. The receiver chain covering each 20 GHz sub-band is centered at different frequency bands and it down-converts the received spectrum down to an intermediate frequency (IF) of 10 MHz to reduce the impact of 1/f noise. The sample-under-test, is excited by a series of sinusoidal tones with frequency spanning from 180 GHz to 300 GHz in steps of 10 kHz. The scanning rate could be anywhere between 1-10 GHz/second. The reflected waveform, from the sample, is detected by the receiver, which would need to resolve the absorption dips in the spectrum separated by ~ 500 kHz, and with a frequency resolution of about 10 kHz.

Fig. 1 shows the schematic of the direct conversion receiver. An alternative version with a dual down conversion (heterodyne) architecture is also being investigated to optimize the overall receiver sensitivity.

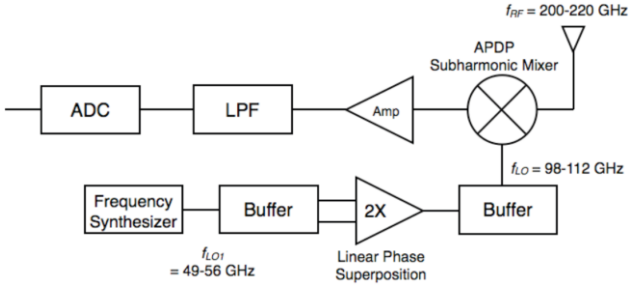


Fig. 1. Block diagram of the direct conversion receiver for 200-220 GHz band

SUMMARY OF RESULTS

The overall system link budget analysis have been performed and summarized below in Table 1.

Table 3. Summary of the direct conversion receiver.

Parameters	Mixer in (RF) port	Mixer out port	Amplifier out port	IF out port
CNR (dB)	49.4	13.9	13.9	13.9
Power (dBm)	-20	-34.4	0.3	-1.5
Gain (dB)	0	-14.4	20.3	18.5
Noise Figure (dB)	0	14.7	17.5	17.5

An anti-parallel diode based mixer has been designed in a 130 nm CMOS process. The circuit schematic of the mixer is shown in Figure 2.

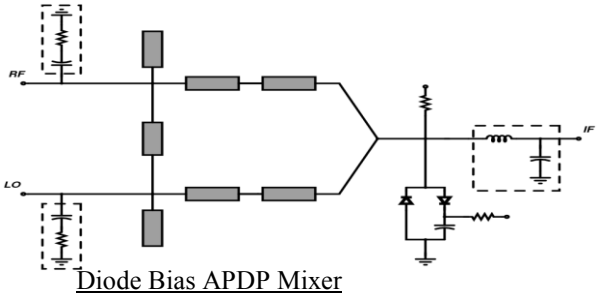


Fig. 2. Simple schematic of an APDP mixer with an RF of 200 GHz, and an LO of 100 GHz. The LO power assumed is 0 dBm. The mixer gain is – 11 dB with an isolation of -13 dB.

Keywords: Spectrometer, sub-terahertz, CMOS, receiver.

INDUSTRY INTERACTIONS

Texas Instruments

TASK ID# 1836.036, SIGNAL GENERATION FOR 200-300 GHZ SPECTROMETERS

K.K.O, UTD, k.k.o@utdallas.edu

SIGNIFICANCE AND OBJECTIVES

As part of the effort to help open up high millimeter and sub-millimeter wave frequency range for moderate volume and cost applications, this task is studying the feasibility of realizing a transmitter in CMOS for a rotational spectrometer that detects harmful molecules and analyzes breath.

TECHNICAL APPROACH

This task will study the feasibility of realizing a transmitter for a rotational spectrometer in CMOS. The transmitted power should be ~10-100 μW. The main challenge is increasing the output frequency range, power, and frequency for phase locked signals. To realize a fast scan rate with a 10-kHz step, use of a fractional-N synthesizer will be investigated. The oscillator will operate at lower frequency than the output. The output signal is generated using a combination of an N-push technique and non-linear effects. This task will help generate the LO signal for the receiver.

SUMMARY OF RESULTS

To examine the feasibility of phase locking 300-GHz signal, a 200-GHz frequency divide four circuit driven by a 200-GHz oscillator with a 410-GHz push-push output shown in Figure 1 is fabricated in TI 45-nm CMOS. The circuit is being prepared for measurements.

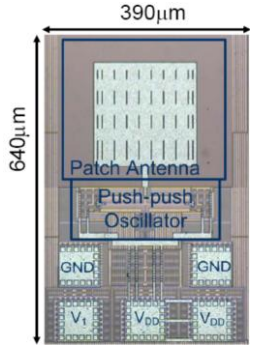


Figure 1: A 410-GHz oscillator fabricated in 45-nm CMOS. It integrates a patch antenna for quasi-optical measurements. Output power is -49 dBm.

The output power and tuning range of 410-GHz oscillator is too low for the spectrometer. To sufficiently increase these, most likely the oscillator should operate at even lower frequency. As mentioned, the output signal is generated using a combination of an N-push technique and non-linear effects. A 4-push oscillator is shown in Figure 2.

The performance trade-off for operating the oscillator at 2, 4, and 8 times below the output frequency has been evaluated. It appears that operation at 8 times below the output frequency should allow generation of sufficient output power and tuning range for a single transmitter to cover the 180-300 GHz output range. The transmitter architecture including that for the fundamental oscillator is being finalized. The structure will be fabricated and measured this year.

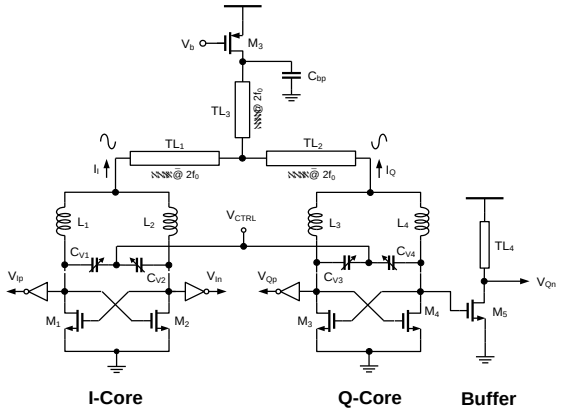


Figure 2: A potential architecture for signal generator.

Approaches to achieve a fast scan rate (~ 1GHz/sec) with a step size of 10 kHz in a fractional-N synthesizer are also being investigated.

Keywords: rotational spectrometer, transmitter, CMOS, millimeter-wave.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] K. K. O et al., "Feasibility for Sub-Millimeter Wave CMOS Integrated Circuits," **(Invited)** 2010 Government Microcircuit Applications and Critical Technology Conference, March, 2010, Las Vegas, NV

[3] D. Shim et al., "Paths to Terahertz CMOS Integrated Circuits," **(Invited)** 2009 Custom Integrated Circuits Conference.

[3] E.-Y. Seok et al., "Paths to Terahertz CMOS Integrated Circuits," Accepted to IEEE Journal of Solid State Circuits.

TASK ID# 1836.037, DEVELOPMENT OF ANTENNA AND CHIP INTERFACE SYSTEMS FOR MILLIMETER WAVE AND SUB-MILLIMETER WAVE APPLICATIONS

RASHAUNDA HENDERSON, UNIVERSITY OF TEXAS AT DALLAS, rmh072000@utdallas.edu
ANDREW BLANCHARD, UNIVERSITY OF TEXAS AT DALLAS

SIGNIFICANCE AND OBJECTIVES

Feasibility study to develop techniques for designing and integrating high performance passive and RF matching components in the millimeter and sub-millimeter wave band. Techniques to improve radiation characteristics for antennas integrated into a CMOS processing strategy. This work is significant to developing cost-effective packaging for millimeter wave CMOS systems.

TECHNICAL APPROACH

The technical approach is to improve performance of planar antennas by using novel broadband geometries as compared to microstrip patches. The antennas will be integrated with CMOS ICs using a post-CMOS fabrication process utilizing photo-definable dielectric layers and gold metallization. Broadband antenna design and matching will be incorporated to minimize mismatch between the IC and antenna. Multiple transmission lines will be studied for optimizing CMOS integration. Simulation tools include FEKO for antenna design and Ansoft HFSS for interconnect and integration design. These results will lead to affordable mm-wave CMOS electronics for automotive radar and spectrometers for harmful molecule detection.

SUMMARY OF RESULTS

A novel planar antenna has been designed with input return loss bandwidth of 55% (where |S11| is better than 10 dB) from 4.6 to 8.2 GHz. This design has been implemented in Rogers RT/Duroid (ε_r = 2.2) and will be scaled to millimeter wave frequencies using benzocyclobutene (BCB) (ε_r =2.36). The aperture antenna is fed using the popular uniplanar transmission line, coplanar waveguide (CPW). Lumped element models are being developed for microstrip, CPW and grounded coplanar waveguide for use in circuit simulators and best performance interconnects between millimeter wave CMOS ICs and broadband antennas. Goals for year two include demonstrating 1) a broadband planar antenna up to 110 GHz, 2) best-performing transmission line designs up to 300 GHz in 65 nm CMOS back end of line and post-CMOS BCB processes. Fig. 1 shows the top view of the broadband aperture antenna and Fig. 2 shows the input return loss for the design comparing simulation and measurement.

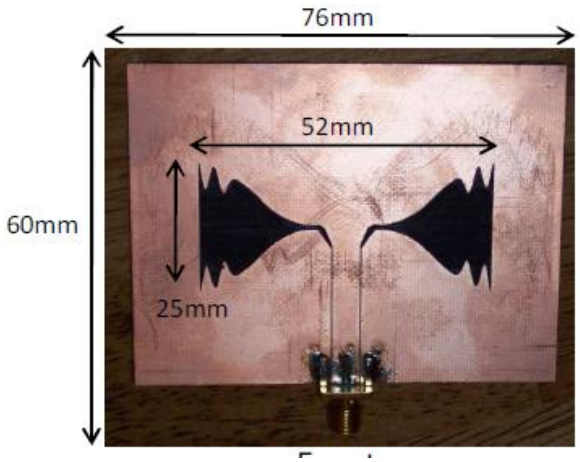


Figure 1: Broadband planar aperture antenna.

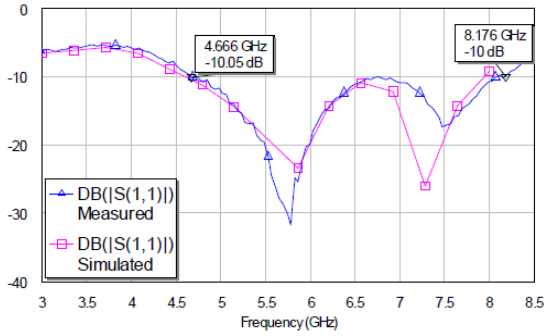


Figure 2: Measured and simulated antenna return loss.

Keywords: antennas, integration, CMOS, broadband, TMLs

INDUSTRY INTERACTIONS

Intel

MAJOR PAPERS/PATENTS

[1] R. Islam et al., "Performance of Planar Transmission Lines for Millimeter-Wave CMOS," Accepted to SRC TechCon 2010, September 2010, Austin, TX.

[2] R. Pierce et al, "Broadband Modified Bowtie Aperture Antenna," Accepted to SRC TechCon 2010, September 2010, Austin, TX.

TASK ID# 1836.038, A HYBRID 14-BIT ANALOG-TO-DIGITAL CONVERTER FOR BROADBAND APPLICATIONS

JOSE SILVA-MARTINEZ, TEXAS A&M UNIVERSITY, COLLEGE STATION, jsilva@ece.tamu.edu
AYDIN KARSILAYAN, TEXAS A&M UNIVERSITY, COLLEGE STATION

SIGNIFICANCE AND OBJECTIVES

High resolution, high bandwidth and low power ADCs are a relevant need according to the International Technology Roadmap for Semiconductors. In this project, a 5th-order ΣΔ ADC architecture is implemented. Digital signal processing is used to reduce sensitivity to clock jitter. Robustness against saturation from blockers is achieved using a low power low-resolution control at the front-end.

TECHNICAL APPROACH

A low power, wide bandwidth 5th-order CT-ΣΔ ADC with improved tolerance to blockers shown in Figure 1 is proposed. The blocker detection is realized by using an array of comparators that monitor the internal signal nodes to detect potential saturation conditions. Excessively large signals activated the comparator outputs activating the out-of-loop PGA which attenuates the input signal so as to reduce the internal signals to within the ADC's linear range. Blocker tolerance is achieved without changing any of the ADC internal loop parameters, therefore this scheme offers fast settling times with moderate SNDR degradation in the presence of blockers.

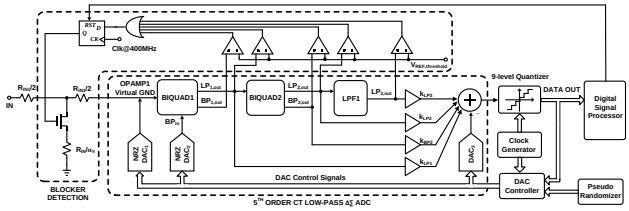


Figure 1: 5th-order ΣΔ modulator with saturation detection and input attenuator.

SUMMARY OF RESULTS

The proposed system is currently been implemented in a 1.2V, 90nm CMOS technology. The ADC shows stability to the sudden appearance of the blocker at 100MHz with input power as large as 8.7 dBFS in presence of an inband signal at 5MHz and –6 dBFS. Although not within the loop, the manipulation of the ADC input stage makes the system to be disturbed. Worst case recovery time of the system in response to a sudden blocker at the ADC input is less than 1us. Figure 2 depicts the blocker tolerance performance in the presence of a -6dBFS in-band input signal and various conditions. The worst-case condition occurs for a blocker around 40MHz; the proposed technique improves the blocker tolerance by 12dB when compared with the blocker tolerance of the typical ADC.

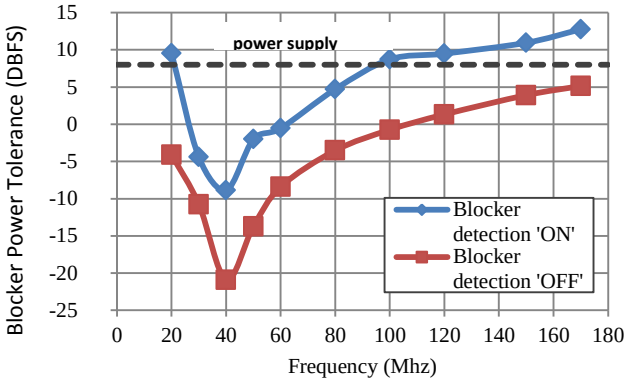


Fig.2. Blocker Tolerance in the presence of a -6dBFS in-band signal at 5 MHz

At the worst case, the SNR degrades by 29 dB due to the attenuation of 12 dB at ADC input and due to the increase in the in-band noise floor. The voltage swing at each internal node increases; hence, system non-linearities produce intermodulation products folding part of the out-of-band noise into baseband.

Keywords: ΔΣ modulator, ADC, blocker-tolerance, clock-jitter, continuous-time filters

INDUSTRIAL LIAISONS

Douglas Garrity, Freescale Semiconductor
Vijay Rentala and Alex Reyes, Texas Instruments Inc.
Stewart Taylor, Intel Corporation

PARTICIPATING STUDENTS

Hemasundar Mohan Geddada, Chang Joon Park, PhD students and Aravind Padyana, MSc student

MAJOR PAPERS/PATENTS

[1] J. Silva-Martinez, A. Karsilayan, H. M. Geddada, A. Padyana and C. J. Park, "A Blocker Tolerant Broadband Analog-to-Digital Converter Architecture," SRC TECHCON 2010 Proceedings, September 2010.

[2] C.-Y. Lu, M. Onabajo, V. Gadde, H.-P. Chen, Y. C. Lo, V. Periasamy and J. Silva-Martinez, "A 25MHz Bandwidth 5th-Order Continuous-Time Lowpass Sigma-Delta Modulator With 69dB Dynamic Range Using Time-Domain Quantization and Feedback," IEEE J. Solid-State Circuits. vol. 45, pp. 1795-1808, Sept. 2010.

TASK ID# 1836.039, UXID: UNCLONABLE MIXED-SIGNAL INTEGRATED CIRCUITS IDENTIFICATION

FARINAZ KOUSHANFAR, RICE UNIVERSITY, farinaz@rice.edu

SIGNIFICANCE AND OBJECTIVES

This project aims at the design and implementation of a new mixed-signal architecture for physical unclonable functions (PUF). PUFs provide efficient means for hardware protection and enable many new security applications including but not limited to remote activation and monitoring of the genuine hardware.

TECHNICAL APPROACH

The introduced novel PUF architecture converts the analog variations present in device leakage currents to a unique digital quantity at high speed and low power. Larger variations in leakage current lead to robust digital responses in presence of fluctuations in operational conditions such as temperature and supply voltage. Experimental results suggest about less than 5% PUF output instability in presence of 10% variations in V_{DD} and over 70°C fluctuations in temperature. The project is in phase of chip layout design.

SUMMARY OF RESULTS

Figure 1 depicts the architecture of the new PUF circuit. First, PV sensitive currents are generated by using individual FETS whose gate voltages are tied to a sub-threshold voltage source. Next, based on the input challenge, a subset of currents are selected and combined using the differential current switches. The combined values are then compared and converted to digital responses using a latch-based current base sense amplifier. The implementation details are omitted due to space constraint but are available upon request.

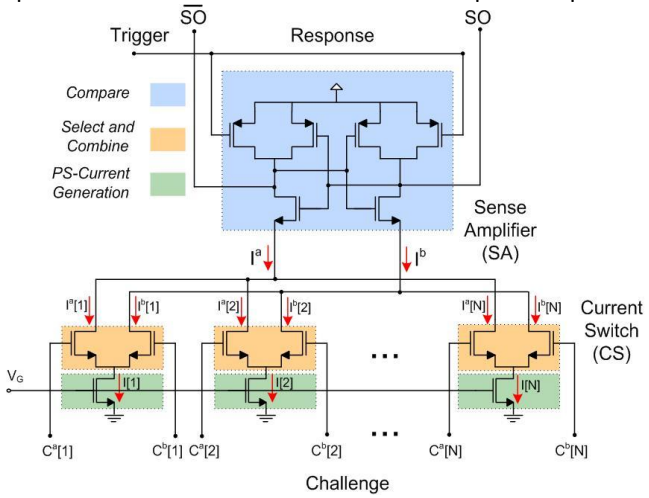


Figure 1: Leakage current-based PUF architecture

The gate voltage of the current generator FETs must be carefully tuned in order to achieve reliable operation at the sense amp and obtain maximal dependence on process parameter variations. Figure 2 shows the average response error rate under fluctuations in temperature for different gate voltages. For very small gate voltages, the currents will be so small that cannot trigger the sense amp. For larger gate voltages, the transistors exit the sub-threshold operation region, and the currents will be less sensitive to the variations in process parameters as a result. The experiments suggest that the optimal gate voltage must be 0.3Vdd. For this optimal, the error rate under extreme military temperature conditions, is less than 5%.

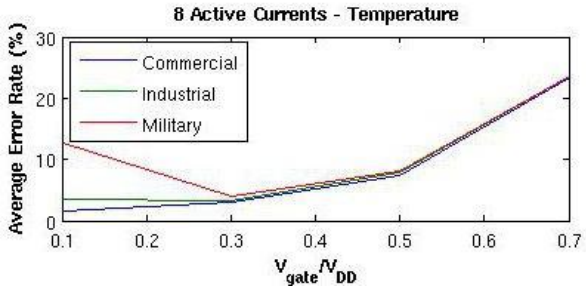


Figure 2: Average response error rate versus the current generators gate voltage.

The target system is composed of 64 sense amps each producing a single response bit. Each sense amp is connected to 128 current generator FETs and differential current switches. The challenges activate a subset of the currents based on the number. The sense amplifier automatically stops the current flow immediately after the responses are settled which results in extremely low power consumption.

Currently, we are in process of physical implementation, top level integration and taping out the above mentioned chip in IBM9LP technology. The target run date is September 27 through MOSIS. The chip occupies a 4mm×4mm of area, and is designed for a 32 pin package. Two sets of supplies are considered to keep the analog circuitry immune from digital noise. The test will be performed at different operational conditions to confirm response stability and robustness.

Keywords: physically unclonable functions, sub-threshold leakage, process variation, hardware security

INDUSTRY INTERACTIONS

IBM Austin Research Lab, Texas Instrument

TASK ID# 1836.040, ENERGY-EFFICIENT CMOS 10GS/S 6-BIT ADC WITH EMBEDDED EQUALIZATION

DR. SAMUEL PALERMO, TEXAS A&M UNIVERSITY, spalermo@ece.tamu.edu

SIGNIFICANCE AND OBJECTIVES

The ADC architecture proposed here aims to significantly improve the energy efficiency of Nyquist-rate ADCs for high-speed medium-resolution applications. In order to achieve this goal, this work will use a low-power time-interleaved (TI) successive-approximation-register (SAR) ADC with embedded decision feedback equalization.

TECHNICAL APPROACH

SAR architecture has proved to achieve the best energy efficiency for this application. In order to achieve the required conversion rate time-interleaved structure with unit SAR ADCs is used. The target design is a 6-bit 10GS/s ADC with figure of merit (FOM) better than 0.5pJ/conv.-step. To further relax the digital processing and achieve better efficiency for the whole receiver, especially for high-speed link applications, ADC with embedded equalization is considered.

SUMMARY OF RESULTS

As mentioned earlier, a time-interleaved SAR ADC architecture is used to achieve the best energy efficiency. Figure 1 shows the block diagram of the 6-bit 10GS/s ADC. As shown, the target ADC consists of 8 parallel time-interleaved sub-ADCs. On the lower level, seven time-interleaved unit SAR ADCs form each sub-ADC.

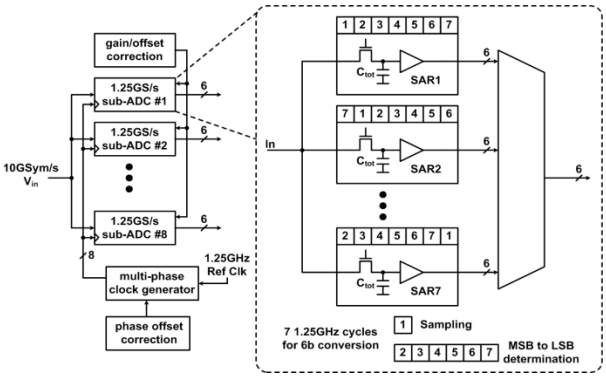


Figure 1: The block diagram of the proposed 6-bit 10GS/s time-interleaved SAR ADC.

Although high time-interleaving factor may seem to result in better energy efficiency, it introduces another issue. Now, any mismatch among sampling clocks of different channels can result in performance degradation of the entire ADC. System simulations show that the absolute phase matching of each 1.25GHz sampling clock in Figure 1 should be better than 0.5ps. Moreover, due to time interleaving, the offset and gain mismatches between parallel channels should be calibrated as well.

This ADC can be used as the front-end of a receiver in a high-speed link in order to implement complex equalization schemes in digital domain. Embedding part of the equalization in ADC can potentially result in higher resolution ISI cancellation and/or better power efficiency. However, the main challenge is to make sure that the power/area overhead due to the embedded equalization is small enough to justify this approach.

The schematic simulation of a 6-bit 1.25GS/s sub-ADC is performed in 90nm CMOS technology. Each sub-ADC should have a bandwidth equal to the Nyquist bandwidth of the 10GS/s ADC, i.e., 5GHz. Simulations show an abrupt ADC performance degradation at large frequencies. This is mainly due to the front-end T/H. Hence, bootstrapped sampling switches are used to increase the effective resolution bandwidth of each sub-ADC to more than 5GHz. Besides, because of bootstrapping, power consumption of the front-end T/H can be decreased for the same linearity. Table 1 shows the power breakdown of the sub-ADC from schematic simulations for both cases in 90nm CMOS technology.

Table 1: Power breakdown of simulated 6-bit 1.25GS/s sub-ADC in 90nm CMOS technology

Block	Power (mW)	
	Simple NMOS Samp. Switches	Bootstrapped NMOS Samp. Switches
Front-End T/H	3.06	2.17
Comparators+ Latches	1.54	1.54
DACs	0.125	0.125
Total	4.725	3.835

Keywords: Embedded equalization, energy efficient, high speed, successive approximation register (SAR) ADC, time interleaved

INDUSTRY INTERACTIONS

Texas Instruments, Intel

TASK ID#1836.041, A HIGH-EFFICIENCY SINGLE-INDUCTOR MULTIPLE-INPUT MULTIPLE-OUTPUT INTEGRATED DC-DC CONVERTER FOR ENERGY-HARVESTING APPLICATIONS

HOI LEE, UT-DALLAS, hoilee@utdallas.edu

SIGNIFICANCE AND OBJECTIVES

Today's technologies enable harvesting various energy sources from the ambient environment. This research aims to investigate new approaches in a high-efficiency energy conversion system that can make the best use of multiple available energy sources harvest from the environment by optimally combining them for ultimately realizing low-power self-powered devices.

TECHNICAL APPROACH

This research will develop a high-efficiency, cost-effective single-inductor multiple-input multiple-output (SIMIMO) DC-DC conversion system. The proposed SIMIMO converter is capable of optimally extracting and combining different energy sources from different independent harvested input sources and simultaneously providing multiple, independent and controllable output voltages. In particular, a single-inductor dual-input dual-output (SIDIDO) boost converter will be first realized to demonstrate the proposed concept. Joint design optimization strategies of the proposed SIDIDO converter for minimizing the cross regulation and maximizing the power efficiency especially for light-load condition will be focused on.

SUMMARY OF RESULTS

A SIDIDO boost converter has developed in the first year of this project. The converter can extract energy from two independent inputs via time-multiplexing scheme. A switching-timing-aware pulse-frequency modulation (STAPFM) control as shown in Fig. 1 is developed not only to minimize the power losses at light-load condition but also to regulate two independent outputs without having the cross-regulation problem [1].

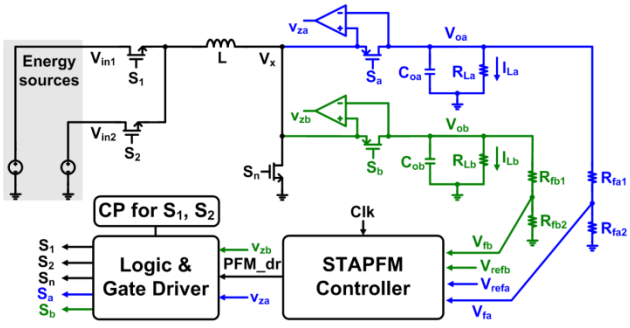


Figure 1: Structure of single-inductor dual-input dual-output boost converter with STAPFM control.

The STAPFM control can also change the switching frequency of the converter at multiples of a pre-defined clock frequency based on the load-current variation for reducing the switching power loss and ensuring the predictable noise spectrum.

The proposed converter was implemented in a 0.35-µm standard CMOS process. Simulation results show that the proposed STAPFM scheme reduces the converter switching power loss by up to 23 times compared with a conventional fixed-frequency pulse-width-modulated control. The proposed STAPFM controller only dissipates 15µW. The proposed converter can deliver a maximum output power of 16mW and the converter achieves 89% peak efficiency at the output power of 6mW.

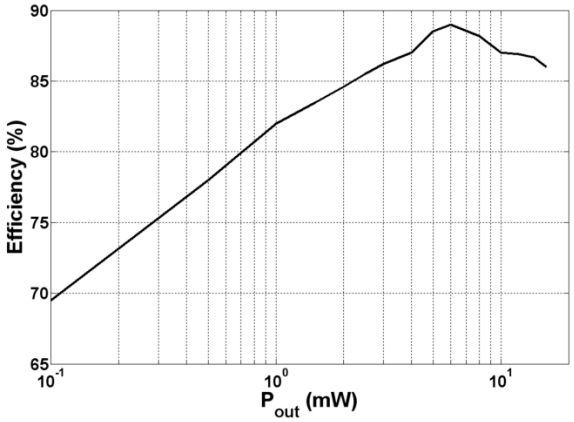


Figure 2: Simulated power efficiency of the proposed SIDIDO boost converter with STAPFM control.

Keywords: Boost converter, cross regulation, single-inductor dual-input dual-output converter, switching converter, switching-time-aware pulse-frequency control

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] M. Du and H. Lee, "An efficiency-enhanced SIDIDO boost regulator with switching-time-aware pulse-frequency-modulation for energy harvesting applications," 2011 IEEE Applied Power Electronics Conference and Exposition, Feb. 2011, Fort Worth, TX, USA, submitted for publication.

TASK ID# 1836.042, ADAPTIVE DATA PREDICTION BASED RECEIVER FOR POWER-EFFICIENT HIGH-RESOLUTION ULTRASOUND IMAGING SYSTEMS

DONGSHENG MA, THE UNIVERSITY OF TEXAS AT DALLAS, dma@email.arizona.edu

SIGNIFICANCE AND OBJECTIVES

High-resolution portable ultrasound imaging systems are highly demanded in the medical diagnostics due to unique features of convenience, low cost and accurately examining the moving tissues. The objective of this research is to develop an adaptive data prediction based (**ADPB**) receiver to break through the dynamic range and SNR limitation of those current ultrasound imaging products.

TECHNICAL APPROACH

To enhance dynamic range and reduce the noise without extra cost, two types of the ADPB receiver are proposed, as shown in Fig. 1. In both systems, an adaptive linear predictor is employed to estimate the next sample signal based on the past ones. A high-resolution digital signal is generated by quantizing the fine redundancy between the input and the predicted signal. Hence, the wide dynamic-range requirement can be significantly relaxed. Furthermore, by eliminating the time-gain compensator of the traditional receiver and its control circuitry, the noise, distortion as well as power consumption induced by them are completely removed.

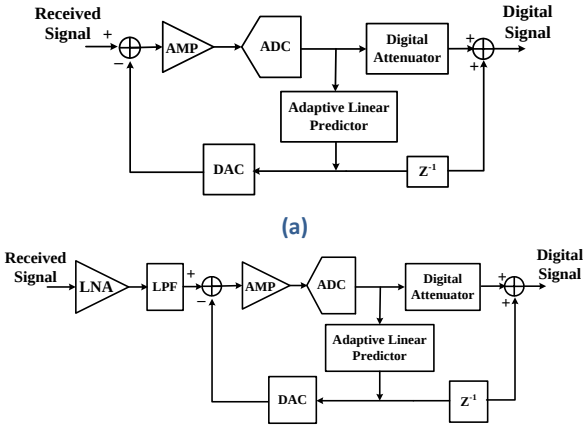


Figure 1: The proposed (a) Type I and (b) Type II adaptive data prediction based ultrasound imaging receiver.

SUMMARY OF RESULTS

The reconstructed ultrasound images in Fig. 2 illustrate performance improvements. The ADPB receiver shows a much clearer objective with more than 22-dB dynamic range increment.

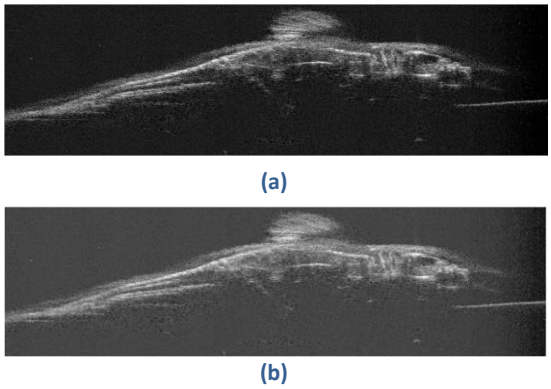


Figure 2: Reconstructed ultrasound imaging by using (a) conventional receiver and (b) the proposed ADPB receiver.

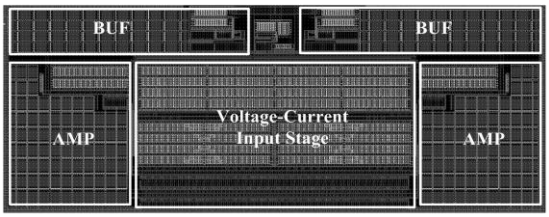


Figure 3: Microphotograph of a low-noise variable gain amplifier.

In the proposed ADPB receiver architecture, a low-noise variable-gain amplifier is employed to accommodate the dynamic range of ADC. By using a current-feedback topology, the measured gain range of the amplifier is from 13.8 dB to 36.3 dB with 7.41 nV/$\sqrt{\text{Hz}}$ noise floor in the bandwidth of 10 MHz. The microphotograph of the amplifier is shown in Fig.3.

Keywords: Ultrasound Imaging Receiver, High Resolution, Dynamic Range, Adaptive Data Prediction

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Y. K. Wang et al, "Adaptive Data Prediction Based Receiver for Power-Efficient High-Resolution Ultrasound Imaging Systems", *Advanced Research Institute for Biomedical Imaging Workshop*, Oct. 2009.

[2] Y. K. Wang et al, "Low-Noise CMOS Time-Gain-Compensation Amplifier for Ultrasound Imaging Receivers", submitted to *IEEE Transactions on Circuit and Systems*-II.

TASK ID# 1836.043, A MONOLITHIC HIGH VOLTAGE LINEAR AMPLIFIER

PING GUI, SOUTHERN METHODIST UNIVERSITY, pgui@smu.edu

SIGNIFICANCE AND OBJECTIVES

This project seeks to design a monolithic integrated high-voltage linear amplifier to be used as the transmitter in ultrasonic systems for improved imaging quality. The proposed linear amplifier will significantly reduce the harmonic distortions and achieve good power efficiency. The design methods and techniques can be applied to other applications.

TECHNICAL APPROACH

Present ultrasound systems use pulser drivers as the transmitter. Albeit being simple, pulser drivers introduce harmonic distortions in the output waveform, which prevents Harmonic Imaging techniques from being used. We investigate two different architectures for designing linear amplifiers: class-AB and switching amplifiers. Novel techniques such as fully differential structure, nested Miller compensation, and totem-pole techniques are explored reduce the second harmonic distortions (HD2) and obtain high voltage output swing, wide bandwidth and high slew rate in the class-AB amplifier. Modulation schemes such as sigma-delta, PWD, etc will be explored to achieve good linearity and high power efficiency in the switching amplifier.

SUMMARY OF RESULTS

Since the project got started in August 1, 2009, we have successfully designed two class-AB linear amplifiers using 0.7 um SOI process with 120 V CMOS devices. Two techniques, Totem-pole and fully-differential architectures, shown in Fig. 1, are explored to obtain a high output voltage swing beyond the breakdown voltage of the MOSFET transistors. The amplifier employing totem-pole technique produces a single-ended output to directly drive the ultrasound transducer with 180Vpp voltage signal while achieving a good linearity (THD = -40 dB and HD2 = -50 dB). The fully-differential class-AB amplifier is able to provide a high output voltage up to 180Vpp with an ultra-low HD2, below -100 dB. Both amplifiers can work with ultrasonic signals of frequency from 1 to 5 MHz, with a slew rate of greater than 11.4 V/ns, and an average power dissipation of less than 140 mW [1], which allows four channels to be implemented in the same IC. The design was implemented and taped out for fabrication in June 2010.

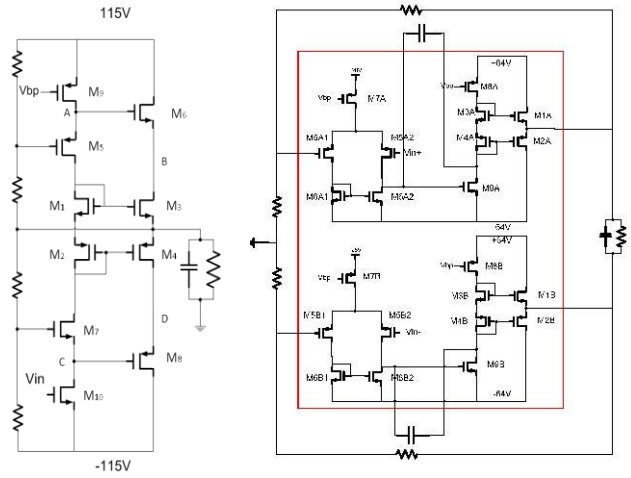


Figure 1: (a) The schematic of a totem-pole output stage of a class-AB amp to obtain large output swing. (b) The schematic of a differential class-AB output stage which cancels HD2.

The goals for the remaining two years are: a) to explore techniques in class-AB amplifier to further improve the bandwidth to cover up to 20 MHz signals; b) to explore techniques in conjunction with class-D amplifier to achieve both good linearity and power efficiency ; c) to compare the two architectures in terms of linearity, power dissipation, design complexity and cost.

Keywords: Linear Amplifier, High Voltage, HD2, Voltage Swing, Class-D Amplifier.

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] Z. Gao, P. Gui, I. Oguzman, X. Xu, K. Vasanth, " A High Voltage Linear Amplifier for Ultrasound Applications", SRC TECHCON, 2010.

TASK ID# 1836.044, STATISTICAL MODELS AND METHODS FOR DESIGN AND TEST OF NON-DIGITAL COMPONENTS

XIN LI, CARNEGIE MELLON UNIVERSITY, xinli@ece.cmu.edu
SHAWN BLANTON AND LAWRENCE PILEGGI, CARNEGIE MELLON UNIVERSITY

SIGNIFICANCE AND OBJECTIVES

Develop, implement, and validate through experiment the statistical models and methods for the design of SRAM bit cells and their surrounding analog periphery circuits with user-provided constraints on performance, yield and quality.

TECHNICAL APPROACH

A unified statistical analysis engine is developed to predict SRAM performance, yield, reliability and testability by fast Monte Carlo method. The proposed engine adapts the recent advance of Gibbs sampling from the statistics community to adaptively search the variation space and speed up the convergence of Monte Carlo analysis. Our experimental results demonstrate that the proposed Gibbs sampling method achieves 3~10× runtime speedup over other state-of-the-art techniques without surrendering any accuracy.

SUMMARY OF RESULTS

SRAM bit cells are generally designed with minimum-size devices, and can be significantly impacted by large-scale process variations posed by nanoscale manufacturing technology. It becomes increasingly critical to evaluate the statistical behavior of SRAM bit cell both efficiently and accurately. Since SRAM bit cells typically have extremely small failure probability, a simple Monte Carlo method suffers from slow convergence rate as only few random samples will fall into the failure region. To improve the sampling efficiency, importance sampling has been proposed to directly sample the failure region based on a distorted probability density function (PDF), instead of the original PDF of process variations.

Applying importance sampling to SRAM analysis, however, is not trivial. Ideally, in order to maximize prediction accuracy, we should sample the failure region that is most likely to occur. Such a goal, however, is extremely difficult to achieve, since we never know the exact failure region in practice. Motivated by this observation, a novel Gibbs sampling method is developed to improve the efficiency of importance sampling. Unlike the traditional Monte Carlo algorithm that samples a given PDF, the proposed Gibbs sampling approach does not need to know the sampling PDF explicitly. Instead, it adaptively searches the failure region and then generates random samples in it. From this point of view, Gibbs sampling can be conceptually viewed as a unique Monte Carlo method with an integrated optimization engine which allows us to efficiently explore the failure region. As a result, SRAM failure probability can be accurately predicted with a minimum number of sampling points.

As a demonstration example, we consider an industrial 65nm SRAM cell. For testing and comparison purpose, three different importance sampling methods are implemented to estimate the failure probability: (1) mixture importance sampling by IBM (MIS), (2) minimum-norm importance sampling by MIT (MNIS), and (3) Gibbs sampling (proposed). Figure 1 shows the estimated failure probability (normalized) as a function of the number of random samples. Note that the proposed Gibbs sampling is substantially more accurate than the other two traditional methods (i.e., MIS and MNIS) given the same number of random samples.

In this future, we will take advantage of the high efficiency of the proposed Gibbs sampling method to further study the design trade-offs (e.g., speed, power, yield, reliability, testability, etc.). We will also use the proposed statistical analysis engine to study SRAM reliability and testability.

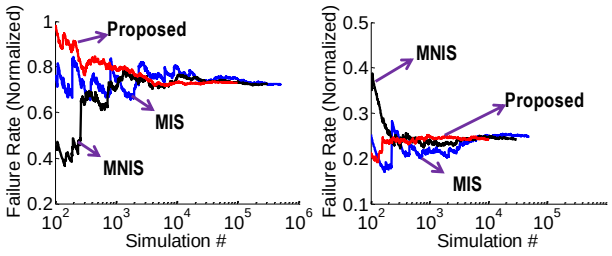


Figure 1: Convergence rate of different Monte Carlo algorithms for SRAM failure rate prediction. (Left) Failure due to read noise margin. (Right) Failure due to write noise margin.

Keywords: memory, parametric yield, statistical analysis

INDUSTRY INTERACTIONS

Texas Instruments, Freescale, IBM, Intel

MAJOR PAPERS/PATENTS

[1] C. Dong and X. Li, "Toward a unified statistical analysis engine of SRAM yield, reliability and testability via Gibbs sampling," SRC TECHCON, 2010.

TASK ID# 1836.045: FREQUENCY CHANNELIZED ADC FOR WIDE BANDWIDTH SYSTEMS

WON NAMGOONG, UNIVERSITY OF TEXAS AT DALLAS, namgoong@utdallas.edu

SIGNIFICANCE AND OBJECTIVES

The objective of this work is to develop a new approach for achieving low-power, compact, medium-to-high resolution (≥ 6 ENOB) analog-to-digital conversion for multi-gigahertz wideband signal.

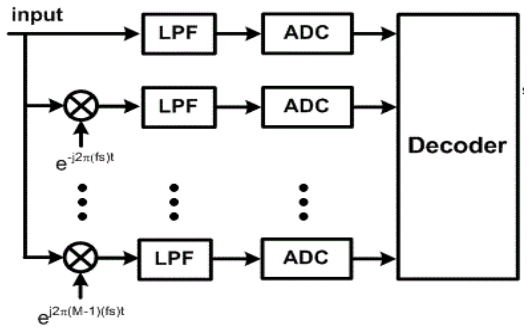
TECHNICAL APPROACH

As designing both high resolution and high sampling frequency data converter is difficult, the wideband signal can be decomposed into a large number of narrow frequency subbands using a cascade of mixers and low pass filters. The resulting subband outputs are then digitized using narrowband ADCs operating at a fraction of the signal Nyquist rate. The proposed architecture should enable efficient medium-to-high resolution (≥ 6 ENOB) data conversion of a multi-gigahertz wideband signal.

SUMMARY OF RESULTS

To digitize a multi-gigahertz bandwidth signal, a commonly used approach is to time-interleave multiple ADCs, each operating at a fraction of the desired sampling frequency. Such time-interleaved ADC (TIA) suffers from numerous implementation challenges, mostly resulting from the large input bandwidth that each ADC must support. A fundamental problem of the time-interleaved architecture is the mismatches among the demultiplexing channels. These mismatches are especially pronounced when operating at high data rates, as small transistors with corresponding small input capacitance are employed to meet the bandwidth requirements. The resulting offset problems often increase the design complexity by requiring additional compensation circuitries. Another important drawback is the high sensitivity to sampling jitter caused by aliasing of the wideband input signal. Power consumption is also significant in TIA because of the bandwidth, power, and accuracy trade-off in preamplifier/comparator circuitry (assuming flash ADCs for high speed) and the need to generate accurate multi-phase clocks.

Instead of channelizing by time-interleaving ADCs, the received signal can be channelized into multiple frequency subbands with an ADC in each subband channel operating at a fraction of the effective sampling frequency. The same number of ADCs with each sampling at the same frequency as the ADCs in TIA achieves the same effective sampling frequency. As designing band pass filters centered at high frequencies to generate the multiple frequency subbands is difficult, especially in integrated circuits, the wideband signal can be decomposed using a bank of mixers and low pass filters (see Figure below) as in our earlier work. The advantage of the frequency channelized ADC (FCA) is that the input signal bandwidth to each ADC is reduced by approximately the number of subbands, greatly mitigating many of the TIA implementation challenges caused by the wide input signal bandwidth to each ADC. As a result, FCA enables data conversion that is more robust to channel mismatches and sampling jitter than TIA. Furthermore, power consumption is reduced as the design of preamplifier/comparator circuitry is simplified, and the use of power-hungry multiple-phase clock generator is replaced by simple frequency dividers (as described later). Another important advantage is that amplification is much easier in the FCA than in the TIA. As FCA amplifies the subband signal, the amplifier gain-bandwidth product required is a fraction of that in TIA, which needs to amplify the entire signal bandwidth before sampling.



Keywords: ADC, digital compensation, frequency channelization,

INDUSTRY INTERACTIONS

Texas Instruments, Freescale

MAJOR PAPERS/PATENTS

None to date

TASK ID# 1836.046, RECONFIGURABLE ANTENNA INTERFACE FOR LOW POWER WIRELESS SENSOR NODES

DAVID ALLSTOT, UNIVERSITY OF WASHINGTON, allstot@ee.washington.edu
KARTHIK NATARAJAN, JEFFEREY WALLING, UNIVERSITY OF WASHINGTON

SIGNIFICANCE AND OBJECTIVES

Reconfigurable radio on a sensor platform can lower the platform cost. In addition to the reconfigurability, battery consumption is critical in autonomous sensor nodes. An efficient reconfigurable power amplifier targeted towards the MICS (Med-Radio) and the Zigbee standards will be designed and fabricated.

TECHNICAL APPROACH

A reconfigurable antenna interface requires configuration flexibility in terms of frequency and mode control. Different modulation techniques necessitate reconfiguration of the power amplifier to be able to switch from the varying envelopes modulation schemes (ASK) to fixed envelopes ones (FSK).

Body Area Network (BAN) applications require very low EIRP, typically around few microwatts. For the BAN, Class C amplifiers suit perfectly as they radiate small amount of power with high efficiency.

SUMMARY OF RESULTS PATENTS

An example class C amplifier with a tapped capacitor output matching network and third harmonic trap is shown in Figure 1.

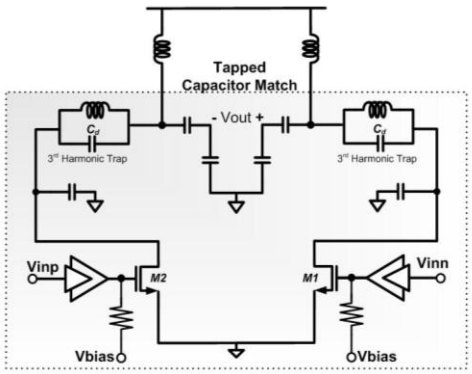


Figure 1: Class C PA with Tapped Capacitor Matching Network

The third harmonic trap is necessary to improve suppression of the large third harmonic component seen at the output due to non-linear operation. The PA is driven with self-biased analog inverters and a DC bias can be provided to the gate of the PA through a large pull-up resistor. With V_{bias}=0, class C operation is achieved. By changing V_{bias}>0, the PA can be operated in the any of the other linear PA modes.

The PA has been designed for fabrication in a 130 nm RF CMOS process with 8 metal layers. The post-extracted simulated PAE of the PA vs. input power is shown in Figure 2. The PA attains a maximum PAE of 48% is obtained, which is ~ 3X better than previously designed PAs for MICS compliant BANs.

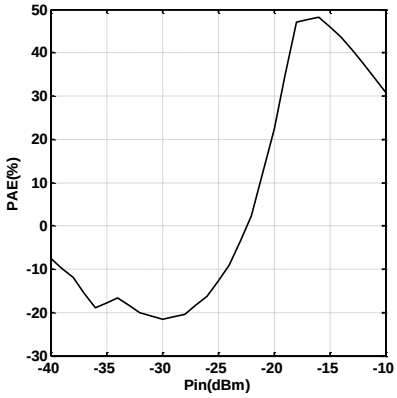


Figure 2: PAE Vs Pin Class C Mode

The power transfer characteristic isn't linear, as expected due to Class-C operation. At peak efficiency, an output power of -8 dBm (158 μW), which is higher than necessary for MICS operation.

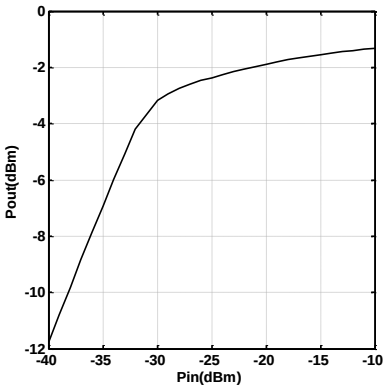


Figure 3: POUT Vs Pin Linear Mode

Figure 3 shows output power vs. input power, when a DC bias of 300 mV is applied to the gate is shown in Figure 5. The peak PAE of the PA is only 20% but the transfer curve is pretty linear.

Keywords: BAN, Sensor Node, Class C, Reconfigurable

INDUSTRY INTERACTIONS

Ajith Amarasekara, Texas Instruments

TASK ID # 1836.047, INTEGRATION OF MILLIMETER WAVE ANTENNAS USING SYSTEM IN PACKAGE TECHNIQUES

RASHAUNDA HENDERSON, UNIVERSITY OF TEXAS AT DALLAS, rmh072000@utdallas.edu

SIGNIFICANCE AND OBJECTIVES

Feasibility study to develop new techniques for the integration of broadband, high performance antennas with state-of-the-art millimeter wave CMOS circuits. Support the development of low cost automotive radar and spectrometer applications. This work is significant to achieving packaged performance metrics while being affordable.

TECHNICAL APPROACH

The technical approach is to design a methodology that optimizes performance of foundry CMOS silicon circuits with broadband antennas integrated onto a low cost package substrate. Antennas are printed on PCB using short feeds suitable for millimeter and sub-millimeter wave frequencies. Flip-chip assembly is used to attach the IC to the substrate and provide the smallest footprint and highest performance. Simulation is used to predict loss tangent influence and fabrication is used to confirm the results. Method of moments (MOM) tools including Sonnet, Agilent Momentum and AWR Axiem are being studied for frequency-dependent loss tangent control.

SUMMARY OF RESULTS

Transmission line performance studies were conducted via simulation to determine if printed circuit board (PCB) material could be accurately modeled up to 100 GHz. The required substrate thickness for single-mode operation was determined to be approximately 125 µm. Flame retardant 4 (FR4) is the standard dielectric used in PCBs but has loss tangent values quoted by manufacturers at distinct frequencies (typically no higher than 15 GHz). Vendors who supply the material in the necessary thicknesses have been identified as Nelco or Isola with dielectric constant of 3.65 and loss tangent of 0.01. This material is anisotropic and studies were conducted of various electromagnetic (EM) vendors to determine which could reasonably model loss tangent that is frequency dependent. Figure 1 shows the concept view of the CMOS IC flip-chip attached to the low cost substrate. Table 1 summarizes the results of three EM simulation tools for a 50 ohm microstrip transmission line fabricated in FR4. Figure 2 shows simulated return loss for a single via in FR4 using Sonnet. Year 2 deliverables include demonstrating flip chip attach and broadband antenna performance up to 300 GHz.

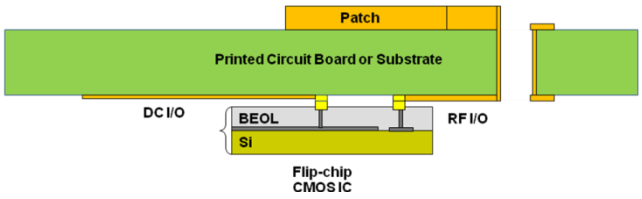


Figure 1: Concept of a CMOS IC flip-chip attached to a low cost PCB integrated with an antenna.

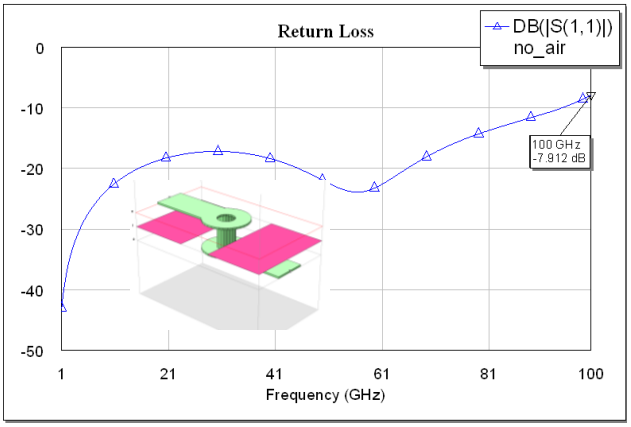


Figure 2: Sonnet simulation of return loss for FR408 via.

Table 1: MOM Simulation study of 50 Ω line on FR4/PCB

	Sonnet	ADS Momentum	AWR Axiem
Loss tangent control	Simple	Complex, Relaxation Model	Advance material properties
|S21|(dB) for 125 µm FR4	1.75 @ 100 GHz	1.75 @ 100 GHz	1.9 @75 GHz

Keywords: antenna in package, FR4, millimeter wave CMOS

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

None to report.

TASK ID# 1836.048, MILLIMETER AND SUBMILLIMETER GAS SENSORS: SYSTEM ARCHITECTURES FOR CMOS DEVICES

FRANK C. DE LUCIA, OHIO STATE UNIVERSITY, fcd@mps.ohio-state.edu

SIGNIFICANCE AND OBJECTIVES

The objective of this project is to develop an approach to a compact and inexpensive gas sensor based on millimeter and submillimeter (mm/submm) spectroscopy and implemented in CMOS technology. The dramatic cost, size, and power savings of CMOS will make this attractive sensor competitive in the mass market.

TECHNICAL APPROACH

We have recently demonstrated that powerful and unique sensors in the mm/submm spectral region are now practical. This task (coordinated with other tasks that will provide the necessary CMOS antennas, receivers, and transmitters) seeks to develop and demonstrate architectures appropriate for the mass market. This will be accomplished by an iterative interaction between our sensor design background, the development of an intermediate approach based on wireless technology, and the CMOS design teams.

SUMMARY OF RESULTS

In its initial phases this project is designed to interface closely with three CMOS development projects. These projects are to develop a probe source for the gas sensor, a sensitive heterodyne receiver, and antennas to transmit the microwave power from the source, through the gas interaction region, and onto the detector.

We have considered the trade space among sensor specificity and sensitivity on one hand and the variables within CMOS based technology. By iterating with our CMOS collaborators, we have arrived at an optimization of the technology for this application and this optimization is being used for the CMOS design.

In parallel with this effort, our project is developing a system, shown in Fig. 1, based on technology that is becoming commercially available from the wireless industry. This will allow us to demonstrate for interested parties systems that are substantially smaller and less expensive than our current systems that are based on one-of-a-kind III-V technology. The final CMOS implementation will significantly reduce the size/cost further.

The results of our calculations and simulations have been provided to our CMOS collaborators, but have not been published in the open literature. We list below two

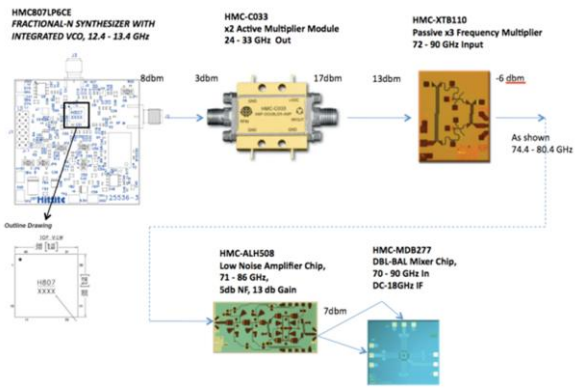


Figure 1: The architecture for the intermediate wireless implementation to demonstrate reduction in size/cost on the path to CMOS implementation.

publications that discuss both the baseline system that has been used to validate the parameters provided and a discussion of the underlying spectroscopy [1, 2].

In the coming year the specifications for the CMOS devices will become available, and we will iteratively provide feed back based on our sensor analysis for the projected characteristics of the CMOS based sensors. We also expect to have a breadboard version of our wireless implementation operational.

Keywords: compact submillimeter spectroscopic gas sensor

STUDENTS

Jennifer Holt
Mark Patrick

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS

[1] F. C. De Lucia, "The Submillimeter: A Spectroscopist's View," J. Mol. Spec. **261**, 1-17 (2010).

[2} I. R. Medvedev, C. F. Neese, G. M. Plummer, and F. C. De Lucia, "Submillimeter spectroscopy for chemical analysis with absolute specificity," Opt. Lett. **35**, 1533-1535 (2010).

TASK ID# 1836.049, ON-CHIP CURRENT-SENSING TECHNIQUES FOR SWITCHING DC-DC CONVERTERS

PI HOI LEE, UT-DALLAS, hoilee@utdallas.edu

SIGNIFICANCE AND OBJECTIVES

The aim of this project is to develop and verify on-chip compact current sensors using standard CMOS technologies and a novel current-controlled scheme for improving the operation speed of the current-mode DC-DC regulators, thereby enhancing the profile and the power efficiency of the power converters.

TECHNICAL APPROACH

In this one-year project, a dynamically-biased shunt feedback has been developed in both peak and valley current sensors to improve the speed and the accuracy of the current sensing. An auto-selectable peak- and valley-current control (ASPVCC) has also been proposed to relax the settling-time requirement of the current sensing for further improving the sensing speed. A buck regulator with the proposed ASPVCC and dynamically-biased shunt feedback current sensors was realized in a 0.35µm CMOS for performance verifications.

SUMMARY OF RESULTS

A buck regulator with the proposed ASPVCC is developed (Fig. 1) [2]. The proposed control automatically switches to the peak-current control when D ≥ 0.5, whereas it is under the valley-current control when D < 0.5. Since the peak-current control (valley-current control) avoids small on-time (off-time) of duty ratio ranging from 0 – 0.5 (0.6 - 1), the proposed ASPVCC reduces the settling time requirement of current sensing by two times and thus enables the current-mode controlled regulator to operate at a higher switching frequency.

To realize the ASPVCC, both peak and valley current sensors using dynamically-biased shunt feedback are developed [1]. Both current sensors are compact, as their area is about 30 times smaller than that of power transistors. To lower the power dissipation of the controller, only one (either peak or valley) current sensor is operating at any given D by powering off the other counterpart and the ratio between the current consumption of the current sensor and the load current is always smaller than 0.3%.

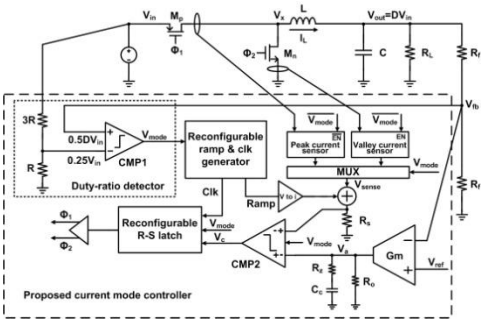


Figure 1: The buck regulator with auto-selectable peak- and valley-current control scheme.

Table I provides comparisons of different buck regulators for portable applications. Compared to reported regulators, the proposed buck regulator is able to operate at the highest switching frequency and to use the smallest inductor with peak power efficiency of 91%.

Table 1: Performance Comparisons of Proposed Work and State-of-the-Art Current-Mode Buck Regulators

	JSSC 04	JSSC 07	This work
Topology	Current-mode	Current-mode	Current-mode
Technology	0.6 µm	0.5 µm	0.35 µm
Chip area	2.9 mm2	4.5 mm2	0.54 mm2
Input voltage (V)	3.0 - 5.2	2.6 - 3.5	2.7 - 4.2
Frequency	1 MHz	0.78 MHz	5 MHz
Peak efficiency	89.5%	85.7%	91%
Max. output current	450 mA	800 mA	500 mA
Inductor	4.7 µH	3.9 µH	1 µH

Keywords: Auto-selectable peak- and valley-current control, DC-DC converters, dynamically-biased shunt feedback, switching converters

INDUSTRY INTERACTIONS

Texas Instruments and IBM

MAJOR PAPERS/PATENTS

[1] M. Du and H. Lee, "An integrated speed- and accuracy-enhanced CMOS current sensor with dynamically-biased shunt feedback for current-mode buck regulators," IEEE TCAS-I, to appear in Dec. 2010.

[2] M. Du and H. Lee, "A 5-MHz 91% peak power efficiency current-mode buck regulator with an auto-switchable peak- and valley-current control scheme," IEEE CICC Sep. 2010, accepted for publication.

TASK ID# 1836.052, AN ULTRA-LOW POWER SIGNAL PROCESSING WITH SMART ANALOG-ENABLED PRE-CONDITIONING STAGE FOR INERTIAL SENSING APPLICATIONS

ROOZBEH JAFARI, UT DALLAS, rjafari@utdallas.edu
WON NAMGOONG, UT DALLAS, namgoong@utdallas.edu

SIGNIFICANCE AND OBJECTIVES

We will provide a complete design framework for an ultra low power signal processing module that will activate full signal chain only when patterns of interest from sensors (motion, ECG) are identified. The ultra low power signal processing module will be designed to operate at minimum supply voltage levels.

TECHNICAL APPROACH

We propose an ultra-low power and light-weight analog front end signal conditioning module for inertial sensors that can perform preliminary signal processing without activating the main signal chain. The preliminary signal conditioning will be performed by means of pattern recognition, at the beginning with very low power and low precision, gradually increasing the power and precision. When a particular pattern of interest is likely recognized, the next stage is activated and eventually, the complete signal chain is activated, when necessary, for further comprehensive processing. For patterns of interest that have a low duty cycle (~1%), we expect to reduce the overall power consumption of the system by several orders of magnitudes.

SUMMARY OF RESULTS

A scalable signal processing methodology based on the concept of normalized cross correlation (NCC) was developed. Each component classifier is a binary template classifier based on the NCC. Every incoming event is compared to a pre-computed template of the target event. This comparison assigns a score value, based on a similarity measure between the incoming event and the template. For classification, the score is compared against a threshold value, and the event is classified as accept or reject. A rejection causes processing to stop for that event. Normalizing the template and incoming signal vector to zero-mean unit vectors constrains Euclidean matching to the surface of a hypersphere of unit radius. This constrained matching is more shape-oriented than the simple Euclidean distance and produces equivalent ranking to the standard NCC measure. A scoring function, $\gamma(\mathcal{T}, f, \tau)$, based on NCC between the signal and the template is defined as follows:

$$\gamma(\mathcal{T}, f, \tau) = \frac{\sum_t [f(t+\tau) - \bar{f}_t][\mathcal{T}(t) - \bar{\mathcal{T}}_t]}{\sqrt{\sum_t [f(t+\tau) - \bar{f}_t]^2 \sum_t [\mathcal{T}(t) - \bar{\mathcal{T}}_t]^2}}$$

The data readings from sensors were acquired at 12 bits per sample. Synthetically, the number of bits per samples was reduced for validation of our proposed technique. The Receiver Operating Characteristic (ROC) curve of each template matching classifier on 'stand to sit' is shown in Figure 3 with different colors. The ROC curve shows true acceptance rate versus false acceptance rate for a binary classifier system as its discrimination threshold is varied. Figure 3 represents sensitivity vs. compliment of specificity. The results suggest that bit resolutions for over 4-bits exhibit a good accuracy for template matching. In the next phase of the study, we will investigate a network of template matching blocks with additional tunable parameters that can leverage a complete screening circuit for rejecting non-target events as early as possible with the lowest power budget.

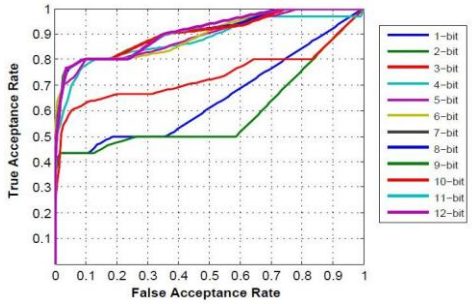


Figure 1: Receiver Operating Characteristic (ROC) curve for template matching at various bit resolutions.

Keywords: low power signal processing, programmable signal processing block, wake-up circuitry

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] S. Ostadabbas, R. Jafari, Spectral Spatio-Temporal Template Extraction of EEG Signals, International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC), August 31, September 4, 2010, Buenos Aires, Argentina.

TASK ID# 1836.053, HIGH-EFFICIENCY HIGHLY-INTEGRATED LED DRIVER SYSTEMS FOR SOLID-STATE LIGHTING APPLICATIONS

HOI LEE, UT-DALLAS, hoilee@utdallas.edu
DIAN ZHOU, UT-DALLAS

SIGNIFICANCE AND OBJECTIVES

Solid-state LED lighting for general illumination can bring significant energy saving and environmental benefits to the society. This research aims to investigate methods of increasing the level of integration of the LED driver for cost reduction and to develop efficiency-enhancement techniques for maximizing the power efficiency of the LED driver.

TECHNICAL APPROACH

This research will develop a low-cost highly-integrated high-efficiency LED driver system by exploring new topologies to design DC-DC converters in the LED driver system, developing circuit techniques to maximize the power efficiency of the LED driver, and employing statistical computational method to model and analyze the LED driver for better predicting system performances due to component variations. This project will first to develop a three-level buck regulator as the non-isolated LED driver. The proposed three-level buck regulator can reduce the voltage rating of each power switch and the power losses compared to the conventional two-level power converters.

SUMMARY OF RESULTS

In this research, a three-level buck regulator as shown in Fig. 1 is selected as the starting point to convert V_{in} = 35V to V_{out} of about 6V. Two switch pairs and three flying capacitors C_{f1} and C_{f2} are employed to build the three-level converter. By increasing the conventional two-level buck converter to three-level topology, each power switch blocks less voltage and thus reducing the overall switching power loss. The volt seconds across the inductor are reduced and so does the ripple current. The conduction power loss in the power switch is thus decreased. In addition, as the voltage rating of each power switch is reduced, it is easier to increase the level of integration of the high-input-voltage power converter using commercial CMOS process technologies.

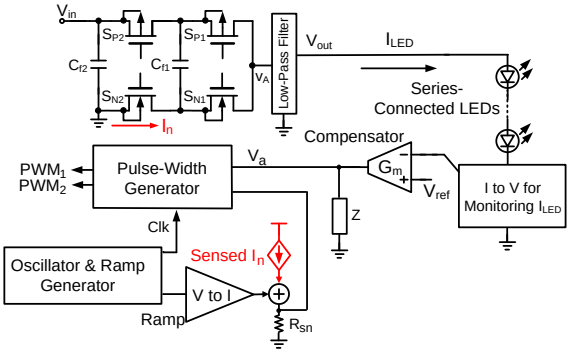


Figure 1: Structure of three-level buck regulator with valley current control.

The proposed three-level converter adopts the constant-frequency valley-current control. Fig. 2 shows the principle of the control. It can be shown that $v_{A1}T_2 = v_{A2}T_1$ = constant. If $v_{A1} > v_{A2}$, the controller forces $T_1 > T_2$ to discharge the net capacitor behind v_{A1} more than that behind v_{A2}, bringing the two voltages closer together. Fig. 3 shows the valley current sensor, in which current through power switch S_{N2} is sensed to get the valley current information for the control loop. The use of the dynamically-biased shunt feedback can push non-dominant poles in the sensor to higher frequencies with low quiescent current and enables the converter to operate at high switching frequency.

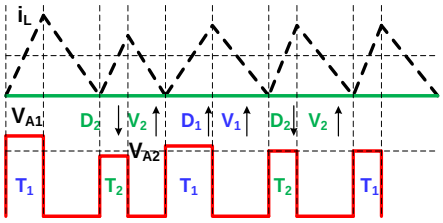


Figure 2: Balancing capacitor voltage by valley-current control in the three-level buck regulator.

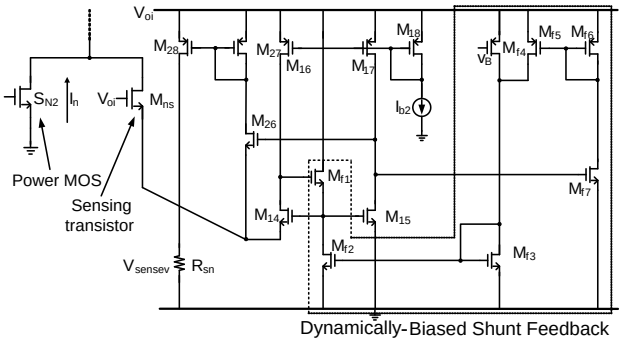


Figure 3: Proposed valley current sensor using dynamically-biased shunt feedback

Keywords: DC-DC converter, LED driver, solid-state LED lighting, three-level converter, valley-current control

INDUSTRY INTERACTIONS

Freescale Inc.

TASK ID# 1836.054, SILICON BASED BEAMFORMING ARRAYS FOR MILLIMETER WAVE SYSTEMS

MURAT TORLAK, UNIVERSITY OF TEXAS AT DALLAS, torlak@utdallas.edu

SIGNIFICANCE AND OBJECTIVES

The purpose of this project is to advance CMOS beamforming arrays for millimeter and the near-THz imaging systems. The main benefit of using silicon at the near-THz region is the possibility of fully integrating the receiver and transmitter components (LNAs, mixers, VCOs, PLLs, PAs, and on-chip antennas) onto a single package.

TECHNICAL APPROACH

There are many challenges and opportunities for integration of antenna arrays into silicon substrate for millimeter imaging systems. We plan to use an architecture with digitally controlled RF phase shifters to achieve a high beamforming gain for millimeter wave imaging systems. We plan to incorporate antennas optimized for silicon on chip and verify the design via antenna simulators and actual measurements using UTD's antenna measurement chamber. Finally, we will incorporate beamforming array into silicon on chip mm-Wave radio with the aid of our industrial and TXACE collaborators to verify the proposed design and to analyze the design trade-offs.

SUMMARY OF RESULTS

We have initial results on two tasks since the beginning of the project in Spring of 2010.

- Mathematical and simulation models for silicon on chip phased arrays in millimeter-wave imaging systems
- Development of 2.4 GHz antenna array for verification of the mathematical imaging models [1].

To develop accurate mathematical models, we are investigating the integration of functionalities such as polarization, I/Q mismatch removal, array calibration, and wideband channel equalization into silicon along with beamforming circuits. There are two typical beamforming systems used in RF systems. One approach uses N full transceivers including the baseband circuitry to achieve optimal capacity for all channel conditions. This multi antenna architecture based on digitally controlled baseband circuits gives ultimate flexibility in terms of manipulating transmitted and received signals such as providing up to N separate beams. Due to very high hardware complexity and very high system power consumption of N full transceivers, we plan to use the alternative architecture with digitally controlled RF phase shifters with single baseband stream. This architecture achieves high beamforming gain in an arbitrary direction with N RF phase shifters. We plan to extend this architecture to multiple beams/multiple bands using the parallelism of RF phase shifters. This is critical since we have limited performance of CMOS circuits which may be operating close to f_T, etc. In addition to challenges in mm- Wave propagation medium, integration of antennas and active circuit components on a single chip has its own unique problems. Especially designing silicon based antennas has to be addressed appropriately. Literature reports low radiation efficiency for antennas with silicon substrate (²r = 11:2 for silicon) and low resistivity. To illustrate the impact of dielectric constant of materials around antennas, an approximated ratio of the radiated power into air and into dielectric substrate is shown in Figure 1. Ansoft HFSS is used to carry out simulations.

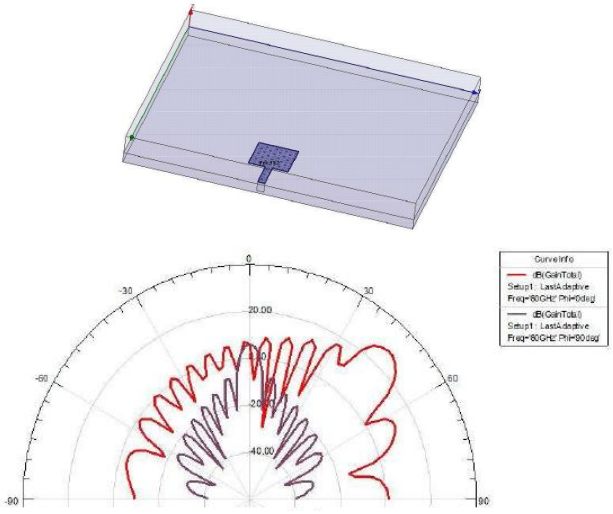


Figure 1: (a) 0.6 × 0.6mm patch antenna simulated in HFSS over silicon substrate (b) Simulated 2-D beam pattern for 16 × 16 planar array,

Keywords: Millimeter waves, imaging, beamforming, silicon antennas, antenna array

INDUSTRY INTERACTIONS

Texas Instruments

MAJOR PAPERS/PATENTS

[1] A. Morshedi and M. Torlak, "Measured Comparison of Dual-Branch Signaling over Space and Polarization Diversity," in revision, IEEE Trans. On Antennas and Propagation.

TASK ID# 1836.055, SPICE MODELS AND ANALOG CIRCUITS FOR NANOSCALE SILICON CHEMICAL- AND BIOLOGICAL-SENSORS

ERIC VOGEL, THE UNIVERSITY OF TEXAS AT DALLAS, eric.vogel@utdallas.edu

SIGNIFICANCE AND OBJECTIVES

Nanoscale chemical and biological sensors have been demonstrated, but little attention has been given to SPICE models and support circuitry. This project will develop physically realistic SPICE models for the sensor device. SPICE model creation will be followed by design of suitable support circuitry for a complete system.

TECHNICAL APPROACH

The design of circuits to support the biological sensor will require a suitable SPICE model which comprehends the unique properties of this device. Generating such a SPICE model in turn requires a thorough understanding of the physics of the sensor and its operating environment. To improve the understanding of the biosensor device physics and generate the necessary data for a suitable SPICE model, a combination of theoretical analysis and TCAD modeling is being utilized. With a SPICE model available, block specifications will be defined and reference support circuits developed.

SUMMARY OF RESULTS

An example of the sensor element under study is shown in Figure 1. Initial studies have focused on understanding the bias conditions and coupling of the back gate to the overlying electrolyte. We have demonstrated that the back gate of SOI-based sensors is coupled to the electrolyte in a complex manner and modulates the top channel thus controlling the device operating point. [1-2]

A sophisticated one-dimensional model of the sensor device has been developed which takes into account Fermi-Dirac statistics, Poisson-Boltzmann, site-binding theory, properties of the electrolyte, and complex coupling present in the test device. A plot of the potential through the device based on this model is shown in Figure 2.

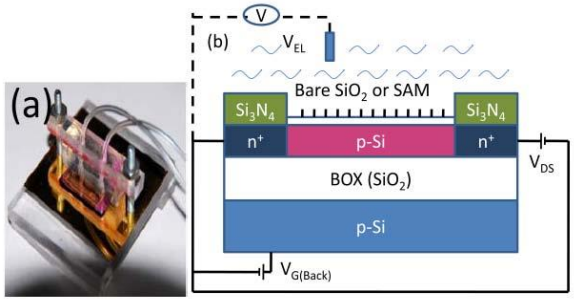


Figure 1: (a) Photograph of sensor chip mounted on microfluidic delivery system (b) Sensor cross-section with measurement circuit.

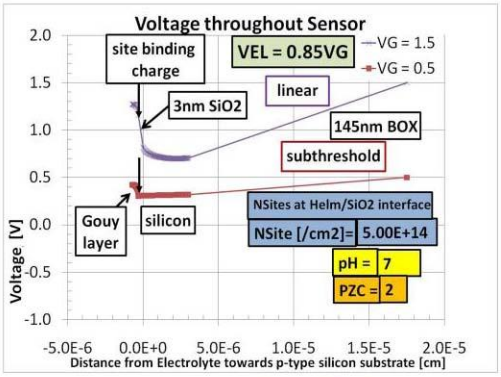


Figure 2: Simulated potential profile from sensor back gate to electrolyte in depletion (subthreshold) and inversion (linear) at 85% coupling.

Further work with 2-D models in TCAD tool Sentaurus has provided additional understanding leading to a preliminary SPICE model responsive to pH sensing.

In the second and third years of this project the focus will move to improving the preliminary SPICE model, extending the current site binding theory to include biological species such as proteins, and consideration of modeling the noise characteristics of the device. Further work will define specifications for support circuitry blocks necessary to form a complete sensing platform, and this will be followed by actual design of support circuitry with interactive feedback for SPICE model improvement.

Keywords: Chemical, Biological, Sensor, SPICE, model.

INDUSTRY INTERACTIONS

Texas Instruments.

MAJOR PAPERS/PATENTS

[1] P. G. Fernandes, et al, "Impact of Back-Gate Biasing on Ultra-thin Silicon-On-Insulator-Based Nanoribbon Sensors," IEEE International SOI Conference, Oct. 2010 (accepted).

[2] P. G. Fernandes, et al, “Effect of Back-Gate Biasing on Floating Electrolytes in Silicon-On-Insulator-Based Nanoribbon Sensors”, (submitted).

CONTACT TxACE

To become a TxACE partner,
please contact:

Kenneth K. O, Director
972-883-5556

To discuss our core facilities in Dallas and how to obtain access to them, please contact:

Eric Vogel, Associate Director
972-883-5556

To receive future TxACE requests for proposals, please contact:

Donna Kuchinski
djk091000@utdallas.edu
972-883-5556

TxACE is based at The University of Texas at Dallas. We are located in the Engineering and Computer Science North building, ECSN 3.302.
Our mailing address is:

Texas Analog Center of Excellence
The University of Texas at Dallas, EC37
800 W Campbell Rd
Richardson, TX 75080

ecs.utdallas.edu/TxACE

SRC

TxACE
TEXAS ANALOG
CENTER OF EXCELLENCE